TJA1046

Dual high-speed CAN transceiver with Standby mode

Rev. 4 — 24 November 2025 Product data sheet

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1 General description

The TJA1046 is a dual high-speed CAN transceiver that provides two interfaces between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN-bus. It is composed of two fully independent TJA1044 transceivers. The transceivers are designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller. The TJA1046 guarantees robust communication at data rates up to 5 Mbit/s as used in, for example, CAN FD networks

The TJA1046 offers a feature set optimized for 12 V automotive applications and excellent ElectroMagnetic Compatibility (EMC) performance.

Additionally, the TJA1046 features:

- Ideal passive behavior to the CAN-bus when the supply voltage is off
- A very low-current Standby mode with bus wake-up capability
- Excellent EMC performance, even without a common mode choke

The HVSON package allows for more than 70 % PCB space saving compared with traditional SO packages. These features make the TJA1046 an excellent choice for networks containing more than one HS-CAN interface requiring a low-power mode with wake-up capability via the CAN-bus, especially for body and gateway control units.

The TJA1046 implements the CAN physical layer as defined in ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5. Additional timing parameters defining loop delay symmetry are specified. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. The TJA1046C features shorter propagation delay, supporting larger network topologies.

2 Features and benefits

2.1 General

- Two fully independent TJA1044 HS-CAN transceivers combined in a single package
- Fully ISO 11898-2:2024, SAE J2284-1 to SAE J2284-5, and SAE J1939-14 compliant[1]
- Very low-current Standby mode with host and bus wake-up capability
- Optimized for use in 12 V automotive systems
- Low electromagnetic emissions and high electromagnetic immunity, tested according to EMC standards IEC-TS62228 and SAE J2962-2:2024[2]
- Leadless HVSON14 package (3.0 mm × 4.5 mm) with improved Automated Optical Inspection (AOI) capability

1 Compliant with the exception of parameters $V_{CM(STEP)}$ and $V_{CM(PP)}$; intended as an indication of emission performance. Note that the device fullfills the EMC requirements, as evidenced through IBEE reports available on request.

2 Verified by an external test house for TJA1046CTK.

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- Can interface with 3.3 V and 5 V-supplied microcontrollers, provided the microcontroller I/Os are 5 V tolerant.
- AEC-Q100 qualified
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- Shorter propagation delay on the TJA1046CTK variant supports larger network topologies (see Table 8)

2.2 Predictable and fail-safe behavior

- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus (high-ohmic) when the supply voltage drops below the switch-off undervoltage threshold
- Transmit Data (TXD) and bus dominant time-out functions
- Internal biasing of TXDx and STBx input pins

2.3 Protection

- High ESD handling capability on the bus pins (8 kV IEC and HBM)
- Bus pins protected against transients in automotive environments
- Undervoltage detection on VCCx pins
- Thermally protected

3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	on pins VCC1 and VCC2	4.5	—	5.5	V
I_{CC}	supply current	per transceiver:				
		Standby mode; $V_{TXDx} = V_{CC}$	—	10	15	µA
		Normal mode				
		recessive; $V_{TXDx} = V_{CC}$	2	5	10	mA
		dominant; V_{TXDx} =0V	20	45	70	mA
		dominant; V_{TXDx} =0 V; short circuit on bus lines; –3V < ($V_{CANH} = V_{CANL}$) < +18 V	2	80	110	mA
$V_{uvd(stb)}$	standby undervoltage detection voltage	on pins VCC1 and VCC2	3.5	4	4.3	V
$V_{uvd(swoff)}$	switch-off undervoltage detection voltage		1.3	2.4	3.4	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 on pins CANH1, CANH2, CANL1 and CANL2	-8	—	+8	kV
V_{CANH}	voltage on pins CANHx	limiting value according to IEC60134	-42	—	+42	V
V_{CANL}	voltage on pin pins CANLx	limiting value according to IEC60134	-42	—	+42	V
T_{vj}	virtual junction temperature		-40	—	+150	°C

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4 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1046TK TJA1046CTK	HVSON14	plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2

5 Block diagram

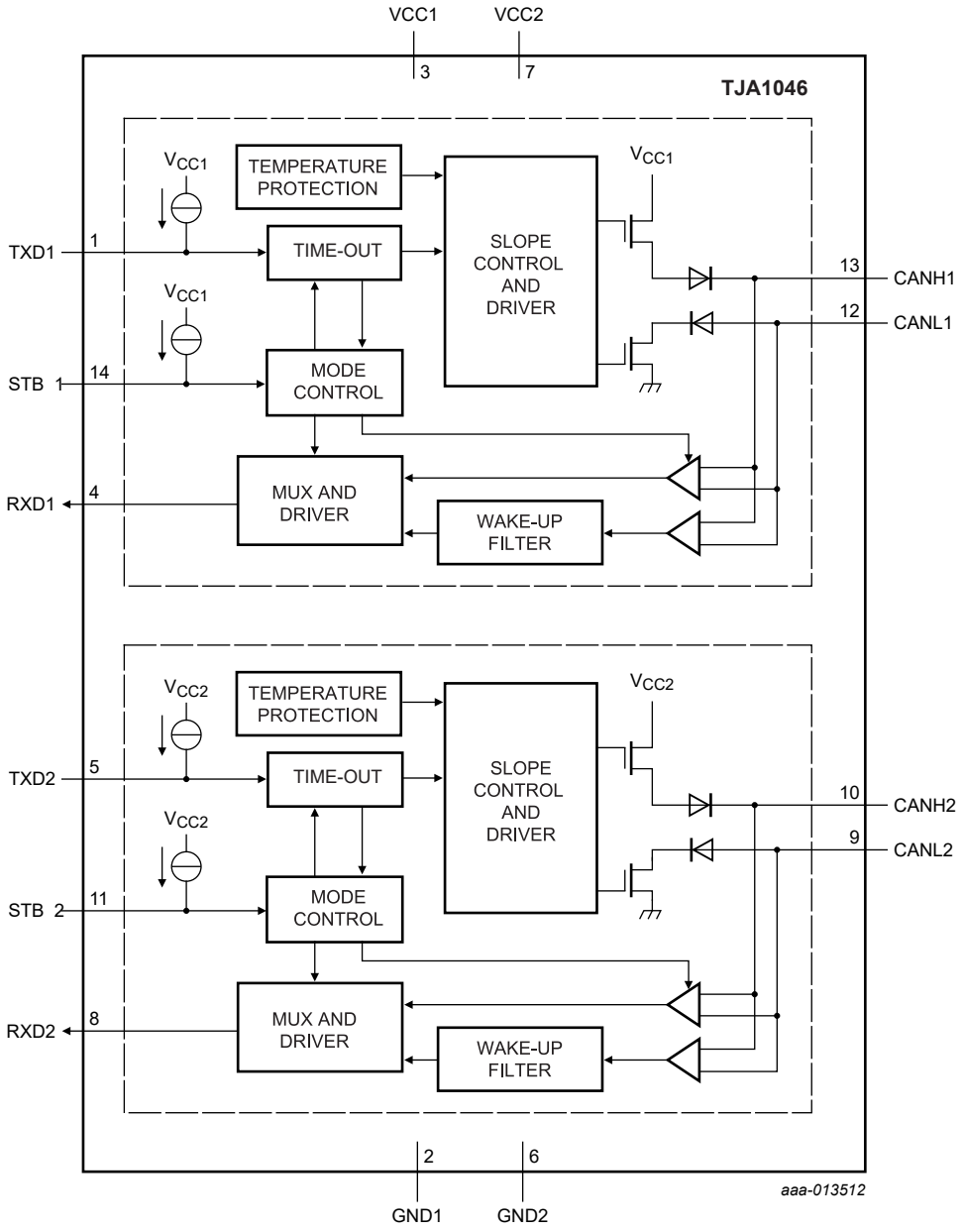


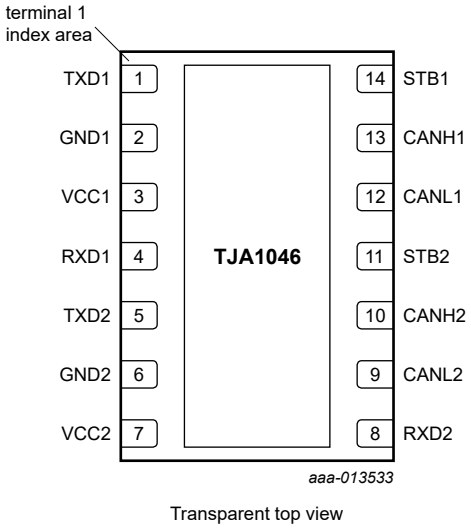
Figure 1. Block diagram

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6 Pinning information

6.1 Pinning



Transparent top view

Figure 2. Pin configuration diagram

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
TXD1	1	I	transmit data input 1
GND1[2]	2	G	transceiver ground 1
VCC1	3	P	transceiver supply voltage 1
RXD1	4	O	receive data output 1; reads out data from the bus lines 1
TXD2	5	I	transmit data input 2
GND2[2]	6	G	transceiver ground 2
VCC2	7	P	transceiver supply voltage 2
RXD2	8	O	receive data output 2; reads out data from the bus lines 2
CANL2	9	AIO	LOW-level CAN-bus line 2
CANH2	10	AIO	HIGH-level CAN-bus line 2
STB2	11	I	Standby mode control input 2
CANL1	12	AIO	LOW-level CAN-bus line 1
CANH1	13	AIO	HIGH-level CAN-bus line 1
STB1	14	I	Standby mode control input 1

[1] Type description
- I: digital input
- O: digital output
- AIO: analog input/output
- P: power supply
- G: ground

[2] HVSON14 package die supply ground is connected to both the GNDx pins and the exposed center pad. The GNDx pins must be connected together externally in the application and soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.

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7 Functional description

7.1 Operating modes

The TJA1046 supports two operating modes per transceiver, Normal and Standby. The operating mode is selected independently for each transceiver via pins STB1 and STB2. See Table 4 for a description of the operating modes under normal supply conditions.

Table 4. Operating modes

Mode	Inputs		Outputs	
	Pin STB1/STB2	Pin TXD1/TXD2	CAN driver	Pin RXD1/RXD2
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Standby	HIGH	x[1]	biased to ground	follows BUS when wake-up detected
				HIGH when no wake-up detected

[1] x = don't care

7.1.1 Normal mode

A LOW level on pin STBx selects Normal mode. In this mode, the enabled transceiver can transmit and receive data via the bus lines CANHx and CANLx (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXDx. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

7.1.2 Standby mode

A HIGH level on pin STBx selects Standby mode. In Standby mode, the enabled transceiver cannot transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a

low-power differential receiver monitors the bus lines for activity.

In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied from V_{CCX} and is able to detect CAN-bus activity. Pin RXDx follows the bus after a wake-up request has been detected. A transition to Normal mode is triggered when STBx is forced LOW.

7.2 Remote wake-up (via the CAN-bus)

The CAN transceivers contain separate wake-up circuits that operate independently of each other. When a dedicated wake-up pattern (specified in ISO 11898-2: 2024) is detected on the bus, the associated transceiver wakes up from Standby mode. This filtering helps avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases generated by noise or spikes on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

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Dominant or recessive bits inserted between these phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$, respectively, are ignored

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 3). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event. Pin RXDx remains HIGH until the wake-up event has been triggered.

After a wake-up sequence has been detected, the transceiver will remain in Standby mode with the bus signals reflected on RXDx. Note that dominant or recessive phases lasting less than $t_{fltr(wake)bus}$ will not be detected by the low-power differential receiver and will not be reflected on RXDx in Standby mode.

A wake-up event is not flagged on RXDx if any of the following events occurs while a valid wake-up pattern is being received:

- The transceiver switches to Normal mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A V_{CC} undervoltage is detected ($V_{CC} < V_{uvd(stb)}$; see Section 7.3.3)

If any of these events occur while a wake sequence is being received, the internal wake-up logic is reset. The complete wake-up sequence will then need to be retransmitted to trigger a wake-up event.

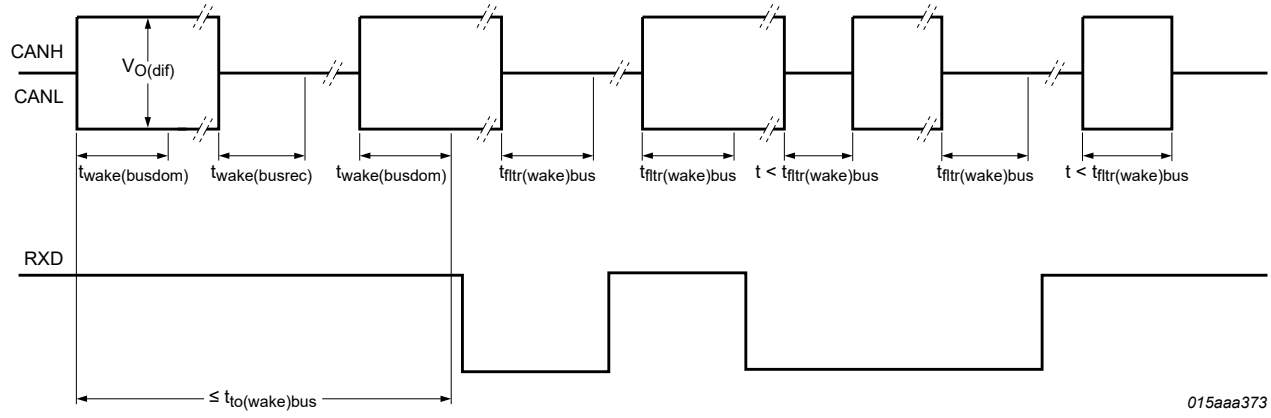


Figure 3. Wake-up timing

7.3 Fail-safe features

7.3.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXDx goes LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXDx is set HIGH.

The TXD dominant time-out time also defines the minimum possible bit rate of approximately 25 kbit/s. Each of the transceivers in the TJA1046 has its own TXD dominant time-out timer. The two timers operate independently of each other.

7.3.2 Internal biasing of TXDx and STBx input pins

Pins TXDx and STBx have internal pull-ups to V_{CCx} to ensure a safe, defined state in case they are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize supply current.

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7.3.3 Undervoltage detection on pins VCCx

The TJA1046 features two fully independent supply voltages. If V_{CCx} drops below the standby undervoltage detection level, $V_{uvd(stb)}$, the transceiver switches to Standby mode. The logic state of pin STBx is ignored until V_{CCx} has recovered. A LOW level on TXDx is also ignored. This precaution prevents the bus being driven dominant while V_{CCx} is recovering. TXDx will continue to be ignored until a HIGH level (bus recessive) is detected.

If V_{CCx} drops below the switch-off undervoltage detection level, $V_{uvd(swoff)}$, the transceiver switches off and disengages from the bus (zero load; bus pins floating) until V_{CCx} has recovered.

Each of the transceivers in the TJA1046 has its own undervoltage protection circuit. The two circuits operate independently of each other.

7.3.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, both output drivers are disabled. When the virtual junction temperature drops below $T_{j(sd)}$ again, the output drivers recover independently once TXDx has been reset to HIGH. Including the TXDx condition prevents output driver oscillation due to small variations in temperature. Each of the transceivers in the TJA1046 has its own temperature protection circuit. The two circuits operate independently of each other.

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8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	on pins CANH1, CANL1, CANH2, CANL2	–42	+42	V
		on pins VCC1, VCC2	–0.3	+7	V
		on any other pin [2]	–0.3	V_{CC} + 0.3	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		–27	+27	V
V_{trt}	transient voltage	on pins CANH1, CANL1, CANH2, CANL2 [3]			
		pulse 1	–100	—	V
		pulse 2a	—	75	V
		pulse 3a	–150	—	V
		pulse 3b	—	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω) [4]			
		on pins CANH1, CANL1, CANH2, CANL2	–8	+8	kV
		SAE J2962-2:2024 (330 pF, 2 kΩ) on pins CANH, CANL [5]			
		powered air discharge	–15	+15	kV
		powered contact discharge	–8	++8	kV
		Human Body Model (HBM); 100 pF, 1.5 kΩ			
		on any pin [6]	–4	+4	kV
		on pins CANH1, CANL1, CANH2, CANL2 [7]	–8	+8	kV
		Machine Model (MM); 200 pF, 0.75 µH, 10 Ω [8]			
		on any pin	–200	+200	V
		Charged Device Model (CDM); field Induced charge; 4 pF [9]			
		on corner pins	–750	+750	V
		on any other pin	–500	+500	V
T_{vj}	virtual junction temperature	[10]	–40	+150	°C
T_{stg}	storage temperature	[11]	–55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
[2] Maximum voltage should never exceed 7 V.
[3] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637.
[4] Verified by an external test house according to IEC TS 62228, Section 4.
[5] Verified by an external test house according to ISO 10605 for TJA1046CTK.
[6] According to AEC-Q100-002.
[7] Pins stressed to reference group containing all ground and supply pins, emulating the application circuits (Figure 5). HBM pulse as specified in AEC-Q100-002 used.
[8] According to AEC-Q100-003.
[9] According to AEC-Q100-011.
[10] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
[11] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

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9 Thermal characteristics

Table 6. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HVSON14 package	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case[2]		9	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		3	K/W

[1] According to JEDEC JESD51-2, JESD51-5, and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm).

[2] Case temperature refers to the center of the heatsink at the bottom of the package.

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10 Static characteristics

Table 7. Static characteristics

T_{vj} = –40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; R_L = 60 Ω; C_L = 100 pF unless specified otherwise; All voltages are defined with respect to ground. Positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pins VCC1 and VCC2						
V_{CC}	supply voltage		4.5	—	5.5	V
$V_{uvd(stb)}$	standby undervoltage detection voltage	[2]	3.5	4	4.3	V
$V_{uvd(swoff)}$	switch-off undervoltage detection voltage	[2]	1.3	2.4	3.4	V
I_{CC}	supply current	per transceiver:				
		Standby mode; $V_{TXDx} = V_{CC}$	—	10	15	µA
		Normal mode				
		recessive; $V_{TXDx} = V_{CC}$	2	5	10	mA
		dominant; V_{TXDx} =0V	20	45	70	mA
		dominant; V_{TXDx} =0 V; short circuit on bus lines; –3V < ($V_{CANH} = V_{CANL}$) < +18 V	2	80	110	mA
Standby mode control input; pins STB1 and STB2						
V_{IH}	HIGH-level input voltage		2	—	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	—	0.8	V
I_{IH}	HIGH-level input current	per transceiver; $V_{STBx} = V_{CC}$	–1	—	+1	µA
I_{IL}	LOW-level input current	per transceiver; V_{STBx} =0V	–15	—	–1	µA
CAN transmit data input; pins TXD1 and TXD2						
V_{IH}	HIGH-level input voltage		2	—	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	—	0.8	V
I_{IH}	HIGH-level input current	per transceiver; $V_{TXDx} = V_{CCx}$	–5	—	+5	µA
I_{IL}	LOW-level input current	per transceiver; V_{TXDx} =0V	–260	–150	–70	µA
C_i	input capacitance	[3]	—	5	10	pF
CAN receive data output; pins RXD1 and RXD2						
I_{OH}	HIGH-level output current	per transceiver; $V_{RXDx} = V_{CCx}$ – 0.4 V	–8	–3	–1	mA
I_{OL}	LOW-level output current	per transceiver; V_{RXDx} = 0.4 V; bus dominant	1	—	12	mA
Bus lines; pins CANH1, CANL1, CANH2 and CANL2						
$V_{O(dom)}$	dominant output voltage	VTXDx =0 V; t< tto(dom)TXD				
		pin CANHx; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANLx; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V

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Table 7. Static characteristics...*continued*

T_{vj} = –40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; R_L = 60 Ω; C_L = 100 pF unless specified otherwise; All voltages are defined with respect to ground. Positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym} = V_{CCx} – V_{CANHx} – V_{CANLx}$	–400	—	+400	mV
V_{TXsym}	transmitter voltage symmetry	VTXsym = VCANHx + VCANLx; f_{TXD} = 250 kHz, 1 MHz and 2.5 MHz; C_{SPLIT} = 4.7 nF [3] [4]	$0.9V_{CC}$	—	$1.1V_{CC}$	V
$V_{O(dif)}$	differential output voltage	dominant; Normal mode; VTXDx =0 V; t< tto(dom)TXD				
		R_L = 50 Ω to 65 Ω	1.5	—	3	V
		R_L = 45 Ω to 70 Ω	1.4	—	3.3	V
		R_L = 2240 Ω	1.5	—	5	V
		recessive; no load				
		Normal mode: $V_{TXDx} = V_{CCx}$	–50	—	+50	mV
		Standby mode	–0.2	—	+0.2	V
$V_{O(rec)}$	recessive output voltage	Normal mode; $V_{TXDx} = V_{CC}$; no load	2	$0.5V_{CC}$	3	V
		Standby mode; no load	–0.1	—	+0.1	V
$V_{th(RX)dif}$	differential receiver threshold voltage	–12 V ≤ V_{CANLx} ≤ +12 V; –12 V ≤ V_{CANHx} ≤ +12 V				
		Normal mode	0.5	—	0.9	V
		Standby mode	0.4	—	1.15	V
$V_{rec(RX)}$	receiver recessive voltage	–12 V ≤ V_{CANL} ≤ +12 V; –12 V ≤ V_{CANH} ≤ +12 V				
		Normal mode	–4	—	0.5	V
		Standby mode	–4	—	0.4	V
$V_{dom(RX)}$	receiver dominant voltage	–12 V ≤ V_{CANL} ≤ +12 V; –12 V ≤ V_{CANH} ≤ +12 V				
		Normal mode	0.9	—	9.0	V
		Standby mode	1.15	—	9.0	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	–12 V ≤ V_{CANL} ≤ +12 V; –12 V ≤ V_{CANH} ≤ +12 V; Normal mode	50	—	300	mV
$I_{O(sc)dom}$	dominant short-circuit output current	per transceiver; V_{TXDx} =0 V; t< tto(dom)TXD; V_{CC} =5 V				
		pin CANHx; V_{CANHx} = –15 V to +40 V	–100	–70	–40	mA
		pin CANLx; V_{CANLx} = –15 V to +40 V	40	70	100	mA
$I_{O(sc)rec}$	recessive short-circuit output current	per transceiver; Normal mode; $V_{CANHx} = V_{CANLx}$ = –27 V to +32 V; $V_{TXDx} = V_{CC}$	–5	—	+5	mA
I_L	leakage current	per transceiver; V_{CC} = 0 V or V_{CC} shorted to GND via 47 kΩ; $V_{CANHx} = V_{CANLx}$ =5V	–5	—	+5	µA

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Table 7. Static characteristics...*continued*

T_{vj} = –40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; R_L = 60 Ω; C_L = 100 pF unless specified otherwise; All voltages are defined with respect to ground. Positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_i	input resistance	–2V ≤ V_{CANL} ≤ +7 V; –2V ≤ V_{CANH} ≤ +7 V [3]	9	15	28	kΩ
ΔR_i	input resistance deviation	0V ≤ V_{CANL} ≤ +5 V; 0V ≤ V_{CANH} ≤ +5 V [3]	–3	—	+3	%
$R_{i(dif)}$	differential input resistance	–2V ≤ V_{CANL} ≤ +7 V; –2V ≤ V_{CANH} ≤ +7 V [3]	19	30	52	kΩ
C_i	input capacitance	[3]	—	—	20	pF
$C_{i(dif)}$	differential input capacitance	[3]	—	—	10	pF
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature	[3]	—	185	—	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.
[2] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.
[3] Not tested in production; guaranteed by design.
[4] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 7.

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11 Dynamic characteristics

Table 8. Dynamic characteristics

T_{vj} = –40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; R_L = 60 Ω; C_L = 100 pF unless specified otherwise. All voltages are defined with respect to ground. All values are specified per transceiver.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH1, CANH2, CANL1, CANL2, TXD1, TXD2, RXD1 and RXD2; see Figure 4 and Figure 6						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	TJA1046CTK; Normal mode	—	62	90	ns
		TJA1046TK; Normal mode	—	65	105	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	TJA1046CTK; Normal mode	—	75	90	ns
		TJA1046TK; Normal mode		90	105	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	TJA1046CTK; Normal mode	—	60	100	ns
		TJA1046TK; Normal mode		60	115	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	TJA1046CTK; Normal mode	—	90	110	ns
		TJA1046TK; Normal mode	—	65	135	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	TJA1046CTK; Normal mode	50	—	195	ns
		TJA1046TK; Normal mode	50	—	210	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	TJA1046CTK, Normal mode	50	—	195	ns
		TJA1046TK; Normal mode	50	—	210	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set B (tbit(TXD) ≥ 200 ns, up to 5 Mbit/s); see Figure 4 and Figure 6						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	–45	—	+10	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	–80	—	+20	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	–45	—	+15	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set A ($t_{bit(TXD)}$ ≥ 500 ns, up to 2 Mbit/s); see Figure 4 and Figure 6						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	–65	—	+30	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	–100	—	+50	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	–65	—	+40	ns
Dominant time-out time						
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXDx} = 0 V; Normal mode [2]	0.8	3	6.5	ms
Mode transitions						
$t_{d(stb-norm)}$	standby to normal mode delay time	[3]	7	25	47	µs
Bus wake-up timing; pins CANH1, CANH2, CANL1, and CANL2; see Figure 3						
$t_{wake(busdom)}$	bus dominant wake-up time	Standby mode [4]	0.5	—	3	µs
$t_{wake(busrec)}$	bus recessive wake-up time	Standby mode [4]	0.5	—	3	µs
$t_{to(wake)bus}$	bus wake-up time-out time	Standby mode [3]	0.8	3	6.5	ms
$t_{fltr(wake)bus}$	bus wake-up filter time	Standby mode [5]	0.5	1	3	µs

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

[3] Standby-to-Normal mode transition occurs between the min and max values. It is guaranteed not to occur below the min value; it is guaranteed to occur above the max value.

[4] A dominant/recessive phase shorter than the min value is guaranteed not be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.

[5] Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.

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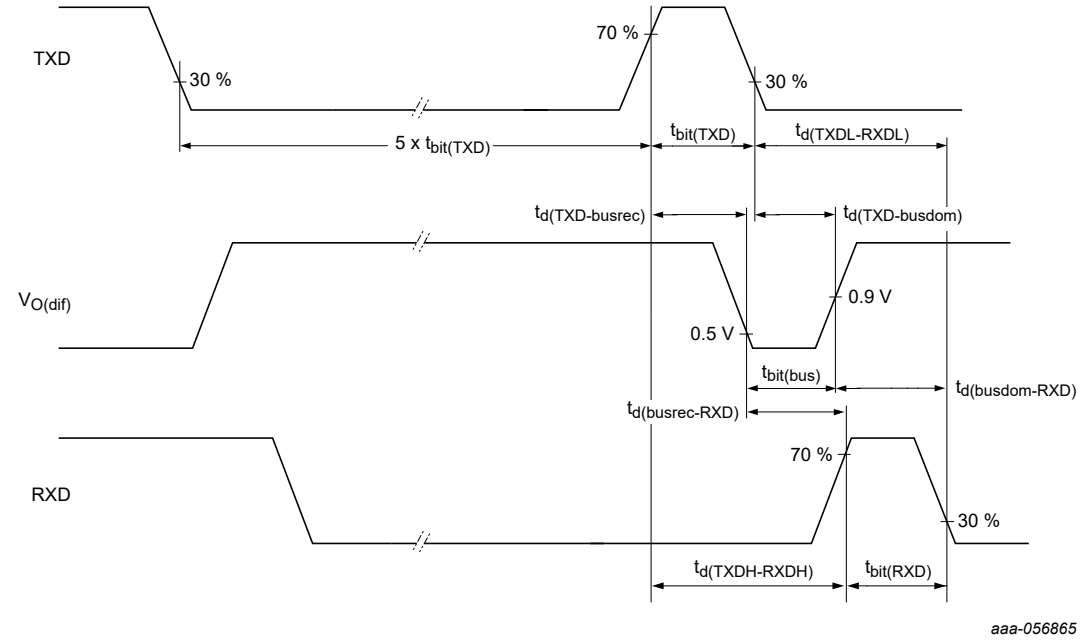


Figure 4. CAN transceiver timing diagram according to ISO 11898-2:2024

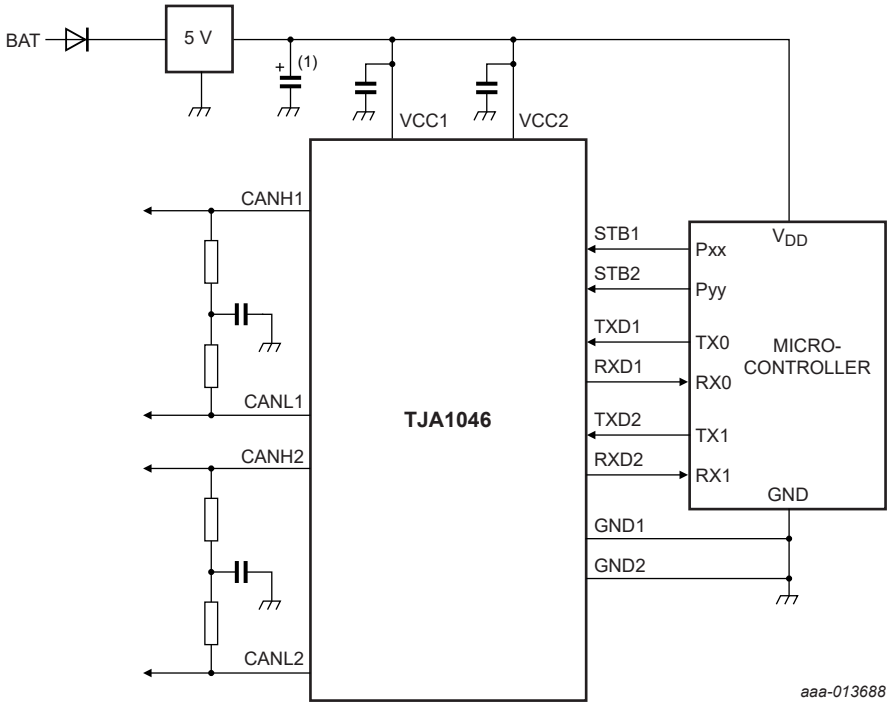
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12 Application information

The minimum external circuitry needed with the TJA1046 is shown in Figure 5. See the Application Hints (Section 12.2) for further information about external components and PCB layout requirements.

12.1 Application diagram



(1) Optional, depends on regulator

Figure 5. Typical application with a 5 V microcontroller

12.2 Application hints

Further information on the application of the TJA1046 can be found in NXP AH1308 *Application Hints - Standalone high speed CAN transceivers Mantis TJA1044/TJA1057 and Dual-Mantis TJA1046*.

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13 Test information

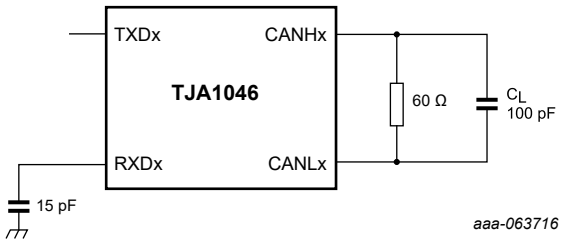


Figure 6. CAN transceiver timing test circuit

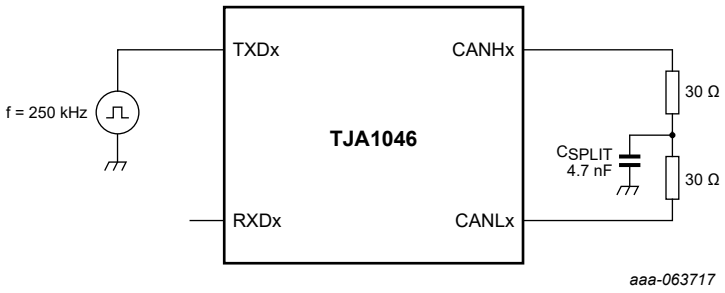


Figure 7. Test circuit for measuring transceiver driver symmetry

14 Quality information

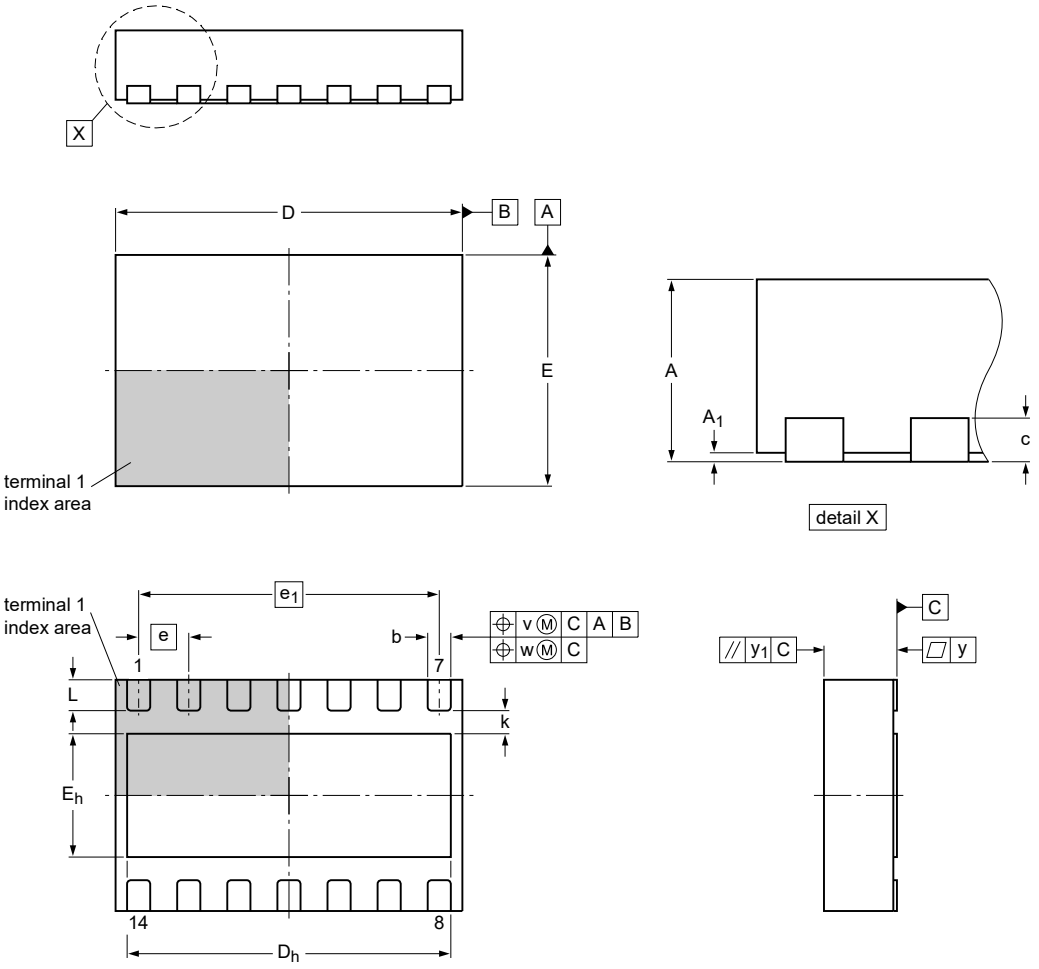
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

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15 Package outline

HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
	max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
mm	nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Figure 8. Package outline SOT1086-2 (HVSON14)

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16 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in JESD625-A or equivalent standards.

17 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 9) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and Table 10

Table 9. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering. See Figure 9.

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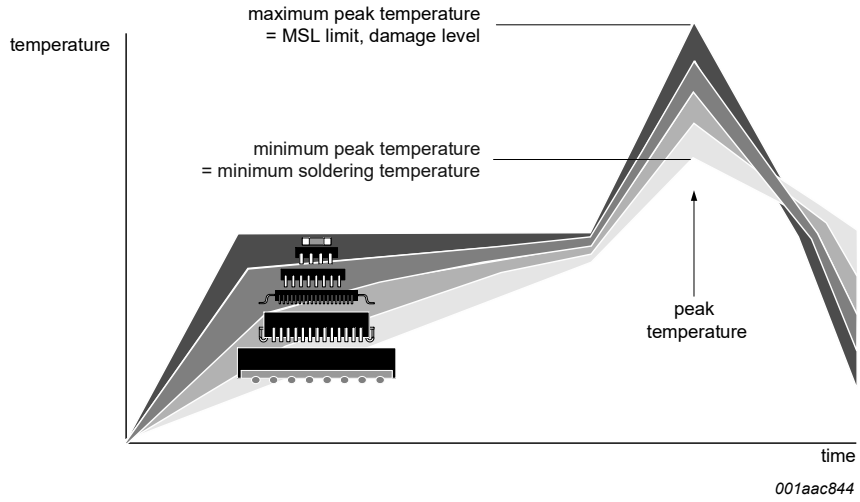


Figure 9. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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18 Appendix: ISO 11898-2:2024 parameter cross-reference lists

Table 11. ISO 11898-2:2024 to NXP data sheet parameter conversion[1]

ISO 11898-2:2024		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating			
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)}$	short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	$R_{DIFF_pas_rec}$	$R_{i(dif)}$	differential input resistance
Single-ended internal resistance	$R_{SE_pas_rec_H}$ $R_{SE_pas_rec_L}$	R_i	input resistance
Matching of internal resistance	m_R	ΔR_i	input resistance deviation
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA driver symmetry			
Driver symmetry	V_{sym_vcc}	V_{TXsym}	transmitter voltage symmetry
Optional HS-PMA transmit dominant time-out			
Transmit dominant time-out	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time

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Table 11. ISO 11898-2:2024 to NXP data sheet parameter conversion[1] *...continued*

ISO 11898-2:2024		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA implementation loop delay requirements for parameter sets A, B and C			
Loop delay for parameter sets A and B	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
Loop delay for parameter set C		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Propagation delay from TXD to CAN_H/CAN_L for parameter set C	$t_{prop(TXD_BUS)}$	$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant
		$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive
Propagation delay from CAN_H/CAN_L to RXD for parameter set C	$t_{prop(BUS_RXD)}$	$t_{d(busdom-RXD)}$	delay time from bus dominent to RXD
		$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD
HS-PMA implementation data signal timing requirements for parameter sets A, B and C			
Transmitted recessive bit width variation	$t_{\Delta Bit(Bus)}$	$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation
Received recessive bit width variation	$t_{\Delta Bit(RXD)}$	$\Delta t_{bit(RXD)}$	received recessive bit width deviation
Receiver timing symmetry	$t_{\Delta REC}$	Δt_{rec}	receiver timing symmetry
HS-PMA implementation SIC timing and impedance for parameter set C			
Differential internal resistance (CAN_H to CAN_L)	$R_{DIFF_act_rec}$	$R_{i(dif)actrec}$	active recessive phase differential input resistance
Internal single-ended resistance	$R_{SE_act_rec}$	$R_{i(actrec)}$	active recessive phase input resistance
Start time of active signal improvement phase	$t_{act_rec_start}$	$t_{d(TXD-busactrec)start}$	delay time from TXD to bus active recessive start
End time of active signal improvement phase	$t_{act_rec_end}$	$t_{d(TXD-busactrec)end}$	delay time from TXD to bus active recessive end
Start time of passive recessive phase	$t_{pas_rec_start}$	$t_{d(TXD-buspasrec)start}$	delay time from TXD to bus passive recessive start
PMA voltage wake-up control timing			
CAN activity filter time, long/short	t_{Filter}	$t_{wake(busdom)}$ $t_{wake(busrec)}$	bus dominant wake-up time bus recessive wake-up time
Wake-up time-out	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up pattern signaling	t_{Flag}	$t_{startup(RXD)}$	RXD start-up time
		$t_{startup(INH)}$	INH start-up time
		$t_{startup(ERR_N)}$	ERR_N start-up time
Number of recessive bits before next SOF			
Number of recessive bits before a new SOF shall be accepted	n_{Bits_idle}	$N_{bit(idle)}$	number of idle bits before a SOF is accepted
BitFilter in CAN FD data phase			
CAN FD data phase bitfilter (option 1)	$\rho_{Bitfilter_option1}$	$t_{fltr(bit)dom}$	dominant bit filter time
CAN FD data phase bitfilter (option 2)	$\rho_{Bitfilter_option2}$		
HS-PMA bus biasing control timing			
Time-out for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time
Bus bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	bus bias reaction time

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[1] A number of proprietary NXP parameters are equivalent to parameters defined in ISO 11898-2:2024, but use different symbols. This conversion table allows ISO parameters to be cross-referenced with their NXP counterparts. The NXP parameters are defined in the Static and Dynamic characteristics tables. The conversion table provides a comprehensive listing - individual devices may not include all parameters.

19 Revision history

Table 12. Revision history

Document ID	Release date	Description
TJA1046 v.4	24 November 2025	• Added variant TJA1046CTK with shorter propagation delay • ISO 11898-2:2024 compliance – Changed ISO 11898-2:2016 to ISO 11898-2:2024 throughout – Table 8: formatting of CAN (FD) timings revised – Section 18: cross-reference table updated • Table 1, Table 7, and Table 8: VCC range extended from 4.75 V to 5.25 V (±5 %) to 4.5 V to 5.5 V (±10 %) • Section 2.1 – SAE J1939-14 compliance added – EMC compliance updated – Statement on TJA1046CTK shorter propagation delay added • Section 2.2: Updated text describing supply undervoltage behavior • Table 1: Parameter $V_{uvs(swoff)}$ added • Table 3: Added Type column and related footnotes • Table 5 – Reformatted V_{ESD} section, added/changed footnotes – SAE J2962-2:2024 VESD entries added • Table 6: reformatted, addition of parameters $R_{th(j-c)}$ and Ψ_{j-top} • Table 7: added footnote 2 • Table 8: added footnotes • Original Figures 4 and 5 combined in new single Figure 4 • Revised Figure 6 and Figure 7 • Legal information: disclaimers updated
TJA1046 v.3	06 September 2017	—
TJA1046 v.2.01	23 May 2016	—
TJA1046 v.1	28 May 2015	• Initial version

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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