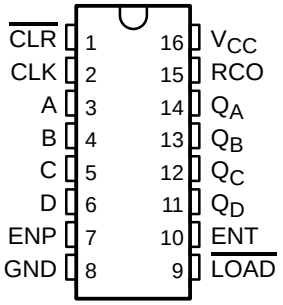
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**

**CD54AC163 . . . F PACKAGE**
**CD74AC163 . . . E OR M PACKAGE**
**(TOP VIEW)**




## description/ordering information

The ’AC163 devices are 4-bit binary counters. These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change, coincident with each other, when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

The counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. Presetting is synchronous; therefore, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function is synchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{CLR}$ to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15, with $Q_A$ high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These devices feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –55°C to 125°C | PDIP – E | Tube | CD74AC163E | CD74AC163E |
| | SOIC – M | Tube | CD74AC163M | AC163M |
| | | Tape and reel | CD74AC163M96 | |
| | CDIP – F | Tube | CD54AC163F3A | CD54AC163F3A |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

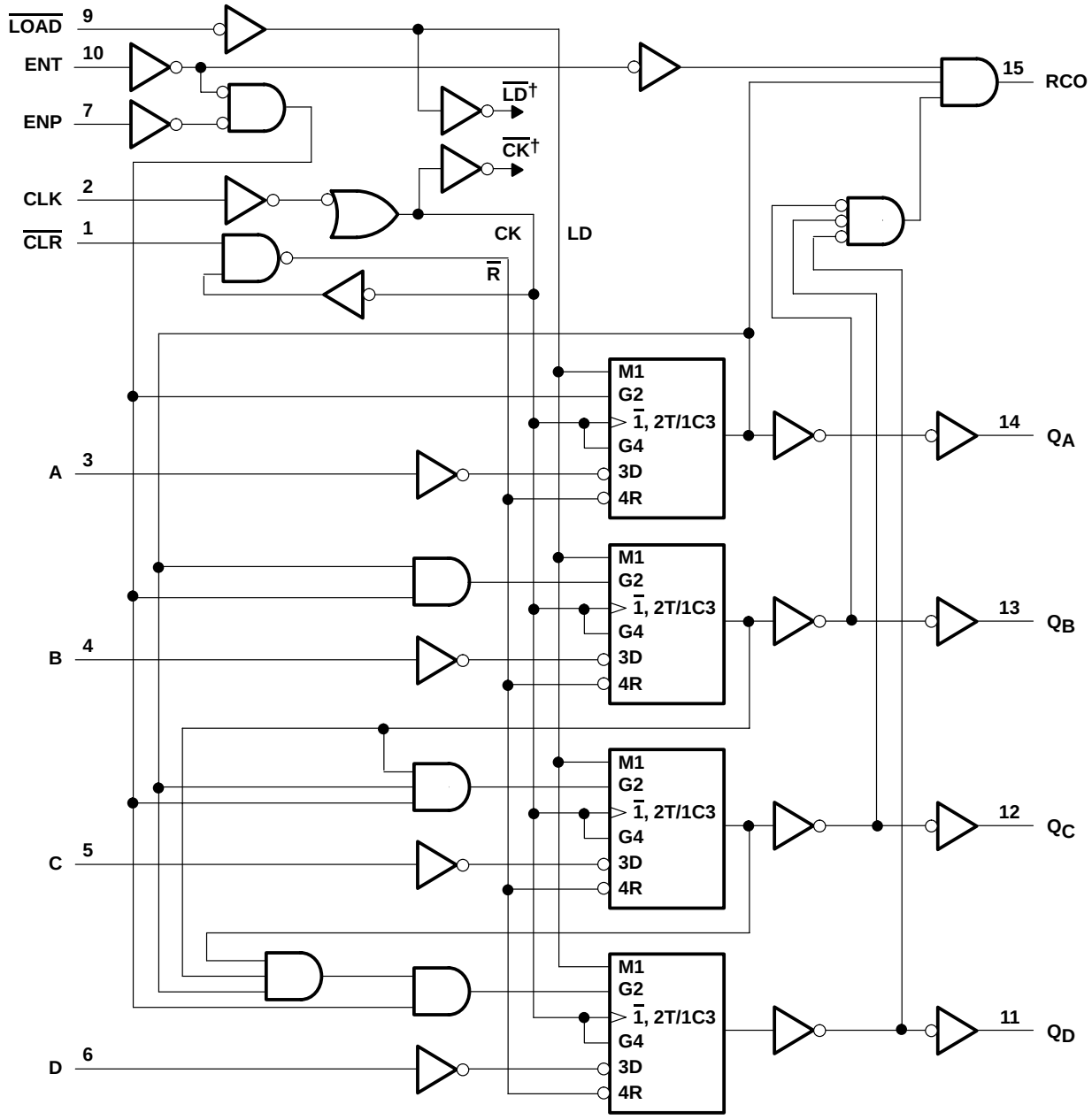
**FUNCTION TABLE**

| INPUTS | | | | | | OUTPUTS | | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | ENP | ENT | $\overline{LOAD}$ | A,B,C,D | $Q_n$ | RCO | |
| L | ↑ | X | X | X | X | L | L | Reset (clear) |
| h | ↑ | X | X | l | l | L | L | Parallel load |
| h | ↑ | X | X | l | h | H | Note 1 | |
| h | ↑ | h | h | h | X | Count | Note 1 | Count |
| h | X | l | X | h | X | $q_n$ | Note 1 | Inhibit |
| h | X | X | l | h | X | $q_n$ | L | |

H = high level, L = low level, X = don't care, h = high level one setup time prior to the CLK low-to-high transition, l = low level one setup time prior to the CLK low-to-high transition, q = the state of the referenced output prior to the CLK low-to-high transition, and ↑ = CLK low-to-high transition.

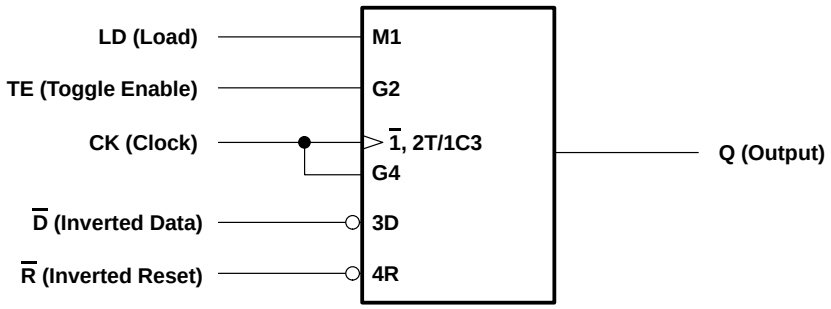
NOTE 1: The RCO output is high when ENT is high and the counter is at terminal count (HHHH).

## logic diagram (positive logic)

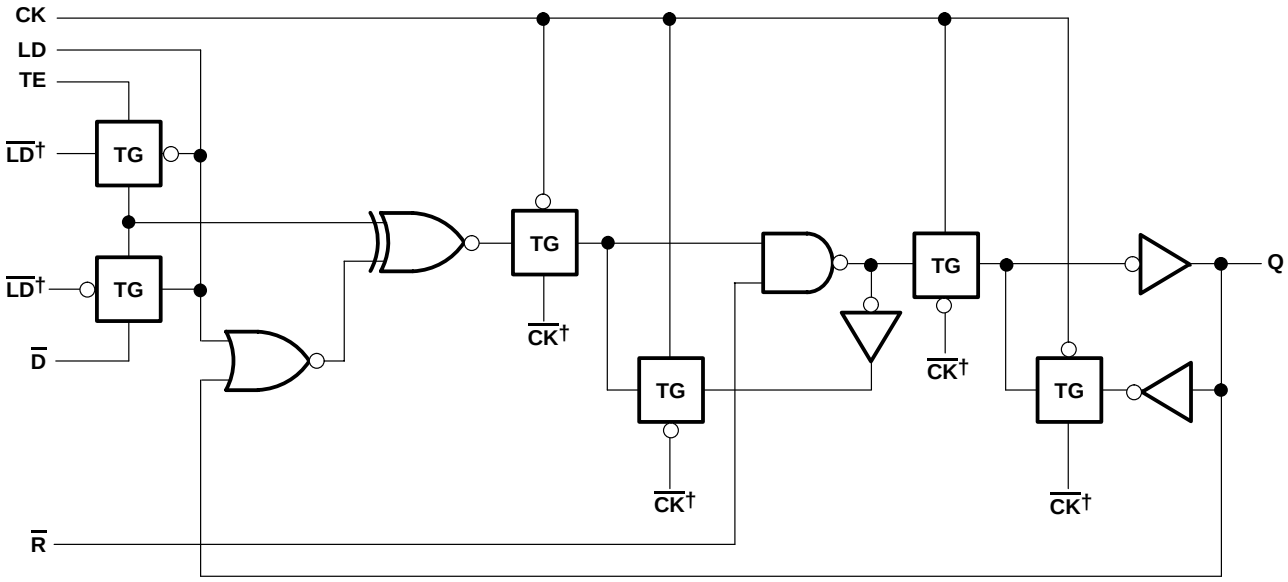



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

## logic symbol, each D/T flip-flop




## logic diagram, each D/T flip-flop (positive logic)

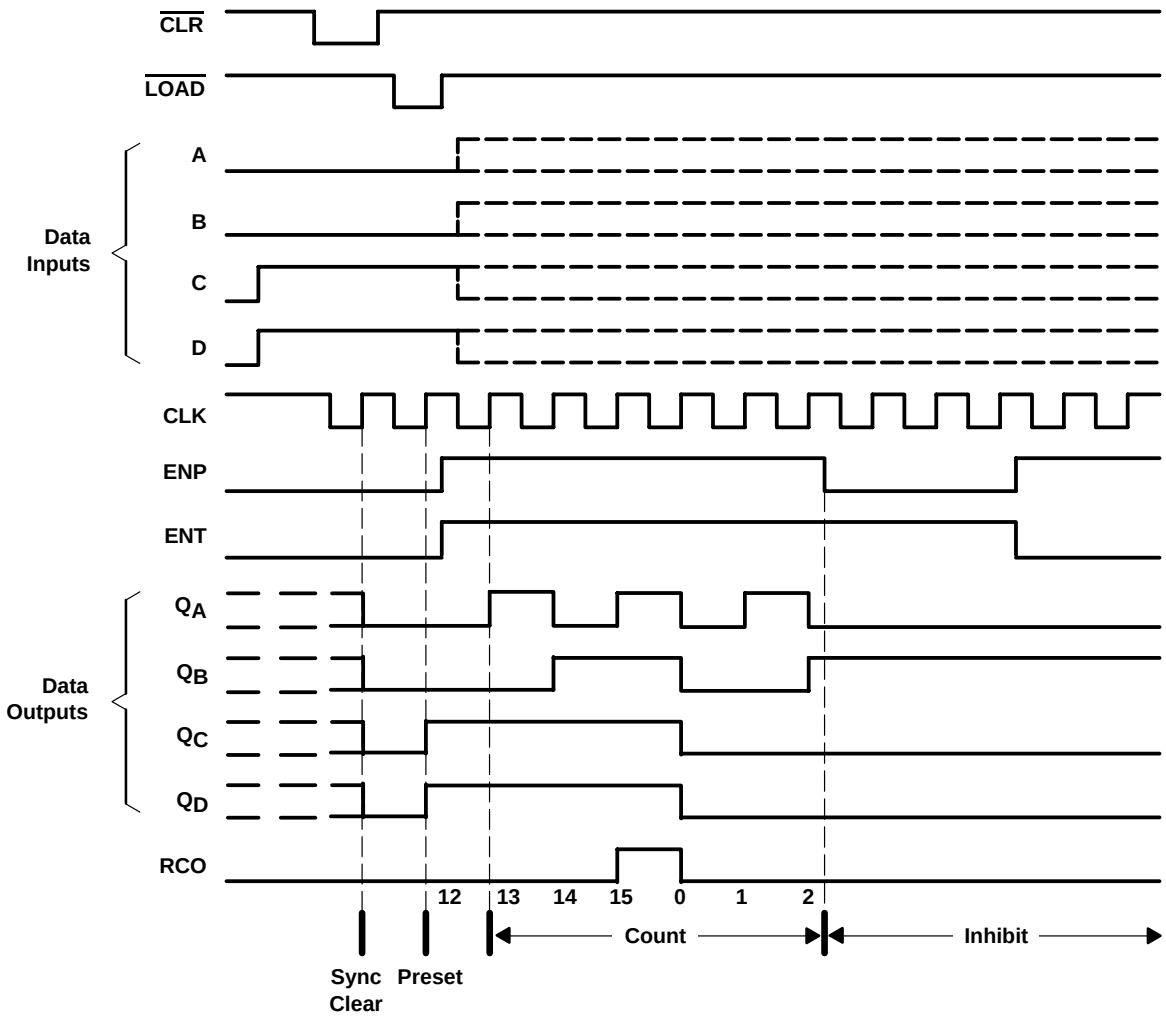



† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

### typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 6 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 2) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): E package . . . . . 67°C/W
M package . . . . . 73°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4)

| | | | $T_A$ = 25°C | | –55°C to 125°C | | –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 1.5 | 5.5 | 1.5 | 5.5 | 1.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.5 V | 1.2 | | 1.2 | | 1.2 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.5 V | | 0.3 | | 0.3 | | 0.3 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | –24 | | –24 | | –24 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 1.5 V to 3 V | | 50 | | 50 | | 50 | ns |
| | | $V_{CC}$ = 3.6 V to 5.5 V | | 20 | | 20 | | 20 | |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | –55°C to 125°C | | –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –50 μA | 1.5 V | 1.4 | | 1.4 | | 1.4 | | V |
| | | | 3 V | 2.9 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | 2.4 | | 2.48 | | |
| | | $I_{OH}$ = –24 mA | 4.5 V | 3.94 | | 3.7 | | 3.8 | | |
| | | $I_{OH}$ = –50 mA† | 5.5 V | – | | 3.85 | | – | | |
| | | $I_{OH}$ = –75 mA† | 5.5 V | – | | – | | 3.85 | | |
| $V_{OL}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 1.5 V | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 12 mA | 3 V | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 50 mA† | 5.5 V | | – | | 1.65 | | – | |
| | | $I_{OL}$ = 75 mA† | 5.5 V | | – | | – | | 1.65 | |
| $I_I$ | $V_I = V_{CC}$ or GND | | 5.5 V | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | 8 | | 160 | | 80 | μA |
| $C_i$ | | | | | 10 | | 10 | | 10 | pF |

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | | $V_{CC}$ | –55°C to 125°C | | –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 1.5 V | | 7 | | 8 | MHz |
| | | | 3.3 V ± 0.3 V | | 64 | | 73 | |
| | | | 5 V ± 0.5 V | | 90 | | 103 | |
| $t_w$ | Pulse duration | CLK high or low | 1.5 V | 69 | | 61 | | ns |
| | | | 3.3 V ± 0.3 V | 7.7 | | 6.8 | | |
| | | | 5 V ± 0.5 V | 5.5 | | 4.8 | | |
| $t_{su}$ | Setup time, before CLK↑ | A, B, C, or D | 1.5 V | 63 | | 55 | | ns |
| | | | 3.3 V ± 0.3 V | 7 | | 6.1 | | |
| | | | 5 V ± 0.5 V | 5 | | 4.4 | | |
| | | ENP or ENT | 1.5 V | 63 | | 55 | | |
| | | | 3.3 V ± 0.3 V | 9.6 | | 8.2 | | |
| | | | 5 V ± 0.5 V | 5 | | 4.4 | | |
| | | $\overline{LOAD}$ low | 1.5 V | 75 | | 66 | | |
| | | | 3.3 V ± 0.3 V | 8.4 | | 7.4 | | |
| | | | 5 V ± 0.5 V | 6 | | 5.3 | | |
| | | $\overline{CLR}$ inactive | 1.5 V | 75 | | 66 | | |
| | | | 3.3 V ± 0.3 V | 8.4 | | 7.4 | | |
| | | | 5 V ± 0.5 V | 6 | | 5.3 | | |
| $t_h$ | Hold time, after CLK↑ | A, B, C, or D | 1.5 V | 0 | | 0 | | ns |
| | | | 3.3 V ± 0.3 V | 0 | | 0 | | |
| | | | 5 V ± 0.5 V | 0 | | 0 | | |
| | | ENP or ENT | 1.5 V | 0 | | 0 | | |
| | | | 3.3 V ± 0.3 V | 0 | | 0 | | |
| | | | 5 V ± 0.5 V | 0 | | 0 | | |
| | | $\overline{LOAD}$ low | 1.5 V | 0 | | 0 | | |
| | | | 3.3 V ± 0.3 V | 0 | | 0 | | |
| | | | 5 V ± 0.5 V | 0 | | 0 | | |
| | | $\overline{CLR}$ inactive | 1.5 V | 0 | | 0 | | |
| | | | 3.3 V ± 0.3 V | 0 | | 0 | | |
| | | | 5 V ± 0.5 V | 0 | | 0 | | |

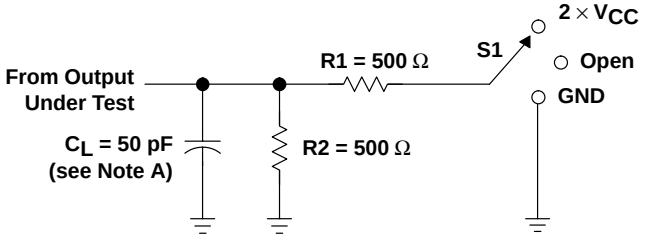
**switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | –55°C to 125°C | | –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 1.5 V | 7 | | 8 | | MHz |
| | | | 3.3 V ± 0.3 V | 64 | | 73 | | |
| | | | 5 V ± 0.5 V | 90 | | 103 | | |
| $t_{pd}$ | CLK | RCO | 1.5 V | – | 209 | – | 190 | ns |
| | | | 3.3 V ± 0.3 V | 6 | 23.4 | 6 | 21 | |
| | | | 5 V ± 0.5 V | 4.3 | 16.7 | 4.3 | 15.2 | |
| | | Any Q | 1.5 V | – | 207 | – | 188 | |
| | | | 3.3 V ± 0.3 V | 5.9 | 23.1 | 5.9 | 21 | |
| | | | 5 V ± 0.5 V | 4.2 | 16.5 | 4.2 | 15 | |
| | ENT | RCO | 1.5 V | – | 129 | – | 117 | |
| | | | 3.3 V ± 0.3 V | 3.6 | 14.4 | 3.7 | 13.1 | |
| | | | 5 V ± 0.5 V | 2.6 | 10.3 | 2.7 | 9.4 | |

**operating characteristics, $T_A$ = 25°C**

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load | 66 | pF |

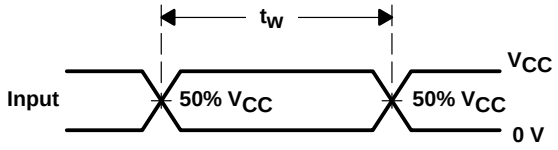
## PARAMETER MEASUREMENT INFORMATION



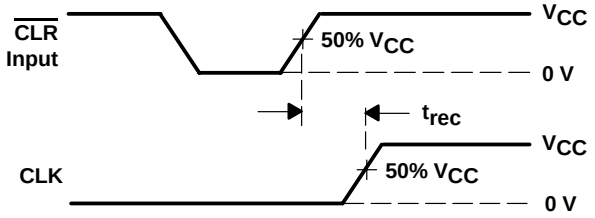

NOTE: When $V_{CC}$ = 1.5 V, R1 and R2 = 1 kΩ.

**LOAD CIRCUIT**

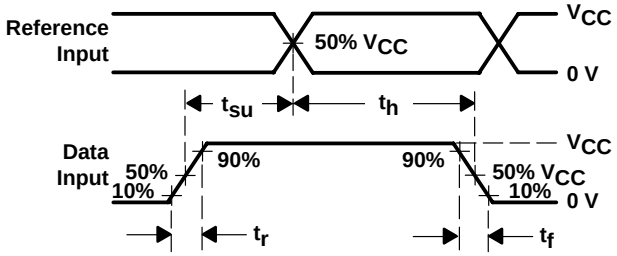
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



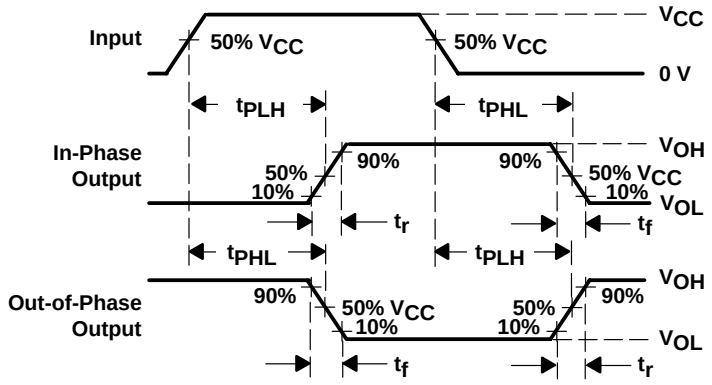

**VOLTAGE WAVEFORMS**
**PULSE DURATION**



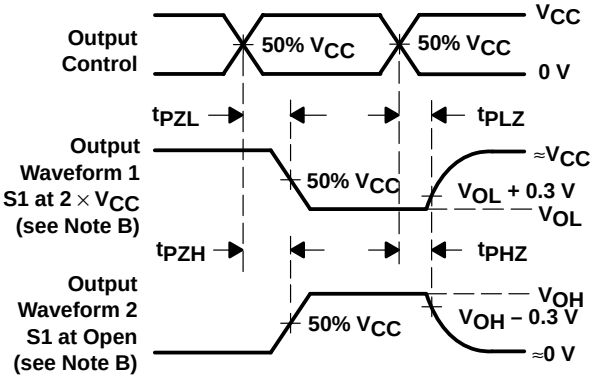

**VOLTAGE WAVEFORMS**
**RECOVERY TIME**




**VOLTAGE WAVEFORMS**
**SETUP AND HOLD AND INPUT RISE AND FALL TIMES**




**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY AND OUTPUT TRANSITION TIMES**




**VOLTAGE WAVEFORMS**
**OUTPUT ENABLE AND DISABLE TIMES**

NOTES:
A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, $f_{max}$ is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
G. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
H. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
I. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CD54AC163F3A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54AC163F3A |
| CD54AC163F3A.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54AC163F3A |
| CD74AC163E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74AC163E |
| CD74AC163E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74AC163E |
| CD74AC163M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | AC163M |
| CD74AC163M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC163M |
| CD74AC163M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC163M |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54AC163, CD74AC163 :**

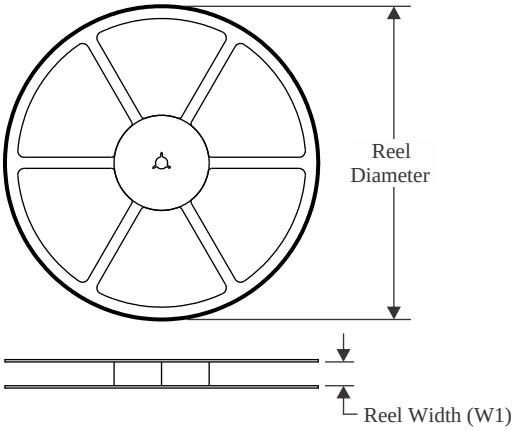
- Catalog : CD74AC163
- Military : CD54AC163

NOTE: Qualified Version Definitions:

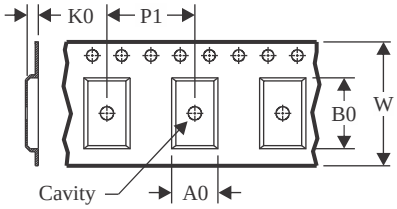
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

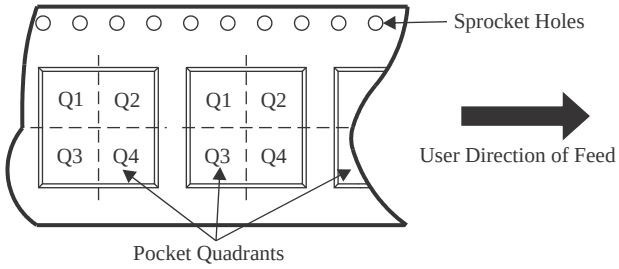



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

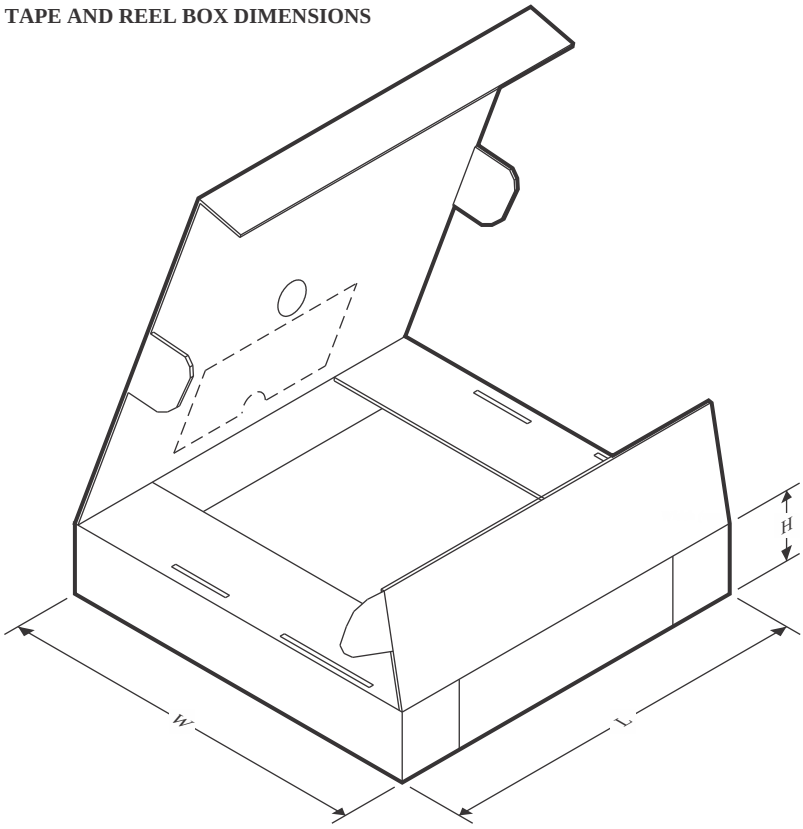
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74AC163M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

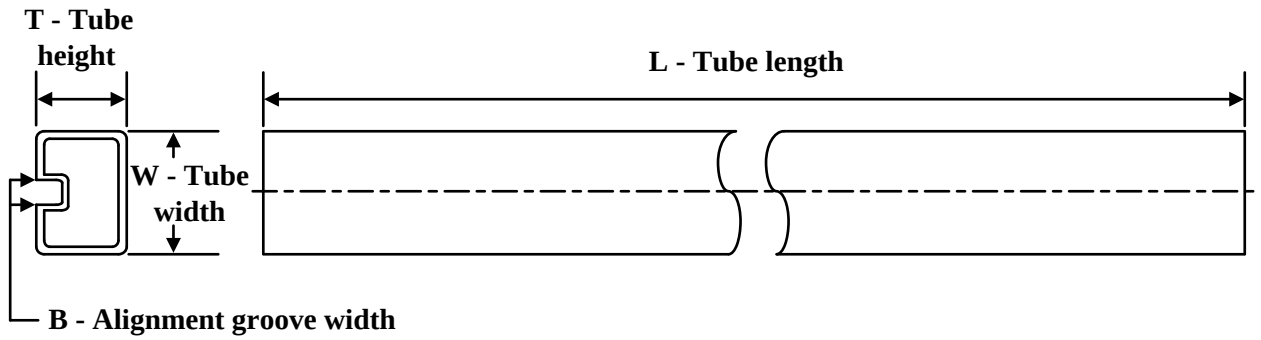
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74AC163M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |

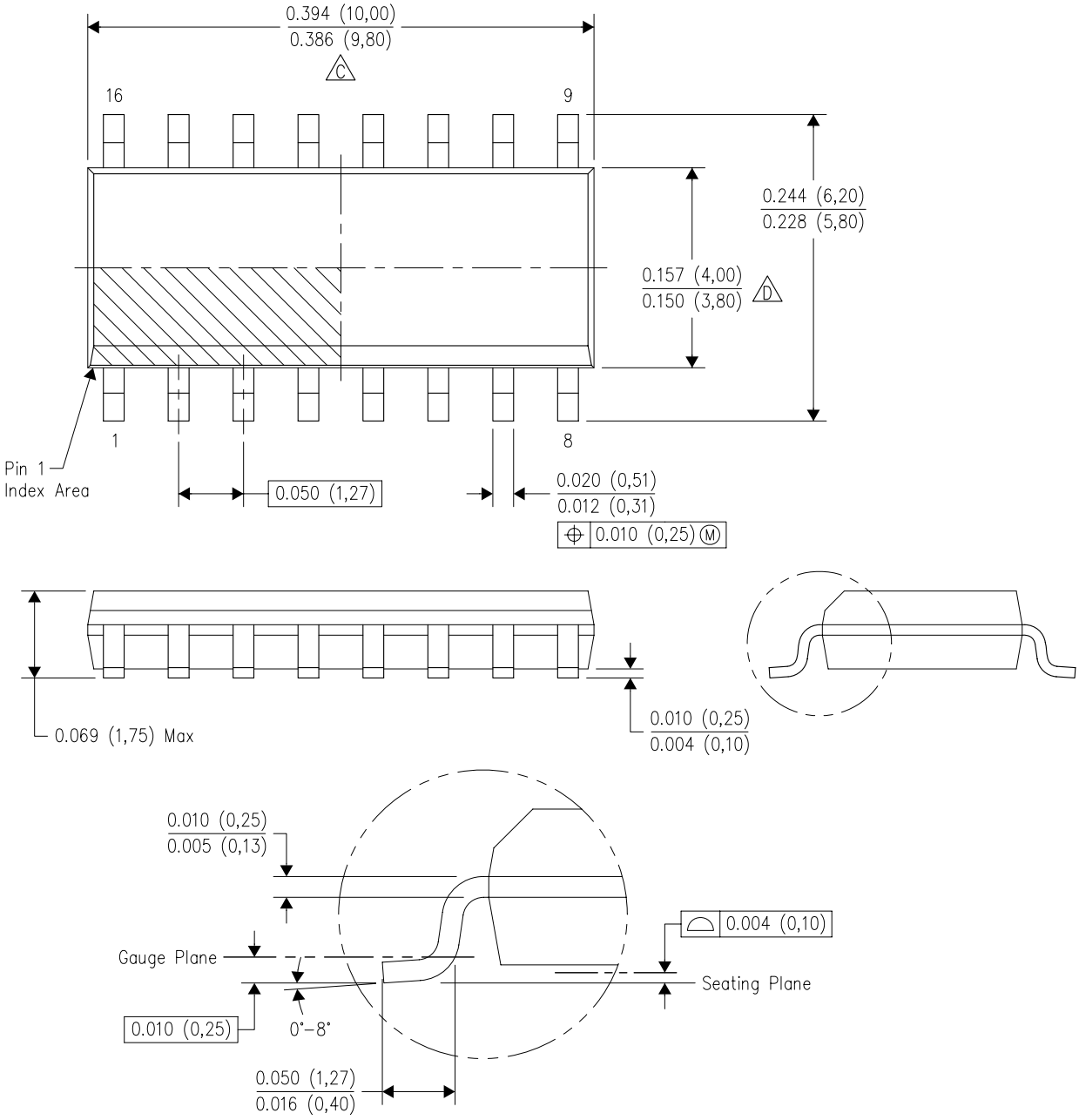
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74AC163E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC163E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC163E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC163E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

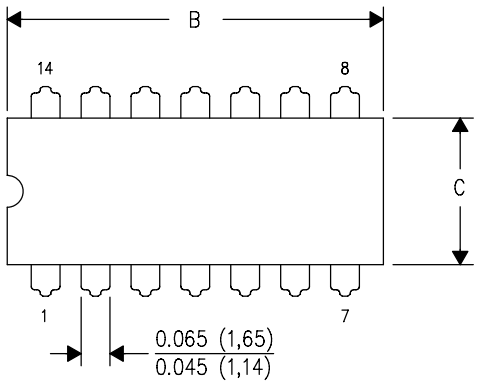



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

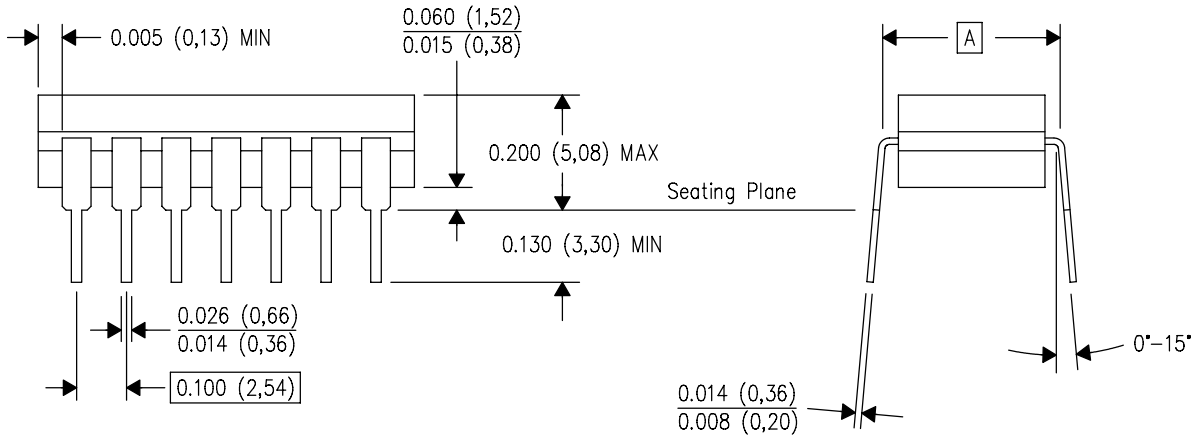
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



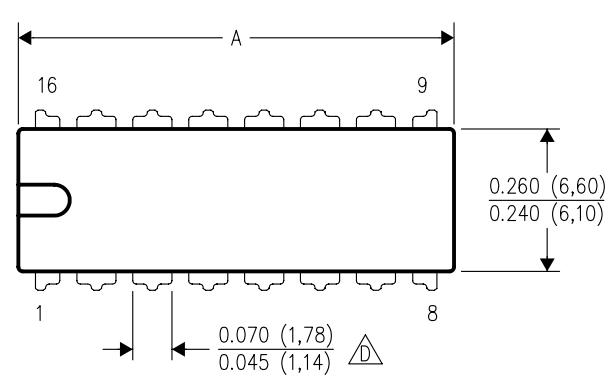

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

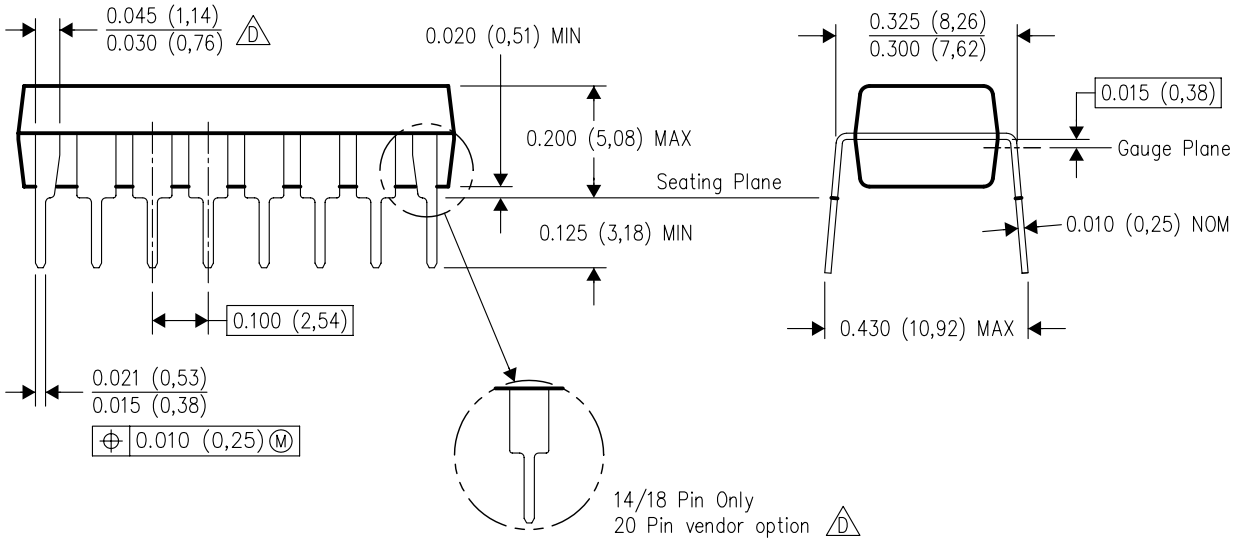
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Last updated 10/2025