SNx4HC4020 14 位异步二进制计数器

1 特性

- 2V 至 6V 的宽工作电压范围
- 输出可驱动多达 10 个 LSTTL 负载
- 低功耗，I_{CC} 最大值为 80μA
- t_{pd} 典型值 = 12ns
- ±4mA 输出驱动（在 5 V 时）
- 低输出电流，最大值 1μA

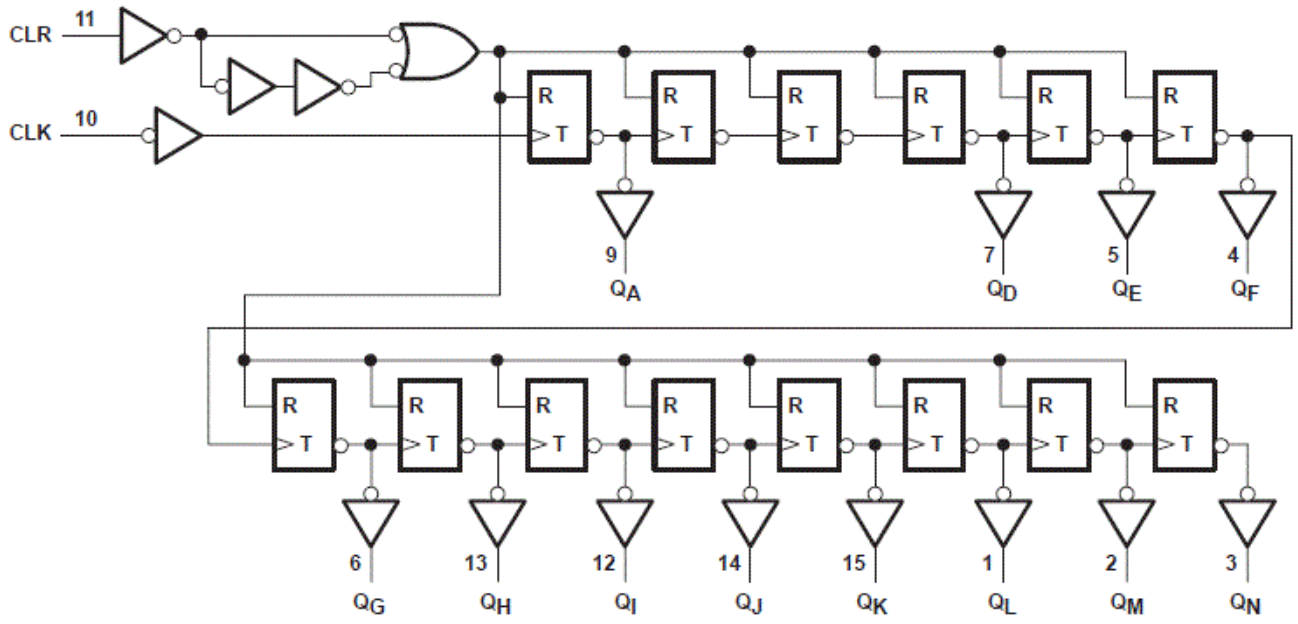
2 说明

’HC4020 器件是 14 级纹波进位二进制计数器，会在时钟脉冲的负边沿触发一次计数。当清零 (CLR) 输入变为高电平时，计数器将独立于时钟 (CLK) 输入复位为零（所有输出为低电平）。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
SN74HC4020D	SOIC (16)	9.90mm × 3.90mm
SN74HC4020N	PDIP (16)	19.31mm × 6.35mm
SN74HC4020NS	SO (16)	6.20mm × 5.30mm
SN74HC4020PW	TSSOP (16)	5.00mm × 4.40mm
SN54HC4020J	CDIP (16)	24.38mm × 6.92mm
SNJ54HC4020FK	LCCC (20)	8.89mm × 8.45mm
SNJ54HC4020W	CFP (16)	10.16mm × 6.73mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

功能方框图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Table of Contents

1 特性 1
2 说明 1
3 Revision History 2
4 Pin Configuration and Functions 3
5 Specifications 4
5.1 Absolute Maximum Ratings 4
5.2 Recommended Operating Conditions(1) 4
5.3 Thermal Information 4
5.4 Electrical Characteristics 5
5.5 Timing Characteristics 5
5.6 Switching Characteristics 6
5.7 Operating Characteristics 6
6 Parameter Measurement Information 7
7 Detailed Description 8
7.1 Overview 8
7.2 Functional Block Diagram 8
7.3 Device Functional Modes 8
8 Power Supply Recommendations 9
9 Layout 9
9.1 Layout Guidelines 9
10 Device and Documentation Support 10
10.1 Documentation Support 10
10.2 接收文档更新通知 10
10.3 支持资源 10
10.4 Trademarks 10
10.5 Electrostatic Discharge Caution 10
10.6 术语表 10
11 Mechanical, Packaging, and Orderable Information 10

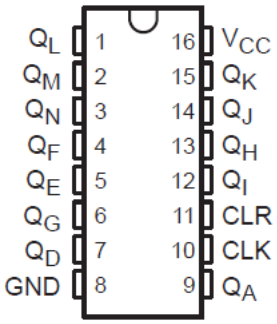
3 Revision History

注：以前版本的页码可能与当前版本的页码不同

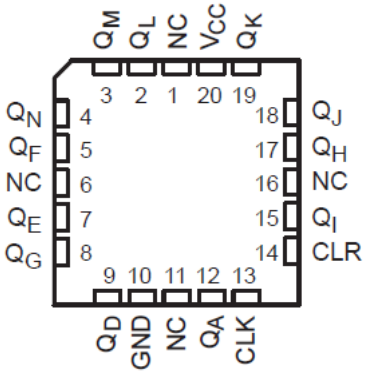
Changes from Revision E (September 2003) to Revision F (February 2022)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准	1

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4 Pin Configuration and Functions



J, W, D, DB, N, NS, or PW Package
16-Pin CDIP, CFP, SOIC, SSOP, PDIP, SO, or TSSOP
Top View



NC – No internal connection

FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input clamp current(2)	(V_I < 0 or V_I > V_{CC})		±20	mA
I_{OK}	Output clamp current(2)	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions(1)

			SN54HC4020			SN74HC4020			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		-55		125	-40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC		D (SOIC) 16 PINS	DB (SSOP) 16 PINS	N (PDIP) 16 PINS	NS (SO) 16 PINS	PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	73	82	67	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

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5.4 Electrical Characteristics

over recommended operating free-air temperature range (unelss otherwise noted)

PARAMETER		TEST CONDITIONS(1)	V_{CC} (V)	T_A = 25°C			SN54HC4020		SN74HC4020		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 20 μA	2	1.9	1.998		1.9		1.9		V
			4.5	4.4	4.499		4.4		4.4		
			6	5.9	5.999		5.9		5.9		
		I_{OH} = – 4 mA	4.5	3.98	4.3		3.7		3.84		
		I_{OH} = – 5.2 mA	6	5.48	5.8		5.2		5.34		
V_{OL}	Low-level output voltage	I_{OL} = 20 μA	2		0.002	0.1		0.1		0.1	V
			4.5		0.001	0.1		0.1		0.1	
			6		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6		0.15	0.26		0.4		0.33	
I_I	Input hold current	V_I = V_{CC} or 0	6		±0.1	±100		±1000		±1000	nA
I_{CC}	Supply current	V_I = V_{CC} or 0. I_O = 0	6			8		160		80	μA
C_i	Input capacitance		2 to 6		3	10		10		10	pF

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} (V)	T_A = 25°C		SN54HC4020		SN74HC4020		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{CLK}	Clock frequency		2		5.5		3.7		4.3	MHz
			4.5		28		19		22	
			6		33		22		25	
t_W	Pulse duration	CLK high or low	2	90		135		115		ns
			4.5	18		27		23		
			6	15		23		20		
		CLR high	2	70		105		90		
			4.5	14		21		18		
			6	12		18		25		
t_{su}	Setup time, CLR inactive before CLK ↓		2	60		90		75		ns
			4.5	12		18		15		
			6	10		15		13		

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5.6 Switching Characteristics

C_L = 50 pF. See Parameter Measurement Information

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	T_A = 25°C			SN54HC4020		SN74HC4020		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2	5.5	10		3.7		4.3		ns
			4.5	28	45		19		22		
			6	33	53		22		25		
t_{pd}	CLK	Q_A	2		62	150		225		190	ns
			4.5		16	30		45		38	
			6		12	26		38		32	
t_{PHL}	CLR	Any	2		63	140		210		175	ns
			4.5		17	28		42		35	
			6		13	24		36		30	
t_t		Any	2		28	75		110		95	ns
			4.5		8	15		22		19	
			6		6	13		19		16	

5.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	88	pF

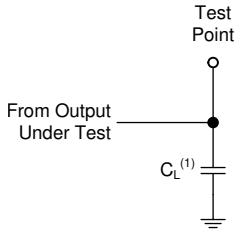
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6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

图 6-1. Load Circuit for Push-Pull Outputs

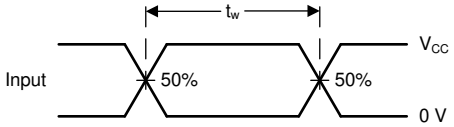


图 6-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

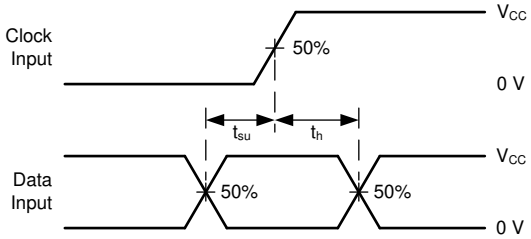
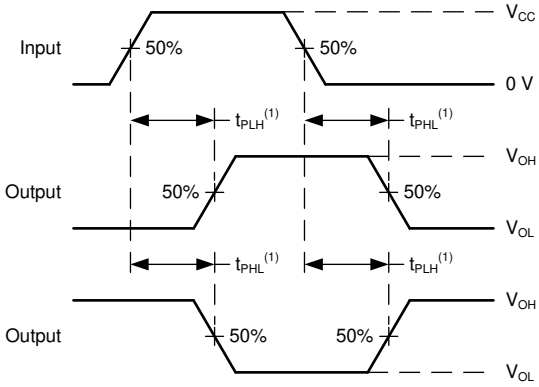
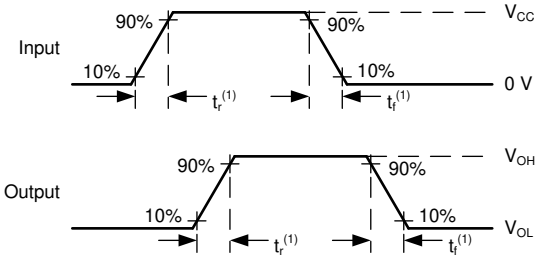


图 6-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

图 6-4. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t.

图 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs

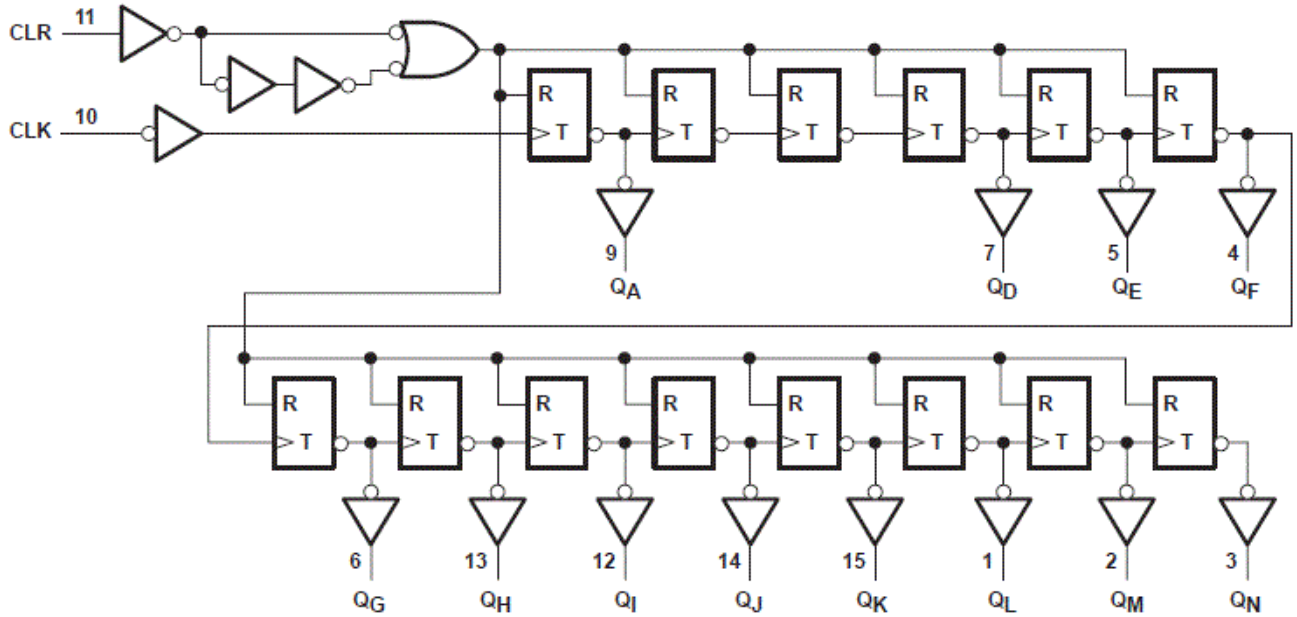
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7 Detailed Description

7.1 Overview

The ’HC4020 devices are 14-stage binary ripple-carry counters that advance on the negative-going edge of the clock pulse. The counters are reset to zero (all outputs low) independently of the clock (CLR) input when the clear (CLR) input goes high.

7.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

图 7-1. Functional Block Diagram

7.3 Device Functional Modes

Function Table
(each buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

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8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
85003012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85003012A SNJ54HC 4020FK
8500301EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301EA SNJ54HC4020J
8500301FA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301FA SNJ54HC4020W
SN54HC4020J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC4020J
SN54HC4020J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC4020J
SN74HC4020D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	HC4020
SN74HC4020DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC4020N
SN74HC4020N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC4020N
SN74HC4020NSR	NRND	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020NSR.A	NRND	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	HC4020
SN74HC4020PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4020
SN74HC4020PWT	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	HC4020
SNJ54HC4020FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85003012A SNJ54HC 4020FK
SNJ54HC4020FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85003012A SNJ54HC 4020FK
SNJ54HC4020J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301EA SNJ54HC4020J
SNJ54HC4020J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301EA SNJ54HC4020J

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54HC4020W	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301FA SNJ54HC4020W
SNJ54HC4020W.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301FA SNJ54HC4020W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC4020, SN74HC4020 :

- Catalog : SN74HC4020

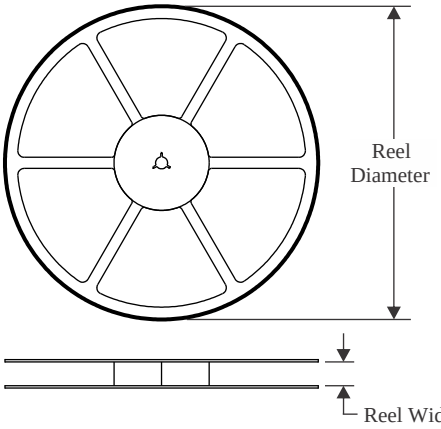
- Military : SN54HC4020

NOTE: Qualified Version Definitions:

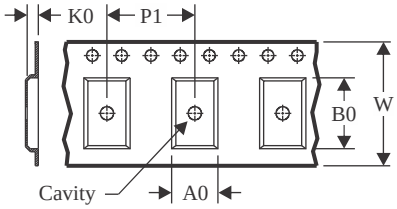
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

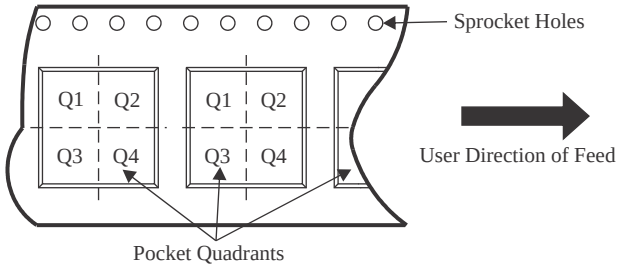


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

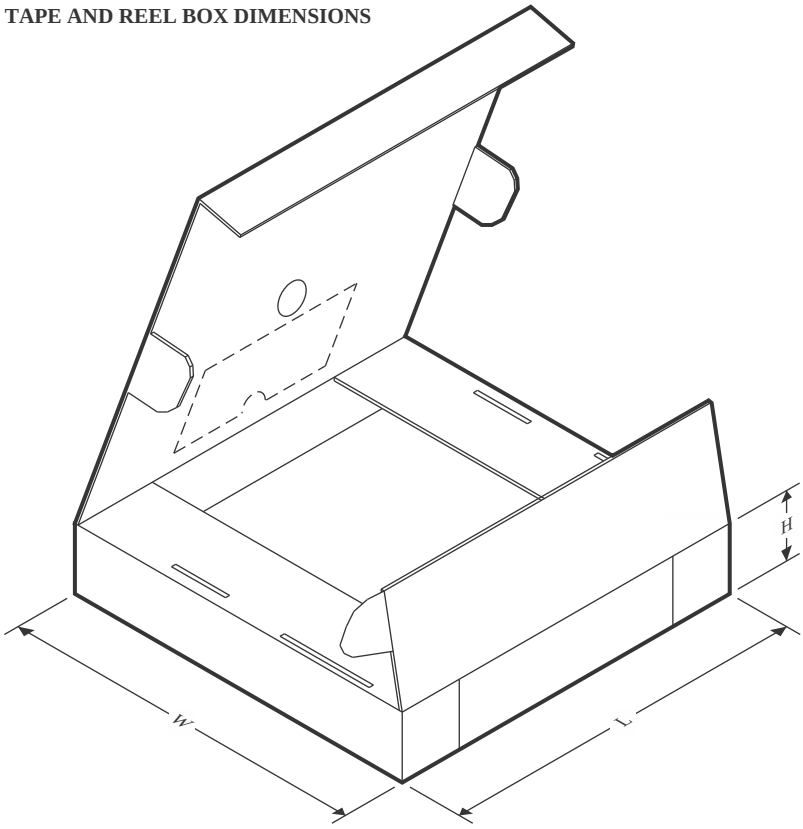
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4020DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4020NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HC4020PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4020PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4020PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
SN74HC4020PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4020PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4020PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

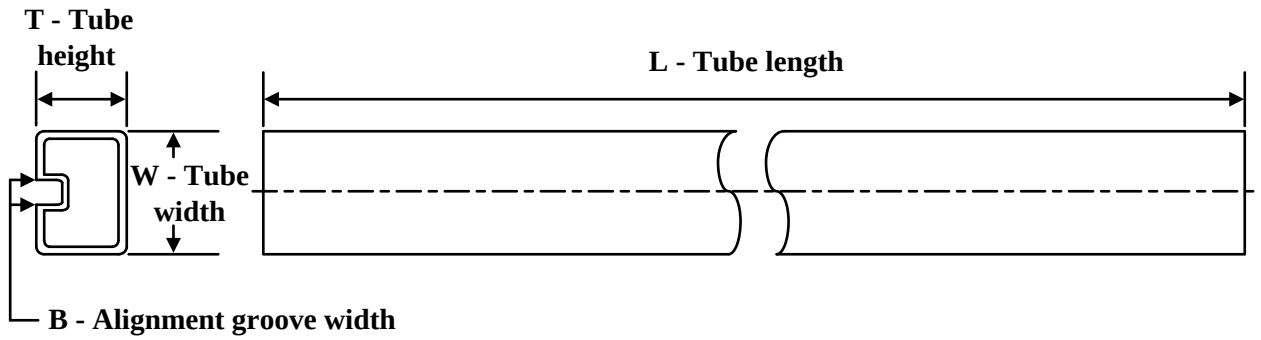
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

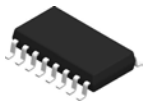
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4020DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC4020NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74HC4020PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74HC4020PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74HC4020PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74HC4020PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC4020PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC4020PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
85003012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8500301FA	W	CFP	16	25	506.98	26.16	6220	NA
SN74HC4020N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4020N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4020N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4020N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC4020FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC4020FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC4020W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54HC4020W.A	W	CFP	16	25	506.98	26.16	6220	NA

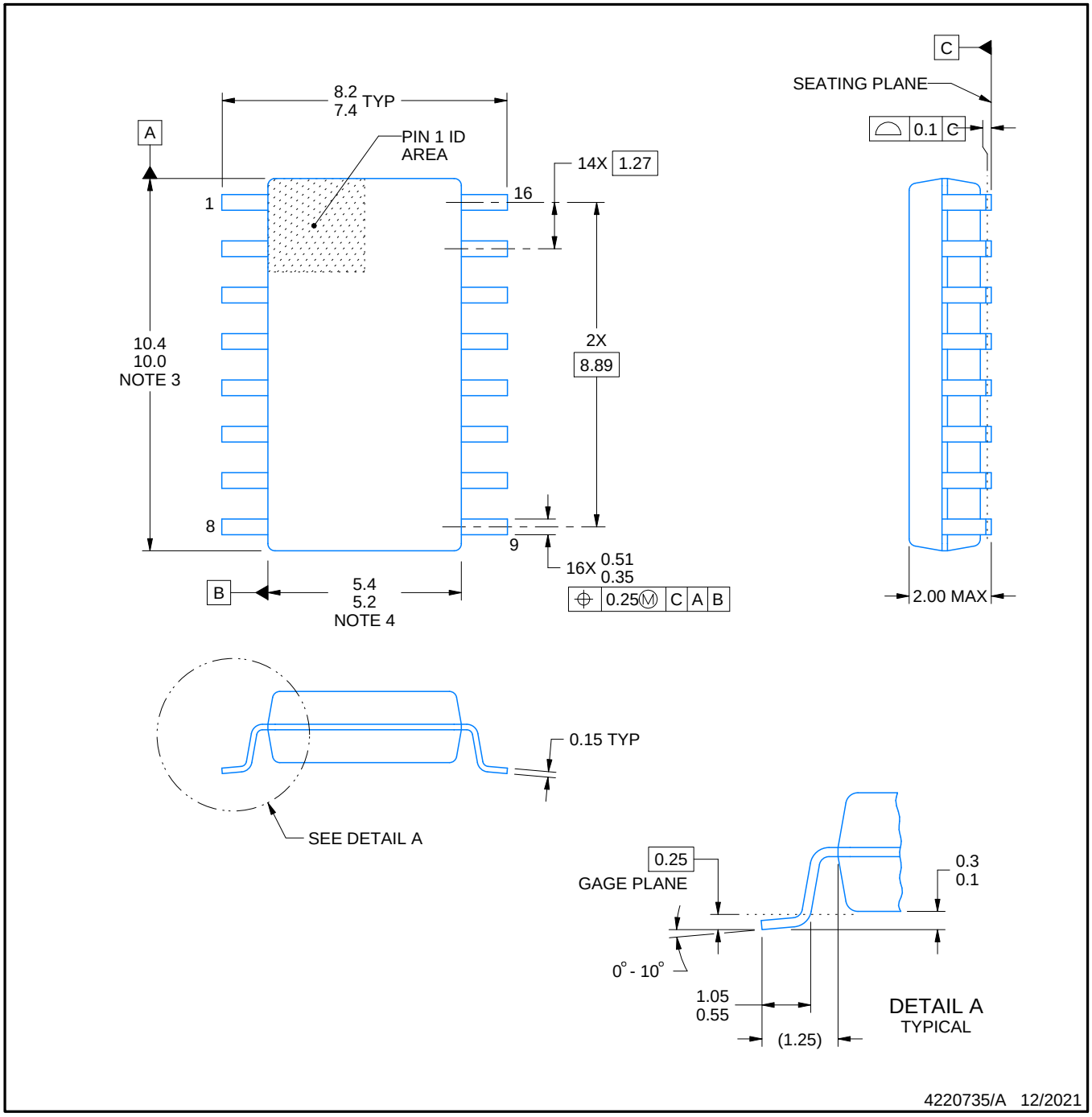


PACKAGE OUTLINE

NS0016A

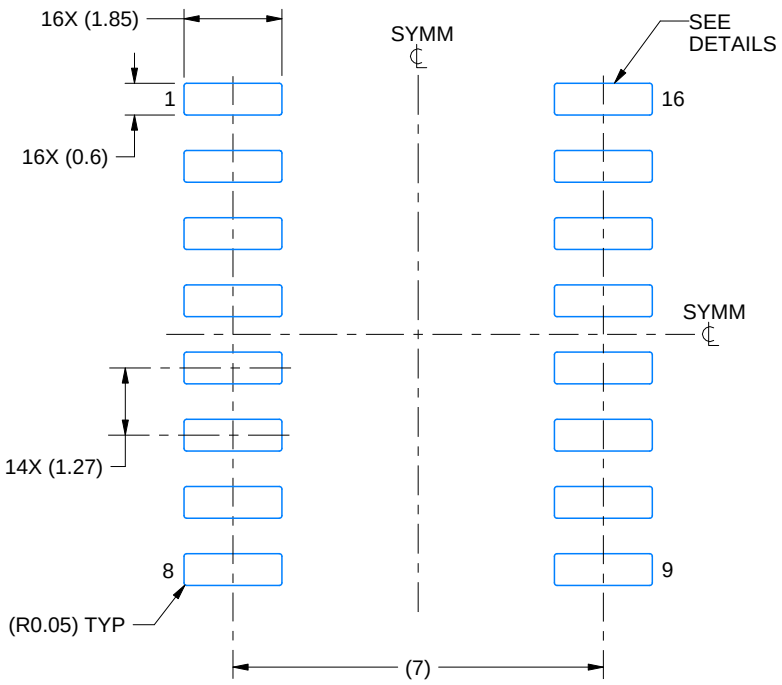
SOP - 2.00 mm max height

SOP

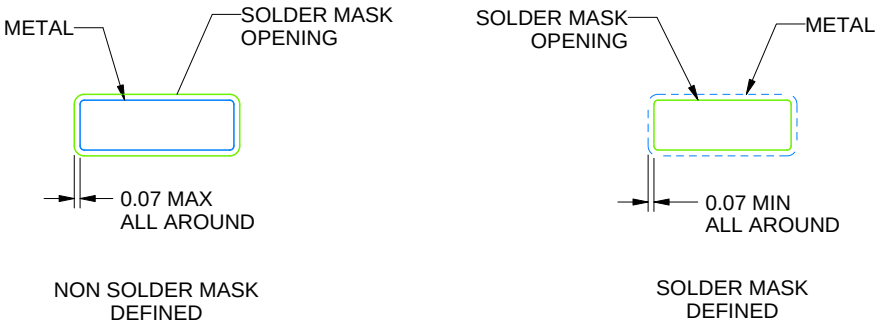


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

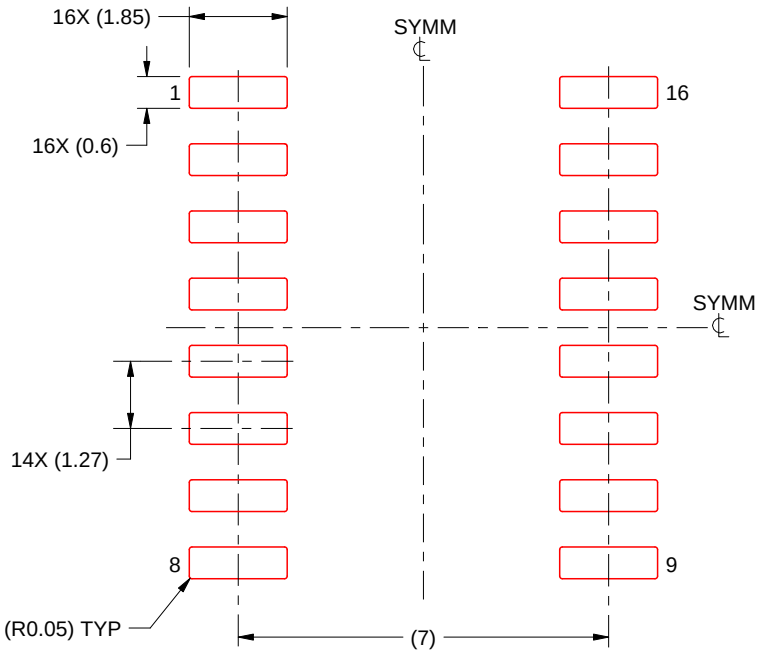
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



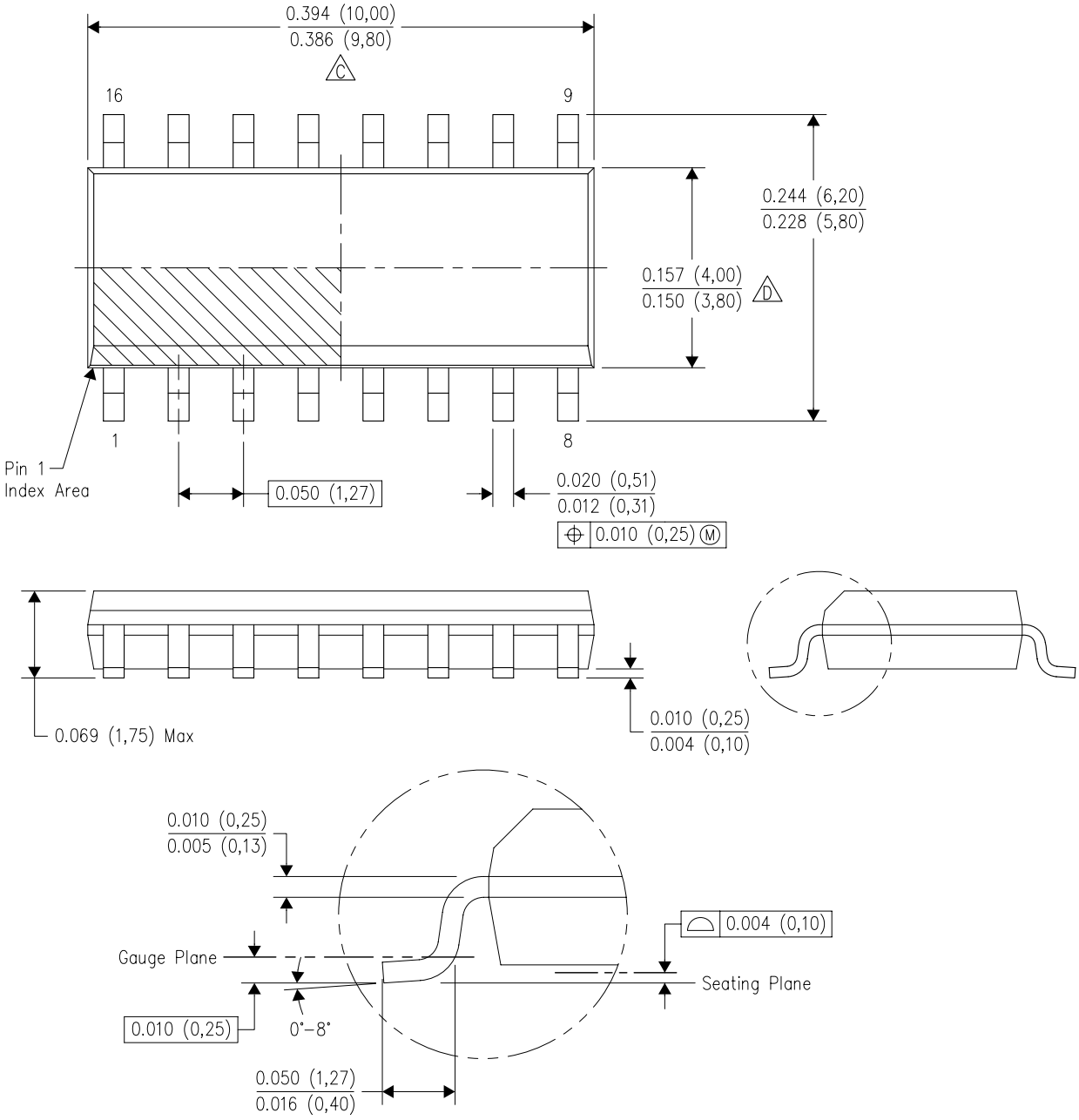
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

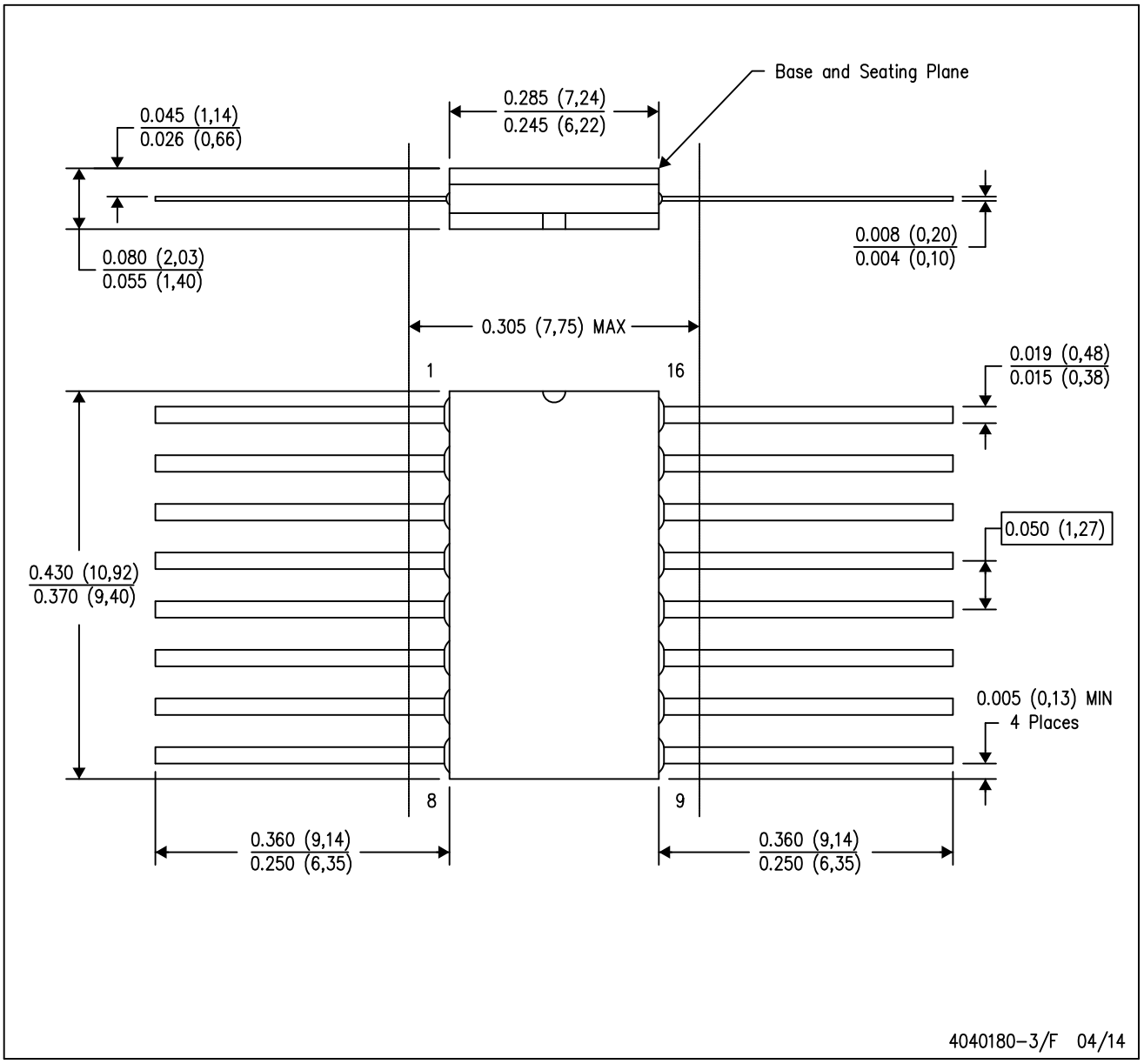
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

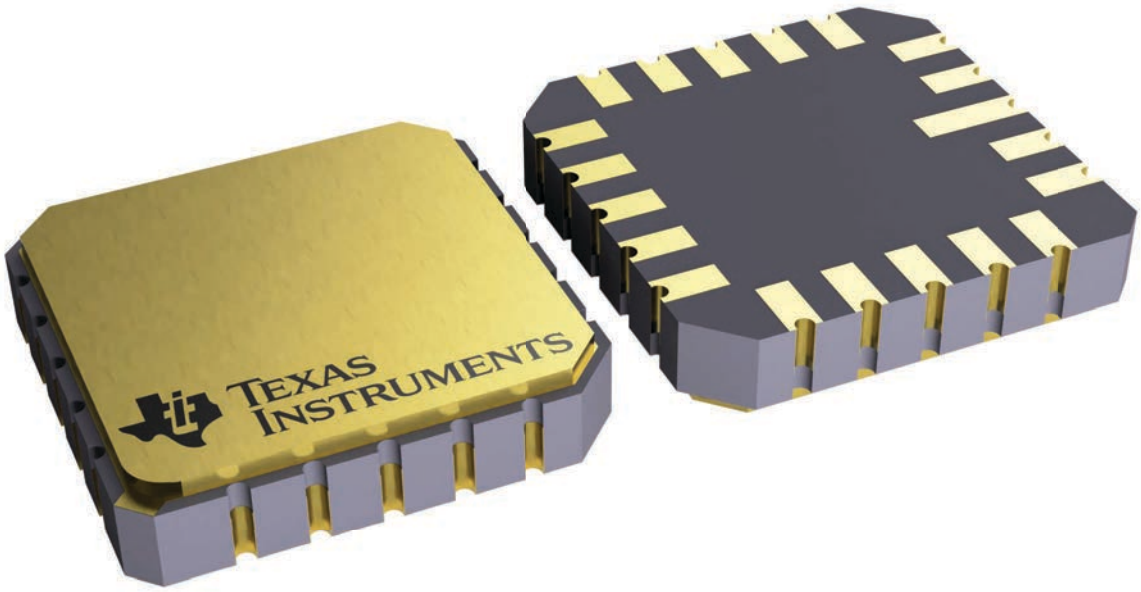
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

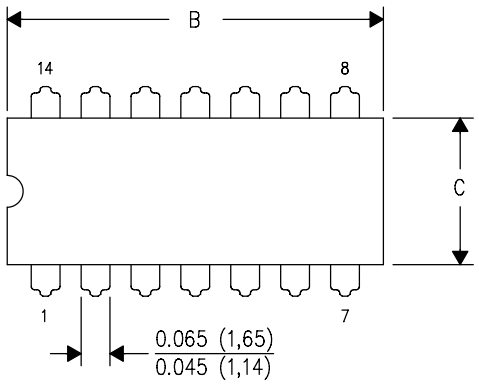


4229370VA\

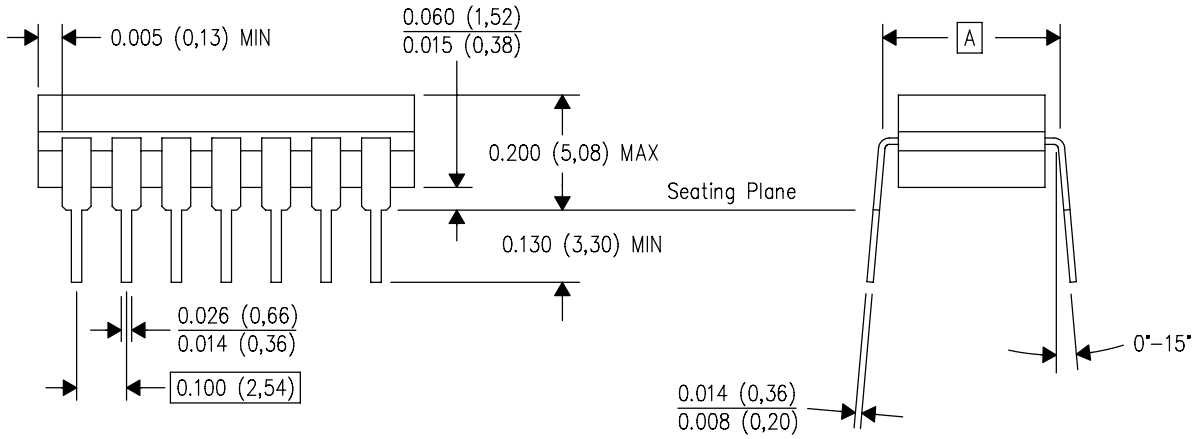
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

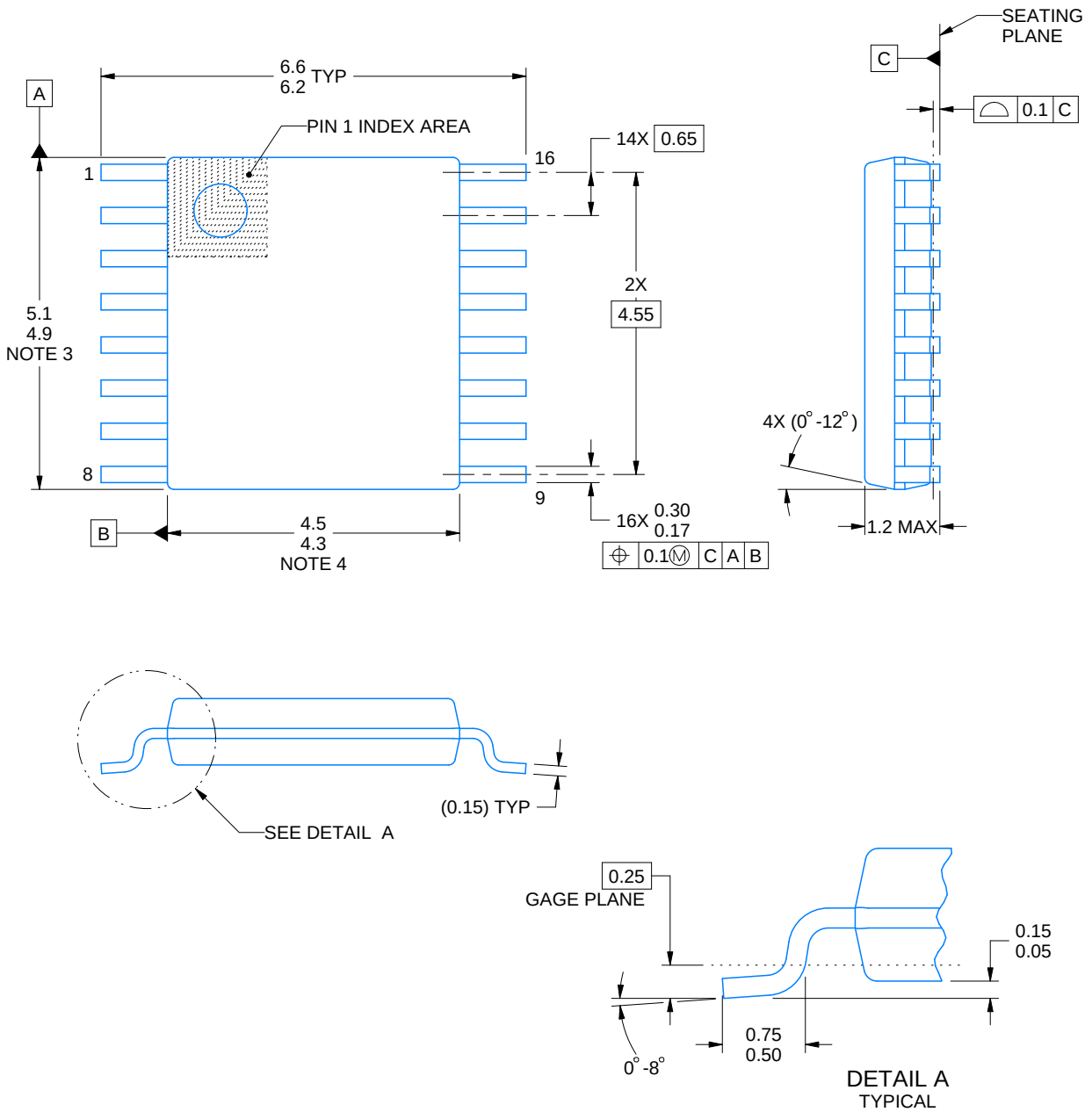
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

PW0016A

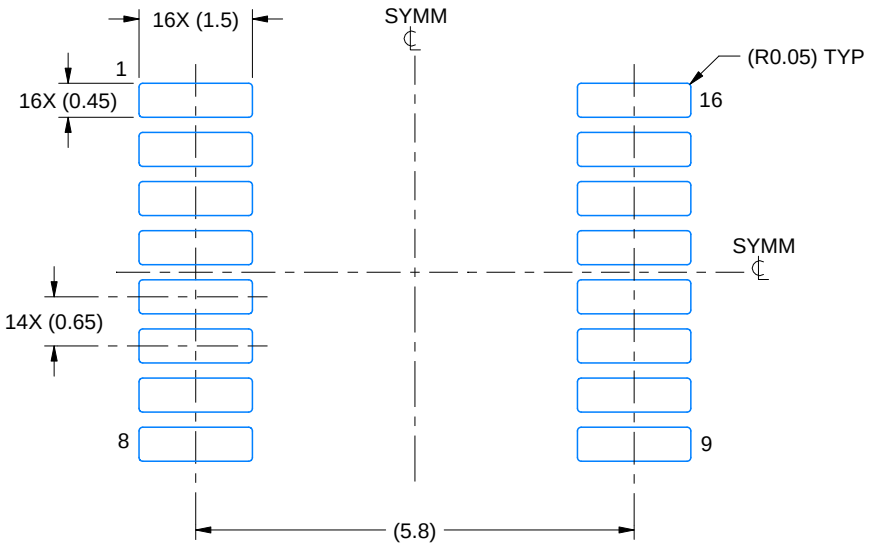
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

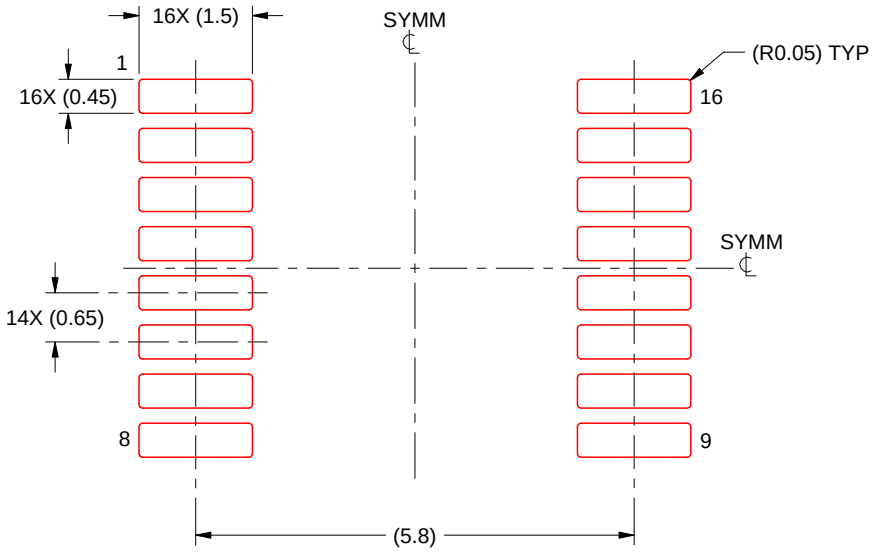


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

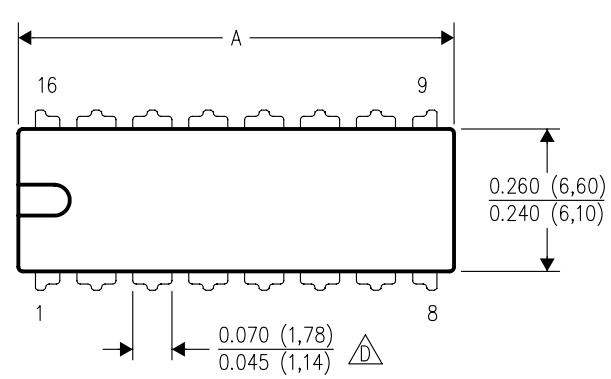
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

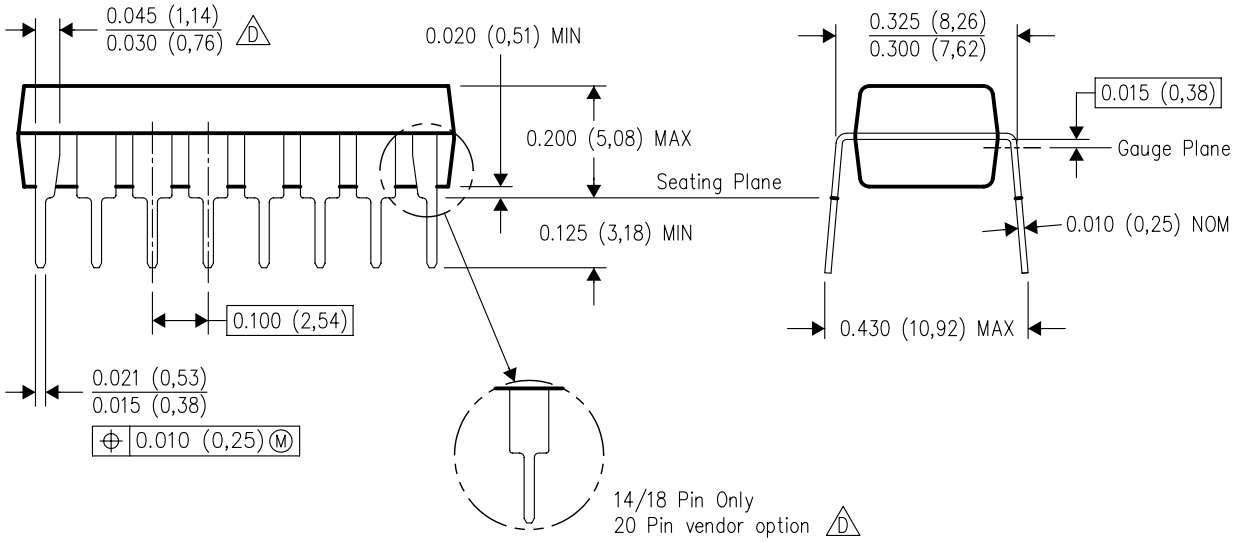
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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