TLC2274AM-MIL 先进 LinCMOS 轨至轨运算放大器

1 特性

- 输出摆幅包括两个电源轨
- 低噪声：在 f = 1kHz 时为 9nV/√Hz（典型值）
- 低输入偏置电流：1pA（典型值）
- 完全符合单电源及双电源操作的要求
- 共模输入电压范围包括负轨
- 高增益带宽：2.2MHz（典型值）
- 高转换率：3.6V/μs（典型值）
- 低输入偏移电压：在 T_A = 25°C 时为 2.5mV（最大值）
- 包括精简模型
- 可升级 TLC272 和 TLC274 的性能
- 可用于 Q-Temp 汽车

2 应用

- 白色家电（冰箱、洗衣机）
- 手持监控系统
- 配置控制和打印支持
- 变送器接口
- 电池供电类 应用

3 说明

TLC2274AM-MIL 器件是一款由德州仪器 (TI) 生产的四通道运算放大器。此器件在单电源或双电源应用中表现出优异的轨到轨输出性能，能够进一步扩大动态 范围。TLC2274AM-MIL 器件提供 2MHz 带宽和 3V/μs 转换率，适用于高速 应用。这些器件能够提供出色的交流性能，其噪声、输入偏移电压和功耗均低于现有 CMOS 运算放大器。TLC2274AM-MIL 器件的电压噪声为 9nV/√Hz，是竞争对手解决方案的二分之一。

TLC2274AM-MIL 器件具有高输入阻抗和低噪声特性，是用于高阻抗源（如压电传感器）小信号调节的绝佳选择。该器件属于微功耗级别，因此在手持式监控和遥感应用中 运转良好。此外，该器件的单电源或双电源具有轨到轨输出特性，是与模数转换器 (ADC) 对接的理想选择。对于精密 应用，TLC2272AM-MIL 器件的最大输入偏移电压为 950μV。该器件的额定工作电压为 5V 或 ±5V。

TLC2274AM-MIL 器件还在标准设计中对 TLC272 进行了显著升级，提供更高的输出动态范围、更低的噪声电压和更低的输入偏移电压。凭借这一系列增强特性，该器件能够用于更广泛的 应用。对于 需要 更高输出驱动和更宽输入电压范围的应用，请参见 TLV2432 和 TLV2442 器件。

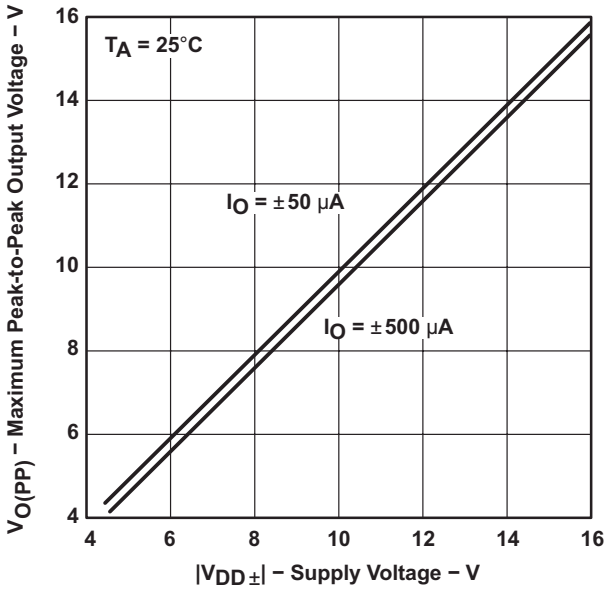
如果设计需要单个放大器，请参阅 TLV2211、TLV2221 和 TLV2231 系列。这些器件是 SOT-23 封装中的单轨至轨运算放大器。它们的尺寸较小且功耗较低，因此是高密度、电池供电设备的理想选择。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLC2274AM-MIL	SOIC (14)	3.91mm × 8.65mm
	CDIP (14)	6.67mm × 19.56mm
	LCCC (20)	8.89mm × 8.89mm
	CFP (14)	6.35mm × 19.30mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

最大峰-峰值输出电压与电源电压



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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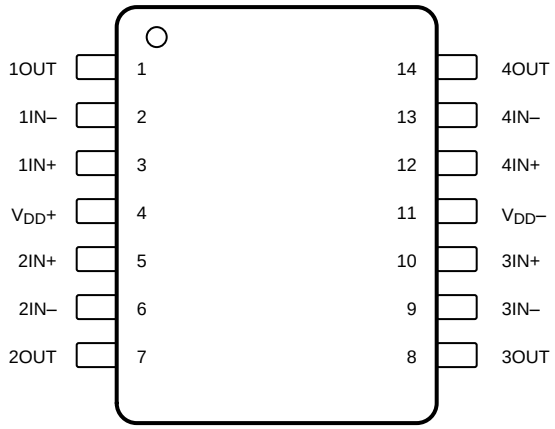
4 修订历史记录

日期	修订版本	注
2017 年 6 月	*	最初发布版本

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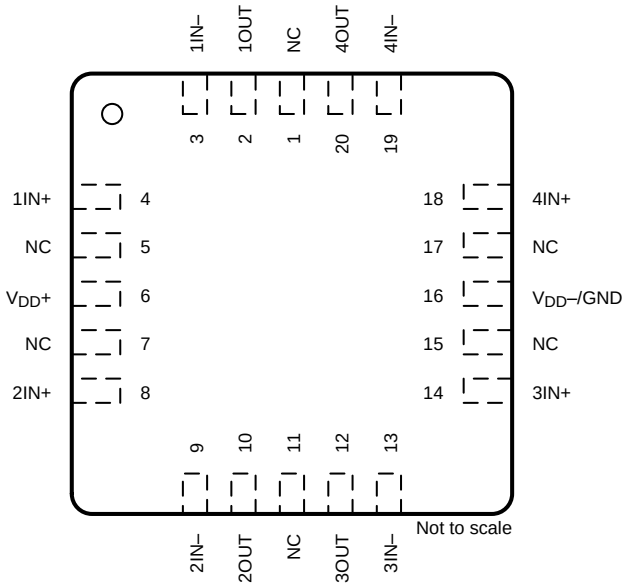
5 Pin Configuration and Functions

D or J Package
14-Pin SOIC or CDIP
Top View



Not to scale

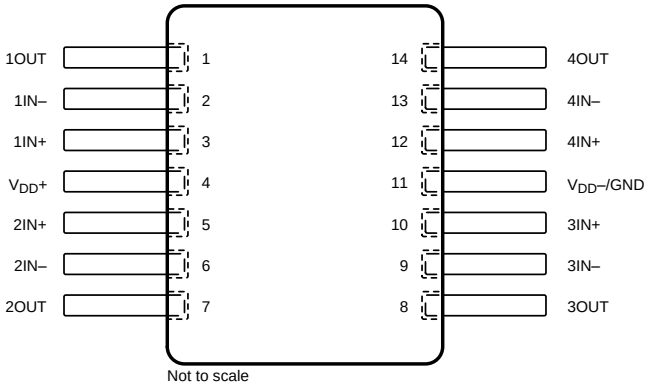
FK Package
20-Pin LCCC
Top View



Not to scale

NC – No internal connection

W Package
10-Pin CFP
Top View



Not to scale

NC – No internal connection

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Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	D, J, N, or W	FK		
1IN+	3	4	I	Non-inverting input, Channel 1
1IN–	2	3	I	Inverting input, Channel 1
1OUT	1	2	O	Output, Channel 1
2IN+	5	8	I	Non-inverting input, Channel 2
2IN–	6	9	I	Inverting input, Channel 2
2OUT	7	10	O	Output, Channel 2
3IN+	10	14	I	Non-inverting input, Channel 3
3IN–	9	13	I	Inverting input, Channel 3
3OUT	8	12	O	Output, Channel 3
4IN+	12	18	I	Non-inverting input, Channel 4
4IN–	13	19	I	Inverting input, Channel 4
4OUT	14	20	O	Output, Channel 4
V_{DD}+	4	6	—	Positive (highest) supply
V_{DD}–	11	16	—	Negative (lowest) supply
V_{DD}–/GND	—	—	—	Negative (lowest) supply
NC	—	1, 5, 7, 11, 15, 17	—	No connection

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{DD}+(2)		8	V
V_{DD}–(2)	–8		V
Differential input voltage, V_{ID}(3)		±16	V
Input voltage, V_I (any input)(2)	V_{DD}– – 0.3	V_{DD}+	V
Input current, I_I (any input)		±5	mA
Output current, I_O		±50	mA
Total current into V_{DD}+		±50	mA
Total current out of V_{DD}–		±50	mA
Duration of short-circuit current at (or below) 25°C(4)	Unlimited		
Operating ambient temperature range, T_A	–55	125	
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD}+ and V_{DD}–.
(3) Differential voltages are at IN+ with respect to IN–. Excessive current will flow if input is brought below V_{DD}– – 0.3 V.
(4) The output may be shorted to either supply. Temperature or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	Devices in D packages	±2000	V
	Charged-device model (CDM), per AEC Q100-011	Devices in D packages	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}±	Supply voltage	±2.2	±8	V
V_I	Input voltage	V_{DD}–	V_{DD}+ – 1.5	V
V_{IC}	Common-mode input voltage	V_{DD}–	V_{DD}+ – 1.5	V
T_A	Operating ambient temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLC2274AM-MIL					UNIT
		D (SOIC)	J (CDIP)	FK (LCCC)	N (PDIP)	W (CFP)	
		14-PIN	14-PIN	20-PIN	14-PIN	14-PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)(3)	115.6	—	—		—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (2)(3)	61.8	16.2	18		121.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.9	—	—		—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.3	—	—		—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.4	—	—		—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—		8.68	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7 (plastic) or MIL-STD-883 Method 1012 (ceramic).

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6.5 Electrical Characteristics V_{DD} = 5 V

at specified ambient temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	T_A = 25°C			300	950	µV
			T_A = –55°C to 125°C				1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				2		µV/°C
	Input offset voltage long-term drift(1)	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				0.002		µV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	T_A = 25°C			0.5	60	pA
			T_A = –55°C to 125°C				800	
I_{IB}	Input bias current	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	T_A = 25°C			1	60	pA
			T_A = –55°C to 125°C				800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; $\|V_{IO}\|$ ≤ 5 mV	T_A = 25°C		–0.3	2.5	4	V
			T_A = –55°C to 125°C		0	2.5	3.5	
V_{OH}	High-level output voltage	I_{OH} = –20 µA				4.99		V
		I_{OH} = –200 µA	T_A = 25°C		4.85	4.93		
			T_A = –55°C to 125°C		4.85			
		I_{OH} = –1 mA	T_A = 25°C		4.25	4.65		
			T_A = –55°C to 125°C		4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 50 µA			0.01		V
			I_{OL} = 500 µA	T_A = 25°C		0.09	0.15	
				T_A = –55°C to 125°C			0.15	
			I_{OL} = 5 mA	T_A = 25°C		0.9	1.5	
				T_A = –55°C to 125°C			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 10 kΩ(2)	T_A = 25°C		15	35		V/mV
			T_A = –55°C to 125°C		15			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V; R_L = 1 MΩ(2)				175		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	T_A = 25°C		70	75		dB
			T_A = –55°C to 125°C		70			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD} / 2, no load	T_A = 25°C		80	95		dB
			T_A = –55°C to 125°C		80			
I_{DD}	Supply currrent	V_O = 2.5 V, no load	T_A = 25°C			4.4	6	mA
			T_A = –55°C to 125°C				3	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ(2), C_L = 100 pF(2)	T_A = 25°C		2.3	3.6		V/µs
			T_A = –55°C to 125°C		1.7			
V_n	Equivalent input noise voltage	f = 10 Hz				50		nV/√Hz
		f = 1 kHz				9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz				1		µV
		f = 0.1 Hz to 10 Hz				1.4		
I_n	Equivalent input noise current					0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ(2)	A_V = 1			0.0013%		
			A_V = 10			0.004%		
			A_V = 100			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ(2), C_L = 100 pF(2)				2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ(2), C_L = 100 pF(2)				1		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ(2), Step = 0.5 V to 2.5 V, C_L = 100 pF(2)	To 0.1%			1.5		µs
			To 0.01%			2.6		

(1) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(2) Referenced to 0 V.

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Electrical Characteristics V_{DD} = 5 V (continued)

at specified ambient temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
φ_m	Phase margin at unity gain	R_L = 10 kΩ(2), C_L = 100 pF(2)		50		°
	Gain margin	R_L = 10 kΩ(2), C_L = 100 pF(2)		10		dB

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6.6 Electrical Characteristics V_{DD}± = ±5 V

at specified ambient temperature, V_{DD}± = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		300	950	μV
				T_A = –55°C to 125°C			1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				2		μV/°C
	Input offset voltage long-term drift	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				0.002		μV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		0.5	60	pA
				T_A = –55°C to 125°C			800	
I_{IB}	Input bias current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		1	60	pA
				T_A = –55°C to 125°C			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; $\|V_{IO}\|$ ≤ 5 mV		T_A = 25°C	–5.3	0	4	V
				T_A = –55°C to 125°C	–5	0	3.5	
V_{OM}+	Maximum positive peak output voltage	I_O = –20 μA				4.99		V
		I_O = –200 μA		T_A = 25°C	4.85	4.93		
				T_A = –55°C to 125°C	4.85			
		I_O = –1 mA		T_A = 25°C	4.25	4.65		
				T_A = –55°C to 125°C	4.25			
V_{OM}–	Maximum negative peak output voltage	V_{IC} = 0 V,	I_O = 50 μA			–4.99		V
			I_O = 500 μA	T_A = 25°C	–4.85	–4.91		
				T_A = –55°C to 125°C	–4.85			
			I_O = 5 mA	T_A = 25°C	–3.5	–4.1		
				T_A = –55°C to 125°C	–3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V; R_L = 10 kΩ		T_A = 25°C	20	50		V/mV
				T_A = –55°C to 125°C	20			
		V_O = ±4 V; R_L = 1 MΩ				300		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = –5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C	75	80		dB
				T_A = –55°C to 125°C	75			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD+} = 2.2 V to ±8 V, V_{IC} = 0 V, no load		T_A = 25°C	80	95		dB
				T_A = –55°C to 125°C	80			
I_{DD}	Supply currrent	V_O = 0 V, no load		T_A = 25°C		4.8	6	mA
				T_A = –55°C to 125°C			6	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF		T_A = 25°C	2.3	3.6		V/μs
				T_A = –55°C to 125°C	1.7			
V_n	Equivalent input noise voltage	f = 10 Hz				50		nV/√Hz
		f = 1 kHz				9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz				1		μV
		f = 0.1 Hz to 10 Hz				1.4		
I_n	Equivalent input noise current					0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = ±2.3, f = 20 kHz, R_L = 10 kΩ		A_V = 1		0.0011%		
				A_V = 10		0.004%		
				A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF				2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ, C_L = 100 pF				0.54		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ, Step = –2.3 V to 2.3 V, C_L = 100 pF		To 0.1%		1.5		μs
				To 0.01%		3.2		
φ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF				52		°
	Gain margin	R_L = 10 kΩ, C_L = 100 pF				10		dB

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6.7 Typical Characteristics

Table 1. Table of Graphs

			FIGURE (1)
V_{IO}	Input offset voltage	Distribution	1, 2
		vs Common-mode voltage	3, 4
α_{VIO}	Input offset voltage temperature coefficient	Distribution	5, 6 (2)
I_{IB} /I_{IO}	Input bias and input offset current	vs Ambient temperature	7 (2)
V_I	Input voltage	vs Supply voltage	8
		vs Ambient temperature	9 (2)
V_{OH}	High-level output voltage	vs High-level output current	10 (2)
V_{OL}	Low-level output voltage	vs Low-level output current	11, 12 (2)
V_{OM+}	Maximum positive peak output voltage	vs Output current	13 (2)
V_{OM-}	Maximum negative peak output voltage	vs Output current	14 (2)
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	15
I_{OS}	Short-circuit output current	vs Supply voltage	16
		vs Ambient temperature	17 (2)
V_O	Output voltage	vs Differential input voltage	18, 19
A_{VD}	Large-signal differential voltage amplification	vs Load resistance	20
	Large-signal differential voltage amplification and phase margin	vs Frequency	21, 22
	Large-signal differential voltage amplification	vs Ambient temperature	23 (2), 24 (2)
z_0	Output impedance	vs Frequency	25, 26
CMRR	Common-mode rejection ratio	vs Frequency	27
		vs Ambient temperature	28
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	29, 30
		vs Ambient temperature	31 (2)
I_{DD}	Supply current	vs Supply voltage	(2), 32 (2)
		vs Ambient temperature	(2), 33 (2)
SR	Slew rate	vs Load Capacitance	34
		vs Ambient temperature	35 (2)
V_O	Inverting large-signal pulse response		36, 37
	Voltage-follower large-signal pulse response		38, 39
	Inverting small-signal pulse response		40, 41
	Voltage-follower small-signal pulse response		42, 43
V_n	Equivalent input noise voltage	vs Frequency	44, 45
	Noise voltage over a 10-second period		46
	Integrated noise voltage	vs Frequency	47
THD+N	Total harmonic distortion + noise	vs Frequency	48
	Gain-bandwidth product	vs Supply voltage	49
		vs Ambient temperature	50 (2)
φ_m	Phase margin	vs Load capacitance	51
	Gain margin	vs Load capacitance	52

(1) For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.
(2) Data at high and low temperatures are applicable only within the rated operating ambient temperature ranges of the various devices.

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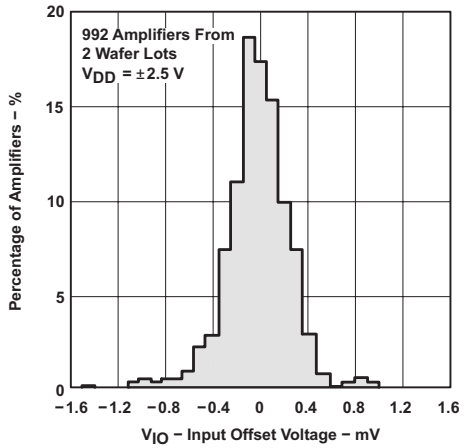


Figure 1. Distribution of Input Offset Voltage

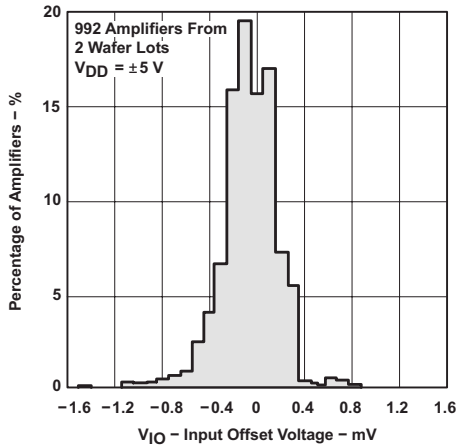


Figure 2. Distribution of Input Offset Voltage

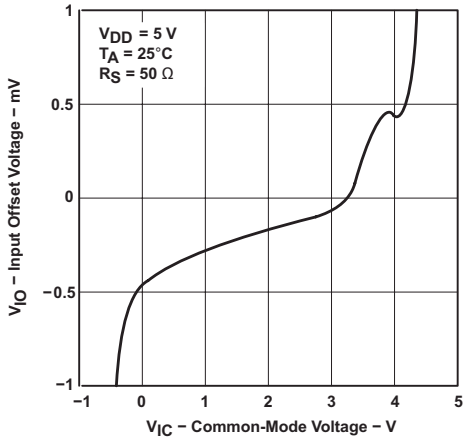


Figure 3. Input Offset Voltage vs Common-Mode Voltage

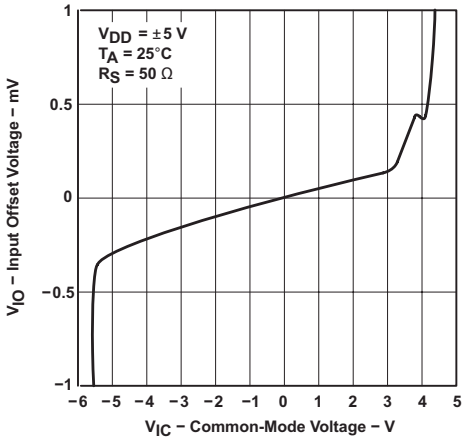


Figure 4. Input Offset Voltage vs Common-Mode Voltage

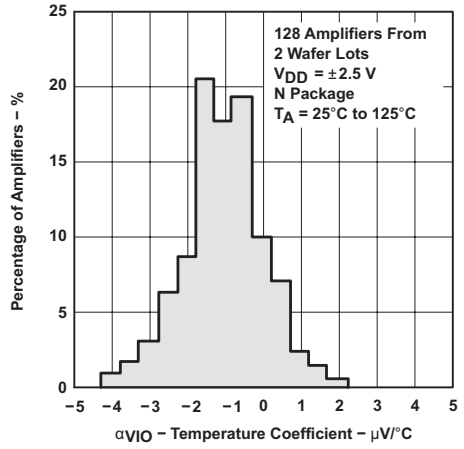


Figure 5. Distribution vs Input-Offset-Voltage Temperature Coefficient

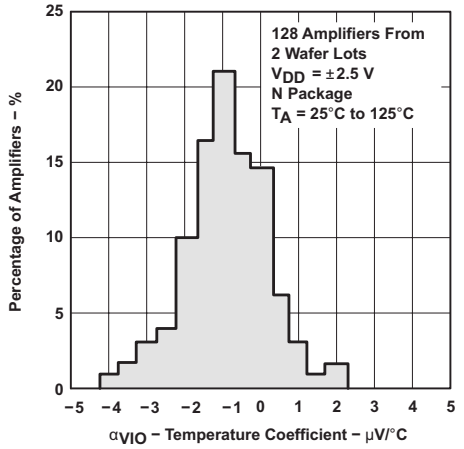


Figure 6. Distribution vs Input-Offset-Voltage Temperature Coefficient

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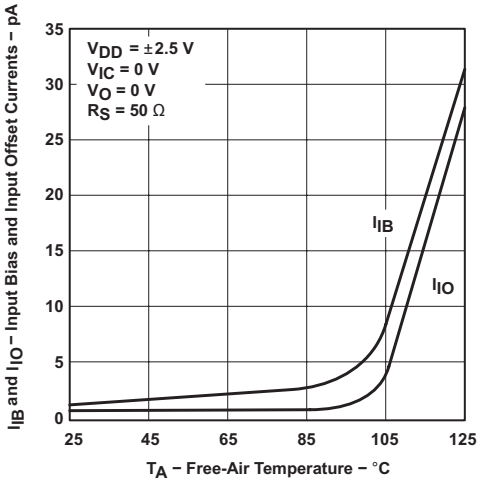


Figure 7. Input Bias and Input Offset Current vs Ambient Temperature

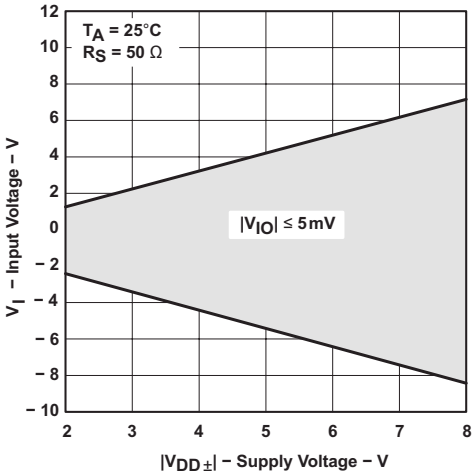


Figure 8. Input Voltage vs Supply Voltage

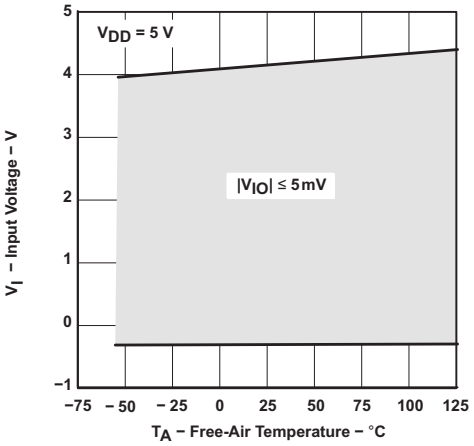


Figure 9. Input Voltage vs Ambient Temperature

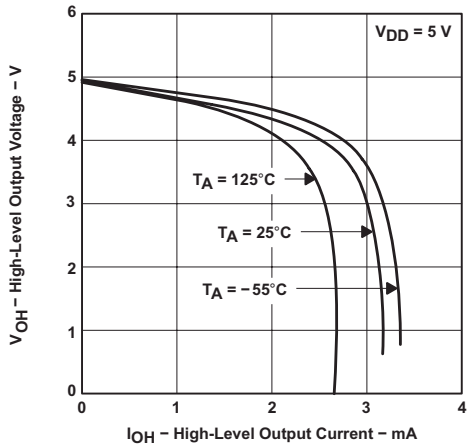


Figure 10. High-Level Output Voltage vs High-Level Output Current

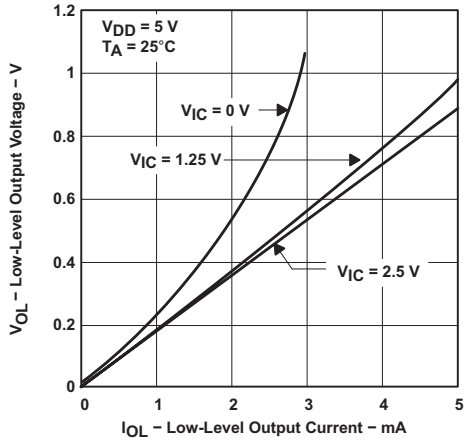


Figure 11. Low-Level Output Voltage vs Low-Level Output Current

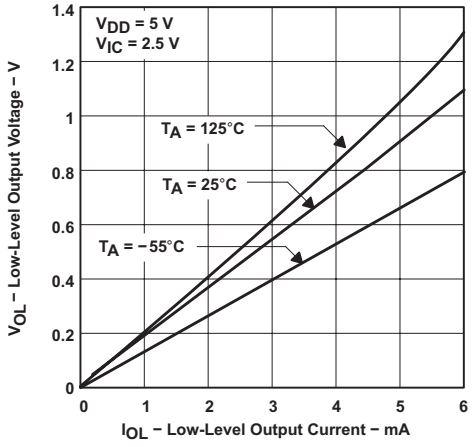


Figure 12. Low-Level Output Voltage vs Low-Level Output Current

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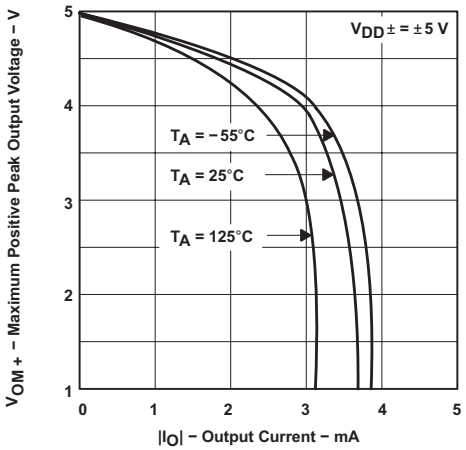


Figure 13. Maximum Positive Peak Output Voltage vs Output Current

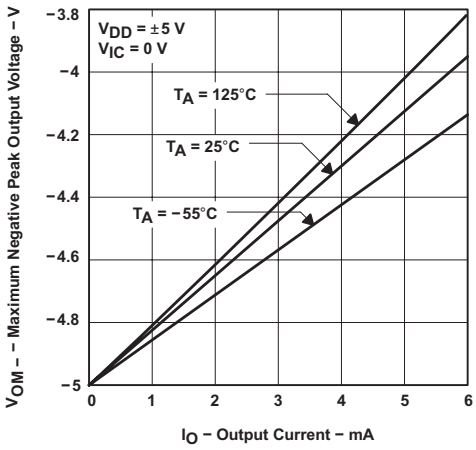


Figure 14. Maximum Negative Peak Output Voltage vs Output Current

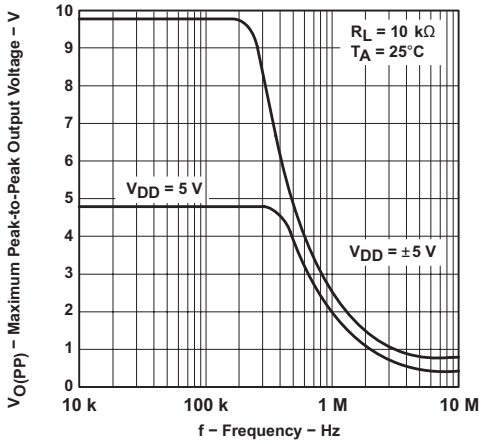


Figure 15. Maximum Peak-to-Peak Output Voltage vs Frequency

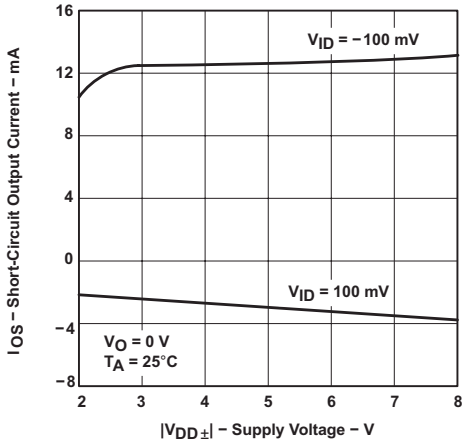


Figure 16. Short-Circuit Output Current vs Supply Voltage

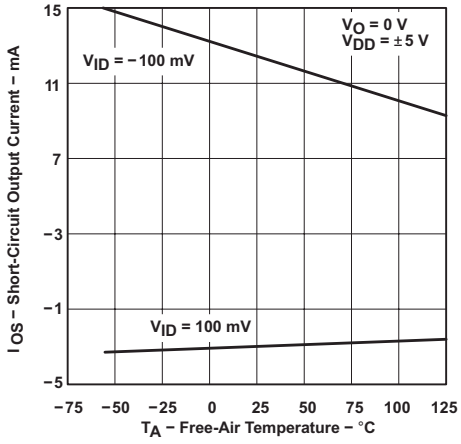


Figure 17. Short-Circuit Output Current vs Ambient Temperature

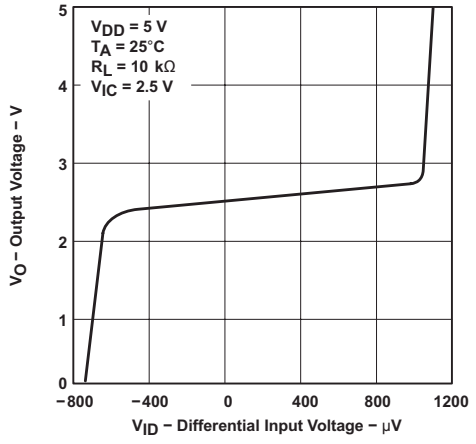


Figure 18. Output Voltage vs Differential Input Voltage

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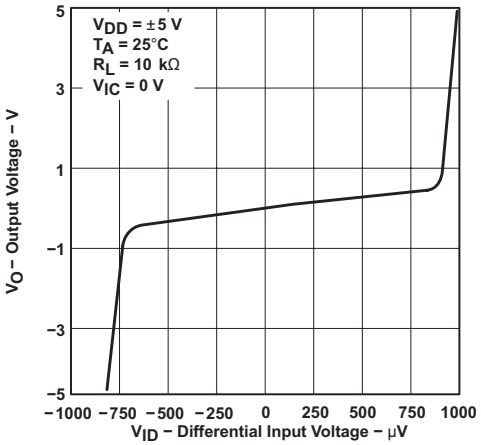


Figure 19. Output Voltage vs Differential Input Voltage

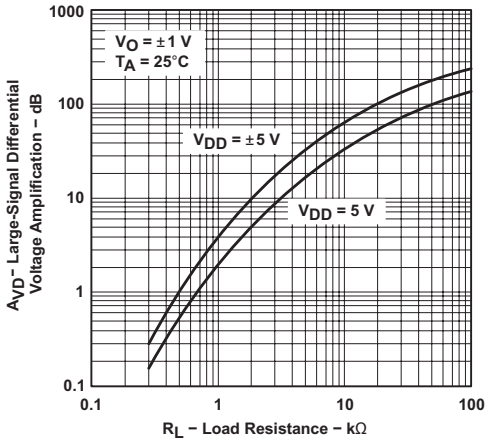


Figure 20. Large-Signal Differential Voltage Amplification vs Load Resistance

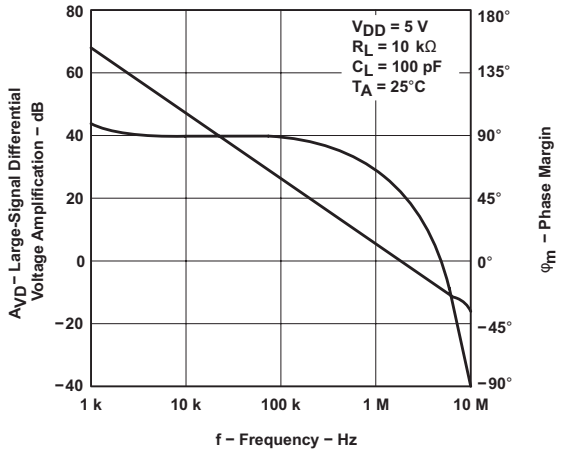


Figure 21. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

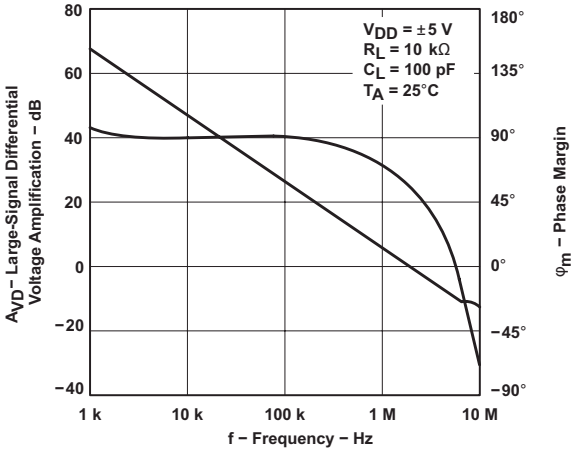


Figure 22. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

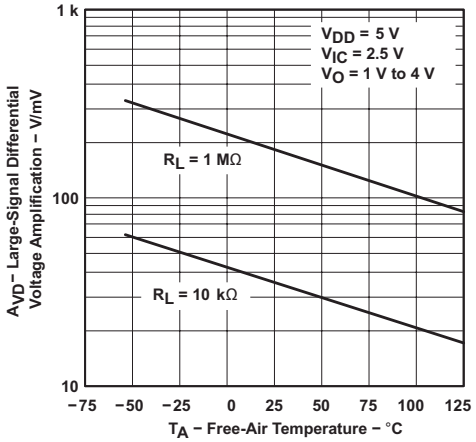


Figure 23. Large-Signal Differential Voltage Amplification vs Ambient Temperature

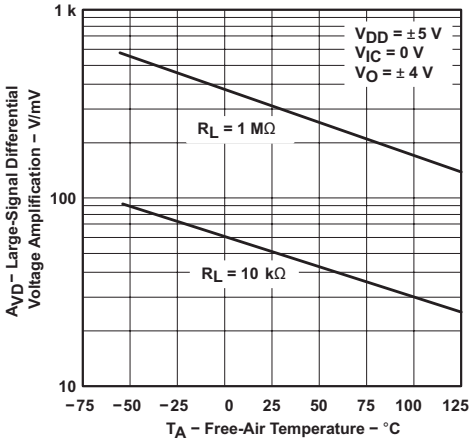


Figure 24. Large-Signal Differential Voltage Amplification vs Ambient Temperature

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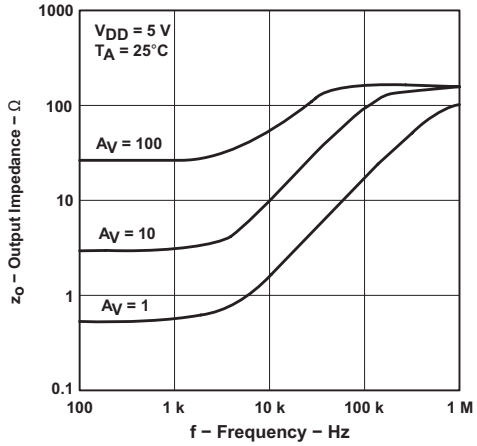


Figure 25. Output Impedance vs Frequency

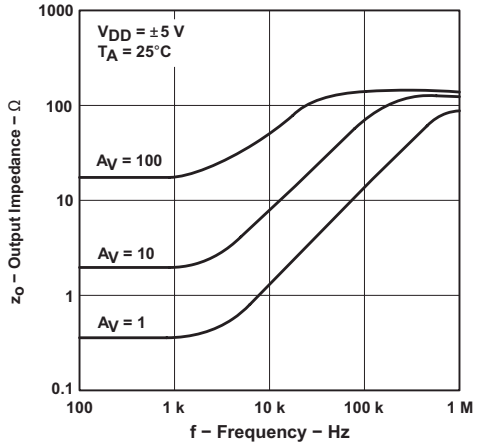


Figure 26. Output Impedance vs Frequency

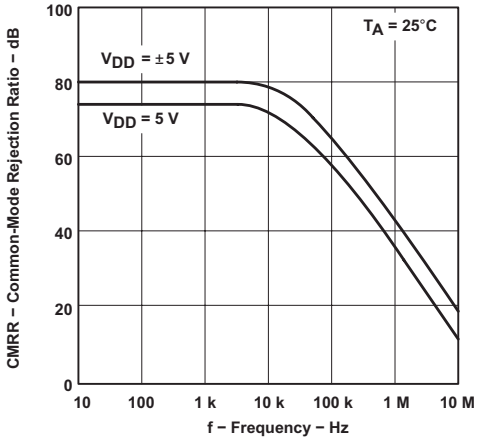


Figure 27. Common-Mode Rejection Ratio vs Frequency

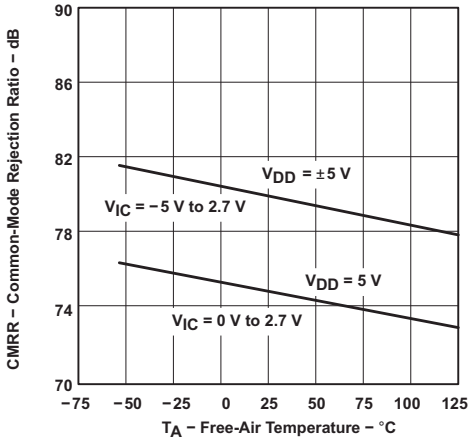


Figure 28. Common-Mode Rejection Ratio vs Ambient Temperature

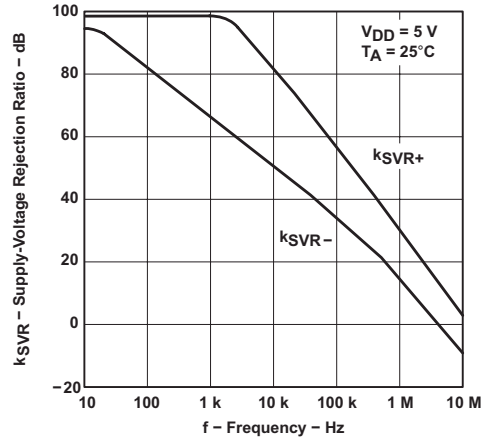


Figure 29. Supply-Voltage Rejection Ratio vs Frequency

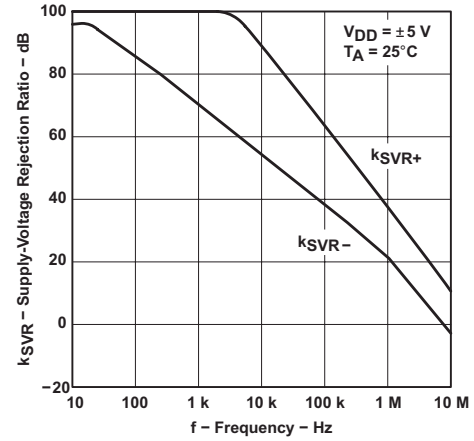


Figure 30. Supply-Voltage Rejection Ratio vs Frequency

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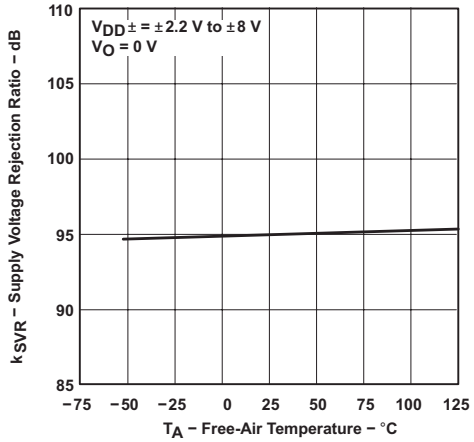


Figure 31. Supply-Voltage Rejection Ratio vs Ambient Temperature

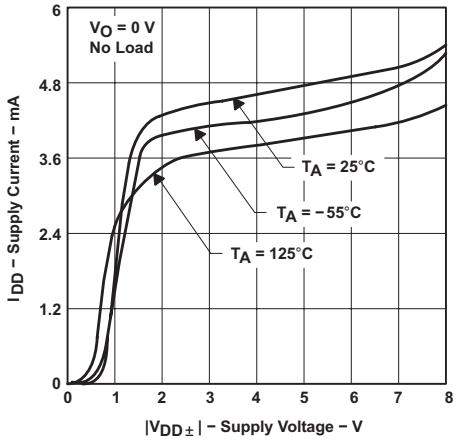


Figure 32. Supply Current vs Supply Voltage

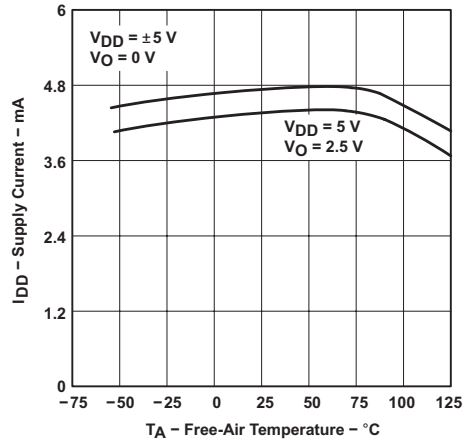


Figure 33. Supply Current vs Ambient Temperature

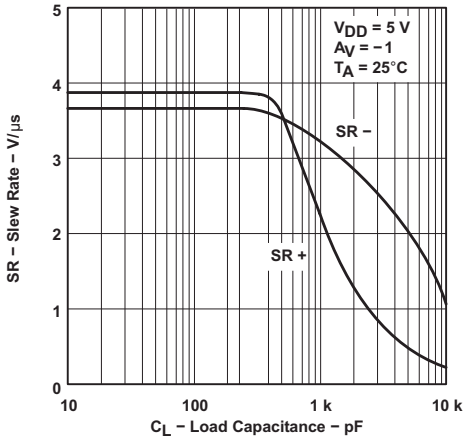


Figure 34. Slew Rate vs Load Capacitance

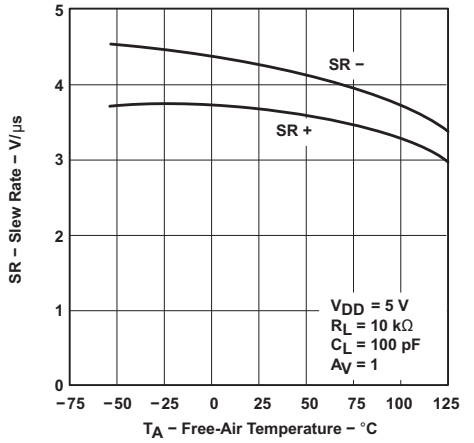


Figure 35. Slew Rate vs Ambient Temperature

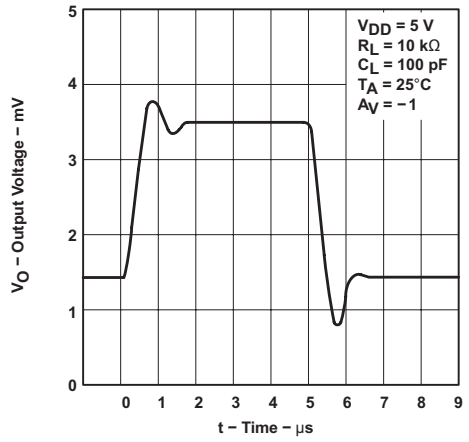


Figure 36. Inverting Large-Signal Pulse Response

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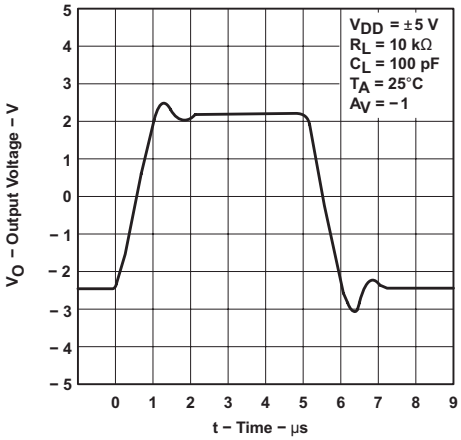


Figure 37. Inverting Large-Signal Pulse Response

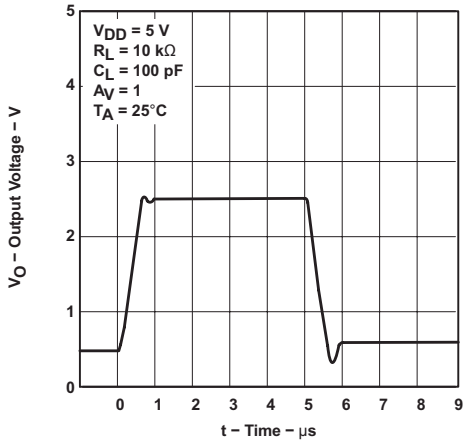


Figure 38. Voltage-Follower Large-Signal Pulse Response

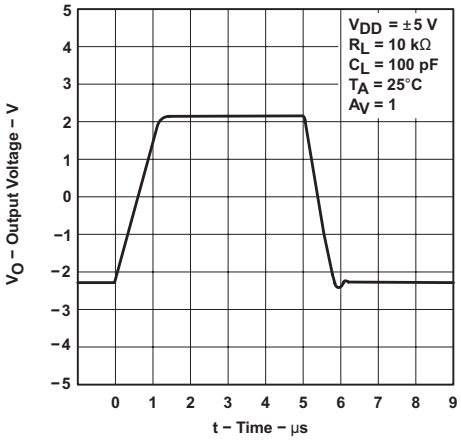


Figure 39. Voltage-Follower Large-Signal Pulse Response

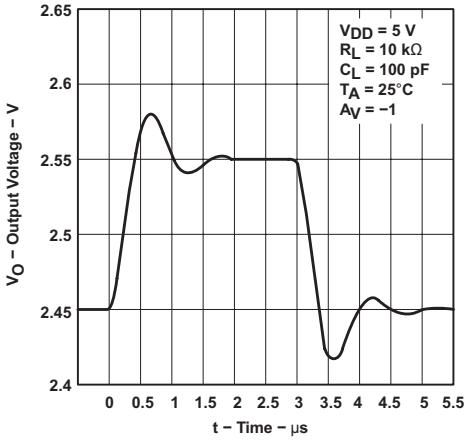


Figure 40. Inverting Small-Signal Pulse Response

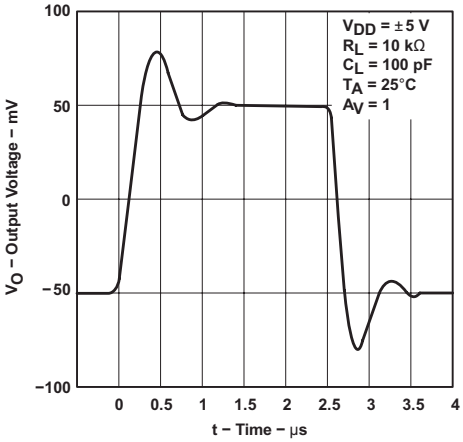


Figure 41. Inverting Small-Signal Pulse Response

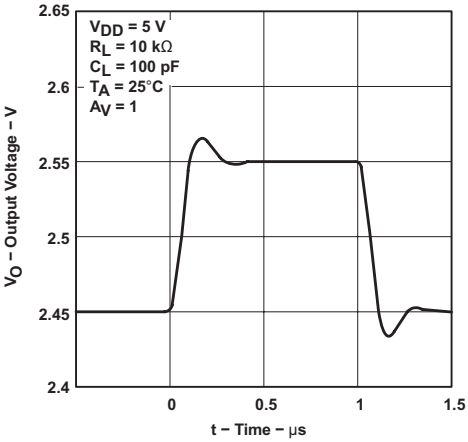


Figure 42. Voltage-Follower Small-Signal Pulse Response

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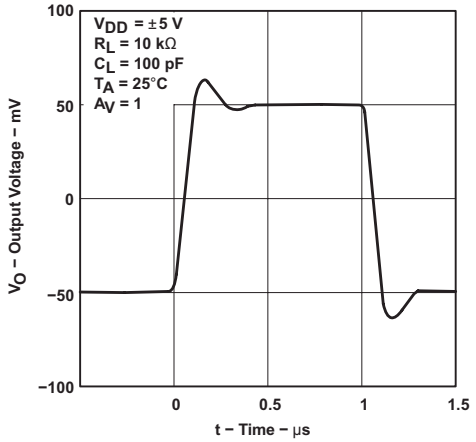


Figure 43. Voltage-Follower Small-Signal Pulse Response

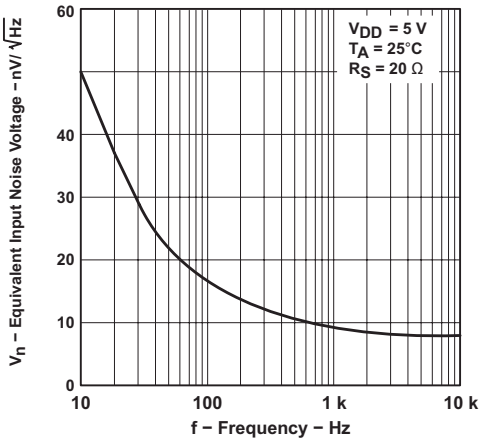


Figure 44. Equivalent Input Noise Voltage vs Frequency

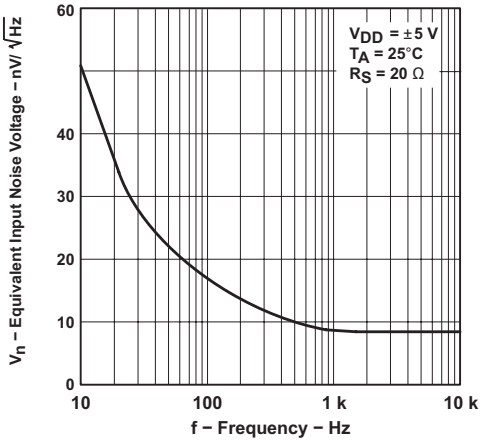


Figure 45. Equivalent Input Noise Voltage vs Frequency

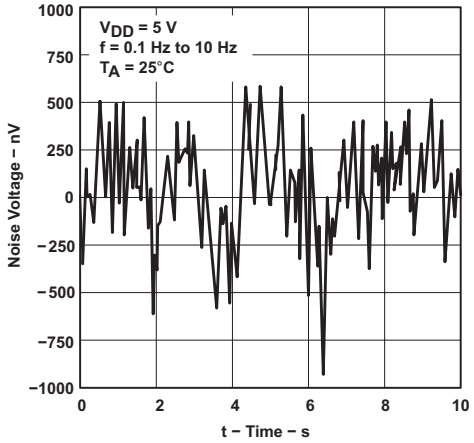


Figure 46. Noise Voltage Over a 10-Second Period

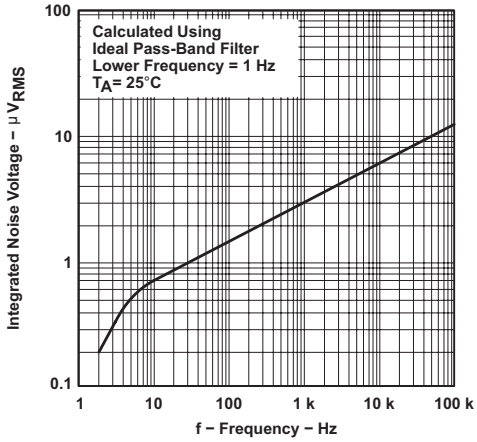


Figure 47. Integrated Noise Voltage vs Frequency

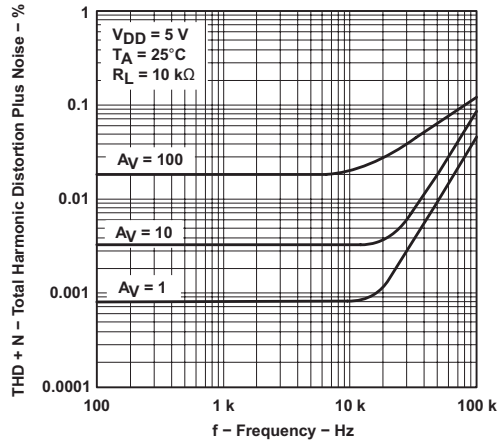


Figure 48. Total Harmonic Distortion + Noise vs Frequency

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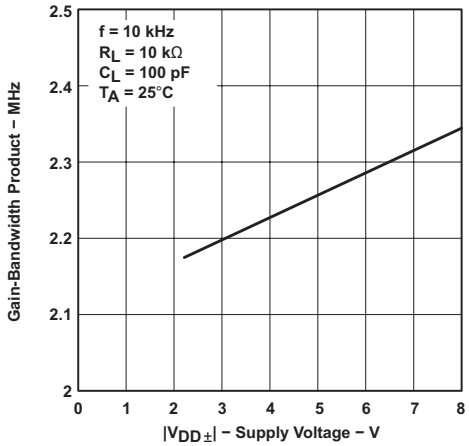


Figure 49. Gain-Bandwidth Product vs Supply Voltage

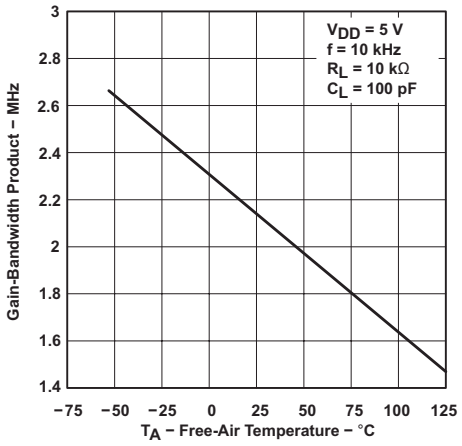


Figure 50. Gain-Bandwidth Product vs Ambient Temperature

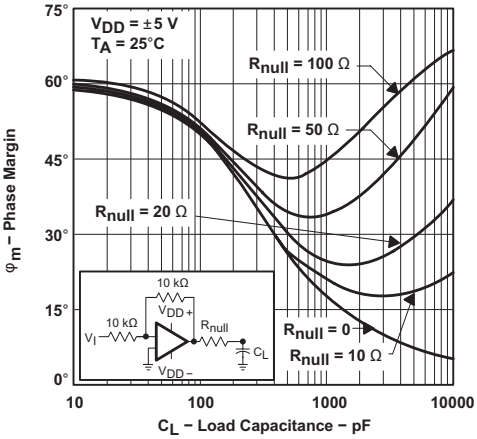


Figure 51. Phase Margin vs Load Capacitance

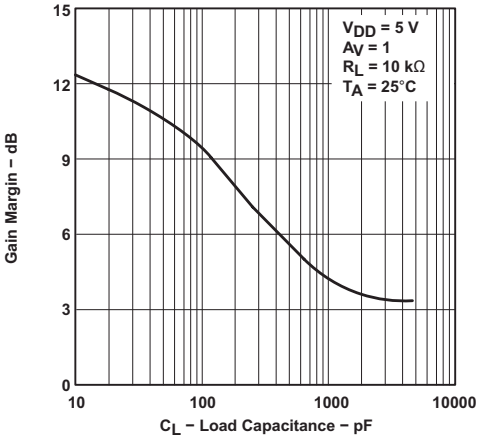


Figure 52. Gain Margin vs Load Capacitance

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7 Detailed Description

7.1 Overview

The TLC2274AM-MIL device is a rail-to-rail output operational amplifier. The device operates from a 4.4-V to 16-V single supply or ±2.2-V to ±8-V dual supply, is unity-gain stable, and is suitable for a wide range of general-purpose applications.

7.2 Functional Block Diagram

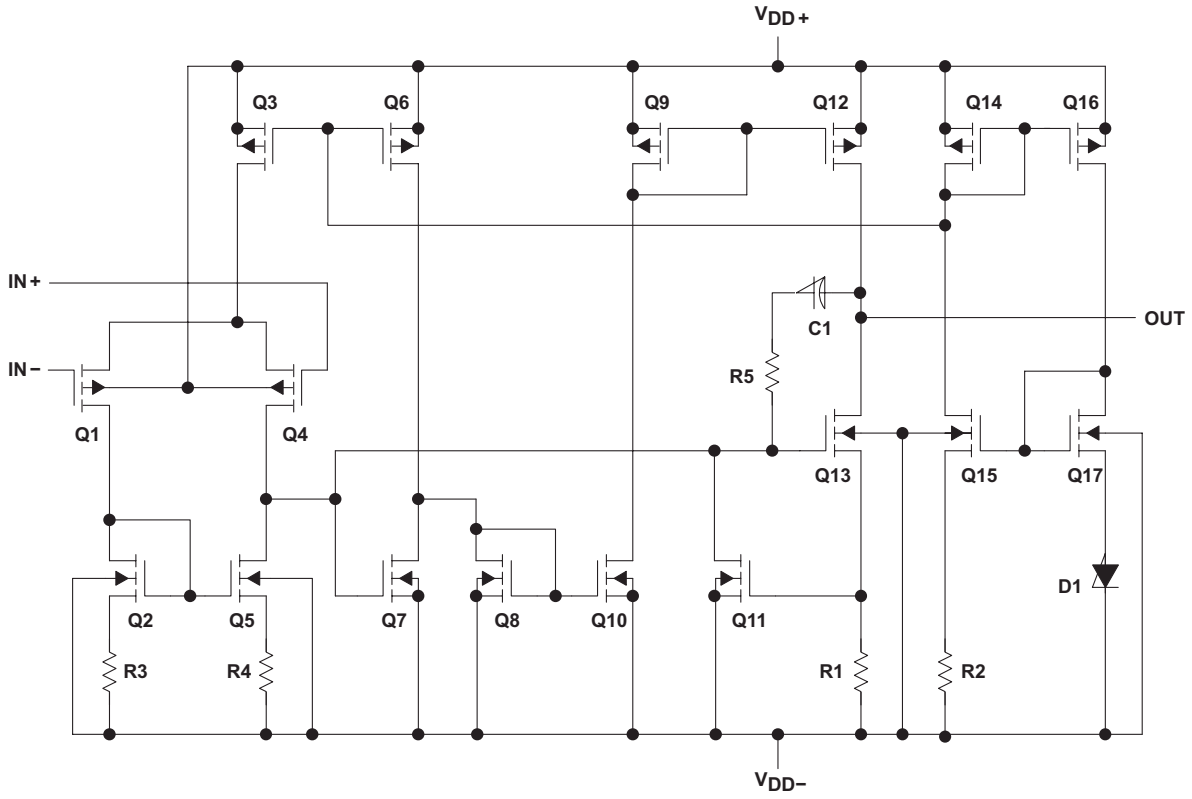


Table 2. Device Component Count(1)

COMPONENT	COUNT
Transistors	76
Resistors	52
Diodes	18
Capacitors	6

(1) Includes both amplifiers and all ESD, bias, and trim circuitry.

7.3 Feature Description

The TLC2274AM-MIL device features 2-MHz bandwidth and voltage noise of 9 nV/$\sqrt{\text{Hz}}$ with performance rated from 4.4 V to 16 V across a temperature range (–55°C to 125°C). LinMOS suits a wide range of audio, automotive, industrial, and instrumentation applications.

7.4 Device Functional Modes

The TLC2274AM-MIL device is powered on when the supply is connected. The device may operate with single or dual supply, depending on the application. The device is in its full-performance mode once the supply is above the recommended value.

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8 Application and Implementation

NOTE

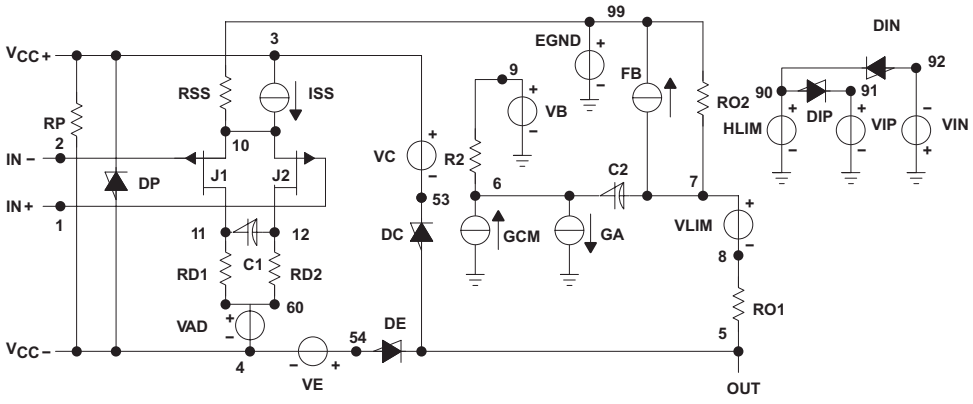
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8.1 Application Information

8.1.1 Macromodel Information

Macromodel information provided was derived using MicroSim Parts™, the model generation software used with MicroSim PSpice™. The Boyle macromodel (1) and subcircuit in Figure 53 were generated using the TLC2274AM-MIL typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit




```
.SUBCKT TLC227x 1 2 3 4 5
C1      11      12      1214E−12
C2      6       7       760.00E−12
DC      5       53      53DX
DE      54      5       5DX
DLP     90      91      91DX
DLN     92      90      90DX
DP      4       3       3DX
EGND    99      0       0POLY (2) (3,0) (4,) 0 .5 .5
FB      99      0       0POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 −1E6 1E6 1E6 −1E6
GA      6       0       011 12 377.0E−6
GCM 0 6 10 99 134E−9
ISS     3       10      10DC 216.OE−6
HLIM    90      0       0VLIM 1K
J1      11      1       210 JX
J2      12      10      110 JX
R2      6       9       9100.OE3
RD1     60      11      112.653E3
RD2     60      12      122.653E3
R01     8       5       550
R02     7       99      9950
RP      3       2       44.310E3
RSS     10      99      99925.9E3
VAD     60      4       4−.5
VB      9       0       0DC 0
VC 3 53 DC .78
VE      54      4       4DC .78
VLIM    7       8       8DC 0
VLP     91      0       0DC 1.9
VLN     0       92      92DC 9.4
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=1.500E−12BETA=1.316E-3
+ VTO=−.270)
.ENDS
```

Figure 53. Boyle Macromodel and Subcircuit

(1) *Macromodeling of Integrated Circuit Operational Amplifiers*, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

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8.2 Typical Application

8.2.1 High-Side Current Monitor

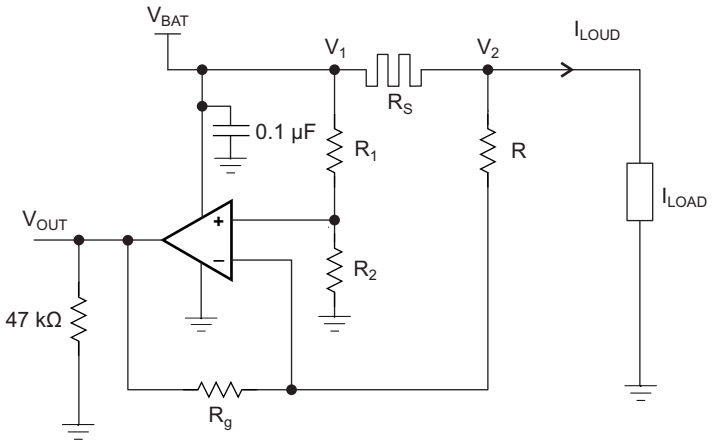


Figure 54. Equivalent Schematic (Each Amplifier)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

PARAMETER		VALUE
V_{BAT}	Battery voltage	12 V
R_{SENSE}	Sense resistor	0.1 Ω
I_{LOAD}	Load current	0 A to 10 A
	Operational amplifier	Set in differential configuration with gain = 10

8.2.1.2 Detailed Design Procedure

This circuit is designed for measuring the high-side current in automotive body control modules with a 12-V battery or similar applications. The operational amplifier is set as differential with an external resistor network.

8.2.1.2.1 Differential Amplifier Equations

Equation 1 and Equation 2 are used to calculate V_{OUT}.

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g}-\frac{R_1}{R_2}}{1+\frac{R_1}{R_2}}\times\frac{V_1+V_2}{2}+\frac{1+\frac{1}{2}\left(\frac{R_1}{R_2}+\frac{R}{R_g}\right)}{1+\frac{R_1}{R_2}}(V_1-V_2)\right) \quad (1)$$

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g}-\frac{R_1}{R_2}}{1+\frac{R_1}{R_2}}\times V_{BAT}+\frac{1+\frac{1}{2}\left(\frac{R_1}{R_2}+\frac{R}{R_g}\right)}{1+\frac{R_1}{R_2}}\times R_S\times I_{Load}\right) \quad (2)$$

In an ideal case $R_1 = R$ and $R_2 = R_g$, and V_{OUT} can then be calculated using Equation 3:

$$V_{OUT} = \frac{R_g}{R}\times R_S\times I_{Load} \quad (3)$$

However, as the resistors have tolerances, they cannot be perfectly matched.

$R_1 = R \pm \Delta R_1$

$R_2 = R_2 \pm \Delta R_2$

$R = R \pm \Delta R$

$R_g = R_g \pm \Delta R_g$

$$Tol = \frac{DR}{R} \tag{4}$$

By developing the equations and neglecting the second order, the worst case is when the tolerances add up. This is shown by Equation 5.

$$V_{OUT} = \pm (4\ Tol)\frac{R_g}{R + R_g} \times V_{BAT} + \left(1 \pm 2\ Tol\left(1 + \frac{2R}{R + R_g}\right)\right)\frac{R_g}{R} \times R_S \times I_{LOAD}$$

where

- Tol = 0.01 for 1%
- Tol = 0.001 for 0.1%

(5)

If the resistors are perfectly matched, then Tol = 0 and V_{OUT} is calculated using Equation 6.

$$V_{OUT} = \frac{R_g}{R} \times R_S \times I_{LOAD} \tag{6}$$

The highest error is from the common mode, as shown in Equation 7.

$$4\ (Tol)\frac{R_g}{R + R_g} \times V_{BAT} \tag{7}$$

Gain of 10, R_g / R = 10, and Tol = 1%:

Common mode error = ((4 × 0.01) / 1.1) × 12 V = 0.436 V

Gain of 10 and Tol = 0.1%:

Common mode error = 43.6 mV

The resistors were chosen from 2% batches.

R_1 and R 12 kΩ

R_2 and R_g 120 kΩ

Ideal Gain = 120 / 12 = 10

The measured value of the resistors:

R_1 = 11.835 kΩ

R = 11.85 kΩ

R_2 = 117.92 kΩ

R_g = 118.07 kΩ

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8.2.1.3 Application Curves

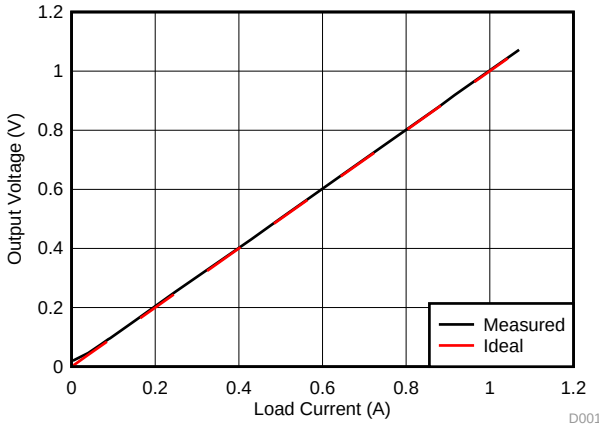


Figure 55. Output Voltage Measured vs Ideal (0 to 1 A)

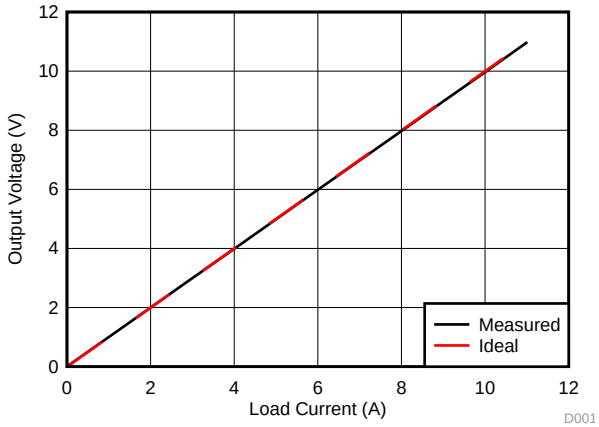


Figure 56. Output Voltage Measured vs Ideal (0 to 10 A)

9 Power Supply Recommendations

Supply voltage for a single supply is from 4.4 V to 16 V, and from ±2.2 V to ±8 V for a dual supply. In the high-side sensing application, the supply is connected to a 12-V battery.

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10 Layout

10.1 Layout Guidelines

The TLC2274AM-MIL device is a wideband amplifier. To realize the full operational performance of the device, good high-frequency printed-circuit-board (PCB) layout practices are required. Low-loss 0.1-μF bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

10.2 Layout Example

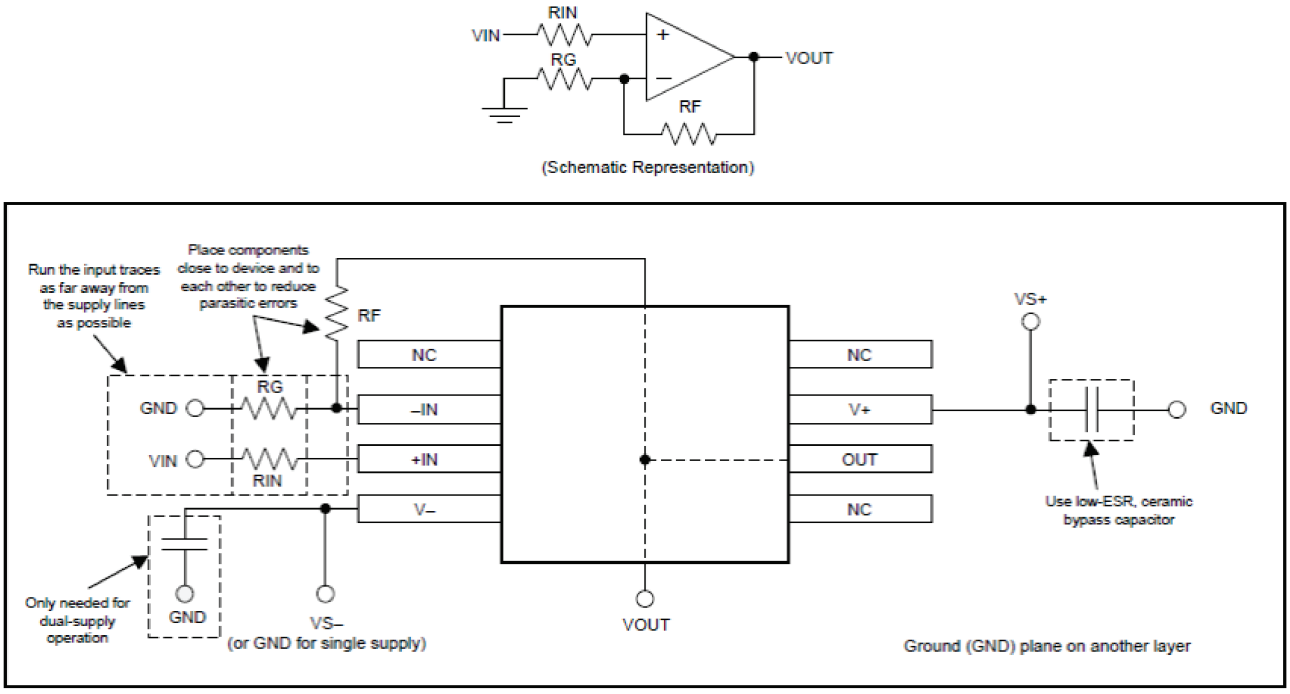


Figure 57. Layout Example

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11 器件和文档支持

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是针对指定器件提供的最新数据。本数据随时可能发生变更并且不对本文档进行修订，恕不另行通知。要获得这份数据表的浏览器版本，请查阅左侧的导航窗格。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9318202Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202Q2A TLC2274 AMFKB
5962-9318202QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QCA TLC2274AMJB
5962-9318202QDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QDA TLC2274AMWB
TLC2274AMFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202Q2A TLC2274 AMFKB
TLC2274AMFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202Q2A TLC2274 AMFKB
TLC2274AMJB	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QCA TLC2274AMJB
TLC2274AMJB.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QCA TLC2274AMJB
TLC2274AMWB	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QDA TLC2274AMWB
TLC2274AMWB.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QDA TLC2274AMWB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

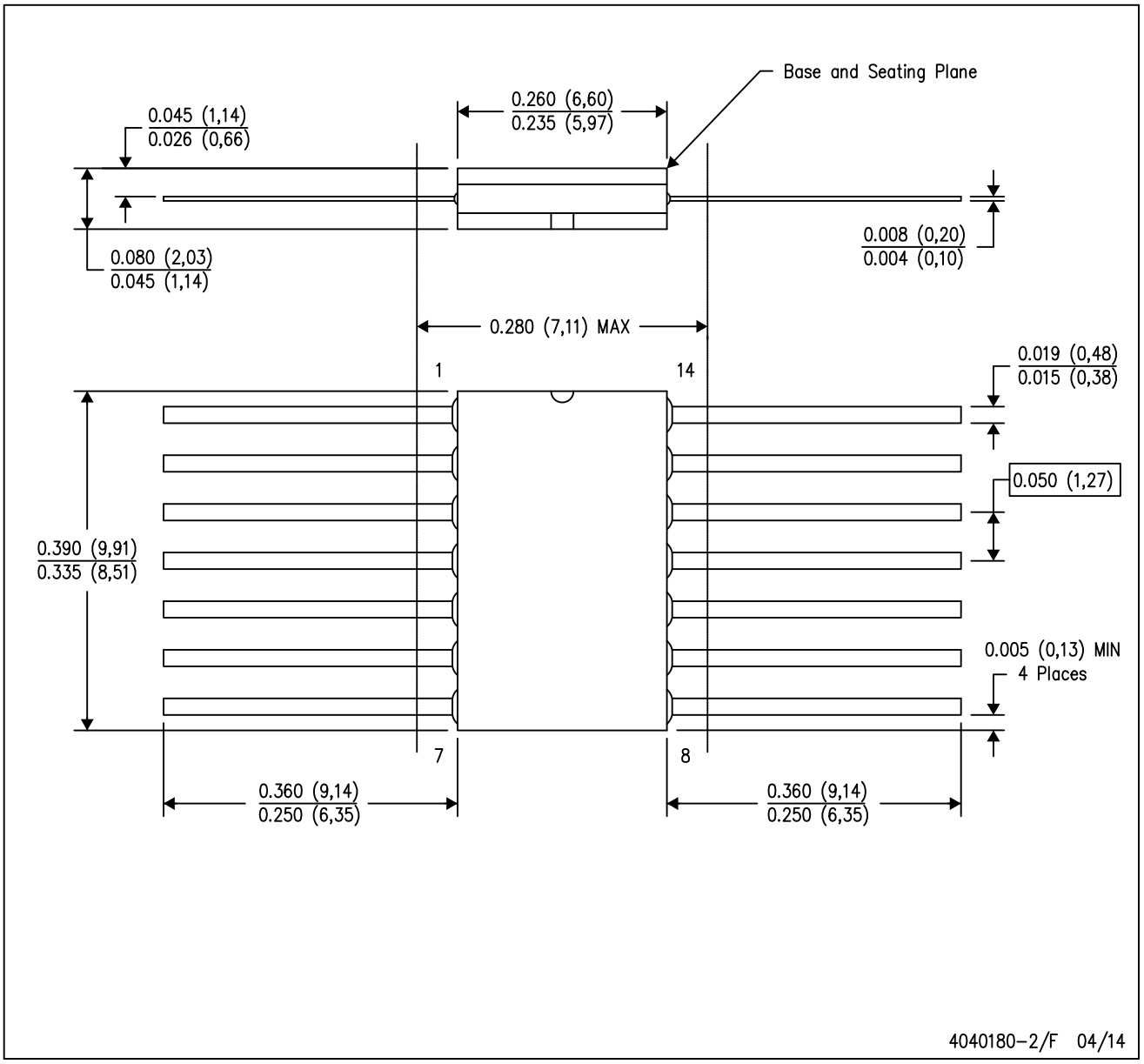
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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

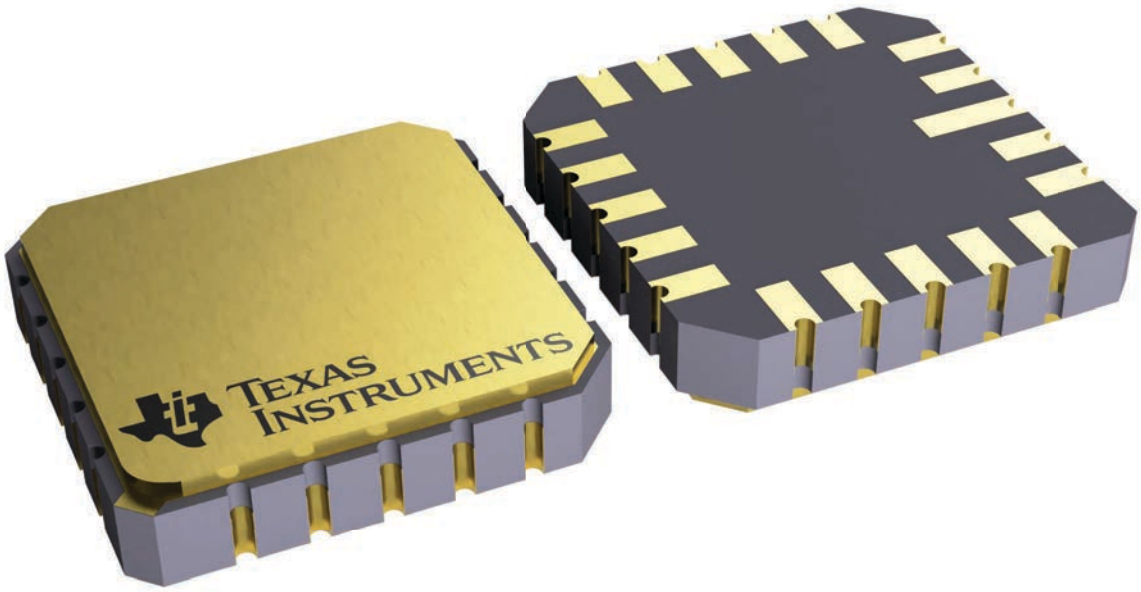
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

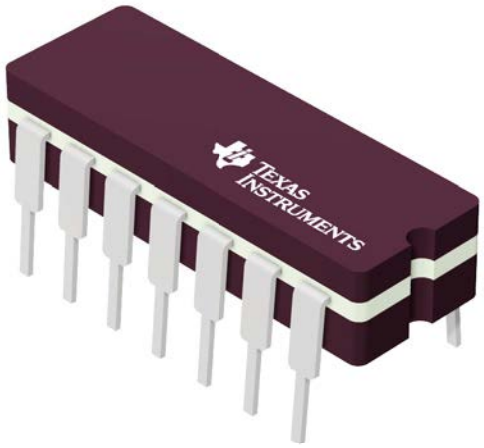


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

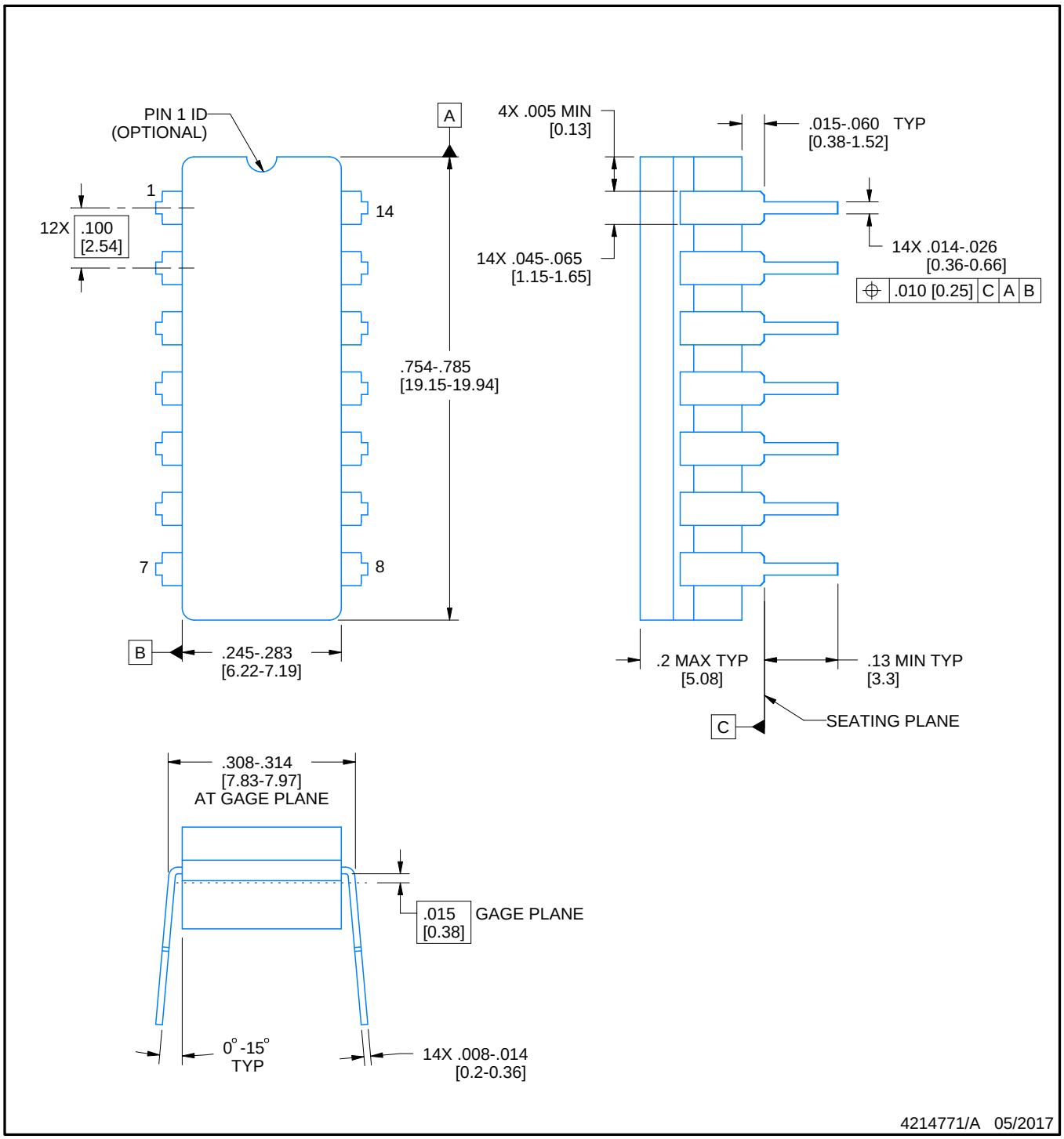


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

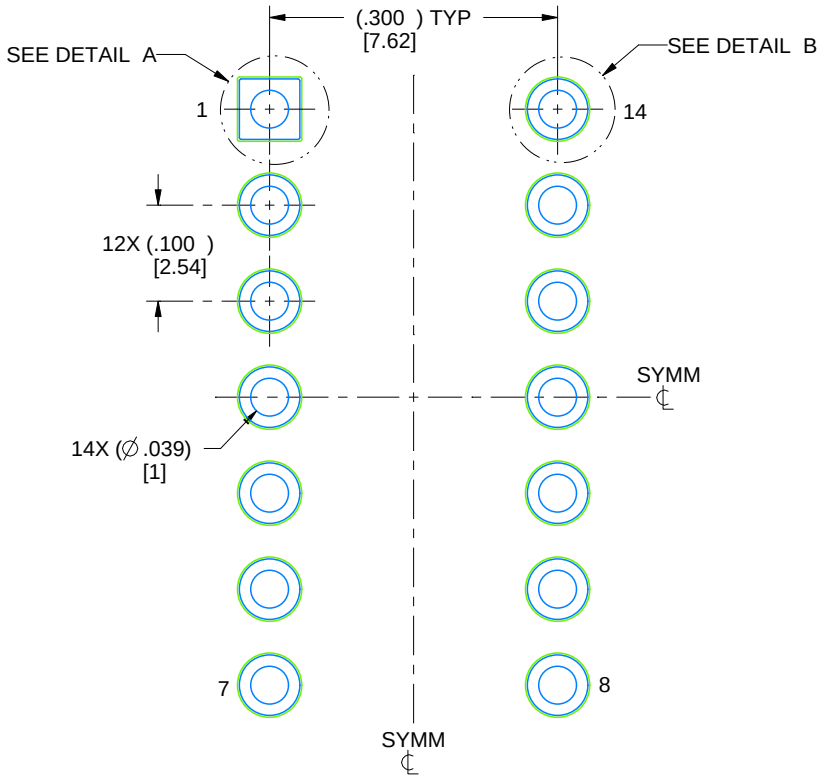
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

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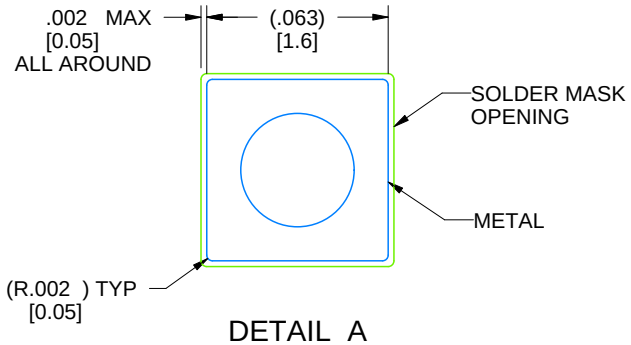
J0014A

CDIP - 5.08 mm max height

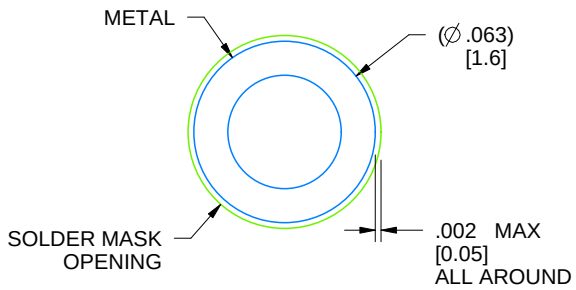
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

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