ZHEJIANG UNIU-NE Technology CO.,LTD

浙 江 宇 力 微 新 能 源 科 技 有 限 公 司

U3401/2 Data Sheet

V 1.2

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■ General Description

The U3401/2 600V synchronous buck controller regulates from a high input voltage source or from an input rail subject to high voltage transients, minimizing the need for external surge suppression components. A high-side switch minimum on-time of 60 ns gives large step-down ratios, enabling the direct step-down conversion from a 100V nominal input to low-voltage rails for reduced system complexity and solution cost. The U3401/2 continues to operate during input voltage dips as low as 16.5V, at nearly 100% duty cycle if needed, making it an excellent choice for high-performance 100V battery automotive applications, ADAS (surround view ECU) and HEV/EV systems.

Forced-PWM (FPWM) operation eliminates switching frequency variation to minimize EMI, while user-selectable diode emulation lowers current consumption at light-load conditions. Measuring the voltage drop across the low-side MOSFET or with an optional current sense resistor gives cycle-by-cycle overcurrent protection. The adjustable switching frequency as high as 0.5MHz can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications.

■ Applications

- High-Power Automotive DC/DC Regulator
- Automotive Motor Drives, ADAS
- HEV/EV Power Compliant to LV-148

■ Key Features

- AEC-Q100 Qualified for Automotive Applications:
  - ➢ Device Temperature Grade 1:–40°C to +125°C Ambient Temperature Range
- Versatile Synchronous Buck DC/DC Controller
  - ➢ Wide Input Voltage Range of 16.5V to 600V
  - ➢ Adjustable Output Voltage
  - ➢ Voltage-mode Control With Line Feedforward
- Meets CISPR 25 EMI Standard
- Lossless $R_{DS(on)}$ or Shunt Current Sensing
- Switching Frequency From 10 kHz to 0.5MHz
  - ➢ SYNC In and SYNC Out Capability
- 60ns Minimum On-Time for High V_{IN} / V_{OUT} Ratio
- 180ns Minimum Off-Time for Low Dropout
- 1.2V Reference With ± 1% Feedback Accuracy
- 8.5V Gate Drivers for Standard V_{TH} MOSFETs
  - ➢ 220ns Adaptive Dead-Time Control
  - ➢ 1.5A Source and 1.8A Sink Capability
  - ➢ Low-Side Soft Start for Prebiased Start-Up
- Adjustable Soft Start or Optional Voltage Tracking
- Precision Enable Input and Open-Drain Power- Good Indicator for Sequencing and Control
- Inherent Protection Features for Robust Design
  - ➢ Hiccup-Mode Overcurrent Protection
  - ➢ Input UVLO With Hysteresis
  - ➢ VCC and Gate-Drive UVLO Protection
  - ➢ Thermal Shutdown Protection With Hysteresis
- 16-Pin SOP Package With Wettable Flanks
- Create a Custom Design Using the U3401/2 With UNI-SEMI ® Power Designer

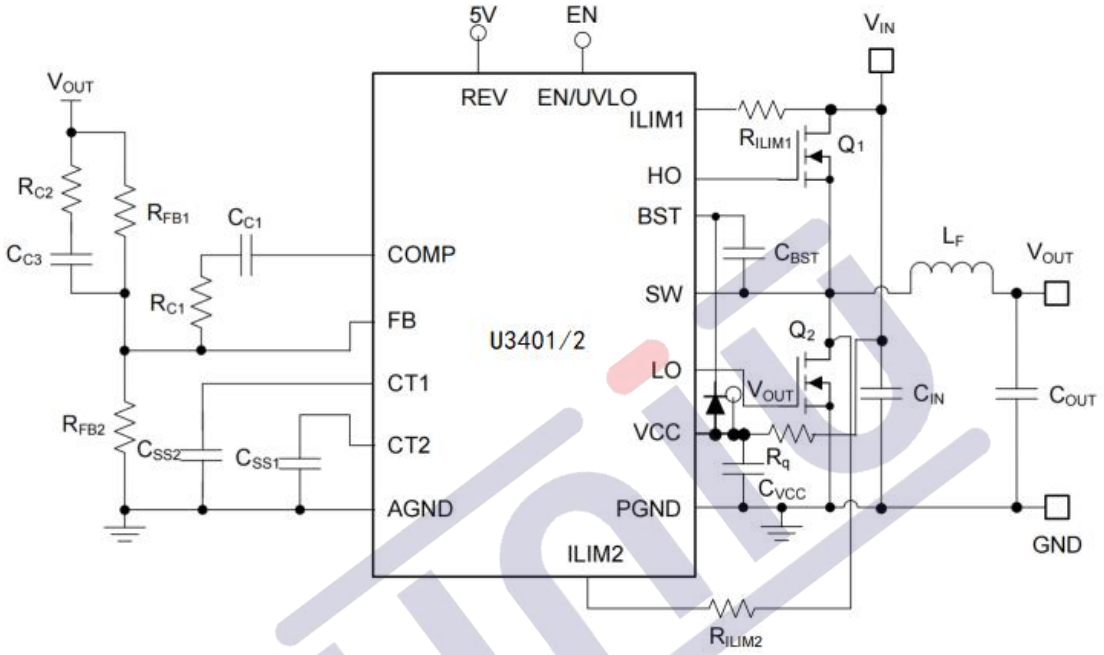
■ Device Information(1)

Part Number	Package	Body Size (Nom)
U3401/2	SOP(16)	10mm × 6.3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet

■ Typical Application Circuit and Efficiency Performance

V_{OUT} = 12 V, F_{SW} = 60kHz



■ Output Power Table

Part Number	Package	VIN	IO+/IO-	OUT
U3401	SOP-16	20~400V	1.5A/1.8A	ADJ
U3402	SOP-16	10~400V	1.5A/1.8A	ADJ

Note:

1.Default for Buck Converter Application

2.The practical output power is determined by the output voltage and thermal condition

■ Description (continued)

The U3401/2 voltage-mode controller with line feedforward drives external high-side and low-side N -channel power switches with robust 8.5V gate drivers suitable for standard-threshold MOSFETs. Adaptively-timed gate drivers with 1.5A source and 1.8A sink capability minimize body diode conduction during switching transitions, reducing switching losses and improving thermal performance when driving MOSFETs at high input voltage and high frequency. The U3401/2 can be powered from the output of the switching regulator or another available source, further improving efficiency.

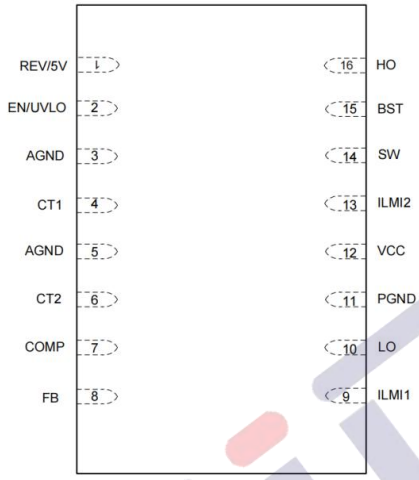
A 180° out-of-phase clock output relative to the internal oscillator at SYNCOUT works well for cascaded or multi-channel power supplies to reduce input capacitor ripple current and EMI filter size. Additional features of the U3401/2 include a configurable soft start, an open-drain power-good monitor for fault reporting and output-monitoring, monotonic start-up into prebiased loads, integrated VCC bias supply regulator and bootstrap diode, external power supply tracking, precision enable input with hysteresis for adjustable line undervoltage lockout (UVLO), hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

The U3401/2 controller is offered in a 10mm × 6.3mm thermally enhanced, 16-pin SOP package with additional spacing for high-voltage pins and wettable flanks for optical inspection of solder joint fillets.

■ Pin Configuration and Functions

RGY Package 16-Pin SOP With Wettable Flanks

Top View



Connect Exposed Pad on bottom to AGND and PGND on the PCB

■ Pin Functions

Pin		I/O(1)	Description
NO.	Name		
1	REV	O	the REV pin is nominally 0.8 V.
2	EN/UVLO	I	Enable input and undervoltage lockout programming pin. If the EN/UVLO voltage is below 0.4V, the controller is in the shutdown mode with all functions disabled. If the EN/UVLO voltage is greater than 0.4V and less than 1.2V, the regulator is in standby mode with the VCC regulator operational, the SS pin grounded, and no switching at the HO and LO outputs. If the EN/UVLO voltage is above 1.2V, the SS/TRK voltage can ramp and pulse-width modulated gate-drive signals are delivered to the HO and LO pins. A 10μA current source is enabled when EN/UVLO exceeds 1.2V and flows through the external UVLO resistor divider to provide hysteresis. Hysteresis can be adjusted by varying the resistance of the external divider.
3	AGND	P	Analog ground. Return for the internal 0.8V voltage reference and analog circuits.
4	CT1	I	Soft-start and voltage-tracking pin. An external capacitor and an internal 10μA current source set the ramp rate of the error amplifier reference during start-up. When the SS/TRK pin voltage is less than 1.2V, the SS/TRK voltage controls the noninverting input of the error amp. When the SS/TRK voltage exceeds 1.2V, the amplifier is controlled by the internal 1.2V reference. SS/TRK is discharged to ground during standby and fault conditions. After start-up, the SS/TRK voltage is clamped 115mV above the FB pin voltage. If FB falls due to a load fault, SS/TRK is discharged to a level 115mV above FB to provide a controlled recovery when the fault is removed. Voltage tracking can be implemented by connecting a low impedance reference between 0V and 1.2V to the SS/TRK pin. The 10μA SS/TRK charging current flows into the reference and produces a voltage error if the impedance is not low. Connect a minimum capacitance from SS/TRK to AGND of 1uF.

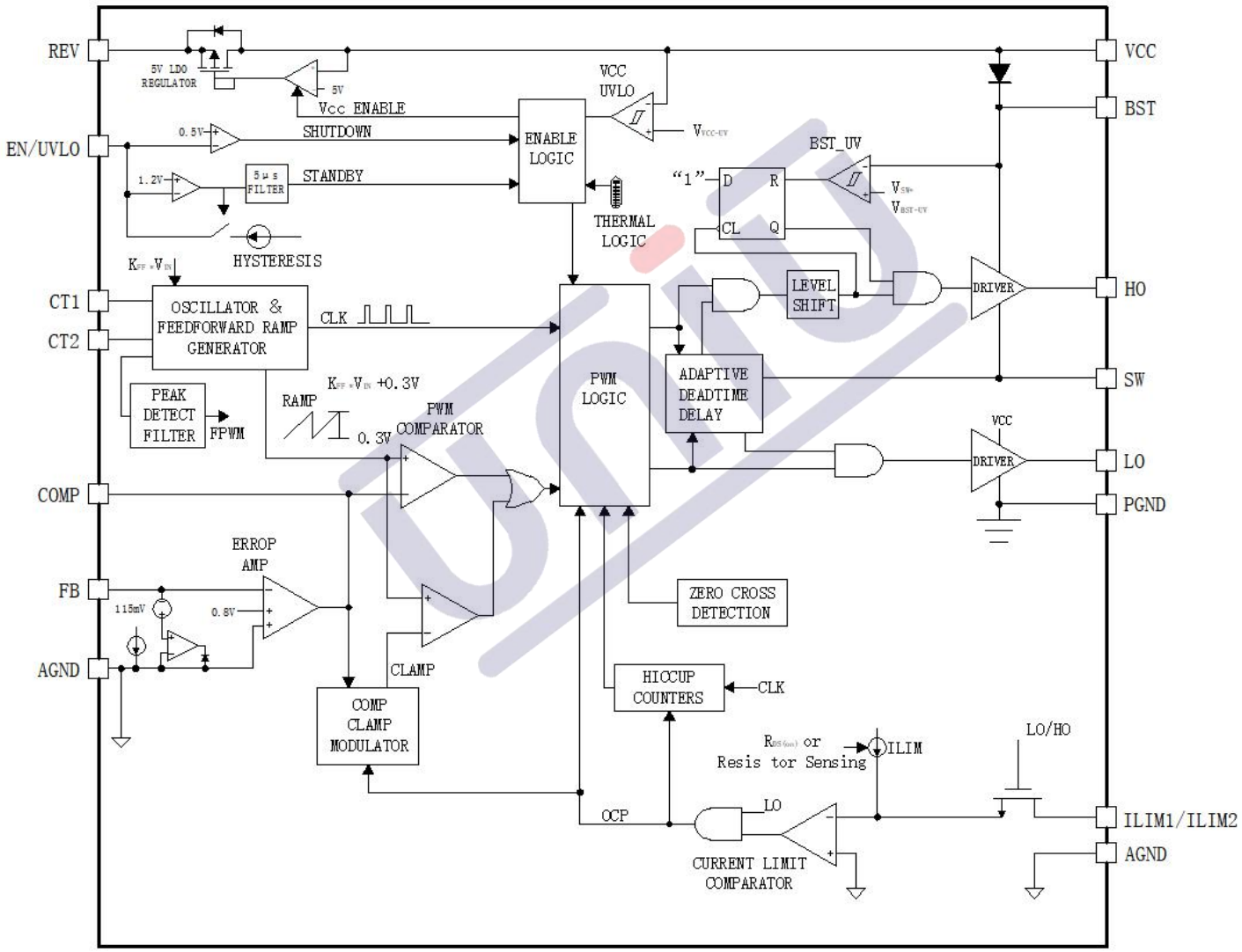
Pin		I/O(1)	Description
NO.	Name		
5	AGND	P	Analog ground. Return for the internal 0.8V voltage reference and analog circuits.
6	CT2	I	An external capacitor and an internal 18μA current source set the ramp rate of the error amplifier reference during start-up.
7	COMP	O	Low impedance output of the internal error amplifier. Connect the loop compensation network between the COMP pin and the FB pin.
8	FB	I	Feedback connection to the inverting input of the internal error amplifier. A resistor divider from the output to this pin sets the output voltage level. The regulation threshold at the FB pin is nominally 1.2V.
9	ILIM1	I	Current limit adjust and current sense comparator input. A current sourced from the ILIM pin through an external resistor programs the threshold voltage for valley current limiting. The opposite end of the threshold adjust resistor can be connected to either the drain of the low-side MOSFET for $R_{DS(on)}$ sensing or to a current sense resistor connected to the source of the low-side FET.
10	LO	P	Low-side MOSFET gate drive output. Connect to the gate of the low-side synchronous rectifier FET through a short, low inductance path.
11	PGND	P	Power ground return pin for the low-side MOSFET gate driver. Connect directly to the source of the low- side MOSFET or the ground side of a shunt resistor.
12	VCC	O	Output of the 8.5V bias regulator. Locally decouple to PGND using a low ESR/ESL capacitor located as close as possible to the controller. Controller bias can be supplied from an external supply that is greater than the internal VCC regulation voltage. Use caution when applying external bias to ensure that the applied voltage is not greater than the minimum VIN voltag·e and does not exceed the VCC pin maximum operating rating, see Recommended Operating Conditions
13	ILIM2	I	Current limit adjust and current sense comparator input. A current sourced from the ILIM pin through an external resistor programs the threshold voltage for valley current limiting. The opposite end of the threshold adjust resistor can be connected to either the drain of the low-side MOSFET for $R_{DS(on)}$ sensing or to a current sense resistor connected to the source of the low-side FET.
14	SW	P	Switching node of the buck controller. Connect to the bootstrap capacitor, the source terminal of the high- side MOSFET and the drain terminal of the low-side MOSFET using short, low inductance paths.
15	BST	O	Bootstrap supply for the high-side gate driver. Connect to the bootstrap (boot) capacitor. The bootstrap capacitor supplies current to the high-side FET gate and must be placed as close as possible to controller. If an external bootstrap diode is used to reduce the time required to charge the bootstrap capacitor, connect the cathode of the diode to the BST pin and anode to VCC.
16	HO	P	High-side MOSFET gate drive output. Connect to the gate of the high-side MOSFET through a short, low inductance path.

(1) P = Power, G = Ground, I = Input, O = Output.

■ Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required to meet requirements for high reliability and robustness. Standard quad-flat no-lead (SOP16) packages do not have solderable or exposed pins and terminals that are easily viewed. It is therefore difficult to visually determine whether or not the package is successfully soldered onto the printed-circuit board (PCB). The wettable-flank process was developed to resolve the issue of side-lead wetting of leadless packaging. The U3401/2 is assembled using a 16-pin SOP package with wettable flanks to provide a visual indicator of solderability, which reduces the inspection time and manufacturing costs.

■ Functional Block Diagram



■ Specifications

● Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1).

Item		Min	Max	Unit
Input voltages	VIN	-0.3	600	V
	SW	-1	600	
	SW (20ns transient)	-5	600	
	ILIM	0	600	
	EN/UVLO	-0.3	20	
	VCC	-0.3	20	
	FB, COMP	-0.3	6	
	CT1	-0.3	14	
Output voltages	BST	-0.3	612	V
	BST to VCC	–	600	
	BST to SW	-0.3	20	
	VCC to BST (20ns transient)	–	7	
	LO (20ns transient)	-3	–	
	REV	-0.3	7	
Operating junction temperature, T_J		–	150	°C
Storage temperature, T_{stg}		-55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

● ESD Ratings

Item		Description		Value	Unit
V_{ESD}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B		±500	
				±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

● Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1).

Item				Min	Nom	Max	Unit
V_I	Input voltages	VIN	U3401	24	—	400	V
			U3402	10	—	400	
		SW		-1	—	400	
		ILIM		0	—	400	
		External VCC bias rail		8	—	13	
		EN/UVLO		-0.3	—	12	
V_O	Output voltages	BST		-0.3	—	412	V
		BST to VCC		—	—	400	
		BST to SW		13	—	22	
		REV		—	—	5	
I_{SINK}, I_{SRC}	Sink/source currents	EN/UVLO		-1	—	1	mA
		CT1		—	—	2	
T_J	Operating junction temperature			–40	—	150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.

● Thermal Information

Item	Thermal Metric(1)	U3401/2 RGY (SOP) 16 PINS	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

● Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the -40°C to 150°C junction temperature range unless otherwise stated. V_{IN} = 48 V, $V_{EN/UVLO}$ = VCC, unless otherwise stated (1)(2).

Item	Parameter	Test Conditions		Min	Typ	Max	Unit
Input Supply							
V_{IN}	Operating input voltage range	I_{VCC} ≤ 10mA at V_{VIN} =24V	U3401	24	—	400	V
		I_{VCC} ≤ 10mA at V_{VIN} =10V	U3402	10	—	400	V
I_{Q-RUN}	Operating input current, not switching	$V_{EN/UVLO}$= 10V,		—	1.8	2.1	mA
I_{Q-STBY}	Standby input current	$V_{EN/UVLO}$= 10V		—	1.75	2	mA
I_{Q-SDN}	Shutdown input current	$V_{EN/UVLO}$= 0V, V_{VCC} < 1V		—	13.5	30	μA
REV/VCC Regulator							
V_{REV}	REV regulation voltage	V_{CT1} = 0 V, 24V ≤ V_{VIN} ≤ 100V, 0 mA < I_{VCC} ≤ 20 mA		—	5	—	V
I_{SC-LDO}	REV short-circuit current	VREV = 0 V VCC=12V		—	50	—	mA
V_{VCC-UV}	VCC undervoltage threshold	V_{VCC} rising	U3401	—	15	—	V
			U3402		8.5		
$V_{VCC-UVH}$	VCC undervoltage hysteresis	Rising threshold – falling threshold 3401		—	5	—	V
		Rising threshold – falling threshold 3402			0.8		
$V_{VCC-EXT}$	Maxmum external bias supply voltage	Voltage required to disable VCC regulator		—	—	24	V
I_{VCC}	External REV input current, not switching	V_{EN} = 10V, V_{VCC} = 13 V		—	—	2.3	mA
Enable And Input UVLO							
V_{SDN}	Shutdown to standby threshold	$V_{EN/UVLO}$ rising		—	0.5	—	V
$V_{SDN-HYS}$	Shutdown threshold hysteresis	EN/UVLO rising – falling threshold		—	0.2	—	V
V_{EN}	Standby to operating threshold	$V_{EN/UVLO}$ rising		—	1.2	—	V
I_{EN-HYS}	Standby to operating hysteresis	$V_{EN/UVLO}$ = 1.5 V		9	10	11	μA
Error Amplifier							
V_{REF}	FB reference voltage	FB connected to COMP		—	1200	—	mV
$I_{FB-BIAS}$	FB input bias current	VFB=1.2V	–40°C≤T_J≤125°C	—	—	0.1	μA
			–40°C≤T_J≤150°C	—	—	0.2	μA
$V_{COMP-OH}$	COMP output high voltage	V_{FB} = 0V, COMP sourcing 1 mA		—	5	—	V
$V_{COMP-OL}$	COMP output low voltage	COMP sinking 1 mA		—	—	0.3	V
AVOL	DC gain			—	94	—	dB
GBW	Unity gain bandwidth			—	5	—	MHz
Soft-Start And Voltage Tracking							
I_{SS}	CT1 capacitor charging current	$V_{SS/TRK}$ = 0V		8.5	10	12	μA
R_{SS}	CT1 discharge FET resistance	$V_{EN/UVLO}$ = 1V, $V_{SS/TRK}$ = 0.1V		—	11	—	Ω
V_{SS-FB}	CT1 to FB offset			-15	—	15	mV
$V_{SS-CLAMP}$	CT1 clamp voltage	$V_{SS/TRK}$ – V_{FB} , V_{FB} = 0.8V		—	115	—	mV

● Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated. V_{IN} = 48 V, $V_{EN/UVLO}$ = VCC, unless otherwise stated(1)(2).

Item	Parameter	Test Conditions	Min	Typ	Max	Unit
Oscillator						
F_{SW1}	Oscillator Frequency – 1	CT2 = 100 PF	—	60	—	kHz
F_{SW2}	Oscillator Frequency – 2	CT2 = 200 PF	—	30	—	kHz
F_{SW3}	Oscillator Frequency – 3	CT2 = 300 PF	—	15	—	kHz
Bootstrap Diode And Undervoltage Threshold						
$V_{BST-FWD}$	Diode forward voltage, VCC to BST	VCC to BST, BST pin sourcing 20 mA	—	0.75	0.9	V
I_{Q-BST}	BST to SW quiescent current, not switching	$V_{SS/TRK}$=0V,V_{SW}=48V,V_{BST}=54V	—	80	—	μA
V_{BST-UV}	BST to SW undervoltage detection	V_{BST} – V_{SW} falling	—	3.4	—	V
$V_{BST-HYS}$	BST to SW undervoltage hysteresis	V_{BST} – V_{SW} rising	—	0.42	—	V
PWM Control						
$t_{ON(MIN)}$	Minimum controllable on-time	V_{BST} – V_{SW} = 7 V, HO 50% to 50%	—	40	60	ns
$t_{OFF(MIN)}$	Minimum off-time	V_{BST} – V_{SW} = 7 V, HO 50% to 50%	—	140	200	ns
DC_{100kHz}	Maximum duty cycle	F_{SW} = 100 kHz, 6 V ≤ V_{VIN} ≤ 60 V	98%	99%	—	—
DC_{400kHz}		F_{SW} = 400 kHz, 6 V ≤ V_{VIN} ≤ 60 V	90%	94%	—	—
$V_{RAMP(min)}$	Ramp valley voltage (COMP at 0% duty cycle)		—	300	—	mV
K_{FF}	PWM feedforward gain (V_{IN} / V_{RAMP})	6 V ≤ V_{VIN} ≤ 100 V	—	15	—	V/V
Overcurrent Protect (OCP) – Valley Current Limiting						
I_{RS}	ILIM source current, R_{SENSE} mode	Low voltage detected at ILIM	90	100	110	μA
I_{RDSON}	ILIM source current, $R_{DS(on)}$ mode	SW voltage detected at ILIM, T_J=25°C	180	200	220	μA
I_{RSTC}	ILIM current tempco	R_{DS-ON} mode	—	4500	—	ppm/°C
$I_{RDSONTC}$	ILIM current tempco	R_{SENSE} mode	—	0	—	ppm/°C
$V_{ILIM-TH}$	ILIM comparator threshold at ILIM		—	–200	—	mV
Short-Circuit Protect (SCP) – Duty Cycle Clamp						
$V_{CLAMP-OS}$	Clamp offset voltage – no current limiting	CLAMP to COMP steady state offset voltage	0.2 + V_{VIN}/75			V
$V_{CLAMP-MIN}$	Minimum clamp voltage	CLAMP voltage with continuous current limiting	0.3 + V_{VIN}/150			V
Hiccup Mode Fault Protection						
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycles with current limiting before hiccup off-time activated	128			cycles
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycles with no switching followed by SS/TRK release	8192			cycles

● Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated. V_{IN} = 48 V, $V_{EN/UVLO}$ = VCC, unless otherwise stated (1)(2).

Item	Parameter	Test Conditions	Min	Typ	Max	Unit
Diode Emulation						
V_{ZCD-SS}	Zero-cross detect (ZCD) soft-start ramp	ZCD threshold measured at SW pin 50 clock cycles after first HO pulse	—	0	—	mV
$V_{ZCD-DIS}$	Zero-cross detect disable threshold (CCM)	ZCD threshold measured at SW pin 1000 clock cycles after first HO pulse	—	200	—	mV
V_{DEM-TH}	Diode emulation zero-cross threshold	Measured at SW with V_{SW} rising	–5	0	5	mV
Gate Drivers						
R_{HO-UP}	HO high-state resistance, HO to BST	$V_{BST} – V_{SW}$ = 7V, I_{HO} = – 100 mA	—	1.5	—	Ω
$R_{HO-DOWN}$	HO low-state resistance, HO to SW	$V_{BST} – V_{SW}$ = 7V, I_{HO} = 100 mA	—	0.9	—	Ω
R_{LO-UP}	LO high-state resistance, LO to VCC	$V_{BST} – V_{SW}$ = 7V, I_{LO} = – 100 mA	—	1.5	—	Ω
$R_{LO-DOWN}$	LO low-state resistance, LO to PGND	$V_{BST} – V_{SW}$ = 7V, I_{LO} = 100 mA	—	0.9	—	Ω
I_{HOH} , I_{LOH}	HO, LO source current	$V_{BST} – V_{SW}$ = 7V, HO = SW, LO = AGND	—	2.3	—	A
IH_{OL}, I_{LOL}	HO, LO sink current	$V_{BST} – V_{SW}$ = 7 V, HO = BST, LO =VCC	—	3.5	—	A
Thermal Shutdown						
T_{SD}	Thermal shutdown threshold	T_J rising	—	175	—	°C
T_{SD-HYS}	Thermal shutdown hysteresis		—	20	—	°C

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \cdot R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in Thermal Information.

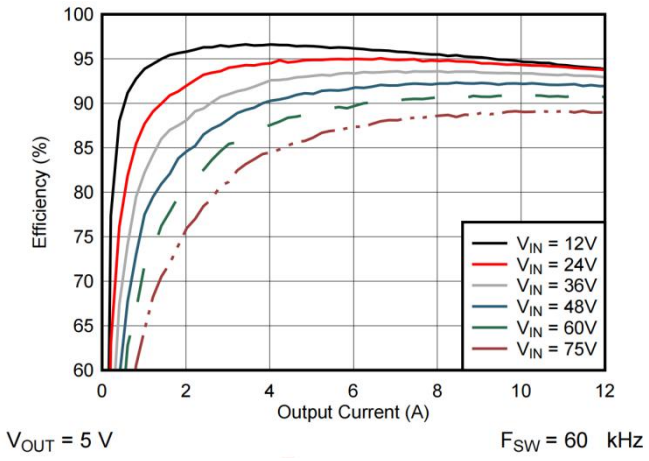
● Switching Characteristics

Typical values correspond to T_J = 25°C

Item	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{HO-TR} T_{LO-TR}	HO, LO rise times	$V_{BST} – V_{SW}$ = 7 V, C_{LOAD} = 1 nF, 20% to 80%	—	7	—	ns
T_{HO-TF} T_{LO-TF}	HO, LO fall times	$V_{BST} – V_{SW}$ = 7 V, C_{LOAD} = 1 nF, 80% to 20%	—	4	—	ns
T_{HO-DT}	HO turn-on dead time	$V_{BST} – V_{SW}$ = 7 V, LO off to HO on, 50% to 50%	—	14	—	ns
T_{LO-DT}	LO turn-on dead time	$V_{BST} – V_{SW}$ = 7 V, HO off to LO on, 50% to 50%	—	14	—	ns

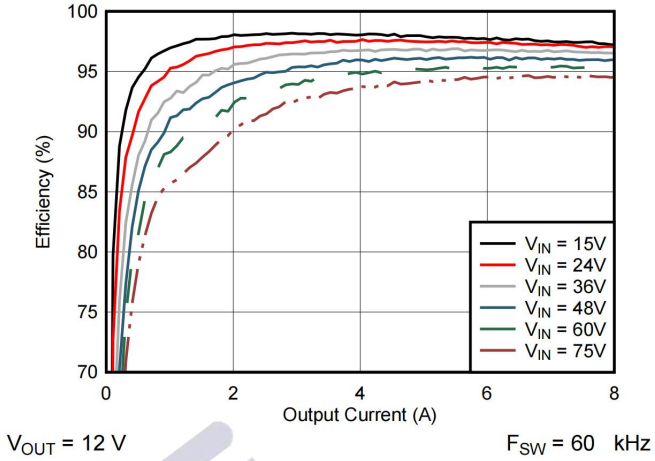
● Typical Characteristics

V_{VIN} = 48 V, EN/UVLO tied to VCC (unless otherwise noted).



V_{OUT} = 5 V F_{SW} = 60 kHz

Figure 1. Efficiency vs Load, CCM



V_{OUT} = 12 V F_{SW} = 60 kHz

Figure 2. Efficiency vs Load, CCM

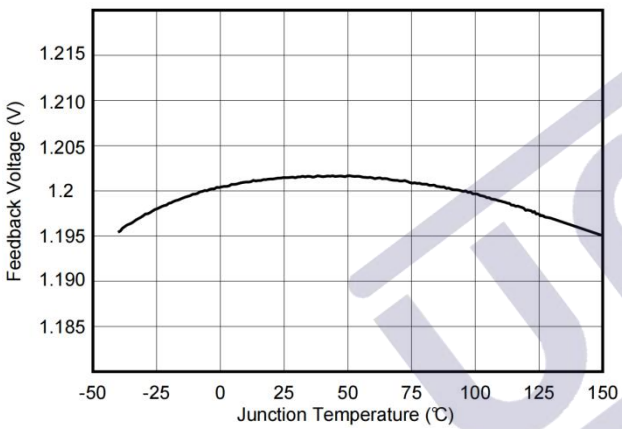


Figure 3. FB Voltage vs Junction Temperature

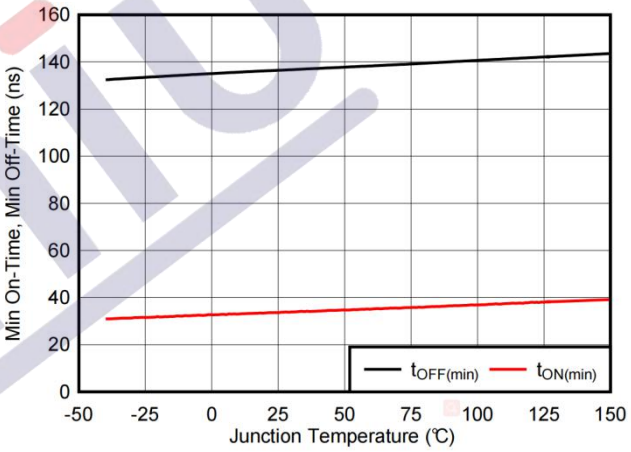
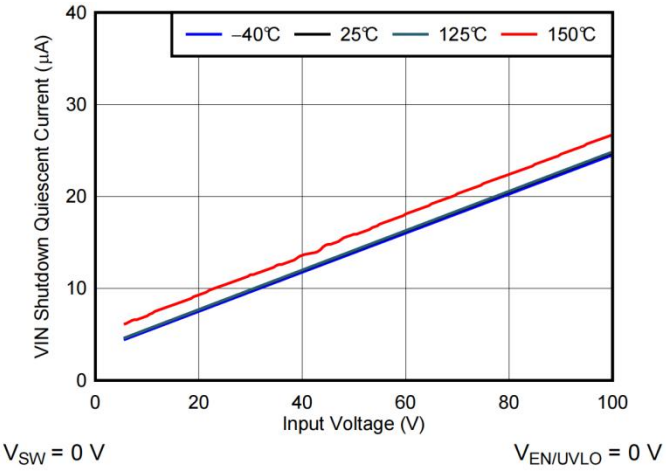
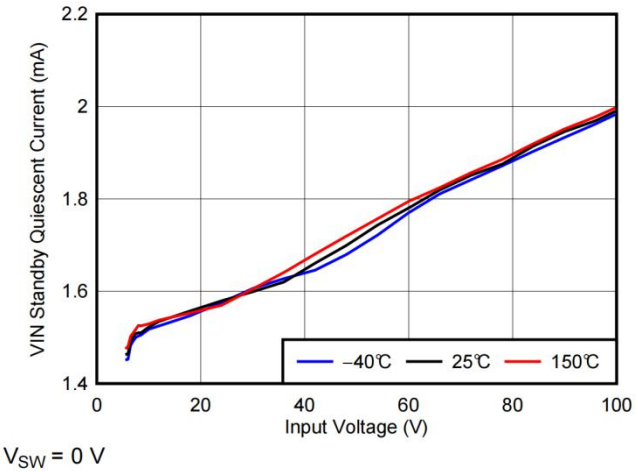


Figure 4. $t_{ON(min)}$ and $t_{OFF(min)}$ vs Junction Temperature



V_{SW} = 0 V $V_{EN/UVLO}$ = 0 V

Figure 5. $I_{Q\text{-}SHD}$ vs Input Voltage



V_{SW} = 0 V

Figure 6. $I_{Q\text{-}STANDBY}$ vs Input Voltage

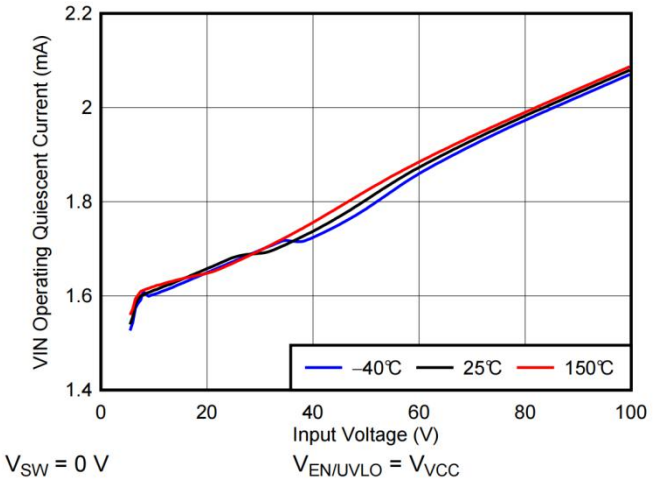


Figure 7. $I_{Q\text{-}OPERATING}$ (Non-switching) vs Input Voltage

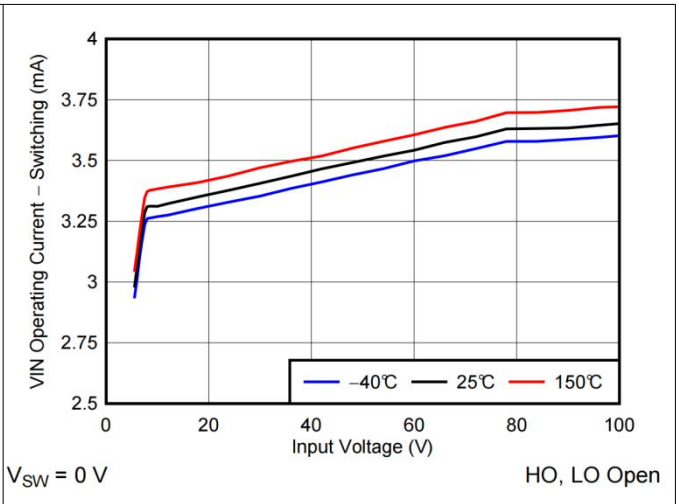


Figure 8. $I_{Q\text{-}OPERATING}$ (Switching) vs Input Voltage

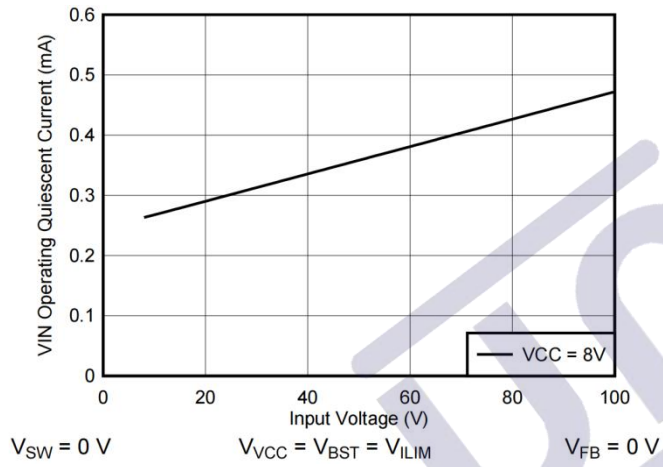


Figure 9. VIN Quiescent Current With External VCC Applied

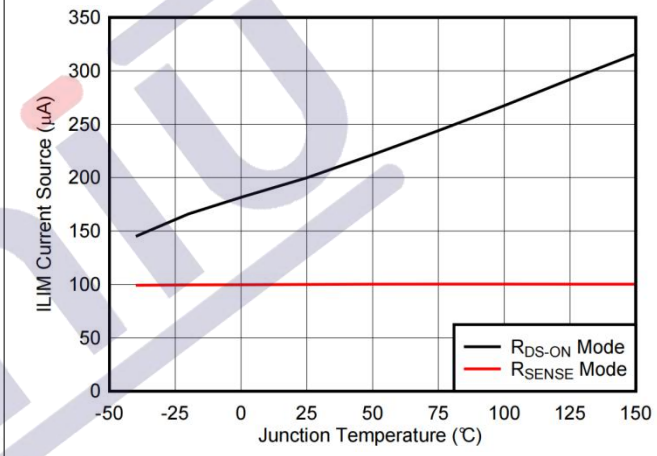


Figure 10. ILIM Current Source vs Junction Temperature

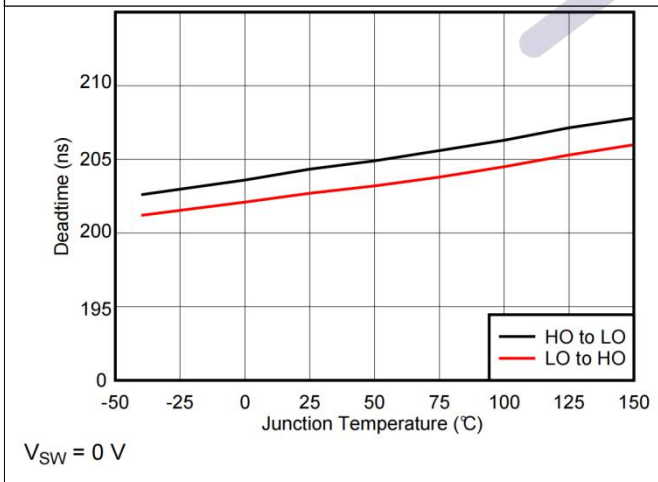


Figure 11. Deadtime vs Junction Temperature

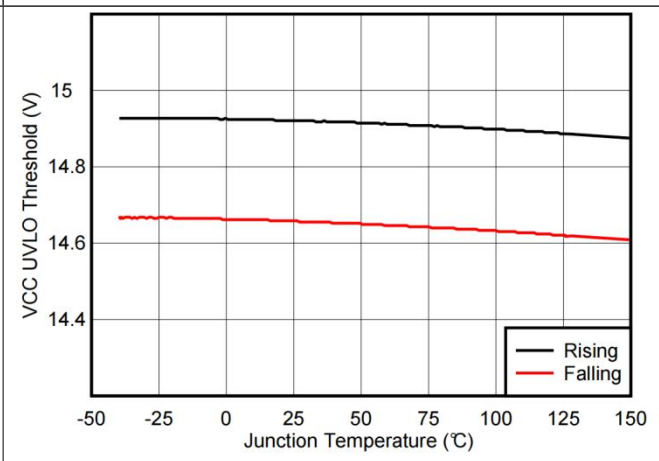


Figure 12. VCC UVLO Thresholds vs Junction Temperature

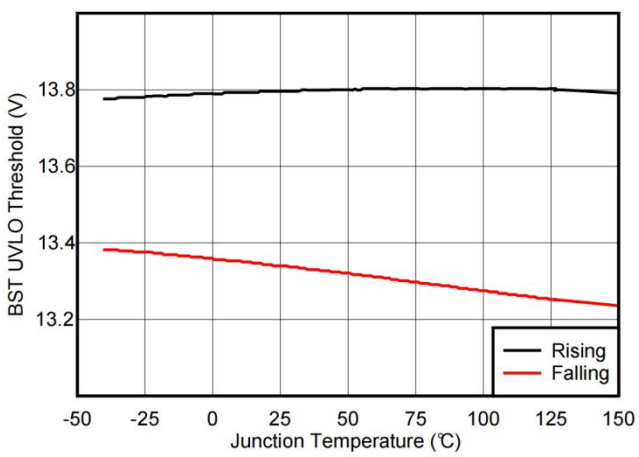


Figure 13. BST UVLO Thresholds vs Junction Temperature

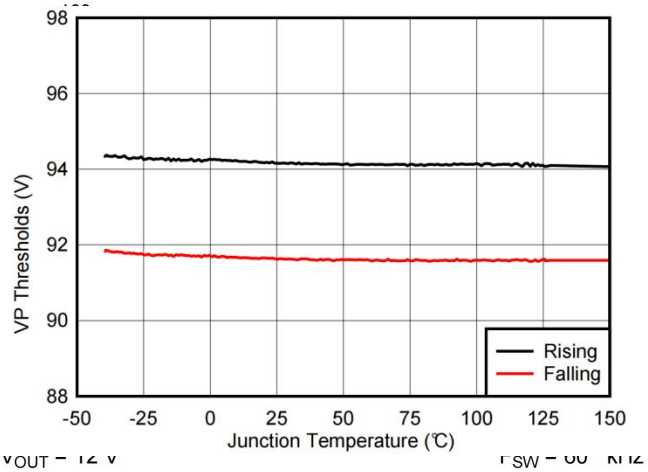


Figure 14. PGOOD UVP Thresholds vs Junction Temperature

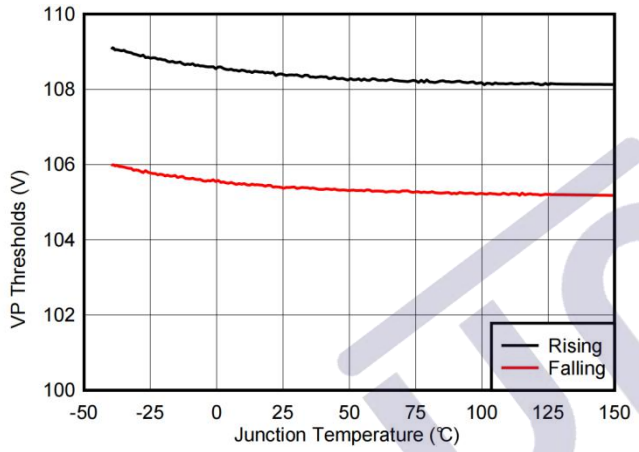


Figure 15. PGOOD OVP Thresholds vs Junction Temperature

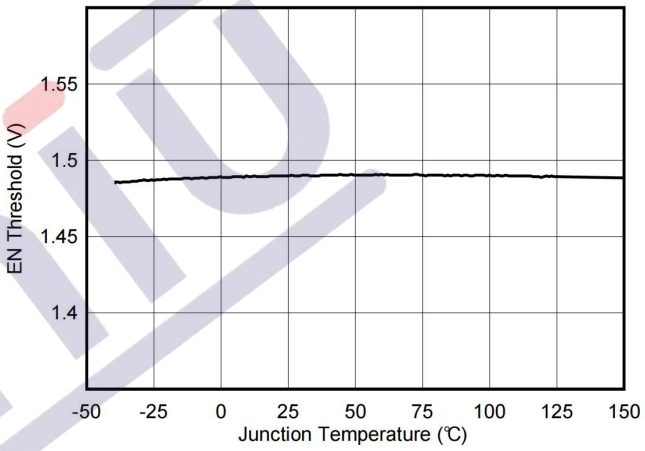


Figure 16. EN/UVLO Threshold vs Junction Temperature

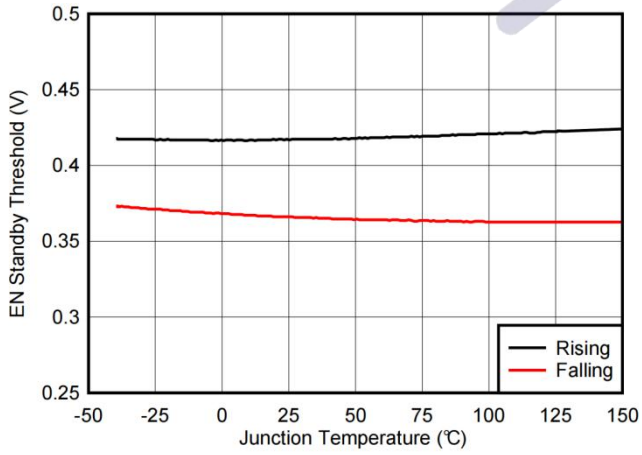


Figure 17. EN Standby Thresholds vs Junction Temperature

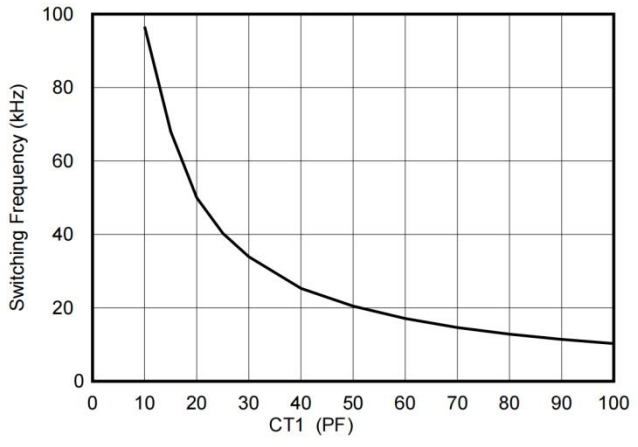
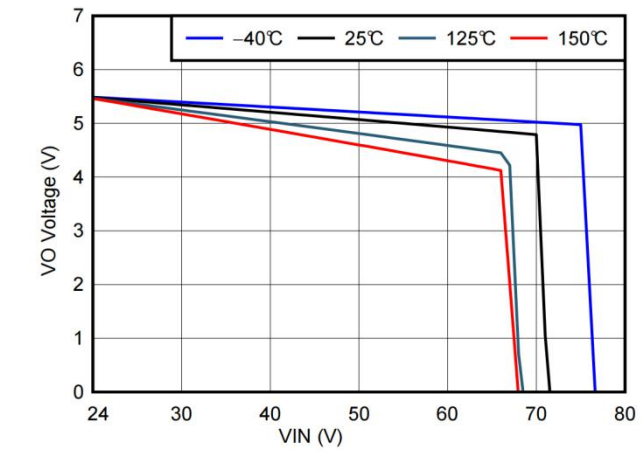
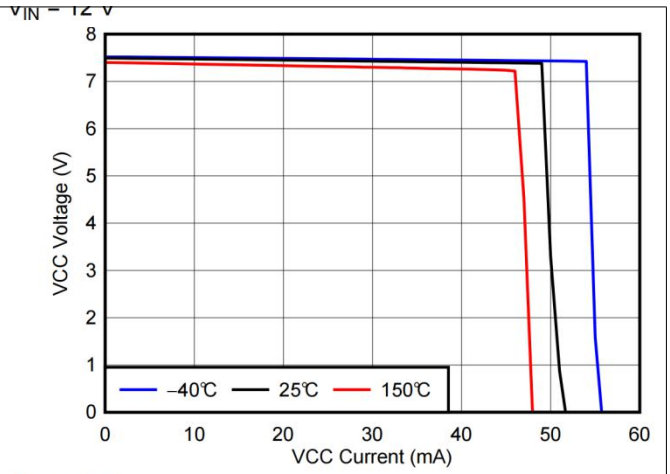


Figure 18. Oscillator Frequency vs RT Resistance



V_O = 5.5 V

Figure 25. VCC vs ICC Characteristic



V_{IN} = 12 V

Figure 26. VCC vs ICC Characteristic

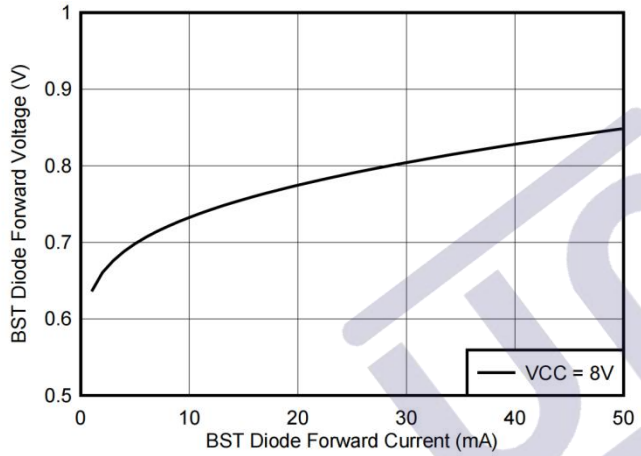


Figure 27. BST Diode Forward Voltage vs Current

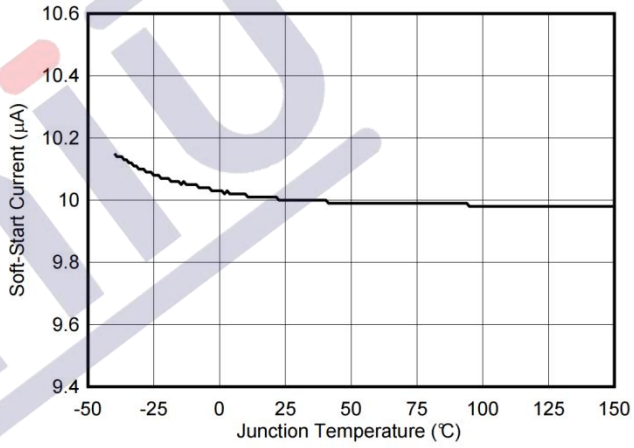


Figure 28. SS/TRK Current Source vs Junction Temperature

■ Detailed Description

● Overview

The U3401/2 is a 600V synchronous buck controller with all of the functions necessary to implement a high efficiency step-down power supply. The output voltage range is from 1.5V to 100V. The voltage-mode control architecture uses input feedforward for excellent line transient response over a wide V_{IN} range. Voltage-mode control supports the wide duty cycle range for high input voltage and low dropout applications as well as when a high voltage conversion ratio (for example, 10 to 1) is required. Current sensing for cycle-by-cycle current limit can be implemented with either the low-side FET $R_{DS(on)}$ or a current sense resistor. The operating frequency is programmable from 10kHz to 0.5MHz. The U3401/2 drives external high-side and low-side NMOS power switches with robust 12V gate drivers suitable for standard threshold MOSFETs. Adaptive dead-time control between the high-side and low-side drivers minimizes body diode conduction during switching transitions. An external bias supply can be connected to the VCC pin to improve efficiency in high-voltage applications. A user-selectable diode emulation feature enables DCM operation for improved efficiency and lower dissipation at light-load conditions.

● Feature Description

◆ Input Range (V_{IN})

The U3401/2 operational input voltage range is from 24V（10V） to 400V. The device is intended for step-down conversions from 12V, 24V, 48V, 60V and 72V unregulated, semiregulated, and fully-regulated supply rails. The application circuit of Figure 29 shows all the necessary components to implement an U3401/2 based wide-V_{IN} step-down regulator using a single supply. The U3401/2 uses an internal LDO subregulator to provide a 12V VCC bias rail for the gate drive and control circuits.

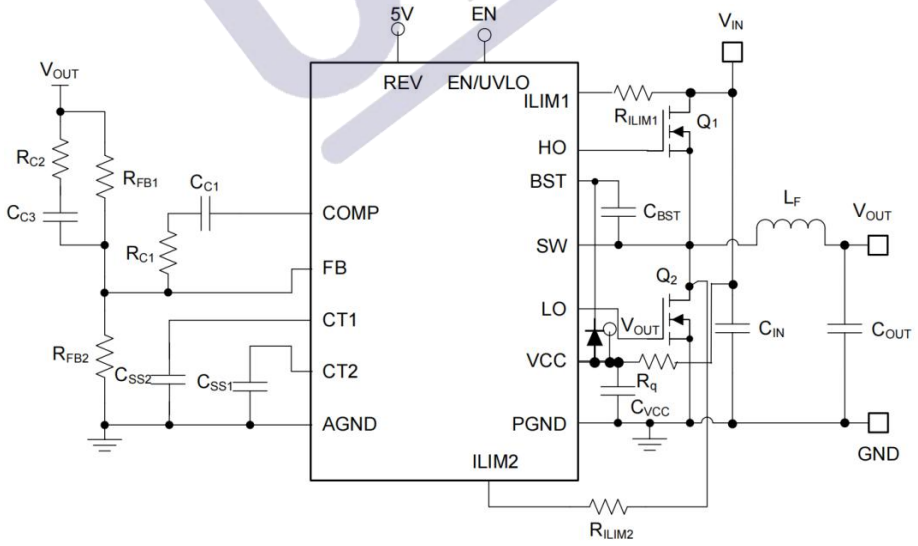


Figure 29. Schematic Diagram for VIN Operating Range of 24V(10V) to 400V

In high voltage applications, take extra care to ensure the V_{IN} pin does not exceed the absolute maximum voltage rating of 400V during line or load transient events. Voltage ringing on the V_{IN} pin that exceeds the Absolute Maximum Ratings can damage the IC. Use high-quality ceramic input capacitors to minimize ringing. An RC filter from the input rail to the V_{IN} pin (for example, 4.7Ω and 0.1μF) provides supplementary filtering at the V_{IN} pin.

◆ Output Voltage Setpoint and Accuracy (FB)

The reference voltage at the FB pin is set at 1.2V with a feedback system accuracy over the full junction temperature range of ±1%. Junction temperature range for the device is –40°C to +125°C. While dependent on switching frequency and load current levels, the U3401/2 is generally capable of providing output voltages in the range of 1.2V to a maximum of slightly less than V_{IN} . The DC output voltage setpoint during normal operation is set by the feedback resistor network, R_{FB1} and R_{FB2} , connected to the output.

◆ High-Voltage Bias Supply Regulator (VCC)

The U3401/2 contains an internal high-voltage VCC regulator that provides a bias supply for the PWM controller and its gate drivers for the external MOSFETs. The input pin (V_{IN}) can be connected directly to an input voltage source up to 400V. The output of the VCC regulator is set to 12V. However, when the input voltage is below the VCC setpoint level, the VCC output tracks V_{IN} with a small voltage drop. Connect a ceramic decoupling capacitor between 1μF and 5μF from VCC to AGND for stability. .

The VCC regulator output has a current limit of 14mA (minimum). At power up, the regulator sources current into the capacitor connected to the VCC pin. When the VCC voltage exceeds its rising UVLO threshold of 16V, the output is enabled (if EN/UVLO is above 1.5V), and the soft-start sequence begins. The output remains active until the VCC voltage falls below its falling UVLO threshold of 12V (typical) or if EN/UVLO goes to a standby or shutdown state.

Internal power dissipation of the VCC regulator can be minimized by connecting the output voltage or an auxiliary bias supply rail (up to 20V) to VCC using a diode D_{VCC} as shown in Figure 30. A diode in series with the input prevents reverse current flow from VCC to V_{IN} if the input voltage falls below the external VCC rail.

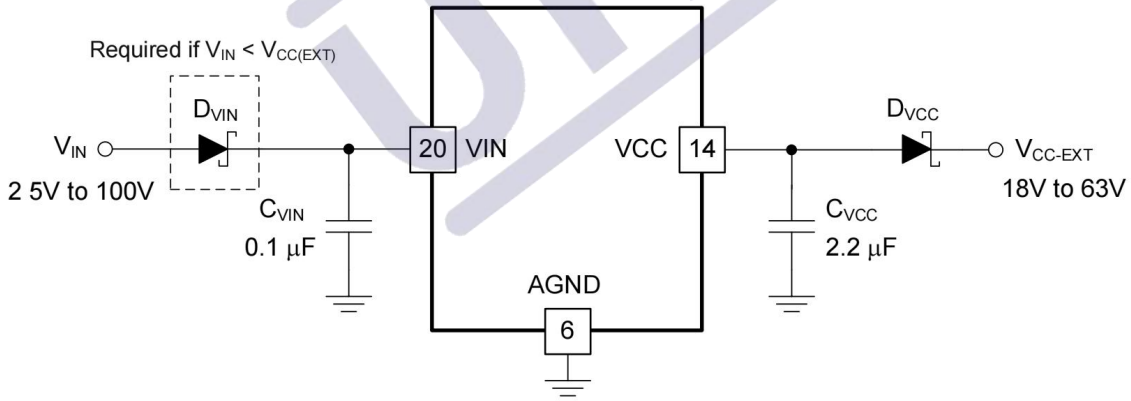


Figure 30. VCC Bias Supply Connection From VOUT or Auxiliary Supply

Note that a finite bias supply regulator dropout voltage exists and is manifested to a larger extent when driving high gate charge (Q_G) power MOSFETs at elevated switching frequencies. For example, at V_{VIN}=60V, the VCC voltage is 12V with a DC operating current, I_{VCC}, of 10mA. Such a low gate drive voltage may be insufficient to fully enhance the power MOSFETs. At the very least, MOSFET on-state resistance, $R_{DS(ON)}$, may increase at such low gate drive voltage.

◆ Precision Enable (EN/UVLO)

The EN/UVLO input supports adjustable input undervoltage lockout (UVLO) with hysteresis programmed by the resistor values for application specific power-up and power-down requirements. EN/UVLO connects to a comparator-based input referenced to a 1.5V bandgap voltage. An external logic signal can be used to drive the EN/UVLO input to toggle the output ON and OFF and for system sequencing or protection. The simplest way to enable the operation of the U3401/2 is to connect EN/UVLO directly to V_{IN}. This allows self start-up of the U3401/2 when V_{CC} is within its valid operating range. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2} as shown in Figure 31 to establish a precision UVLO level.

Use Equation 1 and Equation 2 to calculate the UVLO resistors given the required input turn-on and turn-off voltages.

$$R_{UV1} = \frac{V_{IN(on)} - V_{IN(off)}}{I_{HYS}} \quad (1)$$

$$R_{UV2} = R_{UV1} \times \frac{V_{EN}}{V_{IN(on)} - V_{EN}} \quad (2)$$

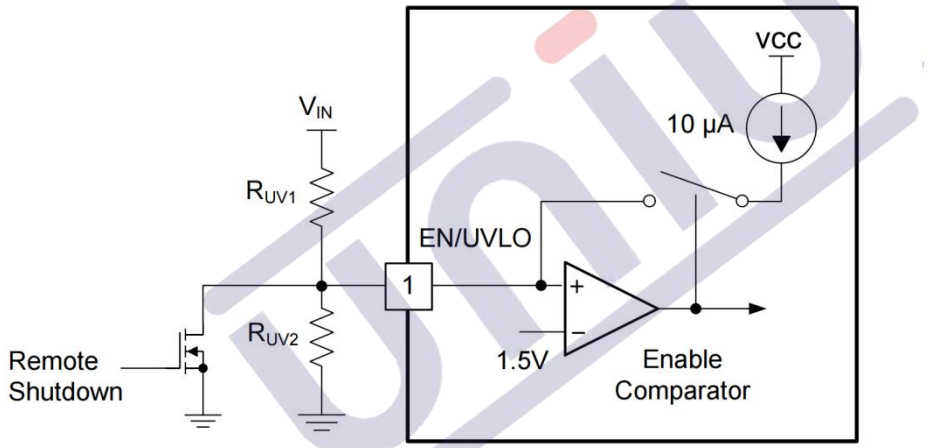


Figure 31. Programmable Input Voltage UVLO Turn-on and Turn-off

The U3401/2 enters a low I_Q shutdown mode when EN/UVLO is pulled below approximately 0.8V. The internal LDO regulator powers off and the internal bias supply rail collapses, shutting down the bias currents of the U3401/2. The U3401/2 operates in standby mode when the EN/UVLO voltage is between the hard shutdown and precision enable (standby) thresholds.

◆ Voltage-Mode Control (COMP)

The U3401/2 incorporates a voltage-mode control loop implementation with input voltage feedforward to eliminate the input voltage dependence of the PWM modulator gain. This configuration allows the controller to maintain stability throughout the entire input voltage operating range and provides for optimal response to input voltage transient disturbances. The constant gain provided by the controller greatly simplifies loop compensation design because the loop characteristics remain constant as the input voltage changes, unlike a buck converter without voltage feedforward. An increase in input voltage is matched by a concomitant increase in ramp voltage amplitude to maintain constant modulator gain. The input voltage feedforward gain, k_{FF} , is 15, equivalent to the input voltage divided by the ramp amplitude, V_{IN}/V_{RAMP} . See Control Loop Compensation for more detail.

◆ Gate Drivers (LO, HO)

The U3401/2 gate driver impedances are low enough to perform effectively in high output current applications where large die-size or paralleled MOSFETs with correspondingly large gate charge, Q_G , are used. Measured at V_{VCC} =12V, the low-side driver of the has a low impedance pulldown path of 15Ω to minimize the effect of dv/dt induced turn-on, particularly with low gate-threshold voltage MOSFETs. Similarly, the high-side driver has 15Ω and 12Ω pullup and pulldown impedances, respectively, for faster switching transition times, lower switching loss, and greater efficiency.

The high-side gate driver works in conjunction with an integrated bootstrap diode and external bootstrap capacitor, C_{BST} . When the low-side MOSFET conducts, the SW voltage is approximately at 0V and C_{BST} is charged from VCC through the integrated boot diode. Connect a 0.1μF or larger ceramic capacitor close to the BST and SW pins.

Furthermore, there is a proprietary adaptive dead-time control on both switching edges to prevent shoot-through and cross-conduction, minimize body diode conduction time, and reduce body diode reverse recovery losses.

◆ Current Sensing and Overcurrent Protection (ILIM)

The U3401/2 implements a lossless current sense scheme designed to limit the inductor current during an overload or short-circuit condition. Figure 36 portrays the popular current sense method using the on-state resistance of the low-side MOSFET. Meanwhile, Figure 37 shows an alternative implementation with current shunt resistor, R_S . The U3401/2 senses the inductor current during the PWM off-time (when LO is high).

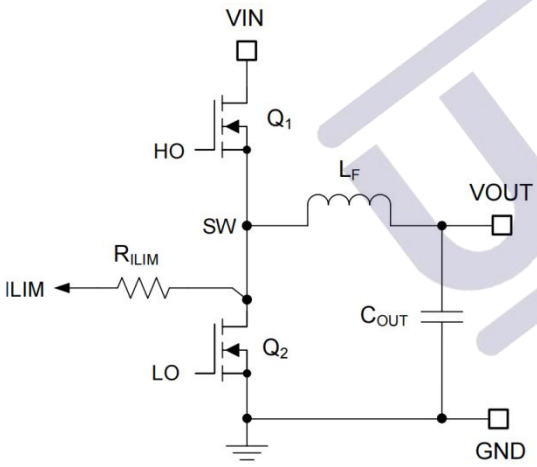


Figure 36. MOSFET $R_{DS(on)}$ Current Sensing

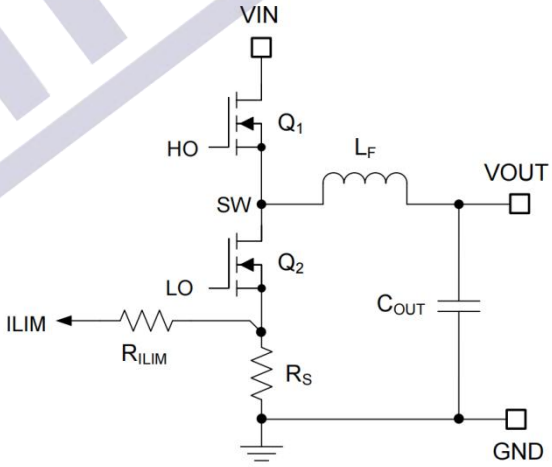


Figure 37. Shunt Resistor Current Sensing

The ILIM pin of the U3401/2 sources a reference current that flows in an external resistor, designated R_{ILIM} , to program of the current limit threshold. A current limit comparator on the ILIM pin prevents further SW pulses if the ILIM pin voltage goes below GND. Figure 38 shows the implementation.

Resistor R_{ILIM} is tied to SW to use the $R_{DS(on)}$ of the low-side MOSFET as a sensing element (termed $R_{DS(on)}$ mode). Alternatively, R_{ILIM} is tied to a shunt resistor connected at the source of the low-side MOSFET (termed R_{SENSE} mode). The U3401/2 detects the appropriate mode at start-up and sets the source current amplitude and temperature coefficient (TC) accordingly.

The ILIM current with R_{DS-ON} sensing is 200μA at 27°C junction temperature and incorporates a TC of +4500 ppm/ °C to generally track the $R_{DS(on)}$ temperature variation of the low-side MOSFET. Conversely, the ILIM current is a constant 100μA in R_{SENSE} mode. This controls the valley of the inductor current during a steady-state overload at the output. Depending on the chosen mode, select the resistance of R_{ILIM} using Equation 6.

$$R_{ILIM} = \begin{cases} \dfrac{I_{OUT} - \Delta I_L / 2}{I_{RDSON}} \times R_{DS(on)Q2}, & R_{DS(on)} \text{ sensing} \\ \dfrac{I_{OUT} - \Delta I_L / 2}{I_{RS}} \times R_S, & \text{Shunt,sensing} \end{cases}$$

Where:ΔI_L is the peak-to-peak inductor ripple current

$R_{DS(on)Q2}$ is the on-state resistance of the low-side MOSFET

I_{RDSON} is the ILIM pin current in R_{DS-ON} mode

R_S is the resistance of the current-sensing shunt element, and

I_{RS} is the ILIM pin current in R_{SENSE} mode. (6)

Given the large voltage swings of ILIM in $R_{DS(on)}$ ensing mode, a capacitor designated C_{ILIM} connected from ILIM to PGND is essential to the operation of the valley current limit circuit. Choose this capacitance such that the time constant $R_{ILIM} \cdot C_{ILIM}$ is approximately 60ns.

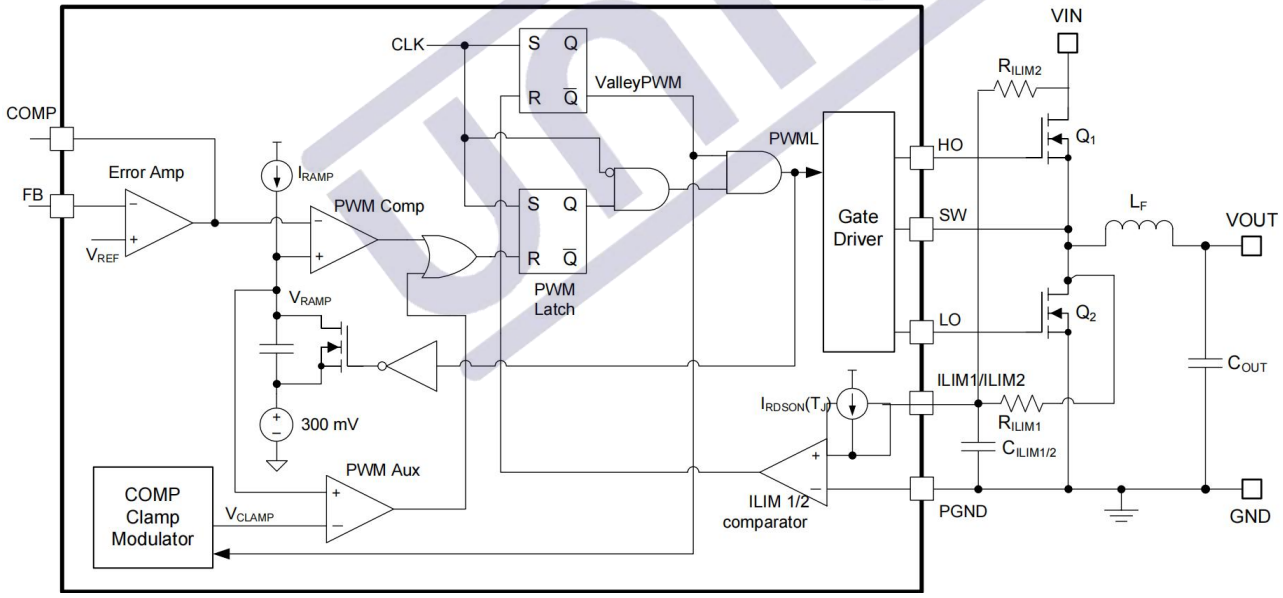


Figure 38. OCP Setpoint Defined by Current Source I_{RDSON} and Resistor R_{ILIM} in R_{DS-ON} Mode

Note that current sensing with a shunt component is typically implemented at lower output current levels to provide accurate overcurrent protection. Burdened by the unavoidable efficiency penalty, PCB layout, and additional cost implications, this configuration is not usually implemented in high-current applications (except where OCP setpoint accuracy and stability over the operating temperature range are critical specifications).

◆ OCP Duty Cycle Limiter

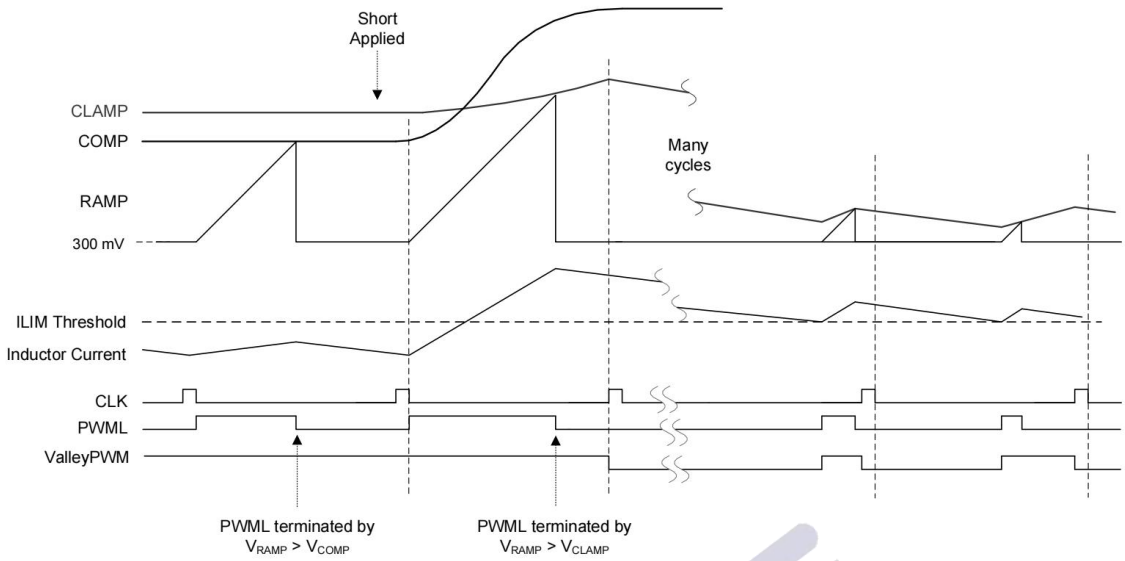


Figure 39. OCP Duty Cycle Limiting Waveforms

In addition to valley current limiting, the U3401/2 uses a proprietary duty-cycle limiter circuit to reduce the PWM on-time during an overcurrent condition. As shown in Figure 38, an auxiliary PWM comparator along with a modulated CLAMP voltage limits how quickly the on-time increases in response to a large step in the COMP voltage that typically occurs with a voltage-mode control loop architecture.

As depicted in Figure 39, the CLAMP voltage, V_{CLAMP} , is normally regulated above the COMP voltage to provide adequate headroom during a response to a load-on transient. If the COMP voltage rises quickly during an overloaded or shorted output condition, the on-time pulse terminates thereby limiting the on-time and peak inductor current. Moreover, the CLAMP voltage is reduced if additional valley current limit events occur, further reducing the average output current.

If the overcurrent condition exists for 128 continuous clock cycles, a hiccup event is triggered and SS is pulled low for 8192 clock cycles before a soft-start sequence is initiated.

● Device Functional Modes

◆ Shutdown Mode

The EN/UVLO pin provides ON / OFF control for the U3401/2. When the EN/UVLO voltage is below 0.8V (typical), the device is in shutdown mode. Both the internal bias supply LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 13.5μA (typical) at V_{IN} = 48V. The U3401/2 also includes undervoltage protection of the internal bias LDO. If the internal bias supply voltage is below its UVLO threshold level, the switching regulator remains off.

◆ Standby Mode

The internal bias supply LDO has a lower enable threshold than the switching regulator. When the EN/UVLO voltage exceeds 1.5V (typical) and is below the precision enable threshold (1.5V typically), the internal LDO is on and regulating. Switching action and output voltage regulation are disabled in standby mode.

◆ Diode Emulation Mode

The U3401/2 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation, the low-side MOSFET is switched off when reverse current flow is detected by sensing of the SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss at no-load and light-load conditions, the disadvantage being slower light-load transient response.

◆ Thermal Shutdown

The U3401/2 includes an internal junction temperature monitor. If the temperature exceeds 155°C (typical), thermal shutdown occurs.

When entering thermal shutdown, the device:

1.Turns off the high-side and low-side MOSFETs.

2.Pulls PIN3 low.

3.Turns off the VCC regulator.

4.Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 20°C (typical).

This is a non-latching protection, and, as such, the device will cycle into and out of thermal shutdown if the fault persists

■ Application and Implementation

● Application Information

◆ Design and Implementation

To expedite the process of designing of a U3401/2 based regulator for a given application, use the U3401/2 Quickstart Calculator available as a free download, as well as numerous U3401/2 reference designs populated in UNIDesigns™ reference design library, or the designs provided in Typical Applications. The U3401/2 is also WEBENCH® Designer enabled.

◆ Pow Train Componentser

Comprehensive knowledge and understanding of the power train components are key to successfully completing a synchronous buck regulator design.

1) Inductor

For most applications, choose an inductance such that the inductor ripple current, ΔI_L , is between 30% and 40% of the maximum DC output current at nominal input voltage. Choose the inductance using Equation 7 based on a peak inductor current given by Equation 8.

$$L_F = \frac{V_{OUT}}{V_{IN}} \times \left(\frac{V_{IN} - V_{OUT}}{\Delta I_L \times F_{SW}} \right) \quad (7)$$

$$I_{L(\text{peak})} = I_{OUT} + \frac{\Delta I_L}{2} \quad (8)$$

Check the inductor datasheet to ensure that the saturation current of the inductor is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as its core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

2) Output Capacitors

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics—equivalent series resistance (ESR) and equivalent series inductance (ESL)—take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT} , filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT} , choose an output capacitance that is larger than that given by Equation 9.

$$C_{OUT} \geq \frac{\Delta I_L}{8F_{SW}\sqrt{\Delta V_{OUT}{}^2 - \left(R_{ESR} \times \Delta I_L\right)^2}} \quad (9)$$

Figure 40 conceptually illustrates the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as rapidly as possible during and after the load step- up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

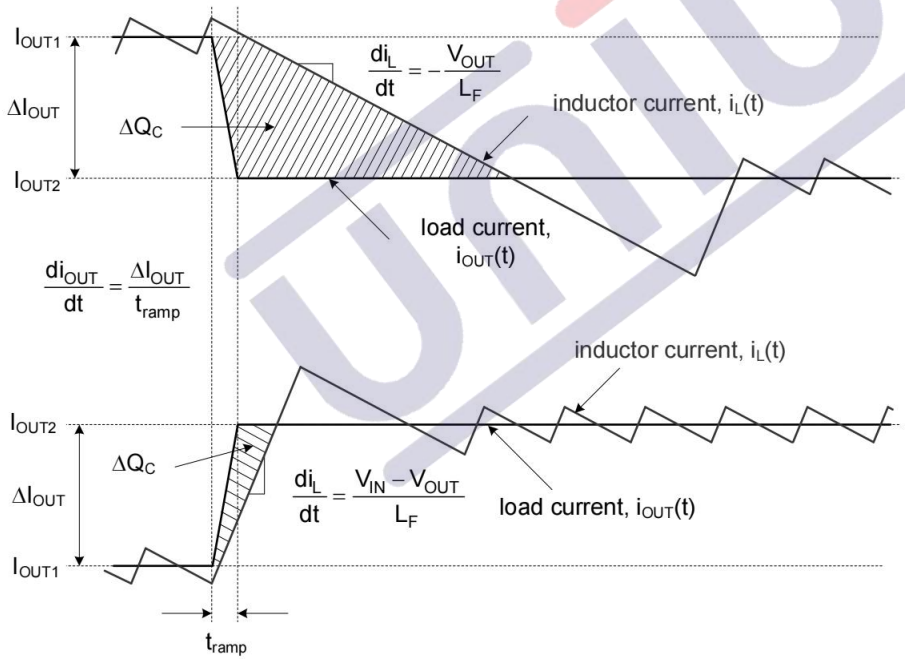


Figure 40. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 48V input to low output voltage (for example, 5V), the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 10% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT}/L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below its nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and limit the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance should be larger than

$$C_{OUT} \geq \frac{L_F \times \Delta I_{OUT}^{\ 2}}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^{\ 2}} \quad (10)$$

The ESR of a capacitor is provided in the manufacturer's data sheet either explicitly as a specification or implicitly in the impedance vs. frequency curve. Depending on type, size and construction, electrolytic capacitors have significant ESR, 5mΩ and above, and relatively large ESL, 5nH to 20nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors, on the other hand, have low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in Equation 9 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. One to four 47μF, 10V, X7R capacitors in 1206 or 1210 footprint is a common choice. Use Equation 10 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with its low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with its large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

3) Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X5R or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. The input capacitor RMS current is given by Equation 11.

$$I_{CIN,rms} = \sqrt{D \times \left(I_{OUT}^{\ 2} \times (1-D) + \frac{\Delta I_L^{\ 2}}{12}\right)} \quad (11)$$

The highest input capacitor RMS current occurs at D=0.5, at which point the RMS current rating of the capacitors should be greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sinks I_{IN} during the 1− D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak ripple voltage

amplitude is given by Equation 12.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR} \quad (12)$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN} , is given by Equation 13.

$$C_{IN} \geq \frac{D \times (1-D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR} \times I_{OUT})} \quad (13)$$

Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and two or three 2.2μF 100V X7R ceramic decoupling capacitors are usually sufficient. Select the input bulk capacitor based on its ripple current rating and operating temperature.

4) Power MOSFETs

The choice of power MOSFETs has significant impact on DC-DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and output charge (Q_G and Q_{OSS} respectively), and vice versa. As a result, the product $R_{DS(on)} \times Q_G$ is commonly specified as a MOSFET figure-of-merit. Low thermal resistance ensures that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection in a U3401/2 application are as follows:

a. $R_{DS(on)}$ at V_{GS} = 12V.

b. Drain-source voltage rating, BV_{DSS} , typically 60V, 80V or 100V, depending on maximum input voltage.

c. Gate charge parameters at V_{GS} = 12V.

d. Output charge, Q_{OSS} , at the relevant input voltage.

e. Body diode reverse recovery charge, Q_{RR} .

f. Gate threshold voltage, $V_{GS(th)}$, derived from the Miller plateau evident in the Q_G vs. V_{GS} plot in the MOSFET data sheet. With a Miller plateau voltage typically in the range of 12Vto 15V, the 12V gate drive amplitude of the U3401/2 provides an adequately-enhanced MOSFET when on and a margin against Cdv/dt shoot-through when off.

The MOSFET-related power losses are summarized by the equations presented in Table 2, where suffixes 1 and 2 represent high-side and low-side MOSFET parameters, respectively. While the influence of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances and SW node ringing, are not included. Consult the U3401/2 Quickstart Calculatorto assist with power loss calculations.

Table 2. Buck Regulator MOSFET Power Losses

POWER LOSS MODE	High-Side MOSFET	Low-Side MOSFET
MOSFET conduction(1)(2)	$P_{cond1} = D \times (I_{OUT}^{\ 2} + \frac{\Delta I_L^{\ 2}}{12}) \times R_{DS(on)1}$	$P_{cond2} = D' \times (I_{OUT}^{\ 2} + \frac{\Delta I_L^{\ 2}}{12}) \times R_{DS(on)2}$
MOSFET switching	$P_{SW1} = V_{IN} \times F_{SW} \left[(I_{OUT} - \frac{\Delta I_L}{2}) \times t_R + (I_{OUT} + \frac{\Delta I_L}{2}) \times t_F \right]$	Negligible
MOSFET gate drive(3)	$P_{Gate1} = V_{CC} \times F_{SW} \times Q_{G1}$	$P_{Gate2} = V_{CC} \times F_{SW} \times Q_{G2}$
MOSFET Output charge(4)	$P_{COSS} = F_{SW} \times (V_{IN} \times Q_{OSS2} + E_{OSS1} - E_{OSS2})$	
Body diode conduction	N/A	$P\text{cond}_{BD} = V_F \times F_{SW} \left[(I_{OUT} + \frac{\Delta I_L}{2}) \times t_{dt1} + (I_{OUT} - \frac{\Delta I_L}{2}) \times t_{dt2} \right]$
Body diode reverse recovery(5)	$P_{RR} = V_{IN} \times F_{SW} \times Q_{RR2}$	

(1)MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4500 ppm/ °C. The MOSFET junction temperature, T_J , and its rise over ambient temperature is dependent upon the device total power dissipation and its thermal impedance. When operating at or near minimum input voltage, ensure that the MOSFET $R_{DS(on)}$ is rated at V_{GS} = 12V.

(2)D' = 1– D is the duty cycle complement.

(3)Gate drive loss is apportioned based on the internal gate resistance of the MOSFET, externally-added series gate resistance and the relevant driver resistance of the U3401/2.

(4)MOSFET output capacitances, C_{oss1} and C_{oss2} , are highly non-linear with voltage. These capacitances are charged losslessly by the inductor current at high-side MOSFET turn-off. During turn-on, however, a current flows from the input to charge the output capacitance of the low-side MOSFET. E_{oss1} , the energy of C_{oss1} , is dissipated at turn-on, but this is offset by the stored energy E_{oss2} on C_{oss2} .

(5)MOSFET body diode reverse recovery charge, Q_{RR} , depends on many parameters, particularly forward current, current transition speed and temperature.

The high-side (control) MOSFET carries the inductor current during the PWM on-time (or D interval) and typically incurs most of the switching losses. It is therefore imperative to choose a high-side MOSFET that balances conduction and switching loss contributions. The total power dissipation in the high-side MOSFET is the sum of the losses due to conduction, switching (voltage-current overlap), output charge, and typically two-thirds of the net loss attributed to body diode reverse recovery.

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or 1–D interval). The low-side MOSFET switching loss is negligible as it is switched at zero voltage – current just commutates from the channel to the body diode or vice versa during the transition deadtimes. The U3401/2, with its adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

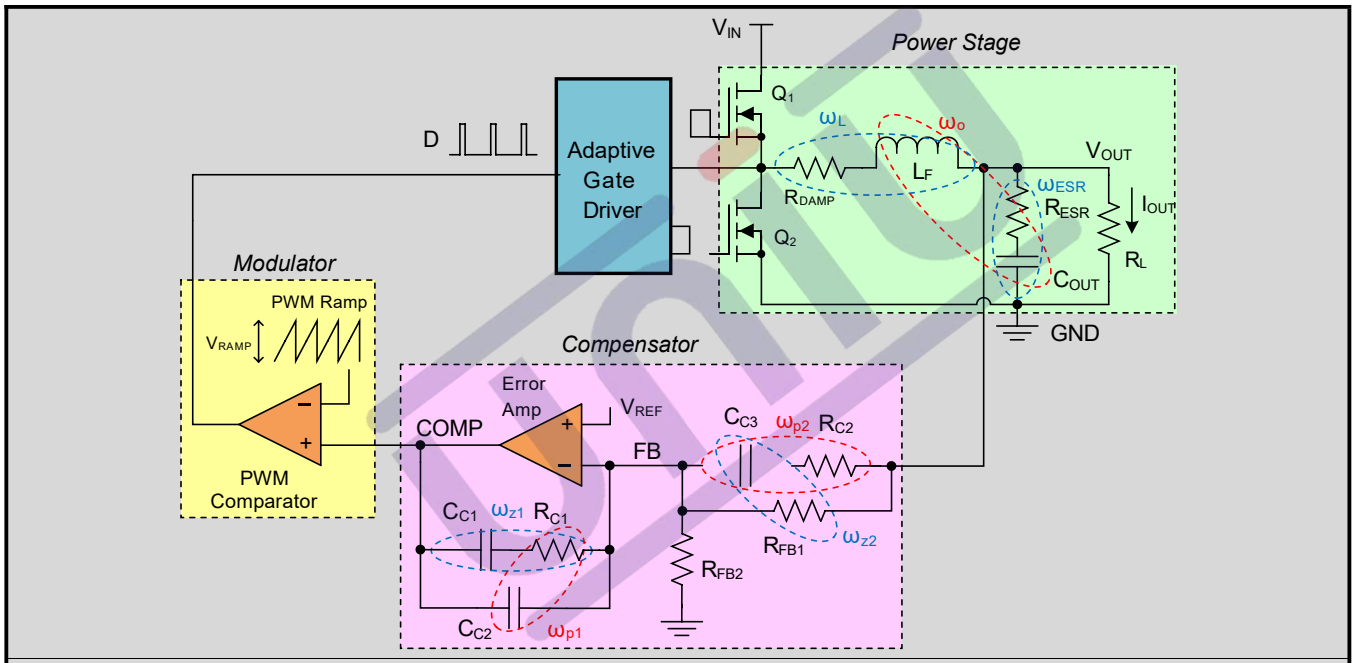
In high step-down ratio applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, it is critical to optimize the low-side MOSFET for low $R_{DS(on)}$. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery. The U3401/2 is well suited to drive TI's portfolio of NexFET™ power MOSFETs.

◆ Control Loop Compensation

The poles and zeros inherent to the power stage and compensator are respectively illustrated by red and blue dashed rings in the schematic embedded in Table 3.

The compensation network typically employed with voltage-mode control is a Type-III circuit with three poles and two zeros. One compensator pole is located at the origin to realize high DC gain. The normal compensation strategy uses two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero, with the remaining compensator pole located at one-half switching frequency to attenuate high frequency noise. The resistor divider network to FB determines the desired output voltage. Note that the lower feedback resistor, R_{FB2} , has no impact on the control loop from an AC standpoint because the FB node is the input to an error amplifier and is effectively at AC ground. Hence, the control loop is designed irrespective of output voltage level. The proviso here is the necessary output capacitance derating with bias voltage and temperature.

Table 3. Buck Regulator Poles and Zeros (1)(2)



Power Stage Poles	Power Stage Zeros	Compensator Poles	Compensator Zeros
$\omega_O = \frac{1}{\sqrt{L_F \times C_{OUT} \times (\frac{1+R_{ESR}/R_L}{1+R_{ESR}/R_{DAMP}})}}$	$\omega_{ESR} = \frac{1}{R_{ESR} \times C_{OUT}}$	$\omega_{P1} = \frac{1}{R_{C1} \times (C_{C1} // C_{C2})} \cong \frac{1}{R_{C1} \times C_{C2}}$	$\omega_{Z1} = \frac{1}{R_{C1} \times C_{C1}}$
$\cong \frac{1}{\sqrt{L_F \times C_{OUT}}}$	$\omega_L = \frac{L_F}{R_{DAMP}}$	$\omega_{P2} = \frac{1}{R_{C2} \times C_{C3}}$	$\omega_{Z2} = \frac{1}{(R_{FB2} \times R_{C2}) \times C_{C3}}$

(1) R_{ESR} represents the ESR of the output capacitor C_{OUT} .

(2) $R_{DAMP} = D \times R_{DS(on)high\text{-}side} + (1- D) \times R_{DS(on)low\text{-}side} + R_{DCR}$, shown as a lumped element in the schematic, represents the effective series damping resistance.

The small-signal open-loop response of a buck regulator is the product of modulator, power train and compensator transfer functions. The power stage transfer function can be represented as a complex pole pair associated with the output LC filter and a zero related to the ESR of the output capacitor. The DC (and low frequency) gain of the modulator and power stage is V_{IN}/V_{RAMP} . The gain from COMP to the average voltage at the input of the

LC filter is held essentially constant by the PWM line feedforward feature of the U3401/2 (15V/V or 23.5 dB).

Complete expressions for small-signal frequency analysis are presented in Table 4. The transfer functions are denoted in normalized form. While the loop gain is of primary importance, a regulator is not specified directly by its loop gain but by its performance related characteristics, namely closed-loop output impedance and audio susceptibility.

Table 4. Buck Regulator Small-Signal Analysis

Transfer Function	Expression
Open-loop transfer function	$T_V(s)=\frac{\hat{V}_{comp}(s)}{\hat{V}_O(s)}\times\frac{\hat{V}_O(s)}{\hat{d}(s)}\times\frac{\hat{d}(s)}{\hat{V}_{comp}(s)}=G_C(s)\times G_{Vd}(s)\times F_M$
Duty-cycle-to-output transfer function	$G_{vd}(s)=\left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right\vert_{\substack{\hat{v}_{in}(s)=0\\ \hat{i}_o(s)=0}}=V_{IN}\frac{1+\frac{s}{\omega_{ESR}}}{1+\frac{s}{Q_o\omega_o}+\frac{s^2}{\omega_o^2}}$
Compensator transfer function(1)	$G_c(s)=\frac{\hat{v}_{comp}(s)}{\hat{v}_o(s)}=K_{mid}\frac{\left(1+\frac{\omega_{z1}}{s}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$
Modulator transfer function	$F_M=\frac{\hat{d}(s)}{\hat{V}_{comP}(s)}=\frac{1}{V_{RAMP}}$

(1) $K_{mid}=R_{C1}/R_{FB1}$ is the mid-band gain of the compensator. By expressing one of the compensator zeros in inverted zero format, the mid-band gain is denoted explicitly.

Figure 41 shows the open-loop response gain and phase. The poles and zeros of the system are marked with x and o symbols, respectively, and a + symbol indicates the crossover frequency. When plotted on a log (dB) scale, the open-loop gain is effectively the sum of the individual gain components from the modulator, power stage, and compensator (see Figure 42). The open-loop response of the system is measured experimentally by breaking the loop, injecting a variable-frequency oscillator signal, and recording the ensuing frequency response using a network analyzer setup.

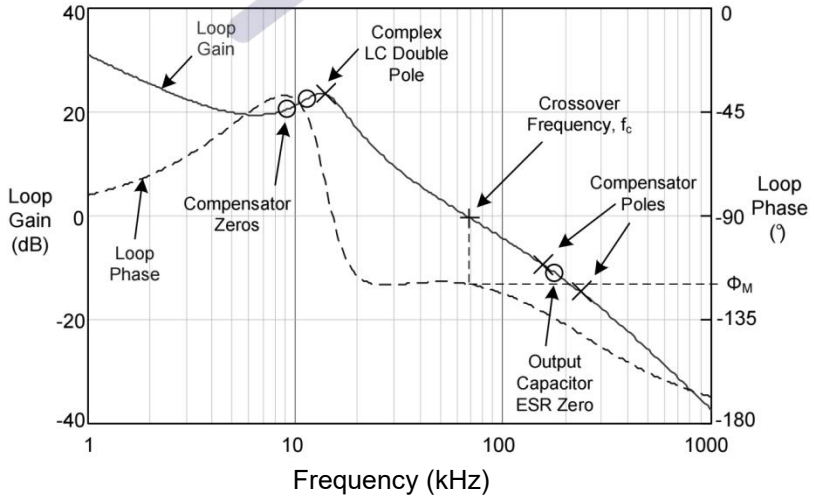


Figure 41. Typical Buck Regulator Loop Gain and Phase With Voltage-Mode Control

If the pole located at ω_{p1} cancels the zero located at ω_{ESR} and the pole at ω_{p2} is located well above crossover, the expression for the loop gain, $T_v(s)$ in Table 4, can be manipulated to yield the simplified expression given in Equation 14.

$$T_V(s) = R_{C1} \times C_{C3} \times \frac{V_{IN}}{V_{RAMP}} \times \frac{\omega_O^{\ 2}}{s} \quad (14)$$

Essentially, a multi-order system is reduced to a single-order approximation by judicious choice of compensator components. A simple solution for the crossover frequency (denoted as f_c in Figure 41) with Type-III voltage- mode compensation is derived as shown in Equation 15 and Equation 16.

$$\omega_C = 2\pi \times f_C = \omega_O \times K_{mid} \times \frac{V_{IN}}{V_{RAMP}} \quad (15)$$

$$K_{mid} = \frac{f_C}{f_O} \times \frac{1}{K_{FF}} = \frac{R_{C1}}{R_{FB1}} \quad (16)$$

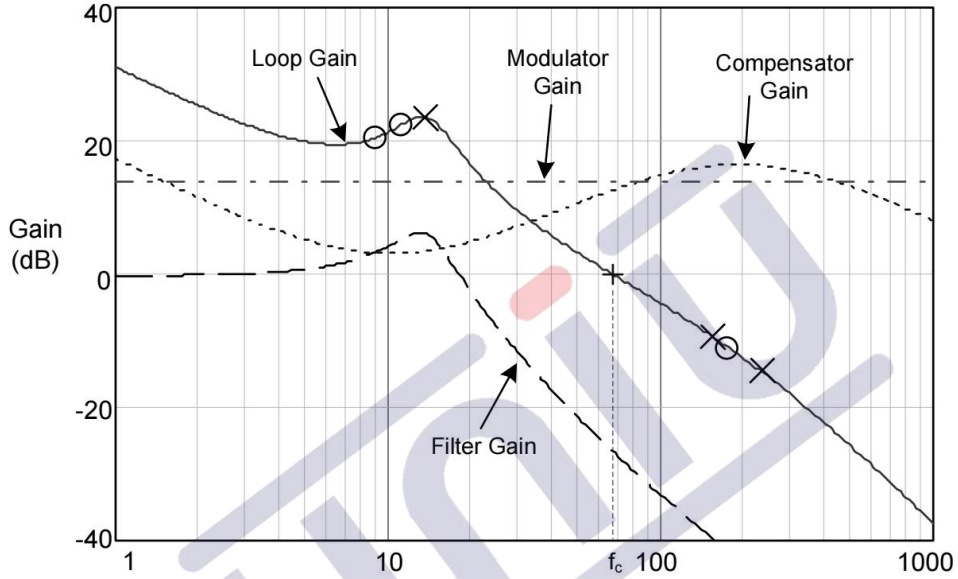


Figure 42. Buck Regulator Constituent Gain Components

The loop crossover frequency is usually selected between one-tenth to one-fifth of switching frequency. Inserting an appropriate crossover frequency into Equation 15 gives a target for the mid-band gain of the compensator, K_{mid} . Given an initial value for R_{FB1} , R_{FB2} is then selected based on the desired output voltage. Values for R_{C1} , R_{C2} , C_{C1} , C_{C2} and C_{C3} are calculated from the design expressions listed in Table 5, with the premise that the compensator poles and zeros are set as follows: $\omega_{z1} = 0.5\omega o$, $\omega_{z2} = \omega o$, $\omega_{p1} = \omega_{ESR}$, $\omega_{p2} = \omega_{SW}/2$.

Table 5. Compensation Component Selection

Resistors	Capacitors
$R_{FB2} = \frac{R_{FB1}}{(V_{OUT}/V_{REF})-1}$	$C_{C1} = \frac{2}{\omega_{Z1} \times R_{C1}}$
$R_{C1} = K_{mid} \times R_{FB1}$	$C_{C2} = \frac{1}{\omega_{P2} \times R_{C1}}$
$R_{C2} = \frac{1}{\omega_{P1} \times C_{C3}}$	$C_{C3} = \frac{1}{\omega_{Z2} \times R_{FB1}}$

Referring to the bode plot in Figure 41, the phase margin, indicated as φ_M , is the difference between the loop phase and –180° at crossover. A target of 50° to 70° for this parameter is considered ideal. Additional phase boost is dialed in by locating the compensator zeros at a frequency lower than the LC double pole (hence why C_{C1} is scaled by a factor of 2 above). This helps mitigate the phase dip associated with the LC filter, particularly at light loads when the Q-factor is higher and the phase dip becomes especially prominent. The ramification of low phase in the frequency domain is an under-damped transient response in the time domain.

The power supply designer now has all the necessary expressions to optimally position the loop crossover frequency while maintaining adequate phase margin over the required line, load and temperature operating ranges. The U3401/2 Quickstart Calculator is available to expedite these calculations and to adjust the bode plot as needed.

◆ EMI Filter Design

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

$$Z_{IN} = \left| -\frac{V_{IN(\min)}^{2}}{P_{IN}} \right| \quad (17)$$

The EMI filter design steps are as follows:

1. Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.
2. Input filter inductor L_{IN} is usually selected between 1μH and 10μH, but it can be lower to reduce losses in a high current design.
3. Calculate input filter capacitor C_F。

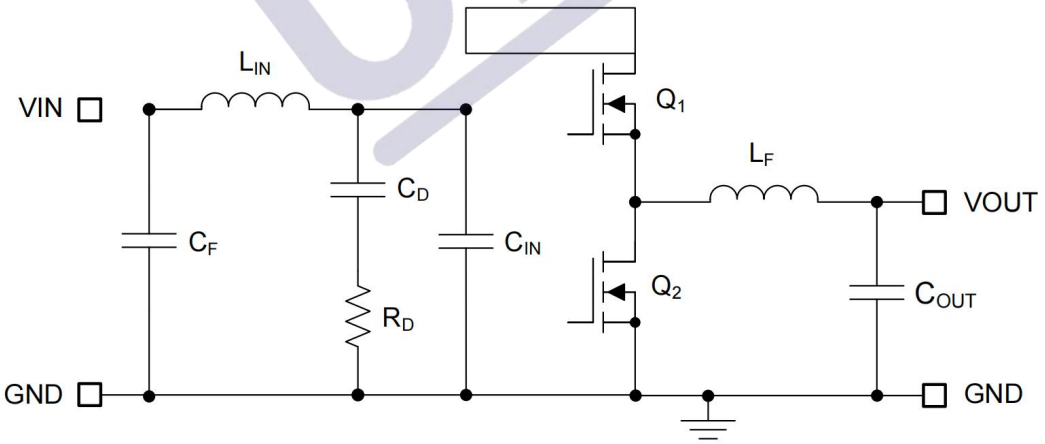


Figure 43. Buck Regulator With π-Stage EMI Filter

By calculating the first harmonic current from Fouriether series of the input current waveform and multiplying it by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by Equation 18.

$$Attn = 20\log\left(\frac{I_{PEAK}}{\pi^2 \times F_{SW} \times C_{IN}} \times 1\mu V\right) \times \sin(\pi \times D_{MAX}) - V_{MAX}$$

Where：

V_{MAX} is the allowed dBμV noise level for the applicable conducted EMI standard, for example CISPR 25 Class 5.

C_{IN} is the existing input capacitance of the buck regulator.

D_{MAX} is the maximum duty cycle.

I_{PEAK} is the peak inductor current. (18)

For filter design purposes, the current at the input can be modeled as a square-wave. Determine the EMI filter capacitance C_F from Equation 19.

$$C_F = \frac{1}{L_{IN}} \times \left\{ \frac{10^{\frac{|Attn|}{40}}}{2\pi \times F_{SW}} \right\}^2 \quad (19)$$

Adding an input filter to aswitching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small such that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. The resonant frequency of the filter is given by Equation 20.

$$f_{res} = \frac{1}{2\pi \times \sqrt{L_{IN} \times C_F}} \quad (20)$$

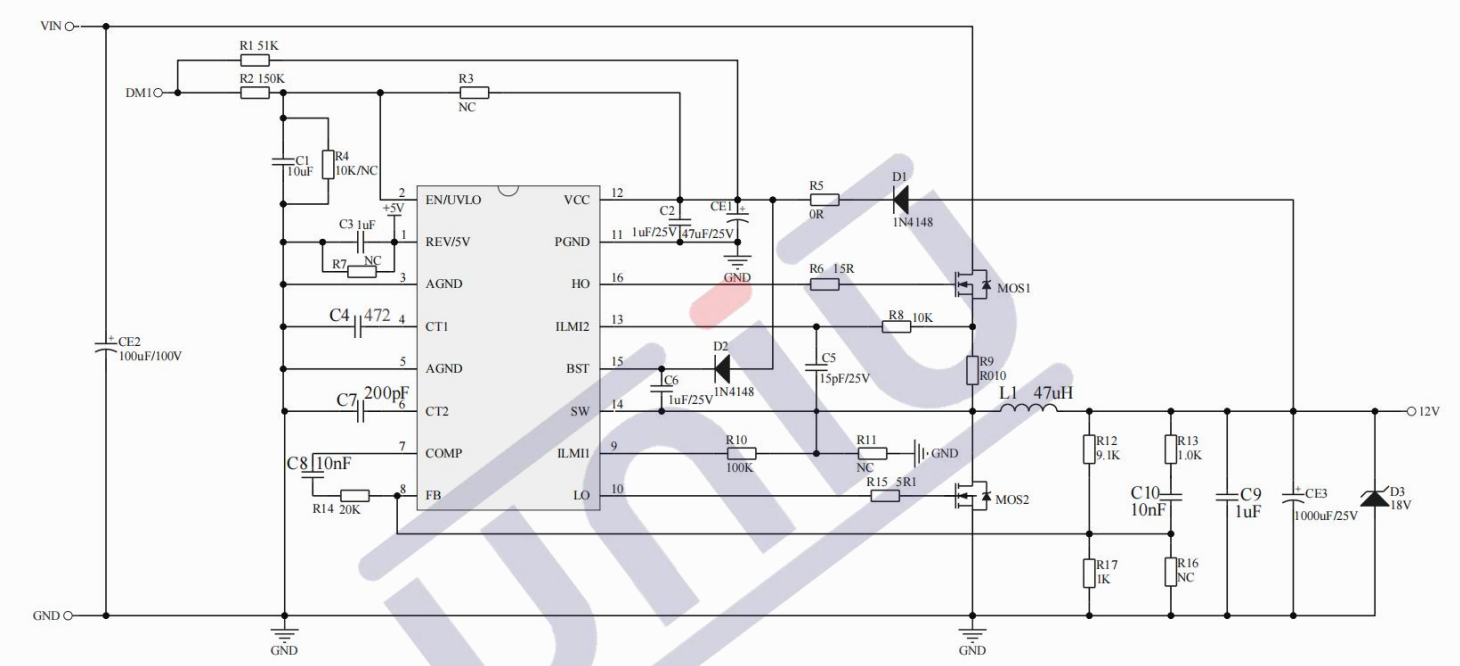
The purpose of R_D is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D . Capacitor C_D should have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN} . This prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance of the filter is high at the resonant frequency (Q of filter formed by L_{IN} and C_{IN} is too high). An electrolytic capacitor C_D can be used for damping with a value given by Equation 21.

$$C_D \geq 4C_{IN} \quad (21)$$

Select the damping resistor R_D using Equation 22.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (22)$$

● Typical Applications



■ Power Supply Recommendations

The U3401/2 buck controller is designed to operate from a wide input voltage range from 24V to 400V. The characteristics of the input supply must be compatible with the Absolute Maximum Ratings and Recommended Operating Conditions tables. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with Equation 23.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (23)$$

Where:

η is the efficiency

If the converter is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables may have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the regulator is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10μF to 47μF is usually sufficient to provide input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The application report Simple Success with Conducted EMI for DC-DC Converters (SNVA489) provides helpful suggestions when designing an input filter for any switching regulator.

■ Layout

● Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuits (with high current and voltage slew rates) to assure appropriate device operation and design robustness. As expected, certain issues must be considered before designing a PCB layout using the U3401/2.The high-frequency power loop of the buck converter power stage is denoted by #1 in the shaded area of Figure 70. The topological architecture of a buck converter means that particularly high di/dt current flows in the components of loop 1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. Also important are the gate drive loops of the low-side and high-side MOSFETs, denoted by 2 and 3, respectively, in Figure 70.

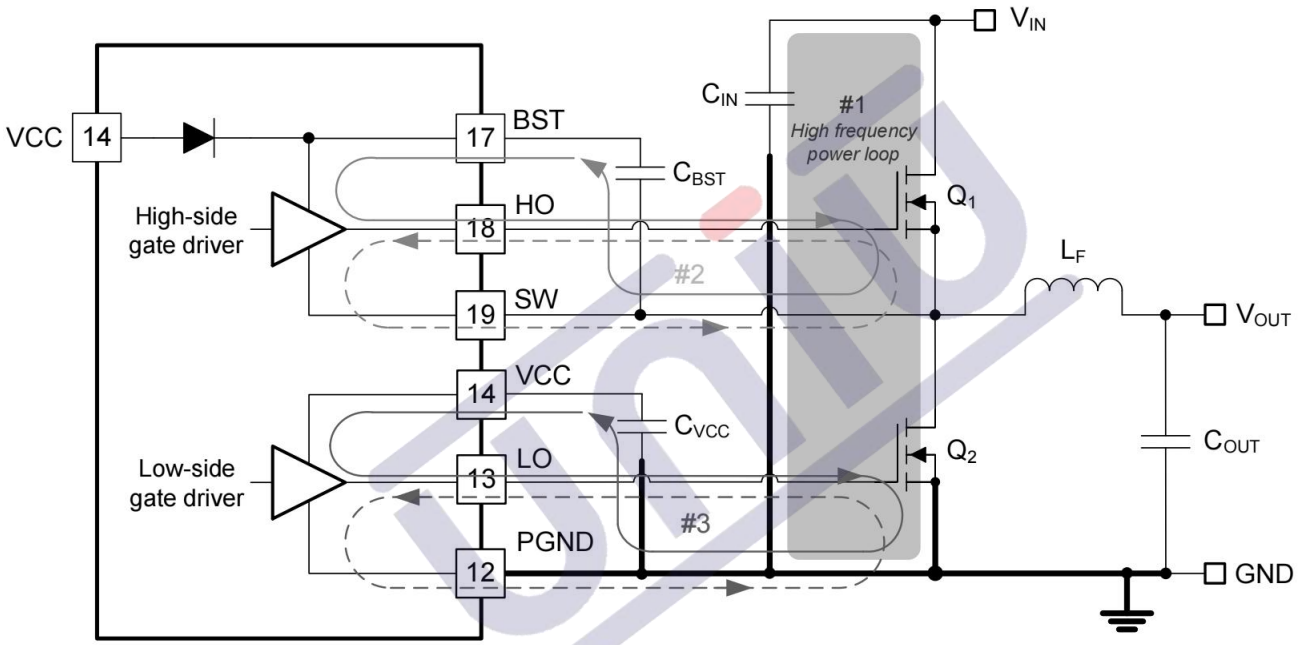


Figure 70. DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops

◆ Power Stage Layout

1. Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). insert at least one inner plane, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.
2. The DC/DC converter has several high-current loops. Minimize the area of these loops in order to suppress generated switching noise and parasitic loop inductance and optimize switching performance.
   1) Loop #1: The most important loop to minimize the area of is the path from the input capacitor(s) through the high- and low-side MOSFETs, and back to the capacitor(s) through the ground connection. Connect the input capacitor(s) negative terminal close to the source of the low-side MOSFET (at ground). Similarly, connect the input capacitor(s) positive terminal close to the drain of the high-side MOSFET (at VIN). Refer to loop #1 of Figure 70.

2) Another loop, not as critical though as loop #1, is the path from the low-side MOSFET through the inductor and output capacitor(s), and back to source of the low-side MOSFET through ground. Connect the source of the low-side MOSFET and negative terminal of the output capacitor(s) at ground as close as possible.

3. The PCB trace defined as SW node, which connects to the source of the high-side (control) MOSFET, the drain of the low-side (synchronous) MOSFET and the high-voltage side of the inductor, must be short and wide. However, the SW connection is a source of injected EMI and thus must not be too large.
4. Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
5. The SW pin connects to the switch node of the power conversion stage and acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop #1 in Figure 70 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (>100 MHz) ringing on the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Ensure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. Provide provisions for snubber network components in the PCB layout. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components as needed.

◆ Gate Drive Layout

The U3401/2 high-side and low-side gate drivers incorporate short propagation delays, adaptive dead-time control and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

Loop2:high-side MOSFET, Q_1 . During the high-side MOSFET turn-on, high current flows from the bootstrap (boot) capacitor through the gate driver and high-side MOSFET, and back to the negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from the gate of the high-side MOSFET through the gate driver and SW, and back to the source of the high-side MOSFET through the SW trace. Refer to loop #2 of Figure 70.

Loop3:low-side MOSFET, Q_2 . During the low-side MOSFET turn-on, high current flows from the VCC decoupling capacitor through the gate driver and low-side MOSFET, and back to the negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from the gate of the low-side MOSFET through the gate driver and GND, and back to the source of the low-side MOSFET through ground. Refer to loop #3 of Figure 70.

UNI strongly recommends following circuit layout guidelines when designing with high-speed MOSFET gate drive circuits.

1. Connections from gate driver outputs, HO and LO, to the respective gate of the high-side or low-side MOSFET must be as short as possible to reduce series parasitic inductance. Use 0.65 mm (25 mils) or wider traces. Use via(s), if necessary, of at least 0.5 mm (20 mils) diameter along these traces. Route HO and SW gate traces as a differential pair from the U3401/2 to the high-side MOSFET, taking advantage of flux cancellation.
2. Minimize the current loop path from the VCC and BST pins through their respective capacitors as these provide the high instantaneous current, up to 1.8A, to charge the MOSFET gate capacitances. Specifically, locate the bootstrap capacitor, C_{BST} , close to the BST and SW pins of the U3401/2 to minimize the area of loop #2 associated with the high-side driver. Similarly, locate the VCC capacitor, C_{VCC}, close to the VCC and PGND pins of the U3401/2 to minimize the area of loop #3 associated with the low-side driver.
3. Placing a 12Ω to 15Ω resistor in series with the boot capacitor, as shown in Figure 55, slows down the high-side MOSFET turn-on transition, serving to reduce the voltage ringing and peak amplitude at the SW node at the expense of increased MOSFET turn-on power loss.

◆ PWM Controller Layout

With the proviso to locate the controller as close as possible to the MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals, current limit setting, and temperature sense are considered in the following:

1. Separate power and signal traces, and use a ground plane to provide noise shielding.
2. Place all sensitive analog traces and components such as COMP, FB, RT, ILIM and SS/TRK away from high-voltage switching nodes such as SW, HO, LO or BST to avoid mutual coupling. Use internal layer(s) as ground plane(s). Pay particular attention to shielding the feedback (FB) trace from power traces and components.
3. The upper feedback resistor can be connected directly to the output voltage sense point at the load device or the bulk capacitor at the converter side.
4. Connect the ILIM setting resistor from the drain of the low-side MOSFET to ILIM and make the connections as close as possible to the U3401/2. The trace from the ILIM pin to the resistor must avoid coupling to a high-voltage switching net.
5. Minimize the loop area from the VCC and VIN pins through their respective decoupling capacitors to the GND pin. Locate these capacitors as close as possible to the U3401/2.

◆ Thermal Design and Layout

The useful operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by:

a. average gate drive current requirements of the power MOSFETs;
b. switching frequency;
c. operating input voltage (affecting bias regulator LDO voltage drop and hence its power dissipation);
d. thermal characteristics of the package and operating environment.

For a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits .The U3401/2 controller is available in a small 6.3mm × 10mm 16-pin SOP (RGY) Power PAD™ package to cover a range of application

requirements. The thermal metrics of this package are summarized in Thermal Information. The application report Semiconductor and IC Package Thermal Metrics provides detailed information regarding the thermal information table.

The 16-pin SOP package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, it is thermally connected to the substrate of the U3401/2 device (ground). This allows a significant improvement in heat sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem. The exposed pad of the U3401/2 is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value. Wide traces of the copper tying in the no-connect pins of the U3401/2 (pins 9 and 16) and connection to this thermal land helps to dissipate heat.

Numerous vias with a 0.3mm diameter connected from the thermal land to the internal and solder-side ground plane(s) are vital to help dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this provide a plane for the power stage currents to flow but it also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The drain pad of the high-side MOSFET is normally connected to a VIN plane for heat sinking. The drain pad of the low-side MOSFET is tied to the SW plane, but the SW plane area is purposely kept relatively small to mitigate EMI concerns.

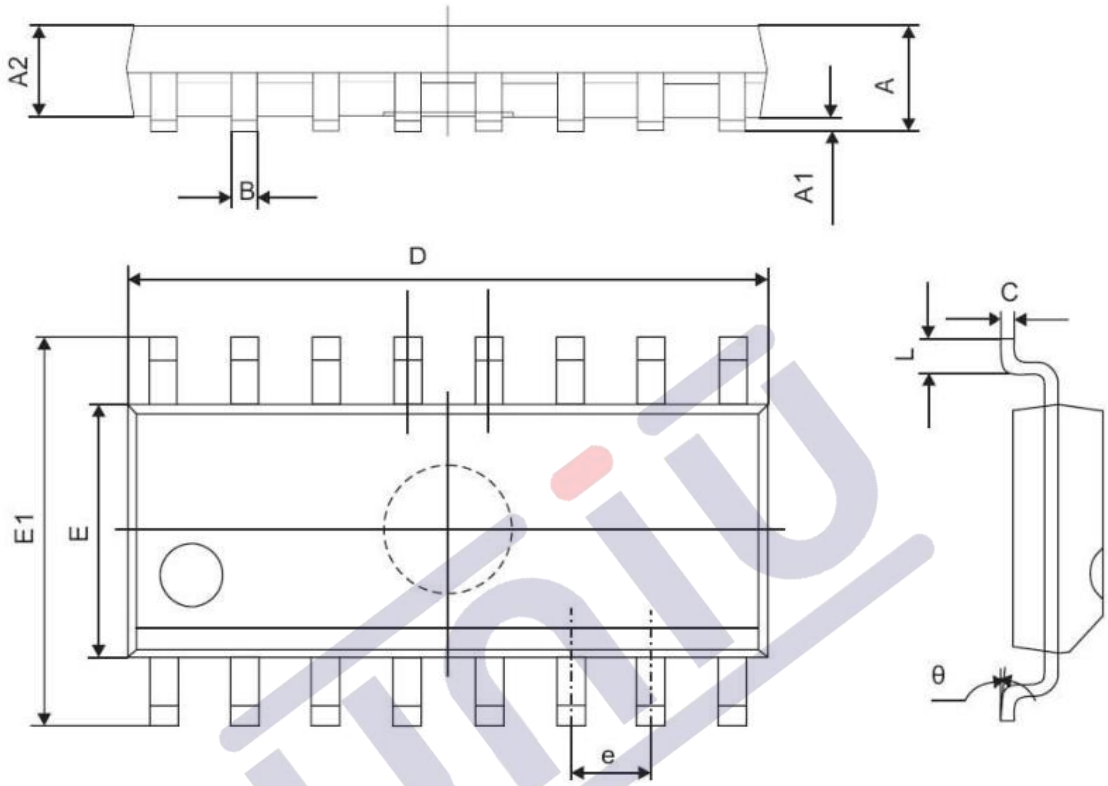
◆ Ground Plane Design

As mentioned previously, using one or more of the inner PCB layers as a solid ground plane is recommended. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. Connect the PGND pin to the system ground plane using an array of vias under the exposed pad. Also connect the PGND directly to the return terminals of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce because of load current variations. The power traces for PGND, VIN and SW can be restricted to one side of the ground plane. The other side of the ground plane contains much less noise and is ideal for sensitive analog trace routes.

■ Mechanical Packaging and Orderable

● Mechanical Packaging

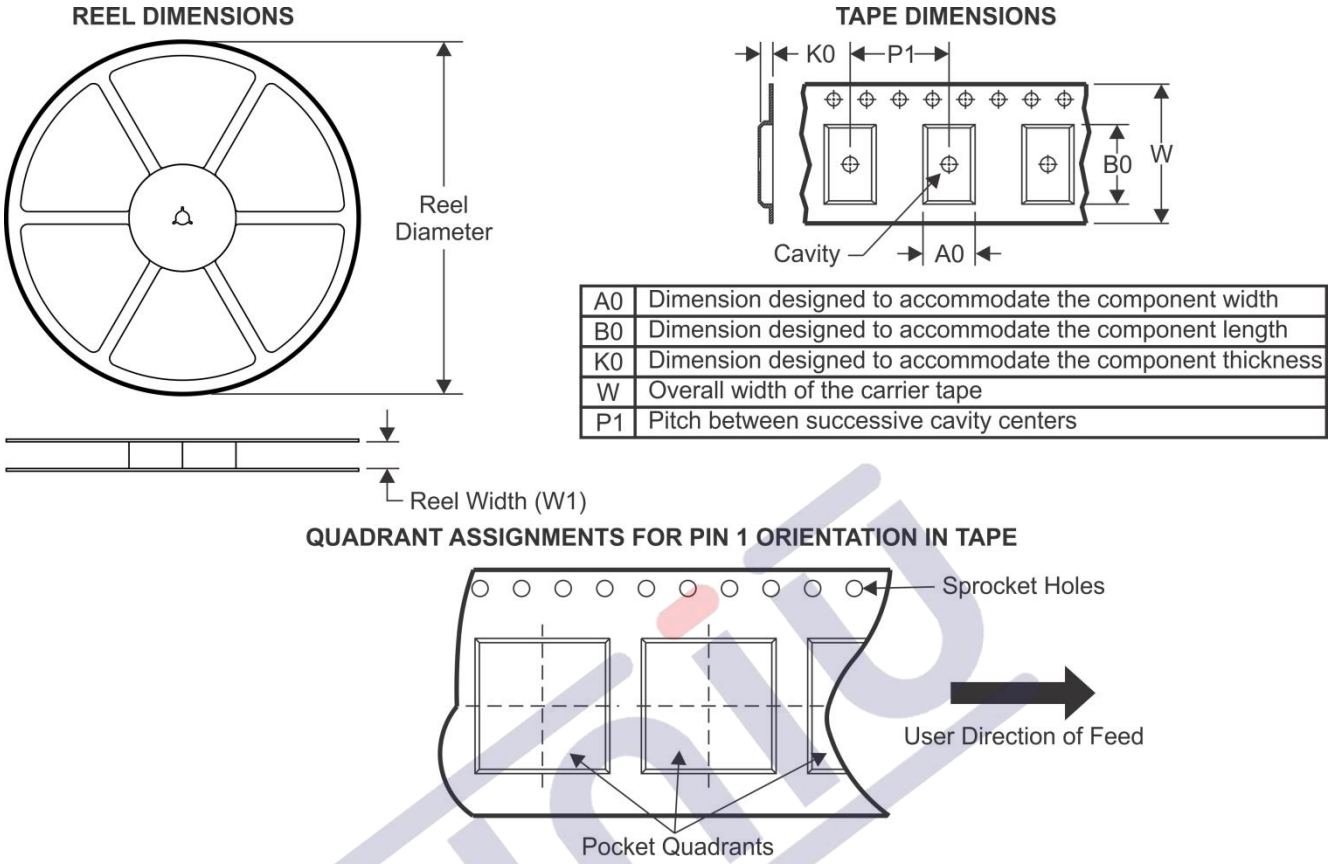
SOP-16



（mm）

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
B	0.330	0.510
C	0.190	0.250
D	9.800	10.000
E	3.800	4.000
E1	5.800	6.300
e	1.270(TYP)	
L	0.400	1.270
θ	0°	8°

● Tape And Reel Information

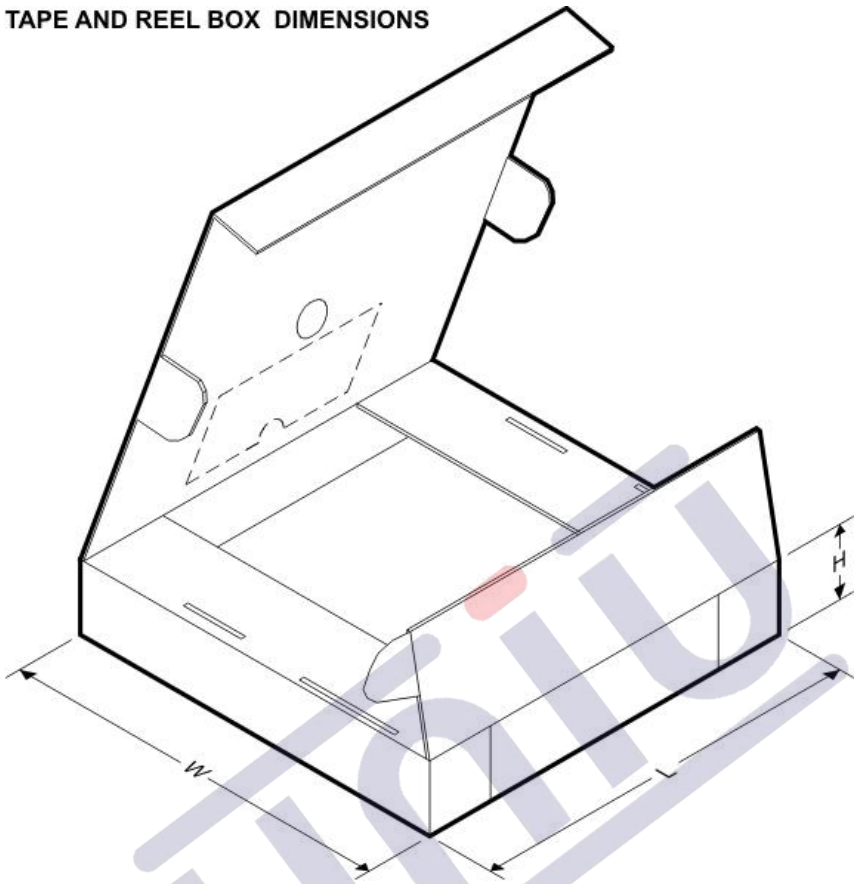


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
U3401	SOP	RGY	16	3000	330.0	16	7	12	1.18	8.0	12.0	Q1
U3402	SOP	RGY	16	3000	330.0	16	7	12	1.18	8.0	12.0	Q1

● Tape And Reelbox Dimensions



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
U3401	SOP	RGY	16	3000	370.0	355.0	55.0
U3402	SOP	RGY	16	3000	370.0	355.0	55.0

1.版本记录

DATE	REV.	DESCRIPTION
2018/04/19	1.0	First Release
2021/01/02	1.1	Layout adjustment
2021/03/10	1.2	Change parameters

2.免责声明

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