TPA3144D2 6W 无电感器立体声 (BTL) D 类音频放大器，具有超低 EMI和 AGL

1 特性

- 电源电压为 7V、THD+N 为 10%、负载为 4Ω 时的功率为 2x6W/通道
- 电源电压为 9.5V、THD+N 为 10%、负载为 6Ω 时的功率为 2x6W/通道
- 电源电压为 10V、THD+N 为 10%、负载为 8Ω 时的功率为 2x6W/通道
- 高达 90% 的高效 D 类运行（负载为 8Ω），无需散热器
- 1W/4Ω/1kHz 时的 THD+N < 0.05%
- A 加权输出噪声 < 65μV
- 在宽电源电压范围内工作 SpeakerGuard™扬声器保护电路的工作电压范围为 4.5V 至 14.4V
- 无电感运行
- 抗电磁干扰 (EMI) 性能增强，具备扩展频谱和 1SPW 运行能力
- SpeakerGuard™扬声器保护功能包括自动增益限制、可调节功率限制器和直流保护
- 可靠的引脚至引脚、引脚接地以及引脚至电源短路保护和热保护
- 4 个可选的固定增益设置
- 单端或差分模拟输入
- 启动时无喀哒声和噼啪声

2 应用

- 电视
- 蓝牙 (BT) 扬声器
- 无线扬声器
- 迷你扬声器
- USB 扬声器
- 消费类音频设备

3 说明

TPA3144D2 是一款高效的 D 类音频功率放大器，适用于以高达 6W 的功率驱动阻抗为 6Ω 或 8Ω（每通道）的桥接式立体声扬声器。

具有扩频控制和 1SPW 调制方案的高级 EMI 抑制技术在满足 EMC 要求的同时支持在输出中使用价格低廉的铁氧体磁珠滤波器，从而降低系统成本。TPA3144D2 不仅针对短路和过载提供全面的保护，而且 SpeakerGuard™扬声器保护电路还包括一个可调节自动增益限制 (AGL)、一个可调节功率限制器和一个直流检测电路，用于保护连接的扬声器。 AGL 可在不发生信号削波的情况下调节最大输出电压，从而增强了扬声器保护效果，提升了音频质量。直流检测及引脚至引脚、引脚接地和引脚至电源短路保护电路可以防止扬声器在生产过程中发生输出直流和引脚短路。同时充分保护输出，防止 GND、PVCC、输出至输出短路。短路保护和热保护具有自动恢复功能。

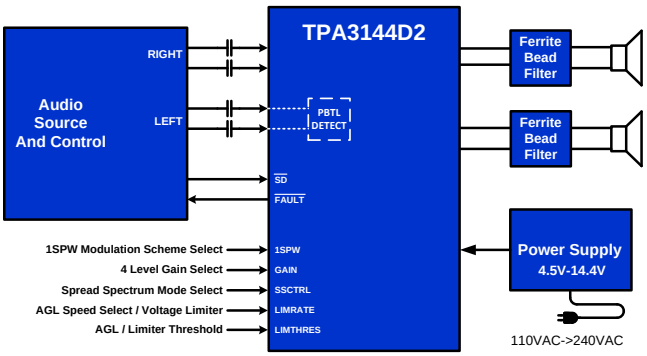
TPA3144D2 可驱动阻抗低至 4Ω 的立体声扬声器。TPA3144D2 的效率在负载为 8Ω 时高达 90%，无需外部散热器，而且 TPA3144D2 可在双层印刷电路板 (PCB) 上实现全功率输出。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPA3144D2	HTSSOP (28)	9.70mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (July 2015) to Revision C **Page**

- Changed the Supply Voltage (AVCC to GND, PVCC to GND) MAX value From: 16 V To: 20 V in the *Absolute Maximum Ratings* ... 5

Changes from Revision A (June 2015) to Revision B **Page**

- Changed Figure 5 ... 8
- Changed Figure 6 ... 8
- Changed Figure 8 ... 8
- Changed Figure 14 ... 9
- Changed Figure 15 ... 9
- Changed Figure 19 ... 15

Changes from Original (April 2015) to Revision A **Page**

- 已更改 “宽电源电压范围”特性从“4.5V 至 13.2V”更改为“4.5V 至 14.4V” ... 1
- Changed Continuous output power TYP from 10 W to 6 W ... 7
- Changed Continuous output power TYP from 10 W to 6 W ... 7
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- Changed Figure 15 ... 9

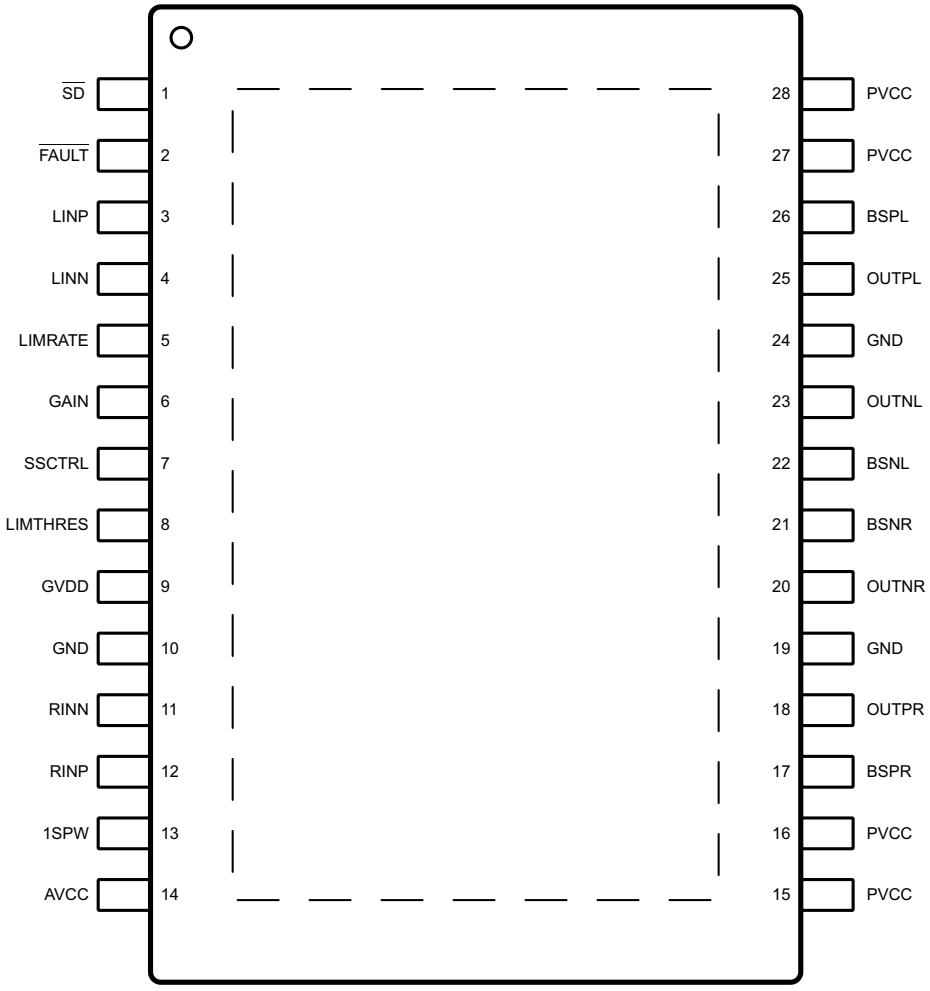
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5 Device Comparison Table

DEVICE NAME	DESCRIPTION
TPA3113D2	6-W Stereo Class-D Audio Power Amplifier with SpeakerGuard™
TPA3131D2	7W Filter-Free Class-D Stereo Amplifier In Space Saving QFN
TPA3130D2	15W Filter-Free Class D Stereo Amplifier with AM Avoidance
TPA3110D2	15W Filter-Free Class D Stereo Amplifier with SpeakerGuard™

6 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP
(Top View)



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Pin Functions

PIN		I/O/P(1)	DESCRIPTION
NAME	NUMBER		
$\overline{SD}$	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
$\overline{FAULT}$	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
LINP	3	I	Positive audio input for left channel. Biased at 3 V. Connect to GND for PBTL mode.
LINN	4	I	Negative audio input for left channel. Biased at 3 V. Connect to GND for PBTL mode.
LIMRATE	5	I	Decay speed for clip free power limiter. Connect a resistor divider from GVDD to GND to set decay speed. Connect directly to GND to disconnect limiter.
GAIN	6	I	4-state Amplifier gain select. Connect a resistor divider from GVDD to GND to set closed loop gain.
SSCTRL	7	I	Spread spectrum control. Connect a resistor divider from GVDD to GND to set mode. Connect to GND for disable spread spectrum.
LIMTHRES	8	I	Voltage limit level for AGL and power limiter. Connect a resistor divider from GVDD to GND to set limit. Connect directly to GVDD to disconnect limiter
GVDD	9	O	High-side FET gate drive supply. Nominal voltage is 7 V. Also should be used as supply for LIMTHRES limit function
GND	10	P	Analog signal ground.
RINN	11	I	Negative audio input for right channel. Biased at 3 V.
RINP	12	I	Positive audio input for right channel. Biased at 3 V.
1SPW	13	I	Modulation scheme select. Low: BD mode, high: 1SPW mode.
AVCC	14	P	Analog supply
PVCC	15	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connected internally.
PVCC	16	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connected internally.
BSPR	17	I	Bootstrap I/O for right channel, positive high-side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
GND	19	P	Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	I	Bootstrap I/O for right channel, negative high-side FET.
BSNL	22	I	Bootstrap I/O for left channel, negative high-side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.
GND	24	P	Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	I	Bootstrap I/O for left channel, positive high-side FET.
PVCC	27	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connected internally.
PVCC	28	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connected internally.
Thermal Pad		P	Connect to GND for best thermal and electrical performance

(1) I = Input, O = Output, P = Power

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVCC to GND, PVCC to GND	–0.3	20	V
	GVDD to GND			V
	GND to GND	-0.3	0.3	V
Input current	To any pin except supply pins		10	mA
Voltage	$\overline{SD}$, $\overline{FAULT}$, 1SPW to GND(2)	–0.3	AVCC + 0.3	V
			10	V/ms
Voltage	GAIN, LIMRATE, LIMTHRES, SSCTRL(3)	–0.3	GVDD + 0.3	V
			100	V/ms
Voltage	RINN, RINP, LINN, LINP	–0.3	6.3	V
Minimum load resistance, R_L	BTL, PVCC > 12 V	4.8		Ω
	BTL, PVCC ≤ 12 V	3.2		
	PBTL, PVCC > 12 V	2.5		
	PBTL, PVCC ≤ 12 V	1.8		
Continuous total power dissipation		See the Thermal Information Table		
Operating free-air temperature range, T_A(4)		–40	85	°C
Temperature range		–65	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage slew rate of these pins must be restricted to no more than 10 V/ms. For higher slew rates, use a 100 kΩ resister in series with the pins.
(3) The voltage slew rate of these pins must be restricted to no more than 100 V/ms. For higher slew rates, use a 100 kΩ resister in series with the pins.
(4) The TPA3144D2 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs SLMA002 for more information about using the TSSOP thermal pad.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	4.5	14.4	V
V_{IH}	High-level input voltage	$\overline{SD}$, 1SPW	2	AVCC	V
V_{IL}	Low-level input voltage	$\overline{SD}$, 1SPW		0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, $R_{PULL-UP}$=100 k, PVCC=14.4 V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, 1SPW, V_I = 2 V, AVCC = 12 V		50	µA
I_{IL}	Low-level input current	$\overline{SD}$, 1SPW, V_I = 0.8 V, AVCC = 12 V		5	µA
T_A	Operating free-air temperature(1)		–40	85	°C
T_J	Operating junction temperature(1)		-40	150	°C

(1) The TPA3144D2 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs SLMA002 for more information about using the TSSOP thermal pad.

7.4 Thermal Information

THERMAL METRIC(1)		TPA3144D2 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC CHARACTERISTICS, T_A = 25°C, AV_{CC} = PV_{CC} = 12 V, R_L = 6 Ω, using the TPA3144D2 EVM which is available at ti.com. (unless otherwise noted)							
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, 10 µF + 680 nF Output Filter			35	40	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load			40	60	µA
$r_{DS(on)}$	Drain-source on-state resistance	I_O = 500 mA, T_J = 25°C Excluding Metal and Bond Wire Resistance	High Side		240		mΩ
			Low side		240		
G	Gain	GAIN = 0 V (GND)		19	20	21	dB
		GAIN = 2.3 V (1/3·GVDD)		25	26	27	
		GAIN = 4.6 V (2/3·GVDD)		31	32	33	
		GAIN = 6.9 V (GVDD)		35	36	37	
t_{on}	Turn-on time	$\overline{SD}$ = 2 V			14		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2.5		µs
GVDD	Gate drive supply	I_{GVDD} = 2 mA		6.4	6.9	7.4	V
t_{DCDET}	DC detect time	V_{RINN} = 3.1 V and V_{RINN} = 2.9 V, or V_{RINN} = 2.9 V and V_{RINN} = 3.1 V			950		ms

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC CHARACTERISTICS, T_A = 25°C, AV_{CC} = PV_{CC} = 12 V, R_L = 6 Ω, using the TPA3144D2 EVM which is available at ti.com. (unless otherwise noted)						
PSRR	Power supply ripple rejection	200-mV_{PP} ripple at 1 kHz, Gain = 20 dB, Inputs ac-coupled to GND		–65		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz		6		W
P_O	Continuous output power	THD+N = 10%, f = 1 kHz, PV_{CC} = 13 V, R_L = 8 Ω		6		W
P_O	Continuous output power, PBTL (mono)	THD+N = 10%, f = 1 kHz, PV_{CC} = 13 V, R_L = 4 Ω		12		W
I_O	Maximum output current	f = 1 kHz, R_L=3 Ω		3.1		A
THD+N	Total harmonic distortion + noise	f = 1 kHz, P_O = 5 W (half-power)		0.06%		
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB, Spread Spectrum off		65		µV
				–80		dBV
	Crosstalk	V_O = 1 Vrms, Gain = 20 dB, f = 1 kHz		–75		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted, Spread Spectrum off		102		dB
OTE	Thermal trip point			150		°C
	Thermal hysteresis			15		°C
TFB	Thermal foldback trip point			125		°C

7.6 Switching Characteristics

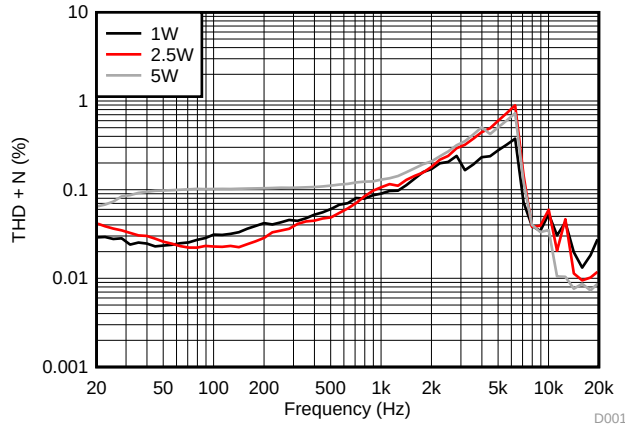
over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
f_{OSC}	Oscillator frequency	250	310	350	kHz
$f_{OSC, SS}$	Oscillator frequency, Spread Spectrum ON	255	315	355	kHz

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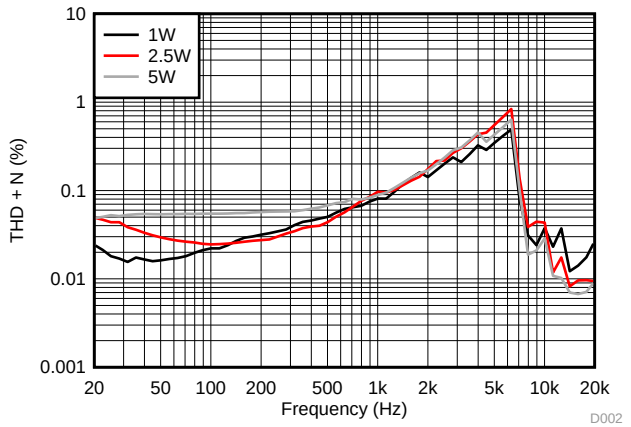
7.7 Typical Characteristics

All Measurements taken at 20dB closed loop gain, 1-kHz audio, T_A = 25°C unless otherwise noted. Measurements were made with AES17 filter using the TPA3144D2 EVM, which is available at ti.com.



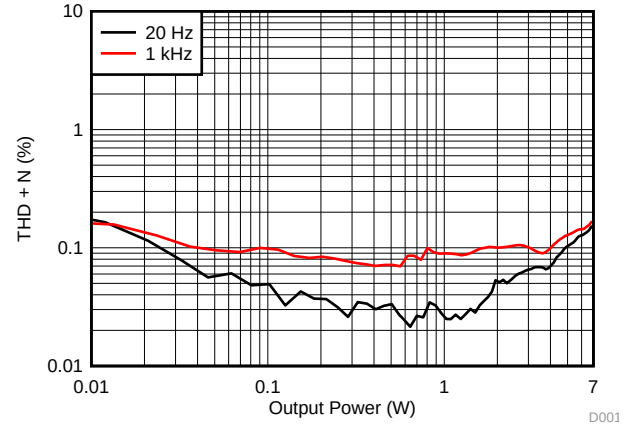
AVCC=PVCC = 12 V, Load = 6 Ω + 47 µH, 1 W, 2.5 W, 5 W

Figure 1. Total Harmonic Distortion vs Frequency, 1SPW (BTL)



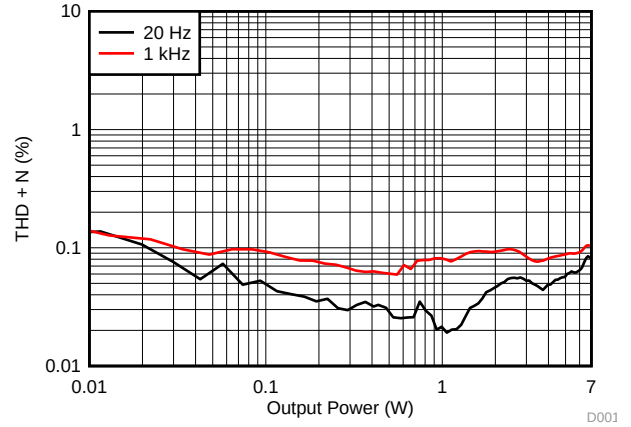
AVCC=PVCC = 13 V, Load = 8 Ω + 66 µH, 1 W, 2.5 W, 5 W

Figure 2. Total Harmonic Distortion vs Frequency, 1SPW (BTL)



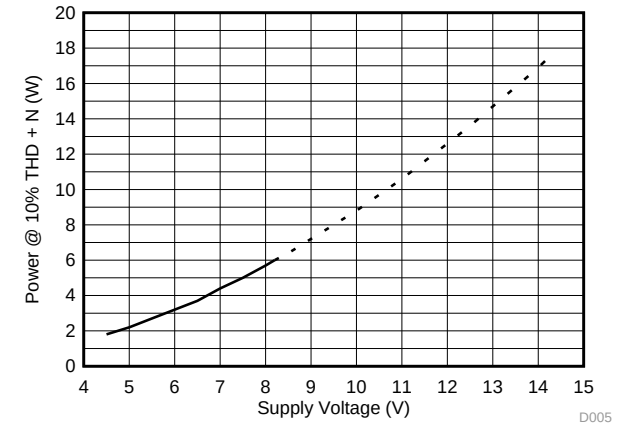
AVCC=PVCC = 12 V, Load = 6 Ω + 47 µH, 20 Hz, 1 kHz, 6.7 kHz

Figure 3. Total Harmonic Distortion + Noise vs Output Power, 1SPW (BTL)



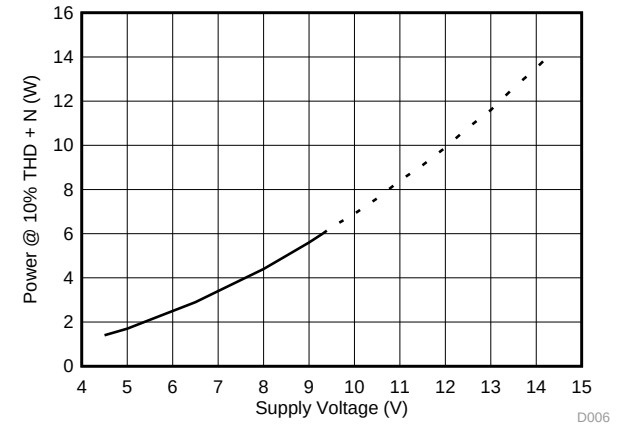
AVCC=PVCC = 13 V, Load = 8 Ω + 66 µH, 20 Hz, 1 kHz, 6.7 kHz

Figure 4. Total Harmonic Distortion + Noise vs Output Power, 1SPW (BTL)



AVCC=PVCC = 4.5 V to 14.4 V, Load = 6 Ω + 47 µH, AGL + PLIM disable (LIMRATE = GND, LIMTHRES = GVDD)

Figure 5. Output Power vs Supply Voltage, 1SPW (BTL)



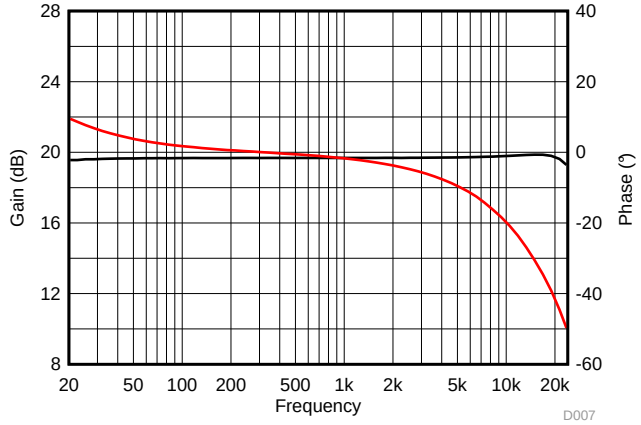
AVCC=PVCC = 4.5 V to 14.4 V, Load = 8 Ω + 66 µH, AGL + PLIM disable (LIMRATE = GND, LIMTHRES = GVDD)

Figure 6. Output Power vs Supply Voltage, 1SPW (BTL)

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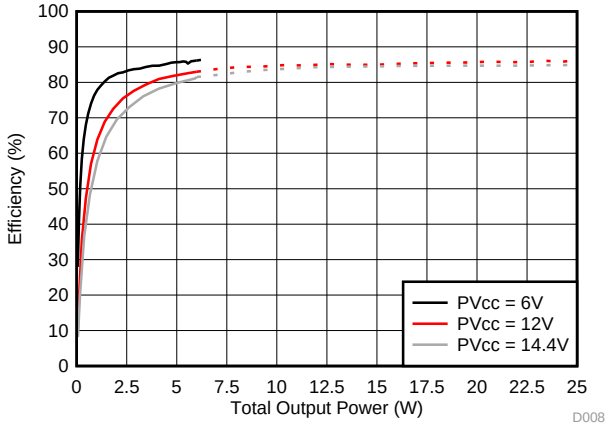
Typical Characteristics (continued)

All Measurements taken at 20dB closed loop gain, 1-kHz audio, T_A = 25°C unless otherwise noted. Measurements were made with AES17 filter using the TPA3144D2 EVM, which is available at ti.com.



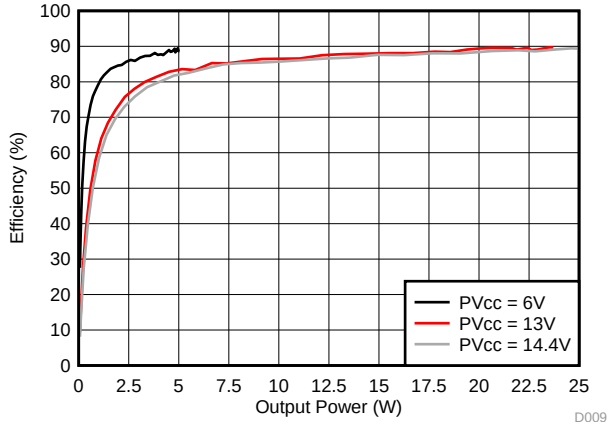
AVCC=PVCC = 12 V, Load = 6 Ω + 47 µH (device pins)

Figure 7. Gain/Phase vs Frequency (BTL)



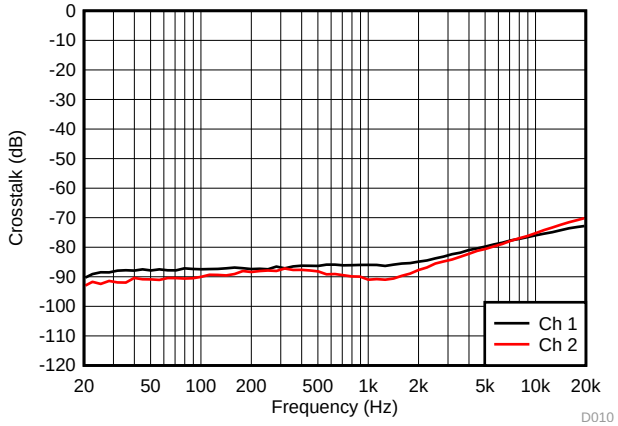
AVCC=PVCC = 6 V, 12 V, 14.4 V, Load = 6 Ω + 47 µH, AGL + PLIM disable (LIMRATE = GND, LIMTHRES = GVDD)

Figure 8. Efficiency vs Output Power, 1SPW (BTL)



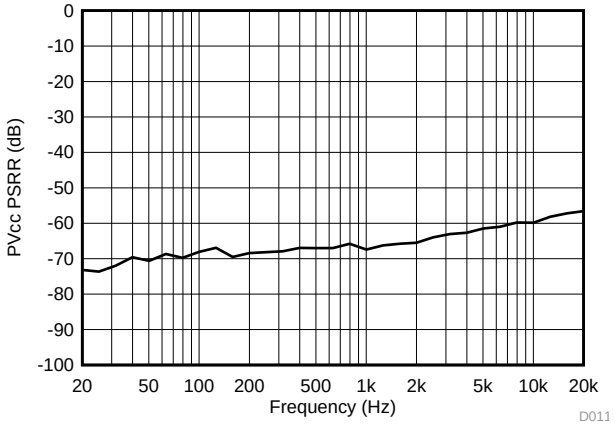
AVCC=PVCC= 6 V, 13 V, 14.4 V, Load = 8 Ω + 66 µH, AGL + PLIM disable (LIMRATE = GND, LIMTHRES = GVDD)

Figure 9. Efficiency vs Output Power, 1SPW (BTL)



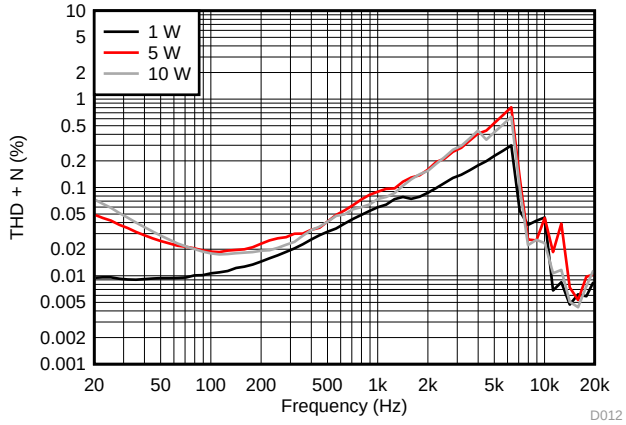
AVCC=PVCC = 12 V, 1 W, Load = 6 Ω + 47 µH

Figure 10. Crosstalk vs Frequency, 1SPW (BTL)



AVCC=PVCC = 12 V, Load = 4 Ω + 33 µH

Figure 11. Supply Ripple Rejection Ratio vs Frequency (BTL)



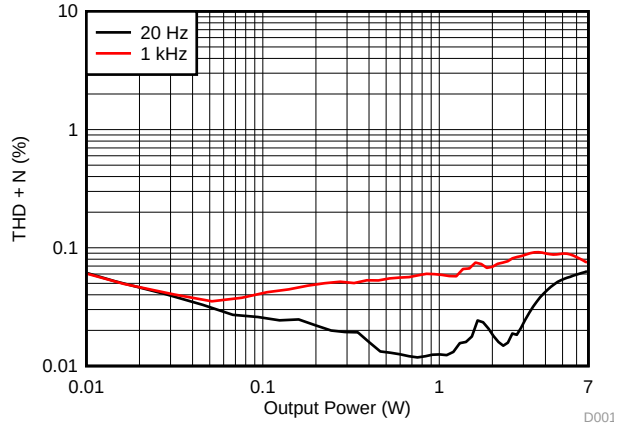
AVCC=PVCC = 13 V, Load = 4 Ω + 33 µH, 1 W, 2.5 W, 10 W

Figure 12. Total Harmonic Distortion + Noise vs Frequency, 1SPW (PBTL)

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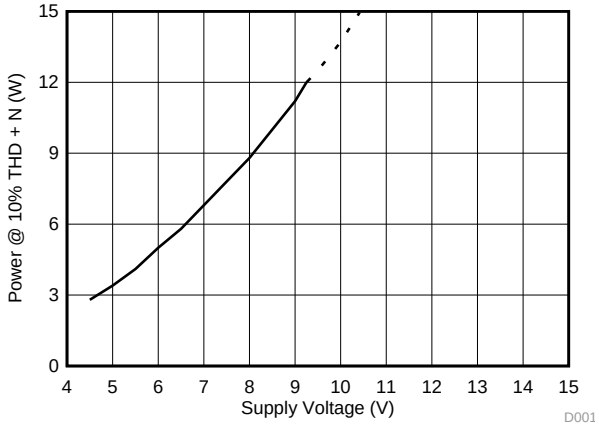
Typical Characteristics (continued)

All Measurements taken at 20dB closed loop gain, 1-kHz audio, T_A = 25°C unless otherwise noted. Measurements were made with AES17 filter using the TPA3144D2 EVM, which is available at ti.com.



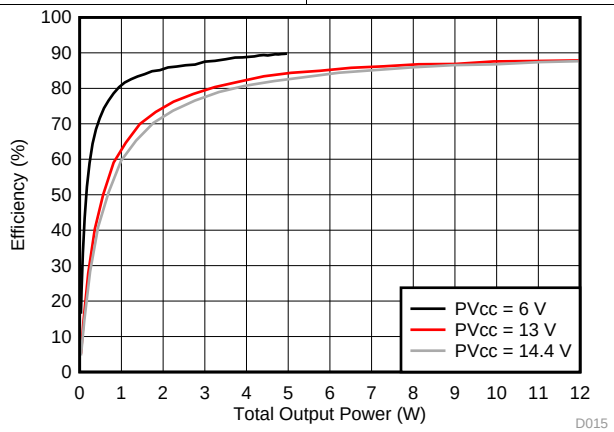
AVCC=PVCC = 13 V, Load = 4 Ω + 33 µH, 20 Hz, 1 kHz, 6.7 kHz

Figure 13. Total Harmonic Distortion + Noise vs Output Power, 1SPW (PBTL)



AVCC=PVCC = 4.5 V to 14.4 V, Load = 4 Ω + 33 µH, AGL + PLIM disable (LIMRATE = GND, LIMTHRES = GVDD)

Figure 14. Output Power vs Supply Voltage, 1SPW (PBTL)



AVCC=PVCC = 6 V, 13 V, 14.4 V, Load = 4 Ω + 33 µH, AGL + PLIM disable (LIMRATE = GND, LIMTHRES = GVDD)

Figure 15. Efficiency vs Output Power, 1SPW (PBTL)

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Specifications* and *Typical Characteristics*.

Most audio analyzers will not give correct readings of Class-D amplifiers' performance due to their sensitivity to out of band noise present at the amplifier output. An AES-17 pre analyzer filter is recommended to use for Class-D amplifier measurements. In absence of such filter, a 30-kHz low-pass filter (10 Ω + 47 nF) can be used to reduce the out of band noise remaining on the amplifier outputs.

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9 Detailed Description

9.1 Overview

To facilitate system design, the TPA3144D2 needs only a single power supply between 4.5 V and 14.4 V for operation. An internal voltage regulator provides suitable voltage levels for the gate driver, digital, and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, as in the high-side gate drive, is accommodated by built-in bootstrap circuitry with integrated boot strap diodes requiring only an external capacitor for each half-bridge.

The audio signal path, including the gate drive and output stage, is designed as identical, independent full-bridges. All decoupling capacitors should be placed as close to their associated pins as possible. In general, the physical loop with the power supply pins, decoupling capacitors and GND return path to the device pins must be kept as short as possible and with as little area as possible to minimize induction (see reference board documentation for additional information).

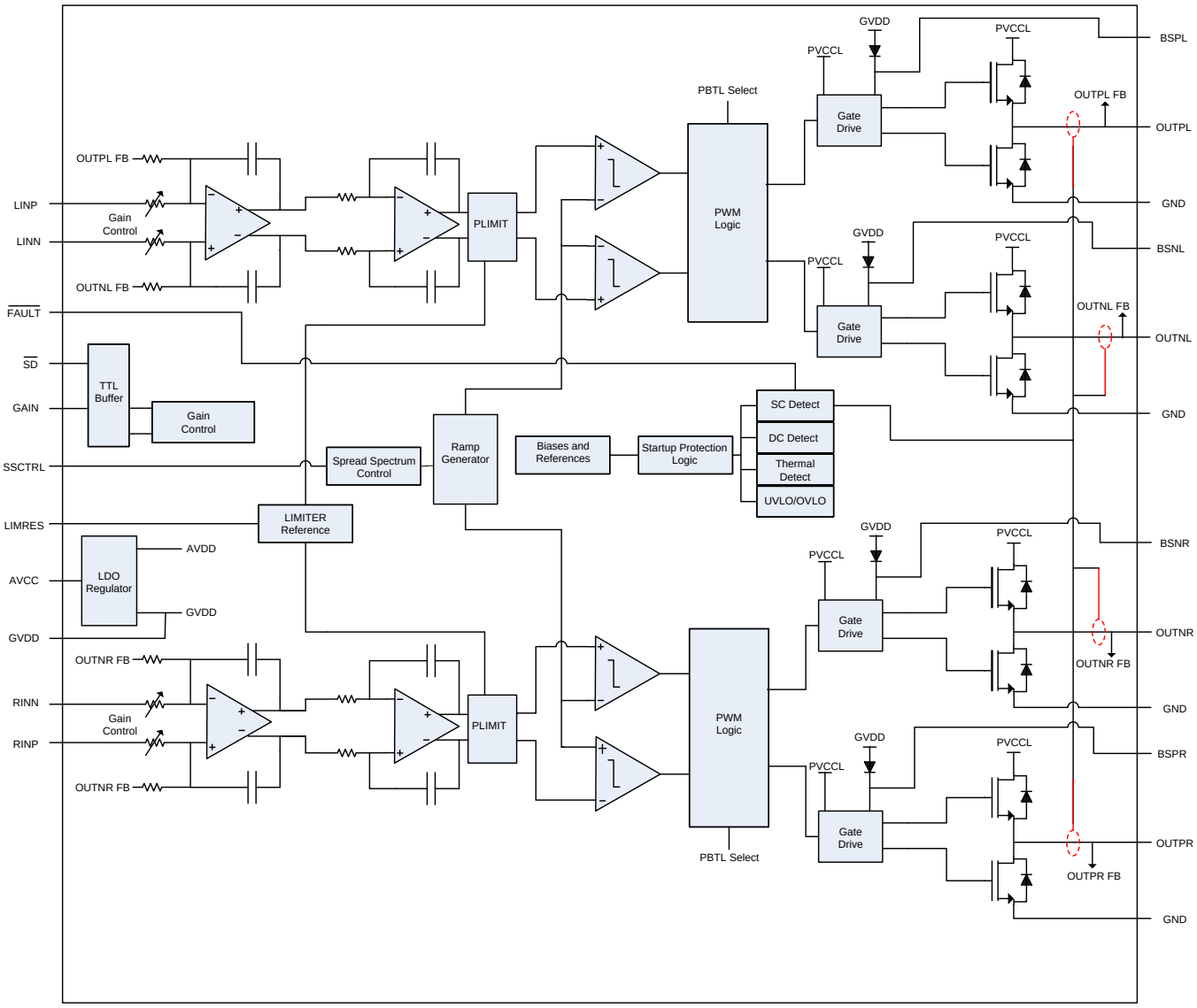
For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BSXX) to the power-stage output pin (OUTXX). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range of 310 kHz, use ceramic capacitors with at least 220-nF capacitance, size 0603 or 0805, for the bootstrap supply. These capacitors ensure sufficient energy storage, even during clipped low frequency audio signals, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of its ON cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. For optimal electrical performance, EMI compliance, and system reliability, each PVCC pin should be decoupled with ceramic capacitors that are placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TPA3144D2 reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The PVCC power supply should have low output impedance and low noise. The power-supply ramp and $\overline{SD}$ release sequence is not critical for device reliability as facilitated by the internal power-on-reset circuit, but it is recommended to release $\overline{SD}$ after the power supply is settled for minimum turn on audible artifacts.

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9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Gain Setting via GAIN Pin

The gain of the TPA3144D2 is set by a voltage applied to the GAIN pin, which is set by a resistor voltage divider with GVDD as supply voltage. The resistance of the voltage divider should be a minimum of 100 kΩ in order not to overload the GVDD regulator of TPA3144D2.

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Feature Description (continued)

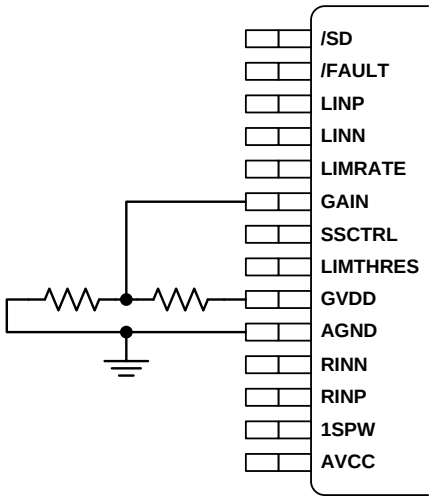


Figure 16. GAIN Pin Voltage Programming by GVDD Resistor Divider

The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_i) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors. The selected input gain is latched at device start up and cannot be changed when $\overline{SD}$ is high.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 7.2 kΩ, which is the absolute minimum input impedance of the TPA3144D2. At the lower gain settings, the input impedance could increase as high as 72 kΩ.

Table 1. Gain Setting

GAIN PIN VOLTAGE	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
	TYP	TYP
0 V (GND)	20	60
2.3 V (1/3·GVDD)	26	30
4.6 V (2/3·GVDD)	32	15
6.9 V (GVDD)	36	9

9.3.2 $\overline{SD}$ Operation

The TPA3144D2 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{SD}$ input pin should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{SD}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

9.3.3 Gain Limit Control, LIMTHRES and LIMRATE

The TPA3144D2 has built-in gain limiters with two operation modes for load and system protection: Voltage limiting and temperature limiting. The voltage limiting mode controls the TPA3144D2 voltage gain to limit the output signal without signal clipping, and the temperature control mode limits the device power dissipation to keep the die temperature within recommended operating conditions. Both voltage limiter and thermal limiter attack and release speeds (time per 0.5dB gain step) are controlled by the LIMRATE pin:

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Table 2. Speaker Guard AGL Settings

LIMRATE VOLTAGE	MODE	AGL ATTACK TIME	TFB ATTACK TIME	AGL/TFB RELEASE TIME
GVDD	FAST	40 µs	200 ms	400 ms
2/3·GVDD	MEDIUM	80 µs	400 ms	800 ms
1/3·GVDD	SLOW	160 µs	800 ms	1600 ms
GND	PLIMIT	DISABLED	DISABLED	DISABLED

LIMRATE accepts a 4-level input signal to setup operation. When LIMRATE is connected to GND, the voltage limiter function is changed to a hard clip action to control the maximum output voltage.

9.3.4 SPEAKERGUARD Automatic Gain Limit, AGL

The TPA3144D2 has a built-in SpeakerGuard AGL to limit excessive output voltage to a non clipping output signal. When an excessive level input signal is sent to TPA3144D2, the SpeakerGuard AGL will automatically reduce the amplifier gain to maintain maximum unclipped output signal to preserve high audio quality and to protect the attached speaker from excessive power. The AGL works with a fast attack speed and a slower release speed to achieve maximum protection and a minimum number of audible artifacts.

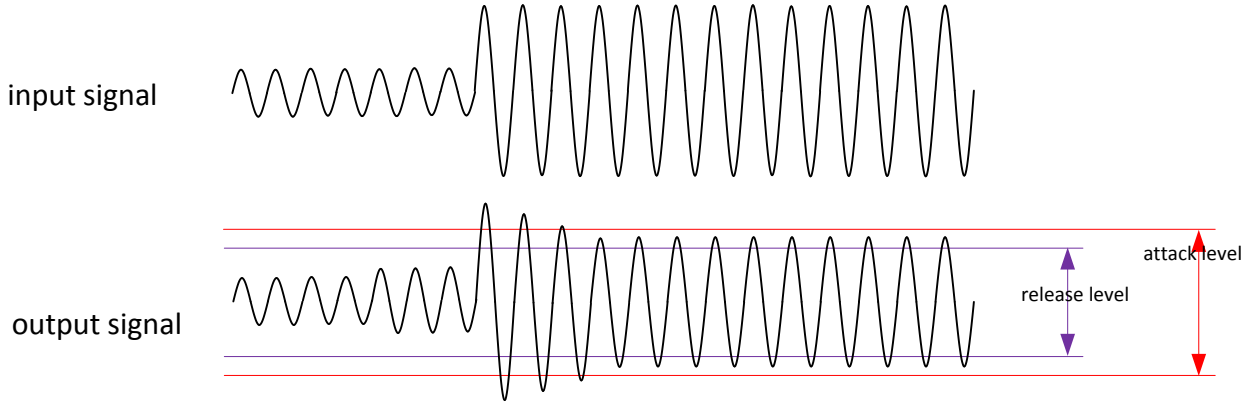


Figure 17. AGL Attack and Release Thresholds

When the input level multiplied by the TPA3144D2 closed loop gain exceeds the limiter threshold set by the LIMTHRES pin voltage, the TPA3144D2 closed loop gain is reduced by a single or by multiple 0.5-dB steps until the output signal voltage gets below the level set by the LIMTHRES pin voltage, or if a –12.0-dB gain reduction limit is reached. When the output voltage gets below the release threshold, the TPA3144D2 closed loop gain is increased by a single or by multiple 0.5-dB steps until the release threshold is reached, or the closed loop gain is at its nominal closed loop gain level. The AGL gain adjustment is applied with a ramp speed selectable by the LIMRATE pin setting.

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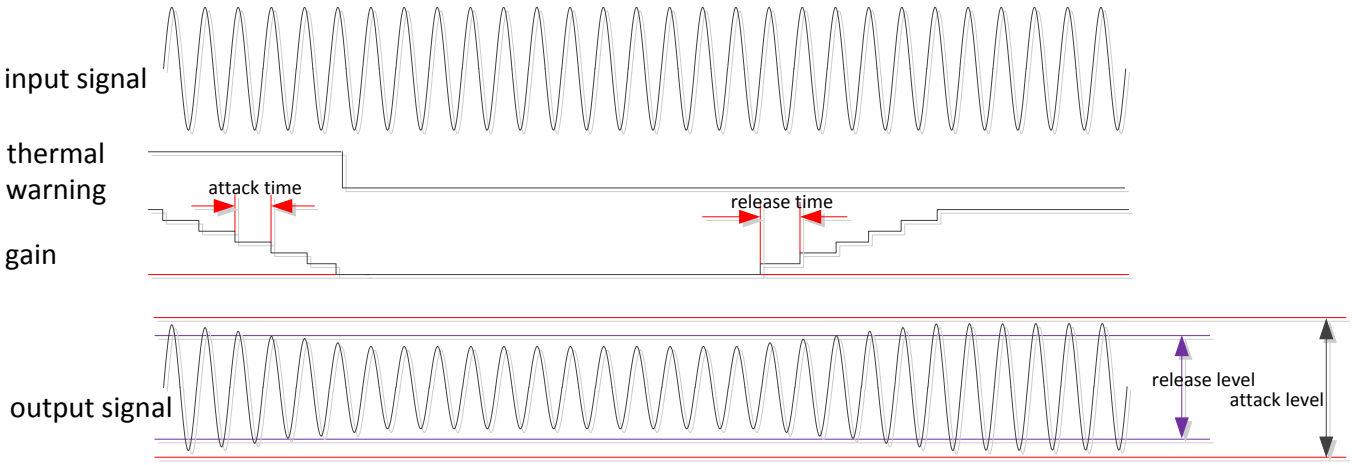


Figure 18. AGL Attack and Release Slopes

9.3.5 Thermal Foldback, TFB

The TPA3144D2 Thermal Foldback, TFB, is designed to protect the TPA3144D2 from excessive die temperature in case the device is operated beyond the recommended temperature or power limit, or with a weaker thermal system than recommended. The TFB works by reducing the on die power dissipation by reducing the TPA3144D2 closed loop gain in steps of 0.5 dB if the temperature trig point is exceeded. Once the die temperature drops below the TFB trig point, the TPA3144D2 closed loop gain is increased by a single or by multiple 0.5-dB steps until either the TFB trig point is reached, the closed loop gain attains the nominal closed loop gain level, or a maximum of 12-dB attenuation is reached, in which case the closed loop gain will be decreased again. The TFB gain adjustment is applied with a ramp speed selectable by the LIMRATE pin setting as shown in Table 2.

9.3.6 PLIMIT

The PLIMIT operation will, if selected, limit the output voltage level to a voltage level below the supply rail. In this case the amplifier operates as if it was powered by a lower supply voltage, and thereby limiting the output power by voltage clipping. PLIMIT threshold is set by the LIMTHRES pin voltage.

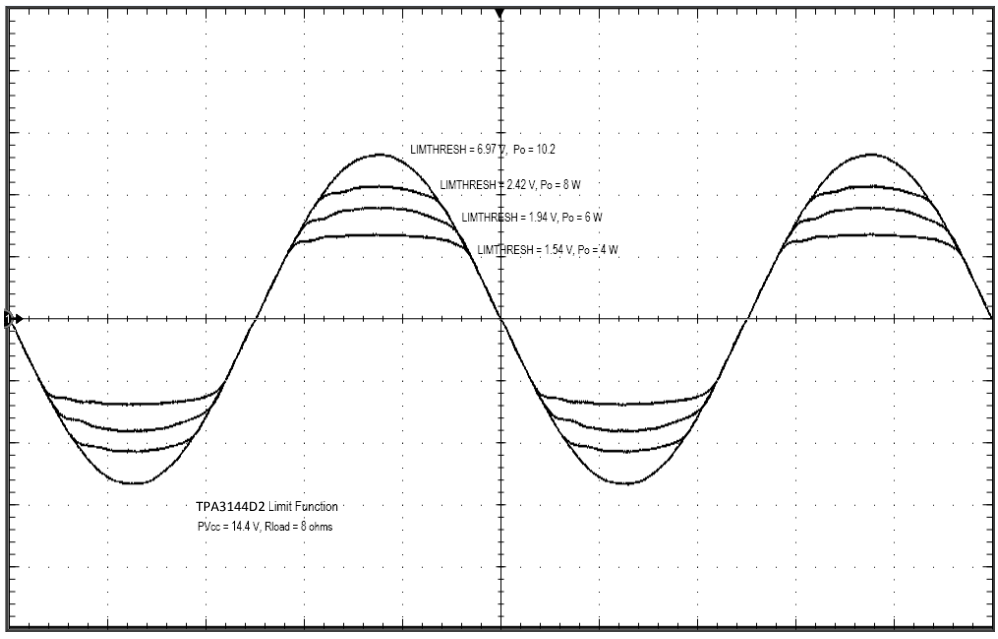


Figure 19. PLIMIT Circuit Operation

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9.3.7 LIMTHRES

The AGL and PLIMIT voltage threshold is set by the applied LIMTHRES voltage. The LIMTHRES voltage is set by a voltage divider from GVDD to GND. The limiting is done by limiting the amplifier output voltage to a fixed maximum value. This limit can be thought of as a "virtual" voltage rail, which is lower than the PVCC supply. This virtual rail is 4 times the voltage at the LIMTHRES pin. This output voltage can be used to calculate the maximum output voltage (unclipped using AGL and clipped using PLIMIT) and power for a given LIMTHRES voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \cdot R_S}\right) \cdot V_P\right)^2}{2 \cdot R_L}, \quad for\, unclipped\ \ power \tag{1}$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.

R_L is the load resistance.

V_P is the peak amplitude of the output possible within the supply rail.

V_P = 4 × LIMTHRES voltage if $V_P < P_{VCC}$

P_{OUT} = Maximum unclipped output power. 10%THD using PLIMIT: 1.25 × PMAX (unclipped)

Increasing the LIMTHRES voltage from a given value increases the maximum output voltage swing until it equals PVCC. Adjusting LIMTHRES to a higher value will disable both the AGL and PLIMIT function and will offer highest available output power, however it is always advised to use the LIMTHRES function if PVCC is higher than the nominal value to prevent shutdown due to over current protection or to reduce frequency of thermal foldback events. To disable the AGL or PLIMIT function, the LIMTHRES pin is simply connected to GVDD.

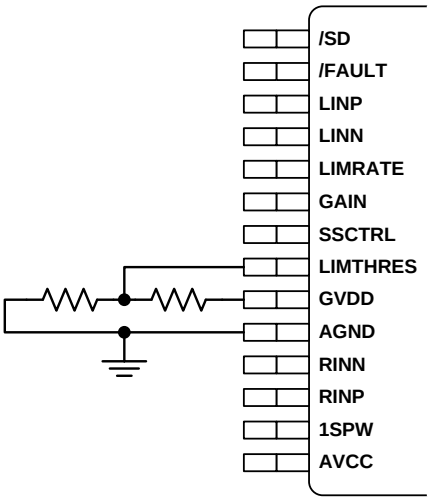


Figure 20. LIMHTRES Pin Voltage Programming by GVDD Resistor Divider

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Table 3. LIMTHRES Typical Operation

TEST CONDITIONS ()	LIMTHRES VOLTAGE (V)	R to GND	R to GVDD	OUTPUT POWER (W), UNCLIPPED, AGL	OUTPUT POWER (W), 10% THD, PLIMIT
PVCC = 12 V, R_L = 4 Ω	1.6	22 kΩ	68 kΩ	4.75	6
PVCC = 12 V, R_L = 6 Ω	1.9	33 kΩ	82 kΩ	4.75	6
PVCC = 12 V, R_L = 8 Ω	2.2	39 kΩ	82 kΩ	4.75	6

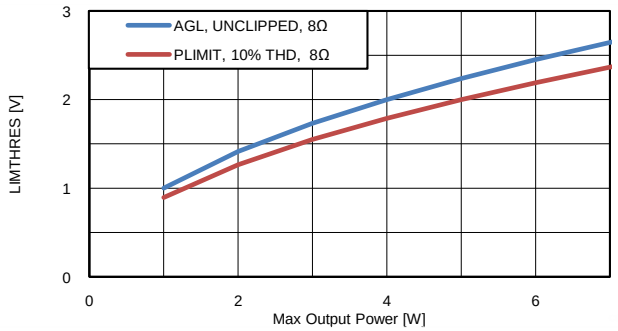


Figure 21. Max Output Power vs LIMTHRES, 8 Ω, PVCC = 12 V

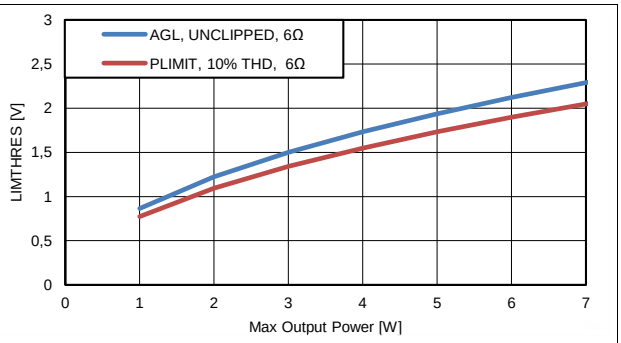


Figure 22. Max Output Power vs LIMTHRES, 6 Ω, PVCC = 12 V

9.3.8 Spread Spectrum and De-Phase Control

The TPA3144D2 has built-in spread spectrum control of the oscillator frequency and de-phase of the PWM outputs to improve EMI performance. Two spread spectrum schemes can be selected, and for operation without spread spectrum, de-phase can be turned off.

De-phase inverts the phase of the output PWM such that the idle output PWM waveforms of the two audio channels are inverted. De-phase does not affect the audio signal, or its polarity.

Spread spectrum mode and de-phase is selected by the applied SSCTRL voltage.

Table 4. Gain Setting

SSCTRL PIN VOLTAGE	SPREAD SPECTRUM MODULATION	DE-PHASE
0 V (GND)	OFF	OFF
2.3 V (1/3·GVDD)	OFF	ON
4.6 V (2/3·GVDD)	SS1 MODULATION	ON
6.9 V (GVDD)	SS2 MODULATION	ON

9.3.9 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the voltage divider circuits for LIMRATE, LIMTHRES, GAIN, and SSCTRL programming voltages.. Add a 1-μF capacitor to ground at this pin.

9.3.10 DC Detect

The TPA3144D2 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the $\overline{\text{FAULT}}$ pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z. To clear the DC Detect it is necessary to cycle the PVCC supply. Cycling $\overline{\text{SD}}$ will NOT clear a DC detect fault.

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A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 14% (for example, +57%, -43%) for more than 950 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the $\overline{SD}$ pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

The minimum differential input voltages required to trigger the DC detect are show in Table 5. The inputs must remain at or above the voltage listed in the table for more than 950 msec to trigger the DC detect.

Table 5. DC Detect Threshold, PVCC=12V

AV(dB)	Vin (mV, differential)	Vout (V, differential)
20	260	2.6
26	130	2.6
32	65	2.6
36	40	2.6

9.3.11 PBTL Select

The TPA3144D2 offers the feature of parallel BTL operation with two outputs of each channel connected directly. If the LINP and LINN input pins (pin 3 and 4) are tied low, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this PBTL (mono) mode, tie LINP and LINN inputs low to GND and apply the input signal to the RINP and RINN inputs and place the speaker between the LEFT and RIGHT outputs with OUTPL connected to OUTNL and OUTPR connected to OUTNR to parallel the output half bridges for highest power efficiency. For an example of the PBTL connection, see the schematic in the *Typical Applications* section.

9.3.12 Short-Circuit Protection and Automatic Recovery Feature

The TPA3144D2 has protection from overcurrent conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the $\overline{FAULT}$ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the $\overline{SD}$ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the $\overline{FAULT}$ pin directly to the $\overline{SD}$ pin. This allows the $\overline{FAULT}$ pin function to automatically drive the $\overline{SD}$ pin low which clears the short-circuit protection latch.

9.3.13 Thermal Protection

Thermal protection on the TPA3144D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the $\overline{FAULT}$ pin.

If automatic recovery from the thermal protection latch is desired, connect the $\overline{FAULT}$ pin directly to the $\overline{SD}$ pin. This allows the $\overline{FAULT}$ pin function to automatically drive the $\overline{SD}$ pin low which clears the thermal protection latch.

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9.4 Device Functional Modes

The TPA3144D2 has the option of running in either BD modulation or 1SPW modulation; this is set by the 1SPW pin.

1SPW = GND: BD-modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

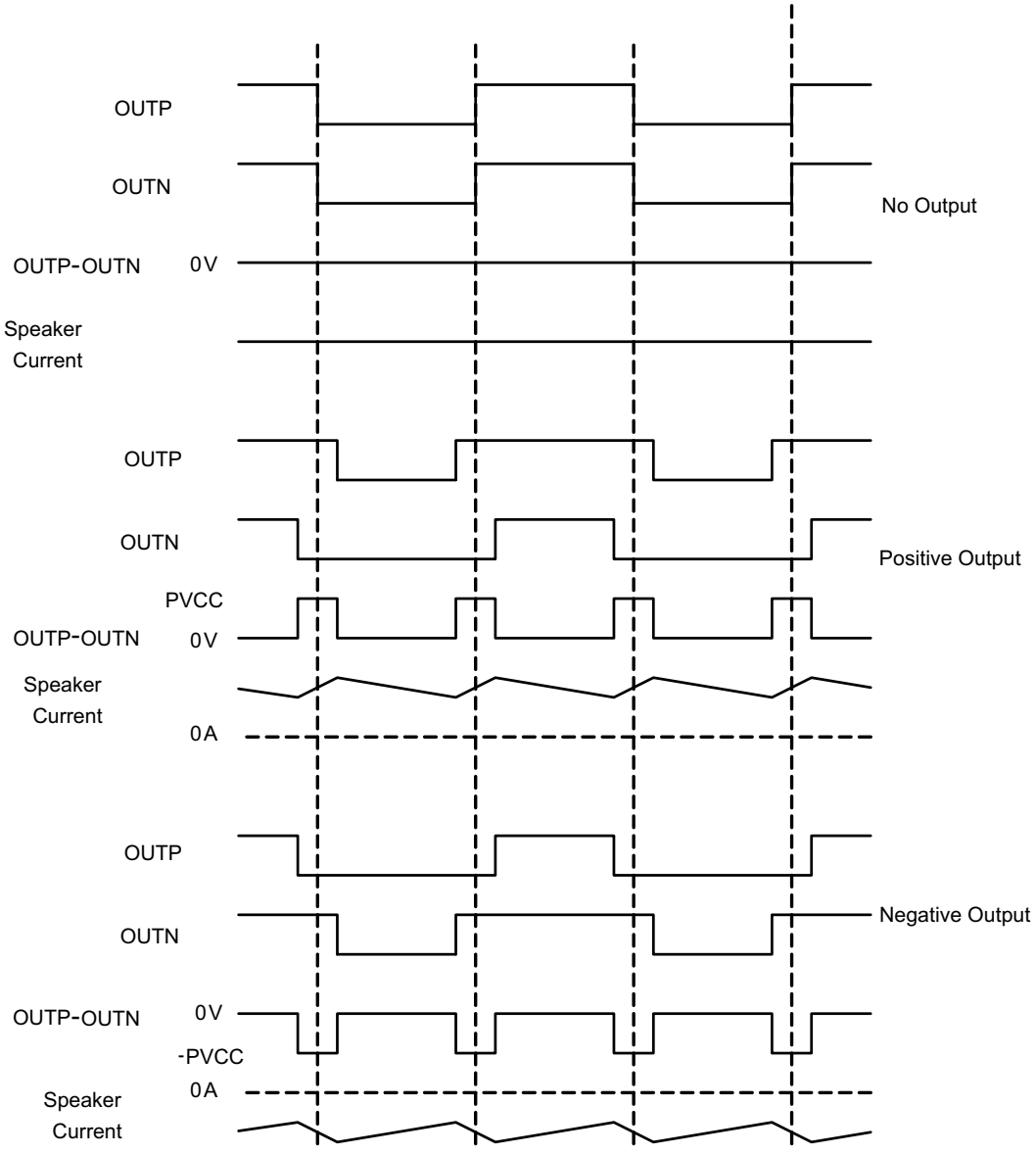


Figure 23. BD Mode Modulation

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Device Functional Modes (continued)

1SPW = HIGH: 1SPW-modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In 1SPW mode the outputs operate at ~15% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses. The THD penalty in 1SPW mode is minimized by the high performance feedback loop. The resulting audio signal at each half output has a discontinuity each time the output rails to GND. This can cause ringing in the audio reconstruction filter unless care is taken in the selection of the filter components and type of filter used.

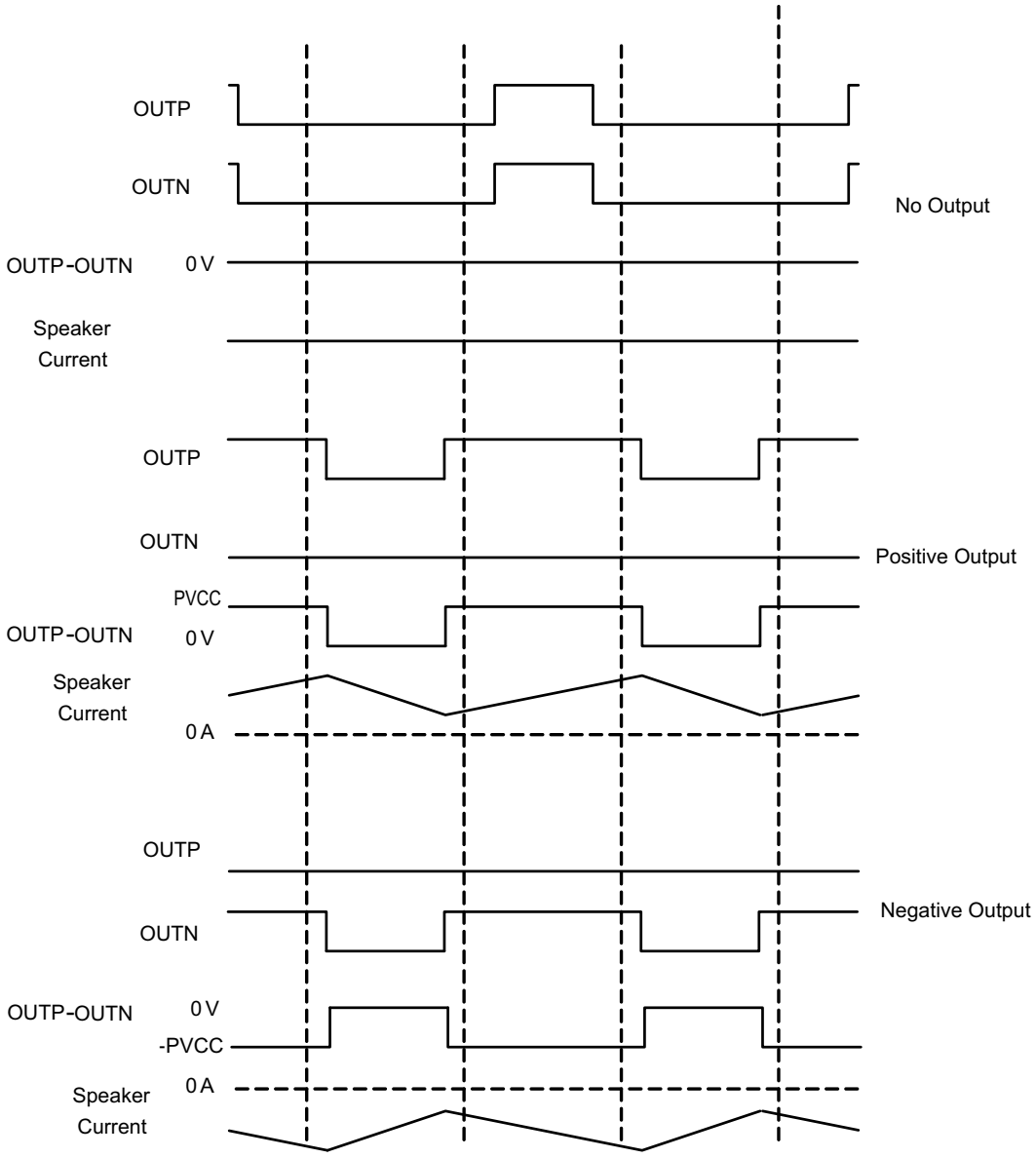


Figure 24. 1SPW Mode Modulation

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPA3144D2 is designed for use in inductor free applications with limited distance wire length) between amplifier and speakers like in TV sets, sound docks and Bluetooth speakers. The TPA3144D2 can either be configured in stereo or mono mode, depending on output power conditions. Depending on output power requirements and necessity for (speaker) load protection, the built in AGL or PLIMIT circuit can be used to control system power, see functional description of these features.

10.2 Typical Applications

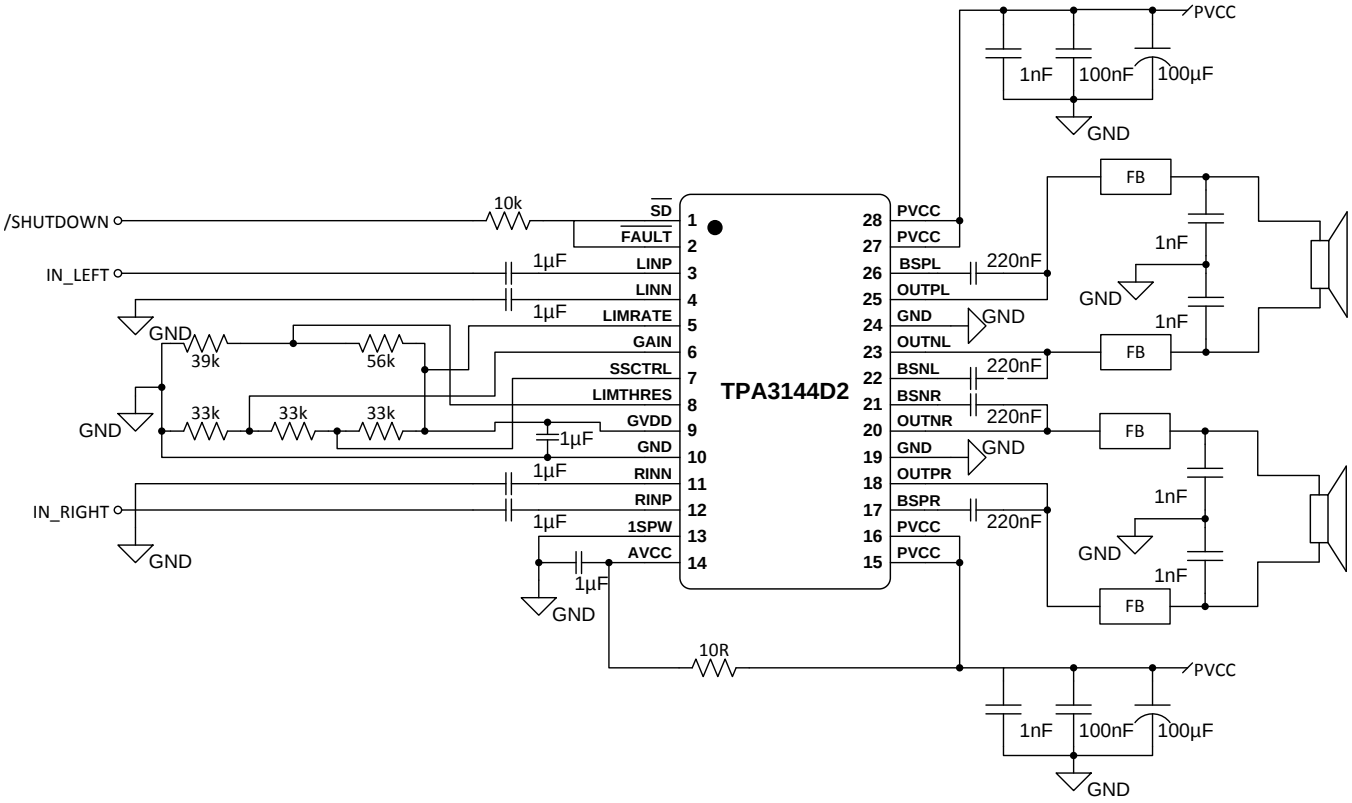
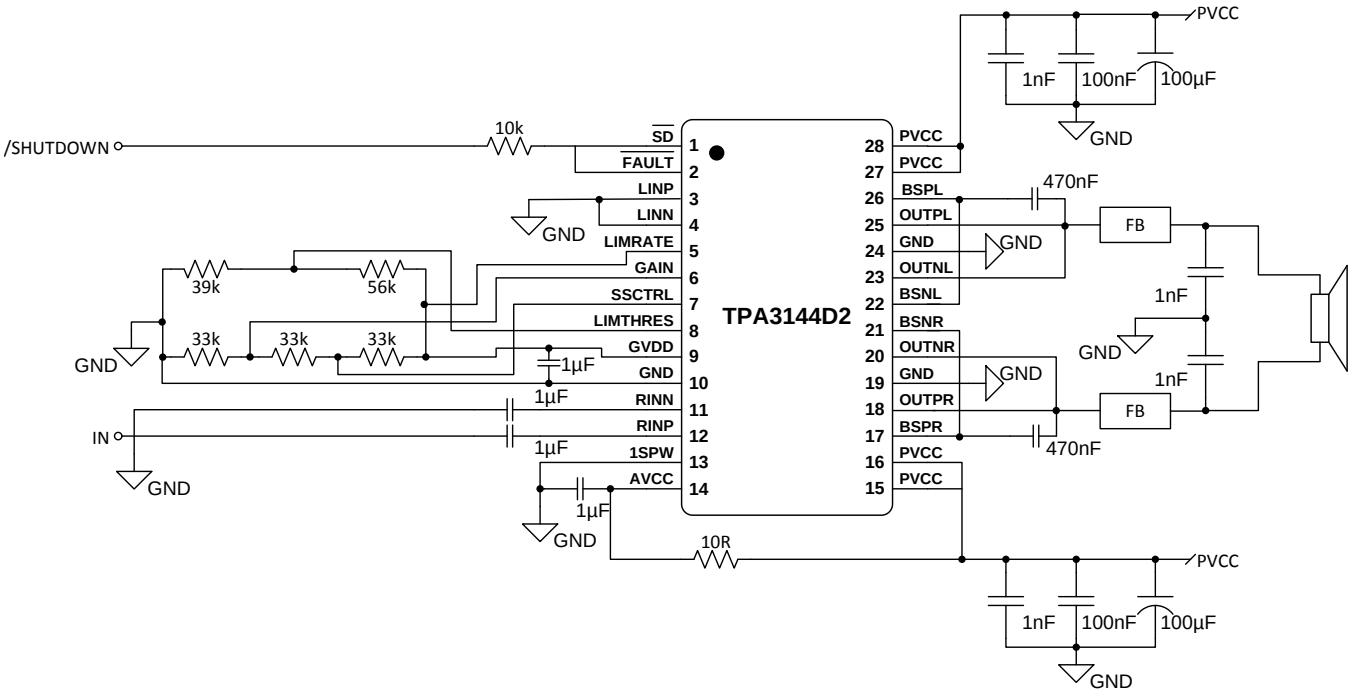


Figure 25. Stereo Class-D Amplifier with BTL Output and Single-Ended Inputs with Spread Spectrum Modulation

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Typical Applications (continued)



(1) 100-kΩ resistor is needed if the PVCC slew rate is more than 10 V/ms.

Figure 26. Stereo Class-D Amplifier with PBTL Output and Single-Ended Input with Spread Spectrum Modulation

10.2.1 Design Requirements

10.2.1.1 PCB Material Recommendation

FR-4 Glass Epoxy material with 1 oz. (35 µm) is recommended for use with the TPA3144D2. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance). It is recommended to use several GND underneath the device thermal pad for thermal coupling to a bottom side copper GND plane for best thermal performance.

10.2.1.2 PVCC Capacitor Recommendation

The large capacitors used in conjunction with each full-bridge, are referred to as the PVCC Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 100 µF, 16 V will support most applications with 12-V power supply. 25-V capacitor rating is recommended for power supply voltage higher than 12-V. For The PVCC capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

10.2.1.3 Decoupling Capacitor Recommendations

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the ceramic capacitors that are placed on the power supply to each full-bridge. They must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 16 V is required for use with a 12-V power supply.

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Typical Applications (continued)

10.2.2 Detailed Design Procedure

A rising-edge transition on $\overline{SD}$ input allows the device to start switching. It is recommended to ramp the PVCC voltage to its desired value before releasing $\overline{SD}$ for minimum audible artefacts.

The device is non-inverting the audio signal from input to output.

The GVDD pin is not recommended to be used as a voltage source for external circuitry.

10.2.2.1 Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the TPA3144D2 amplifier it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the Class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead's current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3144D2 include NFZ2MSM series from Murata.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class D outputs to ground. Suggested values for a simple RC series snubber network would be 10 Ω in series with a 330-pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the GND or the thermal pad beneath the chip.

10.2.2.2 Efficiency: LC Filter Required with the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{CC}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3144D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of $2 \times V_{CC}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

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Typical Applications (continued)

10.2.2.3 When to Use an Output Filter for EMI Suppression

The TPA3144D2 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 100 cm and high power. The TPA3144D2 EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, it LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

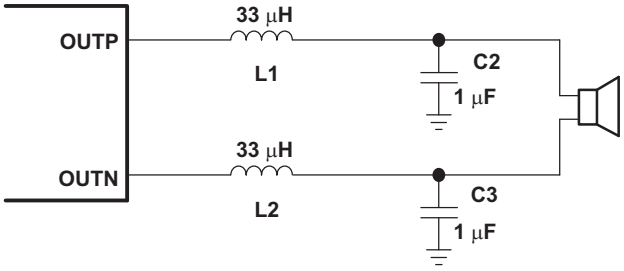


Figure 27. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8 Ω

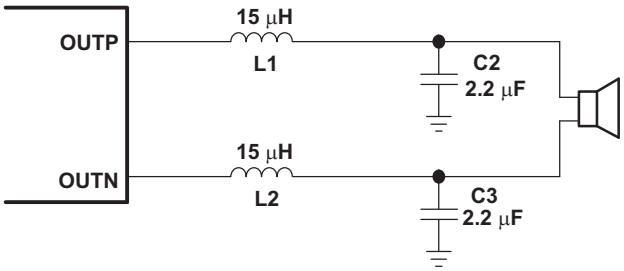


Figure 28. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 6 Ω

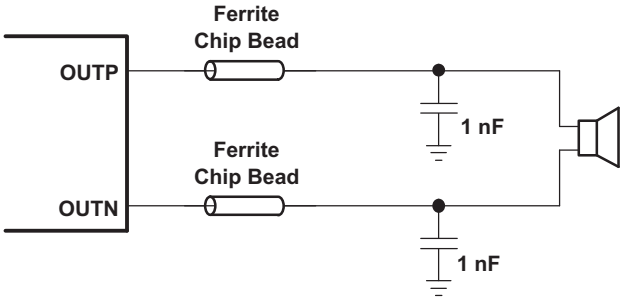


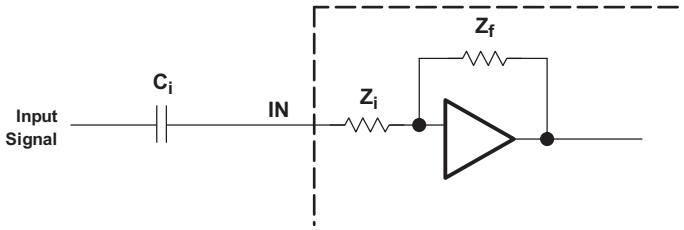
Figure 29. Typical Ferrite Chip Bead Filter (Chip Bead Example:)

10.2.2.4 Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 9 kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.

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Typical Applications (continued)



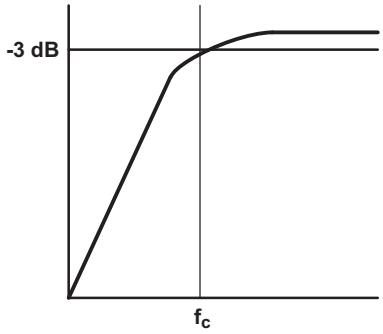
The -3-dB frequency can be calculated using Equation 2. Use the Z_i values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \quad (2)$$

10.2.2.5 Input Capacitor, C_i

In the typical application, an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined in Equation 3.

$$f_c = \frac{1}{2\pi Z_i C_i} \quad (3)$$



The value of C_i is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_i is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (4)$$

In this example, C_i is 0.13 µF; so, one would likely choose a value of 0.15 µF as this value is commonly used. If the gain is known and is constant, use Z_i from Table 1 to calculate C_i. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 3 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

10.2.2.6 BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22-µF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22-µF capacitor must be connected from OUTPx to BSPx, and one 0.22-µF capacitor must be connected from OUTNx to BSNx. (See the application circuit diagram in Figure 25.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

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Typical Applications (continued)

10.2.2.7 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3144D2 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3144D2 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 14 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

10.2.2.8 Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

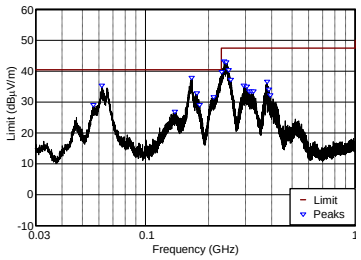
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Typical Applications (continued)

10.2.3 Application Performance Curves

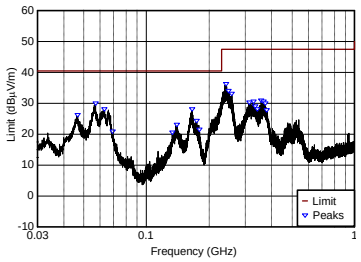
10.2.3.1 EN55013 Radiated Emissions Results

TPA3144D2 EVM, PVCC = 12 V, 8-Ω load, up to 1 meter speaker cable, Spread Spectrum enabled, P_O = 1.25 W



CISPR Class B 3m 30-1000MHz Scan#7- TPA3144D2 EVM with 8R Load, Different ferrite choke, Murata 601FB+1nF, 1-meter cable, Battery supply, SS-TRI, BD, 1.25W, Spkr Wire Config2

Figure 30. Radiated Emission - Horizontal



CISPR Class B 3m 30-1000MHz Scan#7- TPA3144D2 EVM with 8R Load, Different ferrite choke, Murata 601FB+1nF, 1-meter cable, Battery supply, SS-TRI, BD, 1.25W, Spkr Wire Config2

Figure 31. Radiated Emission - Vertical

Table 6. Radiated Emission - Horizontal

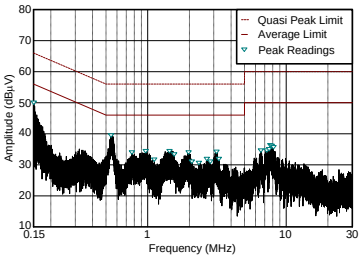
FREQUENCY MHz	LIMIT dBµV/m	PEAKS dBµV/m	Q-PEAK dBµV/m	MARGIN dB	TURN TABLE DEGREES	TOWER cm
166.246	40.457	21.781	21.975	–18.482	44.9	100
237.372	47.457	29.330	29.186	–18.271	326.9	100

Table 7. Radiated Emission - Vertical

FREQUENCY MHz	LIMIT dBµV/m	PEAKS dBµV/m	Q-PEAK dBµV/m	MARGIN dB	TURN TABLE DEGREES	TOWER cm
56.841	40.457	26.213	27.058	–13.399	54	100
241.9	47.457	19.429	20.430	–27.027	–0.1	100

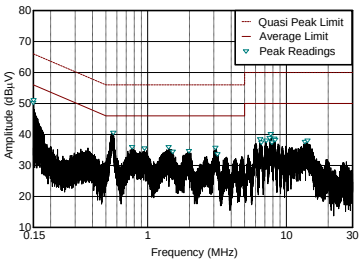
10.2.3.2 EN55022 Conducted Emissions Results

TV (40 inch) from the major TV manufacturer, TPA3144D2 EVM, PVCC = 12 V, 8-Ω speakers, Spread Spectrum enabled, P_O = 1.25 W



CISPR Class B 0.150-30MHz Idle Mode. SS0, Triangular, BD, 1.25 Watt

Figure 32. Conducted Emission - Line



CISPR Class B 0.150-30MHz Idle Mode. SS0, Triangular, BD, 1.25 Watt

Figure 33. Conducted Emission - Neutral

Table 8. Conducted Emission - Line

FREQUENCY MHz	QP LIMIT dBµV	AVE LIMIT dBµV	AVE READINGS dBµV	AVE MARGIN dB	QP READINGS dBµV	QP MARGIN dB
0.156	65.83	55.83	33.774	–22.056	45.956	–19.873
0.552	56	46	28.872	–17.128	39.164	–16.836
0.806	56	46	21.341	–24.659	29.585	–26.415
0.95	56	46	22.678	–23.322	31.471	–24.529
1.485	56	46	22.622	–23.378	31.082	–24.918
1.976	56	46	20.952	–25.048	29.849	–26.151

Table 9. Conducted Emission - Neutral

FREQUENCY MHz	QP LIMIT dBµV	AVE LIMIT dBµV	AVE READINGS dBµV	AVE MARGIN dB	QP READINGS dBµV	QP MARGIN dB
0.158	65.785	55.785	34.022	–21.763	45.398	–20.387
0.554	56	46	29.574	–16.426	40.485	–15.515
0.735	56	46	22.652	–23.348	32.52	–23.48
0.918	56	46	22.699	–23.301	31.849	–24.151
1.402	56	46	23.264	–22.736	32.173	–23.827
7.806	60	50	28.006	–21.994	35.214	–24.786

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11 Power Supply Recommendations

11.1 Power Supply Decoupling, C_S

The TPA3144D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either GND pins or thermal pad) as possible. For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 μF to 1 μF placed as close as possible to the device PVCC leads works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 μF or greater placed near the audio power amplifier is recommended. The 220-μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC pins provide the power to the output transistors, so a 220-μF or larger capacitor should be placed on each PVCC pin. A 10-μF capacitor on the AVCC pin is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class-D noise from entering the linear input amplifiers.

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12 Layout

12.1 Layout Guidelines

The TPA3144D2 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC pins as possible. Large (220 µF or greater) bulk power supply decoupling capacitors should be placed near the TPA3144D2 on the PVCCL and PVCCR supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger mid-frequency cap of value between 0.1µF and 1µF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The AVCC (pin 14) decoupling capacitor should be connected to ground (GND). The PVCC decoupling capacitors should connect to GND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TPA3144D2.
- Output filter—The ferrite EMI filter (Figure 29) should be placed as close to the output pins as possible for the best EMI performance. The LC filter (Figure 27 and Figure 28) should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 6.46 mm by 2.35 mm. Seven rows of solid vias (three vias per row, 0,3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. See the TI Application Report SLMA002 for more information about using the TSSOP thermal pad. For recommended PCB footprints, see figures at the end of this data sheet.

For an example layout, see the TPA3144D2 Evaluation Module (TPA3144D2 EVM) User Manual. Both the EVM user manual and the thermal pad application report are available on the TI Web site at http://www.ti.com.

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12.2 Layout Example

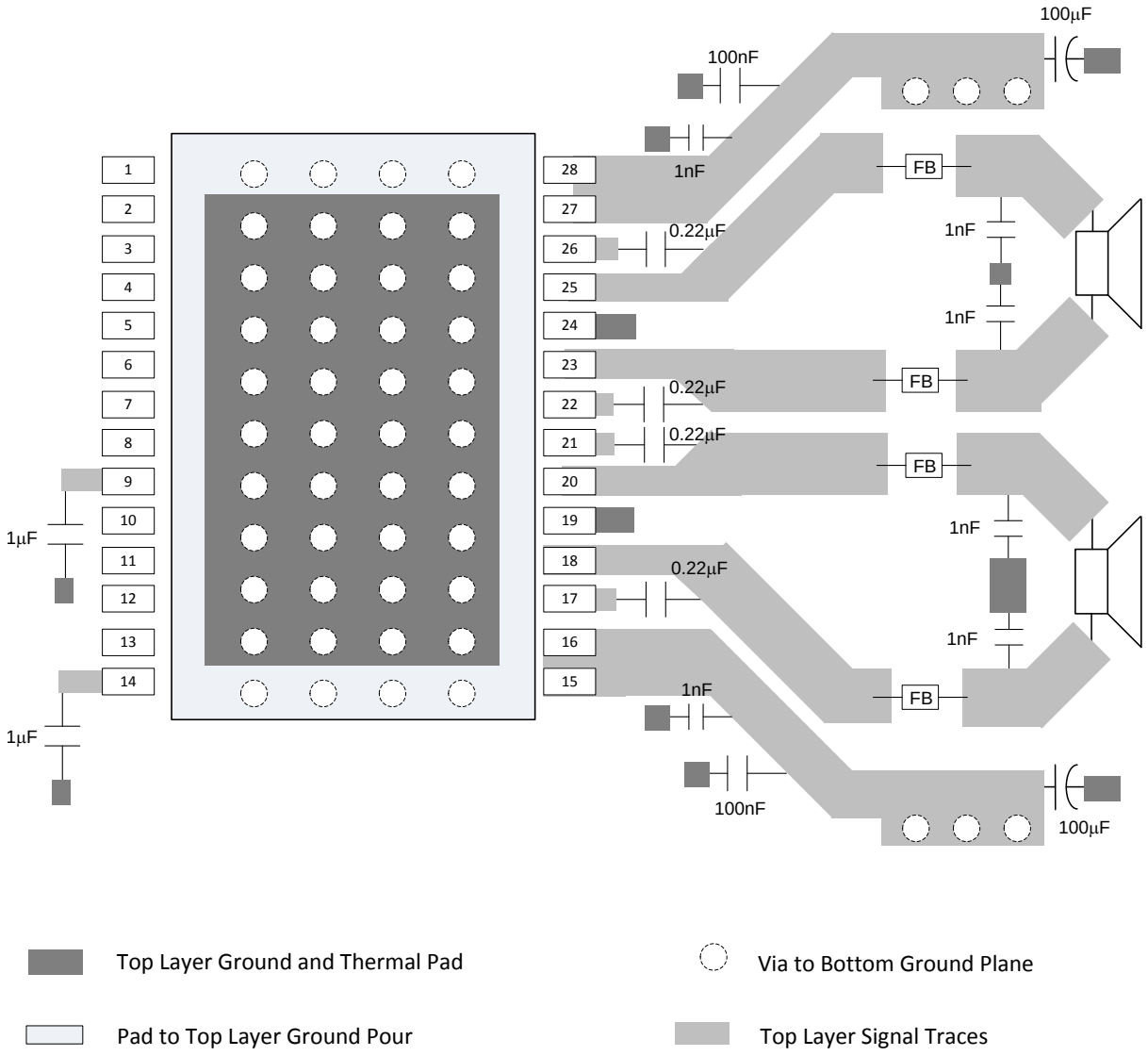


Figure 34. BTL Layout Example

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13 器件和文档支持

13.1 器件支持

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13.2 文档支持

13.2.1 相关文档

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13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA3144D2PWP	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3144D2
TPA3144D2PWP.A	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3144D2
TPA3144D2PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3144D2
TPA3144D2PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3144D2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

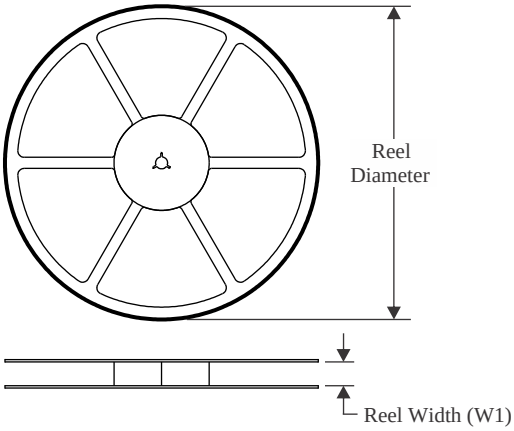
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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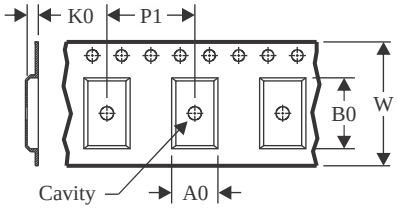
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

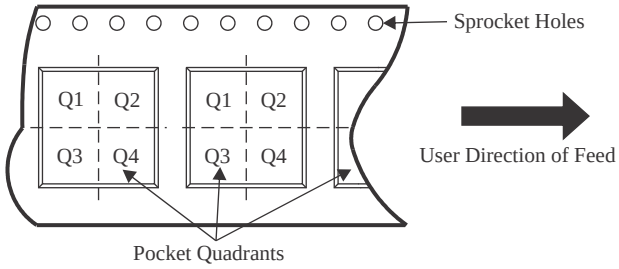


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

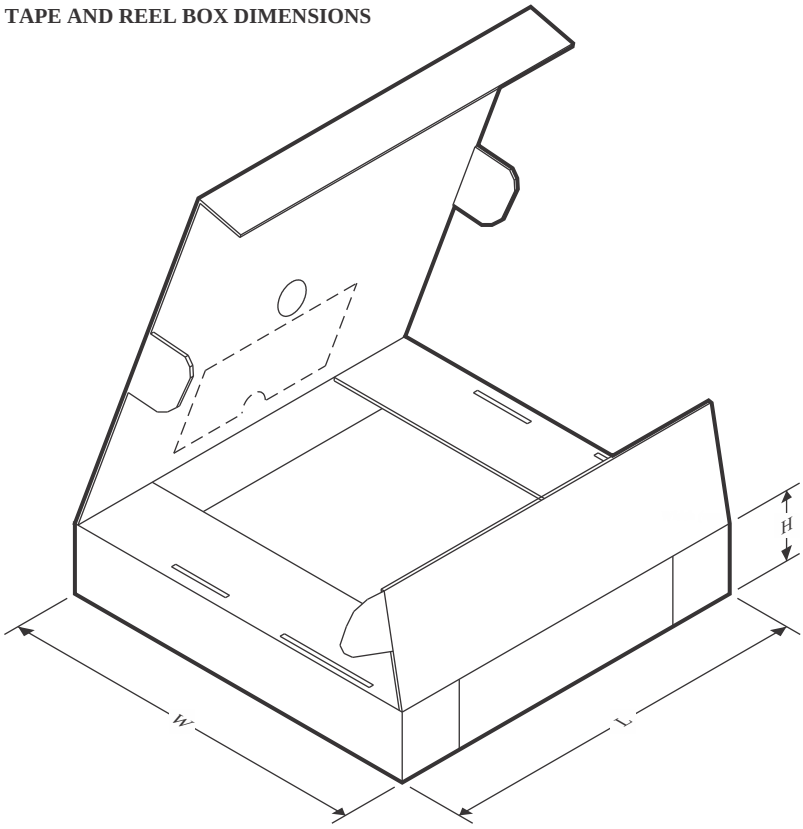
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3144D2PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

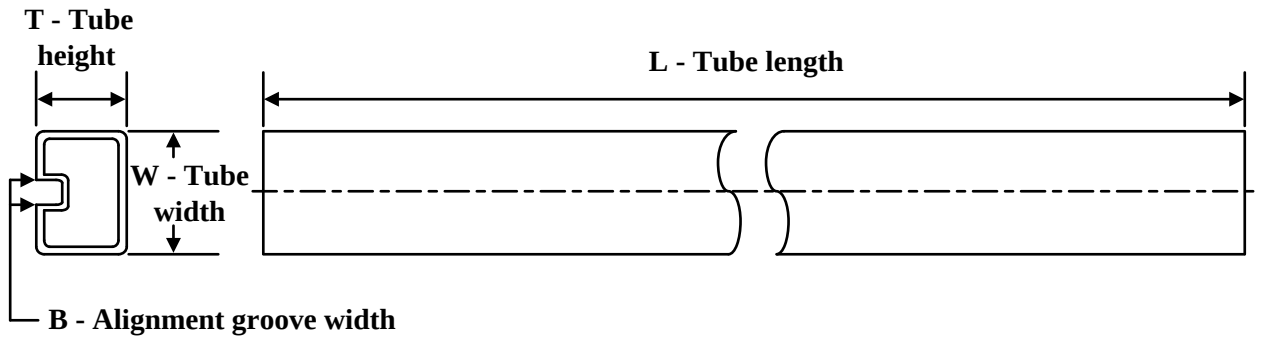
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3144D2PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3144D2PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPA3144D2PWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

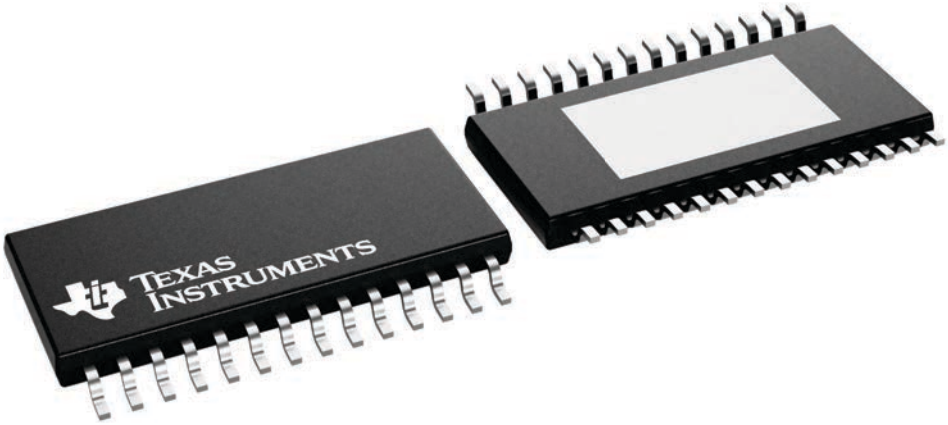
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

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最后更新日期：2025 年 10 月