PE64906

Product Specification

UltraCMOS® Digitally Tunable Capacitor (DTC), 100–3000 MHz

Features

- 3-wire (SPI compatible) serial interface with built-in bias voltage generation and ESD protection
- DuNE™ technology enhanced
- 5-bit, 32-state digitally tunable capacitor
- Shunt configuration C = 0.9–4.6 pF (5.1:1 tuning ratio) in discrete 119–fF steps
- High RF power handling (30 V_{PK} RF) and linearity
- Wide power supply range (2.3–4.8V) and low current consumption (typ. 140 µA at 2.75V)
- High ESD tolerance: 2 kV HBM on all pins
- Packaging: 10-lead 2 × 2 × 0.55 mm QFN

Applications

- Tunable antennas
- Tunable matching networks
- Tunable filter networks

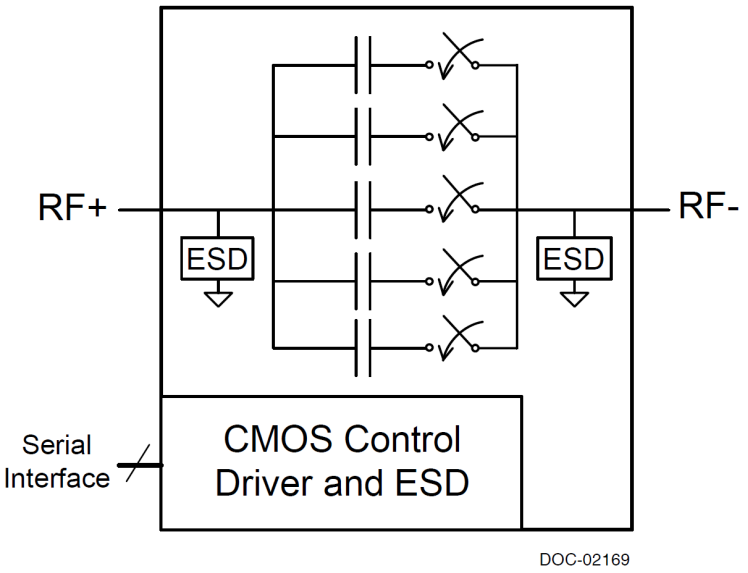


Figure 1. PE64906 functional diagram

Product description

The PE64906 is a DuNE™ technology-enhanced digitally tunable capacitor (DTC) based on pSemi's UltraCMOS® technology. This highly versatile product supports a wide variety of tuning circuit topologies with an emphasis on impedance matching and aperture tuning applications.

The PE64906 offers high RF power handling and ruggedness while meeting challenging harmonic and linearity requirements enabled by pSemi's HaRP™ technology. The device is controlled through the widely supported 3-wire (SPI compatible) interface. All decoding and biasing are integrated on-chip, and no external bypassing or filtering components are required.

DuNE devices feature ease of use while delivering superior RF performance in the form of tuning accuracy, monotonicity, tuning ratio, power handling, size, and quality factor. With built-in bias voltage generation and ESD protection, DTC products provide a monolithically integrated tuning solution for demanding RF applications.

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Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE64906 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
ESD voltage HBM(*)	V_{ESD}	–	2000	V
Note: * Human body model (MIL–STD 883 Method 3015.7)				

Recommended operating conditions

Table 2 lists the PE64906 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE64906 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.30	2.75	4.80	V
Supply current, V_{DD} = 2.75V	I_{DD}	–	140	200	µA
Standby current, V_{DD} = 2.75V	I_{DD}	–	25	–	µA
Digital input high	V_{IH}	1.2	1.8	3.1	V
Digital input low	V_{IL}	0	0	0.57	V
RF input power (50Ω):(1) - 698–915 MHz - 1710–1910 MHz	–	–	–	 +34 +32	dBm
Peak operating RF voltage:(2) - V_P to V_M - V_P to RFGND	–	–	–	 30 30	V_{PK}
Operating temperature range	T_{OP}	-40	+25	+85	°C
Storage temperature range	T_{ST}	-65	+25	+150	°C

Notes:
1. Maximum power available from 50Ω source. Pulsed RF input with 4620-µS period, 50% duty cycle, measured per 3GPP TS 45.005, and measured in shunt between 50Ω ports with RF- connected to GND.
2. Node voltages are defined per the equivalent circuit model schematic in Figure 11. When the DTC is used as a part of reactive network, the impedance transformation could cause the internal RF voltages (V_P and V_M) to exceed the peak operating RF voltage even with the specified RF input power levels. For operation above +20 dBm (100 mW), the complete RF circuit must be simulated using the actual input power and load conditions, and the internal node voltages (V_P and V_M in Figure 11) monitored to not exceed 30 V_{PK}.

Electrical specifications

Table 3 lists the PE64906 key electrical specifications at +25 °C and V_{DD} = 2.8V, unless otherwise specified.

Table 3. PE64906 electrical specifications

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency	–	100	–	3000	MHz
Minimum capacitance, C_{min}	State = 00000, 100 MHz	0.81	0.9	0.99	pF
Maximum capacitance, C_{max}	State = 11111, 100 MHz	3.68	4.6	5.52	pF
Tuning ratio	C_{max}/C_{min}, 100 MHz	–	5.1:1	–	–
Step size	5 bits, 32 states, 100 MHz	–	0.119	–	pF
Quality factor at C_{min}(1)	698–960 MHz with L_S removed 1710–2170 MHz with L_S removed	–	40 40	–	–
Quality factor at C_{max}(1)	698–960 MHz with L_S removed 1710–2170 MHz with L_S removed	–	29 13	–	–
Self-resonant frequency (SRF)	State 00000 State 11111	–	7.9 2.8	–	GHz
Harmonics(2)	2fo, 3fo: 698–915 MHz; P_{IN} = +34 dBm, 50Ω 2fo, 3fo: 1710–1910 MHz; P_{IN} = +32 dBm, 50Ω	–	–	-36 -36	dBm
IMD3	Bands I, II, V/VIII, +20 dBm CW at TX freq, –15 dBm CW at 2TX-RX freq, 50Ω	–	–	-105	dBm
Third-order intercept point (IP3)	Shunt configuration derived from IMD3 spec IP3 = $(2P_{TX} + P_{block} – IMD3) / 2$	–	65	–	dBm
Switching time(3)	State change to 10/90% delta capacitance between only two states.	–	–	12	µs
Startup time(3)	Time from V_{DD} within the specification to all performances within the specification.	–	–	70	µs
Wake-up time(3)	State change from standby mode to RF state to all performances within the specification.	–	–	70	µs

Notes:
1. Q for a shunt DTC is based on a series RLC equivalent circuit. $Q = X_C / R = (X - X_L) / R$, where $X = X_L + X_C$, $X_L = 2 \times \pi \times f \times L$, $X_C = -1 / (2 \times \pi \times f \times C)$, which is equal to removing the effect of parasitic inductance L_S.
2. In shunt between 50Ω. Pulsed RF input with 4620-µs period, 50% duty cycle, measured per 3GPP TS 45.005.
3. To achieve the specified performance, provide a DC path to ground at RF–.

Typical performance data

Figures 2–8 show the typical performance data at +25 °C and 2.75V, unless otherwise specified.

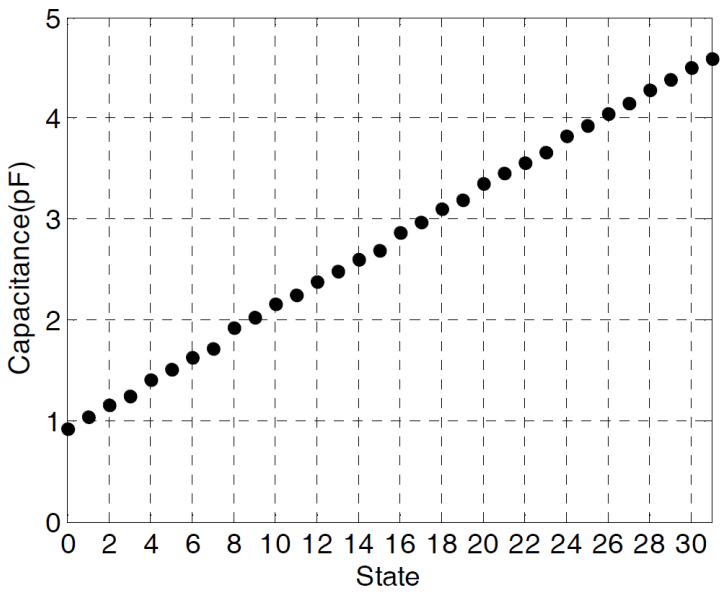


Figure 2. Measured shunt C (at 100 MHz) vs state

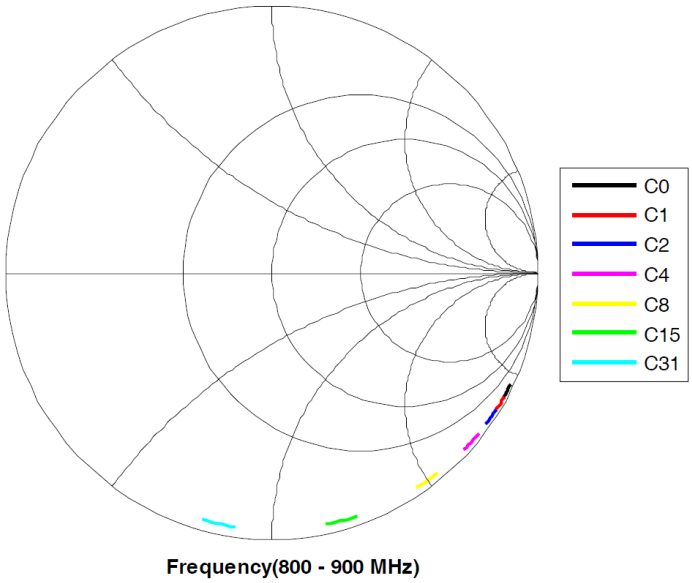


Figure 3. Measured shunt S_{11} (major states)

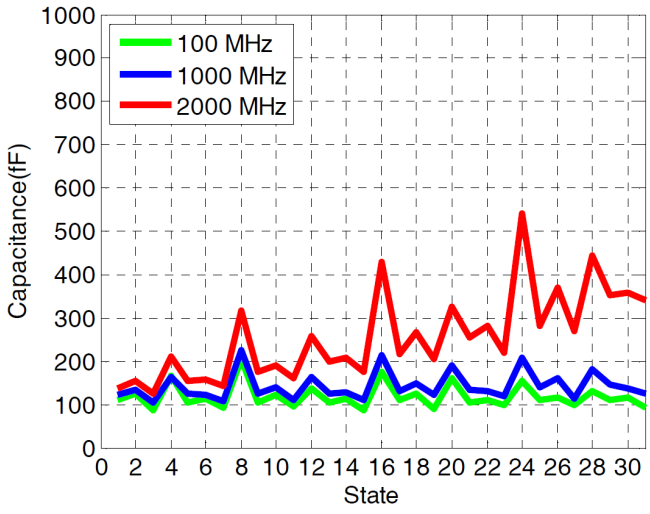


Figure 4. Measured step size vs. state (fequency)

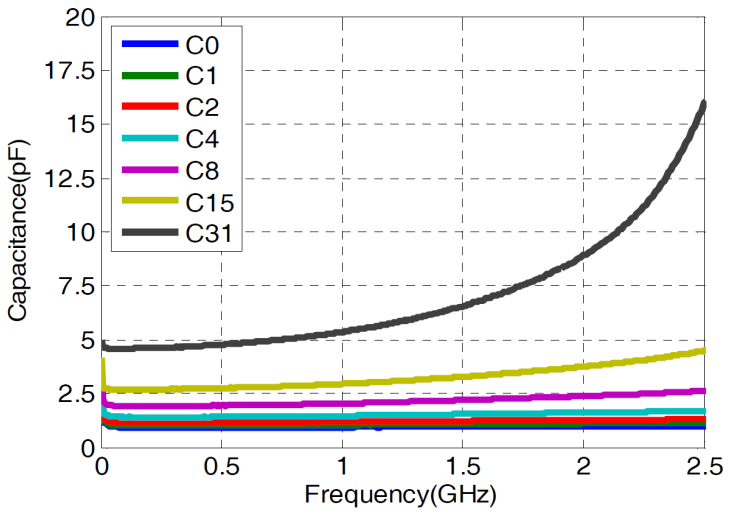


Figure 5. Measured shunt C vs. frequency

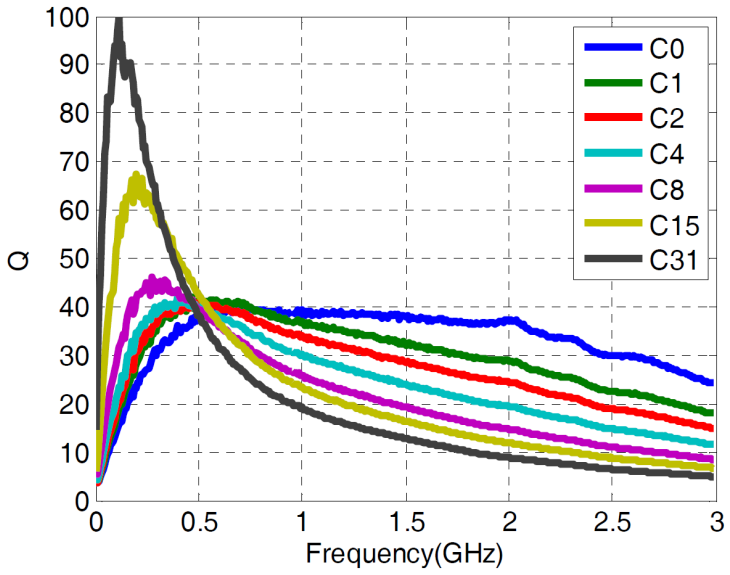


Figure 6. Measured shunt Q vs. frequency (major states)

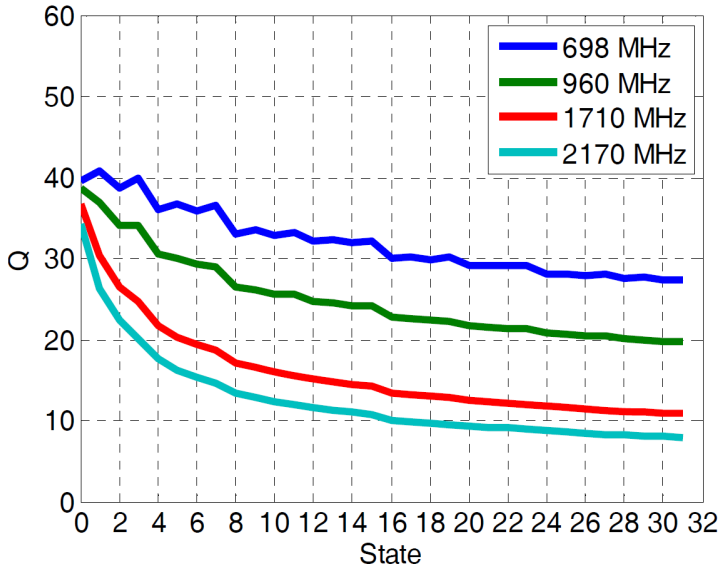


Figure 7. Measured shunt Q vs. state

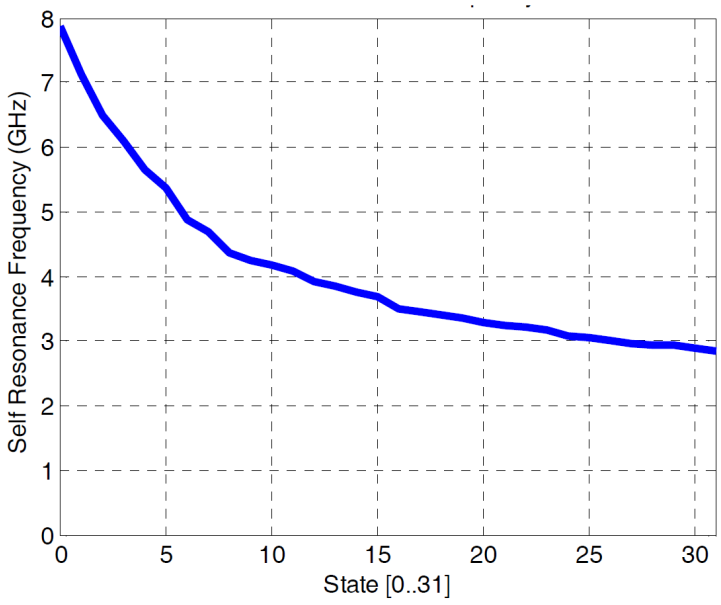


Figure 8. Measured self resonance frequency

Serial interface operation and sharing

The PE64906 is controlled by a 3-wire SPI-compatible interface. As shown in Figure 9, the serial master initiates the start of a telegram by driving the Serial Enable (SEN) line high. Each bit of the 8-bit telegram is clocked in on the rising edge of the Serial Clock (SCL) line. The Serial Data (SDA) bits are clocked by the most significant bit (MSB) first, as shown in Table 4 and Figure 9. Transactions on SDA are allowed on the falling edge of SCL. The DTC activates the data on the falling edge of SEN. The DTC does not count how many bits are clocked and only maintains the last eight bits it received.

You can control multiple DTCs with a single interface by using a dedicated enable (SEN) line for each DTC. The SDA, SCL, and V_{DD} lines can be shared, as shown in Figure 10. The dedicated SEN lines act as a chip select, so each DTC only responds to serial transactions intended for it. This makes each DTC change states sequentially as it is programmed.

Alternatively, you can use a dedicated SDA line with a common SEN. This allows all DTCs to change states simultaneously but requires all DTCs to be programmed even if the state is not changed.

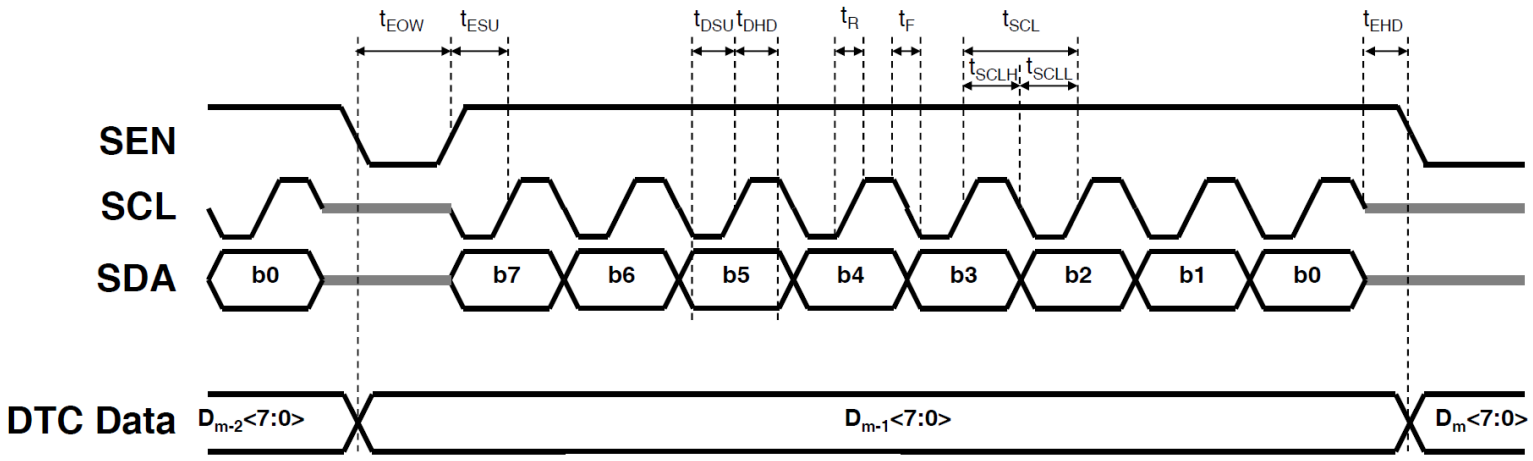


Figure 9. Serial interface timing diagram (oscilloscope view)

Table 4. Register map

b7	b6	b5	b4	b3	b2	b1	b0
0(1)	0(1)	STB(2)	d4	d3	d2	d1	d0
↑ MSB (first in)							LSB (last in) ↑

Notes:
1. These bits are reserved and must be written to 0 for proper operation.
2. The DTC is active when low (set to 0) and in low-current standby mode when high (set to 1).

In Table 5, V_{DD} = 2.75V and -40 °C < T_A < +85 °C, unless otherwise specified.

Table 5. Serial interface timing characteristics

Parameter	Symbol	Min	Max	Unit
Serial clock period	t_{SCL}	38.4	–	ns
SCL low time	t_{SCLL}	13.2	–	
SCL high time	t_{SCLH}	13.2	–	
SCL, SDA, SEN rise time	t_R	–	6.5	
SCL, SDA, SEN fall time	t_F	–	6.5	
SEN rising edge to SCL rising edge	t_{ESU}	19.2	–	
SCL rising edge to SEN falling edge	t_{EHD}	19.2	–	
SDA valid to SCL rising edge	t_{DSU}	13.2	–	
SDA valid after SCL rising edge	t_{DHD}	13.2	–	
SEN falling edge to SEN rising edge	t_{EOW}	38.4	–	

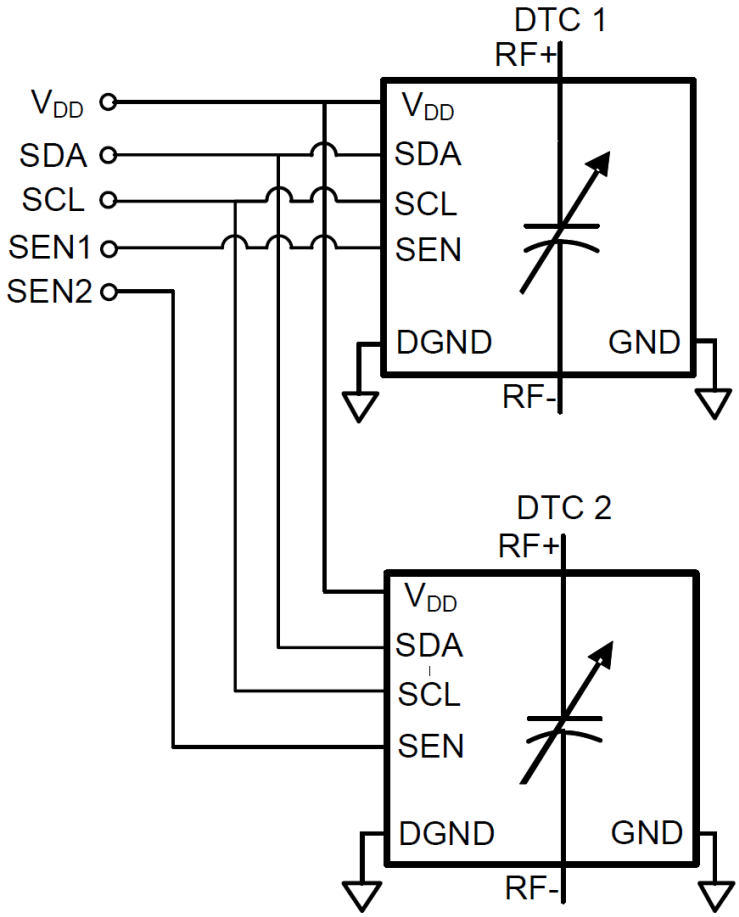


Figure 10. Recommended bus sharing

Equivalent circuit model description

The DTC equivalent circuit model includes all parasitic elements and is accurate in both series and shunt configurations, reflecting physical circuit behavior accurately and providing close correlation to measured data. It can easily be used in circuit simulation programs.

For the V_P and V_M maximum operating limits, see Table 2.

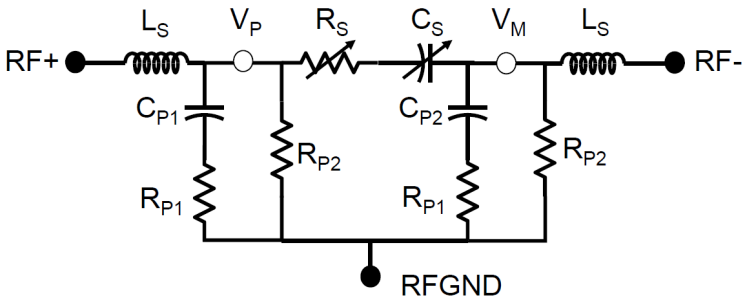


Figure 11. Equivalent circuit model schematic

Table 6. Equivalent circuit model parameters

Variable	Equation (state = 0, 1, 2 ...31)	Unit
C_S	0.127 × state + 0.38	pF
R_S	20 / (state + 20 / (state + 0.7)) + 0.7	Ω
R_{P1}	8 + 3 × (state)	Ω
R_{P2}	25000 + 3 × $(state)^3$	Ω
C_{P1}	-0.0075 × state + 0.52	pF
C_{P2}	0.0096 × state + 0.61	pF
L_S	0.35	nH

Table 7. Equivalent circuit data

State			DTC core		Parasitic elements			
Hex	Binary	Decimal	CS (pF)	RS (Ω)	CP1 (pF)	CP2 (pF)	RP1 (Ω)	RP2 (kΩ)
0x00	00000	0	0.38	1.40	0.52	0.61	8.0	25.0
0x01	00001	1	0.51	2.27	0.51	0.62	11.0	25.0
0x02	00010	2	0.63	2.83	0.51	0.63	14.0	25.0
0x03	00011	3	0.76	3.08	0.50	0.64	17.0	25.1
0x04	00100	4	0.89	3.12	0.49	0.65	20.0	25.2
0x05	00101	5	1.02	3.05	0.48	0.66	23.0	25.4
0x06	00110	6	1.14	2.93	0.48	0.67	26.0	25.6
0x07	00111	7	1.27	2.78	0.47	0.68	29.0	26.0
0x08	01000	8	1.40	2.64	0.46	0.69	32.0	26.5
0x09	01001	9	1.52	2.51	0.45	0.70	35.0	27.2
0x0A	01010	10	1.65	2.39	0.45	0.71	38.0	28.0
0x0B	01011	11	1.78	2.27	0.44	0.72	41.0	29.0
0x0C	01100	12	1.90	2.17	0.43	0.73	44.0	30.2
0x0D	01101	13	2.03	2.08	0.42	0.73	47.0	31.6
0x0E	01110	14	2.16	2.00	0.42	0.74	50.0	33.2
0x0F	01111	15	2.29	1.93	0.41	0.75	53.1	35.1
0x10	10000	16	2.41	1.86	0.40	0.76	56.0	37.3
0x11	10001	17	2.54	1.80	0.39	0.77	59.0	39.7
0x12	10010	18	2.67	1.75	0.39	0.78	62.0	42.5
0x13	10011	19	2.79	1.70	0.38	0.79	65.0	45.6
0x14	10100	20	2.92	1.65	0.37	0.80	68.0	49.0
0x15	10101	21	3.05	1.61	0.36	0.81	71.0	52.8
0x16	10110	22	3.17	1.57	0.36	0.82	74.0	56.9
0x17	10111	23	3.30	1.54	0.35	0.83	77.0	61.5
0x18	11000	24	3.43	1.51	0.34	0.84	80.0	66.5
0x19	11001	25	3.56	1.48	0.33	0.85	83.0	71.9
0x1A	11010	26	3.68	1.45	0.33	0.86	86.0	77.7
0x1B	11011	27	3.81	1.42	0.32	0.87	89.0	84.0
0x1C	11100	28	3.94	1.40	0.31	0.88	92.0	90.9
0x1D	11101	29	4.06	1.37	0.30	0.89	95.0	98.2

State			DTC core		Parasitic elements			
Hex	Binary	Decimal	CS (pF)	RS (Ω)	CP1 (pF)	CP2 (pF)	RP1 (Ω)	RP2 (kΩ)
0x1E	11110	30	4.19	1.35	0.30	0.90	98.0	106.0
0x1F	11111	31	4.32	1.33	0.29	0.91	101.0	114.4

Series operation

In series configuration, the effective capacitance between the RF+ and RF- ports is represented by C_S.

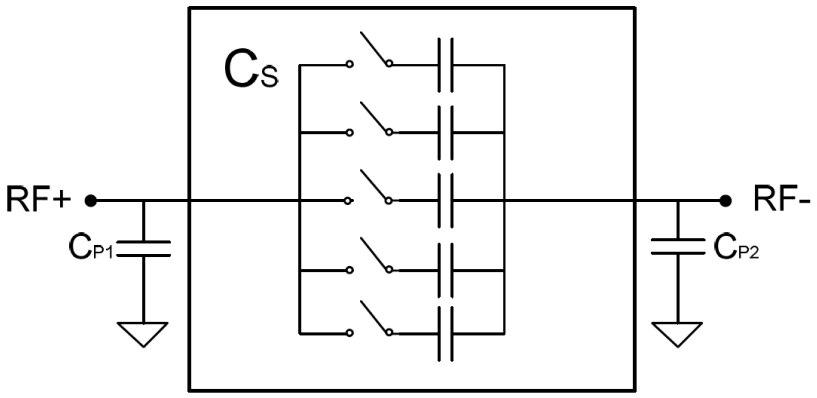


Figure 12. Effective capacitance diagram

The shunt configuration (looking into RF+ when RF- is grounded) has a higher total capacitance at RF+ due to the parallel combination of C_S with parasitic capacitance C_{P1} (C_S + C_{P1}), as shown in Figure 13 and Table 8.

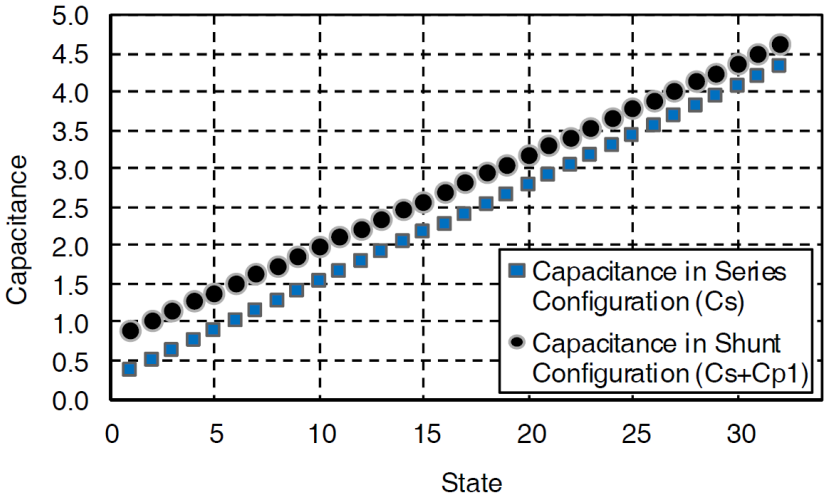


Figure 13. Typical capacitance vs. state

Table 8. Effective capacitance summary

Configuration	Effective capacitance	C_{min} (state 0)	C_{max} (state 31)	Tuning ratio
Series, RF+ to RF-	C_S	0.38	4.32	11.4:1
Shunt, RF+ to GND	C_S + C_{P1}	0.90	4.6	5.1:1

Figure 14 and Figure 15 show S_{11} and S_{21} for series configuration. S_{21} includes mismatch and dissipative losses and is not indicative of tuning network loss. To simulate the tuning network loss, use the equivalent circuit model (Figure 11).

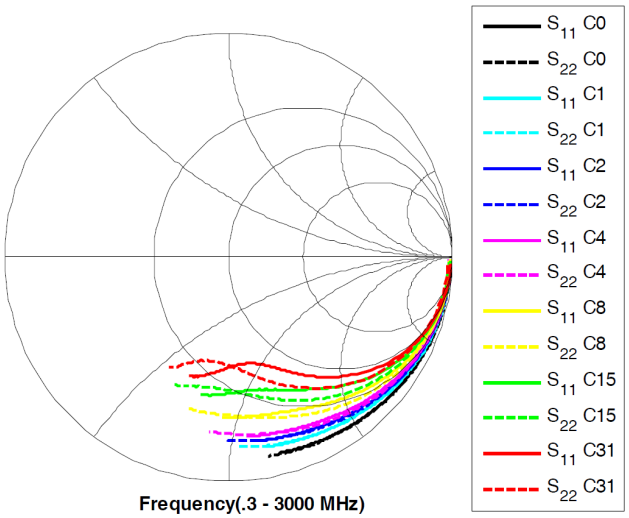


Figure 14. Measured series S_{11}/S_{22} (major states)

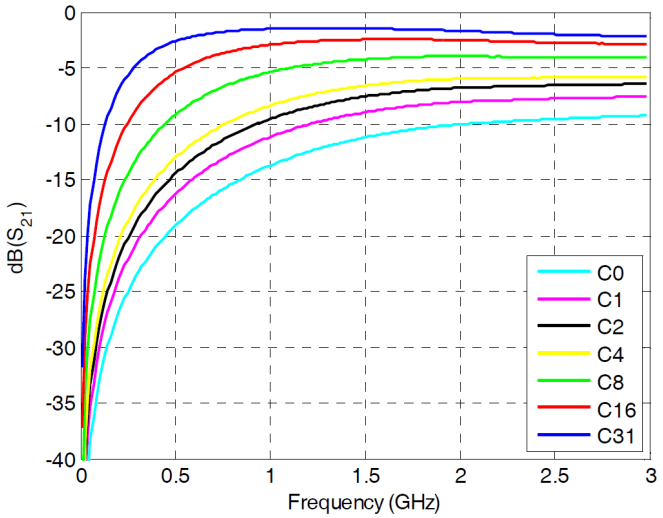


Figure 15. Measured series S_{21} vs. frequency (major states)

When the DTC is part of a reactive network, impedance transformation can cause the internal RF voltages (V_P and V_M in Figure 11) to exceed the peak operating RF voltage. To ensure that neither V_P nor V_M exceed 30 V_{PK}, simulate the complete RF circuit using actual input power and load conditions.

Layout recommendations

For optimal results, place a ground fill directly under the DTC package on the PCB. Layout isolation is essential between all control and RF lines. When using the DTC in a shunt configuration, verify that the RF- pin is solidly grounded to a filled ground plane. To minimize inductance, verify that the ground traces are as short as possible. A continuous ground plane is preferable on the top layer of the PCB. When multiple DTCs are used together, minimize the physical distance between them. To minimize series parasitic inductance, verify that the connection is as wide as possible.

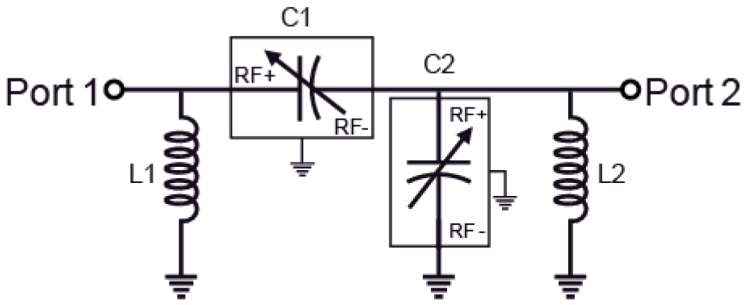


Figure 16. Recommended schematic for multiple DTCs

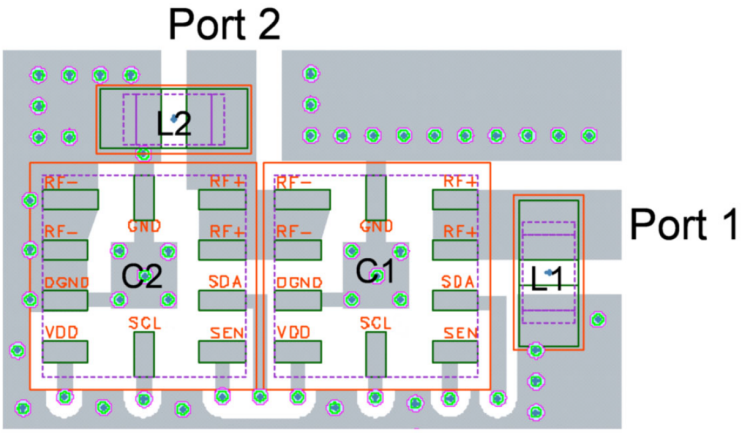


Figure 17. Recommended layout for multiple DTCs

Evaluation board

pSemi designed the 101-0675 evaluation board (EVB) to accurately measure the DTC impedance and loss. Two configurations are available:

- 1-port shunt (J3), and
- 2-port shunt (J4 and J5)

Three calibration standards are provided. The open (J2) and short (J1) standards (104 ps delay) are used to perform port extensions and account for the electrical length and transmission line loss. You can use the thru (J9, J10) standard to estimate the PCB transmission line losses for scalar de-embedding of the 2-port series configuration (J4, J5).

The board consists of a 4-layer stack with two outer layers made of Rogers 4350B (εr = 3.48) and two inner layers of FR4 (εr = 4.80). The total thickness of this board is 62 mils (1.57 mm). The inner layers provide a ground plane for the transmission lines. Each transmission line is designed using a coplanar waveguide (CPWG) with ground plane model using a trace width of 32 mils (0.813 mm), gap of 15 mils (0.381 mm), and a metal thickness of 1.4 mils (0.051 mm).

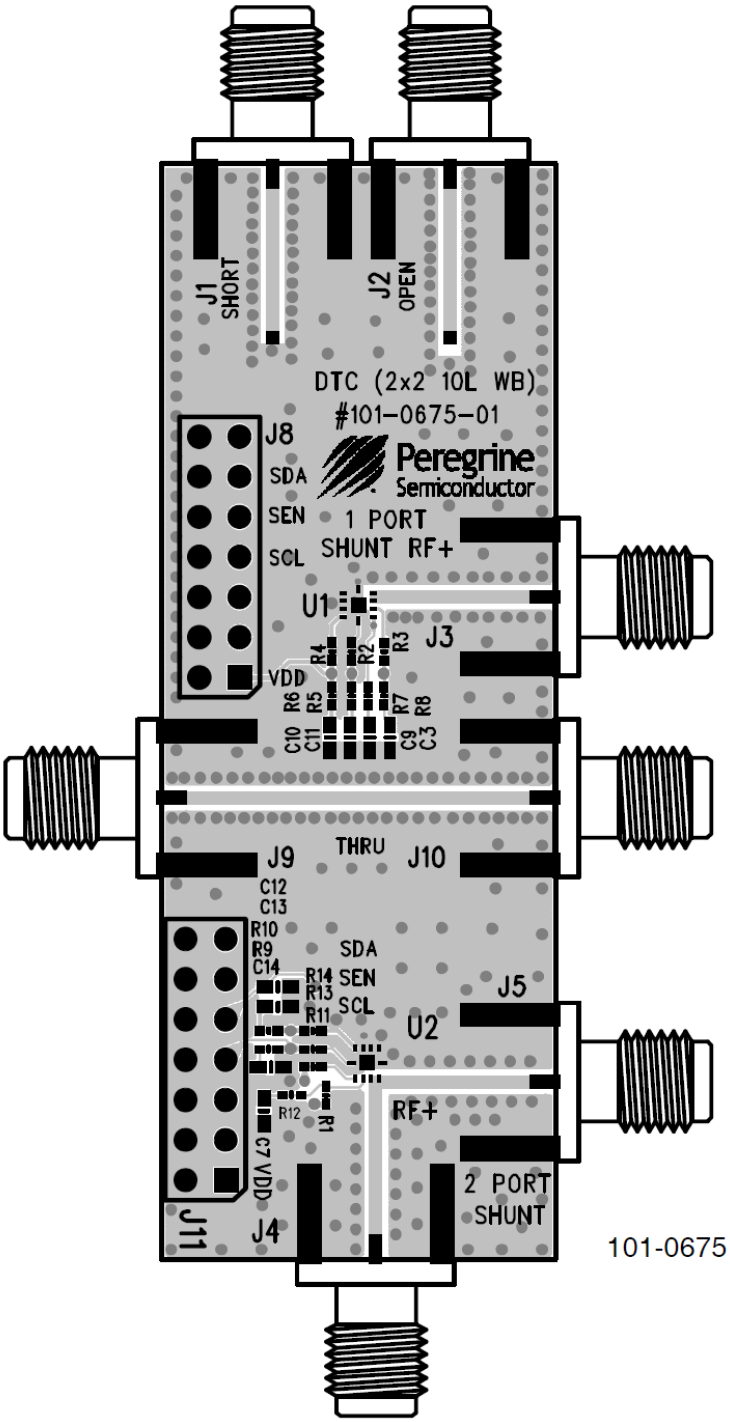


Figure 18. Evaluation board layout

Pin configuration

Figure 19 shows the PE64906 pin configuration for the 10-lead 2 × 2 × 0.55 mm QFN package, and Table 9 lists the description for each pin.

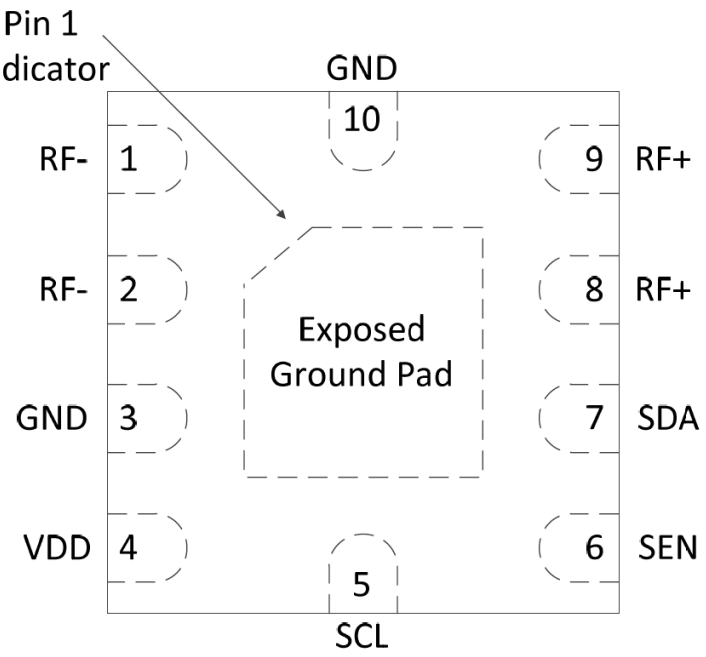


Figure 19. Pin configuration, top view

Table 9. Pin descriptions

Pin no.	Pin name	Description
1, 2[1]	RF-	Negative RF ports
3, 10[2]	GND	Ground
4	V_{DD}	Power supply
5	SCL	Serial interface clock input
6	SEN	Serial interface latch enable input
7	SDA	Serial interface data input
8, 9[3]	RF+	Positive RF ports
Pad[2]	GND	Exposed pad. Ground for proper operation.

Notes:
1. For optimal performance, tie RF- pins 1 and 2 together on the PCB.
2. For optimal performance, tie GND pins 3 and 10 and the exposed ground pad together on the PCB.
3. For optimal performance, tie RF+ pins 8 and 9 together on the PCB.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE64906 moisture sensitivity level rating for the 10-lead 2 × 2 × 0.55 mm QFN package is MSL1.

Package drawing

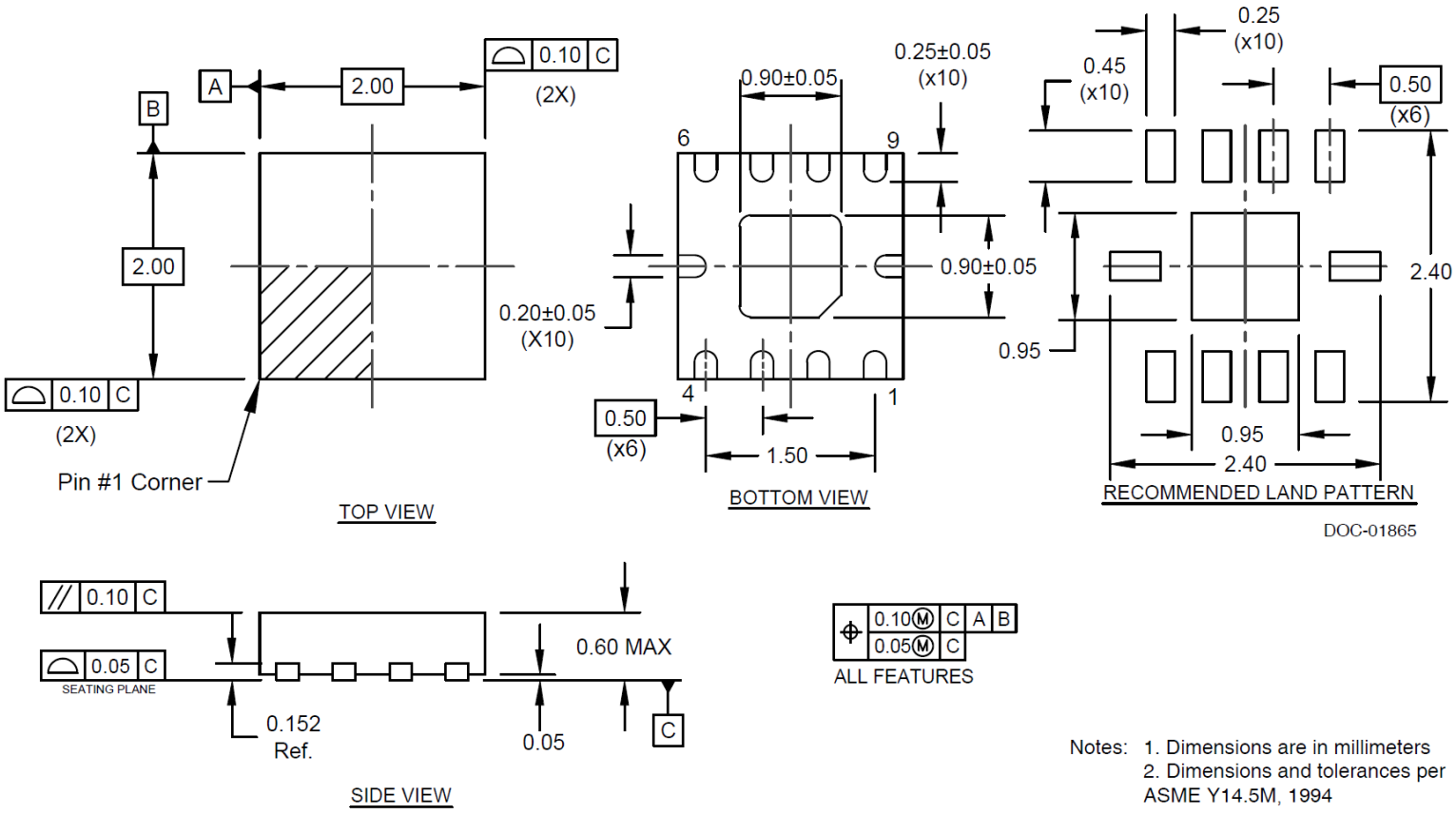
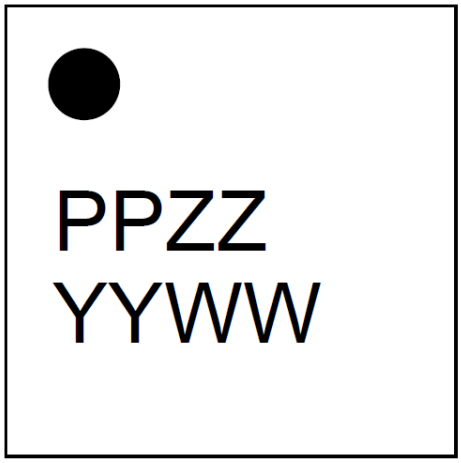


Figure 20. Package mechanical drawing for the 10-lead 2 × 2 × 0.55 mm QFN package

Top-marking specification

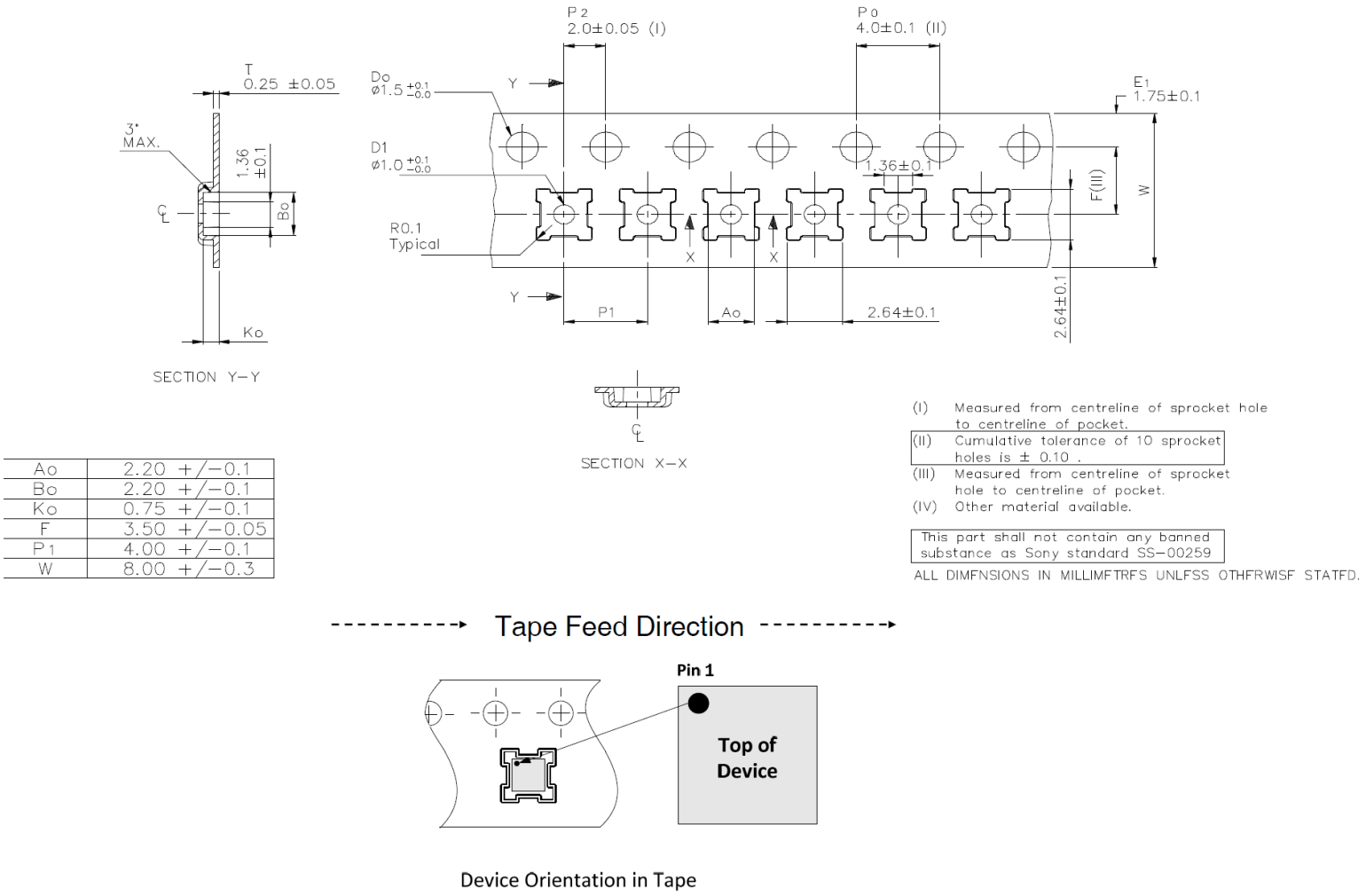


Marking Spec Symbol	Package Marking	Definition
PP	DG*	Part number marking for PE64906
ZZ	00-99	Last two digits of assembly lot code
YY	0-9	Last two digits of assembly year, starting from 2010 (10 for 2010, 11 for 2011, etc.)
WW	01-52	Work week of assembly lot start (01, …, 52)

* Note: (PP), the package marking specific to the PE64906, is shown in the figure instead of the standard pSemi package marking symbol (P)

Figure 21. PE64906 package marking specification

Tape and reel specification



Ao	2.20 +/−0.1
Bo	2.20 +/−0.1
Ko	0.75 +/−0.1
F	3.50 +/−0.05
P1	4.00 +/−0.1
W	8.00 +/−0.3

Figure 22. Tape and reel specification for the 10-lead 2 × 2 × 0.55 mm QFN package

Ordering information

Order code	Description	Packaging	Shipping method
PE64906B-Z	PE64906 UltraCMOS® digitally tunable capacitor	10-lead 2 × 2 × 0.55 mm QFN	3000 units/T&R
EK64906-12	PE64906 evaluation kit	Evaluation kit	1/box

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