SNx4AHC08 四路双输入正与门

1 特性

- 2V 至 5.5V 的工作范围
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求

2 应用

- 服务器
- 网络交换机
- PC 和笔记本电脑
- 电子销售终端

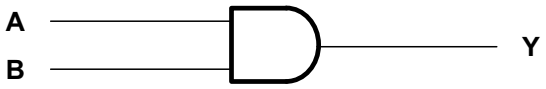
3 说明

SNx4AHC08 器件是四路双输入正与门。此类器件以正逻辑执行布尔函数 $Y = A \cdot B$ 或 $Y = \overline{A + B}$。

器件信息

器件型号	封装(1)	封装尺寸(2)
SN74AHC08	D（SOIC，14）	8.65mm × 3.90mm
	DB（SSOP，14）	6.20mm × 5.30mm
	DGV（TVSOP，14）	3.60mm × 4.40mm
	N（PDIP，14）	19.30mm × 6.35mm
	NS（SO，14）	10.30mm × 5.30mm
	PW（TSSOP，14）	5.00mm × 4.40mm
	RGY（VQFN，14）	3.50mm x 3.50mm
	BQA（WQFN，14）	3mm × 2.5mm
SN54AHC08	FK（LCCC，20）	8.89mm × 8.89mm

(1) 更多相关信息，请参阅第 11 节。
(2) 封装尺寸（长 × 宽）为标称值，不包括引脚。



简化原理图

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4 Pin Configuration and Functions

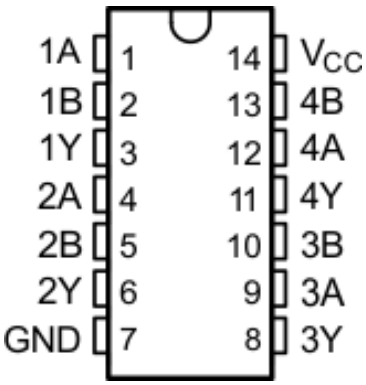


图 4-1. D, DB, DGV, N, NS, PW, or W Package 14-Pin SOIC, SSOP, TVSOP, PDIP, SO, or TSSOP (Top View)

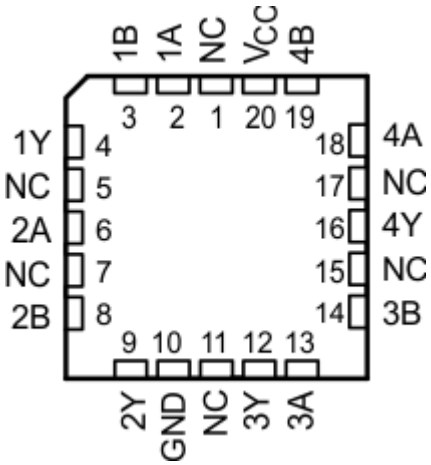


图 4-2. FK Package 20-Pin LCCC (Top View)

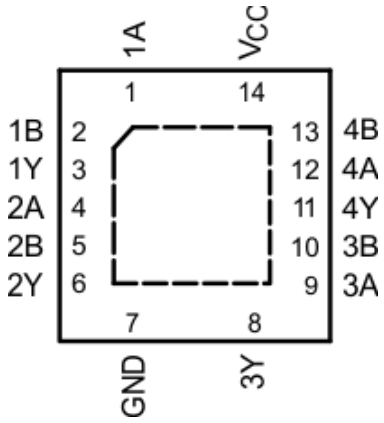


图 4-3. RGY or BQA Package 14-Pin VQFN or WQFN (Top View)

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表 4-1. Pin Functions

PIN				I/O	DESCRIPTION
NAME	SOIC, SSOP, TVSOP, PDIP, SO, TSSOP	VQFN, WQFN	LCCC		
1A	1	1	2	I	1A Input
1B	2	2	3	I	1B Input
1Y	3	3	4	O	1Y Output
2A	4	4	6	I	2A Input
2B	5	5	8	I	2B Input
2Y	6	6	9	O	2Y Output
3Y	8	8	12	O	3Y Output
3A	9	9	13	I	3A Input
3B	10	10	14	I	3B Input
4Y	11	11	16	O	4Y Output
4A	12	12	18	I	4A Input
4B	13	13	19	I	4B Input
GND	7	7	10	—	Ground Pin
NC	—	—	1, 5, 7, 11, 15, 17	—	No Connection
V_{CC}	14	14	20	—	Power Pin

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		– 0.5	7	V
V_I	Input voltage(2)		– 0.5	7	V
V_O	Output voltage, V_O (2)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		-20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC}= 2 V	1.5		V
		V_{CC}= 3V	2.1		
		V_{CC}= 5.5 V	3.85		
V_{IL}	Low-level Input voltage	V_{CC}= 2 V		0.5	V
		V_{CC}= 3 V		0.9	
		V_{CC}= 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC}= 2 V		– 50	mA
		V_{CC}= 3.3 V ± 0.3 V		– 4	
		V_{CC}= 5 V ± 0.5 V		– 8	
I_{OL}	Low-level output current	V_{CC}= 2 V		50	mA
		V_{CC}= 3.3 V ± 0.3 V		4	
		V_{CC}= 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input Transition rise or fall rate	V_{CC}= 3.3 V ± 0.3 V		100	ns/V
		V_{CC}= 5 V ± 0.5 V		20	

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over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
T_A	Operating free-air temperature	SN54AHC08	–55	125	°C
		SN74AHC08	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.4 Thermal Information

THERMAL METRIC(1)		SN74AHC08								UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	96	127	80	76	147.7	87.1	88.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics, T_A = 25°C

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 µA		2 V	1.9	2		V
			3 V	2.9	3		
			4.5 V	4.4	4.5		
	I_{OH} = –4 mA		3 V	2.58			
	I_{OH} = –8 mA		4.5 V	3.94			
V_{OL}	I_{OL} = 50 µA		2 V			0.1	V
			3 V			0.1	
			4.5 V			0.1	
	I_{OH} = 4 mA		3 V			0.36	
	I_{OH} = 8 mA		4.5 V			0.36	
I_I	V_I = 5.5 V or GND		0 V to 5.5 V			±0.1	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			2	µA
C_i	V_I = V_{CC} or GND		5 V		4	10	pF

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5.6 Electrical Characteristics, T_A = –55°C to 125°C

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54AHC08		UNIT
			MIN	MAX	
V_{OH}	I_{OH} = –50 µA	2 V	1.9		V
		3 V	2.9		
		4.5 V	4.4		
	I_{OH} = –4 mA	3 V	2.48		
	I_{OH} = –8 mA	4.5 V	3.8		
V_{OL}	I_{OL} = 50 µA	2 V		0.1	V
		3 V		0.1	
		4.5 V		0.1	
	I_{OH} = 4 mA	3 V		0.5	
	I_{OH} = 8 mA	4.5 V		0.5	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V		±1(1)	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V		20	µA
C_i	V_I = V_{CC} or GND	5 V			pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at VCC = 0 V.

5.7 Electrical Characteristics, T_A = –40°C to 125°C

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A	SN74AHC08		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –50 µA	2 V		1.9		V
		3 V		2.9		
		4.5 V		4.4		
	I_{OH} = –4 mA	3 V		2.48		
	I_{OH} = –8 mA	4.5 V		3.8		
V_{OL}	I_{OL} = 50 µA	2 V			0.1	V
		3 V			0.1	
		4.5 V			0.1	
	I_{OH} = 4 mA	3 V	T_A = –40°C to 85°C		0.44	
			T_A = –40°C to125°C Recommended		0.5	
	I_{OH} = 8 mA	4.5 V	T_A = –40°C to 85°C		0.44	
			T_A = –40°C to125°C Recommended		0.5	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20	µA
C_i	V_I = V_{CC} or GND	5 V	T_A = –40°C to 85°C		10	pF

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5.8 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A or B	Y	C_L = 15 pF	T_A = 25°C		6.2(1)	8.8(1)	ns
				T_A = –55°C to 125°C, SN54AHC08		1(1)	10.5(1)	
				T_A = –40°C to 85°C, SN74AHC08		1	10.5	
				T_A = –40°C to 125°C Recommended, SN74AHC08		1	10.5	
t_{PLH}, t_{PHL}	A or B	Y	C_L = 50 pF	T_A = 25°C		8.7	12.3	ns
				T_A = –55°C to 125°C, SN54AHC08		1	14	
				T_A = –40°C to 85°C, SN74AHC08		1	14	
				T_A = –40°C to 125°C Recommended, SN74AHC08		1	14	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.9 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A or B	Y	C_L = 15 pF	T_A = 25°C		4.3(1)	5.9(1)	ns
				T_A = –55°C to 125°C, SN54AHC08		1(1)	7(1)	
				T_A = –40°C to 85°C, SN74AHC08		1	7	
				T_A = –40°C to 125°C Recommended, SN74AHC08		1	7	
t_{PLH}, t_{PHL}	A or B	Y	C_L = 50 pF	T_A = 25°C		5.8	7.9	ns
				T_A = –55°C to 125°C, SN54AHC08		1	9	
				T_A = –40°C to 85°C, SN74AHC08		1	9	
				T_A = –40°C to 125°C Recommended, SN74AHC08		1	9	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

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5.10 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C(1)

		SN74AHC08		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

(1) Characteristics are for surface-mount packages only.

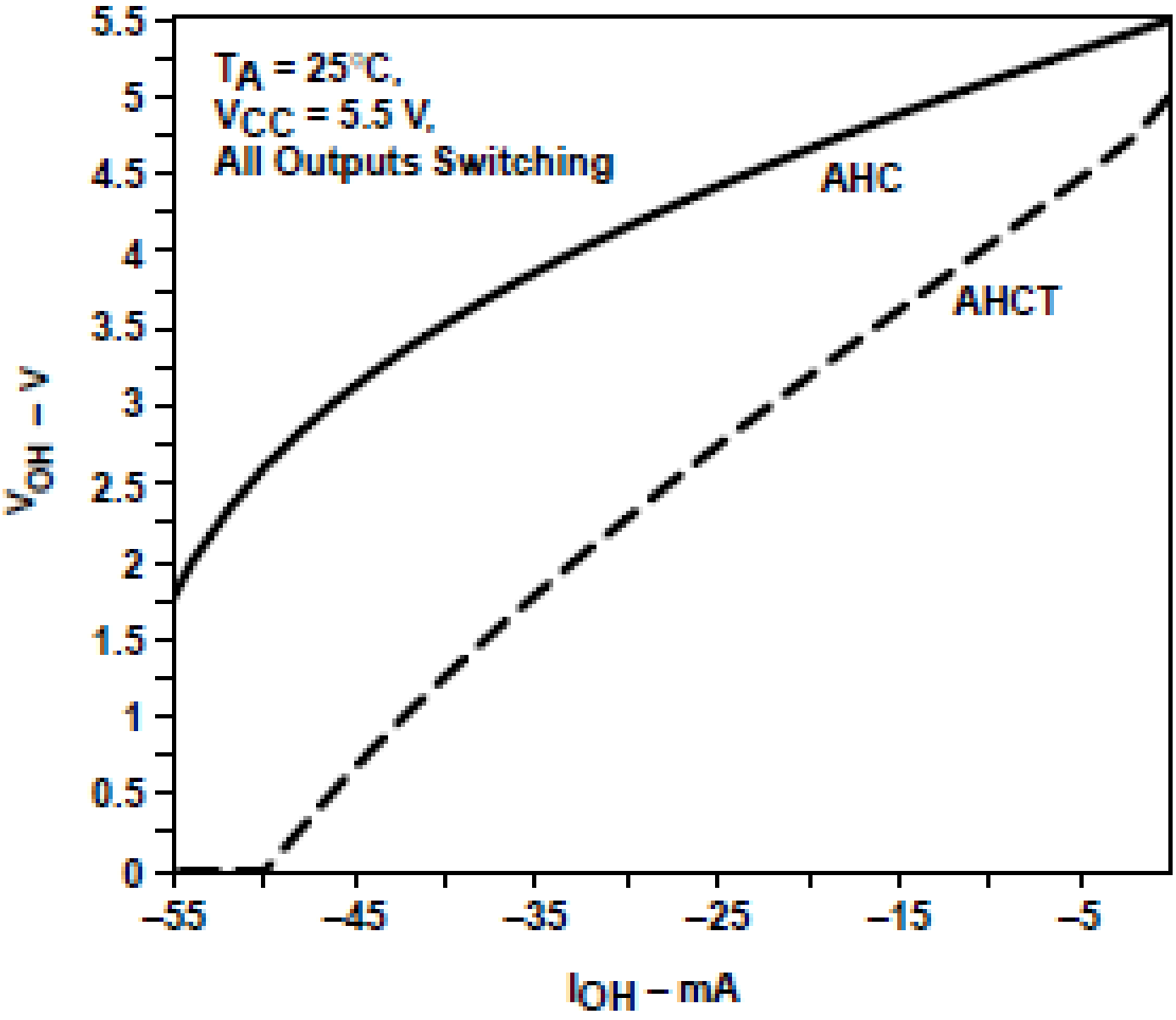
5.11 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	18	pF

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5.12 Typical Characteristics

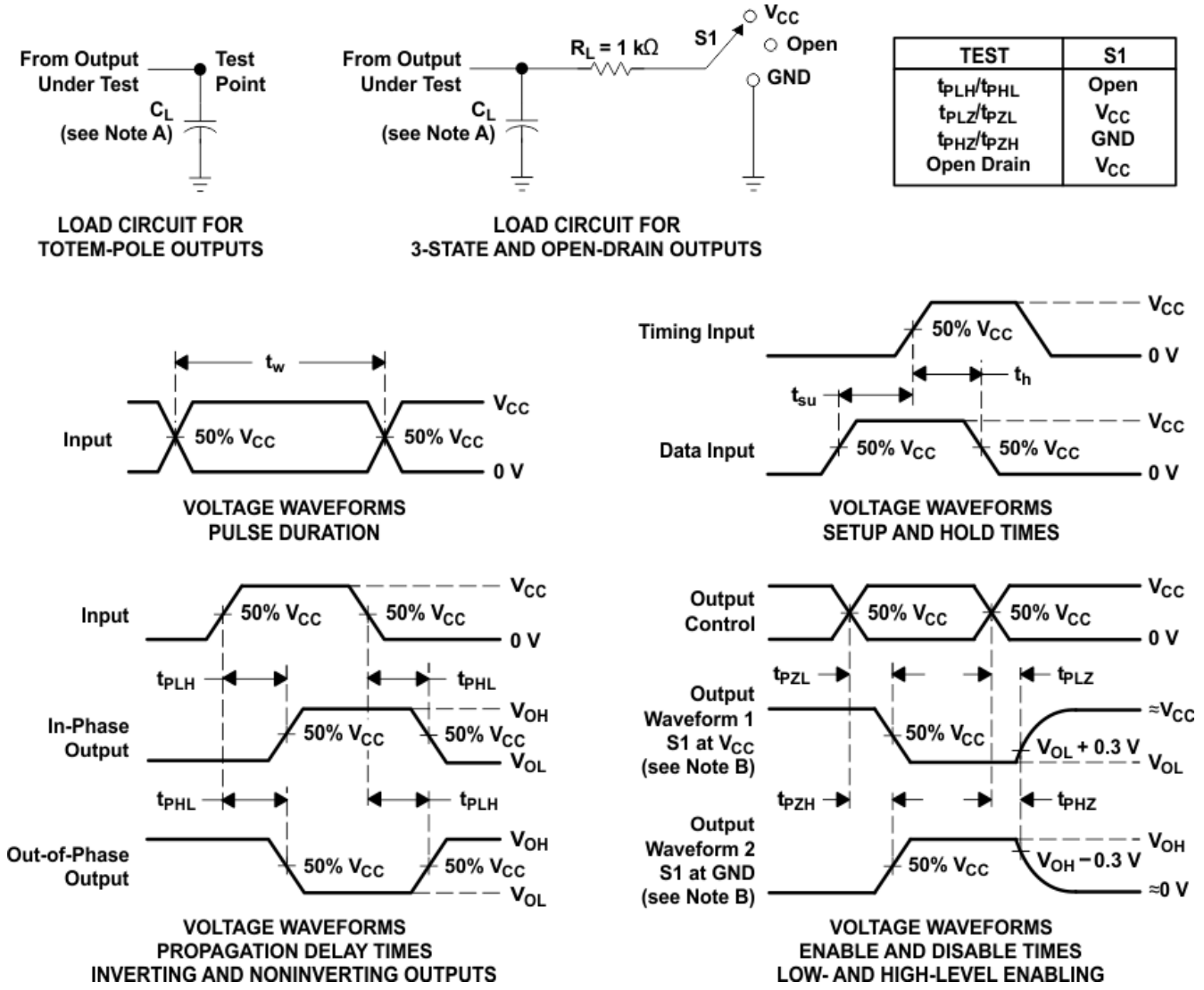


V_{CC} = 5.5 V

图 5-1. AHC Family V_{OL} vs I_{OL}

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6 Parameter Measurement Information



A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O = 50 Ω, t_r ⩽ 3 ns, t_f ⩽ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

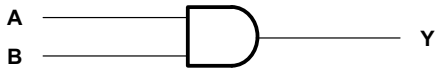
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7 Detailed Description

7.1 Overview

The SNx4AHC08 devices are quadruple 2-input positive-AND gates with low drive that will produce slow rise and fall times. This slow transition reduces ringing on the output signal. The inputs are high impedance when V_{CC} = 0 V.

7.2 Functional Block Diagram



7.3 Feature Description

Slow rise and fall time on outputs allow for low-noise outputs.

7.4 Device Functional Modes

表 7-1 is the function table for the SNx4AHC08.

表 7-1. Function Table (Each Gate)

INPUTS		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L

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8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

A common application for AND gates is the use in power sequencing. Power sequencing is often employed in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning. Using the SN74AHC08 to verify that the processor has turned on can protect it from harmful signals.

8.2 Typical Application

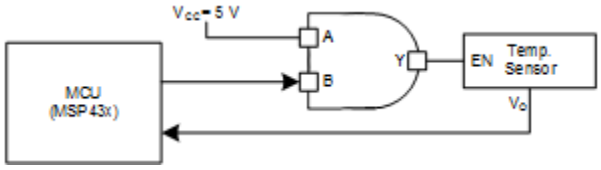


图 8-1. Typical Application Diagram

8.2.1 Design Requirements

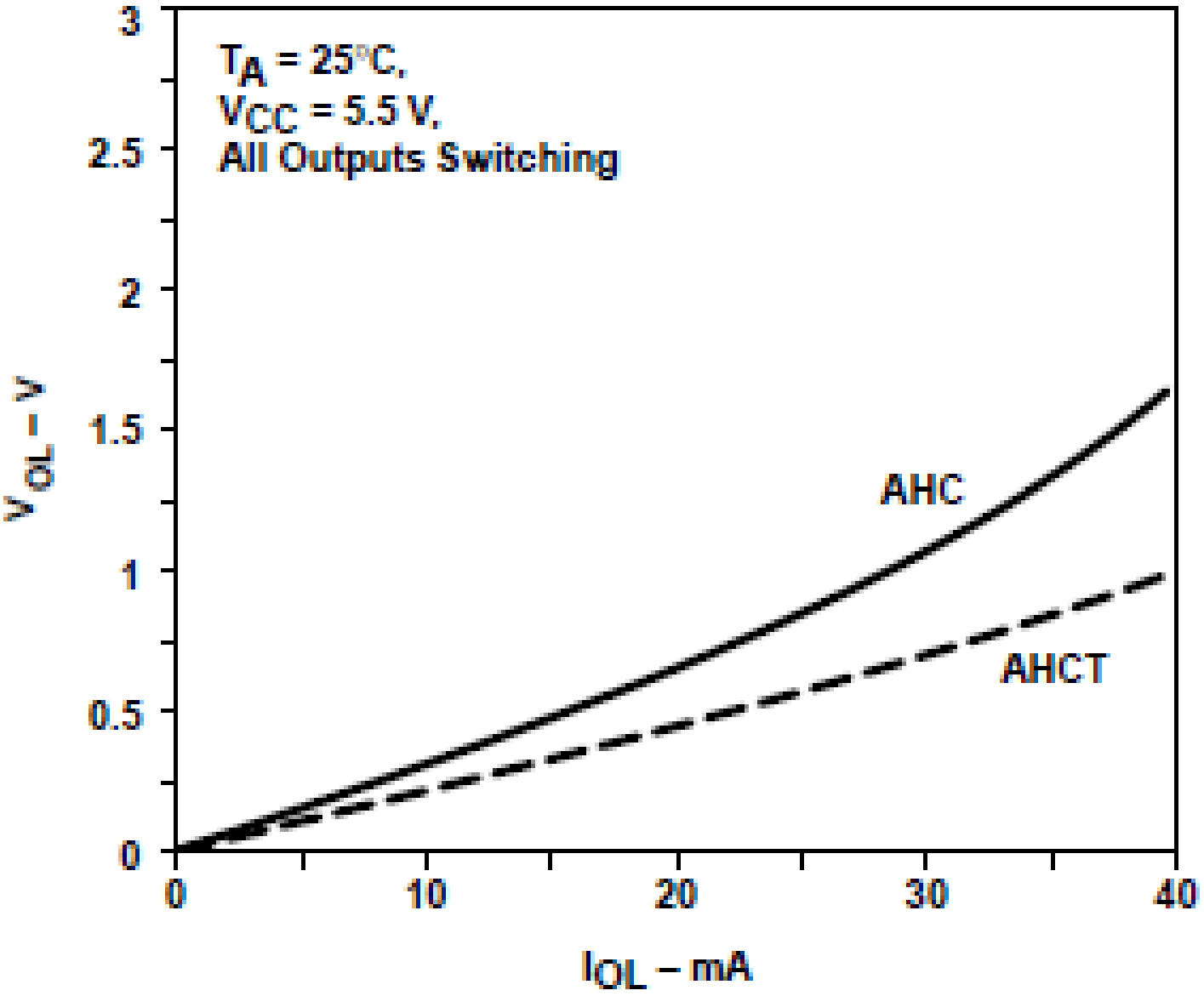
This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended input conditions
   - Rise time and fall time specs: See ($\Delta t/\Delta v$) in the *节 5.3* table.
   - Specified High and low levels: See (V_{IH} and V_{IL}) in the *节 5.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommend output conditions
   - Load currents should not exceed 25 mA per output and 50 mA total for the part
   - Outputs should not be pulled above V_{CC}

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8.2.3 Application Curve



V_{CC} = 5.5 V

图 8-2. AHC Family V_{OH} vs I_{OH}

Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *节 5.1* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and

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1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.3 Layout

8.3.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in 图 8-3 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

8.3.1.1 Layout Example

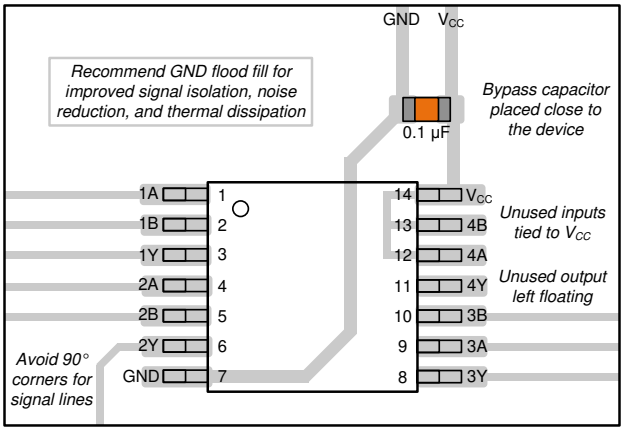


图 8-3. Layout Example for the SNx4AHC08

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC08	Click here	Click here	Click here	Click here	Click here
SN74AHC08	Click here	Click here	Click here	Click here	Click here

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

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9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision K (June 2023) to Revision L (February 2024)	Page
• Updated R θ JA value: RGY = 47 to 87.1, all values in °C/W	6

Changes from Revision J (December 2015) to Revision K (June 2023)	Page
• 向*器件信息* 表中添加了 BQA 封装	1
• Updated R θ JA values: D = 86 to 124.5, PW = 113 to 147.7	6
• Added thermal value for R θ JA: BQA = 88.3, all values in °C/W	6

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9682001Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682001Q2A SNJ54AHC08FK
SN74AHC08BQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHC08
SN74AHC08BQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHC08
SN74AHC08D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	AHC08
SN74AHC08DBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08
SN74AHC08DBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08
SN74AHC08DGVR	NRND	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08
SN74AHC08DGVR.A	NRND	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08
SN74AHC08DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08
SN74AHC08DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08
SN74AHC08DR1G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08
SN74AHC08DR1G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08
SN74AHC08N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC08N
SN74AHC08N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC08N
SN74AHC08NSR	NRND	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08
SN74AHC08NSR.A	NRND	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08
SN74AHC08PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HA08
SN74AHC08PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08
SN74AHC08PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08
SN74AHC08PWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08
SN74AHC08RGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08
SN74AHC08RGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08
SN74AHC08RGYRG4	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08
SN74AHC08RGYRG4.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08
SNJ54AHC08FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682001Q2A SNJ54AHC08FK

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC08, SN74AHC08 :

- Catalog : SN74AHC08
- Enhanced Product : SN74AHC08-EP, SN74AHC08-EP
- Military : SN54AHC08

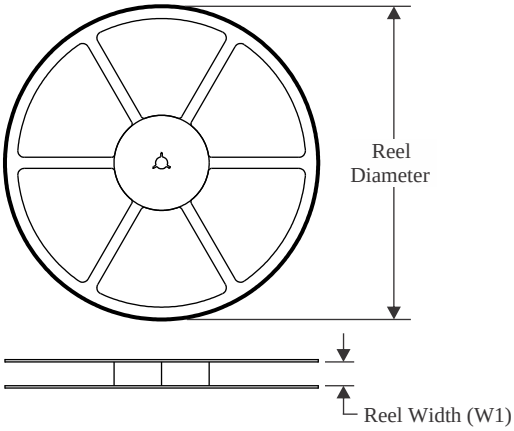
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

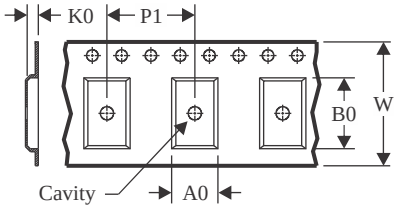
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

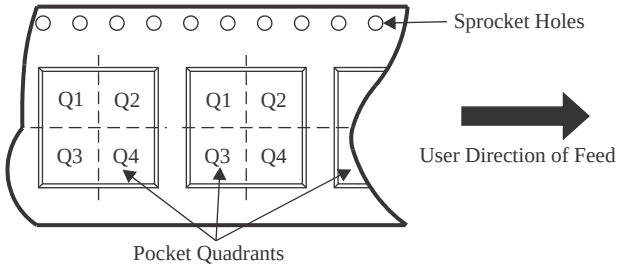


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

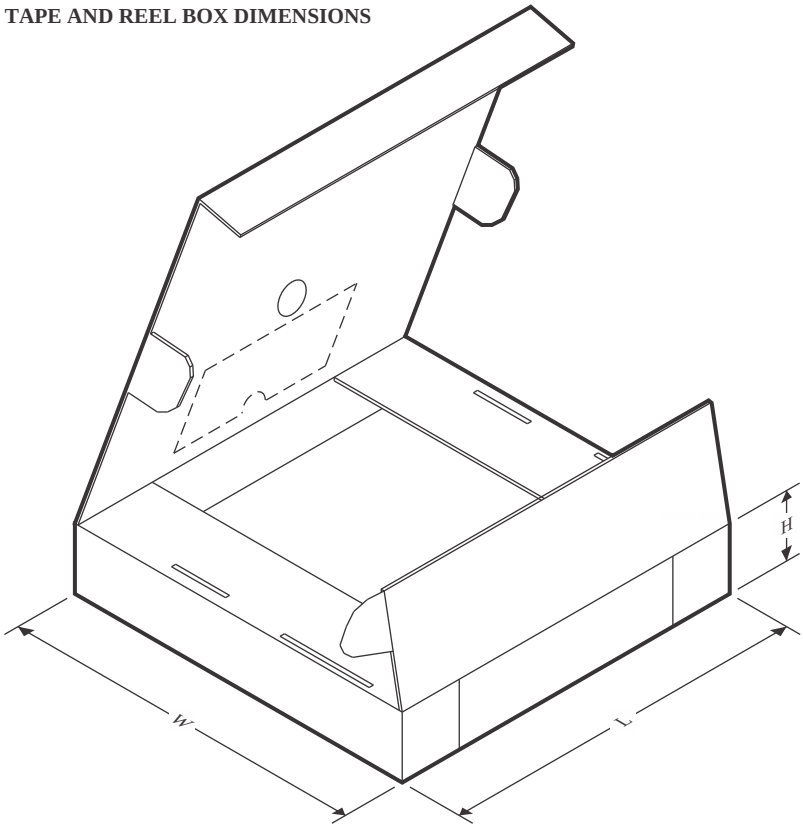
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC08BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC08DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC08DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC08DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC08DR1G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC08NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
SN74AHC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
SN74AHC08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC08RGYRG4	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

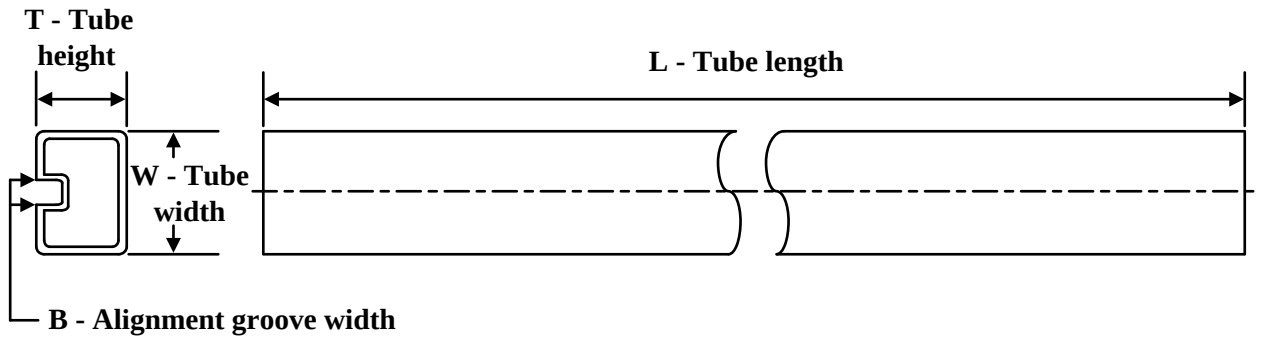
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC08BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC08DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AHC08DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74AHC08DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AHC08DR1G4	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC08NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHC08PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74AHC08PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC08PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC08PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC08PWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74AHC08PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC08RGYR	VQFN	RGY	14	3000	360.0	360.0	36.0
SN74AHC08RGYRG4	VQFN	RGY	14	3000	360.0	360.0	36.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9682001Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74AHC08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC08N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC08N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC08FK	FK	LCCC	20	55	506.98	12.06	2030	NA

GENERIC PACKAGE VIEW

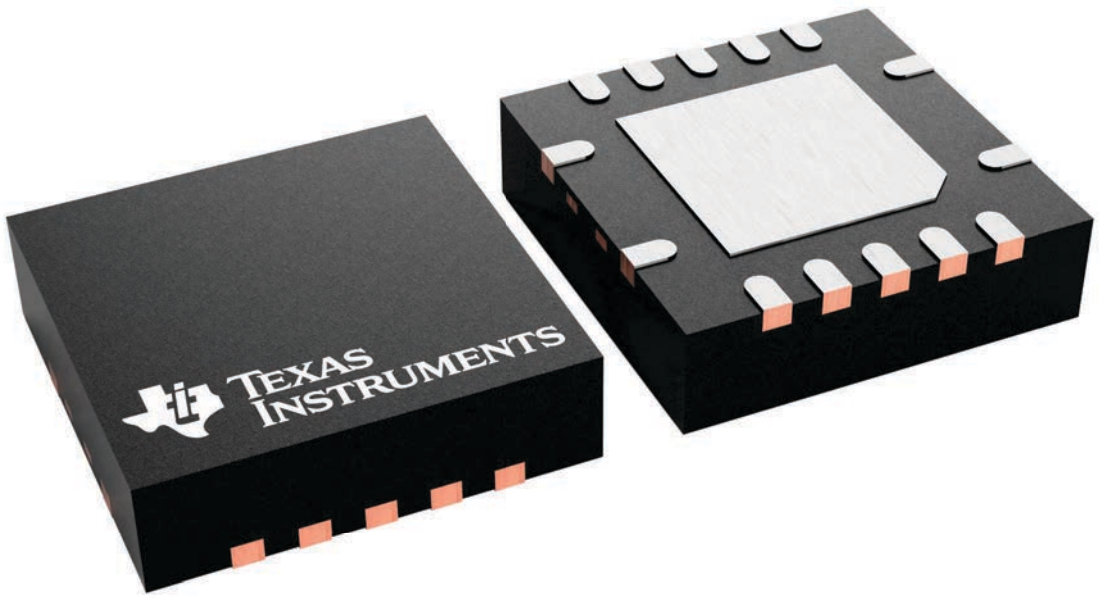
RGY 14

VQFN - 1 mm max height

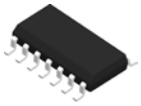
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

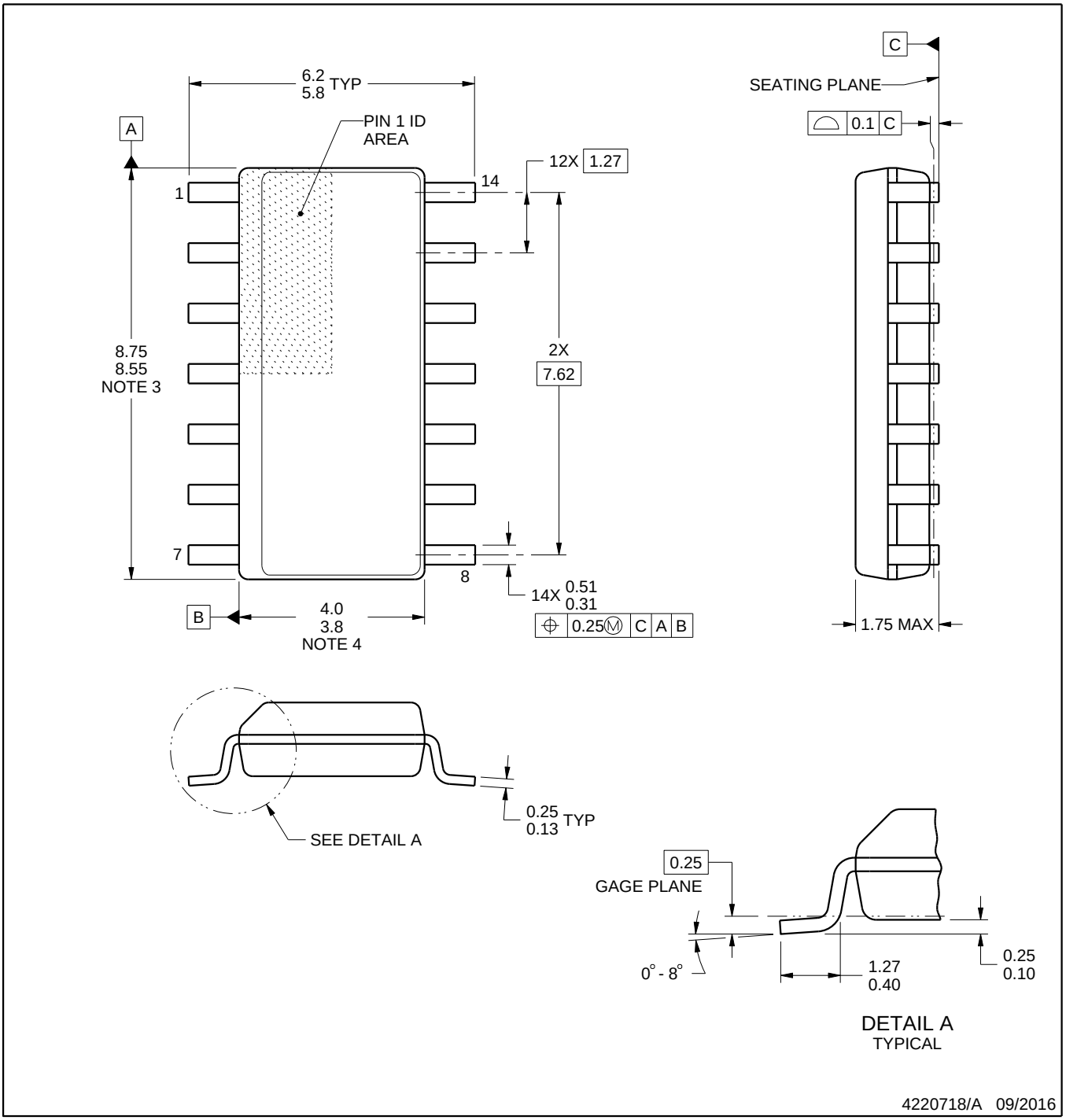


PACKAGE OUTLINE

D0014A

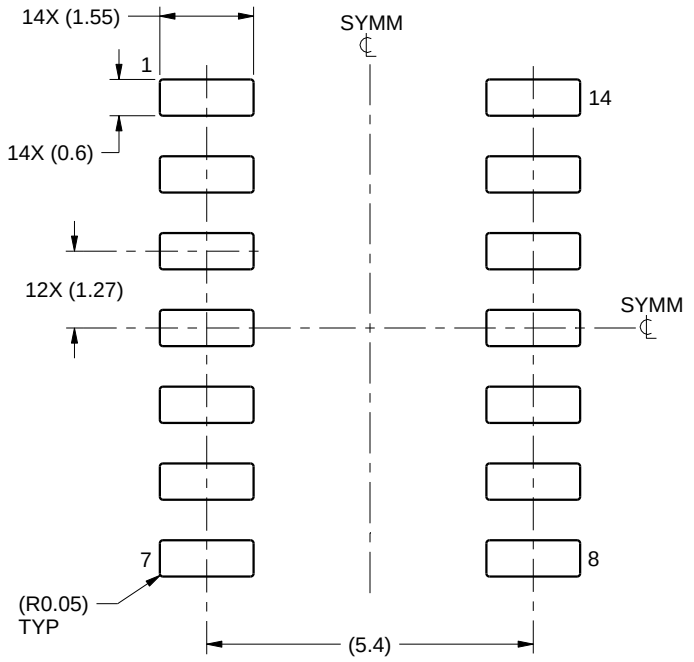
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

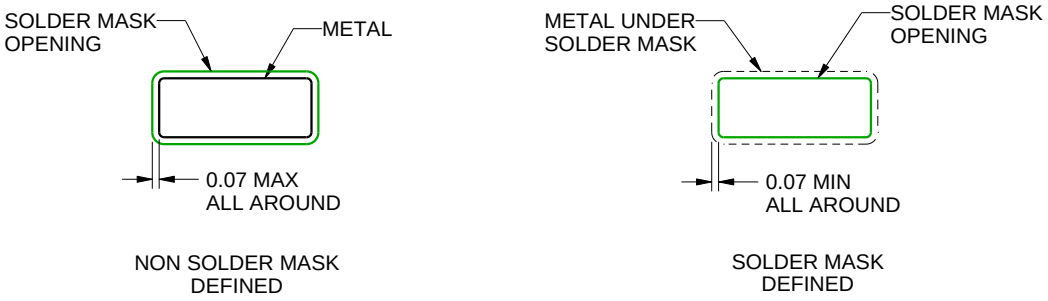


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

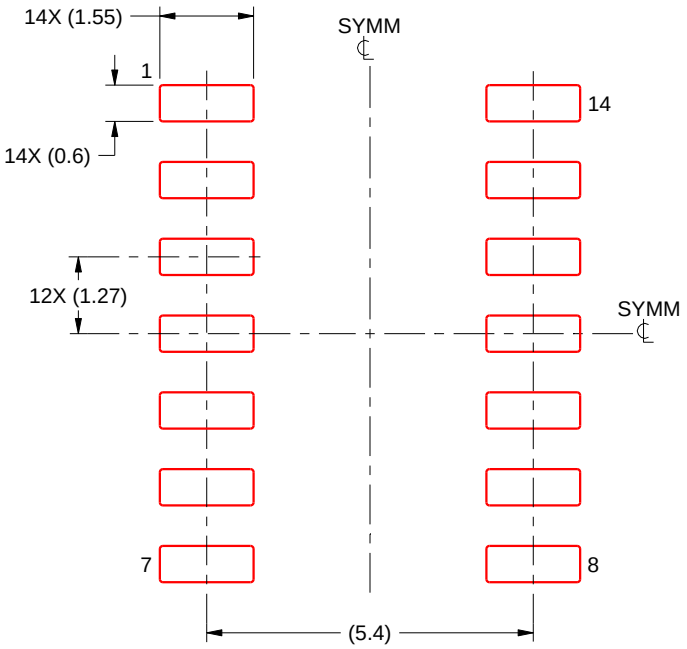
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

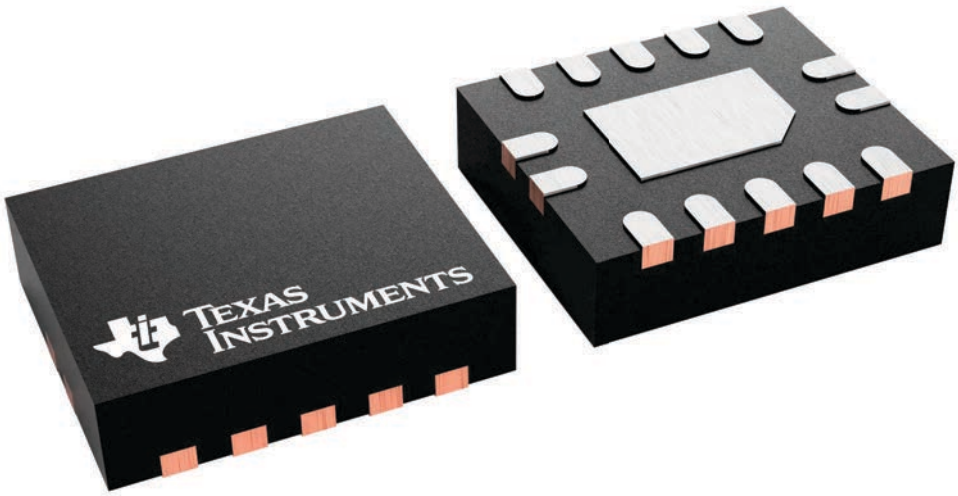
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

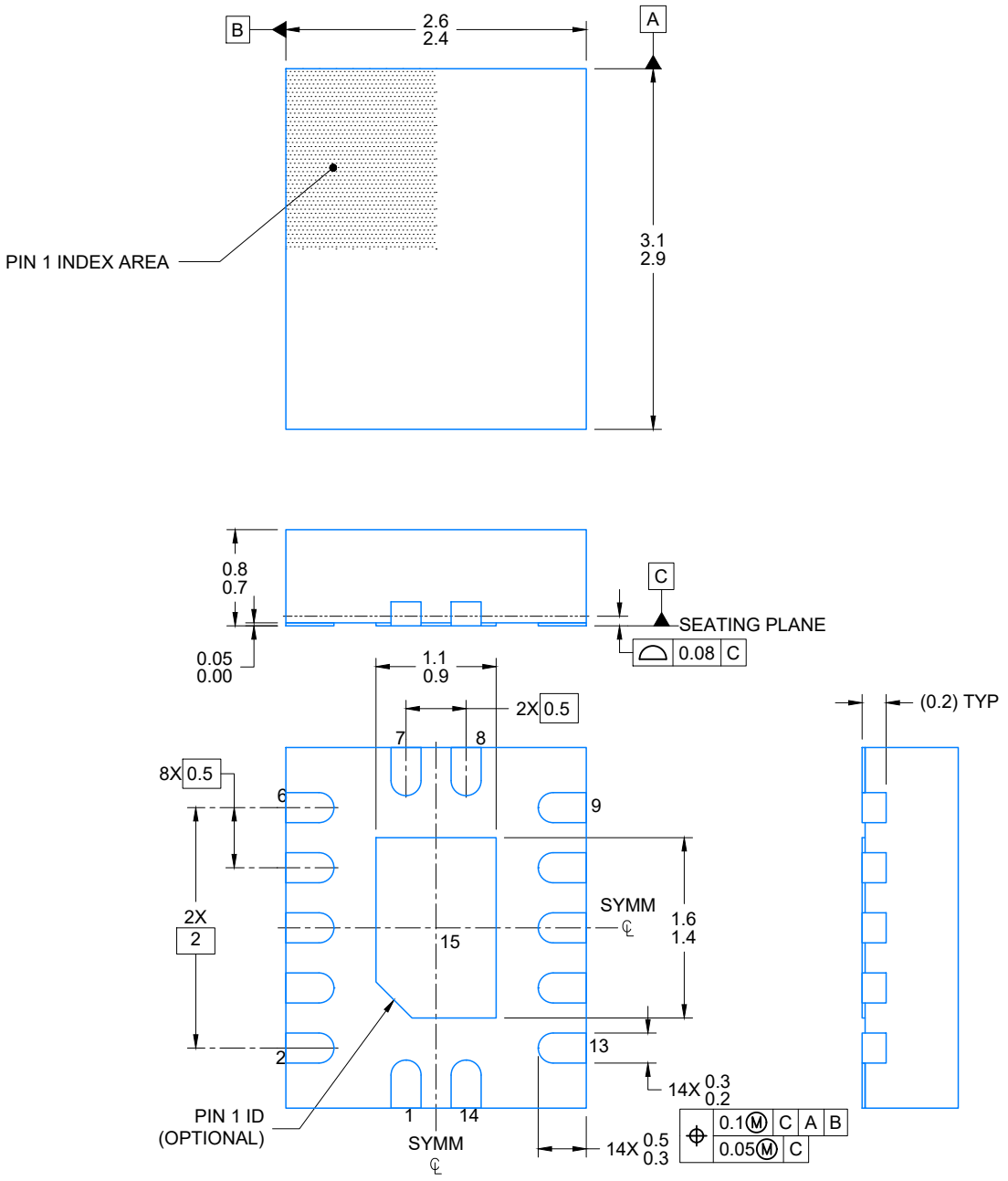


PACKAGE OUTLINE

BQA0014A

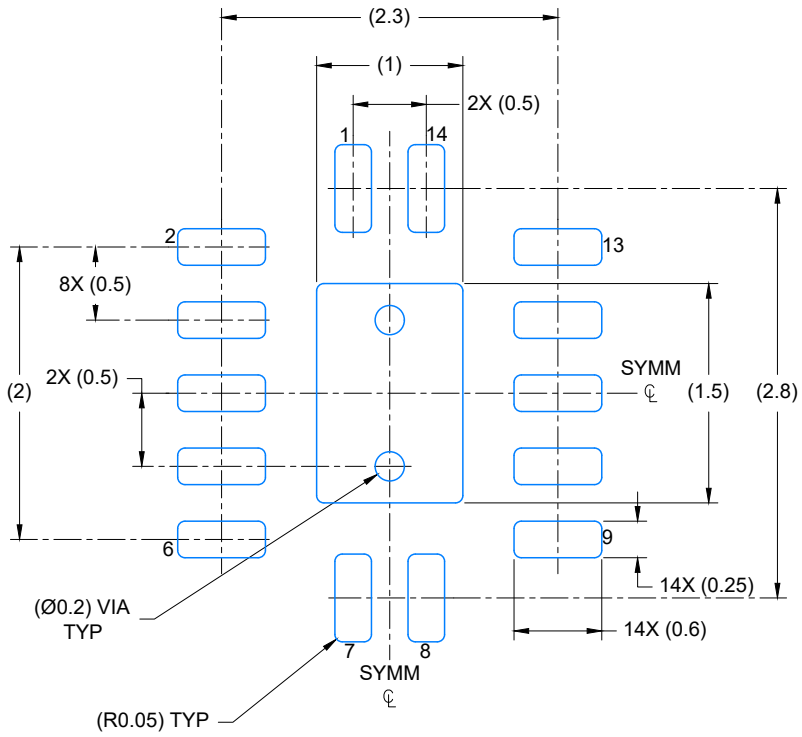
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

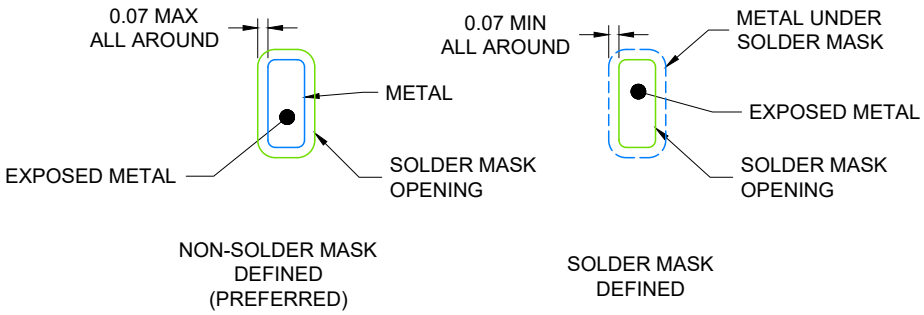


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



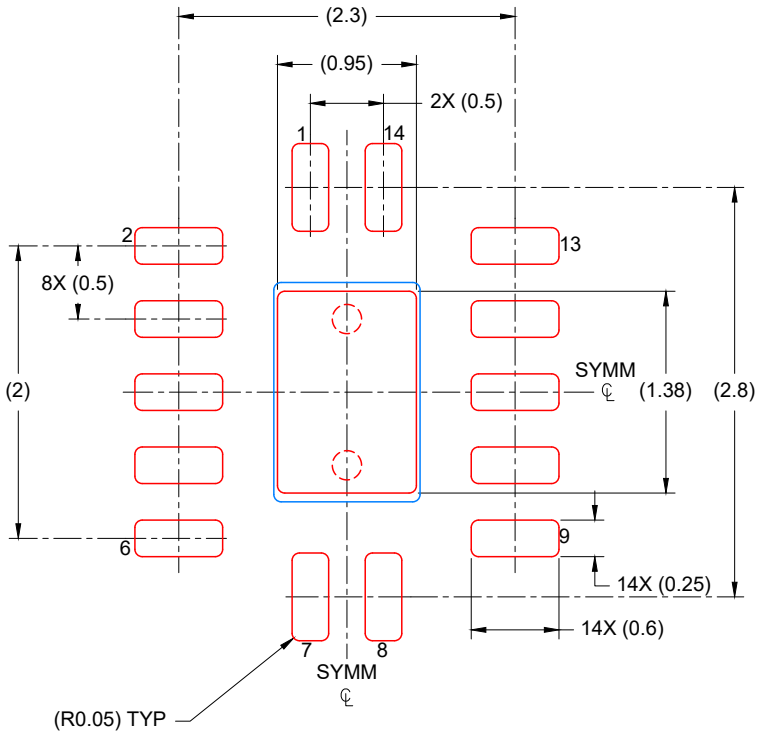
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

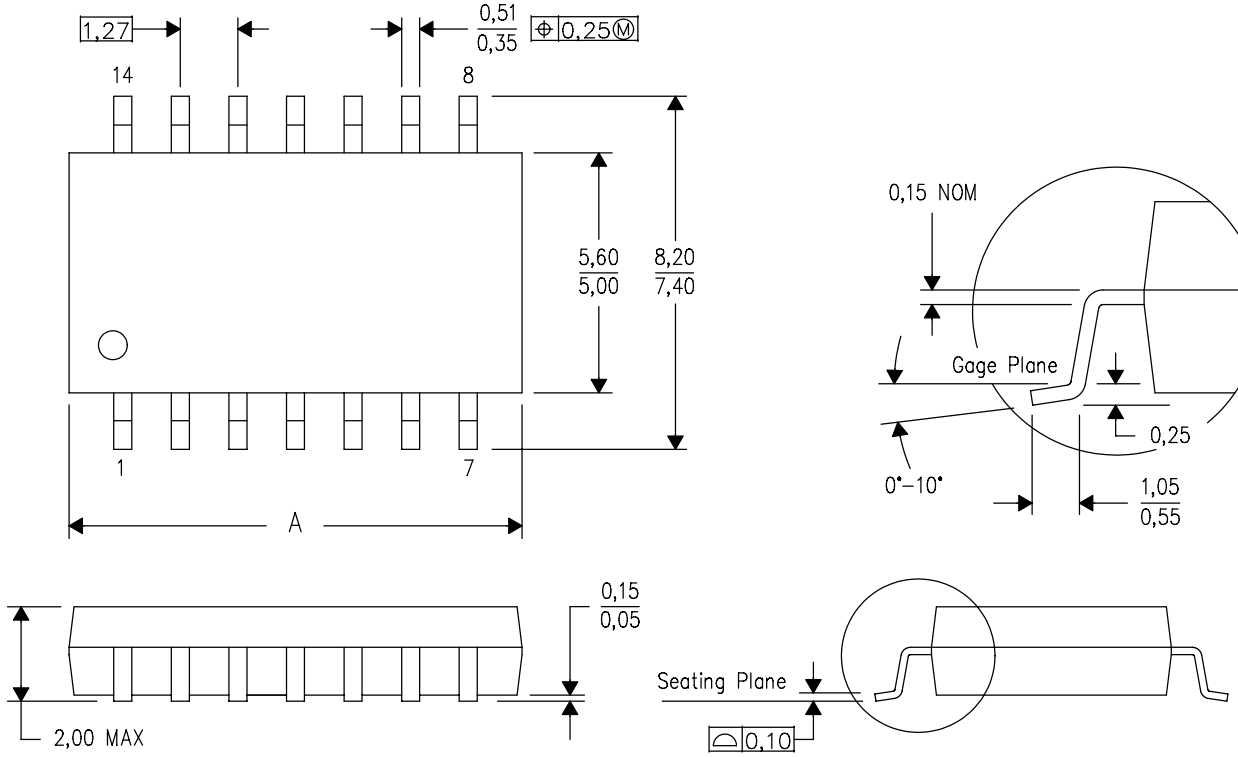
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



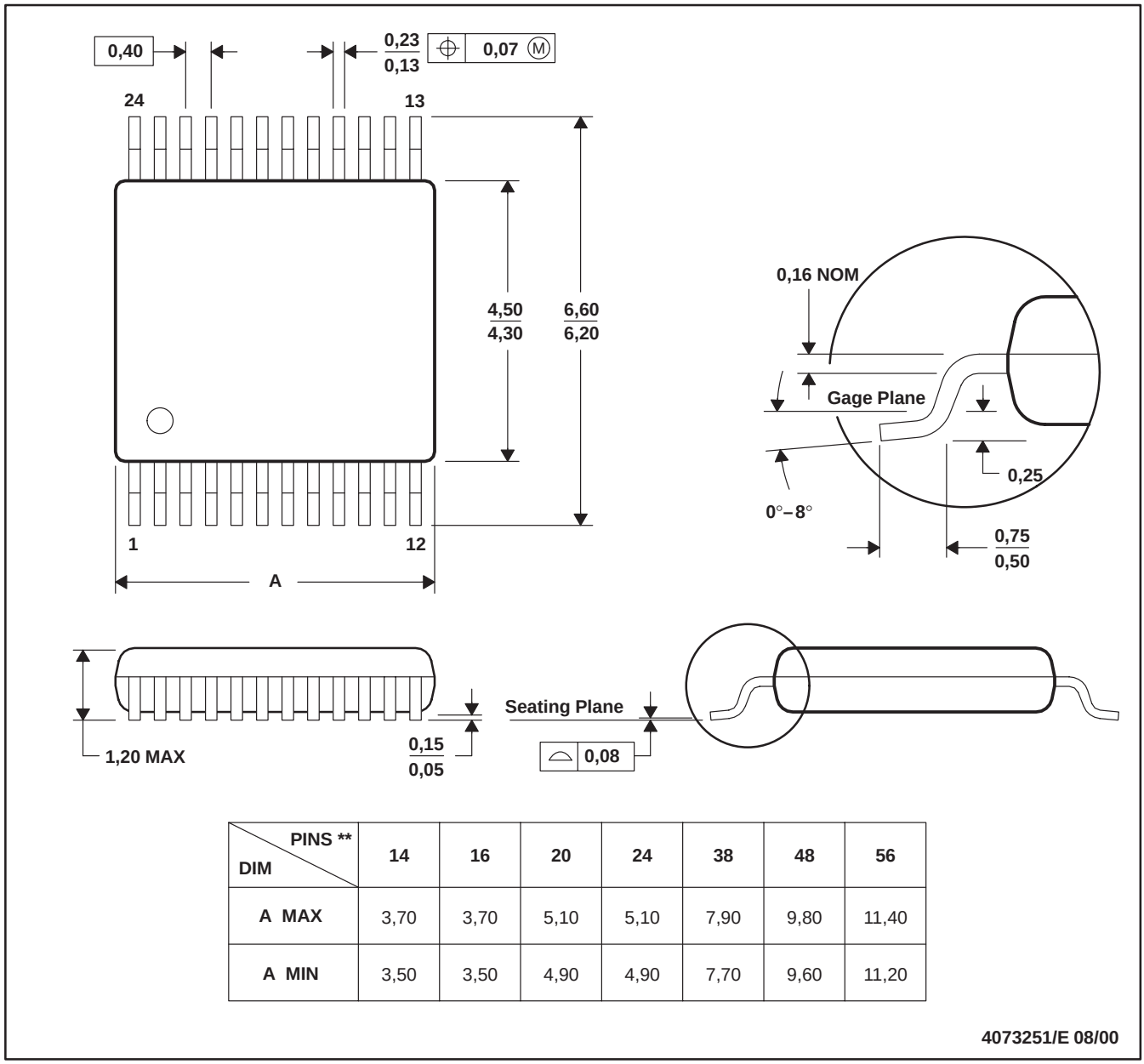
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

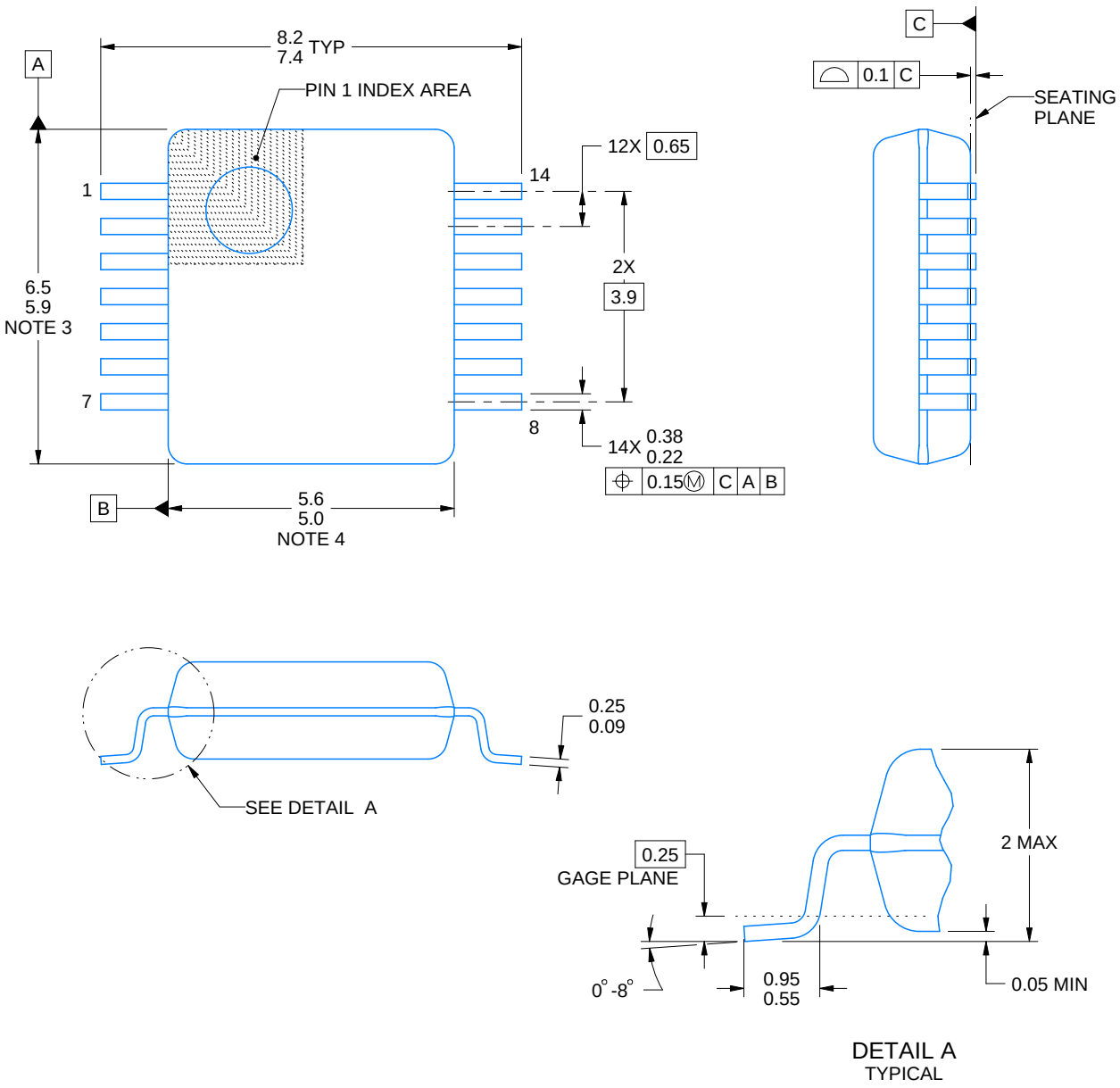
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

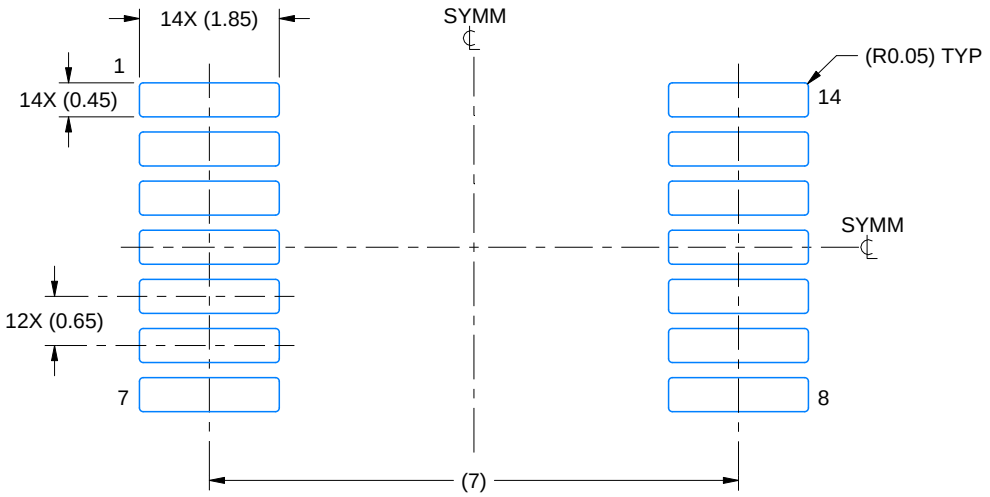
SMALL OUTLINE PACKAGE



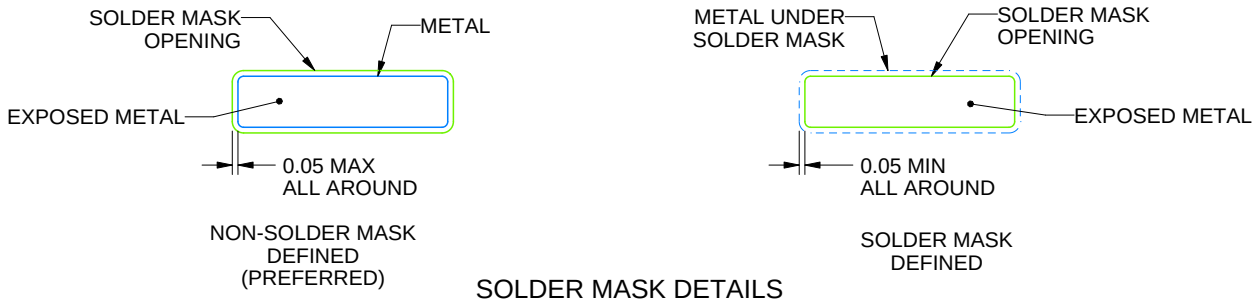
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

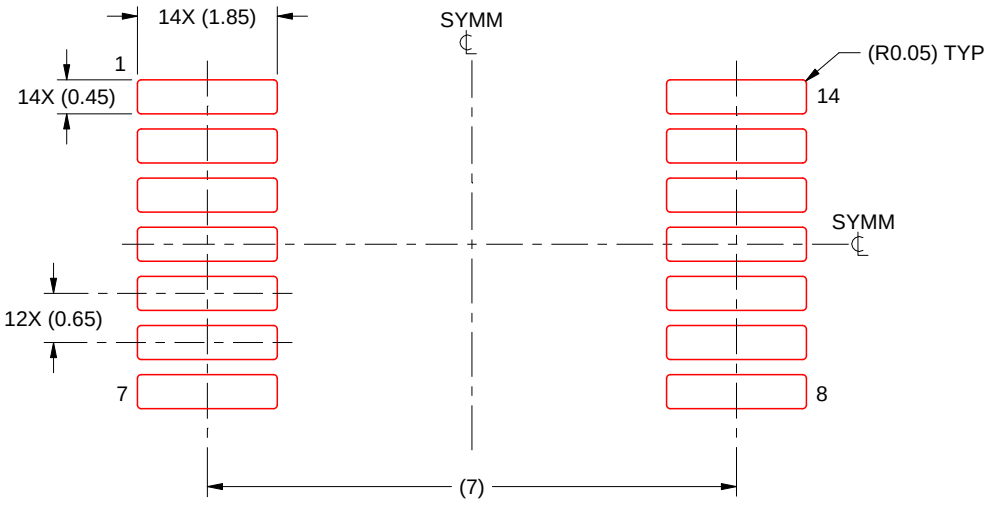


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

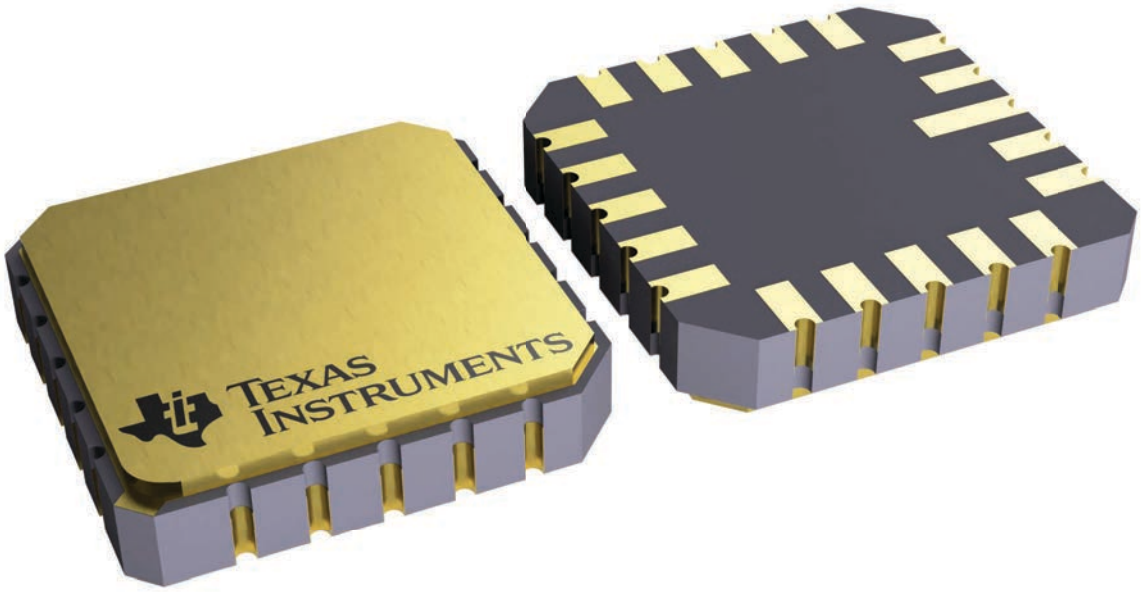
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

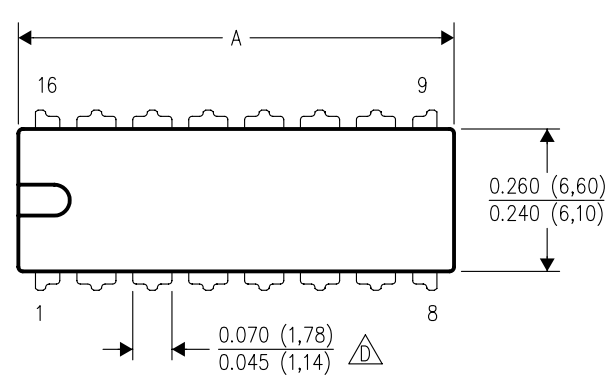


4229370VA\

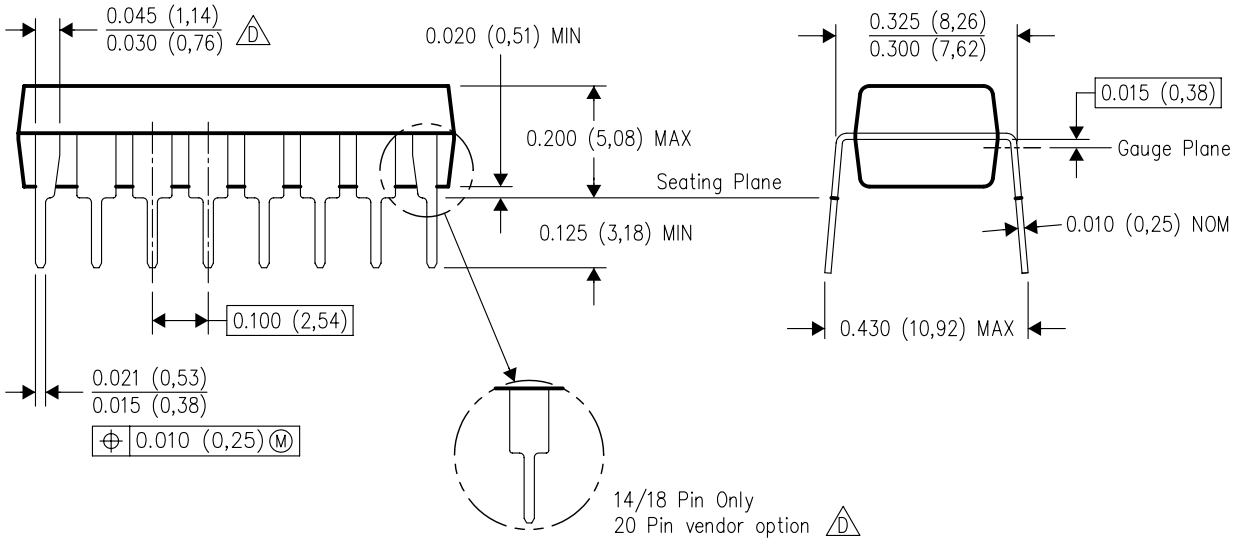
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

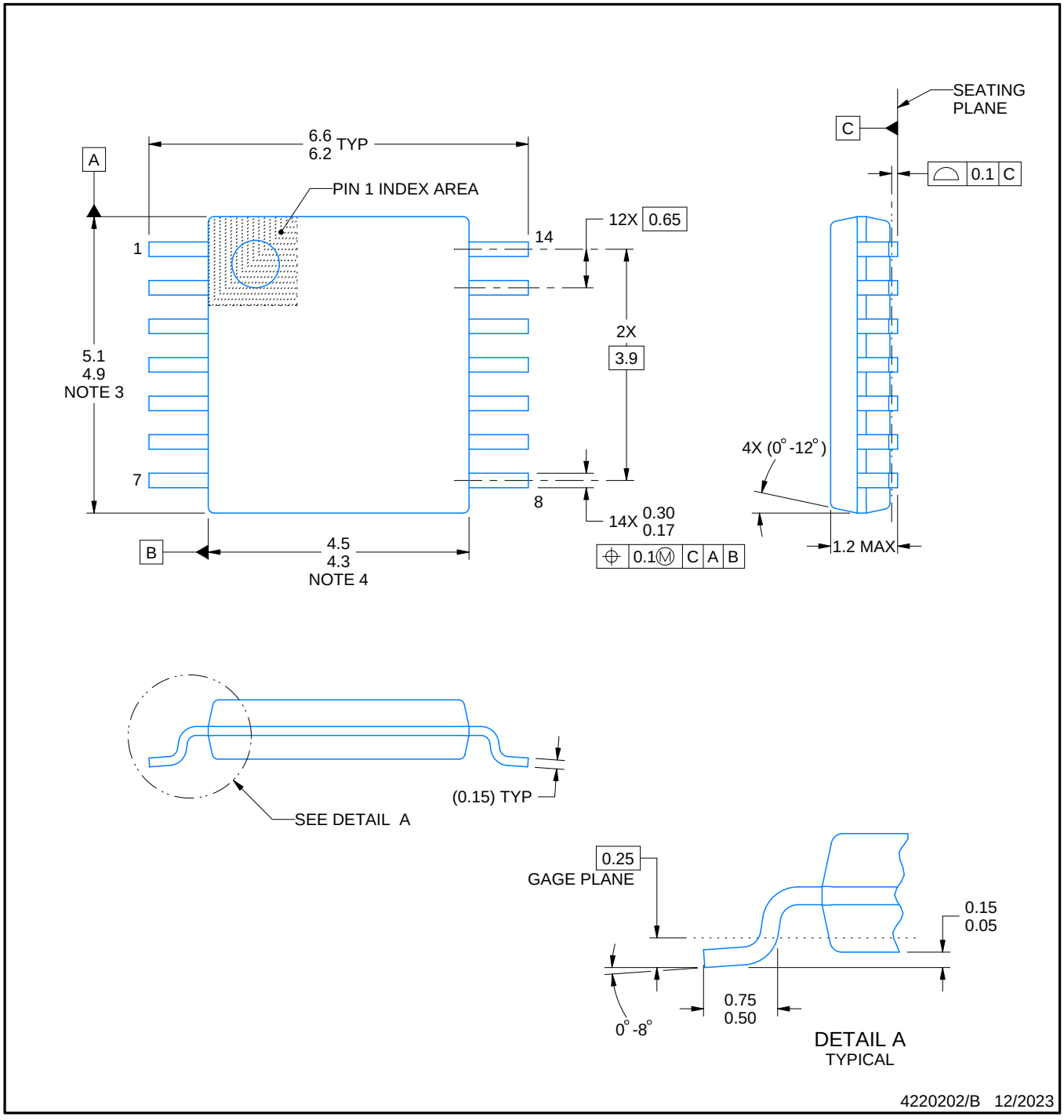
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

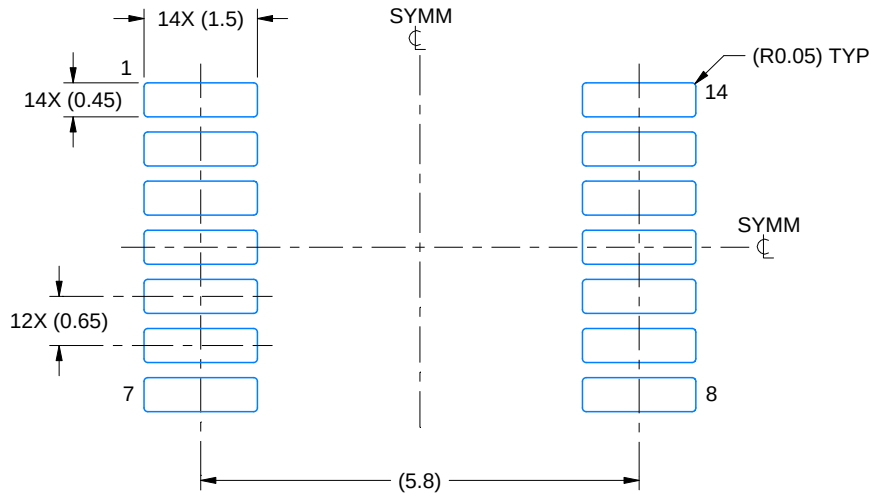
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

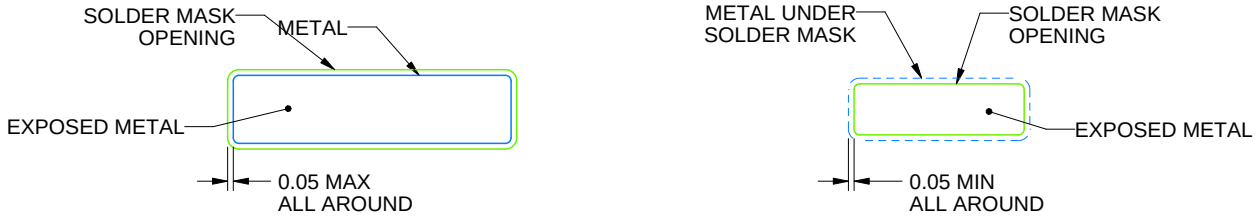


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

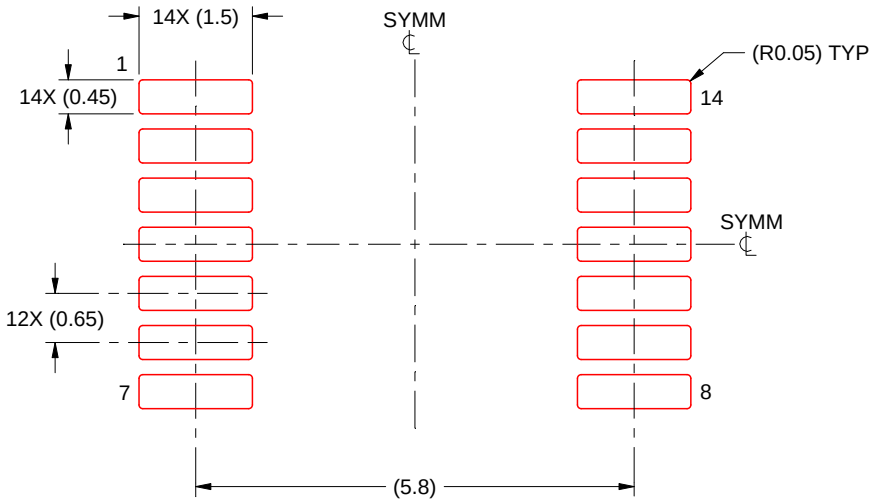


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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