SN74LVC1G08-Q1 单通道双输入正与门

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 1：–40°C 至 +125°C，T_A
- 支持运行： 5V V_{CC}
- 过压容差输入：最高可达 5.5V
- 支持向下转换：到 V_{CC}
- 低功耗：最大 10µA I_{CC}
- 3.3V 时，输出驱动为 ±24mA
- I_{off} 支持带电插入、局部关断模式和后驱动保护
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 完全符合面向汽车应用的标准
- 将多个电源轨的电源正常信号相结合
- 防止在条件为真时传递信号
- 将低电平有效误差信号进行结合

3 说明

该单路 2 输入正与门专为在 1.65V 至 5.5V V_{CC} 电压下运行而设计。

SN74LVC1G08-Q1 器件以正逻辑执行布尔函数或 $Y = A \cdot B$ 或 $Y = \overline{\overline{A} + \overline{B}}$。

该器件专用于使用 I off 的局部断电应用。I off 电路禁用输出，从而可防止其断电时破坏性电流从该器件回流。

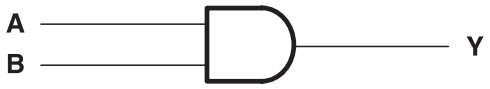
CMOS 器件具有高输出驱动，同时在宽 V_{CC} 工作范围内保持低静态功率耗散。

SN74LVC1G08-Q1 采用多种封装，包括封装尺寸为 1.45mm × 1.00mm 的超小型 DRY 封装。

封装信息

器件名称	封装(1)	封装尺寸(2)
SN74LVC1G08-Q1	DBV（SOT-23，5）	2.90mm × 1.60mm
	DCK（SC70，5）	2.00mm × 1.25mm
	DRY, (SON, 6)	1.45mm × 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



正逻辑图

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4 引脚配置和功能

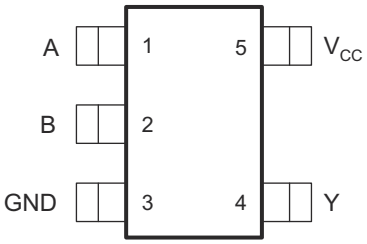


图 4-1. DBV 封装 5 引脚 SOT-23 （顶视图）

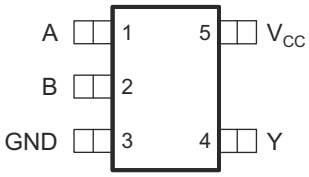
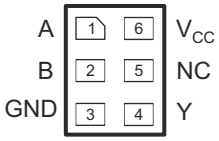


图 4-2. DCK 封装 5 引脚 SC-70 （顶视图）



NC – 无内部连接

请参阅机械制图，了解尺寸。

图 4-3. DRY 封装 6 引脚 SON （顶视图）

引脚功能

引脚			I/O	说明
名称	编号 DBV、DCK	编号 DRY		
A	1	1	输入	输入 A
B	2	2	输入	输入 B
GND	3	3	—	接地
NC		5	—	无内部连接
V_{CC}	5	6	—	正电源
Y	4	4	输出	输出 Y

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5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	6.5	V
V_I	输入电压范围(2)		-0.5	6.5	V
V_O	在高阻抗或断电状态对任一输出施加的电压范围(2)		-0.5	6.5	V
V_O	应用到任一处于高电平或低电平状态输出的电压范围(2) (3)		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	V_I < 0		-50	mA
I_{OK}	输出钳位电流	V_O < 0		-50	mA
I_O	持续输出电流			±50	mA
	通过 V_{CC} 或 GND 的持续电流			±100	mA
T_J	结温			150	°C
T_{stg}	贮存温度		-65	150	°C

(1) 超出*绝对最大额定值*运行可能会对器件造成永久损坏。*绝对最大额定值*并不表示器件在这些条件下或在*建议运行条件*以外的任何其他条件下能够正常运行。如果超出*建议运行条件*但在*绝对最大额定值*范围内使用，器件可能不会完全正常运行，这可能影响器件的可靠性、功能和性能并缩短器件寿命。
(2) 如果遵守输入和输出电流额定值，则可能会超过输入和输出负电压额定值。
(3) V_{CC} 的值在*建议运行条件*表中提供。

5.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模式 (HBM)，符合 AEC Q100-002(1) HBM ESD 分类等级	±2000	V
		充电器件模型 (CDM)，符合 AEC Q100-011 CDM ESD 分类等级	±1000	

(1) AEC Q100-002 指示应当按照 ANSI/ESDA/JEDEC JS-001 规范执行 HBM 应力测试。

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5.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压	工作	1.65	5.5	V
		仅数据保留	1.5		
V_{IH}	高电平输入电压	V_{CC} = 1.65V 至 1.95V	0.65 × V_{CC}		V
		V_{CC} = 2.3V 至 2.7V	1.7		
		V_{CC} = 3V 至 3.6V	2		
		V_{CC} = 4.5V 至 5.5V	0.7 × V_{CC}		
V_{IL}	低电平输入电压	V_{CC} = 1.65V 至 1.95V		0.35 × V_{CC}	V
		V_{CC} = 2.3V 至 2.7V		0.7	
		V_{CC} = 3V 至 3.6V		0.8	
		V_{CC} = 4.5V 至 5.5V		0.3 × V_{CC}	
V_I	输入电压		0	5.5	V
V_O	输出电压		0	V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 1.65V		-4	mA
		V_{CC} = 2.3V		-8	
		V_{CC} = 3V		-16	
				-24	
		V_{CC} = 4.5V		-32	
I_{OL}	低电平输出电流	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3V		16	
				24	
		V_{CC} = 4.5V		32	
$\Delta t/\Delta v$	输入转换上升或下降速率	V_{CC} = 1.8V ± 0.15V，2.5V ± 0.2V		20	ns/V
		V_{CC} = 3.3V ± 0.3V		10	
		V_{CC} = 5V ± 0.5V		5	
T_A	自然通风条件下的工作温度	“Q”后缀器件	-40	125	°C
		“I”后缀器件	-40	85	°C

(1) 器件所有未使用的输入引脚必须保持连接至 V_{CC} 或 GND，以确保器件正常工作。参阅 TI *慢速或浮点 CMOS 输入影响* 应用说明。

5.4 热性能信息

热指标(1)		SN74LVC1G08-Q1			单位
		DBV	DCK	DRY	
		5 引脚	5 引脚	6 引脚	
$R_{\theta JA}$	结至环境热阻	357.1	371	264.4	°C/W
$R_{\theta JCtop}$	结至外壳（顶部）热阻	263.7	297.5	166.6	°C/W
$R_{\theta JB}$	结至电路板热阻	264.4	258.6	142.2	°C/W
ψ_{JT}	结至顶部特征参数	195.6	195.6	26.1	°C/W
ψ_{JB}	结至电路板特征参数	262.2	256.2	141.6	°C/W
$R_{\theta JCbot}$	结至外壳（底部）热阻	–	–	–	°C/W

(1) 有关新旧热指标的更多信息，请参阅 *半导体和 IC 封装热指标* 应用手册。

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5.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数		测试条件	V_{CC}	-40°C 至 85°C			建议 -40°C 至 125°C			单位
				最小值	典型值 (1)	最大值	最小值	典型值	最大值	
V_{OH}		I_{OH} = –100 μA	1.65V 至 5.5V	V_{CC} – 0.1			V_{CC} – 0.15			V
		I_{OH} = -4mA	1.65V	1.2			1.2			
		I_{OH} = -8mA	2.3V	1.9			1.9			
		I_{OH} = -16mA	3V	2.4			2.4			
		I_{OH} = -24mA		2.3			2.3			
		I_{OH} = -32mA	4.5V	3.8			3.8			
V_{OL}		I_{OL} = 100 μA	1.65V 至 5.5V			0.1			0.1	V
		I_{OL} = 4mA	1.65V			0.45			0.45	
		I_{OL} = 8mA	2.3V			0.3			0.3	
		I_{OL} = 16mA	3V			0.4			0.4	
		I_{OL} = 24mA				0.55			0.55	
		I_{OL} = 32mA	4.5V			0.55			0.55	
I_I	A 或 B 输入	V_I=5.5 V 或 GND	0 至 5.5V			±5			±5	μA
I_{off}		V_I 或 V_O = 5.5V	0			±10			±10	μA
I_{CC}		V_I = 5.5V 或 GND，I_O = 0	1.65V 至 5.5V			10			10	μA
ΔI_{CC}		一个输入电压为 V_{CC} – 0.6V，其他输入电压为 V_C 或 GND	3V 至 5.5V			500			500	μA
C_i		V_I = V_{CC} 或 GND	3.3V		4			4		pF

(1) 所有典型值均在 V_{CC} = 3.3V、T_A = 25°C 下测得。

5.6 开关特性，T_A = –40°C 至 125°C

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅 图 6-1）

参数	从（输入）	至（输出）	-40°C 至 125°C								单位
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			最小值	最大值	最小值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A 或 B	Y	1	10	1	7.5	1	6.5	1	6	ns

5.7 开关特性，T_A = –40°C 至 85°C

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅 图 6-2）

参数	从（输入）	至（输出）	-40°C 至 85°C								单位
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			最小值	最大值	最小值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A 或 B	Y	2.4	8	1.1	5.5	1	4.5	1	4	ns

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5.8 工作特性

T_A = 25°C

参数		测试条件	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	单位
			典型值	典型值	典型值	典型值	
C_{pd}	功率耗散电容	f = 10MHz	21	24	26	31	pF

5.9 典型特性

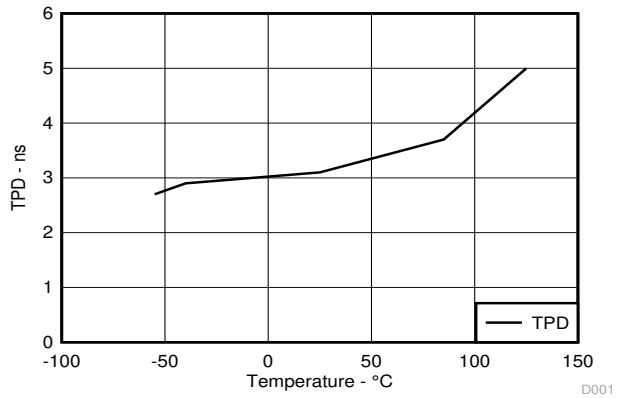


图 5-1. 3.3V V_{CC} 时传输延迟 (t_{pd}) 与温度间的关系

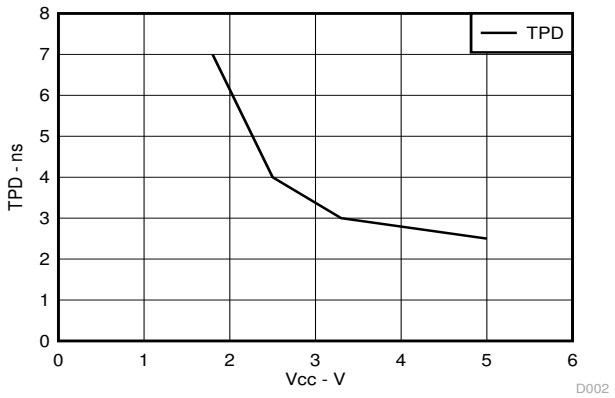
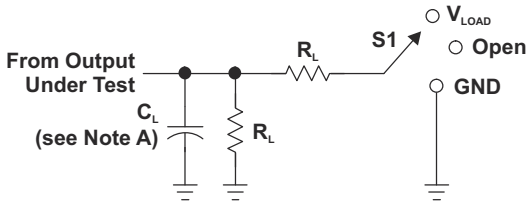


图 5-2. 25°C 时传输延迟 (t_{pd}) 与 V_{CC} 间的关系

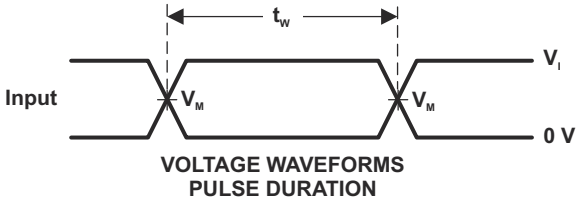
6 参数测量信息



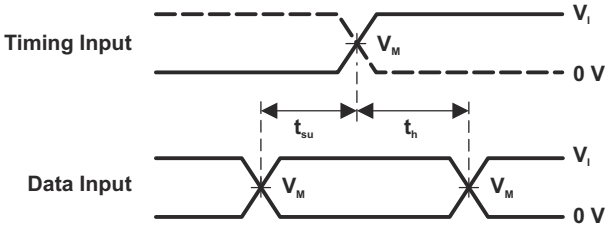
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

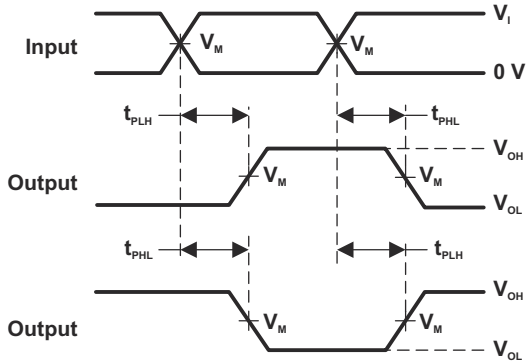
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.3 V



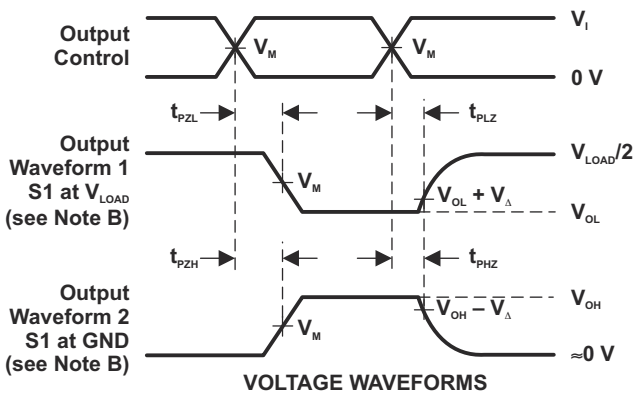
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 6-1. 负载电路和电压波形

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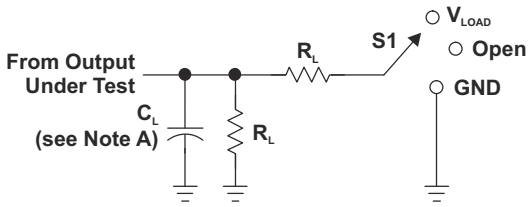
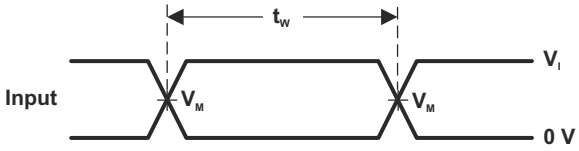


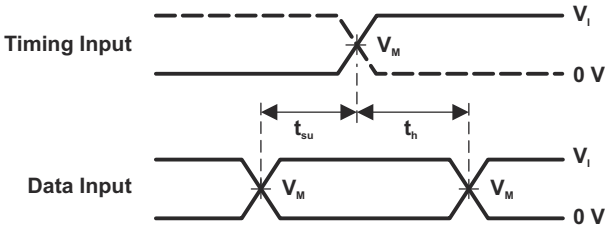
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

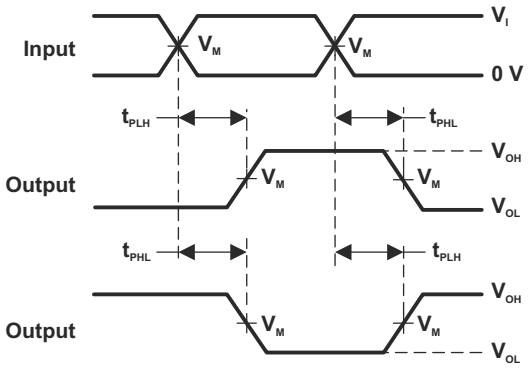
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



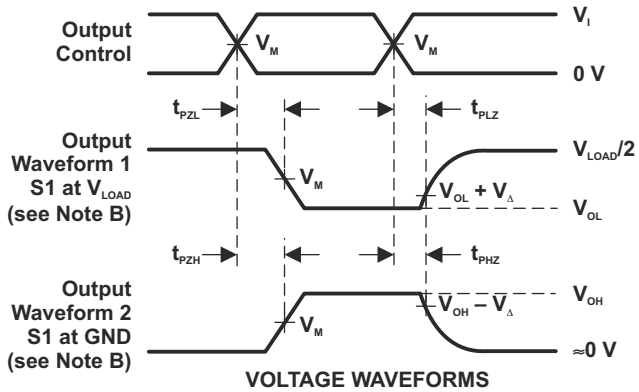
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 6-2. 负载电路和电压波形

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7 详细说明

7.1 概述

SN74LVC1G08-Q1 器件包含一个双输入正逻辑与门，可执行布尔函数 Y = A · B 或 Y = $\overline{\text{A}}$ + $\overline{\text{B}}$。SN74LVC1G08-Q1 通过 Ioff 特性全面支持局部断电应用。Ioff 电路可禁用输出，以防在器件断电时电流回流对器件造成损坏。

7.2 功能方框图

7.3 特性说明

- 1.65V 至 5.5V 的宽工作电压范围
- 支持降压转换
- 输入电压高达 5.5V
- I_{off} 特性允许在 V_{CC} 为 0V 时在输入和输出上产生电压

7.4 器件功能模式

表 7-1. 功能表

输入		输出
A	B	Y
H	H	H
L	X	L
X	L	L

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8 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

SN74LVC1G08-Q1 是一款高驱动 CMOS 器件，可用于实现具有高输出驱动的“与”逻辑，例如 LED 应用。本器件可以在 3.3V 下产生 24mA 驱动电流，因此 SN74LVC1G08-Q1 非常适合驱动多个输出，也适合用于高达 100MHz 的高速应用。输入可耐受 5.5V 电压，允许将该器件降压转换至 V_{CC}。

8.2 典型应用

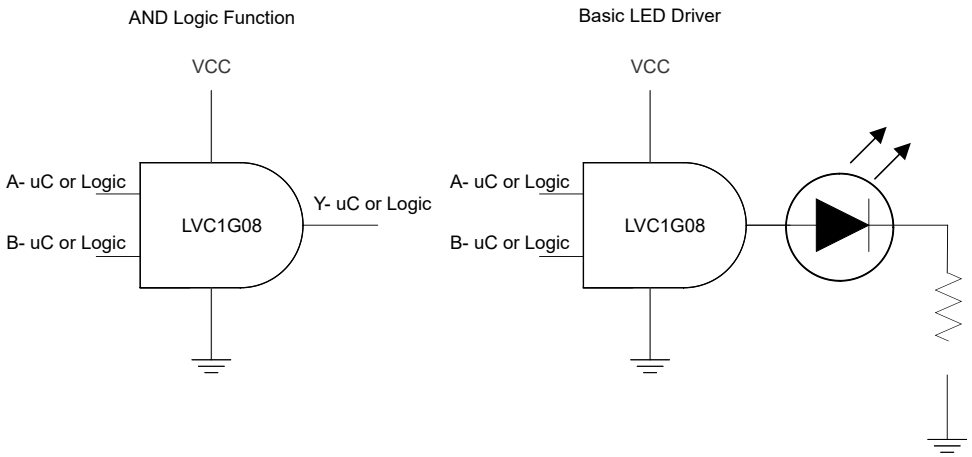

图 8-1. 典型应用示例

8.2.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。避免总线争用，因为它可以驱动超过最大限值的电流。高驱动能力也会在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。

8.2.2 详细设计过程

1. 建议的输入条件
   - 上升时间和下降时间规格。请参阅*建议运行条件* 表中的 $\Delta t/\Delta V$。
   - 指定的高电平和低电平。请参阅*建议运行条件* 表中的 V_{IH} 和 V_{IL}。
   - 输入可耐受过压，允许它们在任何有效 V_{CC} 下高达*建议运行条件* 表中的（V_I 最大值）。
2. 建议的输出条件
   - 每路输出的负载电流不得超过（I_O 最大值）以及该器件的总电流（通过 V_{CC} 或 GND 的持续电流）。这些限值位于*绝对最大额定值* 表中。
   - 输出不应被拉至高于 V_{CC}。

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8.2.3 应用曲线

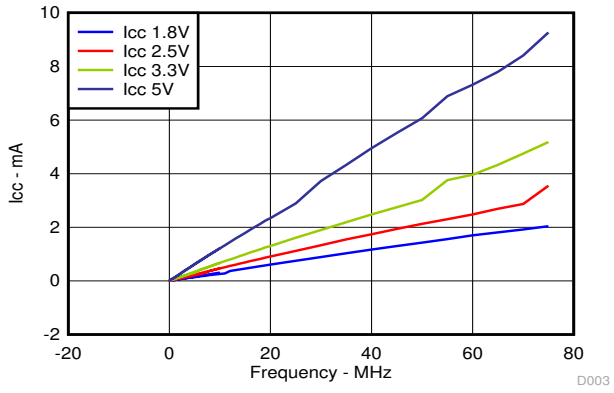

图 8-2. ICC 与频率间的关系

8.3 电源相关建议

电源可以是 *建议运行条件* 表中最小和最大电源电压额定值之间的任何电压。

为了防止功率干扰，请确认每个 Vcc 引脚是否都具有良好的旁路电容器。对于单电源器件，建议使用 0.1 μ F 电容器，如果有多个 Vcc 引脚，则建议为每个电源引脚使用 0.01μF 或 0.022μF 电容器。并联多个旁路电容器以抑制不同的噪声频率。0.1 μ F 和 1 μ F 电容器通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源引脚安装。

8.4 布局

8.4.1 布局指南

当使用多位逻辑器件时，验证输入不会悬空。在许多情况下，未使用数字逻辑器件的全部或部分功能；例如，仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个。不要让此类输入引脚断开，因为外部连接处的未定义电压会导致运行状态。以下指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至高或低偏置以防悬空。向任何特定未使用的输入施加的逻辑电平取决于器件的功能。通常，将这些输入连接到 Gnd 或 Vcc，具体情况视合理性或便利性而定。

8.4.2 布局示例

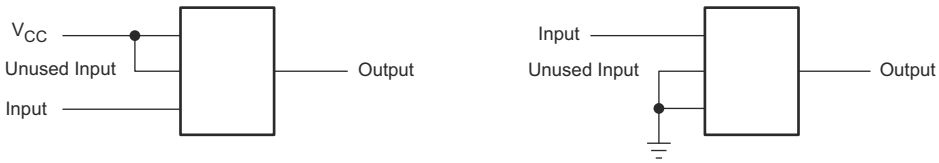

图 8-3. 布局示例

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9 器件和文档支持

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from MAY 20, 2019 to AUGUST 14, 2026 (from Revision G (May 2019) to Revision H (August 2026))	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 将 DBV 封装的结至环境热阻值从：209.4°C/W 更改为：357.1°C/W	5
• 将 DBV 封装的结至外壳（顶部）热阻值从：132.5°C/W 更改为：263.7°C/W	5
• 将 DBV 封装的结至电路板特征值从：118.1°C/W 更改为：264.4°C/W	5
• 将 DBV 封装的结至顶部特征值从：48.8°C/W 更改为：195.6°C/W	5
• 将 DBV 封装的结至电路板特征值从：117.4°C/W 更改为：262.2°C/W	5
• 将 DCK 封装的结至环境热阻值从：244.2°C/W 更改为：371°C/W	5
• 将 DCK 封装的结至外壳（顶部）热阻值从：156.1°C/W 更改为：297.5°C/W	5
• 将 DCK 封装的结至电路板特征值从：130°C/W 更改为：258.6°C/W	5
• 将 DCK 封装的结至顶部特征值从：47.2°C/W 更改为：195.6°C/W	5
• 将 DCK 封装的结至电路板特征值从：130°C/W 更改为：256.2°C/W	5

Changes from Revision F (April 2008) to Revision G (June 2019)	Page
• 根据新的 TI 格式更改了数据表	1
• 向“*器件信息*表”中添加了 DRY 封装。	1
• 添加了*热性能信息* 表	5
• 添加了*典型特性*。	7
• 添加了*详细说明*部分。	10

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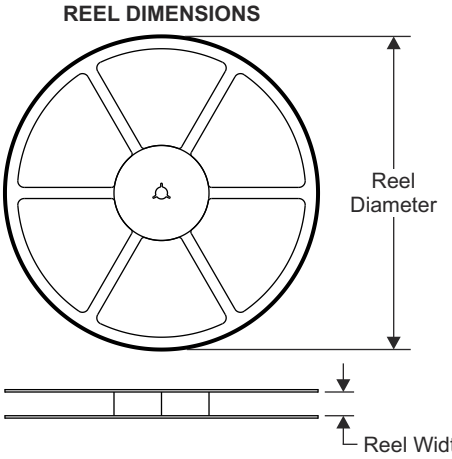
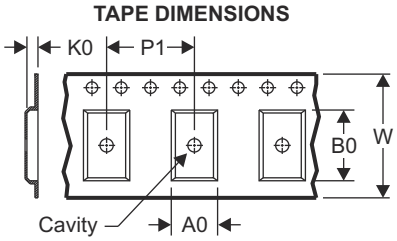
- 添加了*应用和实施*部分。 11
- 添加了*电源建议*部分。 12
- 添加了*布局*部分。 12

11 机械、封装和可订购信息

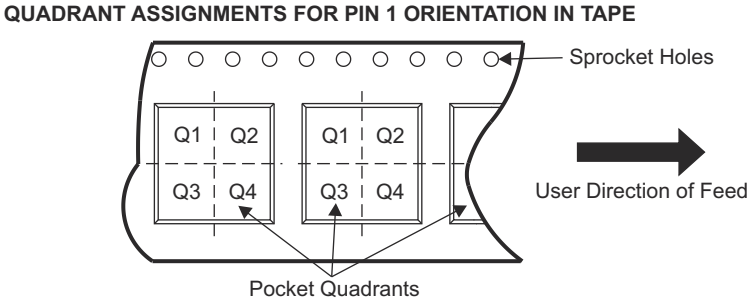
以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

11.1 卷带包装信息





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



器件	封装类型	封装图	引脚	SPQ	卷带直径 (mm)	卷带宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1象限
SN74LVC1G08-Q1	X2SON	DTX	5	3000	180	8.4	1	1.25	0.48	2.0	8.0	Q1

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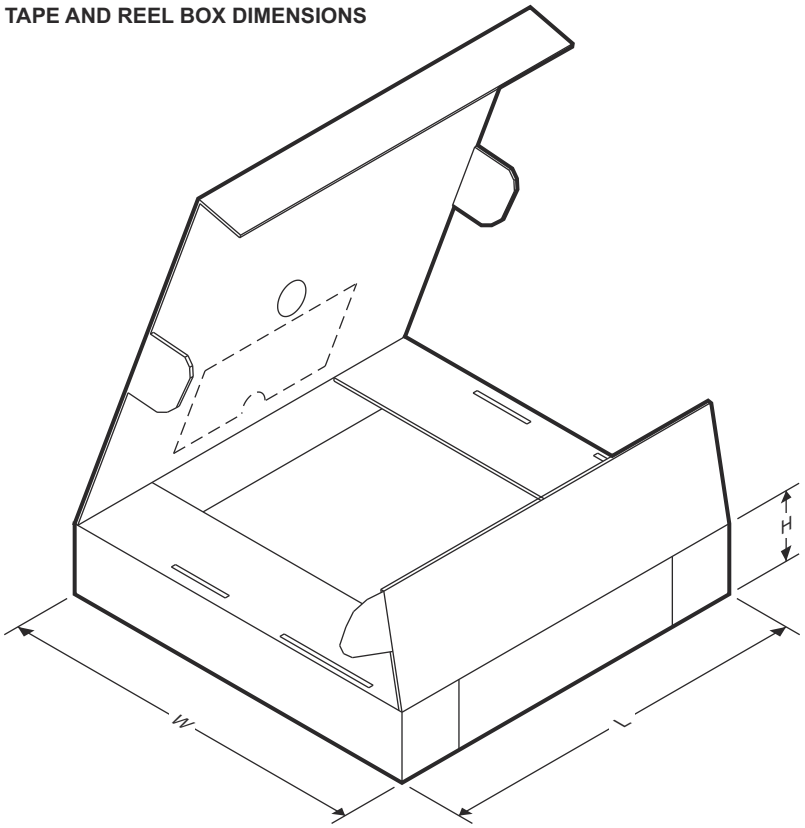
TAPE AND REEL BOX DIMENSIONS



器件	封装类型	封装图	引脚	SPQ	长度 (mm)	宽度 (mm)	高度 (mm)
SN74LVC1G08-Q1	X2SON	DTX	5	3000	210	185	35

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVC1G08QDBVRQ1G4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(33H5, C08O)
74LVC1G08QDBVRQ1G4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(33H5, C08O)
74LVC1G08QDCKRQ1G4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEO
74LVC1G08QDCKRQ1G4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEO
SN74LVC1G08IDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	CEO
SN74LVC1G08IDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CEO
SN74LVC1G08IDCKRQ1.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CEO
SN74LVC1G08QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(33H5, C08O)
SN74LVC1G08QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(33H5, C08O)
SN74LVC1G08QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(33H5, C08O)
SN74LVC1G08QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CEJ, CEO)
SN74LVC1G08QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CEJ, CEO)
SN74LVC1G08QDCKRQ1.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CEJ, CEO)
SN74LVC1G08QDRYRQ1	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EM
SN74LVC1G08QDRYRQ1.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G08-Q1 :

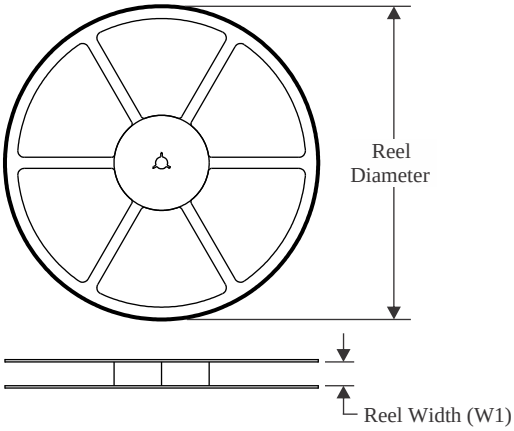
- Catalog : SN74LVC1G08
- Enhanced Product : SN74LVC1G08-EP

NOTE: Qualified Version Definitions:

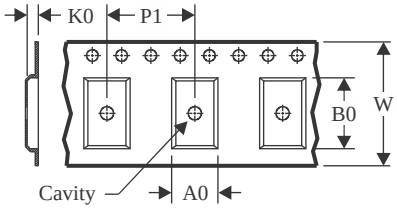
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

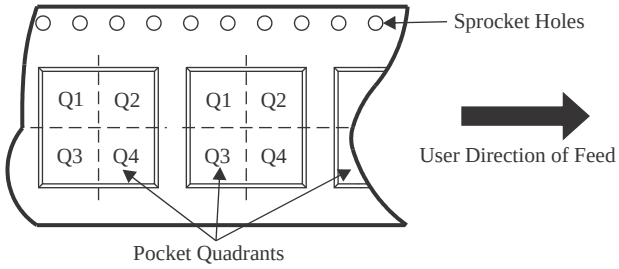


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

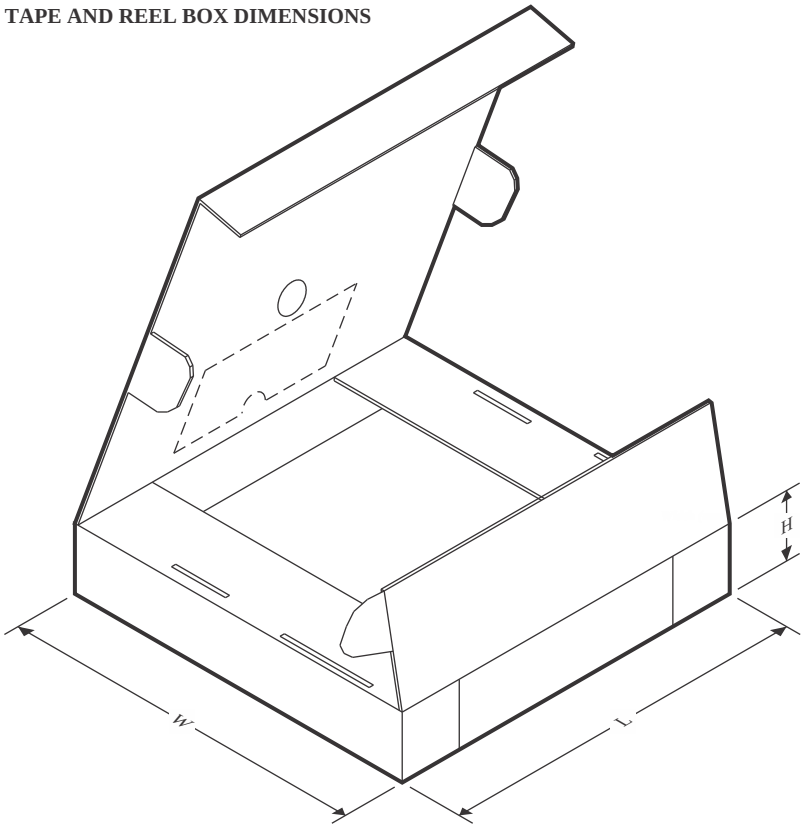
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G08QDBVRQ1G4	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
74LVC1G08QDBVRQ1G4	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
74LVC1G08QDCKRQ1G4	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08IDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G08IDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

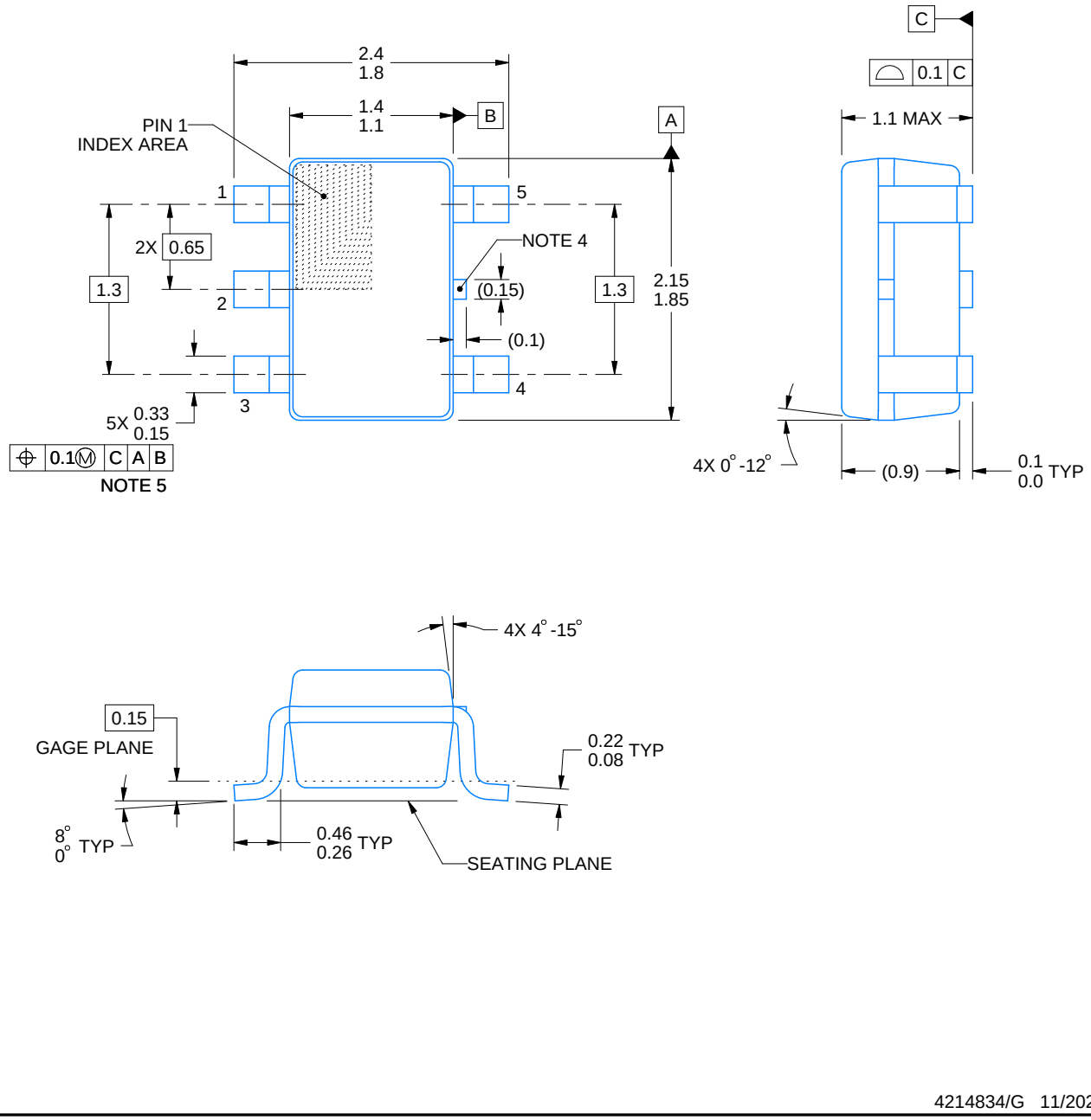
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G08QDBVRQ1G4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74LVC1G08QDBVRQ1G4	SOT-23	DBV	5	3000	200.0	183.0	25.0
74LVC1G08QDCKRQ1G4	SC70	DCK	5	3000	200.0	183.0	25.0
SN74LVC1G08IDCKRQ1	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G08IDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0
SN74LVC1G08QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

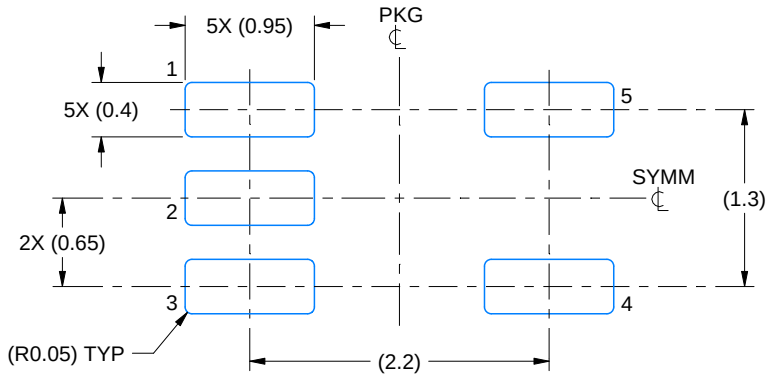
SMALL OUTLINE TRANSISTOR



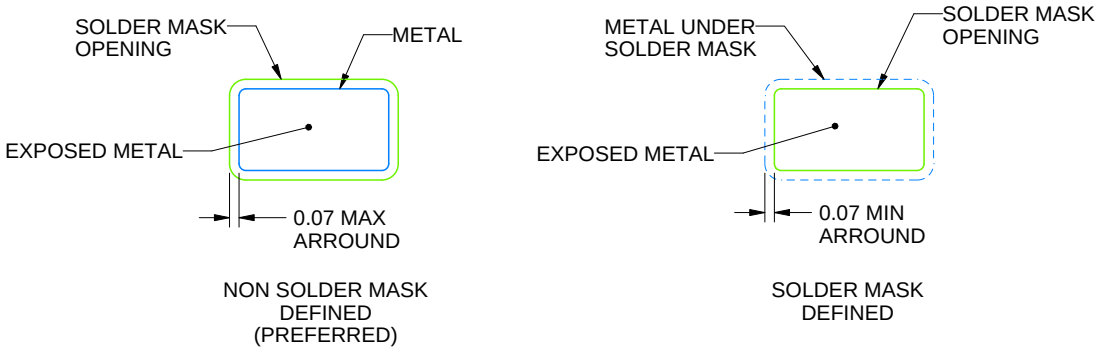
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

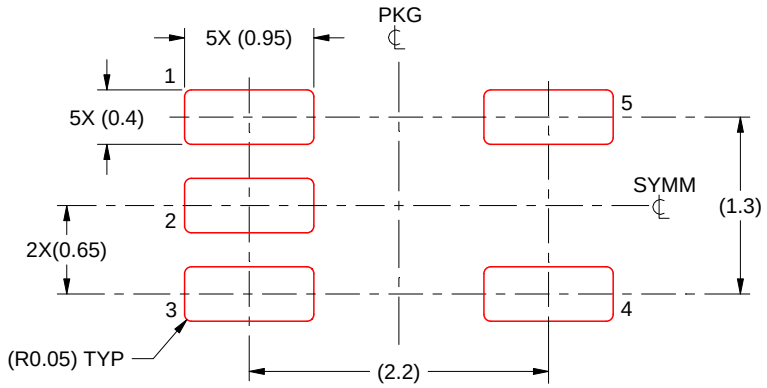


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

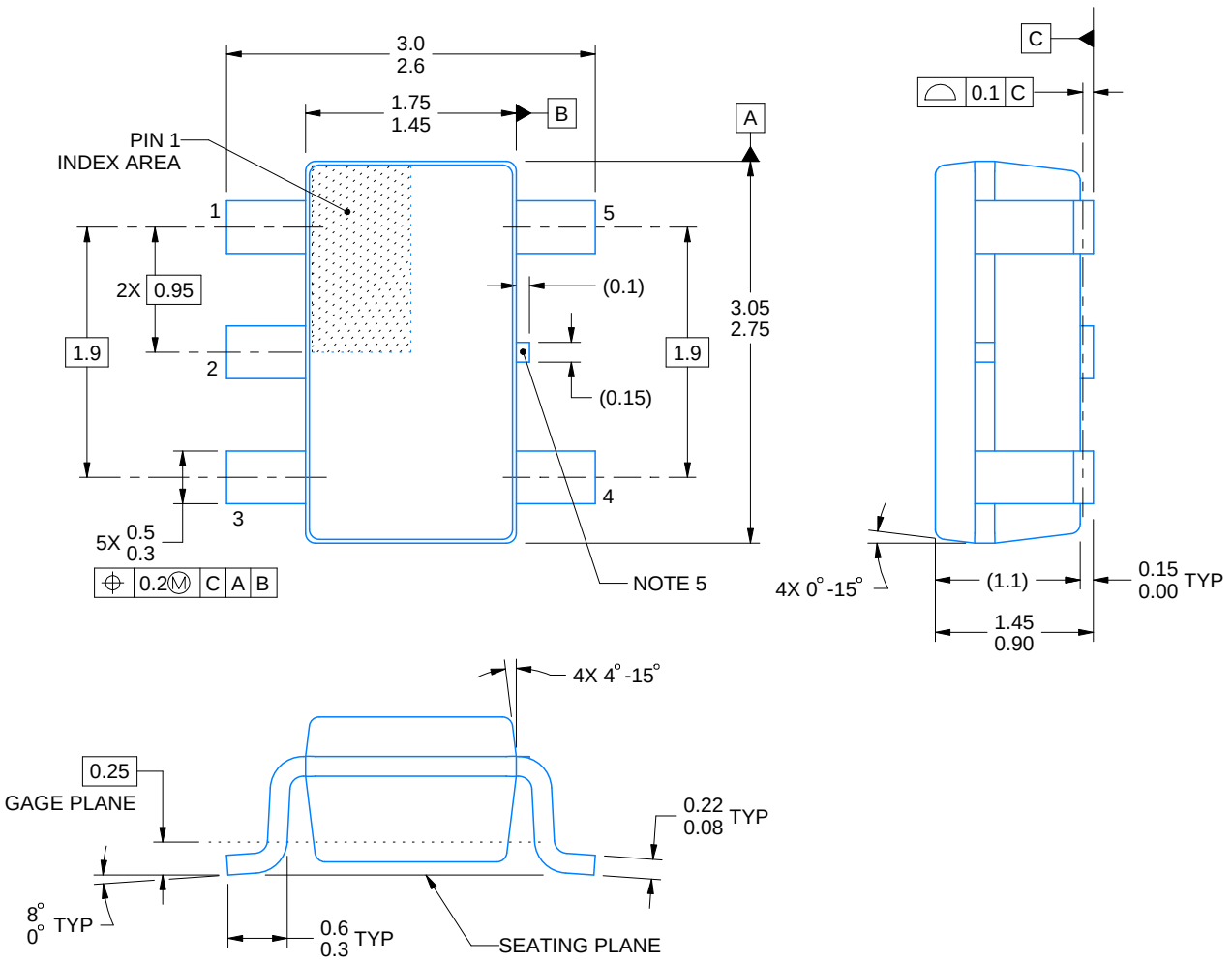
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

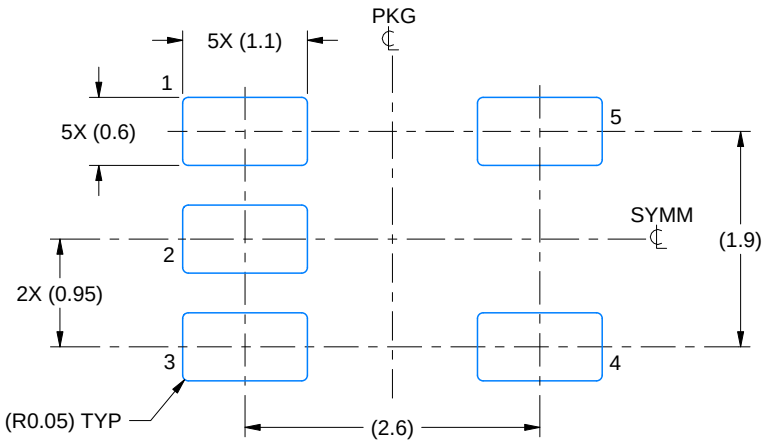
SMALL OUTLINE TRANSISTOR



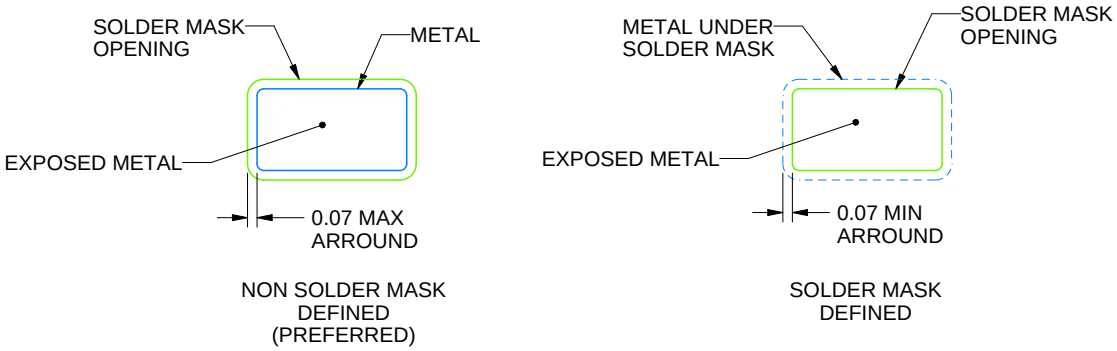
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

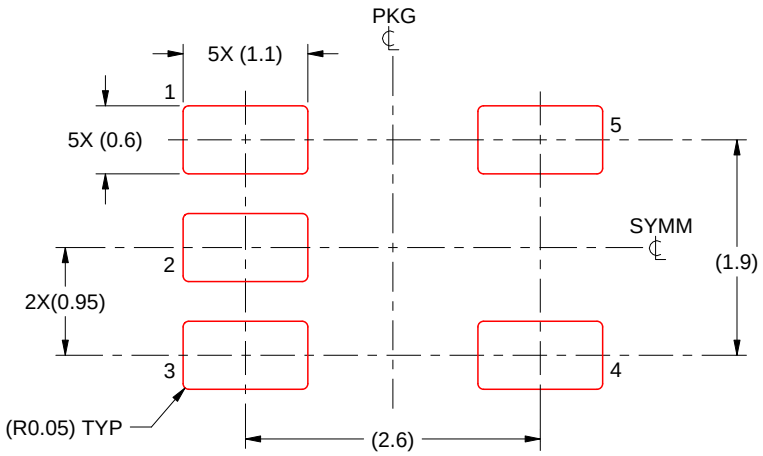


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

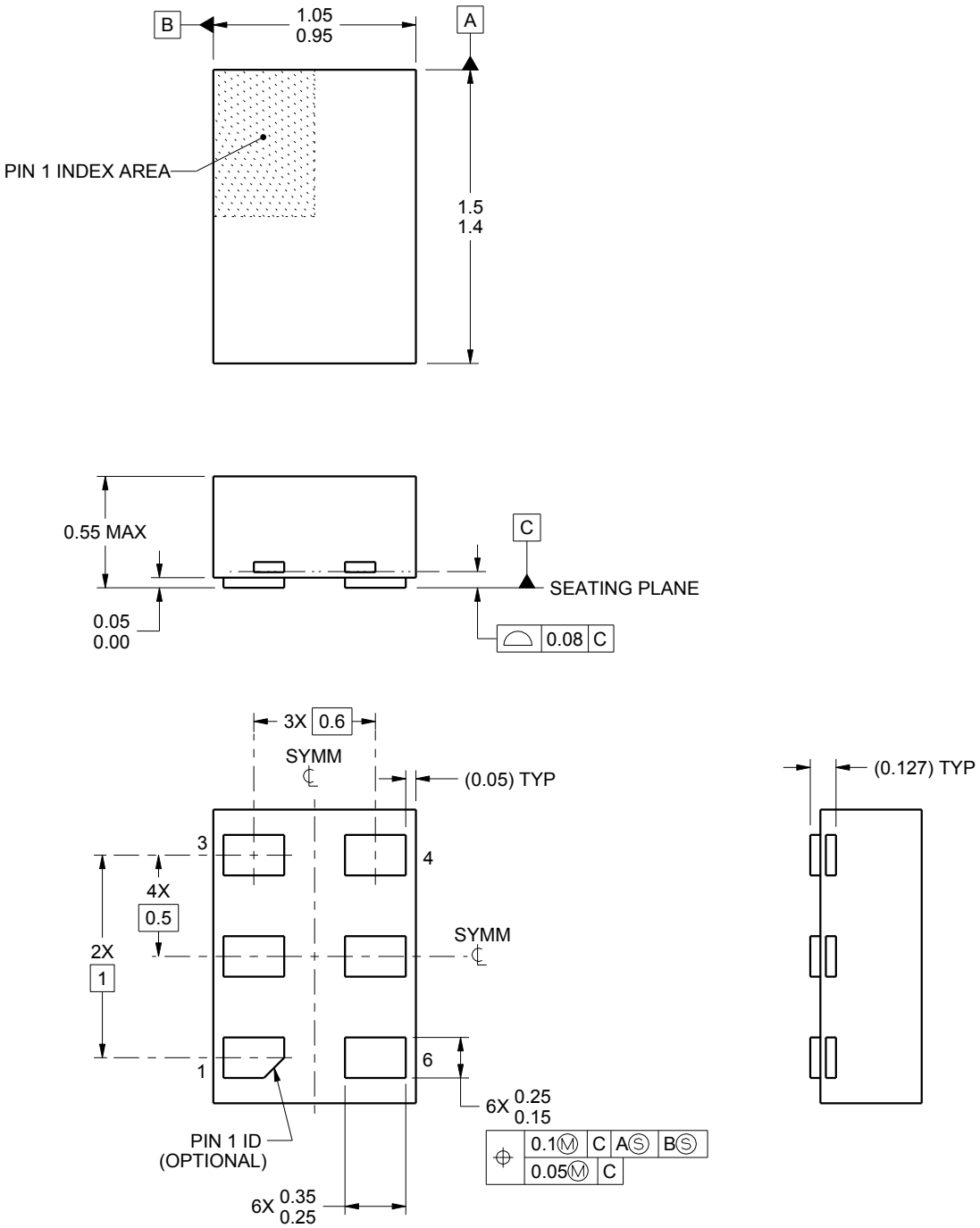
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRY0006B

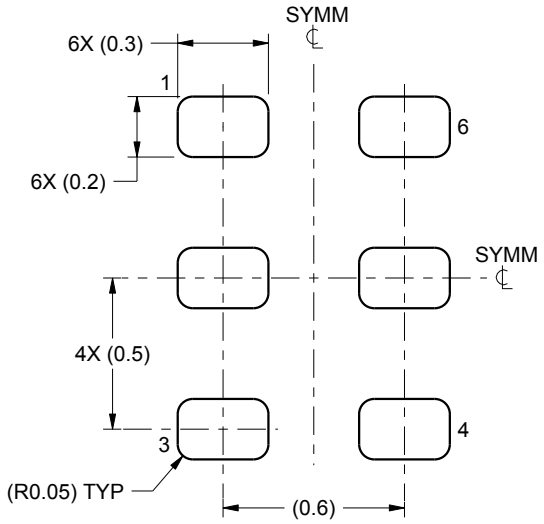
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

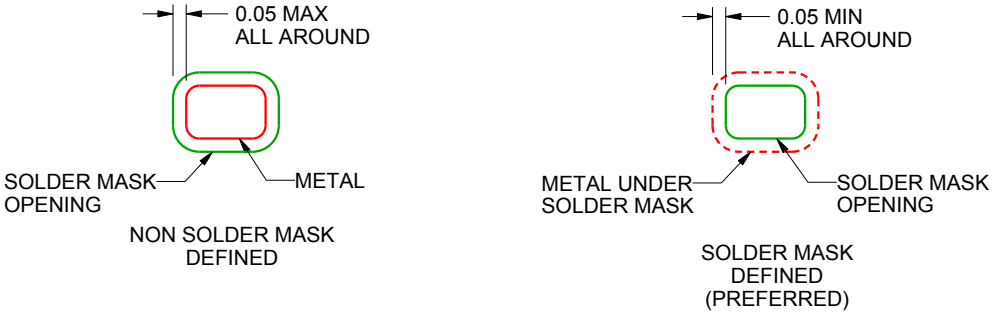


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X

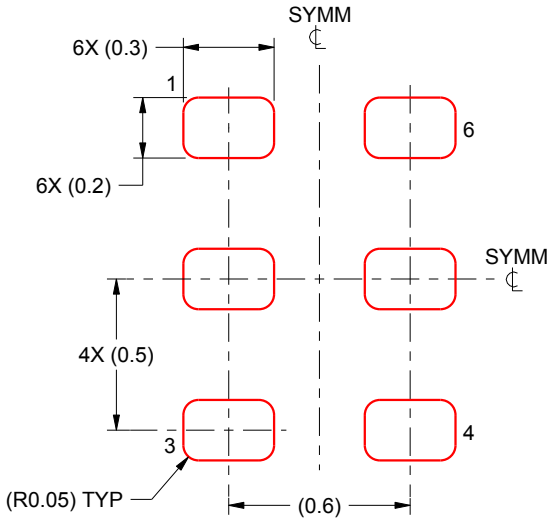


SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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