具有 ACPI 支持的 UCD90160A 16 轨电源序列发生器和监视器

1 特性

- 可对 16 个电压轨进行监控和排序
  - 所有电压轨每 400µs 进行一次采样
  - 具有 2.5V、0.5% 内部 V_{REF} 的 12 位 ADC
  - 排序基于时间、电压轨及引脚相关性
  - 每个监控器具有 4 个可编程欠压和过压阈值
- 每个监控器可提供非易失性误差及峰值日志记录（多达 12 个故障详细条目）
- 针对 10 个电压轨的闭环裕度调节能力
  - 裕度输出可调节轨电压以匹配用户定义的裕度阈值
- 可编程的看门狗计时器和系统复位
- 可轻松级联多个电源序列发生器并加以协调以提供故障响应
- 具备引脚选择电源轨状态功能，用于 ACPI 支持
- 灵活的数字 I/O 配置
- 可级联多个器件
- 响应并监视由 GPI 触发的故障
- 多相位 PWM 时钟发生器
  - 时钟频率为 15.259kHz 至 125MHz
  - 能够为同步开关模式电源配置独立的时钟输出
- JTAG和I^2C/SMBus/PMBus™接口

2 应用

- 有线网络
- 无线基础设施
- 数据通信模块
- 数据中心和企业级计算
- 工厂自动化和控制
- 测试和测量
- 医疗

3 说明

UCD90160A 是一款 16 轨 PMBus/I^2C 可寻址电源序列发生器和监视器。该器件集成一个 12 位 ADC，用于监视多达 16 个电源电压输入。26 个 GPIO 引脚可用于电源使能端、加电复位信号、外部中断、级联或其它系统功能。这些引脚中有 12 个引脚提供 PWM 功能。利用这些引脚，UCD90160A 可支持裕度调节以及通用 PWM 功能。

运用引脚选择电压轨状态功能可实现特定的电源状态。该功能允许使用多达3个GPI来启用和停用任意电压轨。对于执行系统低功耗模式及用于硬件设备的高级配置和电源接口 (ACPI) 规范而言，这一点是很有用处的。

凭借故障引脚功能，可以轻松级联多个器件并对其加以协调，使其同步响应故障。

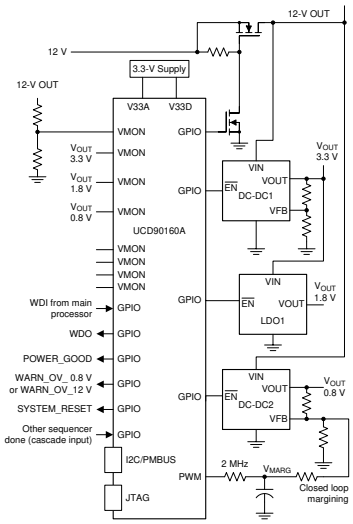
这个TI的 融合数字电源™设计人员软件用于器件配置。这款基于PC的图形用户界面 (GUI) 提供了一种用于配置，存储和监视所有系统操作参数的直观界面。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCD90160A	VQFN (64)	9.00mm x 9.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化应用



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

Changes from Revision B (August 2019) to Revision C **Page**

- Changed Figure 32 ... 45
- Added two more design requirements ... 46

Changes from Revision A (February 2018) to Revision B **Page**

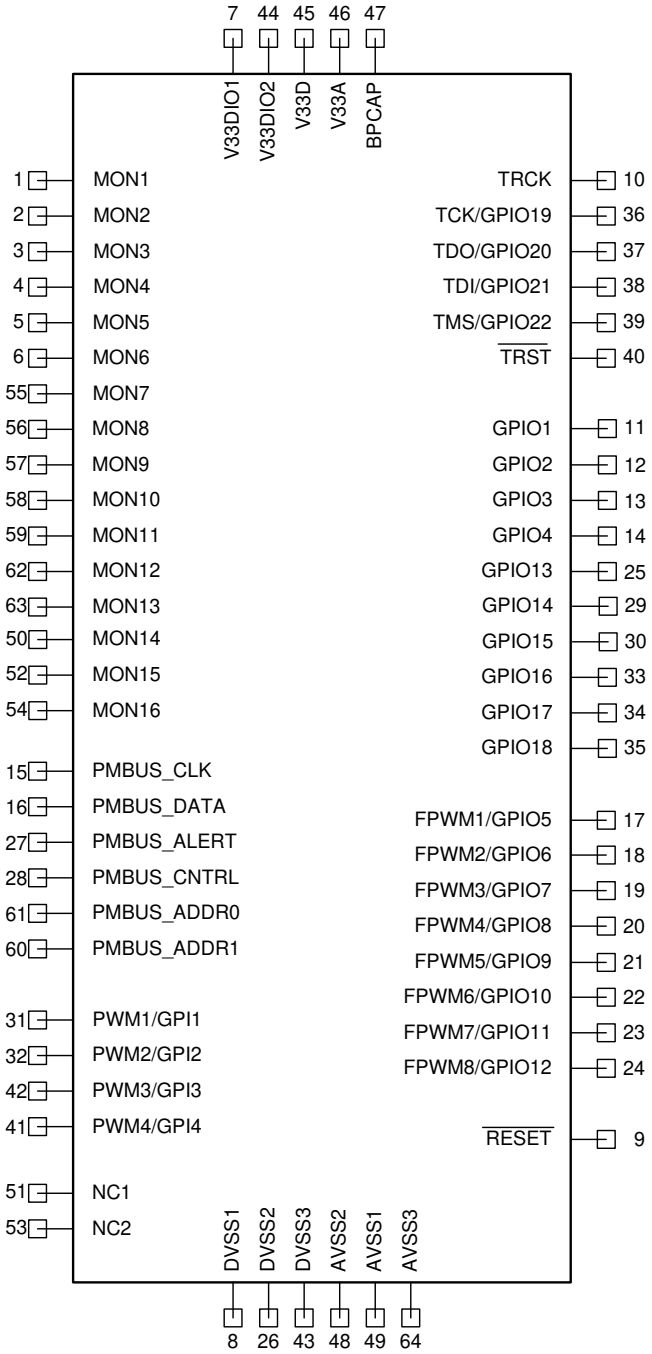
- 已更改 应用 列表中的封装尺寸参数 ... 1
- Changed "52" to "53" ... 5

Changes from Original (September 2016) to Revision A **Page**

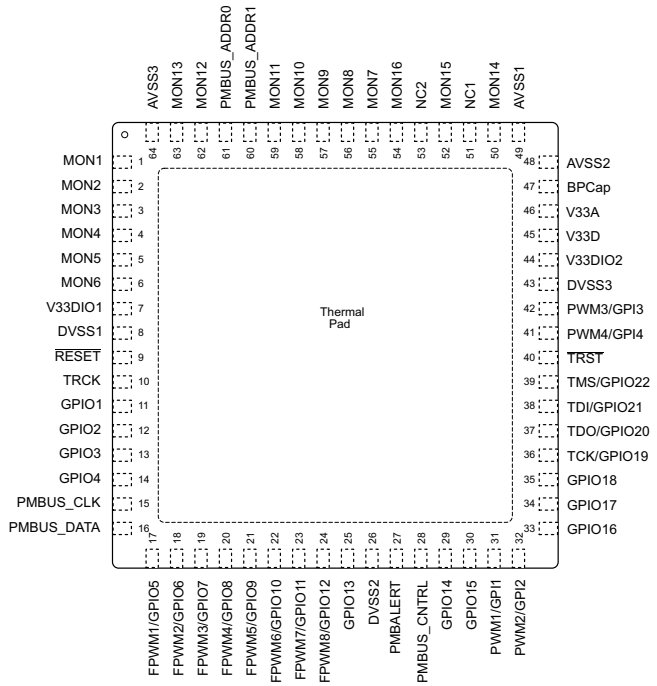
- Changed the *Timing Requirements* table ... 8
- Changed Figure 28 ... 38

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5 Pin Configuration and Functions



RGC Package
64-Pin VQFN
Top View



Pin Functions[1]

PIN		I/O	DESCRIPTION
NAME	NO.		
ANALOG MONITOR INPUTS			
MON1	1	I	Analog input (0 to 2.5 V)
MON2	2	I	Analog input (0 to 2.5 V)
MON3	3	I	Analog input (0 to 2.5 V)
MON4	4	I	Analog input (0 to 2.5 V)
MON5	5	I	Analog input (0 to 2.5 V)
MON6	6	I	Analog input (0 to 2.5 V)
MON7	55	I	Analog input (0 to 2.5 V)
MON8	56	I	Analog input (0 to 2.5 V)
MON9	57	I	Analog input (0 to 2.5 V)
MON10	58	I	Analog input (0 to 2.5 V)
MON11	59	I	Analog input (0 to 2.5 V)
MON12	62	I	Analog input (0 to 2.5 V)
MON13	63	I	Analog input (0 to 2.5 V)
MON14	50	I	Analog input (0.2 to 2.5 V)
MON15	52	I	Analog input (0.2 to 2.5 V)
MON16	54	I	Analog input (0.2 to 2.5 V)
GENERAL-PURPOSE INPUT AND OUTPUT			
GPIO1	11	I/O	General-purpose discrete I/O
GPIO2	12	I/O	General-purpose discrete I/O
GPIO3	13	I/O	General-purpose discrete I/O
GPIO4	14	I/O	General-purpose discrete I/O
GPIO13	25	I/O	General-purpose discrete I/O
GPIO14	29	I/O	General-purpose discrete I/O
GPIO15	30	I/O	General-purpose discrete I/O
GPIO16	33	I/O	General-purpose discrete I/O
GPIO17	34	I/O	General-purpose discrete I/O
GPIO18	35	I/O	General-purpose discrete I/O
PWM OUTPUTS			
FPWM1/GPIO5	17	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM2/GPIO6	18	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM3/GPIO7	19	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM4/GPIO8	20	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM5/GPIO9	21	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM6/GPIO10	22	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM7/GPIO11	23	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM8/GPIO12	24	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
PWM1/GPI1	31	I/PWM	Fixed 10-kHz PWM output or GPI
PWM2/GPI2	32	I/PWM	Fixed 1-kHz PWM output or GPI
PWM3/GPI3	42	I/PWM	PWM (0.93 Hz to 7.8125 MHz) or GPI
PWM4/GPI4	41	I/PWM	PWM (0.93 Hz to 7.8125 MHz) or GPI

(1) The maximum number of configurable rails is 16. The maximum number of configurable GPIs is 8. The maximum number of configurable Boolean Logic GPOs is 16.

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Pin Functions[1] (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PMBus COMM INTERFACE			
PMBUS_CLK	15	I/O	PMBus clock (must have pullup to 3.3 V)
PMBUS_DATA	16	I/O	PMBus data (must have pullup to 3.3 V)
PMBALERT	27	O	PMBus alert, active-low, open-drain output (must have pullup to 3.3 V)
PMBUS_CNTRL	28	I	PMBus control
PMBUS_ADDR0	61	I	PMBus analog address input. Least-significant address bit
PMBUS_ADDR1	60	I	PMBus analog address input. Most-significant address bit
JTAG			
TRCK	10	O	Test return clock
TCK/GPIO19	36	I/O	Test clock or GPIO
TDO/GPIO20	37	I/O	Test data out or GPIO
TDI/GPIO21	38	I/O	Test data in (tie to V_{DD} with 10-kΩ resistor) or GPIO
TMS/GPIO22	39	I/O	Test mode select (tie to V_{DD} with 10-kΩ resistor) or GPIO
$\overline{\text{TRST}}$	40	I	Test reset. Tie to ground with 10-kΩ resistor
INPUT POWER AND GROUNDS			
$\overline{\text{RESET}}$	9		Active-low device reset input. Hold low for at least 2 μs to reset the device. Refer to the Device Reset section.
V33A	46		Analog 3.3-V supply. Refer to the *Layout Guidelines* section.
V33D	45		Digital core 3.3-V supply. Refer to the *Layout Guidelines* section.
V33DIO1	7		Digital I/O 3.3-V supply. Refer to the *Layout Guidelines* section.
V33DIO2	44		Digital I/O 3.3-V supply. Refer to the *Layout Guidelines* section.
BPCap	47		1.8-V bypass capacitor. Refer to the *Layout Guidelines* section.
AVSS1	49		Analog ground
AVSS2	48		Analog ground
AVSS3	64		Analog ground
DVSS1	8		Digital ground
DVSS2	26		Digital ground
DVSS3	43		Digital ground
NC1	51		No Connect
NC2	53		No Connect
QFP ground pad	NA		Thermal pad – tie to ground plane.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Voltage applied at V33D to DV_{SS}	–0.3	3.8	V
Voltage applied at V33A to AV_{SS}	–0.3	3.8	V
Voltage applied to any other pin (2)	–0.3	(V33A + 0.3)	V
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage during operation (V_{33D}, V_{33DIO}, V_{33A})	3	3.3	3.6	V
Operating free-air temperature range, T_A	–40		110	°C
Junction temperature, T_J			125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCD90160A RGC [VQFN] 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	21.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	1.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SUPPLY CURRENT						
I_{V33A}	Supply current(1)	V_{V33A} = 3.3 V		8		mA
I_{V33DIO}		V_{V33DIO} = 3.3 V		2		mA
I_{V33D}		V_{V33D} = 3.3 V		40		mA
I_{V33D}		V_{V33D} = 3.3 V, storing configuration parameters in flash memory		50		mA
ANALOG INPUTS (MON1–MON16)						
V_{MON}	Input voltage range	MON1–MON13	0		2.5	V
		MON14–MON16	0.2		2.5	V
INL	ADC integral nonlinearity		–4		4	LSB
DNL	ADC differential nonlinearity		-2		2	LSB
I_{lkg}	Input leakage current	3 V applied to pin			100	nA
I_{OFFSET}	Input offset current	1-kΩ source impedance	–5		5	µA
R_{IN}	Input impedance	MON1–MON13, ground reference	8			MΩ
		MON14–MON16, ground reference	0.5	1.5	3	MΩ
C_{IN}	Input capacitance				10	pF
$t_{CONVERT}$	ADC sample period	16 voltages sampled, 3.89 µsec/sample		400		µsec
V_{REF}	ADC 2.5 V, internal reference accuracy	0°C to 125°C	–0.5%		0.5%	
		–40°C to 125°C	–1%		1%	
ANALOG INPUT (PMBUS_ADDRx)						
I_{BIAS}	Bias current for PMBus Addr pins		9		11	µA
V_{ADDR_OPEN}	Voltage – open pin	PMBUS_ADDR0, PMBUS_ADDR1 open	2.26			V
V_{ADDR_SHORT}	Voltage – shorted pin	PMBUS_ADDR0, PMBUS_ADDR1 short to ground			0.124	V
DIGITAL INPUTS AND OUTPUTS						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA(2), V_{33DIO} = 3 V			Dgnd + 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –6 mA(3), V_{33DIO} = 3 V	V_{33DIO} – 0.6			V
V_{IH}	High-level input voltage	V_{33DIO} = 3 V	2.1		3.6	V
V_{IL}	Low-level input voltage	V_{33DIO} = 3.5 V			1.4	V
MARGINING OUTPUTS						
T_{PWM_FREQ}	MARGINING-PWM frequency	FPWM1-8	15.260		125000	kHz
		PWM3-4	0.001		7800	
$DUTY_{PWM}$	MARGINING-PWM duty cycle range		0%		100%	
SYSTEM PERFORMANCE						
V_{DD}Slew	Minimum V_{DD} slew rate	V_{DD} slew rate between 2.3 V and 2.9 V	0.25			V/ms
V_{RESET}	Supply voltage at which device comes out of reset	For power-on reset (POR)			2.4	V
t_{RESET}	Low-pulse duration needed at $\overline{RESET}$ pin	To reset device during normal operation	2			µS
$f_{(PCLK)}$	Internal oscillator frequency	T_A = 125°C, T_A = 25°C	240	250	260	MHz
$t_{retention}$	Retention of configuration parameters	T_J = 25°C	100			Years
Write_Cycles	Number of nonvolatile erase/write cycles	T_J = 25°C	20			K cycles

(1) Typical supply current values are based on device programmed but not configured, and no peripherals connected to any pins.
(2) The maximum total current, I_{OL}max, for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified.
(3) The maximum total current, I_{OH}max, for all outputs combined, should not exceed 48 mA to hold the maximum voltage drop specified.

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6.6 Timing Requirements

The timing characteristics and timing diagram for the communications interface that supports I²C/SMBus, and PMBus are shown in Figure 1 and Figure 2.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Typical values at T_A = 25°C and V_{CC} = 3.3 V (unless otherwise noted)						
fSMB	SMBus/PMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		400	kHz
fI2C	I²C operating frequency	Slave mode, SCL 50% duty cycle	10		400	kHz
$t_{(BUF)}$	Bus free time between start and stop		1.3			µs
$t_{(HD:STA)}$	Hold time after (repeated) start		0.6			µs
$t_{(SU:STA)}$	Repeated start setup time		0.6			µs
$t_{(SU:STO)}$	Stop setup time		0.6			µs
$t_{(HD:DAT)}$	Data hold time	Receive mode	0			ns
$t_{(SU:DAT)}$	Data setup time		100			ns
$t_{(TIMEOUT)}$	Error signal/detect	See (1)			35	ms
$t_{(LOW)}$	Clock low period		1.3			µs
$t_{(HIGH)}$	Clock high period	See (2)	0.6			µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time	See (3)			25	ms
t_f	Clock/data fall time	Fall time t_f = 0.9 VDD to (V_{IL}max – 0.15)	20 + 0.1 Cb (4)		300	ns
t_r	Clock/data rise time	Rise time t_r = (V_{IL}max – 0.15) to (V_{IH}min + 0.15)	20 + 0.1 Cb (4)		300	ns
Cb	Total capacitance of one bus line				400	pF

(1) The device times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0] = 0).
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) Cb in picofarads (pF)

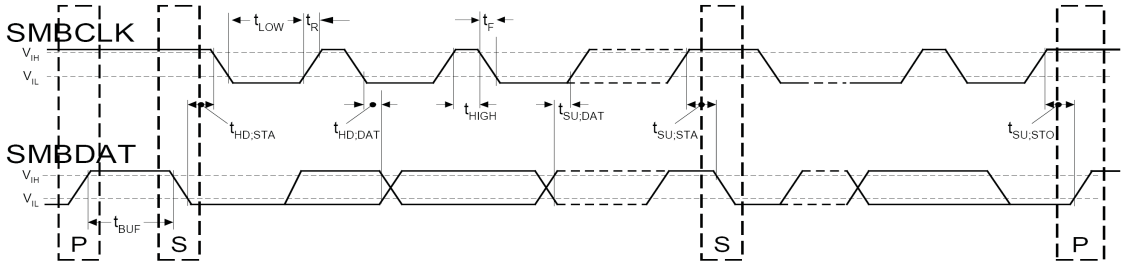


Figure 1. I²C/SMBus Timing Diagram

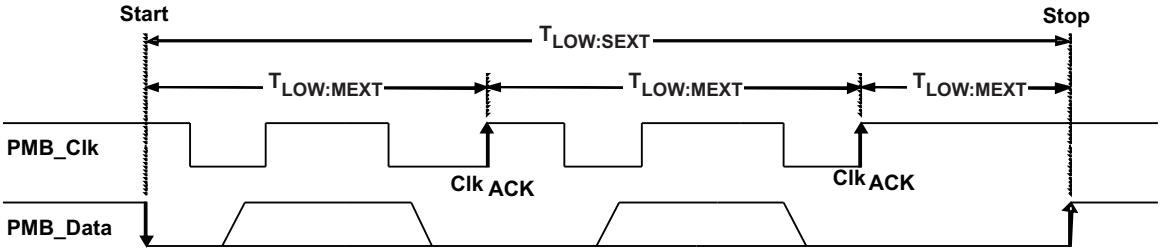


Figure 2. Bus Timing in Extended Mode

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6.7 Typical Characteristics

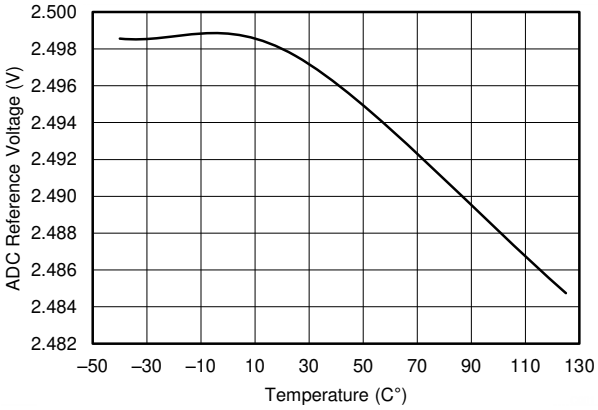


Figure 3. ADC Reference Voltage vs Temperature

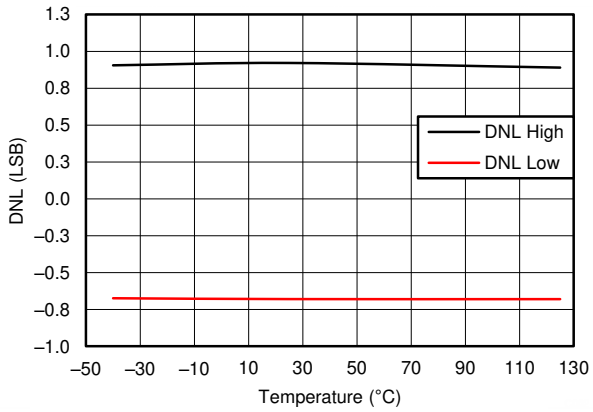


Figure 4. ADC Differential Nonlinearity vs Temperature

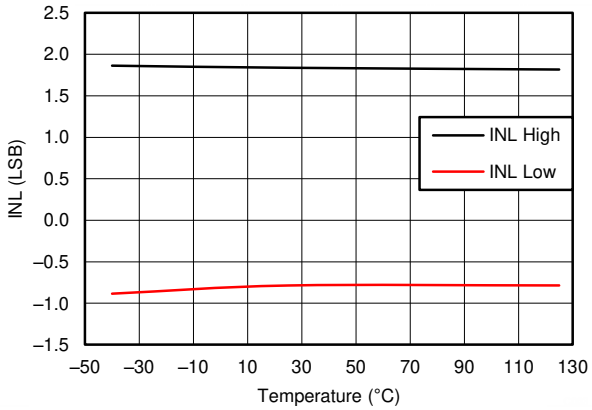


Figure 5. ADC Integral Nonlinearity vs Temperature

7 Detailed Description

7.1 Overview

Electronic systems that include CPU, DSP, microcontroller, FPGA, ASIC, etc. can have multiple voltage rails and require certain power on/off sequences in order to function correctly. The UCD90160A can control up to 16 voltage rails and ensure correct power sequences during normal condition and fault conditions.

In addition to sequencing, UCD90160A can continuously monitor rail voltages, fault conditions, and report the system health information to a PMBus host, improving systems' long term reliability.

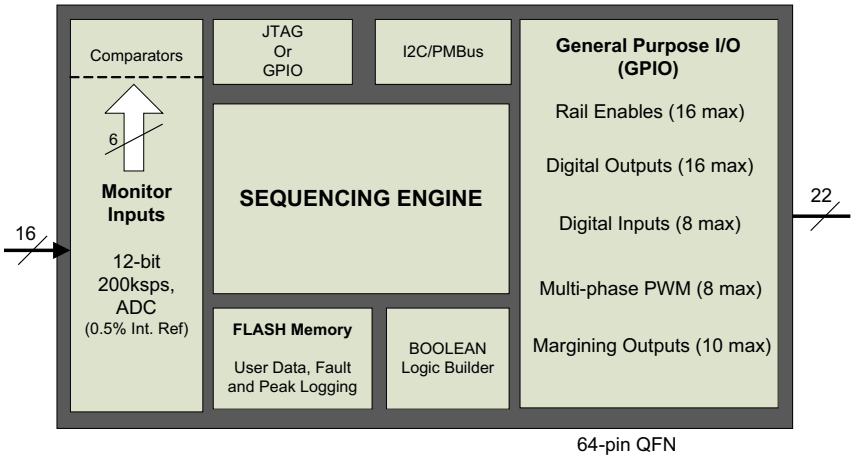
Also, UCD90160A can protect electronic systems by responding to power system faults. The fault responses are conveniently configured with *Fusion Digital Power Designer* software. Fault events are stored in on-chip nonvolatile flash memory with time stamp in order to assist failure analysis.

System reliability can be improved through four-corner testing during system verification. During four-corner testing, each voltage rail is required to operate at the minimum and maximum output voltages, commonly known as margining. UCD90160A can perform closed-loop margining for up to 10 voltage rails. During normal operation, UCD90160A can also actively trim DC output voltages using the same margining circuitry.

UCD90160A supports both PMBus- and pin-based control environments. UCD90160A functions as a PMBus slave. It can communicate with PMBus host with PMBus commands, and control voltage rails accordingly. Also, UCD90160A can be controlled by up to 8 GPIO configured GPI pins. One GPI can be used as fault pin which can shut down rails. The GPIs can be used as Boolean logic input to control up to 16 Logic GPO outputs. Each Logic GPO has a flexible Boolean logic builder. Input signals of the Boolean logic builder can include GPIs, other Logic GPO outputs, and selectable system flags such as POWER_GOOD, faults, warnings, etc. A simple state machine is also available for each Logic GPO pin.

UCD90160A provides additional features such a scascading, pin-selected states, system watchdog, system reset, runtime clock, peak value log, reset counter, and so on. Pin-selected states feature allows users to use up to 3 GPIs to define up to 8 rail states. These states can implement system low-power modes as set out in the Advanced Configuration and Power Interface (ACPI) specification.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Rail Configuration

A rail includes voltage, a power supply enable and a margining output. At least one must be included in a rail definition. Once the user has defined how the power supply rails should operate in a particular system, analog input pins and GPIOs can be selected to monitor and enable each supply (Figure 6).

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Feature Description (continued)

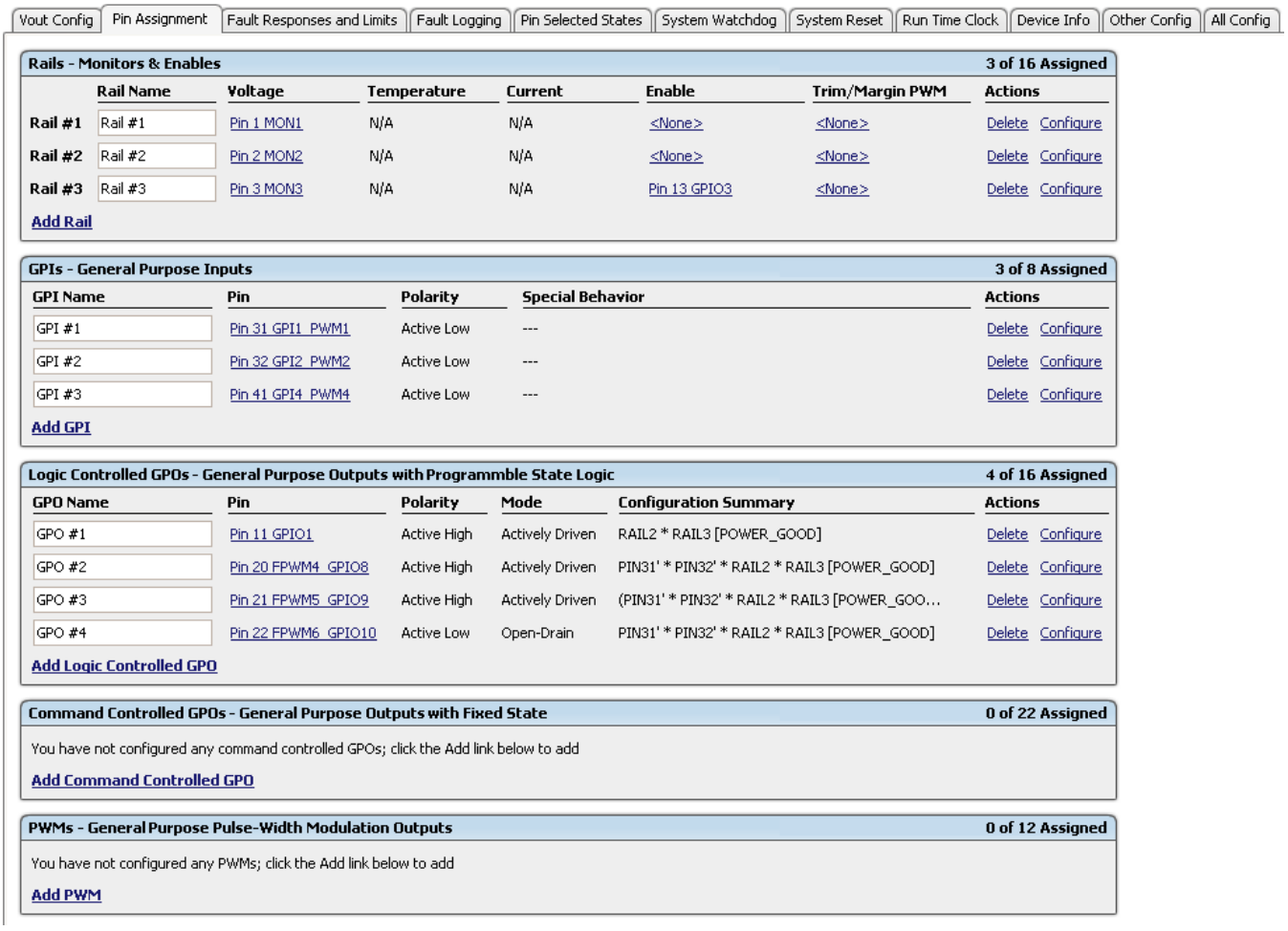


Figure 6. *Fusion Digital Power Designer* Software Pin-Assignment Tab

After the pins have been configured, other key monitoring and sequencing criteria are selected for each rail from the Vout Config tab (Figure 7):

- Nominal operating voltage (V_{OUT})
- Undervoltage (UV) and overvoltage (OV) warning and fault limits
- Margin-low and margin-high values
- Power-good on and power-good off limits
- PMBus or pin-based sequencing control (On/Off Config)
- Rails, GPOs and GPIs for Sequence On dependencies
- Rails, GPOs and GPIs for Sequence Off dependencies
- Turn-on and turn-off delay timing
- Maximum time allowed for a rail to reach POWER_GOOD_ON or POWER_GOOD_OFF after being enabled or disabled
- Other rails to turn off in case of a fault on a rail (fault-shutdown slaves)

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Feature Description (continued)

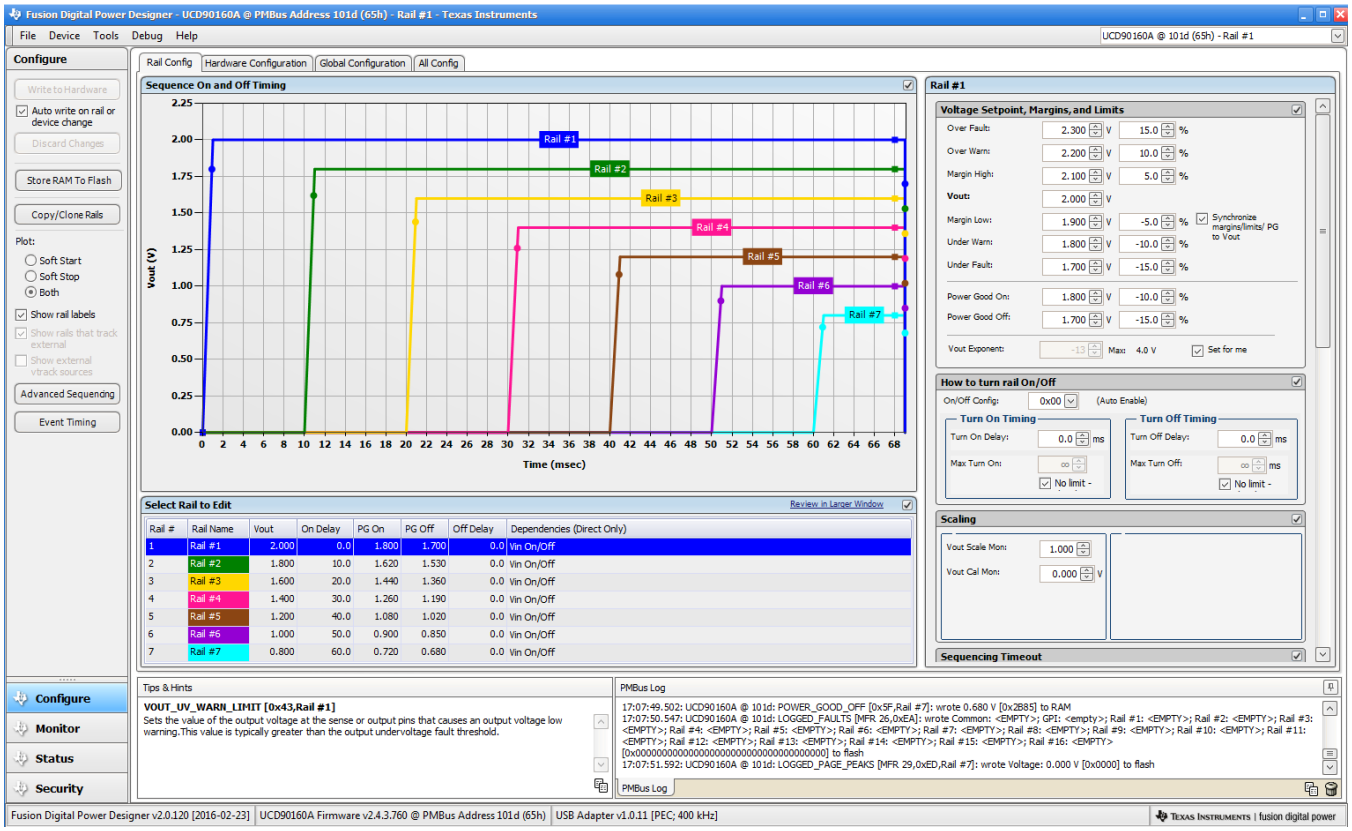


Figure 7. *Fusion Digital Power Designer* Software V_{OUT}-Config Tab

Use the *Synchronize margins/limits/PG to Vout* checkbox to change the nominal operating voltage of a rail and also update all of the other limits associated with that rail according to the percentages shown to the right of each entry.

The plot in the upper left section of Figure 7 shows a simulation of the overall sequence-on and sequence-off configuration, including the nominal voltage, the turnon and turnoff delay times, the power-good on and power-good off voltages and any timing dependencies between the rails.

After a rail voltage has reached its POWER_GOOD_ON voltage and is considered to be in regulation, it is compared against two UV and two OV thresholds in order to determine if a warning or fault limit has been exceeded. If a fault is detected, the UCD90160A responds based on a variety of flexible, user-configured options. Faults can cause rails to restart, shut down immediately, sequence off using turnoff delay times or shut down a group of rails and sequence them back on. Different types of faults can result in different responses.

Fault responses, along with a number of other parameters including user-specific manufacturing information and external scaling and offset values, are selected in the different tabs within the Configure function of the *Fusion Digital Power Designer* software. Once the configuration satisfies the user requirements, it can be written to device SRAM if *Fusion Digital Power Designer* software is connected to a UCD90160A device using an I^2C or PMBus interface. SRAM contents are stored to data flash memory so that the configuration remains in the device after a reset or power cycle.

The *Fusion Digital Power Designer* software Monitor page has a number of options, including a device dashboard and a system dashboard, for viewing and controlling device and system status.

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Feature Description (continued)

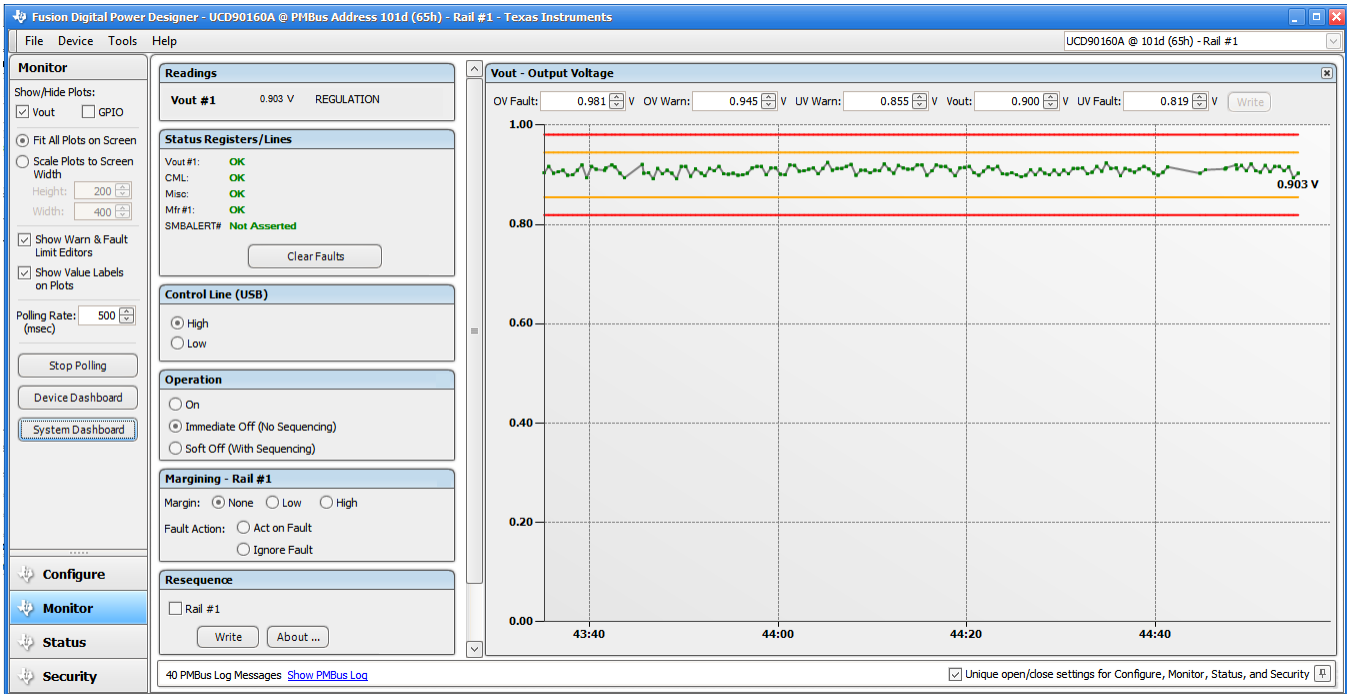


Figure 8. *Fusion Digital Power Designer* Software Monitor Page

The UCD90160A also has rail state for each rail to debug the system.

Table 1. Rail State

RAIL STATE	VALUE	DESCRIPTION
IDLE	1	On condition is not met, or rail is shut down due to fault, or rail is waiting for the resequence
SEQ_ON	2	Wait the dependency to be met to assert ENABLE signal
START_DELAY	3	TON_DELAY to assert ENABLE signal
RAMP_UP	4	Enable is asserted and rail is on the way to reach power good threshold. If the power good threshold is set to 0 V, the rail stays at this state even if the monitored voltage is bigger than 0 V.
REGULATION	5	Once the monitoring voltage is over POWER_GOOD when enable signal is asserted, rails stay at this state even if the voltage is below POWER_GOOD late as long as there is no fault action taken.
SEQ_OFF	6	Wait the dependency to be met to de-assert ENABLE signal
STOP_DELAY	7	TOFF_DELAY to de-assert ENABLE signal
RAMP_DOWN	8	Enable signal is de-asserted and rail is ramping down. This state is only available if TOFF_MAX_WARN_LIMIT is not set to unlimited; or If the turn off is triggered by a fault action, rail must not be under fault retry to show RAMP DOWN state. Otherwise, IDLE state is present.

The UCD90160A also has status registers for each rail and the capability to log faults to flash memory for use in system troubleshooting. This is helpful in the event of a power supply or system failure. The status registers (Figure 9) and the fault log (Figure 10) are available in the *Fusion Digital Power Designer* software. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* (SLVU352) and the PMBus Specification for detailed descriptions of each status register and supported PMBus commands.

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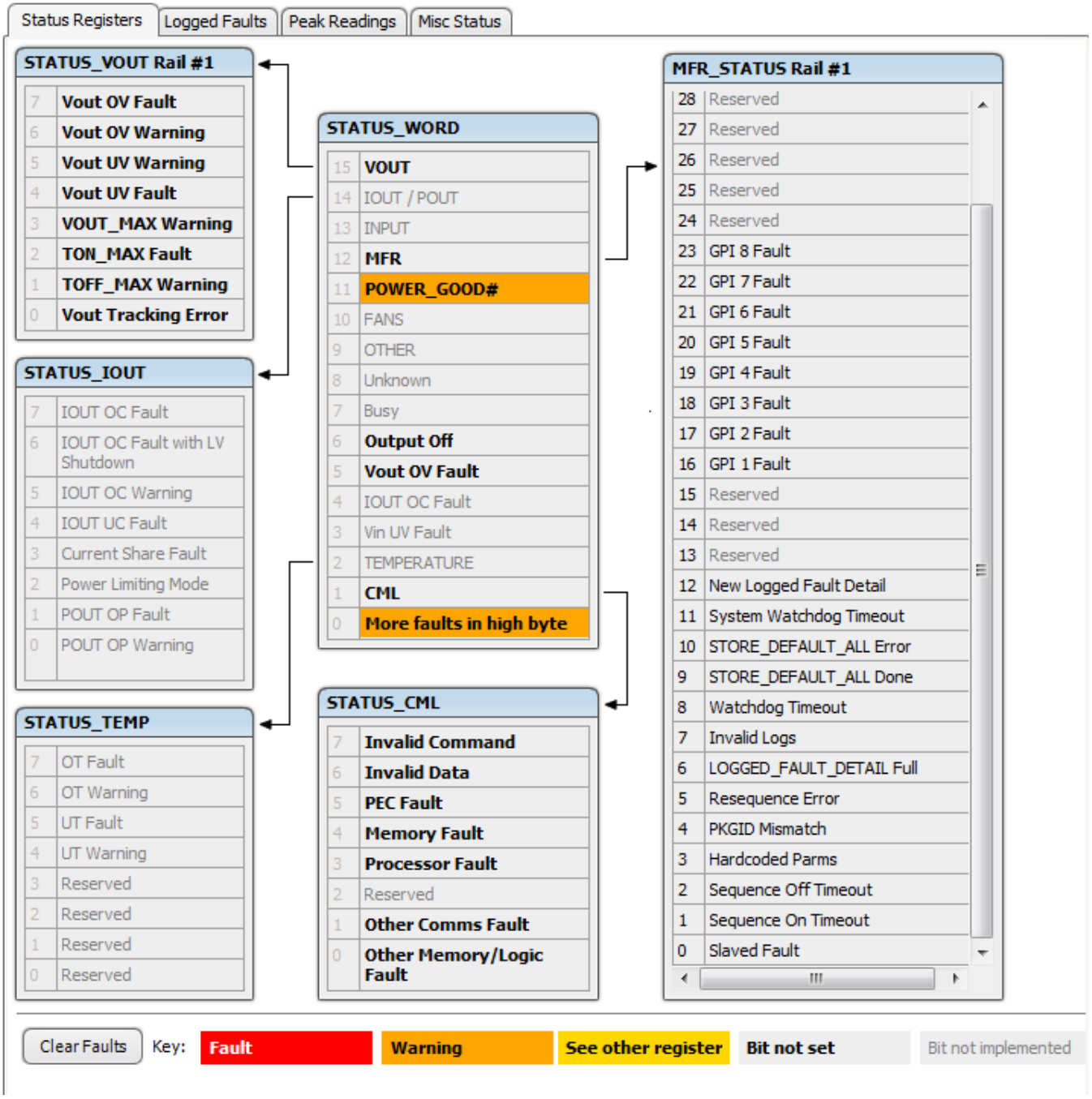


Figure 9. Fusion GUI Rail-Status Register

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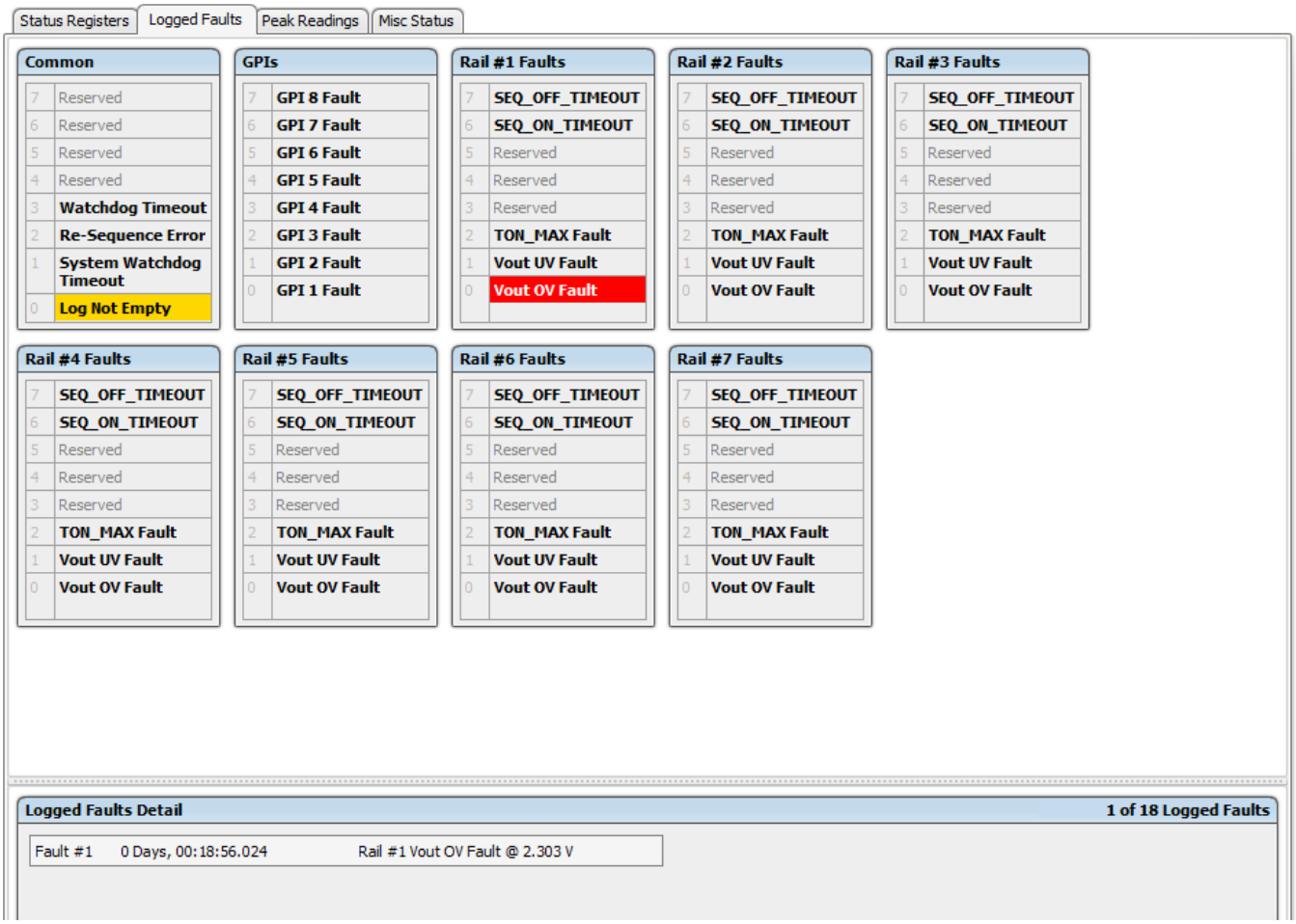


Figure 10. Fusion GUI Flash-Error Log (Logged Faults)

7.3.2 TI Fusion GUI

The Texas Instruments *Fusion Digital Power Designer* is provided for device configuration. This PC-based graphical user interface (GUI) offers an intuitive I^2C/PMBus interface to the device. It allows the design engineer to configure the system operating parameters for the application without directly using PMBus commands, store the configuration to on-chip nonvolatile memory, and observe system status (voltage, etc). *Fusion Digital Power Designer* is referenced throughout the data sheet as *Fusion Digital Power Designer* software and many sections include screen shots. The *Fusion Digital Power Designer* software can be downloaded from www.ti.com.

7.3.3 PMBus Interface

The PMBus is a serial interface specifically designed to support power management. It is based on the SMBus interface that is built on the I^2C physical specification. The UCD90160A supports revision 1.1 of the PMBus standard. Wherever possible, standard PMBus commands are used to support the function of the device. For unique features of the UCD90160A, MFR_SPECIFIC commands are defined to configure or activate those features. These commands are defined in the UCD90xxx Sequencer and System Health Controller PMBUS Command Reference (SLVU352). The most current UCD90xxx PMBus Command Reference can be found within the TI Fusion Digital Power Designer software via the Help Menu (Help, Documentation & Help Center, Sequencers tab, Documentation section).

This document makes frequent mention of the PMBus specification. Specifically, this document is *PMBus Power System Management Protocol Specification Part II – Command Language*, Revision 1.1, dated 5 February 2007. The specification is published by the Power Management Bus Implementers Forum and is available from www.pmbus.org.

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The UCD90160A is PMBus compliant, in accordance with the *Compliance* section of the PMBus specification. The firmware is also compliant with the SMBus 1.1 specification, including support for the SMBus ALERT function. The hardware can support either 100-kHz or 400-kHz PMBus operation.

7.4 Device Functional Modes

7.4.1 Power Supply Sequencing

The UCD90160A can control the turn-on and turn-off sequencing of up to 16 voltage rails by using a GPIO to set a power supply enable pin high or low. In PMBus-based designs, the system PMBus master can initiate a sequence-on event by asserting the PMBUS_CNTRL pin or by sending the OPERATION command over the I^2C serial bus. In pin-based designs, the PMBUS_CNTRL pin can also be used to sequence-on and sequence-off.

The auto-enable setting ignores the OPERATION command and the PMBUS_CNTRL pin. Sequence-on is started at power up after any dependencies and time delays are met for each rail. A rail is considered to be on or within regulation when the measured voltage for that rail crosses the power-good on (POWER_GOOD_ON [(1)]) limit. The rail is still in regulation until the voltage drops below power-good off (POWER_GOOD_OFF). In the case that there isn't voltage monitoring set for a given rail, that rail is considered ON if it is commanded on (either by OPERATION command, PMBUS CNTRL pin, or auto-enable) and (TON_DELAY + TON_MAX_FAULT_LIMIT) time passes. Also, a rail is considered OFF if that rail is commanded OFF and (TOFF_DELAY + TOFF_MAX_WARN_LIMIT) time passes

7.4.1.1 Turn-on Sequencing

The following sequence-on options are supported for each rail:

- Monitor only – do not sequence-on
- Fixed delay time (TON_DELAY) after an OPERATION command to turn on
- Fixed delay time after assertion of the PMBUS_CNTRL pin
- Fixed time after one or a group of parent rails achieves regulation (POWER_GOOD_ON)
- Fixed time after a designated GPI has reached a user-specified state
- Fixed time after a designated GPO has reached a user-specified state
- Any combination of the previous options

The maximum TON_DELAY time is 3276 ms.

7.4.1.2 Turn-off Sequencing

The following sequence-off options are supported for each rail:

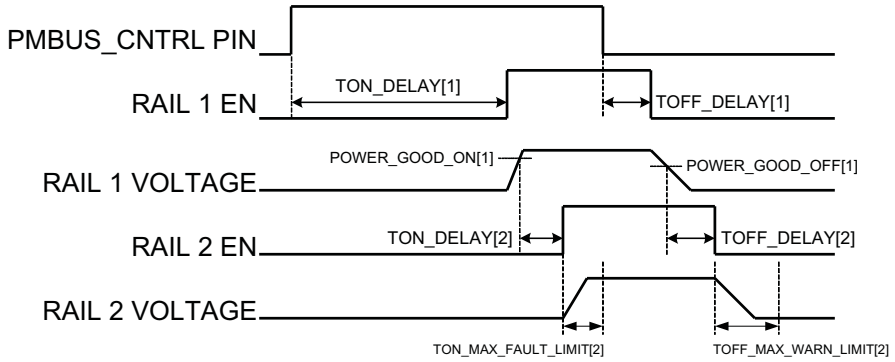
- Monitor only – do not sequence-off
- Fixed delay time (TOFF_DELAY) after an OPERATION command to turn off
- Fixed delay time after deassertion of the PMBUS_CNTRL pin
- Fixed time after one or a group of parent rails drop below regulation (POWER_GOOD_OFF)
- Fixed delay time in response to an undervoltage, overvoltage, or max turn-on fault on the rail
- Fixed delay time in response to a fault on a different rail when set as a fault shutdown slave to the faulted rail
- Fixed delay time in response to a GPI reaching a user-specified state
- Fixed time after a designated GPO has reached a user-specified state
- Any combination of the previous options

The maximum TOFF_DELAY time is 3276 ms.

(1) In this document, configuration parameters such as Power Good On are referred to using Fusion GUI names. *The UCD90xxx Sequencer and System Health Controller PMBus Command Reference* name is shown in parentheses (POWER_GOOD_ON) the first time the parameter appears.

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Device Functional Modes (continued)



- Rail 1 and Rail 2 are both sequenced “ON” and “OFF” by the PMBUS_CNTRL pin only
- Rail 2 has Rail 1 as an “ON” dependency
- Rail 1 has Rail 2 as an “OFF” dependency

Figure 11. Sequence-on and Sequence-off Timing

7.4.1.3 Sequencing Configuration Options

In addition to the turn-on and turn-off sequencing options, the time between when a rail is enabled and when the monitored rail voltage must reach its power-good-on setting can be configured using max turn-on (TON_MAX_FAULT_LIMIT). Max turn-on can be set in 1-ms increments. A value of 0 ms means that there is no limit and the device can try to turn on the output voltage indefinitely.

Rails can be configured to turn off immediately or to sequence-off according to rail and GPI dependencies, and user-defined delay times. A sequenced shutdown is configured by selecting the appropriate rail and GPI dependencies, and turn-off delay (TOFF_DELAY) times for each rail. The turn-off delay times begin when the PMBUS_CNTRL pin is deasserted, when the PMBus OPERATION command is used to give a soft-stop command, or when a fault occurs on a rail that has other rails set as fault-shutdown slaves.

Shutdowns on one rail can initiate shutdowns of other rails or controllers. In systems with multiple UCD90160As, it is possible for each controller to be both a master and a slave to another controller.

7.4.2 Pin-Selected Rail States

This feature allows with the use of up to 3 GPIs to enable and disable any rail. This is useful for implementing system low-power modes and the Advanced Configuration and Power Interface (ACPI) specification that is used for operating system directed power management in servers and PCs. In up to 8 system states, the power system designer can define which rails are on and which rails are off. If a new state is presented on the input pins, and a rail is required to change state, it does so with regard to its sequence-on or sequence-off dependencies.

The OPERATION command is modified when this function causes a rail to change its state. This means that the ON_OFF_CONFIG for a given rail must be set to use the OPERATION command for this function to have any effect on the rail state. The first three pins configured with the GPI_CONFIG command are used to select 1 of 8 system states. Whenever the device is reset, these pins are sampled and the system state, if enabled, are used to update each rail state. When selecting a new system state, changes to the status of the GPIs must not take longer than 1 microsecond. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for complete configuration settings of PIN_SELECTED_RAIL_STATES.

Table 2. GPI Selection of System States

GPI 2 State	GPI 1 State	GPI 0 State	System State
NOT Asserted	**Not** Asserted	**Not** Asserted	0
NOT Asserted	**Not** Asserted	Asserted	1
NOT Asserted	Asserted	**Not** Asserted	2
NOT Asserted	Asserted	Asserted	3
Asserted	**Not** Asserted	**Not** Asserted	4
Asserted	**Not** Asserted	Asserted	5

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Table 2. GPI Selection of System States (continued)

GPI 2 State	GPI 1 State	GPI 0 State	System State
Asserted	Asserted	**Not** Asserted	6
Asserted	Asserted	Asserted	7

7.4.3 Voltage Monitoring

Up to 16 voltages can be monitored using the analog input pins. The input voltage range is 0 to 2.5 V for MON pins 1-6, 55-59, 62, and 63. Pins 50, 52, and 54 can measure down to 0.2 V.

The ADC operates continuously, requiring 3.89 µs to convert a single analog input. Each rail is sampled by the sequencing and monitoring algorithm every 400 µs. The maximum source impedance of any sampled voltage should be less than 4 kΩ. The source impedance limit is particularly important when a resistor-divider network is used to lower the voltage applied to the analog input pins.

MON1 - MON6 can be configured using digital hardware comparators, which can be used to achieve faster fault responses. Each hardware comparator has four thresholds (two UV (Fault and Warning) and two OV (Fault and Warning)). The hardware comparators respond to UV or OV conditions in about 80 µs (faster than 400 µs for the ADC inputs) and can be used to disable rails or assert GPOs. The only fault response available for the hardware comparators is to shut down immediately.

An internal 2.5-V reference is used by the ADC. The ADC reference has a tolerance of ±0.5% between 0°C and 125°C and a tolerance of ±1% between –40°C and 125°C. An external voltage divider is required for monitoring voltages higher than 2.5 V. The nominal rail voltage and the external scale factor can be entered into the *Fusion Digital Power Designer* software and are used to report the actual voltage being monitored instead of the ADC input voltage. The nominal voltage is used to set the range and precision of the reported voltage according to Table 3.

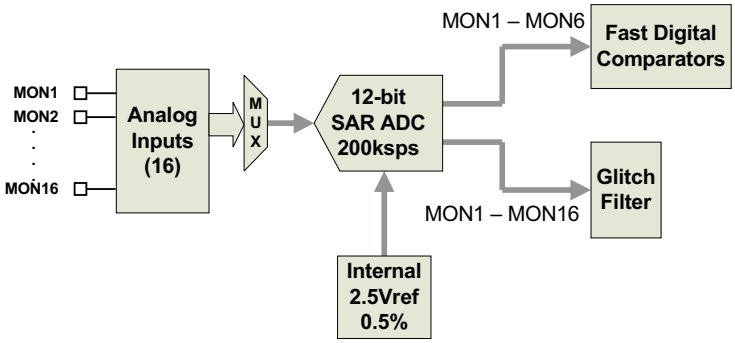


Figure 12. Voltage Monitoring Block Diagram

Table 3. Voltage Range and Resolution

VOLTAGE RANGE (V)	RESOLUTION (mV)
0 to 127.99609	3.90625
0 to 63.99805	1.95313
0 to 31.99902	0.97656
0 to 15.99951	0.48824
0 to 7.99976	0.24414
0 to 3.99988	0.12207
0 to 1.99994	0.06104
0 to 0.99997	0.03052

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Although the monitor results can be reported with a resolution of about 15 μV, the real conversion resolution of 610 μV is fixed by the 2.5-V reference and the 12-bit ADC.

7.4.4 Fault Responses and Alert Processing

The UCD90160A monitors whether the rail stays within a window of normal operation. There are two programmable warning levels (under and over) and two programmable fault levels (under and over). When any monitored voltage goes outside of the warning or fault window, the PMBALERT# pin is asserted immediately, and the appropriate bits are set in the PMBus status registers (see Figure 9). Detailed descriptions of the status registers are provided in the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* and the *PMBus Specification.*

A programmable glitch filter can be enabled or disabled for each MON input. A glitch filter for an input defined as a voltage can be set between 0 and 102 ms with 400-μs resolution. The glitch filter only applies to fault responses; a fault condition that is filtered by the glitch filter will still be recorded in the fault log.

Fault-response decisions are based on results from the 12-bit ADC. The device cycles through the ADC results and compares them against the programmed limits. The time to respond to an individual event is determined by when the event occurs within the ADC conversion cycle and the selected fault response.

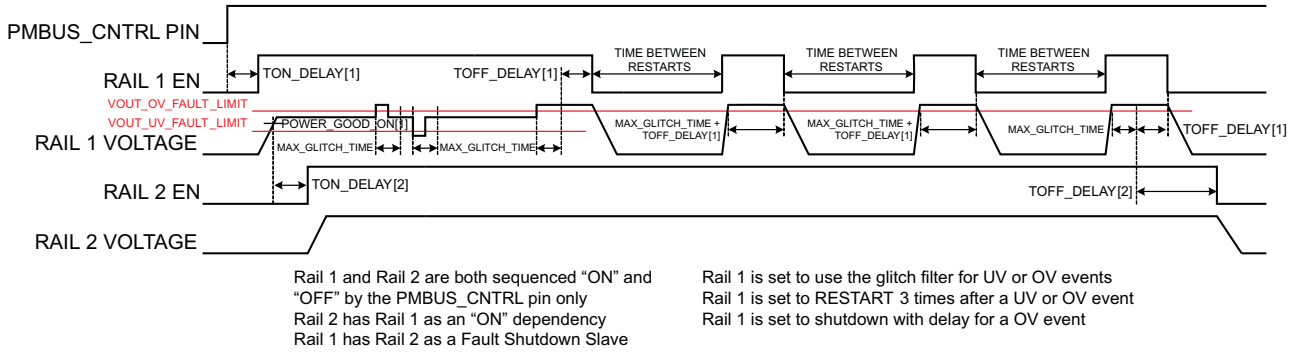


Figure 13. Sequencing and Fault-Response Timing

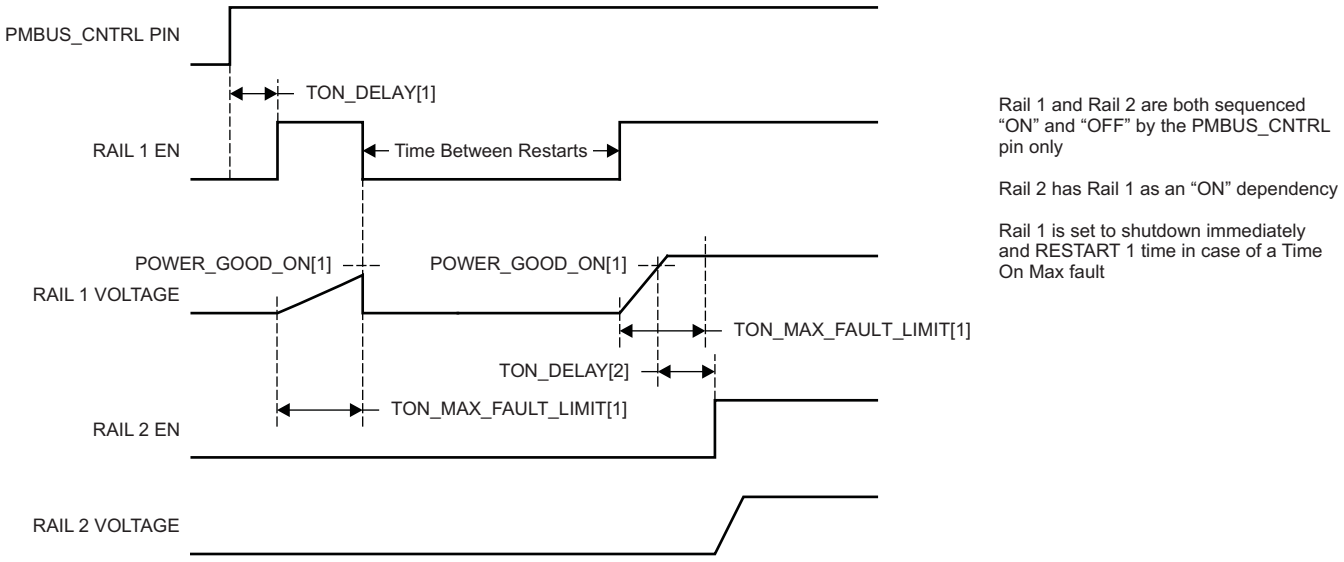


Figure 14. Maximum Turn-on Fault

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The configurable fault limits are:

- **TON_MAX_FAULT** – Flagged if a rail that is enabled does not reach the POWER_GOOD_ON limit within the configured time
- **VOUT_UV_WARN** – Flagged if a voltage rail drops below the specified UV warning limit after reaching the POWER_GOOD_ON setting
- **VOUT_UV_FAULT** – Flagged if a rail drops below the specified UV fault limit after reaching the POWER_GOOD_ON setting
- **VOUT_OV_WARN** – Flagged if a rail exceeds the specified OV warning limit at any time during startup or operation
- **VOUT_OV_FAULT** – Flagged if a rail exceeds the specified OV fault limit at any time during startup or operation
- **TOFF_MAX_WARN** – Flagged if a rail that is commanded to shut down does not reach 12.5% of the nominal rail voltage within the configured time

Faults are more serious than warnings. The PMBALERT# pin is always asserted immediately if a warning or fault occurs. If a warning occurs, the following takes place:

Warning Actions

- Immediately assert the PMBALERT# pin
- Status bit is flagged
- Assert a GPIO pin (optional)
- Warnings are not logged to flash

A number of fault response options can be chosen from:

Fault Responses

- *Continue Without Interruption:* Flag the fault and take no action
- *Shut Down Immediately:* Shut down the faulted rail immediately
- *Shut Down using TOFF_DELAY:* If a fault occurs on a rail, schedule the shutdown of this rail and all fault-shutdown slaves. All selected rails, including the faulty rail, are sequenced off according to their sequence-off dependencies and T_OFF_DELAY times.

Restart

- *Do Not Restart:* Do not attempt to restart a faulted rail after it has been shut down.
- *Restart Up To N Times:* Attempt to restart a faulted rail up to 14 times after it has been shut down. The time between restarts is measured between when the rail enable pin is deasserted (after any glitch filtering and turn-off delay times, if configured to observe them) and then reasserted. It can be set between 0 and 1275 ms in 5-ms increments. Under voltage faults only have a maximum of 1 restart as an option.
- *Restart Continuously:* Same as *Restart Up To N Times* except that the device continues to restart until the fault goes away, it is commanded off by the specified combination of PMBus OPERATION command and PMBUS_CNTRL pin status, the device is reset, or power is removed from the device. This option is not available for under voltage faults.
- *Shut Down Rails and Sequence On (Re-sequence):* Shut down selected rails immediately or after continue-operation time is reached and then sequence-on those rails using sequence-on dependencies and T_ON_DELAY times.

One GPI pin can also trigger faults if the GPI Fault Enable checkbox in Figure 19 is checked and proper responses are set in Figure 20. Refer to *GPI Special Functions* for more details.

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7.4.5 Shut Down All Rails and Sequence On (Resequence)

In response to a fault, or a RESEQUENCE command, the UCD90160A can be configured to turn off a set of rails and then sequence them back on. To sequence all rails in the system, then all rails must be selected as fault-shutdown slaves of the faulted rail. The rails designated as fault-shutdown slaves initiate soft shutdowns regardless of whether the faulted rail is set to stop immediately or stop with delay. Shut-down-all-rails and sequence-on are not performed until retries are exhausted for a given fault.

While waiting for the rails to turn off, an error is reported if any of the rails reaches its *TOFF_MAX_WARN_LIMIT*. There is a configurable option to continue with the resequencing operation if this occurs. After the faulted rail and fault-shutdown slaves sequence-off, the UCD90160A waits for a programmable delay time between 0 and 1275 ms in increments of 5 ms and then sequences-on the faulted rail and fault-shutdown slaves according to the start-up sequence configuration. This is repeated until the faulted rail and fault-shutdown slaves successfully achieve regulation or for a user-selected 1, 2, 3, or 4 times. If the resequence operation is successful, the resequence counter is reset if all of the rails that were resequenced maintain normal operation for one second.

Once shut-down-all-rails and sequence-on begin, any faults on the fault-shutdown slave rails are ignored. If there are two or more simultaneous faults with different fault-shutdown slaves, the more conservative action is taken. For example, if a set of rails is already on its second resequence and the device is configured to resequence three times, and another set of rails enters the resequence state, that second set of rails is only resequenced once. Another example – if one set of rails is waiting for all of its rails to shut down so that it can resequence, and another set of rails enters the resequence state, the device now waits for all rails from both sets to shut down before resequencing.

If any rails at resequence state are caused by a GPI fault response, the whole resequence is suspended until the GPI fault is clear.

7.4.6 GPIOs

The UCD90160A has 22 GPIO pins that can function as either inputs or outputs. Each GPIO has configurable output mode options including open-drain or push-pull outputs that can be actively driven to 3.3 V or ground. There are an additional four pins that can be used as either inputs or PWM outputs but not as GPOs. Table 4 lists possible uses for the GPIO pins and the maximum number of each type for each use. GPIO pins can be dependents in sequencing and alarm processing. They can also be used for system-level functions such as external interrupts, power-goods, resets, or for the cascading of multiple devices. GPOs can be sequenced up or down by configuring a rail without a MON pin but with a GPIO set as an enable.

Table 4. GPIO Pin Configuration Options

PIN NAME	PIN	RAIL EN (16 MAX)	GPI (8 MAX)	GPO (16 MAX)	PWM OUT (12 MAX)	MARGIN PWM (10 MAX)
FPWM1/GPIO5	17	X	X	X	X	X
FPWM2/GPIO6	18	X	X	X	X	X
FPWM3/GPIO7	19	X	X	X	X	X
FPWM4/GPIO8	20	X	X	X	X	X
FPWM5/GPIO9	21	X	X	X	X	X
FPWM6/GPIO10	22	X	X	X	X	X
FPWM7/GPIO11	23	X	X	X	X	X
FPWM8/GPIO12	24	X	X	X	X	X
GPI1/PWM1	31		X		X	
GPI2/PWM2	32		X		X	
GPI3/PWM3	42		X		X	X
GPI4/PWM4	41		X		X	X
GPIO1	11	X	X	X		
GPIO2	12	X	X	X		
GPIO3	13	X	X	X		
GPIO4	14	X	X	X		
GPIO13	25	X	X	X		
GPIO14	29	X	X	X		
GPIO15	30	X	X	X		

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Table 4. GPIO Pin Configuration Options (continued)

PIN NAME	PIN	RAIL EN (16 MAX)	GPI (8 MAX)	GPO (16 MAX)	PWM OUT (12 MAX)	MARGIN PWM (10 MAX)
GPIO16	33	X	X	X		
GPIO17	34	X	X	X		
GPIO18	35	X	X	X		
TCK/GPIO19	36	X	X	X		
TDO/GPIO20	37	X	X	X		
TDI/GPIO21	38	X	X	X		
TMS/GPIO22	39	X	X	X		

7.4.7 GPO Control

The GPIOs when configured as outputs can be controlled by PMBus commands or through logic defined in internal Boolean function blocks. Controlling GPOs by PMBus commands (GPIO_SELECT and GPIO_CONFIG) can be used to have control over LEDs, enable switches, etc. with the use of an I2C interface. See the UCD90xxx Sequencer and System Health Controller PMBus Command Reference for details on controlling a GPO using PMBus commands.

7.4.8 GPO Dependencies

GPIOs can be configured as outputs that are based on Boolean combinations of up to two ANDs, all ORed together (Figure 15). Inputs to the logic blocks can include the first 8 defined GPOs, GPIs and rail-status flags. One rail status type is selectable as an input for each AND gate in a Boolean block. For a selected rail status, the status flags of all active rails can be included as inputs to the AND gate. *_LATCH* rail-status types stay asserted until cleared by a MFR PMBus command or by a specially configured GPI pin. The different rail-status types are shown in Table 5. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for complete definitions of rail-status types. The GPO response can be configured to have a delayed assertion or deassertion. The first 8 GPOs can be chosen as Rail Sequence on/off Dependency. The logic state of the GPO instead of actual pin output is used as dependency condition.

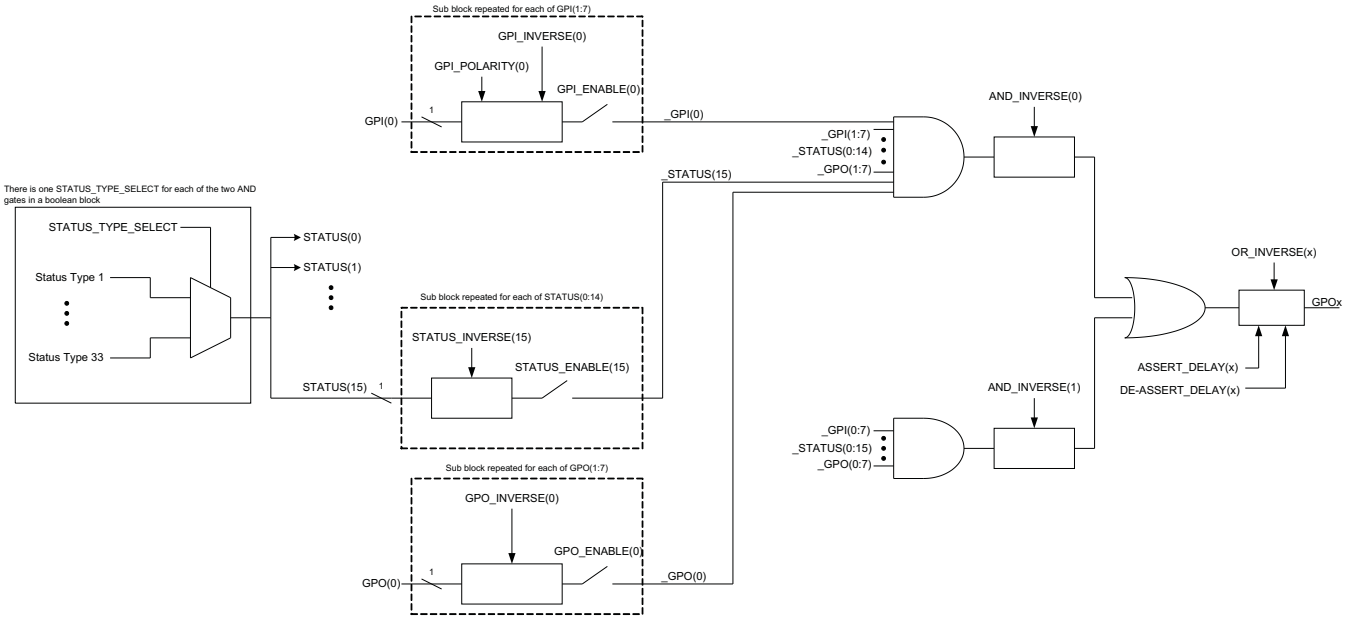


Figure 15. Boolean Logic Combinations

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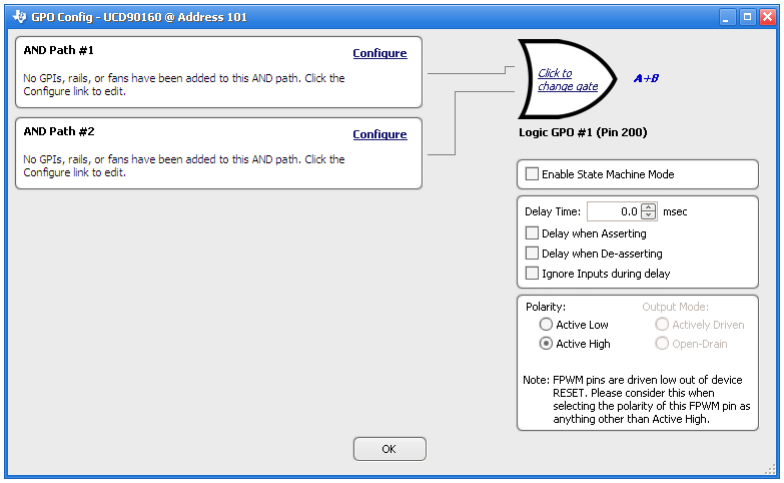


Figure 16. Fusion Boolean Logic Builder

Table 5. Rail-Status Types for Boolean Logic

Rail-Status Types		
POWER_GOOD	TON_MAX_FAULT	VOUT_UV_WARN_LATCH
MARGIN_EN	TOFF_MAX_WARN	VOUT_UV_FAULT_LATCH
MRG_LOW_nHIGH	SEQ_ON_TIMEOUT	TON_MAX_FAULT_LATCH
VOUT_OV_FAULT	SEQ_OFF_TIMEOUT	TOFF_MAX_WARN_LATCH
VOUT_OV_WARN	SYSTEM_WATCHDOG_TIMEOUT	SEQ_ON_TIMEOUT_LATCH
VOUT_UV_WARN	VOUT_OV_FAULT_LATCH	SEQ_OFF_TIMEOUT_LATCH
VOUT_UV_FAULT	VOUT_OV_WARN_LATCH	SYSTEM_WATCHDOG_TIMEOUT_LATCH

When GPO is set to POWER_GOOD, this POWER_GOOD state is based on the actual voltage measurement on the monitor pins assigned to those rails. For a rail that does not have a monitor pin, or have a monitor pin but without voltage monitoring, its POWER_GOOD state is used by sequencing purpose only, and is not be used by the GPO logic evaluation.

7.4.8.1 GPO Delays

The GPOs can be configured so that they manifest a change in logic with a delay on assertion, deassertion, both or none. GPO behavior using delays have different effects depending if the logic change occurs at a faster rate than the delay. On a normal delay configuration, if the logic for a GPO changes to a state and reverts back to previous state within the time of a delay then the GPO does not manifest the change of state on the pin. In Figure 17 the GPO is set so that it follows the GPI with a 3-ms delay at assertion and also at de-assertion. When the GPI first changes to high logic state, the state is maintained for a time longer than the delay allowing the GPO to follow with appropriate logic state. The same goes for when the GPI returns to its previous low logic state. The second time that the GPI changes to a high logic state it returns to low logic state before the delay time expires. In this case the GPO does not change state. A delay configured in this manner serves as a glitch filter for the GPO.

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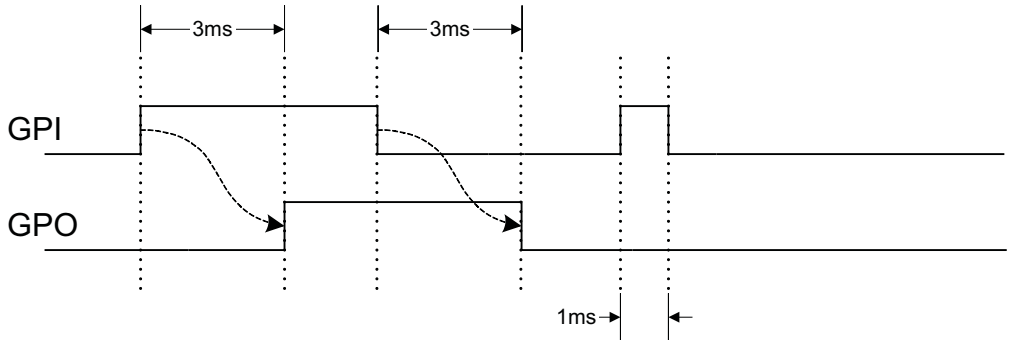


Figure 17. GPO Behavior When Not Ignoring Inputs During Delay

The *Ignore Input During Delay* bit allows to output a change in GPO even if it occurs for a time shorter than the delay. This configuration setting has the GPO ignore any activity from the triggering event until the delay expires. Figure 18 represents the two cases for when ignoring the inputs during a delay. In the case in which the logic changes occur with more time than the delay, the GPO signal looks the same as if the input was not ignored. Then on a GPI pulse shorter than the delay the GPO still changes state. Any pulse that occurs on the GPO when having the *Ignore Input During Delay* bit set has a width of at least the time delay.

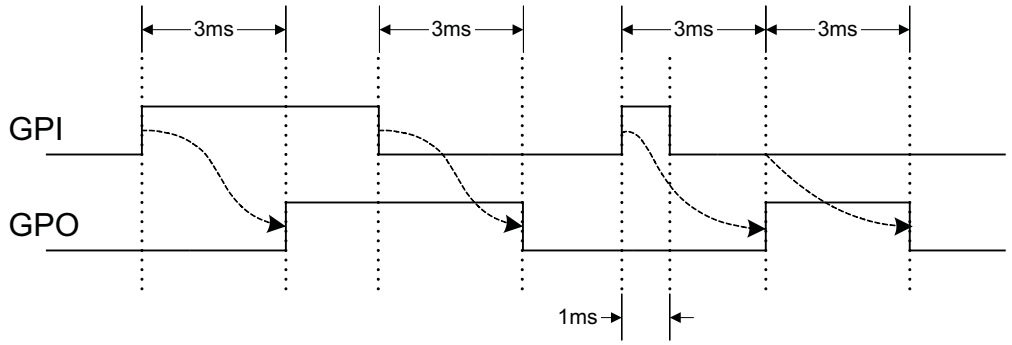


Figure 18. GPO Behavior When Ignoring Inputs During Delay

7.4.8.2 State Machine Mode Enable

When this bit within the GPO_CONFIG command is set, only one of the AND path will be used at a given time. When the GPO logic result is currently TRUE, AND path 0 will be used until the result becomes FALSE. When the GPO logic result is currently FALSE, AND path 1 will be used until the result becomes TRUE. This provides a very simple state machine and allows for more complex logical combinations.

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7.4.9 GPI Special Functions

Special input functions for which GPIs can be used. There can be no more than one pin assigned to each of these functions.

- **GPI Fault Enable** - When set, the de-assertion of the GPI is treated as a fault.
- **Latched Statuses Clear Source** - When a GPO uses a latched status type (_LATCH), a correctly configured GPI clears the latched status.
- **Input Source for Margin Enable** - When this pin is asserted, all rails with margining enabled will be put in a margined state (low or high).
- **Input Source for Margin Low/Not-High** - When this pin is asserted all margined rails will be set to Margin Low as long as the Margin Enable is asserted. When this pin is de-asserted the rails will be set to Margin High.
- **Fault Shutdown Rails** - See *Fault Shutdown Rails*.
- **Configured as Sequencing Debug Pin** - See *Configured as Sequencing Debug Pin*.
- **Configured as Fault Pin** - See *Configured as Sequencing Debug Pin*.
- **Enable Cold Boot Mode** - See *Cold Boot Mode Enable*.

The polarity of GPI pins can be configured to be either Active Low or Active High. The first 3 GPIs that are defined regardless of their main purpose will be used for the PIN_SELECTED_RAIL_STATES command.

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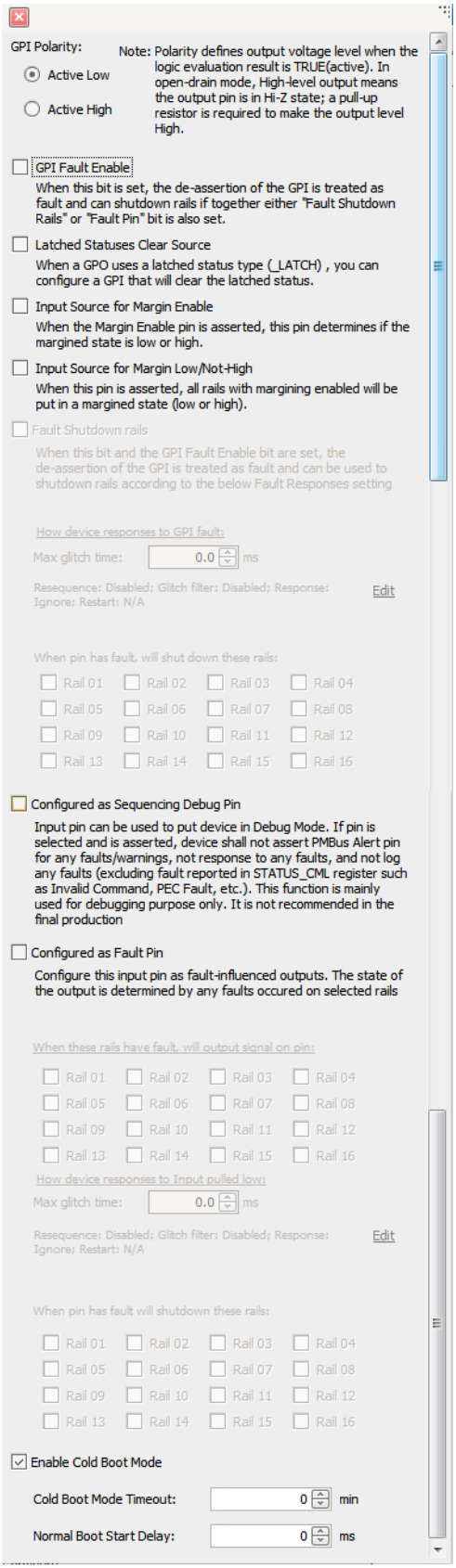


Figure 19. GPI Configurations

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7.4.9.1 Fault Shutdown Rails

GPI Fault Enable must be set to enable this feature. When set, the de-assert of the assigned GPI trigger a number of fault response options (see Figure 20). Retry action is not supported.

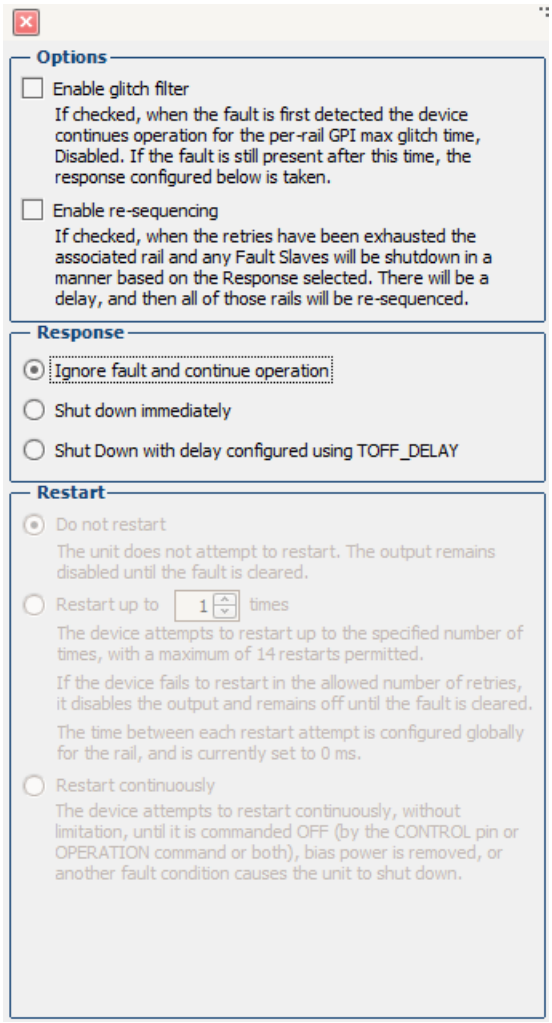


Figure 20. GPI Fault Response

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7.4.9.2 Configured as Sequencing Debug Pin

When the pin is asserted, device does not alert PMBUS_Alert pin, not response for faults, log faults defined in the Table 6. The rail sequence on/off dependency conditions are ignored, as soon as the sequence on/off timeout is expired, the rails will be sequenced on or off accordingly regardless of the timeout action, if the sequence on/off timeout value is set to 0, the rails is sequenced on or off immediately. The fault pins do not pull the fault bus low. The LGPOs affected by these events should be back to it original states.

Table 6. List of Events Affected by Debug Mode

EVENTS	DESCRIPTION
VOUT_OV_FAULT	Voltage Rail is over OV fault threshold
VOUT_OV_WARNING	Voltage Rail is over OV warning threshold
VOUT_UV_FAULT	Voltage Rail is under UV fault threshold
VOUT_UV_WARNING	Voltage Rail is under UV warning threshold
TON_MAX	Voltage Rail fails to reach power good threshold in predefined period
TOFF_MAX Warning	Voltage rail fails to reach power not good threshold in predefined period
All GPI deasserted	No logging, no fault responses, but the function of the GPI is not ignored.
SYSTEM_WATCHDOG_TIMEOUT	System watch timeout
RESEQUENCE_ERROR	Rail fails to resequence
SEQ_ON_TIMEOUT	Rail fails to meeting sequence on dependency in predefined period
SEQ_OFF_TIMEOUT	Rail fails to meeting sequence on dependency in predefined period
SLAVE_FAULT	Rail is shut down due to that its master has fault

7.4.9.3 Configured as Fault Pin

GPI Fault Enable must be set to enable this feature. When set, if there is no fault on a Fault Bus, the Fault Pin is digital input pin and listen to the Fault Bus. When one or multiple UCD90160A devices detect a rail fault (see Table 7), the corresponding Fault Pin is turned into active driven low state, pulling down the Fault Bus and informing all other UCD90160A devices of the corresponding fault. This way, a coordinated action can be taken across multiple devices. After the fault is cleared, the state of the Fault Pin is turned back to an input pin.

Table 7. Events Affecting Fault Pin

EVENTS	DESCRIPTION
RESEQUENCE_ERROR	Rail fails to resequence
SEQ_ON_TIMEOUT	Rail fails to meeting sequence on dependency in predefined period
SEQ_OFF_TIMEOUT	Rail fails to meeting sequence on dependency in predefined period
VOUT_UV_FAULT	Voltage rail is under UV threshold
VOUT_OV_FAULT	Voltage rail is over OV threshold
TON_MAX_FAULT	Voltage rail fails to reach power good threshold in predefined period.

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7.4.9.4 Cold Boot Mode Enable

Cold boot mode is used to heat-up a system by turning on cold boot rails for certain amounts of time when it is under an extreme code temperature. UCD device is communicated with the system via particular GPI (thermal state GPI) which is output from a thermal device. Cold boot mode is only entering once per UCD reset. There is no system watch dog Reset during the cold boot mode.

Device reads the thermal state GPI to determine whether it should start cold boot or not when it is out of reset. When the input of thermal state GPI is DE-ASSERTED, device enters cold boot mode and log the GPI fault if the GPI fault log enable bit is set, otherwise device enters normal mode. The following changes on the thermal state GPI do not introduce any logging. Only one GPI can be assigned for this function and one it is assigned, it cannot be used for any other GPI functions.

The rails used in the cold boot mode are configurable. For those rails with Sequence On Dependency on the thermal state GPI, they (non-cold boot rails) are not powered-up during the cold boot because the dependency is not met. But non-cold boot rails will be power-on under normal mode because thermal state GPI is treated as ASSERTED when cold boot mode is over. For those rails without sequence on dependency on the thermal state GPI, they (cold boot rails) are power-on under both cold boot and normal mode. It is application's responsibility to set the proper ON_OFF_CONFIG for those cold boot rails. Cold boot rails are not power-on if their ON_OFF_CONFIG settings are not met under cold boot mode. Cold boot mode timeout is used to tell how long the device shall stay at the cold boot before it stops monitoring the thermal state GPI and shutdown all cold boot rails with EN control. Normal Boot Start Delay is used to tell how long device should wait to ramp up the powers after all cold boot rails with EN are below POWER_GOOD_OFF.

```
- If system temperature is < threshold degree C (Thermal State GPI)
        o   Yes(DE_ASSERTED):
            § Log GPI fault
            § Start Cold Boot Timeout
            § No System Watchdog output
            § Ramp up the power supplies based on ON_OFF_CONFIG
            § Wait for thermal state GPI ASSERTED OR “Cold Boot Mode Timeout expired”
            § Disable the thermostat input listening mode
            § Force to shutdown down all cold boot rails with EN control immediately
            § Wait all cold boot rails with EN control below POWER_GOOD_OFF
            § Start and Wait “Normal boot Start Delay expired”
- Disable the thermostat input listening mode
- Treated Thermal State GPI as ASSERTED
- Ramp up power supplies based on ON_OFF_CONFIG
```

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7.4.10 Power Supply Enables

Each GPIO can be configured as a rail-enable pin with either active-low or active-high polarity. Output mode options include open-drain or push-pull outputs that can be actively driven to 3.3 V or ground. During reset, the GPIO pins are high-impedance except for FPWM/GPIO pins 17 to 24, which are driven low. External pulldown or pullup resistors can be tied to the enable pins to hold the power supplies off during reset. The UCD90160A can support a maximum of 16 enable pins.

NOTE

GPIO pins that have FPWM capability (pins 17 to 24) should only be used as power supply enable signals if the signal is active high.

7.4.11 Cascading Multiple Devices

A GPIO pin can be used to coordinate multiple controllers by using it as a power good-output from one device and connecting it to the PMBUS_CNTRL input pin of another. This imposes a master/slave relationship among multiple devices. During startup, the slave controllers initiate their start sequences after the master has completed its start sequence and all rails have reached regulation voltages. During shutdown, as soon as the master starts to sequence-off, it sends the shut-down signal to its slaves.

A shutdown on one or more of the master rails can initiate shutdowns of the slave devices. The master shutdowns can be initiated intentionally or by a fault condition. This method works to coordinate multiple controllers, but it does not enforce interdependency between rails within a single controller.

Another method to cascade multiple devices is to connect the power-good output of the first device to a MON pin of the second device; connect the power-good output of the second device to a MON pin of the third device, and so on. Optionally, connect the power-good output of the last device to a MON pin of the first device. The rails controlled by a device have dependency on the previous device's power-good output. This way, the rails controlled by multiple devices can be sequenced. Also, the de-assertion of a power-good output can trigger a UV fault of the next device. The UV fault response can be configured to shut down other rails controlled by the same device. This way, when one rail has fault shutdown, other rails controlled by other devices can be shut down accordingly.

The PMBus specification implies that the power-good signal is active when ALL the rails in a controller are regulating at their programmed voltage. The UCD90160A allows GPIOs to be configured to respond to a desired subset of power-good signals.

Multiple UCD90160A devices can also work together and coordinate when faults happen with fault pin connection. One GPI pins can be configured as Fault Pins. Fault Pin is connected to a Fault Bus. Each Fault Bus is pulled up to 3.3 V by a 10-kΩ resistor. All the UCD90160A devices on the same Fault Bus are informed of the same fault condition. An example of Fault Pin connections is shown in Figure 21.

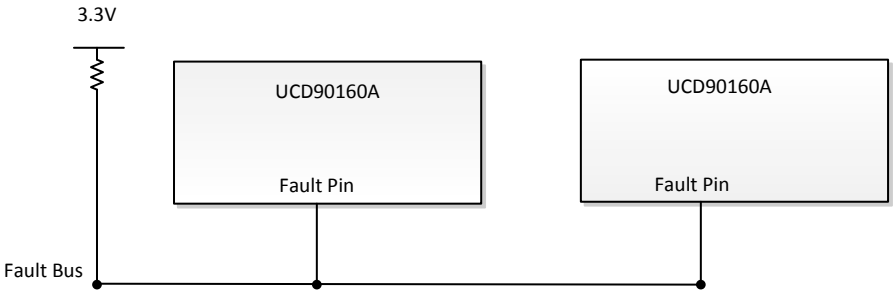


Figure 21. Fault Pin Connections

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7.4.12 PWM Outputs

7.4.12.1 FPWM1-8

Pins 17–24 can be configured as fast pulse-width modulators (FPWMs). The frequency range is 15.260 kHz to 125 MHz. FPWMs can be configured as closed-loop margining outputs, fan controllers or general-purpose PWMs.

Any FPWM pin not used as a PWM output can be configured as a GPIO. One FPWM in a pair can be used as a PWM output and the other pin can be used as a GPO. The FPWM pins are actively driven low from reset when used as GPOs.

The frequency settings for the FPWMs apply to pairs of pins:

- FPWM1 and FPWM2 – same frequency
- FPWM3 and FPWM4 – same frequency
- FPWM5 and FPWM6 – same frequency
- FPWM7 and FPWM8 – same frequency

If an FPWM pin from a pair is not used while its companion is set up to function as a PWM, it is recommended to configure the unused FPWM pin as an active-low open-drain GPO so that it does not disturb the rest of the system. By setting an FPWM, it automatically enables the other FPWM within the pair if it was not configured for any other functionality.

The frequency for the FPWM is derived by dividing down a 250MHz clock. To determine the actual frequency to which an FPWM can be set, must divide 250MHz by any integer between 2 and (2^{14}-1).

The FPWM duty cycle resolution is dependent on the frequency set for a given FPWM. Once the frequency is known the duty cycle resolution can be calculated as Equation 1.

$$\text{Change per Step } (\%)_{FPWM} = \text{frequency} \div (250 \times 10^6 \times 16) \quad (1)$$

Take for an example determining the actual frequency and the duty cycle resolution for a 75MHz target frequency.

1. Divide 250 MHz by 75 MHz to obtain 3.33.
2. Round off 3.33 to obtain an integer of 3.
3. Divide 250MHz by 3 to obtain actual closest frequency of 83.333MHz.
4. Use Equation 1 to determine duty cycle resolution to obtain 2.0833% duty cycle resolution.

7.4.12.2 PWM1-4

Pins 31, 32, 41, and 42 can be used as GPIs or PWM outputs.

If configured as PWM outputs, then limitations apply:

- PWM1 has a fixed frequency of 10 kHz
- PWM2 has a fixed frequency of 1 kHz
- PWM3 and PWM4 frequencies can be 0.93 Hz to 7.8125 MHz.

The frequency for PWM3 and PWM4 is derived by dividing down a 15.625-MHz clock. To determine the actual frequency to which these PWMs can be set, must divide 15.625 MHz by any integer between 2 and (2^{24} – 1). The duty cycle resolution will be dependent on the set frequency for PWM3 and PWM4.

The PWM3 or PWM4 duty cycle resolution is dependent on the frequency set for the given PWM. Once the frequency is known the duty cycle resolution can be calculated as Equation 2.

$$\text{Change per Step } (\%)_{PWM3/4} = \text{frequency} \div (15.625 \times 10^6) \times 100 \quad (2)$$

To determine the closest frequency to 1 MHz that PWM3 can be set to calculate as the following:

1. Divide 15.625 MHz by 1 MHz to obtain 15.625.
2. Round off 15.625 to obtain an integer of 16.
3. Divide 15.625 MHz by 16 to obtain actual closest frequency of 976.563 kHz.
4. Use Equation 2 to determine duty cycle resolution to obtain 6.25% duty cycle resolution.

All frequencies below 238 Hz will have a duty cycle resolution of 0.0015%.

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7.4.13 Programmable Multiphase PWMs

The FPWMs can be aligned with reference to their phase. The phase for each FPWM is configurable from 0° to 360°. This provides flexibility in PWM-based applications such as power supply controller, digital clock generation, and others. See an example of four FPWMs programmed to have phases at 0°, 90°, 180°, and 270° (Figure 22).

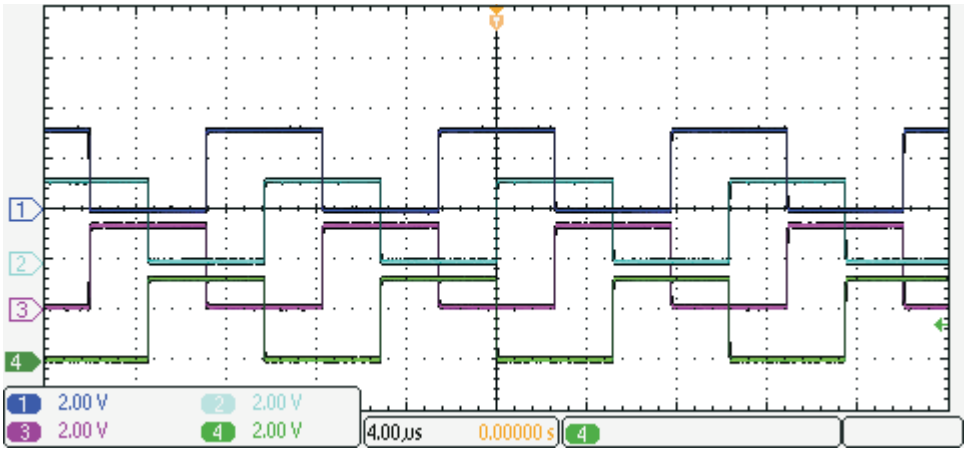


Figure 22. Multiphase PWMs

7.4.14 Margining

Margining is used in product validation testing to verify that the complete system works properly over all conditions, including minimum and maximum power supply voltages, load range, ambient temperature range, and other relevant parameter variations. Margining can be controlled over PMBus using the OPERATION command or by configuring two GPIO pins as margin-EN and margin-UP/DOWN inputs. The MARGIN_CONFIG command in the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* describes different available margining options, including ignoring faults while margining and using closed-loop margining to trim the power supply output voltage one time at power up.

7.4.14.1 Open-Loop Margining

Open-loop margining is done by connecting a power supply feedback node to ground through one resistor and to the margined power supply output (V_{OUT}) through another resistor. The power supply regulation loop responds to the change in feedback node voltage by increasing or decreasing the power supply output voltage to return the feedback voltage to the original value. The voltage change is determined by the fixed resistor values and the voltage at V_{OUT} and ground. Two GPIO pins must be configured as open-drain outputs for connecting resistors from the feedback node of each power supply to V_{OUT} or ground.

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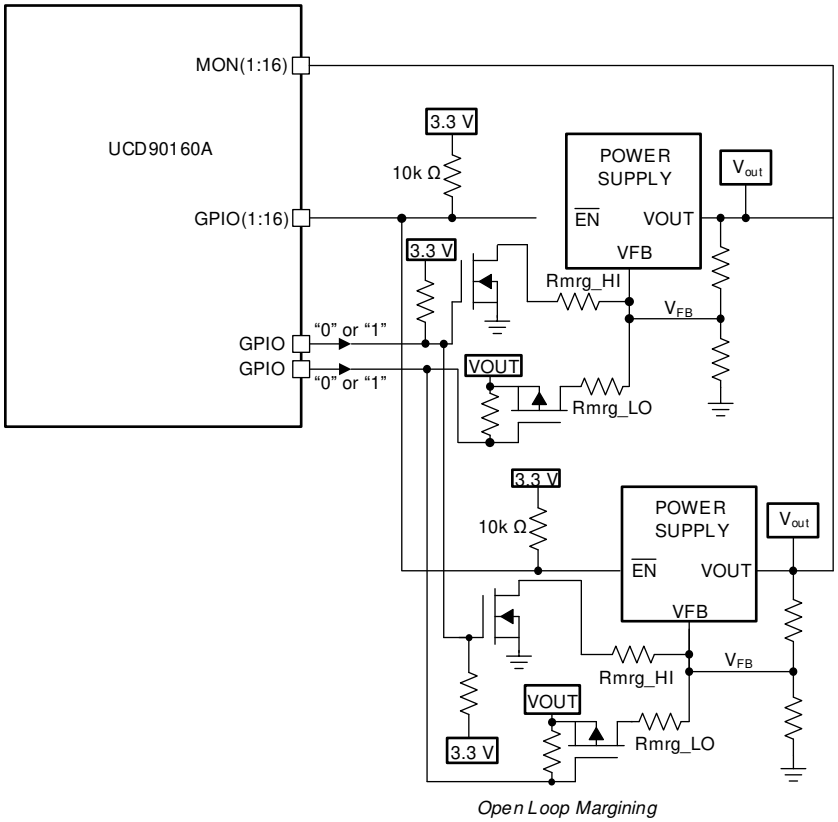


Figure 23. Open-Loop Margining

7.4.14.2 Closed-Loop Margining

Closed-loop margining uses a PWM or FPWM output for each power supply that is being margined. An external RC network converts the FPWM pulse train into a DC margining voltage. The margining voltage is connected to the appropriate power supply feedback node through a resistor. The power supply output voltage is monitored, and the margining voltage is controlled by adjusting the PWM duty cycle until the power supply output voltage reaches the margin-low and margin-high voltages set by the user. The voltage setting resolutions will be the same that applies to the voltage measurement resolution (Table 3). The closed loop margining can operate in several modes (Table 8). Given that this closed-loop system has feed back through the ADC, the closed-loop margining accuracy will be dominated by the ADC measurement. The relationship between duty cycle and margined voltage is configurable so that voltage increases when duty cycle increases or decreases. For more details on configuring the UCD90160A for margining, see the *Voltage Margining Using the UCD9012x* application note (SLVA375).

Table 8. Closed Loop Margining Modes

MODE	DESCRIPTION
DISABLE	Margining is disabled.
ENABLE_TRI_STATE	When not margining, the PWM pin is set to high impedance state.
ENABLE_ACTIVE_TRIM	When not margining, the PWM duty-cycle is continuously adjusted to keep the voltage at VOUT_COMMAND.
ENABLE_FIXED_DUTY_CYCLE	When not margining, the PWM duty-cycle is set to a fixed duty-cycle.

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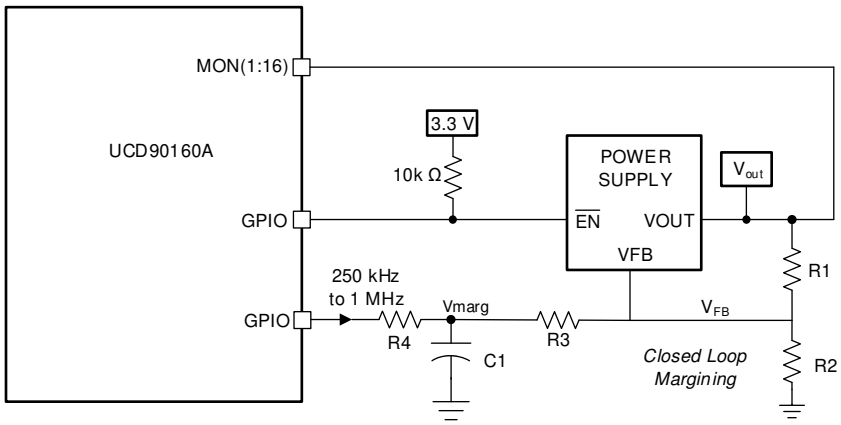


Figure 24. Closed-Loop Margining

7.4.15 System Reset Signal

The UCD90160A can generate a programmable system-reset pulse as part of sequence-on. The pulse is created by programming a GPIO to remain deasserted until the voltage of a particular rail or combination of rails reach their respective POWER_GOOD_ON levels plus a programmable delay time. The system-reset delay duration can be programmed as shown in Table 9. See an example of two SYSTEM RESET signals Figure 25. The first SYSTEM RESET signal is configured so that it de-asserts on Power Good On and it asserts on Power Good Off after a given common delay time. The second SYSTEM RESET signal is configured so that it sends a pulse after a delay time once Power Good On is achieved. The pulse width can be configured between 0.001s to 32.256s. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for pulse width configuration details.

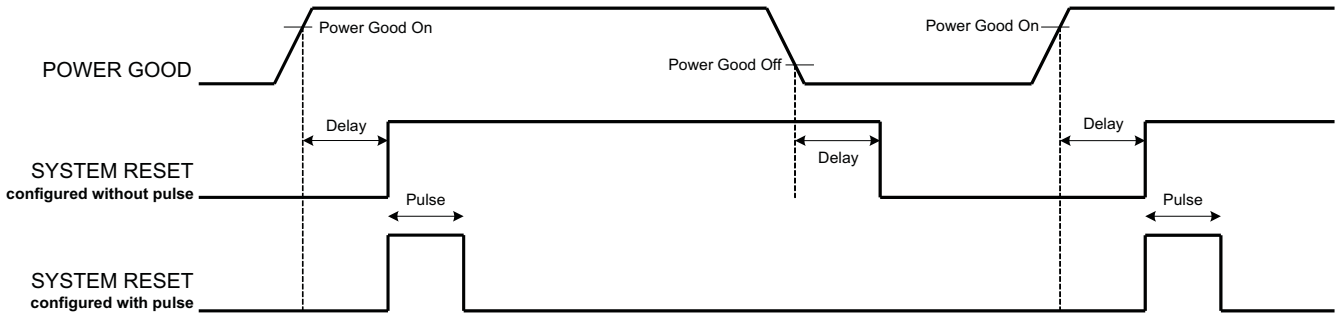


Figure 25. System Reset with and without Pulse Setting

The system reset can react to watchdog timing. In Figure 26 The first delay on SYSTEM RESET is for the initial reset release that would get a CPU running once all necessary voltage rails are in regulation. The watchdog is configured with a Start Time and a Reset Time. If these times expire without the WDI clearing them then it is expected that the CPU providing the watchdog signal is not operating. The SYSTEM RESET is toggled either using a Delay or GPI Tracking Release Delay to see if the CPU recovers.

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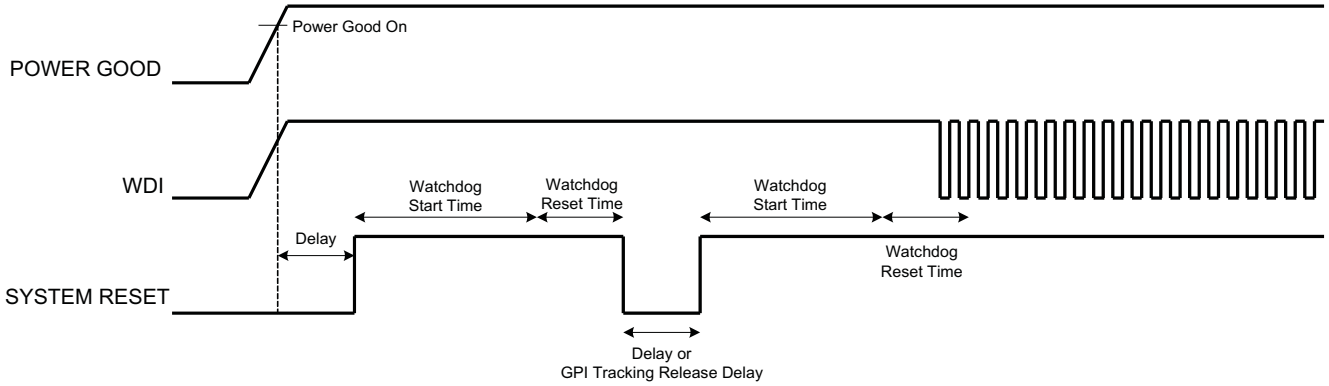


Figure 26. System Reset with Watchdog

Table 9. System-Reset Delay

DELAY
0 ms
1 ms
2 ms
4 ms
8 ms
16 ms
32 ms
64 ms
128 ms
256 ms
512 ms
1.02 s
2.05 s
4.10 s
8.19 s
16.38 s
32.8 s

7.4.16 Watch Dog Timer

A GPI and GPO can be configured as a watchdog timer (WDT). The WDT can be independent of power supply sequencing or tied to a GPIO functioning as a watchdog output (WDO) that is configured to provide a system-reset signal. The WDT can be reset by toggling a watchdog input (WDI) pin or by writing to SYSTEM_WATCHDOG_RESET over I^2C. The WDI and WDO pins are optional when using the watchdog timer. The WDI can be replaced by SYSTEM_WATCHDOG_RESET command and the WDO can be manifested through the Boolean Logic defined GPOs or through the System Reset function.

The WDT can be active immediately at power up or set to wait while the system initializes. Table 10 lists the programmable wait times before the initial timeout sequence begins.

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Table 10. WDT Initial Wait Time

WDT INITIAL WAIT TIME
0 ms
100 ms
200 ms
400 ms
800 ms
1.6 s
3.2 s
6.4 s
12.8 s
25.6 s
51.2 s
102 s
205 s
410 s
819 s
1638 s

The watchdog timeout is programmable from 0.001s to 32.256s. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for details on configuring the watchdog timeout. If the WDT times out, the UCD90160A can assert a GPIO pin configured as WDO that is separate from a GPIO defined as system-reset pin, or it can generate a system-reset pulse. After a timeout, the WDT is restarted by toggling the WDI pin or by writing to SYSTEM_WATCHDOG_RESET over I^2C.

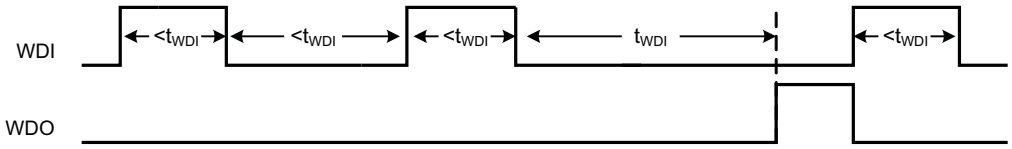


Figure 27. Timing of GPIOs Configured for Watchdog Timer Operation

7.4.17 Run Time Clock

The Run-Time clock output reports in milliseconds and days. Both values are 32-bit numbers. The value is saved in nonvolatile memory whenever a STORE_DEFAULT_ALL command is issued. It can also be saved when a power-down condition is detected (See *Brownout Function*).

The Run-Time clock may also be written. This allows the clock to be periodically corrected by the host. It also allows the clock to be initialized to the actual, absolute time in years (for example, March 23, 2010). The user must translate the absolute time to days and milliseconds.

The three usage scenarios for the Run-Time Clock are:

- **Time from restart (reset or power-on)**. Run-Time Clock starts from 0 each time a restart occurs
- **Absolute run-time, or operating time**. Run-Time Clock is preserved across restarts, recording the total time that the device has been in operation “Boot time” is not included in this period. Only normal operation time is captured here.)
- **Local time**. An external processor sets the Run-Time Clock to real-world time each time the device is restarted.

The Run-Time clock value is used to timestamp any faults that are logged.

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7.4.18 Data and Error Logging to Flash Memory

The UCD90160A can log up to 18 faults and the number of device resets to flash memory. Peak voltage measurements are also stored for each rail. To reduce stress on the flash memory, a 30-second timer is started if a measured value exceeds the previously logged value. Only the highest value from the 30-second interval is written from RAM to flash. Data and Error logging to flash memory can be disabled by user so that the data and error are only stored in the SRAM.

Multiple faults can be stored in flash memory and can be accessed over PMBus to help debug power supply bugs or failures. Each logged fault includes:

- Rail number
- Fault type
- Fault time since previous device reset
- Last measured rail voltage

The total number of device resets is also stored to flash memory. The value can be reset using PMBus.

There are three settings for handling the fault log once it reaches its maximum capacity. These settings allow to keep the latest faults by using a First In, First Out (FIFO) mode.

- FIFO log disabled - The first 18 faults will be logged. No additional faults will be logged until the fault log is cleared.
- FIFO log for all faults - The most recent 18 faults will be logged. Once 18 faults are logged, any additional faults will cause the oldest fault log entry to be lost.
- FIFO log for last half of faults - The first 9 faults will be logged. The most recent 9 faults will also be logged. In the FIFO portion of the log, once 9 faults are logged, any additional faults will cause the oldest fault entry to be lost.

With the brownout function enabled, the run-time clock value, peak monitor values, and faults are only logged to flash when a power-down is detected. The device run-time clock value is stored across resets or power cycles unless the brownout function is disabled, in which case the run-time clock is returned to zero after each reset.

It is also possible to update and calibrate the UCD90160A internal run-time clock via a PMBus host. For example, a host processor with a real-time clock could periodically update the UCD90160A run-time clock to a value that corresponds to the actual date and time. The host must translate the UCD90160A timer value back into the appropriate units, based on the usage scenario chosen. See the REAL_TIME_CLOCK command in the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for more details.

7.4.19 Brownout Function

The UCD90160A can be enabled to turn off all nonvolatile logging until a brownout event is detected. A brownout event occurs if V_{CC} drops below 2.9 V. In order to enable this feature, the user must provide enough local capacitance to deliver up to 80 mA (consider additional load based on GPOs sourcing external circuits such as LEDs) on for 5 ms while maintaining a minimum of 2.6 V at the device. If using the brownout circuit (Figure 28), then a schottky diode should be placed so that it blocks the other circuits that are also powered from the 3.3-V supply.

With this feature enabled, the UCD90160A saves faults, peaks, and other log data to SRAM during normal operation of the device. Once a brownout event is detected, all data is copied from SRAM to Flash if the log is not disabled. Use of this feature allows the UCD90160A to keep track of a single run-time clock that spans device resets or system power down (rather than resetting the run time clock after device reset). It can also improve the UCD90160A internal response time to events, because Flash writes are disabled during normal system operation. This is an optional feature and can be enabled using the MISC_CONFIG command. For more details, see the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference*.

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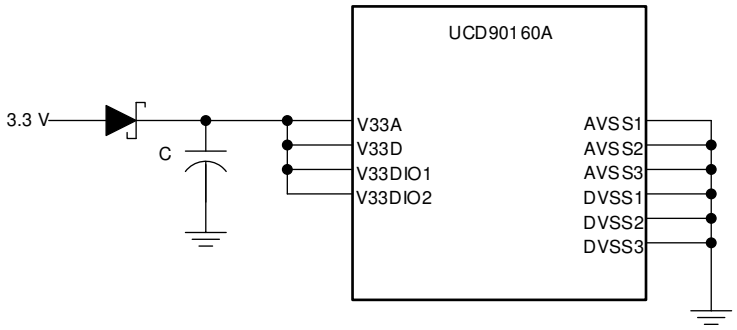


Figure 28. Brownout Circuit

7.4.20 PMBus Address Selection

Two pins are allocated to decode the PMBus address. At power up, the device applies a bias current to each address-detect pin, and the voltage on that pin is captured by the internal 12-bit ADC. The PMBus address is calculated as follows.

$$\text{PMBus Address} = 12 \times \text{bin}(V_{AD01}) + \text{bin}(V_{AD00})$$

Where $\text{bin}(V_{AD0x})$ is the address bin for one of eight addresses as shown in Table 11. The address bins are defined by the MIN and MAX VOLTAGE RANGE (V). Each bin is a constant ratio of 1.25 from the previous bin. This method maintains the width of each bin relative to the tolerance of standard 1% resistors.

Table 11. PMBus Address Bins

ADDRESS BIN	RPMBus PMBus RESISTANCE (kΩ)
open	—
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
short	—

A low impedance (short) on either address pin that produces a voltage below the minimum voltage causes the PMBus address to default to address 126 (0x7E). A high impedance (open) on either address pin that produces a voltage above the maximum voltage also causes the PMBus address to default to address 126 (0x7E).

Address 0 is not used because it is the PMBus general-call address. Addresses 11 and 127 can not be used by this device or any other device that shares the PMBus with it, because those are reserved for manufacturing programming and test. It is recommended that address 126 not be used for any devices on the PMBus, because this is the address that the UCD90160A defaults to if the address lines are shorted to ground or left open. Table 12 summarizes which PMBus addresses can be used. Other SMBus/PMBus addresses have been assigned for specific devices. For a system with other types of devices connected to the same PMBus, see the SMBus device address assignments table in Appendix C of the latest version of the System Management Bus (SMBus) specification. The SMBus specification can be downloaded at System Management Bus (SMBus) Specification.

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Table 12. PMBus Address Assignment Rules

ADDRESS	STATUS	REASON
0	Prohibited	SMBus general address call
1-10	Available	
11	Avoid	Causes conflicts with other devices during program flash updates.
12	Prohibited	PMBus alert response protocol
13-125	Available	
126	For JTAG Use	Default value; may cause conflicts with other devices.
127	Prohibited	Used by TI manufacturing for device tests.

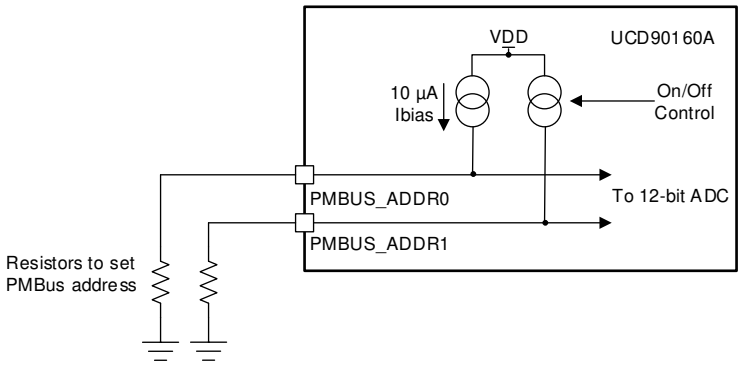


Figure 29. PMBus Address-Detection Method

CAUTION

Address 126 (0x7E) is not recommended to be selected as a permanent PMBus address for any given application design.

Leaving the address in default state as 126 (0x7E) will enable the JTAG and not allow using the JTAG compatible pins (36-39) as GPIOs.

7.4.21 Device Reset

The UCD90160A has an integrated power-on reset (POR) circuit which monitors the supply voltage. At power up, the POR detects the V_{33D} rise. When V_{33D} is less than V_{RESET}, the device comes out of reset.

The device can be forced into the reset state by an external circuit connected to the $\overline{\text{RESET}}$ pin. A logic low voltage on this pin for longer than t_{RESET} holds the device in reset. it comes out of reset within 1 ms after $\overline{\text{RESET}}$ is released, and can return to a logic-high level. To avoid an erroneous trigger caused by noise, connect RESET to a 10-kΩ pullup resistor (from RESET to 3.3 V) and 1000-pF capacitor (from RESET to AVSS).

Any time the device comes out of reset, it begins an initialization routine that lasts about 20 ms. During the Initialization routine, the FPWM pins are held low. and all other GPIO and GPI pins are open-circuit. At the end of initialization, the device begins normal operation as defined by the device configuration.

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7.5 Programming

7.5.1 Device Configuration and Programming

From the factory, the device contains the sequencing and monitoring firmware. It is also configured so that all GPOs are high-impedance (except for FPWM/GPIO pins 17 to 24, which are driven low), with no sequencing or fault-response operation. See *Configuration Programming of UCD Devices*, available from the *Documentation & Help Center* that can be selected from the *Fusion Digital Power Designer* software Help menu, for full UCD90160A configuration details.

After the user has designed a configuration file using *Fusion GUI*, there are three general device-configuration programming options:

1. Devices can be programmed in-circuit by a host microcontroller using PMBus commands over I^2C (see the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference*). Each parameter write replaces the data in the associated memory (RAM) location. After all the required configuration data has been sent to the device, it is transferred to the associated nonvolatile memory (data flash) by issuing a special command, STORE_DEFAULT_ALL. This method is how the *Fusion Digital Power Designer* software normally reads and writes a device configuration. This method may cause unexpected behaviors on GPIO pins which can disable rails that provide power to device. It is not recommended for production programming.
2. The *Fusion Digital Power Designer* software (Figure 30) can create a PMBus or I^2C command script file that can be used by the I^2C master to configure the device. This method may cause unexpected behaviors on GPIO pins which can disable rails that provide power to device. It is not recommended for production programming.

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Programming (continued)

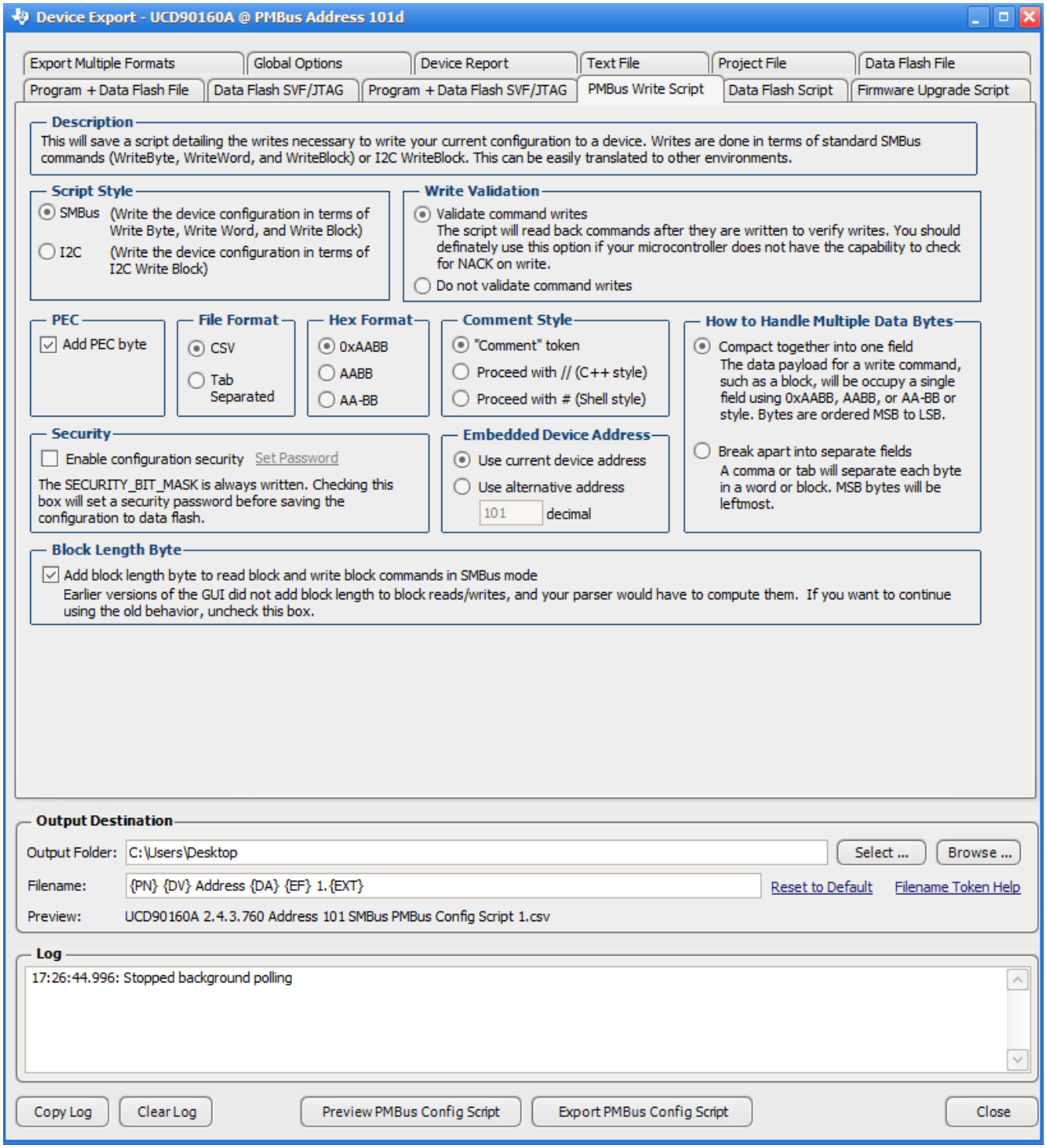


Figure 30. Fusion GUI PMBus Configuration Script Export Tool

3. Another in-circuit programming option is for the *Fusion Digital Power Designer* software to create a data flash image from the configuration file (Figure 31). The configuration files can be exported in Intel Hex, data flash script, Serial Vector Format (SVF) and S-record. The image file can be downloaded into the device using I^2C or JTAG. The *Fusion Digital Power Designer* software tools can be used on-board if the *Fusion Digital Power*

Programming (continued)

Designer software can gain ownership of the target board I^2C bus. It is recommended to use Intel Hex file or data flash script file for production programming because the GPIOs are under controlled states.

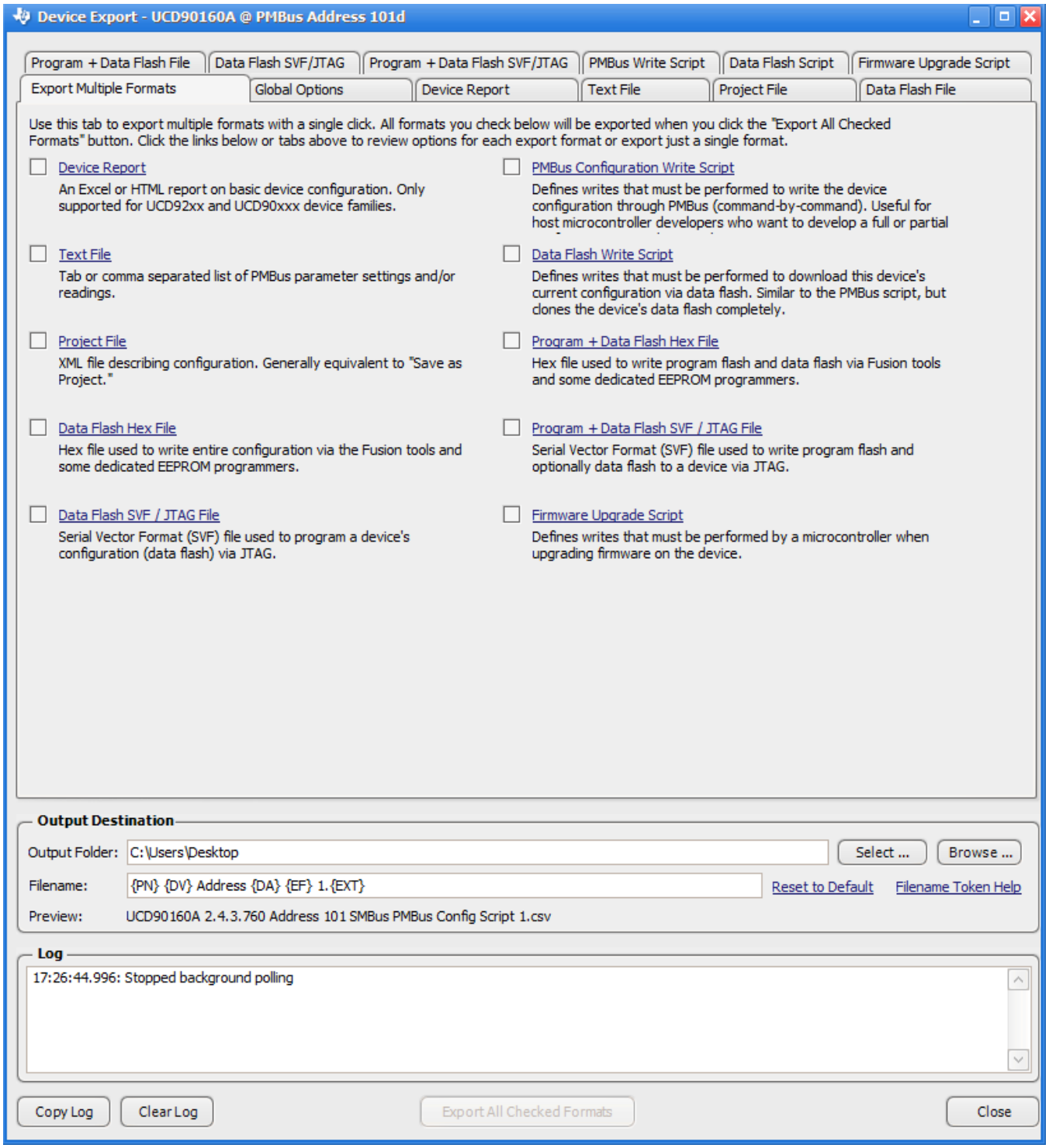


Figure 31. Fusion GUI Device Configuration Export Tool

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Programming (continued)

Devices can be programmed off-board using the *Fusion GUI* tools or a dedicated device programmer. For small runs, a ZIF socketed board with an I^2C header can be used with the standard Fusion GUI or manufacturing GUI. Use the UCD90SEQ64EVM-650: 64-Pin Sequencer Development Board. The *Fusion Digital Power Designer* software can also create a data flash file that can then be loaded into the UCD90160A device using a dedicated device programmer.

The UCD90160A must be powered in order to configure it using an I^2C or PMBus interface. The PMBus clock and data pins must be accessible and must be pulled high to the same V_{DD} supply that powers the device, with pullup resistors between 1 kΩ and 2 kΩ. Do not introduce additional bus capacitance (< 100 pF). Write the user configuration to data flash using a gang programmer via JTAG or I^2C interface before the device is installed in a circuit. To use the I^2C interface, the clock and data lines must be multiplexed or the device addresses must be assigned by socket. The *Fusion Digital Power Designer* software tools can be used for socket addressing. Pre-programming can also be done using a single device test fixture.

Table 13. Configuration Options

	DATA FLASH VIA JTAG	DATA FLASH VIA I^2C(Recommend)	PMBus COMMANDS VIA I^2C
Off-Board Configuration	Data Flash Export (.svf type file)	Data Flash Export (.srec or hex, data flash script type file)	System file/Project file I^2C/PMBus script
	Dedicated programmer	Fusion tools (with exclusive bus access via USB to I^2C adapter)	Fusion tools (with exclusive bus access via USB to I^2C adapter)
On-Board Configuration	Data flash export	Fusion tools (with exclusive bus access via USB to I^2C adapter)	Fusion tools (with exclusive bus access via USB to I^2C adapter)
	IC		

The advantages of off-board configuration include:

- Does not require access to device I^2C bus on board.
- Once soldered on board, full board power is available without further configuration.
- Can be partially reconfigured once the device is mounted.

7.5.1.1 Full Configuration Update While in Normal Mode

Although performing a full configuration of the UCD90160A in a controlled test setup is recommended, there may be times in which it is required to update the configuration while the device is in an operating system. Updating the full configuration based on methods listed in DEVICE CONFIGURATION AND PROGRAMMING section while the device is in an operating system can be challenging because these methods do not permit the UCD90160A to operate as required by application during the programming. During described methods the GPIOs may not be in the desired states which can disable rails that provide power to the UCD90160A device. The UCD90160A has the capability to allow full configuration update while still operating in normal mode.

Updating the full configuration while in normal mode will consist of disabling data flash write protection, erasing the data flash, writing the data flash image and reset the device. It is not required to reset the device immediately but make note that the UCD90160A will continue to operate based on previous configuration with fault logging disabled until reset. See *Configuration Programming of UCD Devices*, available from the *Documentation & Help Center* that can be selected from the *Fusion Digital Power Designer* software **Help** menu, for details. The data flash script file generated from *Fusion Digital Power Designer* software has all the required PMBus commands. This is the recommended method for production programming.

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7.5.2 JTAG Interface

The JTAG port can be used for production programming. Four of the six JTAG pins can also be used as GPIOs during normal operation. See the *Pin Functions* table at the beginning of the document and Table 4 for a list of the JTAG signals and which can be used as GPIOs. The JTAG port is compatible with the IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port and Boundary Scan Architecture specification. Boundary scan is not supported on this device.

The JTAG interface can provide an alternate interface for programming the device. It is disabled by default in order to enable the GPIO pins with which it is multiplexed. There are two conditions under which the JTAG interface is enabled:

- On power-up if the data flash is blank, allowing JTAG to be used for writing the configuration parameters to a programmed device with no PMBus interaction
- When address 126 (0x7E) is detected at power up. A short to ground or an open condition on either address pin will cause an address 126 (0x7E) to be generated which enables JTAG mode.

The *Fusion Digital Power Designer* software can create SVF files (See *Device Configuration and Programming* section) based on a given data flash configuration which can be used to program the desired configuration by JTAG. For Boundary Scan Description Language (BSDL) file that supports the UCD90160A, see the product folder in www.ti.com.

There are many JTAG programmers in the market and they all do not function the same. When using JTAG to configure the device, confirm that the availability of JTAG tools before committing to a programming solution.

7.5.3 Internal Fault Management and Memory Error Correction (ECC)

The UCD90160A verifies the firmware checksum at each power up. If it does not match, then the device waits for I^2C commands but does not execute the firmware. A device configuration checksum verification is also performed at power up. If it does not match, the factory default configuration is loaded. The PMBALERT# pin is asserted and a flag is set in the status register. The error-log checksum validates the contents of the error log to make sure that section of flash is not corrupted.

There is an internal firmware watchdog timer. If it times out, the device resets so that if the firmware program is corrupted, the device goes back to a known state. This is a normal device reset, so all of the GPIO pins are open-drain and the FPWM pins are driven low while the device is in reset. Checks are also done on each parameter that is passed, to make sure it falls within the acceptable range.

Error-correcting code (ECC) is used to improve data integrity and provide high-reliability storage of Data Flash contents. ECC uses dedicated hardware to generate extra check bits for the user data as it is written into the Flash memory. This adds an additional six bits to each 32-bit memory word stored into the Flash array. These extra check bits, along with the hardware ECC algorithm, allow for any single-bit error to be detected and corrected when the Data Flash is read.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

UCD90160A can be used to sequence, monitor and margin up to 10 voltage rails. Typical applications include automatic test equipment, telecommunication and networking equipment, servers and storage systems, and so forth. Device configuration can be performed in *Fusion Digital Power Designer* software without coding effort.

8.2 Typical Application

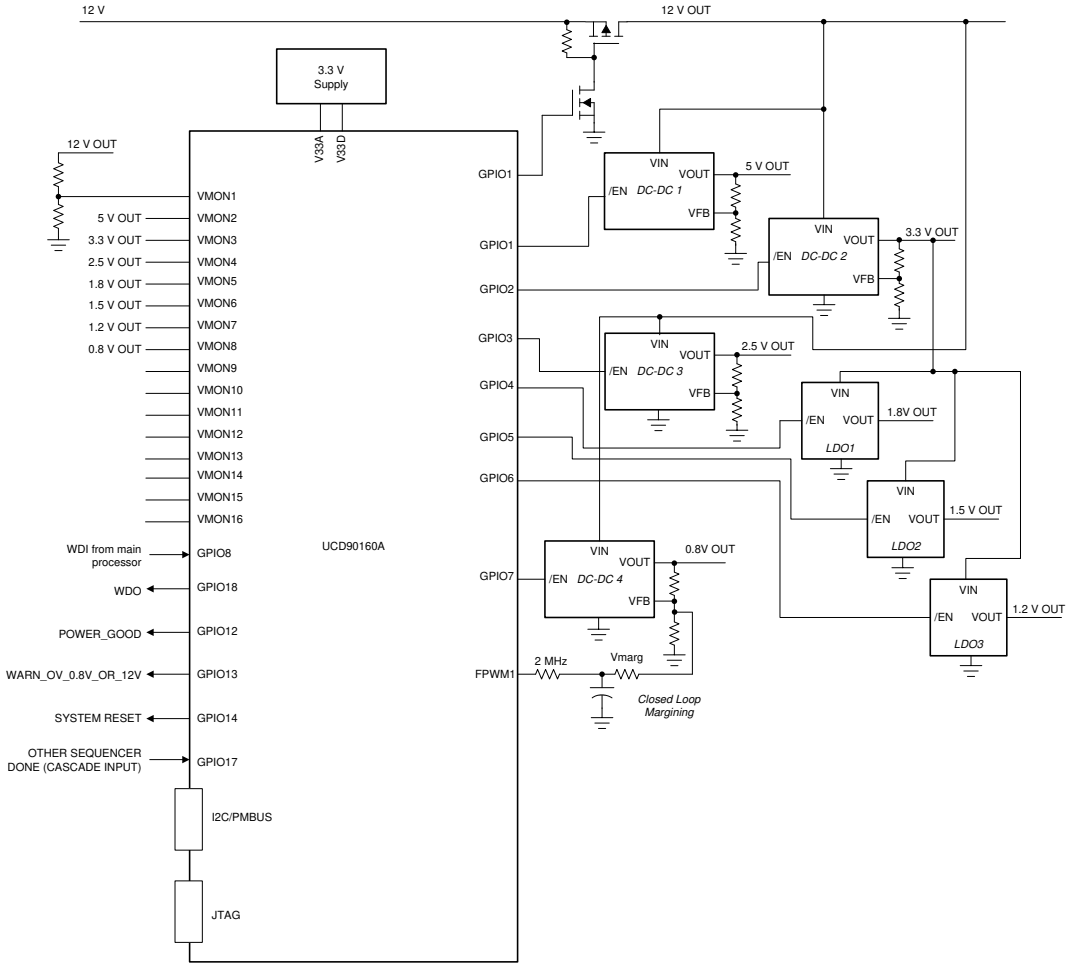


Figure 32. Typical Application Schematic

NOTE

Figure 32 is a simplified application schematic. Voltage dividers such as the ones placed on VMON1 input have been omitted for simplifying the schematic. All VMONx pins which are configured to measure a voltage that exceeds the 2.5V ADC reference are required to have a voltage divider.

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Typical Application (continued)

8.2.1 Design Requirements

The $\overline{\text{TRST}}$ pin must have a 10-kΩ pulldown resistor to ground and the $\overline{\text{RESET}}$ pin must have a 10-kΩ pullup resistor to V_{33D} and a 1-nF decoupling capacitor to ground. The components must be placed as close to the $\overline{\text{RESET}}$ pin as possible.

Depending on application environment, the PMBus signal integrity may be compromised at times. This causes the UCD90160A to receive incorrect PMBus commands. In a particular case, if (D9h) ROM_MODE command is erroneously received by a UCD90160A device, it causes the device to enter ROM mode, in this mode the device does not function unless *Fusion Digital Power Designer* software is connected to the device. To avoid such occurrences in a running system, it is suggested to enable Packet Error Checking (PEC) in the PMBus host. The UCD90160A automatically detects and works with PMBus hosts, both with and without PEC enabled.

The fault log in UCD90160A is checksum protected. After new log entries are written into the fault log, the checksum is updated accordingly. After each device reset, UCD90160A re-calculates the fault log checksum and compares it with the existing checksum. If the two checksums are not the same, the device determines the fault log as corrupted and erases the fault log as a result.

In the event that the V_{33D} power is dropped before the device finishes writing the fault log, the checksum is not updated correctly, thus the fault log is erased at the next power-up. The result is that no new faults are logged.

Such an event usually happens when the main power of the board drops and no standby power can stay alive for V_{33D}. If such a scenario can be anticipated in an application, it is strongly suggested to use the brown-out function and circuit as described in the *Brownout Function* section.

When a pair of FPWM pin are configured as both Rail Enable and PWM(either margining or general purpose PWM) functions, there would be glitches on the pin configured as rail enable when device is out of reset and under initialization, which may impact the connected power rail. It is not recommended to have such configuration.

PMBus commands(system file, project file, PMBus write script file) method is not recommended for the production programming because GPIO pins may have unexpected behaviors which can disable rails that provide power to device. Data flash hex file or data flash script file shall be used for production programming because GPIO pins are under controlled state.

It is mandatory that the V33D power shall be stable and no device reset shall be fired during the device programming. Data flash may be corrupted if failed to follow these rules.

When a pair of FPWM pins are both used for margining, after device is out of reset, the even FPWM pin may output some pulse which is up to the configured duty cycle and frequency. These pulses may cause unexpected behaviors on the margining rail if that rail is regulated before UCD is out of reset. It is recommended to use the even FPWM pin to margin rails that are directly controlled by the device.

Glitch filter on the GPI fault response may not work as expected to filter the glitch. A external glitch filter circuit is required if a noise GPI input is present.

Ignore input during delay feature on the LGPO may latch the given LGPO output if other LGPOs are required to process during the delay period.

WARNING

Do not use the $\overline{\text{RESET}}$ pin to power cycle the rails. Instead, use the PMBus_CNTRL pin as described in the *Power Supply Sequencing* section; or, use the Pin-Selected Rail States function described in the *Pin-Selected Rail States* section.

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Typical Application (continued)

8.2.2 Detailed Design Procedure

Fusion Digital Power Designer software can be used to design the device configuration online or offline (with or without a UCD90160A device connected to the computer). In offline mode, *Fusion Digital Power Designer* software prompts the user to create or open a *Project* file (.xml) at launch. In online mode, *Fusion Digital Power Designer* software automatically detects the device via the PMBus interface and reads the configuration data from the device. A USB-to-GPIO Adapter (HPA172) from Texas Instruments is required to connect *Fusion Digital Power Designer* software using the PMBus interface.

These are the general design steps:

1. Rail setup
2. Rail monitoring configuration
3. GPI configuration
4. Rail sequence configuration
5. Fault response configuration
6. GPO configuration
7. Margining configuration
8. Other configurations such as Pin Selected Rail States, Watchdog Timer, and System Reset.

After configuration changes, click the **Write to Hardware** button to apply the changes. In online mode, then click the **Store RAM to Flash** button to permanently store the new configuration into the device data flash.

8.2.3 Application Curves

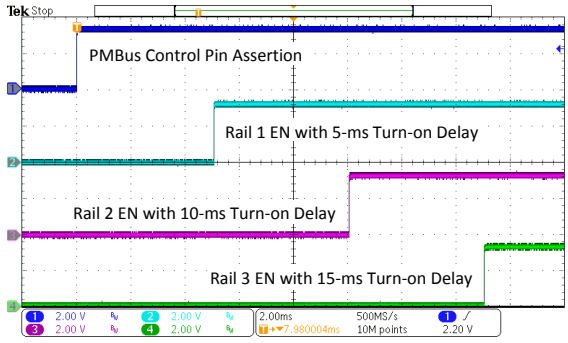


Figure 33. Example Power-On Sequence

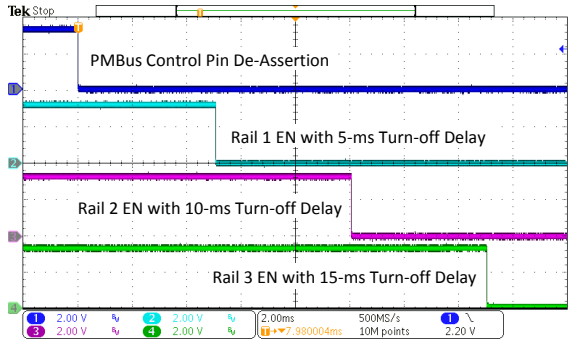


Figure 34. Example Power-Off Sequence

8.2.4 Estimating ADC Reporting Accuracy

The UCD90160A uses a 12-bit ADC and an internal 2.5-V reference (V_{REF}) to convert MON pin inputs into digitally reported voltages. The least significant bit (LSB) value is $V_{LSB} = V_{REF} / 2^N$ where N = 12, resulting in a VLSB = 610 μV. The error in the reported voltage is a function of the ADC linearity errors and any variations in VREF. The total unadjusted error (E_{TUE}) for the UCD90160A ADC is ±5 LSB, and the variation of VREF is ±0.5% between 0°C and 125°C and ±1% between –40°C and 125°C. V_{TUE} is calculated as $V_{LSB} \times E_{TUE}$. The total reported voltage error is the sum of the reference-voltage error and V_{TUE}. At lower monitored voltages, V_{TUE} dominates reported error, whereas at higher monitored voltages, the tolerance of V_{REF} dominates the reported error. Reported error can be calculated using Equation 3, where REFTOL is the tolerance of V_{REF}, V_{ACT} is the actual voltage being monitored at the MON pin, and V_{REF} is the nominal voltage of the ADC reference.

$$RPT_{ERR} = \left(\frac{1+REFTOL}{V_{ACT}}\right) \times \left(\frac{V_{REF} \times E_{TUE}}{4096} + V_{ACT}\right) - 1 \quad (3)$$

From Equation 3, for temperatures between 0°C and 125°C, if V_{ACT} = 0.5 V, then RPT_{ERR} = 1.11%. If V_{ACT} = 2.2 V, then RPT_{ERR} = 0.64%. For the full operating temperature range of –40°C to 125°C, if VACT = 0.5 V, then RPT_{ERR} = 1.62%. If V_{ACT} = 2.2 V, then RPT_{ERR} = 1.14%.

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9 Power Supply Recommendations

Use a 3.3-V power supply with the UCD90160A. At power-up, V33D must ascend from 2.3 V to 2.9 V monotonically with a minimum slew rate of 0.25 V/ms.

10 Layout

10.1 Layout Guidelines

The thermal pad provides a thermal and mechanical interface between the device and the printed circuit board (PCB). Connect the exposed thermal pad of the PCB to the device V_{SS} pins and provide at least a 4 × 4 pattern of PCB vias to connect the thermal pad and V_{SS} pins to the circuit ground on other PCB layers.

For supply-voltage decoupling, provide power supply pin bypass to the device as follows:

- 1-μF, X7R ceramic in parallel with 0.01-μF, X7R ceramic at pin 47 (BPCAP)
- 0.1-μF, X7R ceramic in parallel with 4.7-μF, X5R ceramic at pins 44 (V_{33DIO2}) and 45 (V_{33D})
- 0.1-μF, X7R ceramic at pin 7 (V_{33DIO1})
- 0.1-μF, X7R ceramic in parallel with 4.7-μF, X5R ceramic at pin 46 (V_{33A})
- Connect V33D (pin 45), V33DIO1 (pin 7) and V33DIO2 (pin 44) to 3.3-V supply directly. Connect V33A (pin 46) to V33D through a 4.99-Ω resistor. This resistor and V33A decoupling capacitors form a low-pass filter to reduce noise on V33A.

Depending on use and application of the various GPIO signals used as digital outputs, some impedance control may be desired to quiet fast signal edges. For example, when using the FPWM pins for fan control or voltage margining, the pin is configured as a digital *clock* signal. Route these signals away from sensitive analog signals. It is also good design practice to provide a series impedance of 20 Ω to 33 Ω at the signal source to slow fast digital edges.

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10.2 Layout Example

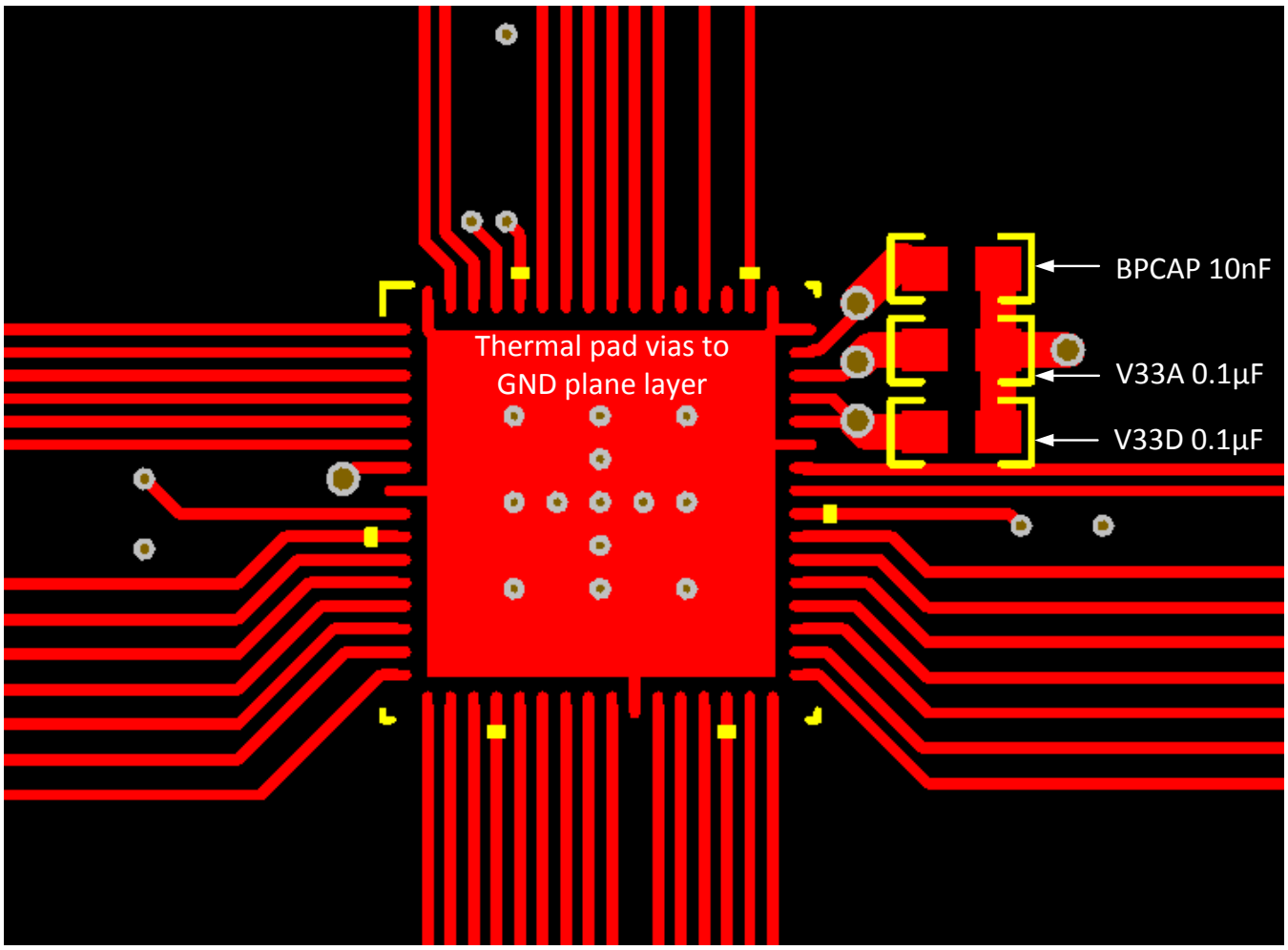


Figure 35. Top Layer

Layout Example (continued)

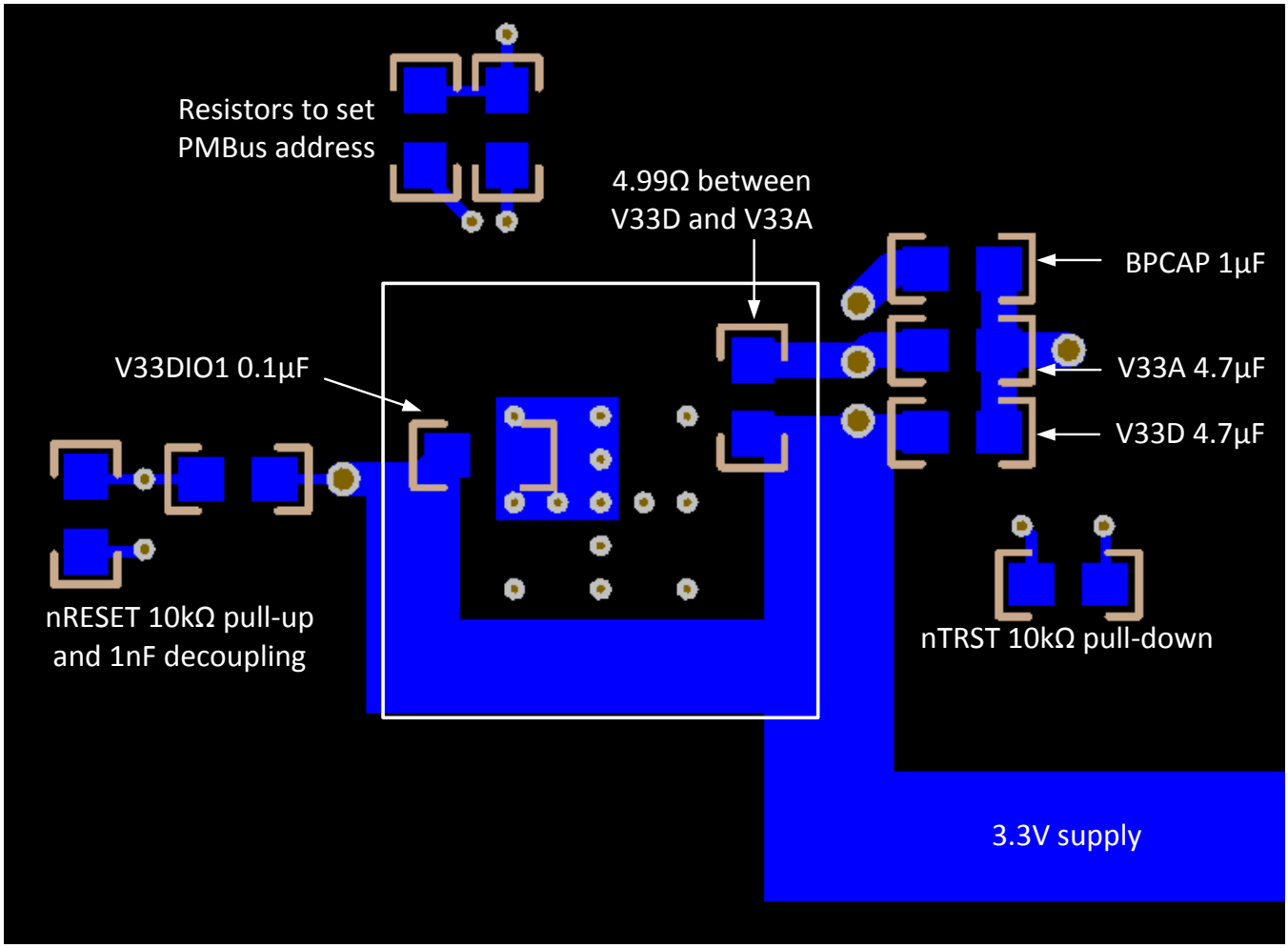


Figure 36. Bottom Layer

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11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

《UCD90xxx 序列发生器和系统健康状况控制器 PMBus™ 命令参考》(SLVU352)

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 商标

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All other trademarks are the property of their respective owners.

11.6 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCD90160ARGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 125	UCD90160A
UCD90160ARGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	UCD90160A
UCD90160ARGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	UCD90160A
UCD90160ARGCRG4	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90160A
UCD90160ARGCRG4.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90160A
UCD90160ARGCRG4.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90160A
UCD90160ARGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90160A
UCD90160ARGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90160A
UCD90160ARGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90160A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

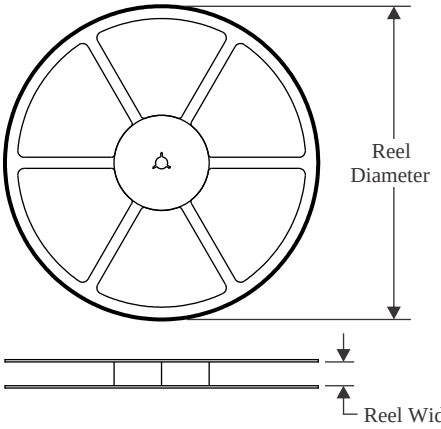
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

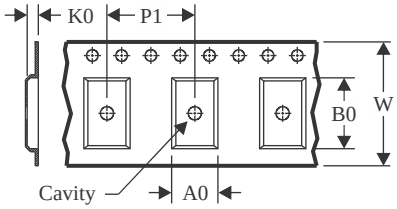
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

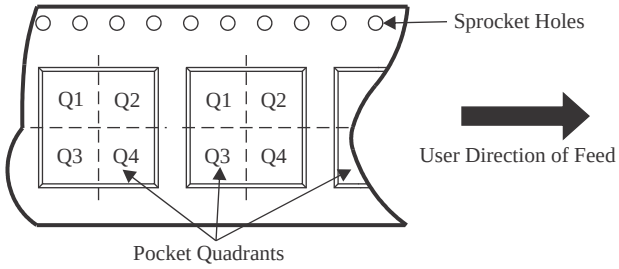


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

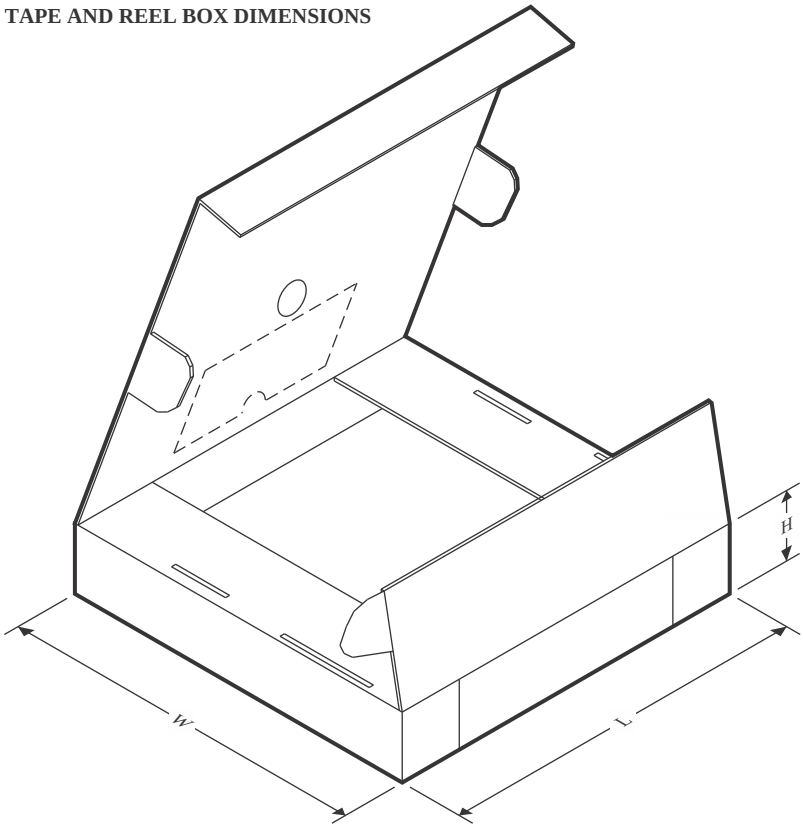
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD90160ARGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
UCD90160ARGCRG4	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
UCD90160ARGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD90160ARGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
UCD90160ARGCRG4	VQFN	RGC	64	2000	367.0	367.0	38.0
UCD90160ARGCT	VQFN	RGC	64	250	210.0	185.0	35.0

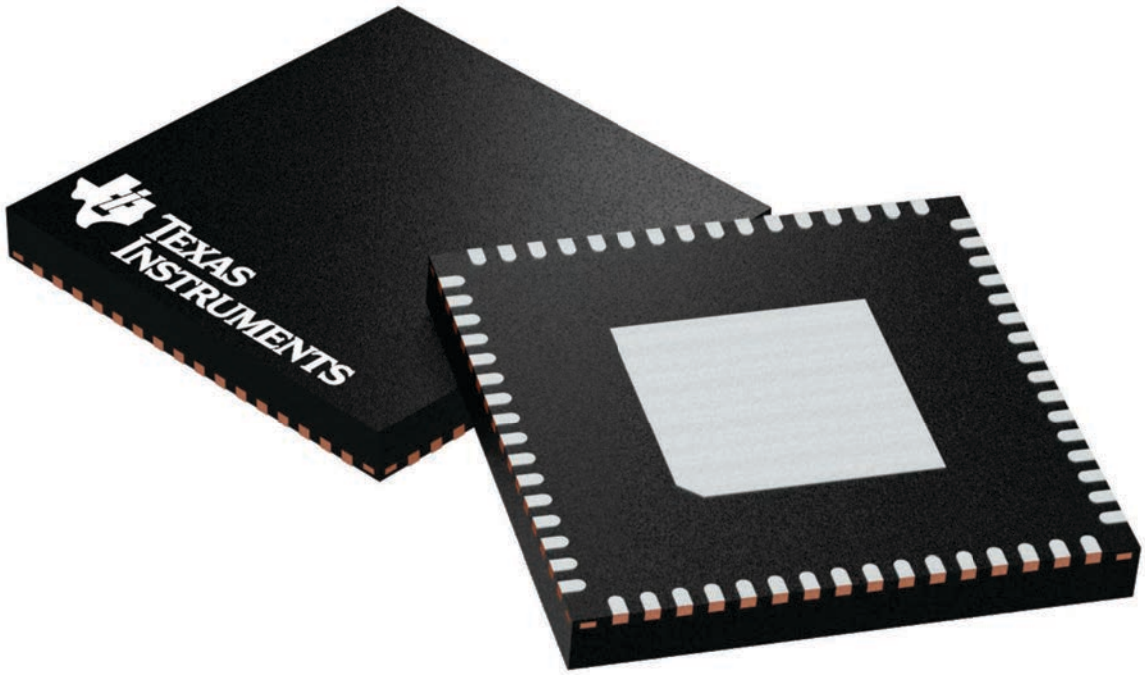
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

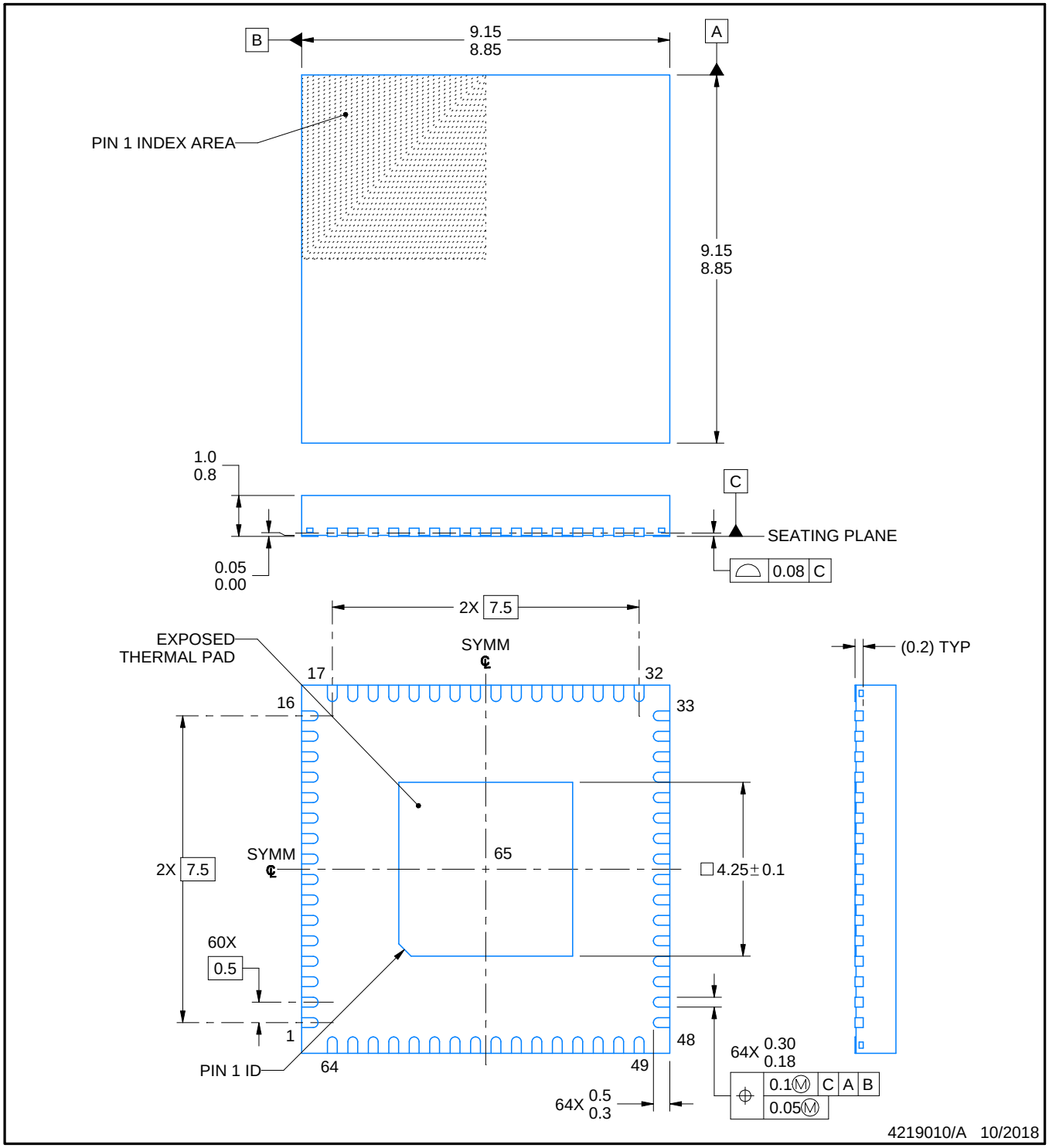
4224597/A

PACKAGE OUTLINE

RGC0064B

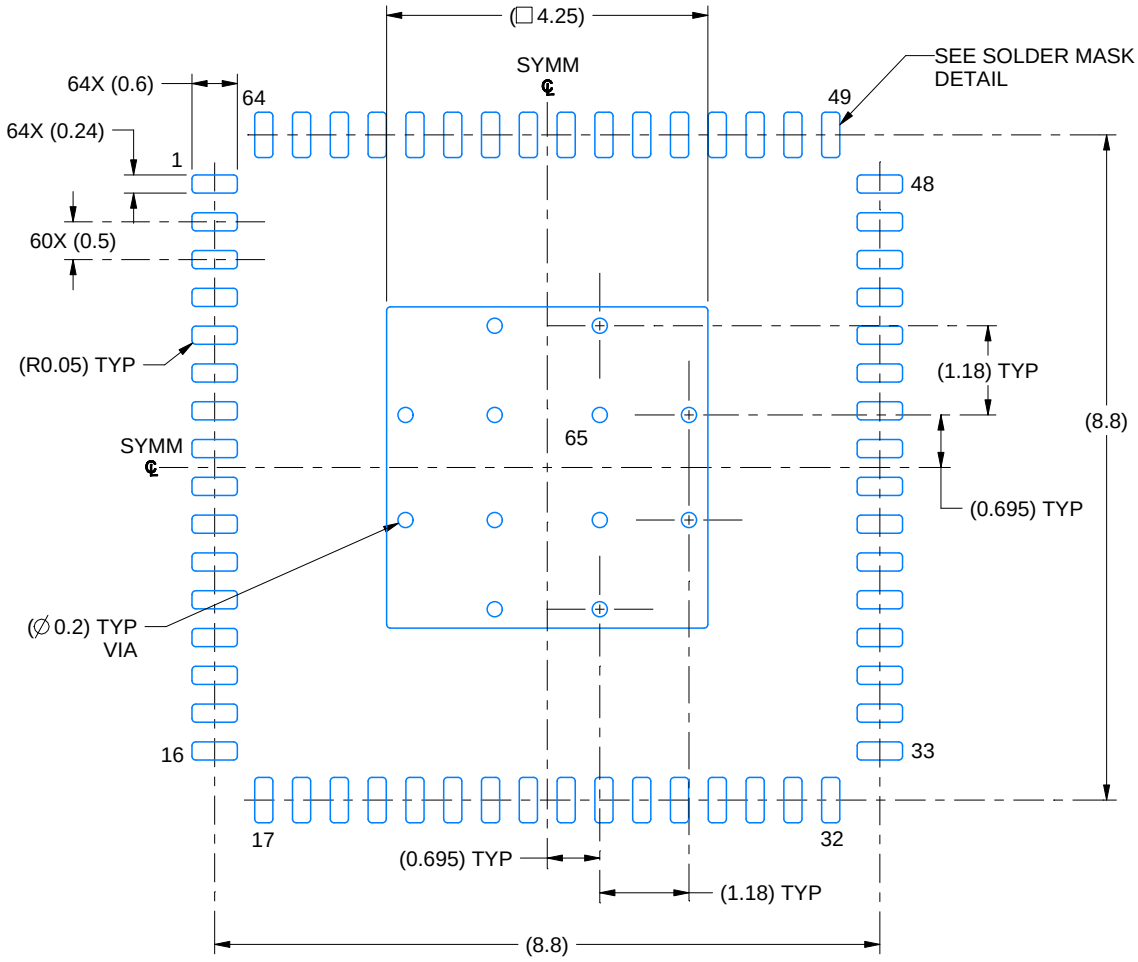
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

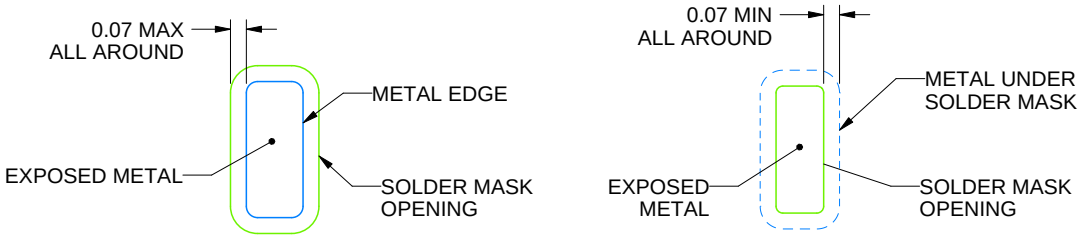


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

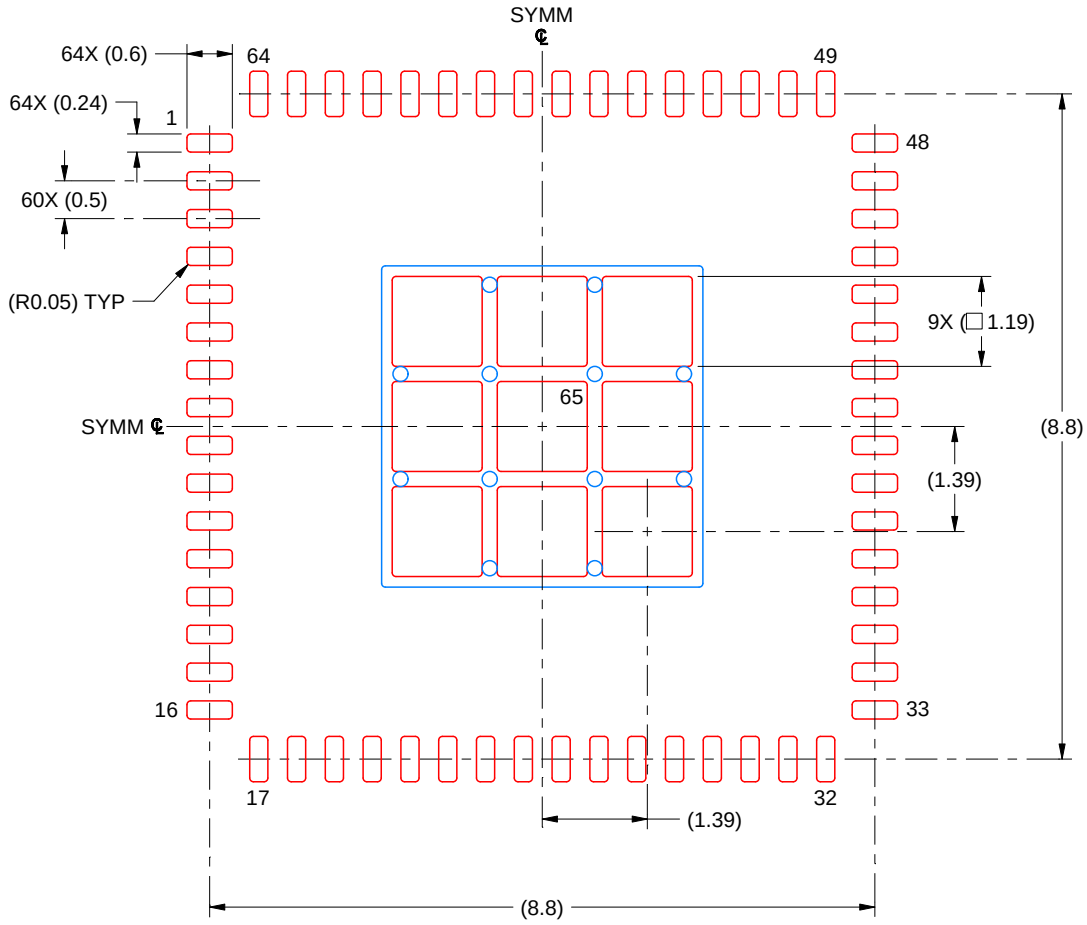


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月