LC75760UJA

LED Driver, 12-channel, Constant Current

The LC75760UJA is 12-channel LED driver having shift register circuit (serial input, series/parallel output), latch circuit, LED driver of the constant current output type. It is usable for display such as illumination, the backlight LED, the warning light of the instrument panel. This LSI has 6-ch PWM (Pulse Width Modulation) function to perform brightness adjustment of the LED. Furthermore, built-in the thermal protection function and open/short/adjacent outputs short detection function.

Features

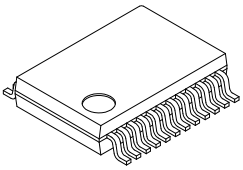
- The LED Driver Outputs of Up to 12-ch can Drive LED Directly
  - Constant Current Output Form
  - Output Voltage: Absolute Maximum Rating 6.8 V
    Maximum Operating Voltage 6.3 V
  - Output Current: Absolute Maximum Rating 60 mA
    Maximum Operating Current 50 mA
  - Output Current Regulation Function (256 Steps)
  - Open/Short/Adjacent Outputs Short Detection Function
  - Slew Rate Limited Switching Function
- Serial Data Communication Supports 4-line Serial Format
  - Support 3.3 V and 5.0 V Operation
  - Maximum Operating Frequency 2 MHz
- Built-in 6-ch PWM Function for Brightness Adjustment of LED
  - Resolution of 128, 256, 512 or 1024 Steps
  - PWM Frame Frequency can be Controlled by Serial Data
- Built-in Thermal Protection Function
  (125°C: Automatic Adjustment of PWM, 150°C: Forced-off All LEDs)
- Provides the ERR Output Pin
  (125°C Temperature Abnormality, Open/Short/Adjacent Outputs Short Abnormality, LED Pull-up Supply Voltage Abnormality, External Resistance Abnormally, Fundamental Clock Abnormality, Reset Action)
- Provides a $\overline{\text{RES}}$ Pin and Built-in Voltage Detection Type Reset Circuit (VDET) for LSI Internal Initialization
- Switch of the Internal Oscillator Operating Mode and the External Clock Operating Mode can be Controlled by Serial Data
- Built-in Oscillator Circuit. (Built-in Resister and Capacitor for Oscillation)
- Built-in External Resistance Value Diagnosis Function for Constant Current
- AEC–Q100 Qualified and PPAP Capable

Typical Applications

- Automotive: Instrument Cluster, HVAC, Head Up Display
- Industrial: Measurement Equipment

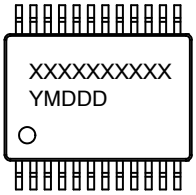
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SSOP24 (225 mil)
CASE 565AR

MARKING DIAGRAM



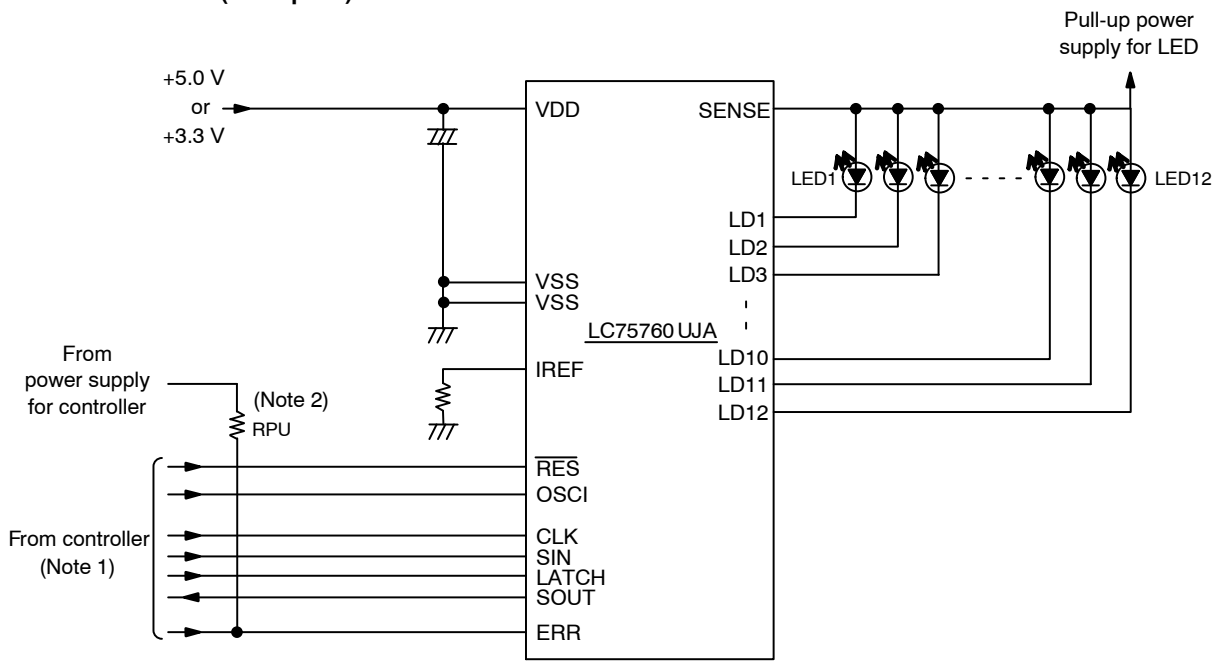
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

See detailed ordering and shipping information on page 63 of this data sheet.

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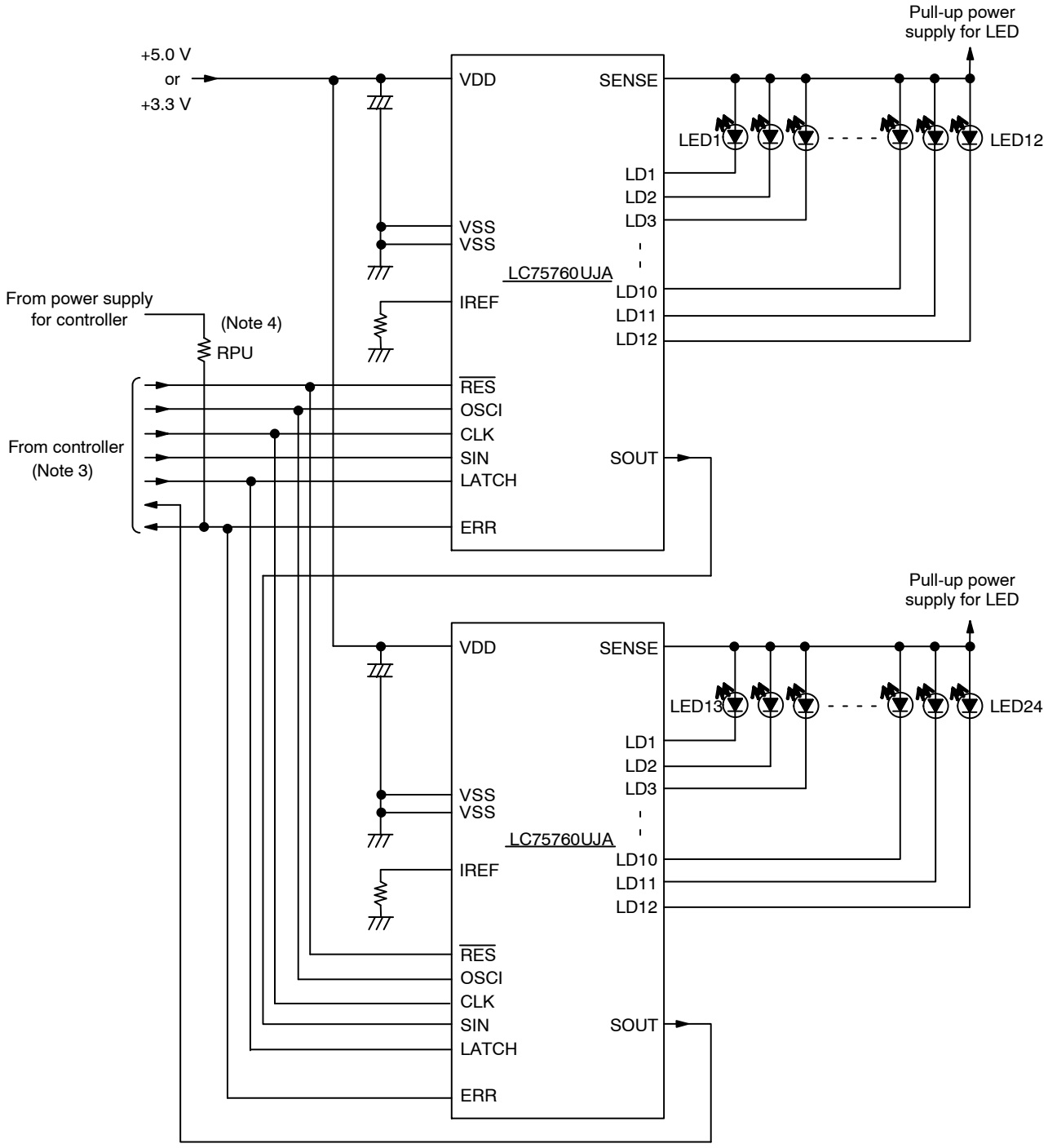
(Example 1) One LC75760UJA is used with 4−line serial interface format.



1. The pins to be connected to the controller (CLK, SIN, LATCH, $\overline{\text{RES}}$, OSCI) can handle 3.3 V or 5 V.
2. The ERR pin with an open-drain output type requires a pull-up resistor (RPU). Select a resistance (between 1 kΩ and 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Figure 1. Application Schematic 1

(Example 2) Two LC75760UJA are used with 4−line serial interface format.



3. The pins to be connected to the controller (CLK, SIN, LATCH, $\overline{\text{RES}}$, OSCI) can handle 3.3 V or 5 V.
4. The ERR pin with an open-drain output type requires a pull-up resistor (RPU). Select a resistance (between 1 kΩ and 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Figure 2. Application Schematic 2

BLOCK DIAGRAM

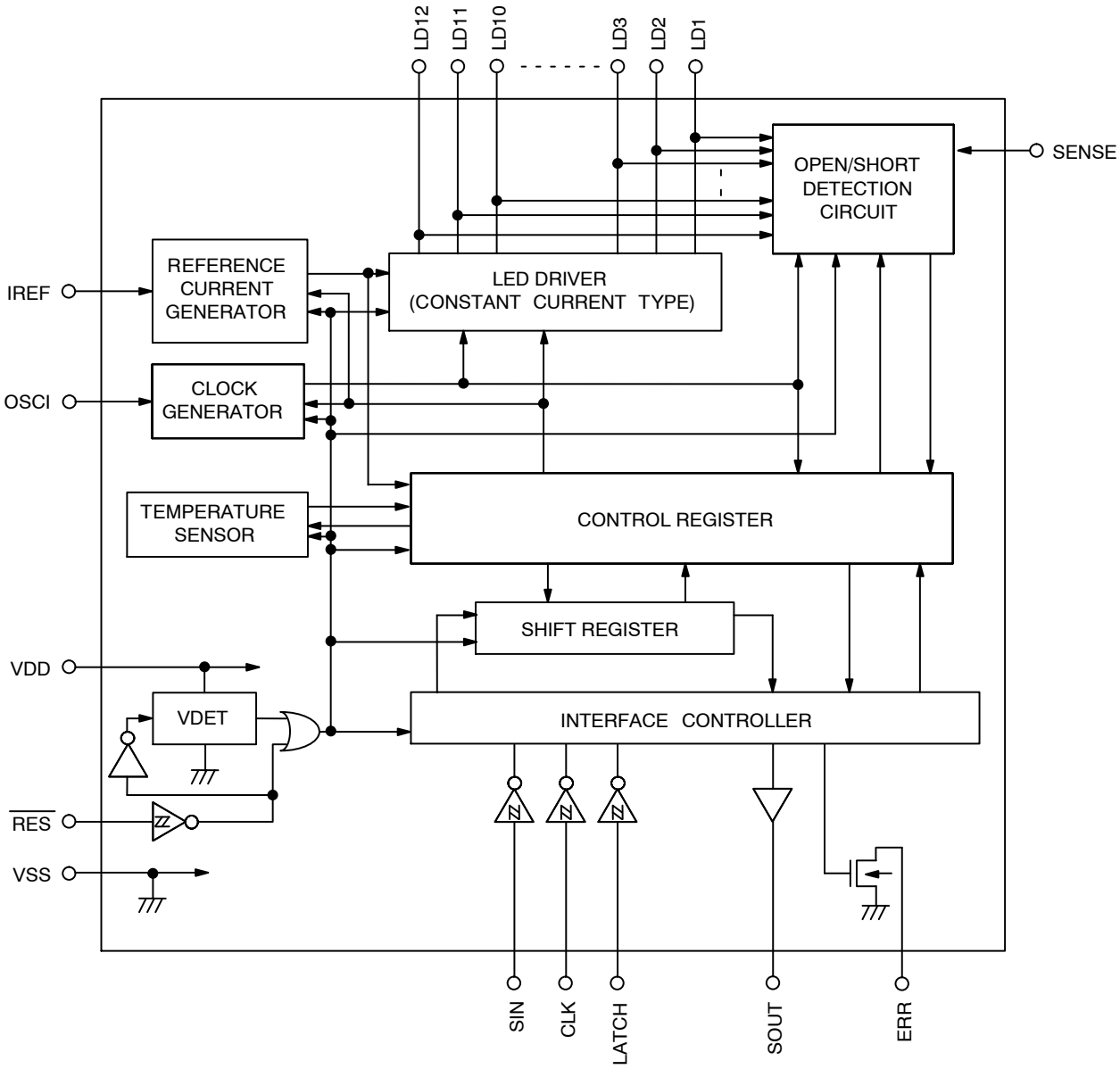


Figure 3. Simplified Block Diagram

PIN ASSIGNMENT

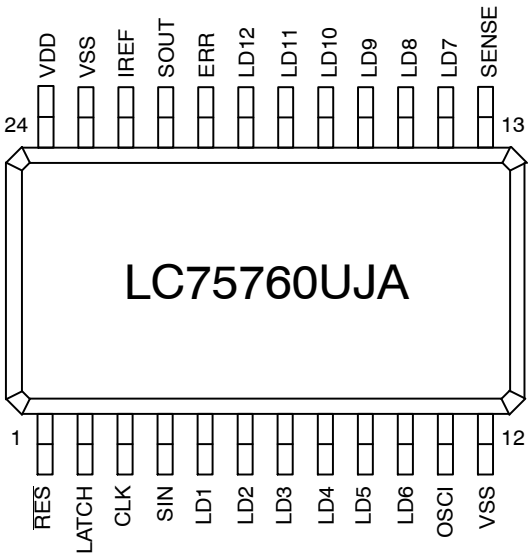


Figure 4. Pin Assignment (Top View)

PIN FUNCTION

Pin Name	Pin No.	Function	Active	I/O	Handing when Unused
VDD	24	This is power supply pin. Supply the voltage between +2.7 V and +5.5 V.	–	–	–
VSS	12, 23	These are power supply pins. Connect to GND.	–	–	–
SIN	4	This is an input pin for serial data transfer, and connects to the controller. Input the serial data. The serial data are received at the rising edge of the shift clock (CLK).	–	I	GND
CLK	3	This is an input pin for serial data transfer, and connects to the controller. Input the shift clock.	↑	I	GND
LATCH	2	This is an input pin for serial data transfer, and connects to the controller. Input the latch pulse.	H	I	GND
OSCI	11	This is an input pin for the external clock. Input the clock ($f_{OSCI}1$ = 200 kHz or $f_{OSCI}2$ = 150 kHz) from the external, when it is the external clock operating mode. Connect to GND, when it is the internal oscillator operating mode.	–	I	GND
$\overline{RES}$	1	This is an input pin for reset. – $\overline{RES}$ = Low(VSS): Reset(Initialization of LSI internal) Refer to “About the reset of the system” for the elaboration. – $\overline{RES}$ = High(VDD): Normal operation	L	I	VDD
LD1 to LD6, LD7 to LD12	5 to 10, 14 to 19	These are LED driver output pins. These output pins are constant current output. Brightness control of the LED is possible by the output current regulation function and the PWM function. When there are LED driver output pins not to use, set mask control data (MLD1 to MLD12) of the corresponding LED driver output pins to “0” (LED turning off).	–	O	OPEN

PIN FUNCTION (continued)

Pin Name	Pin No.	Function	Active	I/O	Handing when Unused
SENSE	13	This is a pull-up voltage monitor pin for LED. Input pull-up power supply voltage (6.3 V max) for LED.	–	I	–
IREF	22	This is a resistance connection pin for reference current (IREF) setting. Connect resistance between IREF pin and GND.	–	I	–
ERR	20	This is error detection signal output pin (open drain output). When temperature abnormality (TSD125 = “1”) or short abnormality of over one LED driver output (SERR = “1”) or open abnormality of over one LED driver output (OERR = “1”) or adjacent outputs short abnormality of over one LED driver output (AERR = “1”) or LED driver supply voltage abnormality (VERR = “1”) or the external resistance value abnormality (IR1,0 = “0,0”, “1,1”) or fundamental clock abnormality (CERR = “1”) or reset action (POR = “1”) of the system occurred, the ERR pin outputs Low (VSS). Furthermore, connect the external pull-up resistor. In addition, if the control data ERD is “1”, application can read each diagnosis result data from the ERR pin with serial data transfer clock.	–	O	OPEN
SOUT	21	This is a serial data output pin for shift registers (CMOS output). This pin outputs data from a falling edge of shift clock (CLK).	–	O	OPEN

MAXIMUM RATINGS (V_{SS} = 0 V)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD} max	Maximum Supply Voltage	VDD	–0.3 to +6.5	V
$V_{IN}1$	Input Voltage	SIN, CLK, LATCH, $\overline{RES}$, OSCI	–0.3 to +6.5	V
$V_{IN}2$		IREF	–0.3 to V_{DD}+0.3	
$V_{IN}3$		SENSE	–0.3 to +6.8	
$V_{OUT}1$	Output Voltage	ERR	–0.3 to +6.5	V
$V_{OUT}2$		SOUT	–0.3 to V_{DD}+0.3	
$V_{OUT}3$		LD1 to LD12	–0.3 to +6.8	
$I_{OUT}1$	Output Current	SOUT, ERR	10	mA
$I_{OUT}2$		LD1 to LD12	60	
$P_{dmax}1$	Allowable Power Dissipation	T_A = +25°C with PCB (Note 5)	1200	mW
$P_{dmax}2$		T_A = +95°C with PCB (Note 5)	525	
$P_{dmax}3$		T_A = +105°C with PCB (Note 5)	430	
$P_{dmax}4$		T_A = +25°C with PCB (Note 6)	2000	
$P_{dmax}5$		T_A = +95°C with PCB (Note 6)	880	
$P_{dmax}6$		T_A = +105°C with PCB (Note 6)	720	
T_J max	Junction Temperature		+150	°C
T_{opr}	Operating Temperature		–40 to +105	°C
T_{stg}	Storage Temperature		–55 to +150	°C

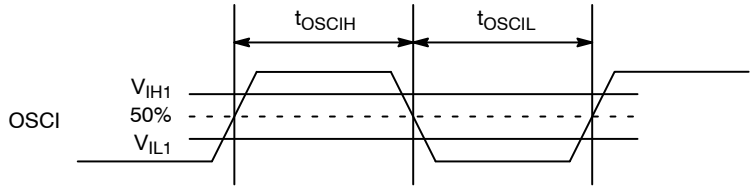
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

5. The PCB is a glass-epoxy board of 76.2 mm × 114.3 mm × 1.6 mm with 2 layers.
6. The PCB is a glass-epoxy board of 76.2 mm × 114.3 mm × 1.6 mm with 4 layers.

RECOMMENDED OPERATING RANGES (V_{SS} = 0 V, T_A = −40 to +105°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	VDD	2.7	–	5.5	V
$V_{IH}1$	Input High-level Voltage	SIN, CLK, LATCH, $\overline{RES}$, OSCI VDD = 3.6 V to 5.5 V	0.45 V_{DD}	–	5.5	V
		SIN, CLK, LATCH, $\overline{RES}$, OSCI VDD = 2.7 V to 3.6 V	0.6 V_{DD}	–	3.6	
$V_{IL}1$	Input Low-level Voltage	SIN, CLK, LATCH, $\overline{RES}$, OSCI	0	–	0.2 V_{DD}	V
VLED	Pull-up Output Voltage for LED	SENSE	–	–	6.3	V
I_{OLED}	LED Driver Output Current	LD1 to LD12	10	30	50	mA
$f_{OSCI}1$	External Clock Operating Frequency	OSCI (Figure 5)	190	200	210	kHz
$f_{OSCI}2$		OSCI (Figure 5)	142.5	150	157.5	
D_{OSCI}	External Clock Duty	OSCI (Figure 5)	40	50	60	%

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.



$$f_{OSCI1.2} = \frac{1}{t_{OSCIH} + t_{OSCIL}} \text{ [kHz]}$$

$$D_{OSCI} = \frac{t_{OSCIH}}{t_{OSCIH} + t_{OSCIL}} \times 100 \text{ [\%]}$$

Figure 5. OSCI Pin Clock Timing

ELECTRICAL CHARACTERISTICS (for the recommended operating ranges)

Symbol	Parameter	Pins	Conditions	Min	Typ	Max	Unit
VH1	Hysteresis	SIN, CLK, LATCH, $\overline{RES}$, OSCI		–	0.03V_{DD}	–	V
IIH1	Input High-level Current	SIN, CLK, LATCH, $\overline{RES}$, OSCI	VI = 5.5 V	–	–	5.0	μA
IIH2		SENSE	VI = 6.3 V, $\overline{RES}$ = “L”	–	–	5.0	μA
IIH3		SENSE	VI = 6.3 V, $\overline{RES}$ = “H”	–	–	100	μA
IIL1	Input Low-level Current	SIN, CLK, LATCH, $\overline{RES}$, OSCI	VI = 0 V	–5.0	–	–	μA
IIL2		SENSE	VI = 0 V, $\overline{RES}$ = “L”	–5.0	–	–	μA
IIL3		SENSE	VI = 0 V, $\overline{RES}$ = “H”	–5.0	–	–	μA
IOFFH1	Output Off Leak Current	ERR	VO = 5.5 V	–	–	5.0	μA
IOFFH2		LD1 to LD12	VO = 6.3 V	–	–	5.0	
VOH1	Output High-level Voltage	SOUT	IO = –4 mA	V_{DD}–0.3	–	–	V
VOL1	Output Low-level Voltage	SOUT, ERR	IO = 4 mA	–	–	0.3	V
IACO1	Output Current Accuracy	LD1 to LD12	ID = 10 mA, V_{DD} = 3.3 V, T_A = 25°C	–5	–	+5	%
IACO2		LD1 to LD12	ID = 30 mA, V_{DD} = 3.3 V, T_A = 25°C	–5	–	+5	
IACO3		LD1 to LD12	ID = 50 mA, V_{DD} = 3.3 V, T_A = 25°C	–5	–	+5	
VDET	Power-down Detection Voltage	VDD		2.0	2.2	2.4	V

ELECTRICAL CHARACTERISTICS (for the recommended operating ranges) (continued)

Symbol	Parameter	Pins	Conditions	Min	Typ	Max	Unit
VSES1	LED Driver Supply Abnormally Voltage	SENSE	V_{DD} = 4.5 V to 5.5 V	4.1	4.2	4.3	V
VSES2		SENSE	V_{DD} = 2.7 V to 5.5 V	2.3	2.4	2.5	
VLOP	Open Detection Voltage of the LED Driver Output	LD1 to LD12	Enabling the open or V_{SS} short detection function of the LED driver output. (Figure 19, Figure 20)	0.4	0.5	0.6	V
VLSH1	Short Detection Voltage of the LED Driver Output	LD1 to LD12	Enabling the VLED short or adjacent outputs short detection function of the LED driver output. (When sets VSH = 0.8 V typ). V_{DD} = 2.7 V to 5.5 V. (Figure 19, Figure 20)	0.7	0.8	0.9	V
VLSH2		LD1 to LD12	Enabling the VLED short or adjacent outputs short detection function of the LED driver output. (When sets VSH = 1.8 V typ). V_{DD} = 2.7 V to 5.5 V. (Figure 19, Figure 20)	1.65	1.8	1.95	V
VLSH3		LD1 to LD12	Enabling the VLED short or adjacent outputs short detection function of the LED driver output. (When sets VSH = 2.8 V typ). V_{DD} = 4.5 V to 5.5 V. (Figure 19, Figure 20)	2.6	2.8	3.0	V
VLSH4		LD1 to LD12	Enabling the VLED short or adjacent outputs short detection function of the LED driver output. (When sets VSH = 3.8 V typ). V_{DD} = 4.5 V to 5.5 V. (Figure 19, Figure 20)	3.55	3.8	4.05	V
fosc	Oscillator Frequency	Oscillator Circuit	Internal oscillator operating mode	140	200	260	kHz
VREF	Reference Voltage	IREF		1.1	1.2	1.23	V
TAC1	Temperature Monitoring Accuracy		Temperature accuracy sensing 125°C abnormality	125	135	150	°C
TAC2			Temperature accuracy sensing 150°C abnormality	150	165	–	°C
Thys	Temperature Hysteresis			–	15	–	°C
$I_{DD}1$	Current Drain	VDD	The reset of the system by the $\overline{RES}$ pin ($\overline{RES}$ = "L") V_{DD} = 5.5 V	–	1	15	μA
$I_{DD}2$		VDD	V_{DD} = 5.5 V, Outputs are open. REXT = 12 kΩ	–	2.5	5.0	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4-LINE SERIAL BUS INTERFACE TIMING CHARACTERISTICS (for the recommended operating ranges)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLK}	Clock Frequency	CLK (Figure 6)	–	–	2	MHz
t_{CKH}	High-level Clock Pulse Width	CLK (Figure 6)	250	–	–	ns
t_{CKL}	Low-level Clock Pulse Width	CLK (Figure 6)	250	–	–	ns
t_{DS}	Data Setup Time	CLK, SIN (Figure 6)	100	–	–	ns
t_{DH}	Data Hold Time	CLK, SIN (Figure 6)	100	–	–	ns
t_{r1}	Rise Time 1	CLK, SIN (Figure 6)	–	100	–	ns
t_{f1}	Fall Time 1	CLK, SIN (Figure 6)	–	100	–	ns
t_{LTS}	LATCH Setup Time	CLK, LATCH (Figure 6)	200	–	–	ns
t_{LTH}	LATCH Hold Time	CLK, LATCH (Figure 6)	200	–	–	ns
t_{WLT}	High-level LATCH Pulse Width	LATCH (Figure 6)	350	–	–	ns
t_{DLT}	SOUT Output Delay Time	CLK, SOUT (Figure 6)	–	–	1500	ns
t_{ERDLT}	ERR Output Delay Time	CLK, ERR (Note 7) (Figure 6)	–	–	1500	ns
t_{SP1}	Permission Noise Pulse Width	CLK, SIN, LATCH (Figure 6)	–	–	50	ns
t_{WRES}	Minimum Reset Pulse Width	$\overline{RES}$ (Figures 19, 20, 24)	1	–	–	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. This item is the reference value when the pull-up register RPU = 4.7 kΩ and the load capacitance CL = 10 pF. The ERR pin is open drain output, so note that this value is changed according to RPU and CL.

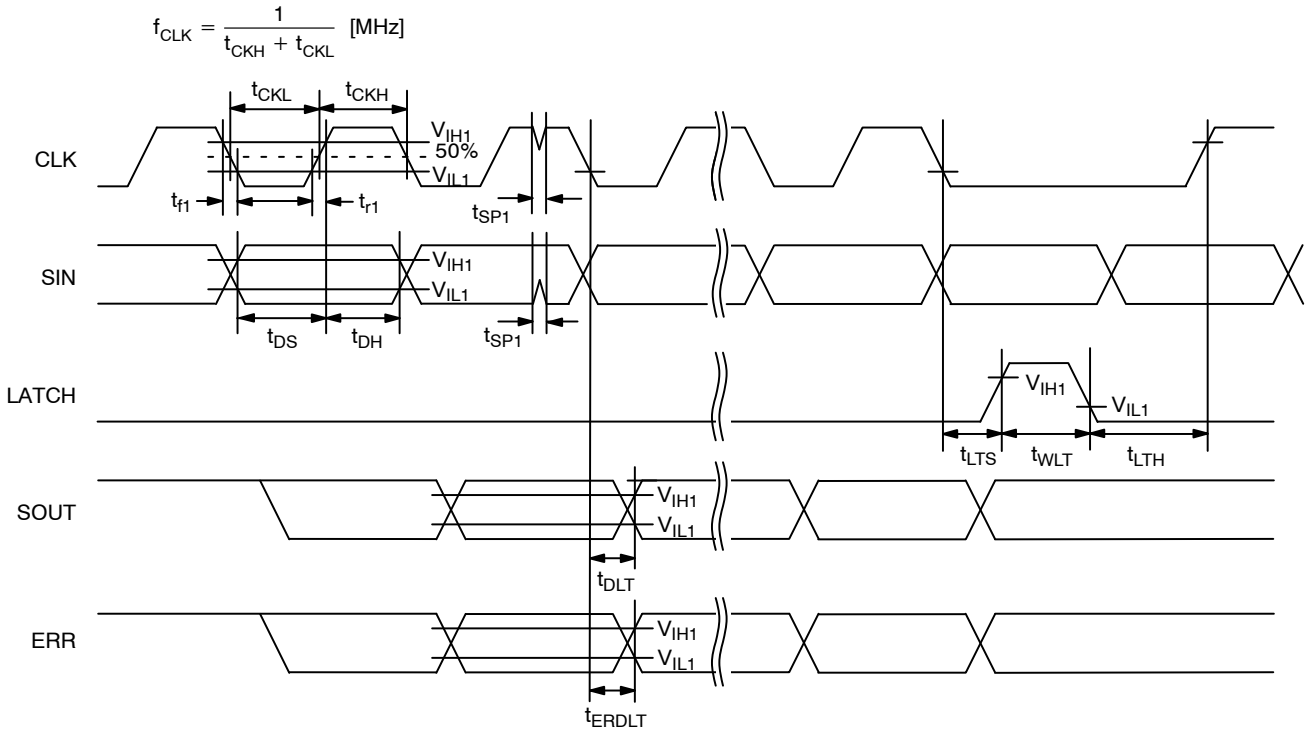


Figure 6. Data Input and Data Output Timing of 4-line Serial Bus Interface

FUNCTIONAL DESCRIPTION

Serial Data Transfer Format (In the Case of 4-line Serial Interface)

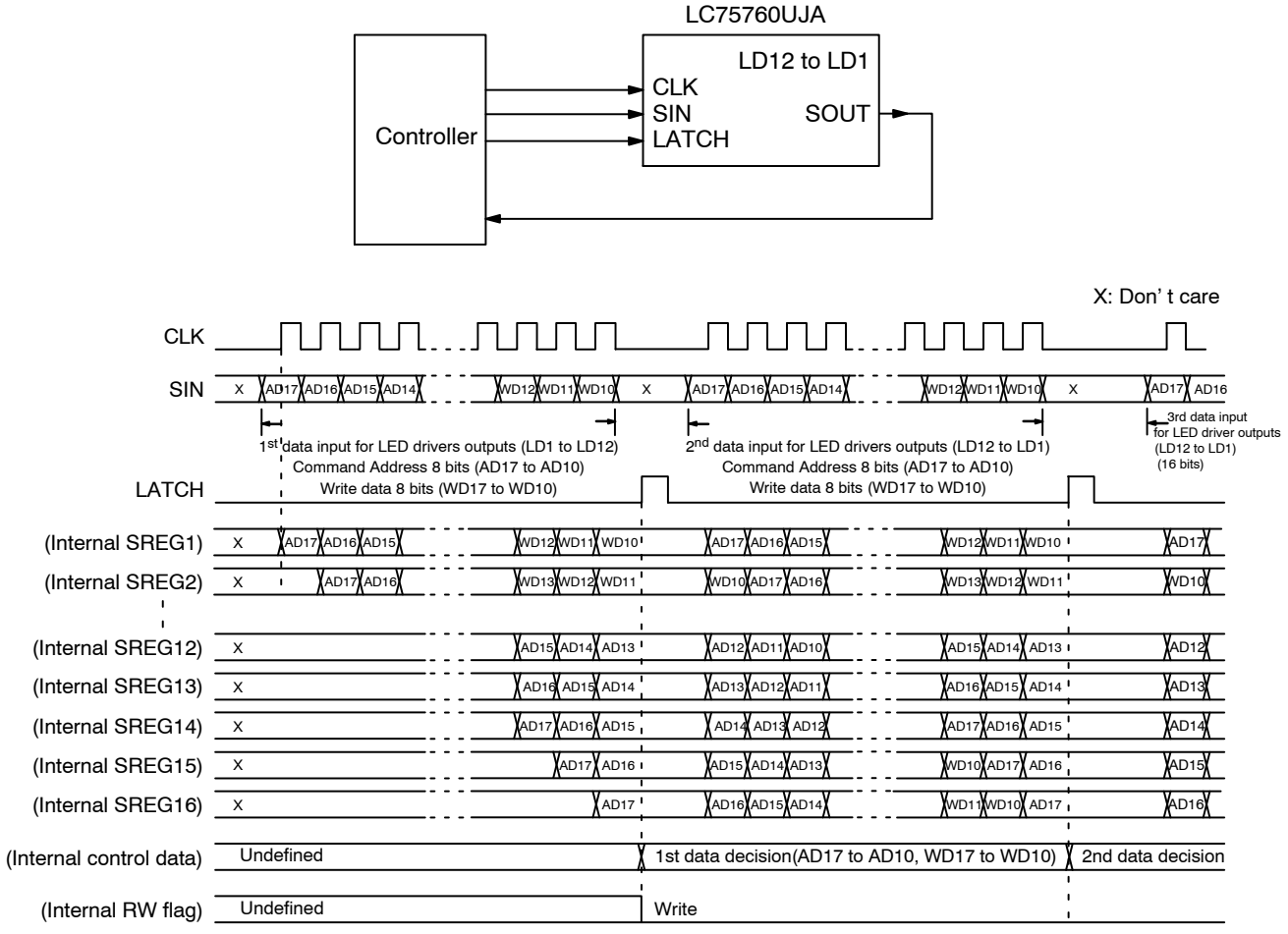
The 4-line serial interface is bidirectional serial interface using four bus lines of the CLK, SIN, SOUT and LATCH signal.

When a controller transmits data to this LSI, the controller transmits data (command address 8 bits, write data 8 bits) of 16 bits per one LSI to SIN pin in order of LSB from MSB and inputs LATCH signal. These serial data are received at the rising edge of the CLK signal. These data are latched and settled at the rising edge of the LATCH signal. When this LSI is a cascade connection, the controller inputs LATCH signal after having transmitted (16 × n) bits to SIN pin.

When a controller receives data from this LSI, the controller transmits data (command address 8 bits, dummy data 8 bits) of 16 bits per one LSI to SIN pin in order of LSB from MSB and inputs LATCH signal. These serial data are received at the rising edge of the CLK signal. This data is latched and settled at the rising edge of the LATCH signal. When read command address (ADn7 to ADn0) of higher 8 bits made a latch is distinguished from read command, read data (RDn7 to RDn0) is set to an internal shift register by a fall of the LATCH signal, and it is output to SOUT pin by a fall of the CLK signal. The controller can receive read data in a rising edge of the CLK signal. When this LSI does a cascade connection, the controller inputs LATCH signal after having transmitted (16 × n) bits to SIN pin.

NOTE: n: The number of connection.

(1) In the Case of One Device Use



Continued on the next page.

Figure 7. Transfer Example of Write Data of 4-line Serial Interface Using One Device

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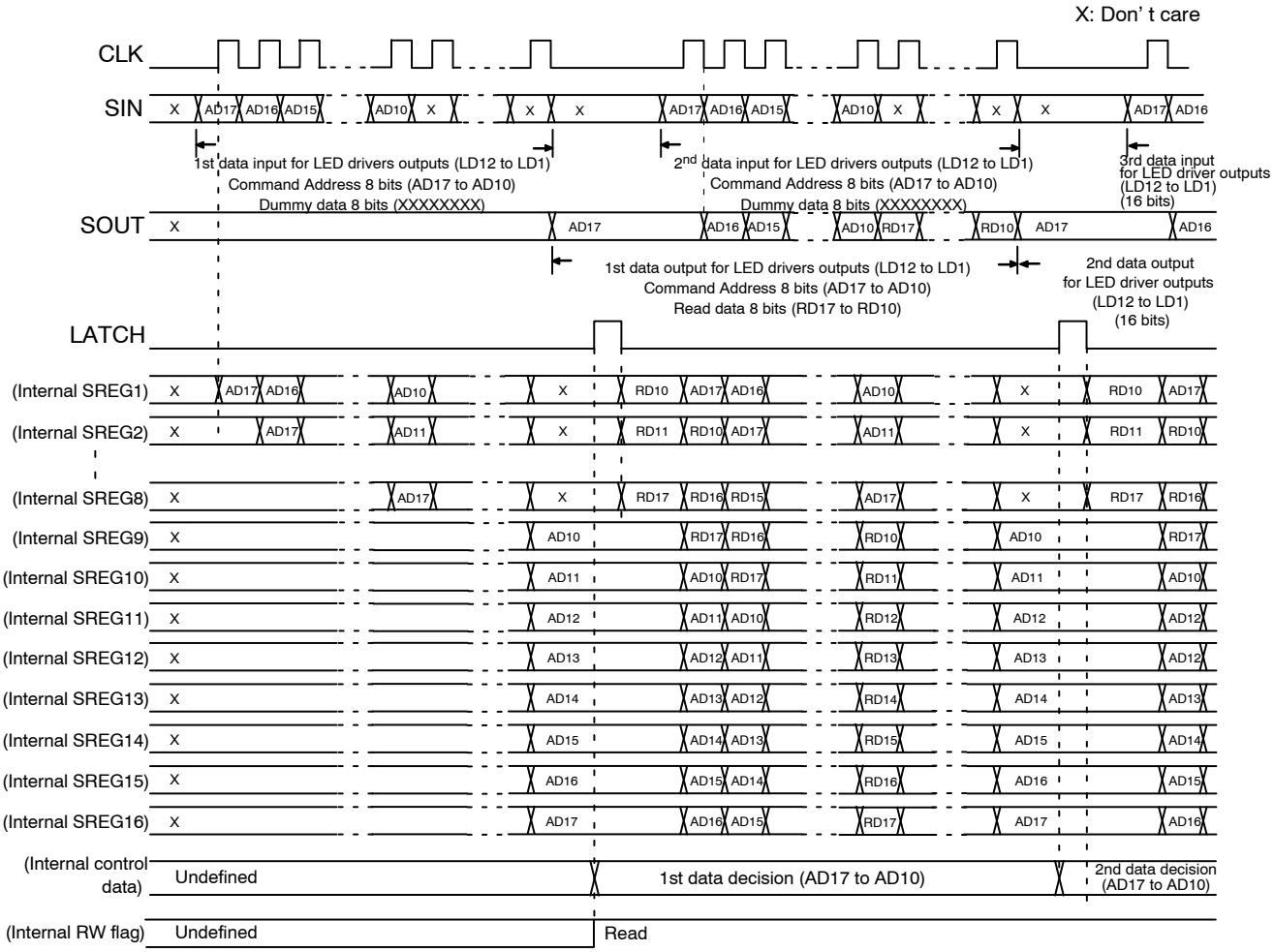


Figure 8. Transfer Example of Read Data of 4-line Serial Interface Using One Device

(2) In the Case of Cascade Connection (the Example of Two Device Connection)

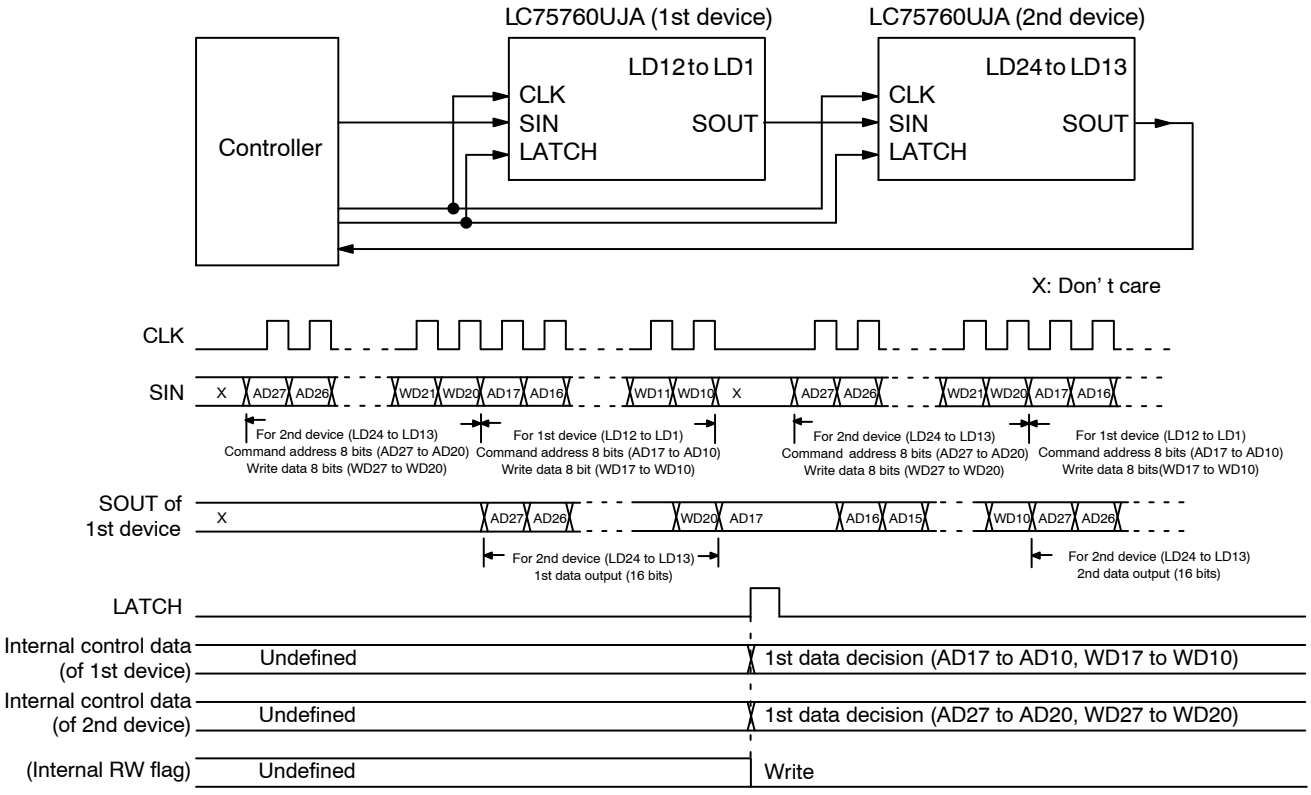


Figure 9. Transfer Example of Write Data of 4-line Serial Interface using Cascade Connection (the Example of Two Device Connection)

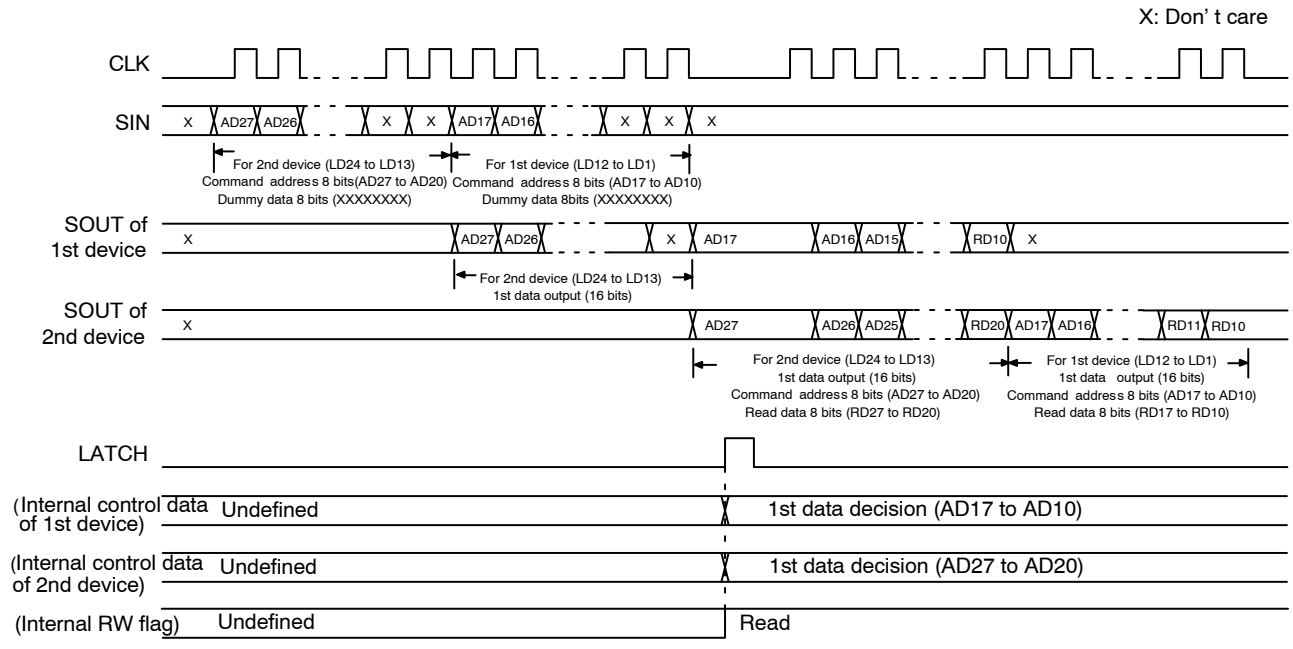


Figure 10. Transfer Example of Read Data of 4-line Serial Interface using Cascade Connection (the Example of Two Device Connection)

(3) In the Case of Reading the Diagnosis Results Data from ERR Pin (When the Control Data ERD = “1”)

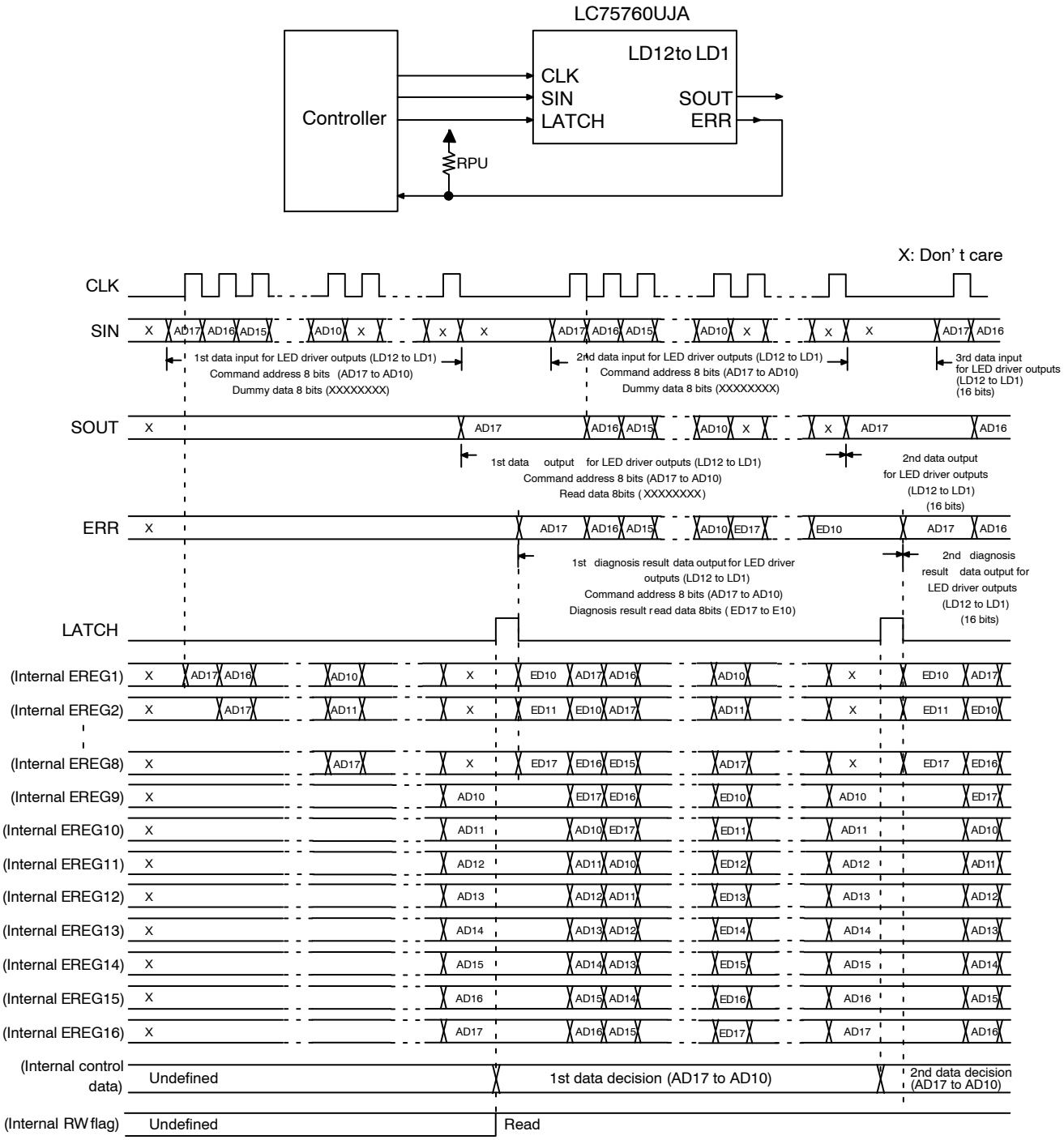


Figure 11. Serial Data Transfer Example of Reading the Diagnosis Result Data from the ERR Pin

List of Control Data

Table 1. LIST OF WRITE COMMAND CONTROL REGISTERS

Command Name	RW	Command Address								Write Data							
		ADn7	ADn6	ADn5	ADn4	ADn3	ADn2	ADn1	ADn0	WDn7	WDn6	WDn5	WDn4	WDn3	WDn2	WDn1	WDn0
Write output current regulation (LD1)	W	0	0	0	0	0	0	0	1	CA17	CA16	CA15	CA14	CA13	CA12	CA11	CA10
Write output current regulation (LD2)	W	0	0	0	0	0	0	1	0	CA27	CA26	CA25	CA24	CA23	CA22	CA21	CA20
Write output current regulation (LD3)	W	0	0	0	0	0	0	1	1	CA37	CA36	CA35	CA34	CA33	CA32	CA31	CA30
Write output current regulation (LD4)	W	0	0	0	0	0	1	0	0	CA47	CA46	CA45	CA44	CA43	CA42	CA41	CA40
Write output current regulation (LD5)	W	0	0	0	0	0	1	0	1	CA57	CA56	CA55	CA54	CA53	CA52	CA51	CA50
Write output current regulation (LD6)	W	0	0	0	0	0	1	1	0	CA67	CA66	CA65	CA64	CA63	CA62	CA61	CA60
Write output current regulation (LD7)	W	0	0	0	0	0	1	1	1	CA77	CA76	CA75	CA74	CA73	CA72	CA71	CA70
Write output current regulation (LD8)	W	0	0	0	0	1	0	0	0	CA87	CA86	CA85	CA84	CA83	CA82	CA81	CA80
Write output current regulation (LD9)	W	0	0	0	0	1	0	0	1	CA97	CA96	CA95	CA94	CA93	CA92	CA91	CA90
Write output current regulation (LD10)	W	0	0	0	0	1	0	1	0	CA107	CA106	CA105	CA104	CA103	CA102	CA101	CA100
Write output current regulation (LD11)	W	0	0	0	0	1	0	1	1	CA117	CA116	CA115	CA114	CA113	CA112	CA111	CA110
Write output current regulation (LD12)	W	0	0	0	0	1	1	0	0	CA127	CA126	CA125	CA124	CA123	CA122	CA121	CA120
Write PWM Ch (LD1,LD2)	W	0	0	0	0	1	1	0	1	x	x	L2C	L2B	L2A	L1C	L1B	L1A
Write PWM Ch (LD3,LD4)	W	0	0	0	0	1	1	1	0	x	x	L4C	L4B	L4A	L3C	L3B	L3A
Write PWM Ch (LD5,LD6)	W	0	0	0	0	1	1	1	1	x	x	L6C	L6B	L6A	L5C	L5B	L5A
Write PWM Ch (LD7,LD8)	W	0	0	0	1	0	0	0	0	x	x	L8C	L8B	L8A	L7C	L7B	L7A
Write PWM Ch (LD9,LD10)	W	0	0	0	1	0	0	0	1	x	x	L10C	L10B	L10A	L9C	L9B	L9A
Write PWM Ch (LD11,LD12)	W	0	0	0	1	0	0	1	0	x	x	L12C	L12B	L12A	L11C	L11B	L11A
Write PWM steps & PWM frame frequency	W	0	0	0	1	0	0	1	1	x	x	PF3	PF2	PF1	PF0	WN1	WN0
Write PWM data (ch1−1)	W	0	0	0	1	0	1	0	0	x	W19	W18	W17	W16	W15	W14	W13
Write PWM data (ch1−2)	W	0	0	0	1	0	1	0	1	x	x	x	x	x	W12	W11	W10
Write PWM data (ch2−1)	W	0	0	0	1	0	1	1	0	x	W29	W28	W27	W26	W25	W24	W23
Write PWM data (ch2−2)	W	0	0	0	1	0	1	1	1	x	x	x	x	x	W22	W21	W20
Write PWM data (ch3−1)	W	0	0	0	1	1	0	0	0	x	W39	W38	W37	W36	W35	W34	W33
Write PWM data (ch3−2)	W	0	0	0	1	1	0	0	1	x	x	x	x	x	W32	W31	W30
Write PWM data (ch4−1)	W	0	0	0	1	1	0	1	0	x	W49	W48	W47	W46	W45	W44	W43
Write PWM data (ch4−2)	W	0	0	0	1	1	0	1	1	x	x	x	x	x	W42	W41	W40
Write PWM data (ch5−1)	W	0	0	0	1	1	1	0	0	x	W59	W58	W57	W56	W55	W54	W53
Write PWM data (ch5−2)	W	0	0	0	1	1	1	0	1	x	x	x	x	x	W52	W51	W50
Write PWM data (ch6−1)	W	0	0	0	1	1	1	1	0	x	W69	W68	W67	W66	W65	W64	W63
Write PWM data (ch6−2)	W	0	0	0	1	1	1	1	1	x	x	x	x	x	W62	W61	W60
Write LED driver output mask 1	W	0	0	1	0	0	0	0	0	x	x	MLD6	MLD5	MLD4	MLD3	MLD2	MLD1

Table 1. LIST OF WRITE COMMAND CONTROL REGISTERS (continued)

Command Name	RW	Command Address								Write Data							
		ADn7	ADn6	ADn5	ADn4	ADn3	ADn2	ADn1	ADn0	WDn7	WDn6	WDn5	WDn4	WDn3	WDn2	WDn1	WDn0
Write LED driver output mask 2	W	0	0	1	0	0	0	0	1	x	x	MLD12	MLD11	MLD10	MLD9	MLD8	MLD7
Write VLED short detection circuit mask 1	W	0	0	1	0	0	0	1	0	x	x	MSH6	MSH5	MSH4	MSH3	MSH2	MSH1
Write VLED short detection circuit mask 2	W	0	0	1	0	0	0	1	1	x	x	MSH12	MSH11	MSH10	MSH9	MSH8	MSH7
Write VSS short detection circuit mask 1	W	0	0	1	0	0	1	0	0	x	x	MSL6	MSL5	MSL4	MSL3	MSL2	MSL1
Write VSS short detection circuit mask 2	W	0	0	1	0	0	1	0	1	x	x	MSL12	MSL11	MSL10	MSL9	MSL8	MSL7
Write open detection circuit mask 1	W	0	0	1	0	0	1	1	0	x	x	MOP6	MOP5	MOP4	MOP3	MOP2	MOP1
Write open detection circuit mask 2	W	0	0	1	0	0	1	1	1	x	x	MOP12	MOP11	MOP10	MOP9	MOP8	MOP7
Write VLED short detection voltage setting 1	W	0	0	1	0	1	0	0	0	VSH4B	VSH4A	VSH3B	VSH3A	VSH2B	VSH2A	VSH1B	VSH1A
Write VLED short detection voltage setting 2	W	0	0	1	0	1	0	0	1	VSH8B	VSH8A	VSH7B	VSH7A	VSH6B	VSH6A	VSH5B	VSH5A
Write VLED short detection voltage setting 3	W	0	0	1	0	1	0	1	0	VSH 12B	VSH 12A	VSH 11B	VSH 11A	VSH 10B	VSH 10A	VSH9B	VSH9A
Write control data 1	W	0	0	1	0	1	0	1	1	x	x	ERD	SR	EXF	OC	TSDN	PLDT
Write control data 2	W	0	0	1	0	1	1	0	0	x	MKAJ	MKOP	MKSL	MKSH	MKIR	VLS1	VLS0
(Unused)	W	0	0	1	0	1	1	0	1	x	x	x	x	x	x	x	x
:		:								:							
(Unused)	W	0	0	1	1	0	0	0	0	x	x	x	x	x	x	x	x
Lock of output current regulation	W	0	0	1	1	0	0	0	1	x	x	x	x	x	x	x	x
Lock of the PWM ch & PWM steps & PWM frame frequency	W	0	0	1	1	0	0	1	0	x	x	x	x	x	x	x	x
Lock of the PWM data	W	0	0	1	1	0	0	1	1	x	x	x	x	x	x	x	x
Lock of LED driver output mask/open/ short	W	0	0	1	1	0	1	0	0	x	x	x	x	x	x	x	x
Lock of control data 1 & control data 2	W	0	0	1	1	0	1	0	1	x	x	x	x	x	x	x	x
Unlock of output current regulation	W	0	0	1	1	0	1	1	0	x	x	x	x	x	x	x	x
Unlock of the PWM ch & PWM steps & PWM frame frequency	W	0	0	1	1	0	1	1	1	x	x	x	x	x	x	x	x
Unlock of the PWM data	W	0	0	1	1	1	0	0	0	x	x	x	x	x	x	x	x
Unlock of LED driver output mask/open/ short	W	0	0	1	1	1	0	0	1	x	x	x	x	x	x	x	x
Unlock of control data 1 & control data 2	W	0	0	1	1	1	0	1	0	x	x	x	x	x	x	x	x
Reset POR flag	W	0	0	1	1	1	0	1	1	x	x	x	x	x	x	x	x
Reset Status flag	W	0	0	1	1	1	1	0	0	x	x	x	x	x	x	x	x
Software reset	W	0	0	1	1	1	1	0	1	x	x	x	x	x	x	x	x
Clearing of the fundamental clock abnormality	W	0	0	1	1	1	1	1	0	x	x	x	x	x	x	x	x
Check of the fundamental clock abnormality	W	0	0	1	1	1	1	1	1	x	x	x	x	x	x	x	x
(Unused)	W	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x
:		:								:							
(Unused)	W	0	1	1	1	1	1	1	1	x	x	x	x	x	x	x	x

8. n: The number of the connection, x: Don’t care.

Table 2. LIST OF READ COMMAND CONTROL REGISTERS

Command Name	RW	Command Address								Read Data							
		ADn7	ADn6	ADn5	ADn4	ADn3	ADn2	ADn1	ADn0	RDn7	RDn6	RDn5	RDn4	RDn3	RDn2	RDn1	RDn0
Read output current regulation (LD1)	R	1	0	0	0	0	0	0	1	CA17	CA16	CA15	CA14	CA13	CA12	CA11	CA10
Read output current regulation (LD2)	R	1	0	0	0	0	0	1	0	CA27	CA26	CA25	CA24	CA23	CA22	CA21	CA20
Read output current regulation (LD3)	R	1	0	0	0	0	0	1	1	CA37	CA36	CA35	CA34	CA33	CA32	CA31	CA30
Read output current regulation (LD4)	R	1	0	0	0	0	1	0	0	CA47	CA46	CA45	CA44	CA43	CA42	CA41	CA40
Read output current regulation (LD5)	R	1	0	0	0	0	1	0	1	CA57	CA56	CA55	CA54	CA53	CA52	CA51	CA50
Read output current regulation (LD6)	R	1	0	0	0	0	1	1	0	CA67	CA66	CA65	CA64	CA63	CA62	CA61	CA60
Read output current regulation (LD7)	R	1	0	0	0	0	1	1	1	CA77	CA76	CA75	CA74	CA73	CA72	CA71	CA70
Read output current regulation (LD8)	R	1	0	0	0	1	0	0	0	CA87	CA86	CA85	CA84	CA83	CA82	CA81	CA80
Read output current regulation (LD9)	R	1	0	0	0	1	0	0	1	CA97	CA96	CA95	CA94	CA93	CA92	CA91	CA90
Read output current regulation (LD10)	R	1	0	0	0	1	0	1	0	CA107	CA106	CA105	CA104	CA103	CA102	CA101	CA100
Read output current regulation (LD11)	R	1	0	0	0	1	0	1	1	CA117	CA116	CA115	CA114	CA113	CA112	CA111	CA110
Read output current regulation (LD12)	R	1	0	0	0	1	1	0	0	CA127	CA126	CA125	CA124	CA123	CA122	CA121	CA120
Read PWM ch (LD1,LD2)	R	1	0	0	0	1	1	0	1	0	0	L2C	L2B	L2A	L1C	L1B	L1A
Read PWM ch (LD3,LD4)	R	1	0	0	0	1	1	1	0	0	0	L4C	L4B	L4A	L3C	L3B	L3A
Read PWM ch (LD5,LD6)	R	1	0	0	0	1	1	1	1	0	0	L6C	L6B	L6A	L5C	L5B	L5A
Read PWM ch (LD7,LD8)	R	1	0	0	1	0	0	0	0	0	0	L8C	L8B	L8A	L7C	L7B	L7A
Read PWM ch (LD9,LD10)	R	1	0	0	1	0	0	0	1	0	0	L10C	L10B	L10A	L9C	L9B	L9A
Read PWM ch (LD11,LD12)	R	1	0	0	1	0	0	1	0	0	0	L12C	L12B	L12A	L11C	L11B	L11A
Read PWM steps & PWM frame frequency	R	1	0	0	1	0	0	1	1	0	0	PF3	PF2	PF1	PF0	WN1	WN0
Read PWM data (ch1−1)	R	1	0	0	1	0	1	0	0	0	W19	W18	W17	W16	W15	W14	W13
Read PWM data (ch1−2)	R	1	0	0	1	0	1	0	1	0	0	0	0	0	W12	W11	W10
Read PWM data (ch2−1)	R	1	0	0	1	0	1	1	0	0	W29	W28	W27	W26	W25	W24	W23
Read PWM data (ch2−2)	R	1	0	0	1	0	1	1	1	0	0	0	0	0	W22	W21	W20
Read PWM data (ch3−1)	R	1	0	0	1	1	0	0	0	0	W39	W38	W37	W36	W35	W34	W33
Read PWM data (ch3−2)	R	1	0	0	1	1	0	0	1	0	0	0	0	0	W32	W31	W30
Read PWM data (ch4−1)	R	1	0	0	1	1	0	1	0	0	W49	W48	W47	W46	W45	W44	W43
Read PWM data (ch4−2)	R	1	0	0	1	1	0	1	1	0	0	0	0	0	W42	W41	W40
Read PWM data (ch5−1)	R	1	0	0	1	1	1	0	0	0	W59	W58	W57	W56	W55	W54	W53
Read PWM data (ch5−2)	R	1	0	0	1	1	1	0	1	0	0	0	0	0	W52	W51	W50
Read PWM data (ch6−1)	R	1	0	0	1	1	1	1	0	0	W69	W68	W67	W66	W65	W64	W63
Read PWM data (ch6−2)	R	1	0	0	1	1	1	1	1	0	0	0	0	0	W62	W61	W60
Read LED driver output mask 1	R	1	0	1	0	0	0	0	0	0	0	MLD6	MLD5	MLD4	MLD3	MLD2	MLD1
Read LED driver output mask 2	R	1	0	1	0	0	0	0	1	0	0	MLD12	MLD11	MLD10	MLD9	MLD8	MLD7

Table 2. LIST OF READ COMMAND CONTROL REGISTERS (continued)

Command Name	RW	Command Address								Read Data							
		ADn7	ADn6	ADn5	ADn4	ADn3	ADn2	ADn1	ADn0	RDn7	RDn6	RDn5	RDn4	RDn3	RDn2	RDn1	RDn0
Read VLED short detection circuit mask 1	R	1	0	1	0	0	0	1	0	0	0	MSH6	MSH5	MSH4	MSH3	MSH2	MSH1
Read VLED short detection circuit mask 2	R	1	0	1	0	0	0	1	1	0	0	MSH12	MSH11	MSH10	MSH9	MSH8	MSH7
Read VSS short detection circuit mask 1	R	1	0	1	0	0	1	0	0	0	0	MSL6	MSL5	MSL4	MSL3	MSL2	MSL1
Read VSS short detection circuit mask 2	R	1	0	1	0	0	1	0	1	0	0	MSL12	MSL11	MSL10	MSL9	MSL8	MSL7
Read open detection circuit mask 1	R	1	0	1	0	0	1	1	0	0	0	MOP6	MOP5	MOP4	MOP3	MOP2	MOP1
Read open detection circuit mask 2	R	1	0	1	0	0	1	1	1	0	0	MOP12	MOP11	MOP10	MOP9	MOP8	MOP7
Read VLED short detection voltage setting 1	R	1	0	1	0	1	0	0	0	VSH4B	VSH4A	VSH3B	VSH3A	VSH2B	VSH2A	VSH1B	VSH1A
Read VLED short detection voltage setting 2	R	1	0	1	0	1	0	0	1	VSH8B	VSH8A	VSH7B	VSH7A	VSH6B	VSH6A	VSH5B	VSH5A
Read VLED short detection voltage setting 3	R	1	0	1	0	1	0	1	0	VSH 12B	VSH 12A	VSH 11B	VSH 11A	VSH 10B	VSH 10A	VSH9B	VSH9A
Read control data 1	R	1	0	1	0	1	0	1	1	0	0	ERD	SR	EXF	OC	TSDN	PLDT
Read control data 2	R	1	0	1	0	1	1	0	0	0	MKAJ	MKOP	MKSL	MKSH	MKIR	VLS1	VLS0
(Unused)	R	1	0	1	0	1	1	0	1	x	x	x	x	x	x	x	x
:		:								:							
(Unused)	R	1	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x
Read Status flag 1	R	1	1	0	0	0	0	0	1	POR	CERR	VERR	AERR	OERR	SERR	TSD150	TSD125
Read Status flag 2	R	1	1	0	0	0	0	1	0	0	0	0	R_LOCK	W_LOCK	P_LOCK	M_LOCK	C_LOCK
Read External resistance diagnosis result	R	1	1	0	0	0	0	1	1	0	0	0	0	0	0	IR1	IR0
Read VLED short detection result 1	R	1	1	0	0	0	1	0	0	0	0	RSH6	RSH5	RSH4	RSH3	RSH2	RSH1
Read VLED short detection result 2	R	1	1	0	0	0	1	0	1	0	0	RSH12	RSH11	RSH10	RSH9	RSH8	RSH7
Read VSS short detection result 1	R	1	1	0	0	0	1	1	0	0	0	RSL6	RSL5	RSL4	RSL3	RSL2	RSL1
Read VSS short detection result 2	R	1	1	0	0	0	1	1	1	0	0	RSL12	RSL11	RSL10	RSL9	RSL8	RSL7
Read open detection result 1	R	1	1	0	0	1	0	0	0	0	0	ROP6	ROP5	ROP4	ROP3	ROP2	ROP1
Read open detection result 2	R	1	1	0	0	1	0	0	1	0	0	ROP12	ROP11	ROP10	ROP9	ROP8	ROP7
Read adjacent outputs short detection result 1	R	1	1	0	0	1	0	1	0	0	0	RAJ6	RAJ5	RAJ4	RAJ3	RAJ2	RAJ1
Read adjacent outputs short detection result 2	R	1	1	0	0	1	0	1	1	0	0	RAJ12	RAJ11	RAJ10	RAJ9	RAJ8	RAJ7
Read the state data of the LED driver output 1	R	1	1	0	0	1	1	0	0	0	0	RLD6	RLD5	RLD4	RLD3	RLD2	RLD1
Read the state data of the LED driver output 2	R	1	1	0	0	1	1	0	1	0	0	RLD12	RLD11	RLD10	RLD9	RLD8	RLD7
(Unused)	R	1	1	0	0	1	1	1	0	x	x	x	x	x	x	x	x
(Unused)	R	1	1	0	0	1	1	1	1	x	x	x	x	x	x	x	x
:		:								:							
(Unused)	R	1	1	1	1	1	1	1	1	x	x	x	x	x	x	x	x

9. n: The number of the connection, x: Don't care.

Control Data Functions

(1) CA17 to CA10, CA27 to CA20, CA37 to CA30, CA47 to CA40, CA57 to CA50, CA67 to CA60, CA77 to CA70, CA87 to CA80, CA97 to CA90, CA107 to CA100, CA117 to CA110, CA127 to CA120 • • • Control Data for Current Value (ID) Setting of the LED Driver Output

By these control data, the current value(ID) of the LED driver output (LD1 to LD12) is set in each ch. Reference current (IREF) is decided by an external resistor connected to IREF pin, and peak output current (IDmax) of the LED driver output is IREF x 500. In addition, these control data are protected by the command [Lock of output current regulation]. It cannot change these control data when the command [Lock of output current regulation] is set. When changing these control data, transmit the command [Unlock of output current regulation]. Afterwards set these control data. These control data are initialized to "(CAn7, CAn6, CAn5, CAn4, CAn3, CAn2, CAn1, CAn0) = (0, 0, 0, 0, 0, 0, 0, 0)" all by the reset action (reset by $\overline{RES}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

CA-n7	CA-n6	CA-n5	CA-n4	CA-n3	CA-n2	CA-n1	CA-n0	Output Current Value (ID)
0	0	0	0	0	0	0	0	(1/256) x (I_{REF} x 500)
0	0	0	0	0	0	0	1	(2/256) x (I_{REF} x 500)
0	0	0	0	0	0	1	0	(3/256) x (I_{REF} x 500)
0	0	0	0	0	0	1	1	(4/256) x (I_{REF} x 500)
0	0	0	0	0	1	0	0	(5/256) x (I_{REF} x 500)
0	0	0	0	0	1	0	1	(6/256) x (I_{REF} x 500)
0	0	0	0	0	1	1	0	(7/256) x (I_{REF} x 500)
0	0	0	0	0	1	1	1	(8/256) x (I_{REF} x 500)
0	0	0	0	1	0	0	0	(9/256) x (I_{REF} x 500)
0	0	0	0	1	0	0	1	(10/256) x (I_{REF} x 500)
0	0	0	0	1	0	1	0	(11/256) x (I_{REF} x 500)
0	0	0	0	1	0	1	1	(12/256) x (I_{REF} x 500)
0	0	0	0	1	1	0	0	(13/256) x (I_{REF} x 500)
0	0	0	0	1	1	0	1	(14/256) x (I_{REF} x 500)
0	0	0	0	1	1	1	0	(15/256) x (I_{REF} x 500)
0	0	0	0	1	1	1	1	(16/256) x (I_{REF} x 500)
:	:	:	:	:	:	:	:	:
0	1	1	1	0	0	0	0	(113/256) x (I_{REF} x 500)
0	1	1	1	0	0	0	1	(114/256) x (I_{REF} x 500)
0	1	1	1	0	0	1	0	(115/256) x (I_{REF} x 500)
0	1	1	1	0	0	1	1	(116/256) x (I_{REF} x 500)
0	1	1	1	0	1	0	0	(117/256) x (I_{REF} x 500)
0	1	1	1	0	1	0	1	(118/256) x (I_{REF} x 500)
0	1	1	1	0	1	1	0	(119/256) x (I_{REF} x 500)
0	1	1	1	0	1	1	1	(120/256) x (I_{REF} x 500)
0	1	1	1	1	0	0	0	(121/256) x (I_{REF} x 500)
0	1	1	1	1	0	0	1	(122/256) x (I_{REF} x 500)
0	1	1	1	1	0	1	0	(123/256) x (I_{REF} x 500)
0	1	1	1	1	0	1	1	(124/256) x (I_{REF} x 500)
0	1	1	1	1	1	0	0	(125/256) x (I_{REF} x 500)
0	1	1	1	1	1	0	1	(126/256) x (I_{REF} x 500)
0	1	1	1	1	1	1	0	(127/256) x (I_{REF} x 500)
0	1	1	1	1	1	1	1	(128/256) x (I_{REF} x 500)

CA-n7	CA-n6	CA-n5	CA-n4	CA-n3	CA-n2	CA-n1	CA-n0	Output Current Value (ID)
1	0	0	0	0	0	0	0	(129/256) x (I_{REF} x 500)
1	0	0	0	0	0	0	1	(130/256) x (I_{REF} x 500)
1	0	0	0	0	0	1	0	(131/256) x (I_{REF} x 500)
1	0	0	0	0	0	1	1	(132/256) x (I_{REF} x 500)
1	0	0	0	0	1	0	0	(133/256) x (I_{REF} x 500)
1	0	0	0	0	1	0	1	(134/256) x (I_{REF} x 500)
1	0	0	0	0	1	1	0	(135/256) x (I_{REF} x 500)
1	0	0	0	0	1	1	1	(136/256) x (I_{REF} x 500)
1	0	0	0	1	0	0	0	(137/256) x (I_{REF} x 500)
1	0	0	0	1	0	0	1	(138/256) x (I_{REF} x 500)
1	0	0	0	1	0	1	0	(139/256) x (I_{REF} x 500)
1	0	0	0	1	0	1	1	(140/256) x (I_{REF} x 500)
1	0	0	0	1	1	0	0	(141/256) x (I_{REF} x 500)
1	0	0	0	1	1	0	1	(142/256) x (I_{REF} x 500)
1	0	0	0	1	1	1	0	(143/256) x (I_{REF} x 500)
1	0	0	0	1	1	1	1	(144/256) x (I_{REF} x 500)
:	:	:	:	:	:	:	:	:
1	1	1	1	0	0	0	0	(241/256) x (I_{REF} x 500)
1	1	1	1	0	0	0	1	(242/256) x (I_{REF} x 500)
1	1	1	1	0	0	1	0	(243/256) x (I_{REF} x 500)
1	1	1	1	0	0	1	1	(244/256) x (I_{REF} x 500)
1	1	1	1	0	1	0	0	(245/256) x (I_{REF} x 500)
1	1	1	1	0	1	0	1	(246/256) x (I_{REF} x 500)
1	1	1	1	0	1	1	0	(247/256) x (I_{REF} x 500)
1	1	1	1	0	1	1	1	(248/256) x (I_{REF} x 500)
1	1	1	1	1	0	0	0	(249/256) x (I_{REF} x 500)
1	1	1	1	1	0	0	1	(250/256) x (I_{REF} x 500)
1	1	1	1	1	0	1	0	(251/256) x (I_{REF} x 500)
1	1	1	1	1	0	1	1	(252/256) x (I_{REF} x 500)
1	1	1	1	1	1	0	0	(253/256) x (I_{REF} x 500)
1	1	1	1	1	1	0	1	(254/256) x (I_{REF} x 500)
1	1	1	1	1	1	1	0	(255/256) x (I_{REF} x 500)
1	1	1	1	1	1	1	1	(256/256) x (I_{REF} x 500)

10. CA17 to CA10: Data for current value setting of the LED driver output (LD1) /
CA27 to CA20: Data for current value setting of the LED driver output (LD2) /
CA37 to CA30: Data for current value setting of the LED driver output (LD3) /
CA47 to CA40: Data for current value setting of the LED driver output (LD4) /
CA57 to CA50: Data for current value setting of the LED driver output (LD5) /
CA67 to CA60: Data for current value setting of the LED driver output (LD6) /
CA77 to CA70: Data for current value setting of the LED driver output (LD7) /
CA87 to CA80: Data for current value setting of the LED driver output (LD8) /
CA97 to CA90: Data for current value setting of the LED driver output (LD9) /
CA107 to CA100: Data for current value setting of the LED driver output (LD10) /
CA117 to CA110: Data for current value setting of the LED driver output (LD11) /
CA127 to CA120: Data for current value setting of the LED driver output (LD12)

(2) L1C, L1B, L1A to L12C, L12B, L12A • • • Control Data for Ch Setting of the PWM Circuits that Adjust Brightness of LED

By these control data, the PWM circuit of the LED driver output is set in each Ch. In addition, these control data are protected by the command [Lock of the PWM ch & PWM steps & PWM frame frequency]. It cannot change these control data when the command [Lock of the PWM ch & PWM steps & PWM frame frequency] is set. When changing these control data, transmit the command [Unlock of the PWM ch & PWM steps & PWM frame frequency]. Afterwards set these control data. These control data are initialized to "(LnC, LnB, LnA) = (0, 0, 1)" all by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

LnC	LnB	LnA	Ch of the PWM Circuit for LED Driver Output LDn
0	0	0	PWM circuit is not selected. (The setting of turning on/off of the duty 100% is possible.)
0	0	1	PWM circuit (Ch1) is selected.
0	1	0	PWM circuit (Ch2) is selected.
0	1	1	PWM circuit (Ch3) is selected.
1	0	0	PWM circuit (Ch4) is selected.
1	0	1	PWM circuit (Ch5) is selected.
1	1	0	PWM circuit (Ch6) is selected.
1	1	1	PWM circuit is not selected. (The setting of turning on/off of the duty 100% is possible.)

11. LnC, LnB, LnA (n = 1 to 12) data are control data that set the Ch of PWM circuit for LED driver output pins LDn (n = 1 to 12).
For example, if (L1C, L1B, L1A) = (0, 0, 1), (L5C, L5B, L5A) = (0, 1, 1) and (L10C, L10B, L10A) = (1, 1, 0) is set, LED driver output pin LD1 select PWM circuit (Ch1) and LED driver output pin LD5 select PWM circuit (Ch3) and LED driver output pin LD10 select PWM circuit (Ch6).

(3) WN1, WN0 • • • Control Data for Setting of the Resolution Number of PWM Steps of LED Driver Output Waveform

These control data bits set the steps number of PWM output (Ch1 to Ch6) of LED driver outputs (LD1 to LD12). In other word, they set the number of effective bits of PWM data. In addition, these control data are protected by the command [Lock of the PWM ch & PWM steps & PWM frame frequency]. It cannot change these control data when the command [Lock of the PWM ch & PWM steps & PWM frame frequency] is set. When changing these control data, transmit the command [Unlock of the PWM ch & PWM steps & PWM frame frequency]. Afterwards set these control data. These control data are initialized to "(WN1, WN0) = (0, 0)" by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

WN1	WN0	The Steps Number of PWM Output (Ch1 to Ch6) of LED Driver Outputs LDn	The Number of Effective Bits of PWM Data per One Channel of PWM Data
0	0	128 steps	7 bits (Wn9 to Wn3)
0	1	256 steps	8 bits (Wn9 to Wn2)
1	0	512 steps	9 bits (Wn9 to Wn1)
1	1	1024 steps	10 bits (Wn9 to Wn0)

12. W19 to W10: PWM data of PWM circuit (Ch1) / W29 to W20: PWM data of PWM circuit (Ch2)
W39 to W30: PWM data of PWM circuit (Ch3) / W49 to W40: PWM data of PWM circuit (Ch4)
W59 to W50: PWM data of PWM circuit (Ch5) / W69 to W60: PWM data of PWM circuit (Ch6)

(4) PF3 to PF0 • • • Control Data for Setting of the Frame Frequency of PWM Output Waveform

These control data bits set the frame frequency of PWM output waveform of LED driver outputs (LD1 to LD12) setting PWM circuits (Ch1 to Ch6). In addition, these control data are protected by the command [Lock of the PWM ch & PWM steps & PWM frame frequency]. It cannot change these control data when the command [Lock of the PWM ch & PWM steps & PWM frame frequency] is set. When changing these control data, transmit the command [Unlock of the PWM ch & PWM steps & PWM frame frequency]. Afterwards set these control data. These control data are initialized to "(PF3, PF2, PF1, PF0) = (1, 0, 0, 0)" all by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

PF3	PF2	PF1	PF0	Frame Frequency of PWM Output Waveform of LED Driver Outputs fp [Hz]		The Number of the Settable Steps of the PWM Circuit			
				Internal Oscillator Operating Mode (Control Data OC = "0")	External Clock Operating Mode (Control Data OC = "1")	128 Steps	256 Steps	512 Steps	1024 Steps
0	0	0	0	fosc / 2048	$f_{OSCI}1,2$ / 2048	Y	Y	Y	Y
0	0	0	1	fosc / 1920	$f_{OSCI}1,2$ / 1920	Y	N	N	N
0	0	1	0	fosc / 1792	$f_{OSCI}1,2$ / 1792	Y	Y	N	N
0	0	1	1	fosc / 1664	$f_{OSCI}1,2$ / 1664	Y	N	N	N
0	1	0	0	fosc / 1536	$f_{OSCI}1,2$ / 1536	Y	Y	Y	N
0	1	0	1	fosc / 1408	$f_{OSCI}1,2$ / 1408	Y	N	N	N
0	1	1	0	fosc / 1280	$f_{OSCI}1,2$ / 1280	Y	Y	N	N
0	1	1	1	fosc / 1152	$f_{OSCI}1,2$ / 1152	Y	N	N	N
1	0	0	0	fosc / 1024	$f_{OSCI}1,2$ / 1024	Y	Y	Y	Y
1	0	0	1	fosc / 896	$f_{OSCI}1,2$ / 896	Y	N	N	N
1	0	1	0	fosc / 768	$f_{OSCI}1,2$ / 768	Y	Y	N	N
1	0	1	1	fosc / 640	$f_{OSCI}1,2$ / 640	Y	N	N	N
1	1	0	0	fosc / 512	$f_{OSCI}1,2$ / 512	Y	Y	Y	N

13. Y = "It is possible of setting". N = "It is impossible of setting".
    If the number of steps of PWM circuit will be set to the step which is impossible of setting, it will set smallest resolution in range which is possible of setting. For example, it is as follows.
    - If it will be set to 256 steps or 512 steps or 1024 steps under (128 steps, 256 steps, 512 steps, 1024 steps) = (Y, N, N, N), it will be set to 128 steps.
    - If it will be set to 512 steps or 1024 steps under (128 steps, 256 steps, 512 steps, 1024 steps) = (Y, Y, N, N), it will be set to 256 steps.
    - If it will be set to 1024 steps under (128 steps, 256 steps, 512 steps, 1024 steps) = (Y, Y, Y, N), it will be set to 512 steps.
14. If (PF3, PF2, PF1, PF0) = (1, 1, 0, 1), (1, 1, 1, 0) or (1, 1, 1, 1) are set, the frame frequency (fosc/1024, $f_{OSCI}1,2/1024$) of setting (PF3, PF2, PF1, PF0) = (1, 0, 0, 0) is selected.
15. fosc = 200 kHz (typ) (When it is internal oscillator operating mode with control data OC = "0".)
    $f_{OSCI}1$ = 200 kHz (typ) (When it is external clock operating mode with control data OC = "1", EXF = "0".)
    $f_{OSCI}2$ = 150 kHz (typ) (When it is external clock operating mode with control data OC = "1", EXF = "1".)

(5) W19 to W10, W29 to W20, W39 to W30, W49 to W40, W59 to W50, W69 to W60 • • • PWM Data of PWM Circuits of the LED Driver Outputs

These control data bits set LED lighting time per one frame of the PWM output waveform of the LED driver outputs (LD1 to LD12) setting PWM circuits (Ch1 to Ch6) separately. In addition, these control data are protected by the command [Lock of the PWM data]. It cannot change these control data when the command [Lock of the PWM data] is set. When changing these control data, transmit the command [Unlock of the PWM data]. Afterwards set these control data.

These control data are initialized to "(Wm9, Wm8, Wm7, Wm6, Wm5, Wm4, Wm3, Wm2, Wm1, Wm0) = (0, 0, 0, 0, 0, 0, 0, 0, 0, 0)" all by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

PWM Data										LED Lighting Time per One Frame			
Wm9	Wm8	Wm7	Wm6	Wm5	Wm4	Wm3	Wm2	Wm1	Wm0	1024 Steps	512 Steps	256 Steps	128 Steps
0	0	0	0	0	0	0	0	0	0	(1/1024) x Tp	(1/512) x Tp	(1/256) x Tp	(1/128) x Tp
0	0	0	0	0	0	0	0	0	1	(2/1024) x Tp	(1/512) x Tp	(1/256) x Tp	(1/128) x Tp
0	0	0	0	0	0	0	0	1	0	(3/1024) x Tp	(2/512) x Tp	(1/256) x Tp	(1/128) x Tp
0	0	0	0	0	0	0	0	1	1	(4/1024) x Tp	(2/512) x Tp	(1/256) x Tp	(1/128) x Tp
0	0	0	0	0	0	0	1	0	0	(5/1024) x Tp	(3/512) x Tp	(2/256) x Tp	(1/128) x Tp
0	0	0	0	0	0	0	1	0	1	(6/1024) x Tp	(3/512) x Tp	(2/256) x Tp	(1/128) x Tp
0	0	0	0	0	0	0	1	1	0	(7/1024) x Tp	(4/512) x Tp	(2/256) x Tp	(1/128) x Tp
0	0	0	0	0	0	0	1	1	1	(8/1024) x Tp	(4/512) x Tp	(2/256) x Tp	(1/128) x Tp
0	0	0	0	0	0	1	0	0	0	(9/1024) x Tp	(5/512) x Tp	(3/256) x Tp	(2/128) x Tp
0	0	0	0	0	0	1	0	0	1	(10/1024) x Tp	(5/512) x Tp	(3/256) x Tp	(2/128) x Tp
0	0	0	0	0	0	1	0	1	0	(11/1024) x Tp	(6/512) x Tp	(3/256) x Tp	(2/128) x Tp
0	0	0	0	0	0	1	0	1	1	(12/1024) x Tp	(6/512) x Tp	(3/256) x Tp	(2/128) x Tp
0	0	0	0	0	0	1	1	0	0	(13/1024) x Tp	(7/512) x Tp	(4/256) x Tp	(2/128) x Tp
0	0	0	0	0	0	1	1	0	1	(14/1024) x Tp	(7/512) x Tp	(4/256) x Tp	(2/128) x Tp
0	0	0	0	0	0	1	1	1	0	(15/1024) x Tp	(8/512) x Tp	(4/256) x Tp	(2/128) x Tp
0	0	0	0	0	0	1	1	1	1	(16/1024) x Tp	(8/512) x Tp	(4/256) x Tp	(2/128) x Tp
0	0	0	0	0	1	0	0	0	0	(17/1024) x Tp	(9/512) x Tp	(5/256) x Tp	(3/128) x Tp
0	0	0	0	0	1	0	0	0	1	(18/1024) x Tp	(9/512) x Tp	(5/256) x Tp	(3/128) x Tp
0	0	0	0	0	1	0	0	1	0	(19/1024) x Tp	(10/512) x Tp	(5/256) x Tp	(3/128) x Tp
0	0	0	0	0	1	0	0	1	1	(20/1024) x Tp	(10/512) x Tp	(5/256) x Tp	(3/128) x Tp
0	0	0	0	0	1	0	1	0	0	(21/1024) x Tp	(11/512) x Tp	(6/256) x Tp	(3/128) x Tp
0	0	0	0	0	1	0	1	0	1	(22/1024) x Tp	(11/512) x Tp	(6/256) x Tp	(3/128) x Tp
0	0	0	0	0	1	0	1	1	0	(23/1024) x Tp	(12/512) x Tp	(6/256) x Tp	(3/128) x Tp
0	0	0	0	0	1	0	1	1	1	(24/1024) x Tp	(12/512) x Tp	(6/256) x Tp	(3/128) x Tp
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	0	0	(509/1024) x Tp	(255/512) x Tp	(128/256) x Tp	(64/128) x Tp
0	1	1	1	1	1	1	1	0	1	(510/1024) x Tp	(255/512) x Tp	(128/256) x Tp	(64/128) x Tp
0	1	1	1	1	1	1	1	1	0	(511/1024) x Tp	(256/512) x Tp	(128/256) x Tp	(64/128) x Tp
0	1	1	1	1	1	1	1	1	1	(512/1024) x Tp	(256/512) x Tp	(128/256) x Tp	(64/128) x Tp
1	0	0	0	0	0	0	0	0	0	(513/1024) x Tp	(257/512) x Tp	(129/256) x Tp	(65/128) x Tp
1	0	0	0	0	0	0	0	0	1	(514/1024) x Tp	(257/512) x Tp	(129/256) x Tp	(65/128) x Tp
1	0	0	0	0	0	0	0	1	0	(515/1024) x Tp	(258/512) x Tp	(129/256) x Tp	(65/128) x Tp
1	0	0	0	0	0	0	0	1	1	(516/1024) x Tp	(258/512) x Tp	(129/256) x Tp	(65/128) x Tp
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	1	0	0	0	(1001/1024) x Tp	(501/512) x Tp	(251/256) x Tp	(126/128) x Tp
1	1	1	1	1	0	1	0	0	1	(1002/1024) x Tp	(501/512) x Tp	(251/256) x Tp	(126/128) x Tp
1	1	1	1	1	0	1	0	1	0	(1003/1024) x Tp	(502/512) x Tp	(251/256) x Tp	(126/128) x Tp
1	1	1	1	1	0	1	0	1	1	(1004/1024) x Tp	(502/512) x Tp	(251/256) x Tp	(126/128) x Tp
1	1	1	1	1	0	1	1	0	0	(1005/1024) x Tp	(503/512) x Tp	(252/256) x Tp	(126/128) x Tp
1	1	1	1	1	0	1	1	0	1	(1006/1024) x Tp	(503/512) x Tp	(252/256) x Tp	(126/128) x Tp
1	1	1	1	1	0	1	1	1	0	(1007/1024) x Tp	(504/512) x Tp	(252/256) x Tp	(126/128) x Tp

(continued)

PWM Data										LED Lighting Time per One Frame			
Wm9	Wm8	Wm7	Wm6	Wm5	Wm4	Wm3	Wm2	Wm1	Wm0	1024 Steps	512 Steps	256 Steps	128 Steps
1	1	1	1	1	0	1	1	1	1	(1008/1024) x Tp	(504/512) x Tp	(252/256) x Tp	(126/128) x Tp
1	1	1	1	1	1	0	0	0	0	(1009/1024) x Tp	(505/512) x Tp	(253/256) x Tp	(127/128) x Tp
1	1	1	1	1	1	0	0	0	1	(1010/1024) x Tp	(505/512) x Tp	(253/256) x Tp	(127/128) x Tp
1	1	1	1	1	1	0	0	1	0	(1011/1024) x Tp	(506/512) x Tp	(253/256) x Tp	(127/128) x Tp
1	1	1	1	1	1	0	0	1	1	(1012/1024) x Tp	(506/512) x Tp	(253/256) x Tp	(127/128) x Tp
1	1	1	1	1	1	0	1	0	0	(1013/1024) x Tp	(507/512) x Tp	(254/256) x Tp	(127/128) x Tp
1	1	1	1	1	1	0	1	0	1	(1014/1024) x Tp	(507/512) x Tp	(254/256) x Tp	(127/128) x Tp
1	1	1	1	1	1	0	1	1	0	(1015/1024) x Tp	(508/512) x Tp	(254/256) x Tp	(127/128) x Tp
1	1	1	1	1	1	0	1	1	1	(1016/1024) x Tp	(508/512) x Tp	(254/256) x Tp	(127/128) x Tp
1	1	1	1	1	1	1	0	0	0	(1017/1024) x Tp	(509/512) x Tp	(255/256) x Tp	(128/128) x Tp
1	1	1	1	1	1	1	0	0	1	(1018/1024) x Tp	(509/512) x Tp	(255/256) x Tp	(128/128) x Tp
1	1	1	1	1	1	1	0	1	0	(1019/1024) x Tp	(510/512) x Tp	(255/256) x Tp	(128/128) x Tp
1	1	1	1	1	1	1	0	1	1	(1020/1024) x Tp	(510/512) x Tp	(255/256) x Tp	(128/128) x Tp
1	1	1	1	1	1	1	1	0	0	(1021/1024) x Tp	(511/512) x Tp	(256/256) x Tp	(128/128) x Tp
1	1	1	1	1	1	1	1	0	1	(1022/1024) x Tp	(511/512) x Tp	(256/256) x Tp	(128/128) x Tp
1	1	1	1	1	1	1	1	1	0	(1023/1024) x Tp	(512/512) x Tp	(256/256) x Tp	(128/128) x Tp
1	1	1	1	1	1	1	1	1	1	(1024/1024) x Tp	(512/512) x Tp	(256/256) x Tp	(128/128) x Tp

16. W19 to W10: PWM data of PWM circuit (Ch1) / W29 to W20: PWM data of PWM circuit (Ch2) /
W39 to W30: PWM data of PWM circuit (Ch3) / W49 to W40: PWM data of PWM circuit (Ch4) /
W59 to W50: PWM data of PWM circuit (Ch5) / W69 to W60: PWM data of PWM circuit (Ch6) /

$$T_p = \frac{1}{f_p}$$

(6) MLD1 to MLD12 • • • Control Data for LED Driver Output Mask Setting

By these control data, mask setting of the LED driver outputs (LD1 to LD12) is set in each Ch. In addition, these control data are protected by the command [Lock of LED driver output mask/open/short]. It cannot change these control data when the command [Lock of LED driver output mask/open/short] is set. When changing these control data, transmit the command [Unlock of LED driver output mask/open/short]. Afterwards set these control data. These control data are initialized to "(MLDn) = (0)" all by the reset action (reset by $\overline{RES}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

MLDn	State of LED Driver Outputs (LDn)
0	LED is off. (LED driver outputs mask setting)
1	LED is on. (The LED is on by depending on the contents of LnA, LnB, LnC. (n = 1 to 12))

17. MLD1: Data for mask setting of the LED driver output (LD1) / MLD2: Data for mask setting of the LED driver output (LD2) /
MLD3: Data for mask setting of the LED driver output (LD3) / MLD4: Data for mask setting of the LED driver output (LD4) /
MLD5: Data for mask setting of the LED driver output (LD5) / MLD6: Data for mask setting of the LED driver output (LD6) /
MLD7: Data for mask setting of the LED driver output (LD7) / MLD8: Data for mask setting of the LED driver output (LD8) /
MLD9: Data for mask setting of the LED driver output (LD9) / MLD10: Data for mask setting of the LED driver output (LD10) /
MLD11: Data for mask setting of the LED driver output (LD11) / MLD12: Data for mask setting of the LED driver output (LD12)

(7) MSH1 to MSH12 • • • Control Data for VLED Short Detection Circuit Mask Setting of the LED Driver Outputs

By these control data, mask setting of VLED short detection circuit of the LED driver outputs (LD1 to LD12) is set in each Ch. In addition, these control data are protected by the command [Lock of LED driver output mask/open/short]. It cannot change these control data when the command [Lock of LED driver output mask/open/short] is set. When changing these control data, transmit the command [Unlock of LED driver output mask/open/short]. Afterwards set these control data. These control data are initialized to "(MSHn) = (1)" all by the reset action (reset by $\overline{RES}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

MSHn	State of the Operation of the VLED Short Detection Circuit	Status Data (SERR)	Result Data of VLED Short Detection (RSH1 to RSH12)
0	VLED short detection circuit of the corresponding LED driver outputs is separated from LED driver outputs, and VLED short detection is impossible. (VLED short detection circuit mask setting)	The status data (SERR) does not reflect result of VLED short detection of the corresponding LED driver outputs.	RSH1 to RSH12 maintains the result data of VLED short detection detected at the time of MSHn = “1”. RSH1 to RSH12 is initialized to “0” all by the command [Reset status flag].
1	VLED short detection circuit of the corresponding LED driver outputs is connected to the LED driver outputs, and VLED short detection is enabled.	The status data (SERR) reflects a result of VLED short detection of the corresponding LED driver outputs.	RSH1 to RSH12 maintains the result data of VLED short detection of the corresponding LED driver outputs.

18. MSH1: Data for mask setting of the VLED short detecting circuit of LED driver output (LD1) /
MSH2: Data for mask setting of the VLED short detecting circuit of LED driver output (LD2) /
MSH3: Data for mask setting of the VLED short detecting circuit of LED driver output (LD3) /
MSH4: Data for mask setting of the VLED short detecting circuit of LED driver output (LD4) /
MSH5: Data for mask setting of the VLED short detecting circuit of LED driver output (LD5) /
MSH6: Data for mask setting of the VLED short detecting circuit of LED driver output (LD6) /
MSH7: Data for mask setting of the VLED short detecting circuit of LED driver output (LD7) /
MSH8: Data for mask setting of the VLED short detecting circuit of LED driver output (LD8) /
MSH9: Data for mask setting of the VLED short detecting circuit of LED driver output (LD9) /
MSH10: Data for mask setting of the VLED short detecting circuit of LED driver output (LD10) /
MSH11: Data for mask setting of the VLED short detecting circuit of LED driver output (LD11) /
MSH12: Data for mask setting of the VLED short detecting circuit of LED driver output (LD12)

(8) MSL1 to MSL12 • • • Control Data for VSS Short Detection Circuit Mask Setting of the LED Driver Outputs

By these control data, mask setting of VSS short detection circuit of the LED driver outputs (LD1 to LD12) is set in each Ch. In addition, these control data are protected by the command [Lock of LED driver output mask/open/short]. It cannot change these control data when the command [Lock of LED driver output mask/open/short] is set. When changing these control data, transmit the command [Unlock of LED driver output mask/open/short]. Afterwards set these control data. These control data are initialized to “(MSLn) = (1)” all by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

MSLn	State of the Operation of the VSS Short Detection Circuit	Status Data (SERR)	Result Data of VSS Short Detection (RSL1 to RSL12)
0	VSS short detection circuit of the corresponding LED driver outputs is separated from LED driver outputs, and VSS short detection is impossible. (VSS short detection circuit mask setting)	The status data (SERR) does not reflect result of VSS short detection of the corresponding LED driver outputs.	RSL1 to RSL12 maintains the result data of VSS short detection detected at the time of MSLn = “1”. RSL1 to RSL12 is initialized to “0” all by the command [Reset status flag].
1	VSS short detection circuit of the corresponding LED driver outputs is connected to the LED driver outputs, and VSS short detection is enabled.	The status data (SERR) reflects a result of VSS short detection of the corresponding LED driver outputs.	RSL1 to RSL12 maintains the result data of VSS short detection of the corresponding LED driver outputs.

19. MSL1: Data for mask setting of the VSS short detecting circuit of LED driver output (LD1) /
MSL2: Data for mask setting of the VSS short detecting circuit of LED driver output (LD2) /
MSL3: Data for mask setting of the VSS short detecting circuit of LED driver output (LD3) /
MSL4: Data for mask setting of the VSS short detecting circuit of LED driver output (LD4) /
MSL5: Data for mask setting of the VSS short detecting circuit of LED driver output (LD5) /
MSL6: Data for mask setting of the VSS short detecting circuit of LED driver output (LD6) /
MSL7: Data for mask setting of the VSS short detecting circuit of LED driver output (LD7) /
MSL8: Data for mask setting of the VSS short detecting circuit of LED driver output (LD8) /
MSL9: Data for mask setting of the VSS short detecting circuit of LED driver output (LD9) /
MSL10: Data for mask setting of the VSS short detecting circuit of LED driver output (LD10) /
MSL11: Data for mask setting of the VSS short detecting circuit of LED driver output (LD11) /
MSL12: Data for mask setting of the VSS short detecting circuit of LED driver output (LD12)

(9) MOP1 to MOP12 • • • Control Data for Open Detection Circuit Mask Setting of the LED Driver Outputs

By these control data, mask setting of open detection circuit of the LED driver outputs (LD1 to LD12) is set in each Ch. In addition, these control data are protected by the command [Lock of LED driver output mask/open/short]. It cannot change these control data when the command [Lock of LED driver output mask/open/short] is set. When changing these control data, transmit the command [Unlock of LED driver output mask/open/short]. Afterwards set these control data. These control data are initialized to "(MOPn) = (1)" all by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

MOPn	State of the Operation of the Open Detection Circuit	Status Data (OERR)	Result Data of Open Detection (ROP1 to ROP12)
0	Open detection circuit of the corresponding LED driver outputs is separated from LED driver outputs, and open detection is impossible. (Open detection circuit mask setting)	The status data (OERR) does not reflect result of open detection of the corresponding LED driver outputs.	ROP1 to ROP12 maintains the result data of open detection detected at the time of MOPn = "1". ROP1 to ROP12 is initialized to "0" all by the command [Reset status flag].
1	Open detection circuit of the corresponding LED driver outputs is connected to the LED driver outputs, and open detection is enabled.	The status data (OERR) reflects a result of open detection of the corresponding LED driver outputs.	ROP1 to ROP12 maintains the result data of open detection of the corresponding LED driver outputs.

20. MOP1: Data for mask setting of the open detecting circuit of LED driver output (LD1) /
MOP2: Data for mask setting of the open detecting circuit of LED driver output (LD2) /
MOP3: Data for mask setting of the open detecting circuit of LED driver output (LD3) /
MOP4: Data for mask setting of the open detecting circuit of LED driver output (LD4) /
MOP5: Data for mask setting of the open detecting circuit of LED driver output (LD5) /
MOP6: Data for mask setting of the open detecting circuit of LED driver output (LD6) /
MOP7: Data for mask setting of the open detecting circuit of LED driver output (LD7) /
MOP8: Data for mask setting of the open detecting circuit of LED driver output (LD8) /
MOP9: Data for mask setting of the open detecting circuit of LED driver output (LD9) /
MOP10: Data for mask setting of the open detecting circuit of LED driver output (LD10) /
MOP11: Data for mask setting of the open detecting circuit of LED driver output (LD11) /
MOP12: Data for mask setting of the open detecting circuit of LED driver output (LD12)

(10) VSH1B, VSH1A to VSH12B, VSH12A • • • Control Data for VLED Short Detection Voltage Setting of the LED Driver Outputs

By these control data, setting of VLED short detection voltage of the LED driver outputs (LD1 to LD12) is set in each Ch. In addition, these control data are protected by the command [Lock of LED driver output mask/open/short]. It cannot change these control data when the command [Lock of LED driver output mask/open/short] is set. When changing these control data, transmit the command [Unlock of LED driver output mask/open/short]. Afterwards set these control data. These control data are initialized to "(VSHnB, VSHnA) = (0, 0)" all by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

VSHnB	VSHnA	VLED Short Detection Voltage of the LED Driver Outputs (LDn)
0	0	VSH = 0.8 V typ. (When the power supply voltage VDD = 2.7 V to 5.5 V.)
0	1	VSH = 1.8 V typ. (When the power supply voltage VDD = 2.7 V to 5.5 V.)
1	0	VSH = 2.8 V typ. (When the power supply voltage VDD = 4.5 V to 5.5 V.)
1	1	VSH = 3.8 V typ. (When the power supply voltage VDD = 4.5 V to 5.5 V.)

21. VSH1B, VSH1A: Data for setting of the VLED short detection voltage of LED driver output (LD1). /
VSH2B, VSH2A : Data for setting of the VLED short detection voltage of LED driver output (LD2). /
VSH3B, VSH3A : Data for setting of the VLED short detection voltage of LED driver output (LD3). /
VSH4B, VSH4A : Data for setting of the VLED short detection voltage of LED driver output (LD4). /
VSH5B, VSH5A : Data for setting of the VLED short detection voltage of LED driver output (LD5). /
VSH6B, VSH6A : Data for setting of the VLED short detection voltage of LED driver output (LD6). /
VSH7B, VSH7A : Data for setting of the VLED short detection voltage of LED driver output (LD7). /
VSH8B, VSH8A : Data for setting of the VLED short detection voltage of LED driver output (LD8). /
VSH9B, VSH9A : Data for setting of the VLED short detection voltage of LED driver output (LD9). /
VSH10B, VSH10A : Data for setting of the VLED short detection voltage of LED driver output (LD10). /
VSH11B, VSH11A : Data for setting of the VLED short detection voltage of LED driver output (LD11). /
VSH12B, VSH12A : Data for setting of the VLED short detection voltage of LED driver output (LD12).

(11) PLDT • • • Control Data for PWM Duty Setting at the Time of the 125°C Detection with the Temperature Sensor

By this control data, the PWM Duty control at the time of the 125°C detection with the temperature sensor is set. This control data is valid for only LED driver output of the PWM setting. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to "(PLDT) = (0)" by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

PLDT	State of the LED Driver Outputs of the PWM Setting
0	When 125°C or above were detected by a temperature sensor, the PWM output waveform is adjusted automatically. (This LSI halves duty of the PWM outputs waveform to suppress the temperature)
1	Even if 125°C or above are detected by a temperature sensor, the PWM output waveform is not adjusted.

(12) TSDN • • • Control Data for Thermal Shut Down Function Setting

By this control data, the thermal shut down function is set to valid or invalid. At the time of TSDN = "0", a thermal shut down function is valid, and this LSI performs thermal shut down actuating when junction temperature 150°C is detected by a temperature sensor. (The LED driver outputs are forcibly set to the turning off state.) At the time of TSDN = "1", a thermal shut down function is invalid and this LSI does not perform thermal shut down actuating when junction temperature 150°C is detected by a temperature sensor. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to "(TSDN) = (0)" by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET) or software reset) of the system.

TSDN	Thermal Shut Down Function
0	Valid
1	Invalid

(13) OC • • • Control Data for Switching the Internal Oscillator Operating Mode and External Clock Operating Mode

This control data bit selects either the internal oscillator operating mode or external clock operating mode. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to "(OC) = (0)" by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system.

OC	Fundamental Clock Operating Mode	Input Pin (OSCI) State
0	Internal oscillator operating mode	Connect to GND
1	External clock operating mode	Input the clock of $f_{OSCI}1$ = 200 kHz or $f_{OSCI}2$ = 150 kHz from the outside

(14) EXF • • • Control Data for Setting the External Clock Operating Frequency

This control data bit sets the operating frequency of the external clock which input into the OSCI pin, when the external clock operating mode (OC = “1”) is set. However, this control data is effective only when external clock operating mode (OC = “1”) is set. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to “(EXF) = (0)” by the reset action (reset by $\overline{RES}$ pin or voltage detection type reset circuit (VDET)) of the system.

EXF	External Clock Operating Frequency f_{OSCI}
0	$f_{OSCI}1$ = 200 kHz
1	$f_{OSCI}2$ = 150 kHz

(15) SR • • • Control Data for Setting the Output Current Rising Time of LED Driver

This control data bit sets the output current rising time of LED driver. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to “(SR) = (0)” by the reset action (reset by $\overline{RES}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

SR	Output Current Rising Time Tld
0	0.5 μs typ
1	1.0 μs typ

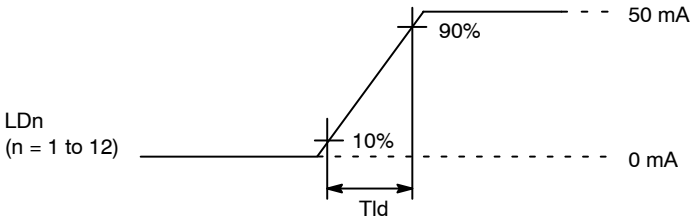


Figure 12. Output Current Rising Time

(16) ERD • • • Control Data for Outputting Each Diagnosis Result Data from ERR Pin

This control data is enabled to output each diagnosis result data “POR, CERR, VERR, AERR, OERR, SERR, TSD150, TSD125, R_LOCK, W_LOCK, P_LOCK, M_LOCK, C_LOCK, IR1, IR0, RSH12 to RSH1, RSL12 to RSL1, ROP12 to ROP1, RAJ12 to RAJ1, RLD12 to RLD1” from ERR pin. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to “(ERD) = (0)” by the reset action (reset by $\overline{RES}$ pin, voltage detection type reset circuit (VDET) of the system.

ERD	ERD Pin Function
0	The ERR pin is set to “L” level at the time of 125°C temperature abnormality, open/short/adjacent outputs short abnormality, LED pull-up supply voltage abnormality, fundamental clock abnormality, reset action.
1	The ERR pin is set to “L” level at the time of 125°C temperature abnormality, open/short/adjacent outputs short abnormality, LED pull-up supply voltage abnormality, fundamental clock abnormality, reset action. In addition, application can output each diagnosis result data “POR, CERR, VERR, AERR, OERR, SERR, TSD150, TSD125, R_LOCK, W_LOCK, P_LOCK, M_LOCK, C_LOCK, IR1, IR0, RSH12 to RSH1, RSL12 to RSL1, ROP12 to ROP1, RAJ12 to RAJ1, RLD12 to RLD1” from ERR pin with serial data transfer clock.

Table 3. LIST OF READ COMMAND CONTROL REGISTERS BY ERR PIN

Command Name	RW	Command Address								Read Data from ERR Output							
		ADn7	ADn6	ADn5	ADn4	ADn3	ADn2	ADn1	ADn0	EDn7	EDn6	EDn5	EDn4	EDn3	EDn2	EDn1	EDn0
Read Status flag 1	R	1	1	1	0	0	0	0	1	POR	CERR	VERR	AERR	OERR	SERR	TSD150	TSD125
Read Status flag 2	R	1	1	1	0	0	0	1	0	0	0	0	R_LOCK	W_LOCK	P_LOCK	M_LOCK	C_LOCK
Read External resistance diagnosis result	R	1	1	1	0	0	0	1	1	0	0	0	0	0	0	IR1	IR0
Read VLED short detection result 1	R	1	1	1	0	0	1	0	0	0	0	RSH6	RSH5	RSH4	RSH3	RSH2	RSH1
Read VLED short detection result 2	R	1	1	1	0	0	1	0	1	0	0	RSH12	RSH11	RSH10	RSH9	RSH8	RSH7
Read VSS short detection result 1	R	1	1	1	0	0	1	1	0	0	0	RSL6	RSL5	RSL4	RSL3	RSL2	RSL1
Read VSS short detection result 2	R	1	1	1	0	0	1	1	1	0	0	RSL12	RSL11	RSL10	RSL9	RSL8	RSL7
Read open detection result 1	R	1	1	1	0	1	0	0	0	0	0	ROP6	ROP5	ROP4	ROP3	ROP2	ROP1
Read open detection result 2	R	1	1	1	0	1	0	0	1	0	0	ROP12	ROP11	ROP10	ROP9	ROP8	ROP7
Read adjacent outputs short detection result 1	R	1	1	1	0	1	0	1	0	0	0	RAJ6	RAJ5	RAJ4	RAJ3	RAJ2	RAJ1
Read adjacent outputs short detection result 2	R	1	1	1	0	1	0	1	1	0	0	RAJ12	RAJ11	RAJ10	RAJ9	RAJ8	RAJ7
Read the state data of the LED driver output 1	R	1	1	1	0	1	1	0	0	0	0	RLD6	RLD5	RLD4	RLD3	RLD2	RLD1
Read the state data of the LED driver output 2	R	1	1	1	0	1	1	0	1	0	0	RLD12	RLD11	RLD10	RLD9	RLD8	RLD7

(17) VLS0,VLS1 • • • Control Data for Setting Abnormal Value of LED Pull-up Supply Voltage VLED

This control data bits set the abnormal value of LED pull-up supply voltage VLED. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to "(VLS0, VLS1) = (1,1)" by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

VLS1	VLS0	Description about the Abnormal Value Detection of LED Pull-up Supply Voltage VLED
0	0	It can't detect an abnormal value of LED pull-up supply voltage.
0	1	In the case of VLED ≤ 4.2 V typ (LED driver supply abnormal voltage), it detects an abnormal value of LED pull-up supply voltage and sets the status data VERR to "1". However, the recommended power supply VDD is between 4.5 V and 5.5 V.
1	0	In the case of VLED ≤ 2.4 V typ (LED driver supply abnormal voltage), it detects an abnormal value of LED pull-up supply voltage and sets the status data VERR to "1".
1	1	

(18) MKIR • • • Control Data for Setting External Resistance Value Abnormality Detection Mask of IREF Pin

The control data bit sets the external resistance value abnormality detection mask of IREF pin. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to "(MKIR) = (1)" by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

MKIR	External Resistance Value Abnormality Detection Operation Statement of IREF Pin
0	It doesn't operate the external resistance value abnormality detection of IREF pin.
1	It operates the external resistance value abnormality detection of IREF pin.

(19) MKSH • • • Control Data for Setting VLED Short Detection Mask of All of LED Driver Outputs from LD1 to LD12

The control data bit sets the VLED short detection mask of all of LED driver outputs from LD1 to LD12. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to "(MKSH) = (1)" by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

MKSH	VLED Short Detection Operation Statement of LED Driver Outputs
0	It doesn't operate the VLED short detection regardless of contents of the control data MSHn.
1	It operates the VLED short detection with contents of the control data MSHn.

22. (n = 1 to 12)

(20) MKSL • • • Control Data for Setting VSS Short Detection Mask of All of LED Driver Outputs from LD1 to LD12

The control data bit sets the VSS short detection mask of all of LED driver outputs from LD1 to LD12. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to "(MKSL) = (1)" by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

MKSL	VSS Short Detection Operation Statement of LED Driver Outputs
0	It doesn't operate the VSS short detection regardless of contents of the control data MSLn.
1	It operates the VSS short detection with contents of the control data MSLn.

23. (n = 1 to 12)

(21) MKOP • • • Control Data for Setting Open Detection Mask of All of LED Driver Outputs from LD1 to LD12

The control data bit sets the open detection mask of all of LED driver outputs from LD1 to LD12. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to "(MKOP) = (1)" by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

MKOP	Open Detection Operation Statement of LED Driver Outputs
0	It doesn't operate the open detection regardless of contents of the control data MOPn.
1	It operates the open detection with contents of the control data MOPn.

24. (n = 1 to 12)

(22) MKAJ • • • Control Data for Setting Adjacent Outputs Short Detection Mask of All of LED Driver Outputs from LD1 to LD12

The control data bit sets the adjacent outputs detection mask of LED driver outputs from LD1 to LD12. In addition, this control data is protected by the command [Lock of control data 1 & control data 2]. It cannot change this control data when the command [Lock of control data 1 & control data 2] is set. When changing this control data, transmit the command [Unlock of control data 1 & control data 2]. Afterwards set this control data. This control data is initialized to "(MKAJ) = (1)" by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

MKAJ	Adjacent Outputs Short Detection Operation Statement of LED Driver Outputs
0	It doesn't operate the adjacent outputs short detection.
1	It operates the adjacent outputs short detection.

Correspondence of Output Pins to Control Data for LED Driver Output Mask Setting

Output Pins	Control Data for LED Driver Output Mask Setting
LD1	MLD1
LD2	MLD2
LD3	MLD3
LD4	MLD4
LD5	MLD5
LD6	MLD6
LD7	MLD7
LD8	MLD8
LD9	MLD9
LD10	MLD10
LD11	MLD11
LD12	MLD12

For example, the table below lists the output states for the LD7 output pin.

MLDJ	Output Pin (LD7) State
0	LED is off.

1	LED is on.
	If (L7C,L7B,L7A) = (0,0,0) is set, the current value is decided by control data “CA77 to CA70” of output current regulation. And duty is 100%.
	If (L7C,L7B,L7A)=(0,0,1) is set, the current value is decided by control data “CA77 to CA70” of output current regulation. And duty is decided by PWM data “W19 to W10” of PWM circuit (Ch1).
	If (L7C,L7B,L7A)=(0,1,0) is set, the current value is decided by control data “CA77 to CA70” of output current regulation. And duty is decided by PWM data “W29 to W20” of PWM circuit (Ch2).
	If (L7C,L7B,L7A)=(0,1,1) is set, the current value is decided by control data “CA77 to CA70” of output current regulation. And duty is decided by PWM data “W39 to W30” of PWM circuit (Ch3).
	If (L7C,L7B,L7A)=(1,0,0) is set, the current value is decided by control data “CA77 to CA70” of output current regulation. And duty is decided by PWM data “W49 to W40” of PWM circuit (Ch4).
	If (L7C,L7B,L7A)=(1,0,1) is set, the current value is decided by control data “CA77 to CA70” of output current regulation. And duty is decided by PWM data “W59 to W50” of PWM circuit (Ch5).
	If (L7C,L7B,L7A)=(1,1,0) is set, the current value is decided by control data “CA77 to CA70” of output current regulation. And duty is decided by PWM data “W69 to W60” of PWM circuit (Ch6).
	If (L7C,L7B,L7A)=(1,1,1) is set, the current value is decided by control data “CA77 to CA70” of output current regulation. And duty is 100%.

Explanation of Status Data

(1) TSD125 • • • 125°C Detection Status Data with the Temperature Sensor

A detection state of the junction temperature with the temperature sensor is set for this status data. When junction temperature is less than 125°C, TSD125 is set to “0”. When junction temperature is 125°C or more, TSD125 is set to “1”. Even if junction temperature falls to less than 125°C after TSD125 has been set to “1”, TSD125 is not set to “0” and maintains “1”. The controller can read this status data by the command [Read status flag 1]. This status data is set to “(TSD125) = (1)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. Therefore it initializes this status data to “(TSD125) = (0)” by transmitting the command [Reset status flag].

TSD125	Status
0	Normal operation
1	The temperature sensor detects 125°C or more

(2) TSD150 • • • 150°C Detection Status Data with the Temperature Sensor

A detection state of the junction temperature with the temperature sensor is set for this status data. When junction temperature is less than 150°C, TSD150 is set to “0”. When junction temperature is 150°C or more, TSD150 is set to “1”. In addition, when the thermal shut down is valid by control data TSDN = “0” and it is at the time of TSD150 = “1”, all LED driver output is set to turn off state forcibly. Even if junction temperature falls to less than 150°C after TSD150 has been set to “1”, TSD150 is not set to “0” and maintains “1”. The controller can read this status data by the command [Read status flag 1]. This status data is set to “(TSD150) = (1)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. Therefore it initializes this status data to “(TSD150) = (0)” by transmitting the command [Reset status flag].

TSD150	Status
0	Normal operation
1	The temperature sensor detects 150°C or more

(3) SERR • • • Master Status Data of the Short Abnormality Detection

A detection state of the short detection circuit of the LED driver outputs is set for this status data. When short abnormality is not detected by LED driver outputs, SERR is set to “0”, and when short abnormality is detected by one or more LED driver output, SERR is set to “1”. Even if short abnormality is not detected after SERR has been set to “1”, SERR is not set to “0” and maintains “1”. The controller can read this status data by the command [Read status flag 1]. This status data is set to “(SERR) = (1)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. Therefore it initializes this status data to “(SERR) = (0)” by transmitting the command [Reset status flag].

SERR	Status
0	Normal operation
1	Short abnormality of one or more LED driver output is detected

(4) OERR • • • Master Status Data of the Open Abnormality Detection

A detection state of the open detection circuit of the LED driver outputs is set for this status data. When open abnormality is not detected by LED driver outputs, OERR is set to “0”, and when open abnormality is detected by one or more LED driver output, OERR is set to “1”. Even if open abnormality is not detected after OERR has been set to “1”, OERR is not set to “0” and maintains “1”. The controller can read this status data by the command [Read status flag 1]. This status data is set to “(OERR) = (1)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. Therefore it initializes this status data to “(OERR) = (0)” by transmitting the command [Reset status flag].

OERR	Status
0	Normal operation
1	Open abnormality of one or more LED driver output is detected

(5) AERR • • • Master Status Data of the Adjacent Outputs Short Abnormality Detection

A detection state of the adjacent outputs short detection circuit of the LED driver outputs is set for this status data. When the adjacent outputs short abnormality is not detected by LED driver outputs, AERR is set to “0”, and when the adjacent outputs short abnormality is detected by one or more LED driver output, AERR is set to “1”. Even if short abnormality is not detected after AERR has been set to “1”, AERR is not set to “0” and maintains “1”. The controller can read this status data by the command [Read status flag 1]. This status data is set to “(AERR) = (1)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. Therefore it initializes this status data to “(AERR) = (0)” by transmitting the command [Reset status flag].

AERR	Status
0	Normal operation
1	Adjacent outputs short abnormality of one or more LED driver output is detected

(6) VERR • • • Status Data of the VLED Voltage Abnormality Detection

A detection state of the VLED voltage abnormality detection circuit is set for this status data. When the VLED voltage abnormality is not detected by SENSE pin, VERR is set to “0”, and when the VLED voltage abnormality is detected by SENSE pin, VERR is set to “1”. Even if VLED voltage abnormality is not detected after VERR has been set to “1”, VERR is not set to “0” and maintains “1”. The controller can read this status data by the command [Read status flag 1]. This status data is set to “(VERR) = (1)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. Therefore it initializes this status data to “(VERR) = (0)” by transmitting the command [Reset status flag].

VERR	Status
0	Normal operation
1	VLED voltage abnormality in SENSE pin is detected

(7) CERR • • • Status Data of the Fundamental Clock Abnormality Detection

A clock detection state of a fundamental clock is set for this status data. When it is the internal oscillator operating mode “(OC) = (0)”, the operating state of an internal oscillation clock is detected. When it is the external clock operating mode “(OC) = (1)”, the operating state of an external clock is detected. The detection of a fundamental clock starts at the rising edge of the LATCH signal at the command [Check of the fundamental clock abnormality]. After that when the fundamental clock is not detected, CERR is set to “1”. And when the fundamental clock is detected, CERR is set to “0”. The controller can read this status data by the command [Read status flag 1]. The CERR can be cleared “(CERR) = (0)” by the command [Clearing of the fundamental clock abnormality]. This status data is set to “(CERR) = (1)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on.

CERR	Status
0	A fundamental clock (an internal oscillation clock or an external clock) is detected
1	A fundamental clock (an internal oscillation clock or an external clock) is not detected

(8) POR • • • Status Data of the Reset Action

The reset active state of the system is set for this status data. When a system does a reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating), POR is set to “1”. The controller can read this status data by the command [Read status flag 1]. This status data is initialized to “(POR) = (0)” by the command [Reset POR flag].

POR	Status
0	Normal operation
1	Reset of the system is executed by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating

(9) C_LOCK • • • Status Data of the Output Current Regulation Lock

A state of lock/unlock of control data “CAn7 to CAn0 (n = 1 to 12)” for current value regulation of the LED driver outputs is set for this status data. When the command [Lock of output current regulation] is transmitted, C_LOCK is set to “1” and the change of these control data “CAn7 to CAn0 (n = 1 to 12)” is impossible. When the command [Unlock of output current regulation] is transmitted, C_LOCK is set to “0” and the change of these control data “CAn7 to CAn0 (n = 1 to 12)” is possible. The controller can read this status data by the command [Read status flag 2]. This status data is initialized to “(C_LOCK) = (0)” by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

C_LOCK	Status
0	Unlock of output current regulation
1	Lock of output current regulation

(10) M_LOCK • • • Status Data of the LED Driver Output Mask/Open/Short Lock

A state of lock/unlock of control data, such as “MLD1 to MLD12” for the LED driver output mask and “MSH1 to MSH12” for the VLED short detection circuit mask of LED driver output and “MSL1 to MSL12” for the VSS short detection circuit mask of LED driver output and “MOP1 to MOP12” for the open detection circuit mask of LED driver output and “VSH1B, VSH1A to VSH12B, VSH12A” for the VLED short detection voltage setting of LED driver output, is set for this status data. When the command [Lock of LED driver output mask/open/short] is transmitted, M_LOCK is set to “1” and the change of these control data “MLD1 to MLD12”, “MSH1 to MSH12”, “MSL1 to MSL12”, “MOP1 to MOP12”, “VSH1B, VSH1A to VSH12B, VSH12A” is impossible. When the command [Unlock of LED driver output mask/open/short] is transmitted, M_LOCK is set to “0” and the change of these control data “MLD1 to MLD12”, “MSH1 to MSH12”, “MSL1 to MSL12”, “MOP1 to MOP12”, “VSH1B, VSH1A to VSH12B, VSH12A” is possible. The controller can read this status data by the command [Read status flag 2]. This status data is initialized to “(M_LOCK) = (0)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

M_LOCK	Status
0	Unlock of LED driver output mask/open/short
1	Lock of LED driver output mask/open/short

(11) P_LOCK • • • Status Data of the PWM ch & PWM Steps & PWM Frame Frequency Lock

A state of lock/unlock of control data, such as “L1C, L1B, L1A to L12C, L12B, L12A” for setting channel of the PWM circuit of the LED driver outputs “LD1 to LD12” and “WN1, WN0” for setting number of the PWM output steps and “PF3 to PF0” for setting frame frequency of PWM output waveform, is set for this status data. When the command [Lock of the PWM ch & PWM steps & PWM frame frequency] is transmitted, P_LOCK is set to “1”, and the change of these control data “L1C, L1B, L1A to L12C, L12B, L12A”, “WN1, WN0”, “PF3 to PF0” is impossible. When the command [Unlock of the PWM ch & PWM steps & PWM frame frequency] is transmitted, P_LOCK is set to “0”, and the change of these control data “L1C, L1B, L1A to L12C, L12B, L12A”, “WN1, WN0”, “PF3 to PF0” is possible. The controller can read this status data by the command [Read status flag 2]. This status data is initialized to “(P_LOCK) = (0)” by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

P_LOCK	Status
0	Unlock of the PWM ch & PWM steps & PWM frame frequency
1	Lock of the PWM ch & PWM steps & PWM frame frequency

(12) W_LOCK • • • Status Data of the PWM Data Lock

A state of lock/unlock of control data, such as “W19 to W10, W29 to W20, W39 to W30, W49 to W40, W59 to W50, W69 to W60” for setting the PWM data of PWM outputs “1ch to 6ch” maping to LED driver outputs “LD1 to LD12”, is set for this status data. When the command [Lock of the PWM data] is transmitted, W_LOCK is set to “1”, and the change of these control data “W19 to W10, W29 to W20, W39 to W30, W49 to W40, W59 to W50, W69 to W60” is impossible. When the command [Unlock of the PWM data] is transmitted, W_LOCK is set to “0”, and the change of these control data “W19 to W10, W29 to W20, W39 to W30, W49 to W40, W59 to W50, W69 to W60” is possible. The controller can read this status data by the command [Read status flag 2]. This status data is initialized to “(W_LOCK) = (0)” by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

W_LOCK	Status
0	Unlock of the PWM data
1	Lock of the PWM data

(13) R_LOCK • • • Status Data of Lock of the Control Data 1 & Control Data 2

A state of lock/unlock of the control data 1 “PLDT, TSDN, OC, EXF, SR, ERD” and the control data 2 “VLS0, VLS1, MKIR, MKSH, MKSL, MKOP, MKAJ”, is set for this status data. When the command [Lock of control data 1 & control data 2] is transmitted, R_LOCK is set to “1” and the change of these control data “PLDT, TSDN, OC, EXF, SR, ERD, VLS0, VLS1, MKIR, MKSH, MKSL, MKOP, MKAJ” is impossible. When the command [Unlock of control data 1 & control data 2] is transmitted, R_LOCK is set to “0” and the change of these control data “PLDT, TSDN, OC, EXF, SR, ERD, VLS0, VLS1, MKIR, MKSH, MKSL, MKOP, MKAJ” is possible. The controller can read this status data by the command [Read status flag 2]. This status data is initialized to “(R_LOCK) = (0)” by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET), software reset or the thermal shut down actuating) of the system.

R_LOCK	Status
0	Unlock of the control data 1 and the control data 2
1	Lock of the control data 1 and the control data 2

Explanation of Read Data

(1) IR0, IR1 • • • Result Data of External Resistance Value Diagnosis

An external resistance diagnosis result of 2 bits depending on resistance connected to IREF pin is set to these read data. The controller can read these data, by the command [Read external resistance diagnosis result]. These read data are initialized to "(IR1,IR0) = (1,1)" by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. Therefore it initializes these read data to "(IR1,IR0) = (0,1)" by transmitting the command [Reset status flag].

Resistance Value of the IREF Pin	Result Data of External Resistance Value Diagnosis	
	IR1	IR0
Less than 11 kΩ	0	0
12 kΩ to 56 kΩ	0	1
More than 62 kΩ	1	1

(2) RSH1 to RSH12 • • • Result Data of VLED Short Detection of LED Driver Outputs from LD1 to LD12

These read data are set the result of VLED short detection of LED driver outputs from LD1 to LD12. When the LED driver outputs are normal operation, the RSHn (n = 1 to 12) are set to "0". When the LED driver outputs are VLED short abnormal state, the RSHn (n = 1 to 12) are set to "1". Even if the LED driver outputs are normal operation after RSHn (n = 1 to 12) have been set to "1", RSHn (n = 1 to 12) are not set to "0" and maintain "1". The controller can read these data by the command [Read VLED short detection result]. These read data are set to "(RSHn) = (1)" by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. Therefore it initializes these read data to "(RSHn) = (0)" by transmitting the command [Reset status flag].

RSHn	Result Data of VLED Short Detection of LED Driver Output
0	Normal operation
1	VLED short abnormal state of an LED driver output

25. The RSHn (n = 1 to 12) are set to the result of VLED short detection of LED driver outputs LDn (n = 1 to 12).

The table below lists the correspondence of LED driver output pins to result data of VLED short detection of LED driver output.

Output Pins	Result Data of VLED Short Detection of LED Driver Output
LD1	RSH1
LD2	RSH2
LD3	RSH3
LD4	RSH4
LD5	RSH5
LD6	RSH6
LD7	RSH7
LD8	RSH8
LD9	RSH9
LD10	RSH10
LD11	RSH11
LD12	RSH12

(3) RSL1 to RSL12 • • • Result Data of VSS Short Detection of LED Driver Outputs from LD1 to LD12

These read data are set the result of VSS short detection of LED driver outputs from LD1 to LD12. When the LED driver outputs are normal operation, the RSLn (n = 1 to 12) are set to “0”. When the LED driver outputs are VSS short abnormal state, the RSLn (n = 1 to 12) are set to “1”. Even if the LED driver outputs are normal operation after RSLn (n = 1 to 12) have been set to “1”, RSLn (n = 1 to 12) are not set to “0” and maintain “1”. The controller can read these data by the command [Read VSS short detection result]. These read data are set to “(RSLn) = (1)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. Therefore it initializes these read data to “(RSLn) = (0)” by transmitting the command [Reset status flag].

RSLn	Result Data of VSS Short Detection of LED Driver Output
0	Normal operation
1	VSS short abnormal state of an LED driver output

26. The RSLn (n = 1 to 12) are set to the result of VSS short detection of LED driver outputs LDn (n = 1 to 12).

The table below lists the correspondence of LED driver output pins to result data of VSS short detection of LED driver output.

Output Pins	Result Data of VSS Short Detection of LED Driver Output
LD1	RSL1
LD2	RSL2
LD3	RSL3
LD4	RSL4
LD5	RSL5
LD6	RSL6
LD7	RSL7
LD8	RSL8
LD9	RSL9
LD10	RSL10
LD11	RSL11
LD12	RSL12

(4) ROP1 to ROP12 • • • Result Data of Open Detection of LED Driver Outputs from LD1 to LD12

These read data are set the result of open detection of LED driver outputs from LD1 to LD12. When the LED driver outputs are normal operation, the ROPn (n = 1 to 12) are set to “0”. When the LED driver outputs are open abnormal state, the ROn (n = 1 to 12) are set to “1”. Even if the LED driver outputs are normal operation after ROPn (n = 1 to 12) have been set to “1”, ROPn (n = 1 to 12) are not set to “0” and maintain “1”. The controller can read these data by the command [Read open detection result]. These read data are set to “(ROPn) = (1)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. Therefore it initializes these read data to “(ROPn) = (0)” by transmitting the command [Reset status flag].

ROPn	Result Data of Open Detection of LED Driver Output
0	Normal operation
1	Open abnormal state of an LED driver output

27. The ROPn (n = 1 to 12) are set to the result of open detection of LED driver outputs LDn (n = 1 to 12).

The table below lists the correspondence of LED driver output pins to result data of open detection of LED driver output.

Output Pins	Result Data of Open Detection of LED Driver Output
LD1	ROP1
LD2	ROP2
LD3	ROP3
LD4	ROP4
LD5	ROP5
LD6	ROP6
LD7	ROP7
LD8	ROP8
LD9	ROP9
LD10	ROP10
LD11	ROP11
LD12	ROP12

(5) RAJ1 to RAJ12 • • • Result Data of Adjacent Outputs Short Detection of LED Driver Outputs from LD1 to LD12

These read data are set the result of adjacent outputs short detection of LED driver outputs from LD1 to LD12. When the LED driver outputs are normal operation, the RAJn (n = 1 to 12) are set to “0”. When the LED driver outputs are adjacent outputs short abnormal state, the RAJn (n = 1 to 12) are set to “1”. Even if the LED driver outputs are normal operation after RAJn (n = 1 to 12) have been set to “1”, RAJn (n = 1 to 12) are not set to “0” and maintain “1”. The controller can read these data by the command [Read adjacent outputs short detection result]. These read data are set to “(RAJn) = (1)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. Therefore it initializes these read data to “(RAJn) = (0)” by transmitting the command [Reset status flag].

RAJn	Result Data of Adjacent Outputs Short Detection of LED Driver Output
0	Normal operation
1	Adjacent outputs short abnormal state of an LED driver output

28. The RAJn (n = 1 to 12) are set to the result of adjacent outputs short detection of LED driver outputs LDn (n = 1 to 12).

The table below lists the correspondence of LED driver output pins to result data of adjacent outputs short detection of LED driver output.

Output Pins	Result Data of Adjacent Outputs Short Detection of LED Driver Output
LD1	RAJ1
LD2	RAJ2
LD3	RAJ3
LD4	RAJ4
LD5	RAJ5
LD6	RAJ6
LD7	RAJ7
LD8	RAJ8
LD9	RAJ9
LD10	RAJ10
LD11	RAJ11
LD12	RAJ12

(6) RLD1 to RLD12 • • • State Data of the LED Driver Outputs from LD1 to LD12

These read data are set the operating state of the LED driver outputs from LD1 to LD12. When the LED driver output is “OFF”, the RLDn (n = 1 to 12) is set to “0”. When the LED driver output is “ON”, the RLDn (n = 1 to 12) is set to “1”. The RLDn (n = 1 to 12) is set by the rising edge of the LATCH signal at the command [Read the state data of the LED driver output]. The controller can read these data by the command [Read the state data of the LED driver output]. These read data are initialized to “(RLDn) = (0)” by the reset action (reset by $\overline{\text{RES}}$ pin or voltage detection type reset circuit (VDET)) of the system at the time of power on. And it initializes these read data to “(RLDn) = (0)” by transmitting the command [Reset status flag].

RLDn	The State of the LED Driver Output
0	OFF
1	ON

29. The RLDn (n = 1 to 12) are set to the state of the LED driver outputs LDn (n = 1 to 12).

The table below lists the correspondence of LED driver output pins to the state data of LED driver output.

Output Pins	The State Data of the LED Driver Output
LD1	RLD1
LD2	RLD2
LD3	RLD3
LD4	RLD4
LD5	RLD5
LD6	RLD6
LD7	RLD7
LD8	RLD8
LD9	RLD9
LD10	RLD10
LD11	RLD11
LD12	RLD12

Explanation of the Constant Current LED Driver Output

(1) About Current Value

This LSI has 12-ch constant current LED driver circuits which can set the current value for each LED driver output. Reference current (IREF) is decided by reference voltage (VREF) outputted from IREF pin, and by an external resistor connected to IREF pin. Peak output current (IDmax) in all LED driver outputs is shown by the following relational Equations.

$$I_{REF} = \frac{V_{REF}}{R_{EXT}} \ [\mu A] \qquad \text{(eq. 1)}$$

$$I_{Dmax} = I_{REF} \times 500 \ [mA] \qquad \text{(eq. 2)}$$

The current value for each LED driver output can be set for each channel by the control data of CA17 to CA10, CA27 to CA20, CA37 to CA30, CA47 to CA40, CA57 to CA50, CA67 to CA60, CA77 to CA70, CA87 to CA80, CA97 to CA90, CA107 to CA100, CA117 to CA110 and CA127 to CA120. In addition, these control data are protected by the command [Lock of output current regulation] and can change it after setting the command [Unlock of output current regulation].

$$I_D = I_{Dmax} \times \frac{((CAn7 \text{ to } CAn0) + 1)}{256} \ [mA] \qquad \text{(eq. 3)}$$

(n = 1 to 12)

For example, in the case of LED driver output LD1 in 50 mA, LED driver output LD2 in 30.4 mA, LED driver output LD3 in 14.8 mA, it is VREF = 1.2 V (typ), REXT = 12 kΩ, IREF = 100 μA, IDmax = 50 mA, CA17 to CA10 = “11111111”, CA27 to CA20 = “10011011”, CA37 to CA30 = “01001011”.

(2) About Control of the On/Off

The on/off control for each LED driver output can be set by the control of MLD1 to MLD12. In addition, these control data are protected by the command [Lock of LED driver output mask/open/short] and can change it after setting the command [Unlock of LED driver output mask/open/short].

This LSI has 6-ch PWM circuits which can set the lighting time (duty) per one frame for each LED driver output. The corresponding LED driver outputs can control a period of the LED lighting per one frame by setting MLD1 to MLD12= “1”, and by setting one of (LnC, LnB, LnA) = (0,0,1), (0,1,0), (0,1,1), (1,0,0), (1,0,1), (1,1,0). In this way, this LSI can coordinate brightness of the LED. When the LED driver output is set a duty of 100% without using PWM function, set LnC, LnB, LnA = “0,0,0” or “1,1,1”.

When the LED driver output is set the PWM function, it needs to set the number (WN1, WN0) of PWM output steps, the frame frequency (PF3 to PF0) of the PWM output waveform, PWM data (Wm9 to Wm0) of the PWM circuit.

MLDn	State of LED Driver Outputs (LDn)
0	LED is off. (LED driver outputs mask setting)
1	LED is on. (The LED is on by depending on the contents of LnC, LnB, LnA)

30. (n = 1 to 12, m = 1 to 6)
31. MLD1: Data for mask setting of the LED driver output (LD1). / MLD2: Data for mask setting of the LED driver output (LD2). / MLD3: Data for mask setting of the LED driver output (LD3). / MLD4: Data for mask setting of the LED driver output (LD4). / MLD5: Data for mask setting of the LED driver output (LD5). / MLD6: Data for mask setting of the LED driver output (LD6). / MLD7: Data for mask setting of the LED driver output (LD7). / MLD8: Data for mask setting of the LED driver output (LD8). / MLD9: Data for mask setting of the LED driver output (LD9). / MLD10: Data for mask setting of the LED driver output (LD10). / MLD11: Data for mask setting of the LED driver output (LD11). / MLD12: Data for mask setting of the LED driver output (LD12).

When there is a LED driver output which doesn’t be used, it is necessary that the control data “MLD1 to MLD12” of LED driver output mask corresponding to the unused LED driver output is set to “0” (LED is off). And it is necessary that the control data “MSH1 to MSH12” of VLED short detection circuit mask, the control data “MSL1 to MSL12” of VSS short detection circuit mask and the control data “MOP1 to MOP12” of open detection circuit mask, corresponding to the unused LED driver output, is set to “0” (Disabled VLED short detection, disabled VSS short detection, disabled open detection).

If those LED driver outputs are opened and those control data are set to “1”, maybe it is the VLED short abnormality detection, VSS short abnormality detection and open short abnormality detection. And the VLED short detection result data “RSH1 to RSH12”, the VSS short detection result data “RSL1 to RSL12” and the open detection result data “ROP1 to ROP12” corresponding to the LED driver is set to “1” and the status data “SERR” and “OERR” is set to “1”. And the ERR pin is set to “L”. So it needs to be careful.

LED Driver Waveforms

(When the PWM output is set to 128 steps by the control data WN1, WN0 = “0,0”.)

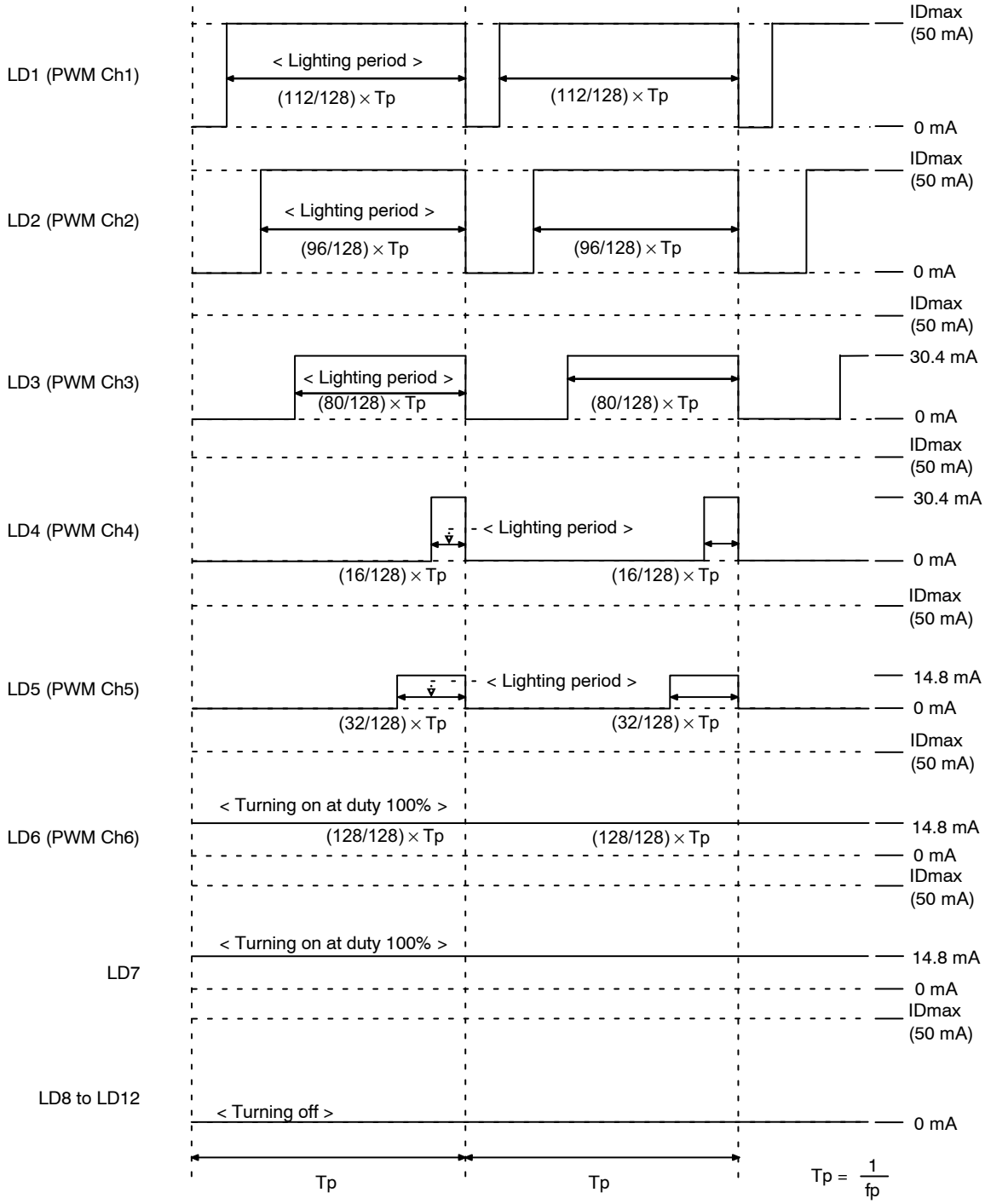


Figure 13. LED Driver Waveforms with PWM Outputs of 128 Steps

Table 4. CURRENT VALUE OF LED DRIVER OUTPUT

Control Data for LED Mask	Control Data for Current Value of the LED								State of LED Driver Output (LD1 to LD12)
MLD1	CA17	CA16	CA15	CA14	CA13	CA12	CA11	CA10	Output Current (I_D)
1	1	1	1	1	1	1	1	1	Output current (LD1): 50 × (256/256) = 50 mA
MLD2	CA27	CA26	CA25	CA24	CA23	CA22	CA21	CA20	Output Current (I_D)
1	1	1	1	1	1	1	1	1	Output current (LD2): 50 × (256/256) = 50 mA
MLD3	CA37	CA36	CA35	CA34	CA33	CA32	CA31	CA30	Output Current (I_D)
1	1	0	0	1	1	0	1	1	Output current (LD3): 50 × (156/256) = 30.4 mA
MLD4	CA47	CA46	CA45	CA44	CA43	CA42	CA41	CA40	Output Current (I_D)
1	1	0	0	1	1	0	1	1	Output current (LD4): 50 × (156/256) = 30.4 mA
MLD5	CA57	CA56	CA55	CA54	CA53	CA52	CA51	CA50	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD5): 50 × (76/256) = 14.8 mA
MLD6	CA67	CA66	CA65	CA64	CA63	CA62	CA61	CA60	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD6): 50 × (76/256) = 14.8 mA
MLD7	CA77	CA76	CA75	CA74	CA73	CA72	CA71	CA70	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD7): 50 × (76/256) = 14.8 mA
MLD8 to MLD12	CAn7	CAn6	CAn5	CAn4	CAn3	CAn2	CAn1	CAn0	Output Current (I_D)
0	X	X	X	X	X	X	X	X	Outputs (LD8 to LD12): LED is off

32. (n = 8 to 12, X: Don't care)

Table 5. LED LIGHTING TIME PER ONE FRAME OF LED DRIVER OUTPUT

Control Data for LED Mask	Data for Setting Channel for PWM Circuits			PWM Data for PWM Circuits	PWM(Ch)
MLD1	L1C	L1B	L1A	(W19 to W10)	LED Lightning Time per One Frame
1	0	0	1	(1,1,0,1,1,1,1,X,X,X)	PWM Ch1 (112/128) × Tp
MLD2	L2C	L2B	L2A	(W29 to W20)	PWM(Ch)
1	0	1	0	(1,0,1,1,1,1,1,X,X,X)	PWM Ch2 (96/128) × Tp
MLD3	L3C	L3B	L3A	(W39 to W30)	PWM(Ch)
1	0	1	1	(1,0,0,1,1,1,1,X,X,X)	PWM Ch3 (80/128) × Tp
MLD4	L4C	L4B	L4A	(W49 to W40)	PWM(Ch)
1	1	0	0	(0,0,0,1,1,1,1,X,X,X)	PWM Ch4 (16/128) × Tp
MLD5	L5C	L5B	L5A	(W59 to W50)	PWM(Ch)
1	1	0	1	(0,0,1,1,1,1,1,X,X,X)	PWM Ch5 (32/128) × Tp
MLD6	L6C	L6B	L6A	(W69 to W60)	PWM(Ch)
1	1	1	0	(1,1,1,1,1,1,1,X,X,X)	PWM Ch6 (128/128) × Tp
MLD7	L7C	L7B	L7A	PWM(Ch)	
1	0	0	0	PWM circuit is not selected, LED is on.	
MLD8 to MLD12	LnC	LnB	LnA	State of LED Driver Outputs (LD8 to LD12)	
0	X	X	X	LED is off.	

33. (n = 8 to 12, X: Don't care)

LED Driver Waveforms

(When the PWM output is set to 256 steps by the control data WN1, WN0 = “0,1”.)

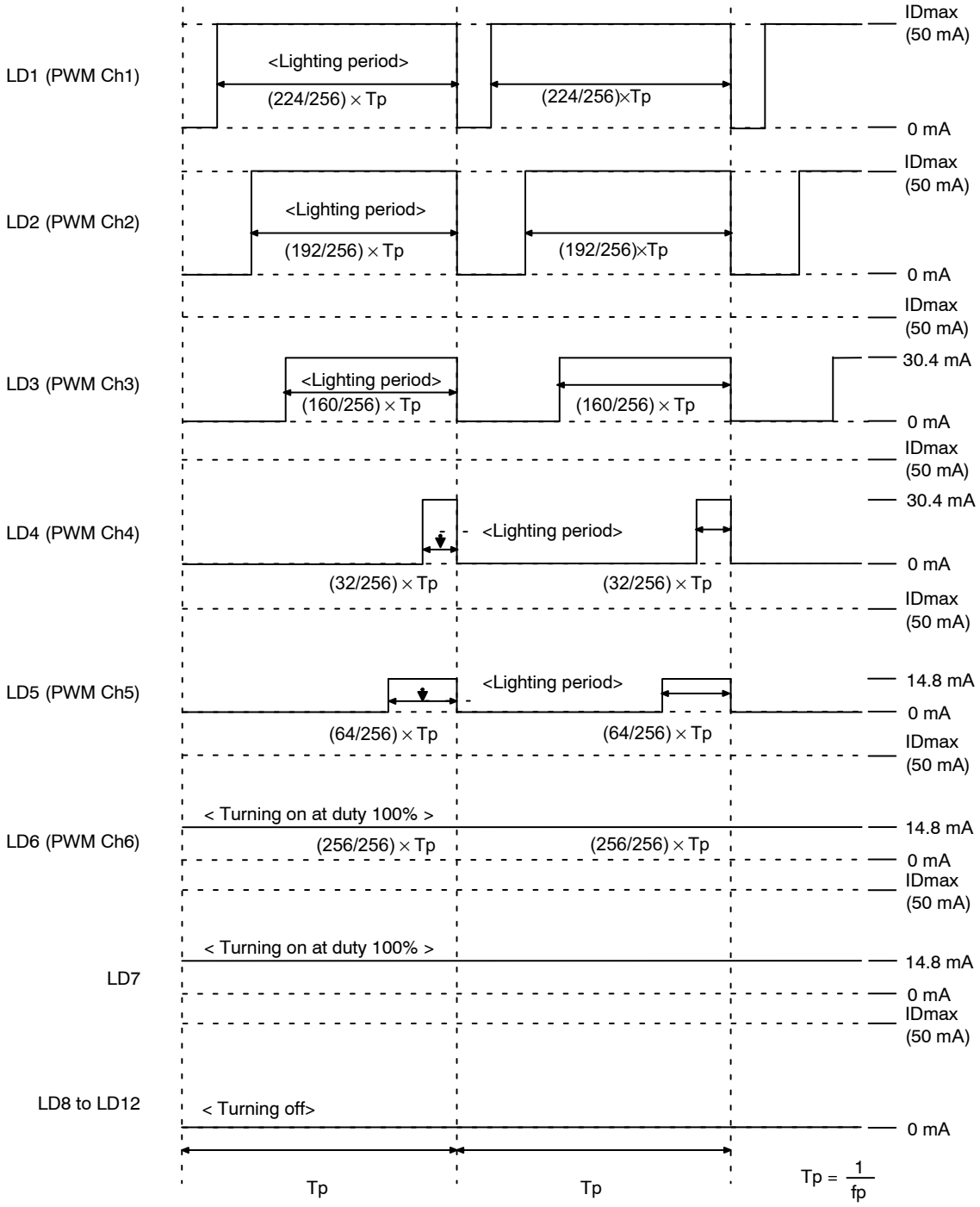


Figure 14. LED Driver Waveforms with PWM Outputs of 256 Steps

Table 6. CURRENT VALUE OF LED DRIVER OUTPUT

Control Data for LED Mask	Control Data for Current Value of the LED								State of LED Driver Output (LD1 to LD12)
MLD1	CA17	CA16	CA15	CA14	CA13	CA12	CA11	CA10	Output Current (I_D)
1	1	1	1	1	1	1	1	1	Output current (LD1): 50 × (256/256) = 50 mA
MLD2	CA27	CA26	CA25	CA24	CA23	CA22	CA21	CA20	Output Current (I_D)
1	1	1	1	1	1	1	1	1	Output current (LD2): 50 × (256/256) = 50 mA
MLD3	CA37	CA36	CA35	CA34	CA33	CA32	CA31	CA30	Output Current (I_D)
1	1	0	0	1	1	0	1	1	Output current (LD3): 50 × (156/256) = 30.4 mA
MLD4	CA47	CA46	CA45	CA44	CA43	CA42	CA41	CA40	Output Current (I_D)
1	1	0	0	1	1	0	1	1	Output current (LD4): 50 × (156/256) = 30.4 mA
MLD5	CA57	CA56	CA55	CA54	CA53	CA52	CA51	CA50	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD5): 50 × (76/256) = 14.8 mA
MLD6	CA67	CA66	CA65	CA64	CA63	CA62	CA61	CA60	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD6): 50 × (76/256) = 14.8 mA
MLD7	CA77	CA76	CA75	CA74	CA73	CA72	CA71	CA70	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD7): 50 × (76/256) = 14.8 mA
MLD8 to MLD12	CAn7	CAn6	CAn5	CAn4	CAn3	CAn2	CAn1	CAn0	Output Current (I_D)
0	X	X	X	X	X	X	X	X	Outputs (LD8 to LD12): LED is off

34. (n = 8 to 12, X: Don't care)

Table 7. LED LIGHTING TIME PER ONE FRAME OF LED DRIVER OUTPUT

Control Data for LED Mask	Data for Setting Channel for PWM Circuits			PWM Data for PWM Circuits	PWM(Ch)
MLD1	L1C	L1B	L1A	(W19 to W10)	LED Lighting Time per One Frame
1	0	0	1	(1,1,0,1,1,1,1,1,X,X)	PWM Ch1 (224/256) × Tp
MLD2	L2C	L2B	L2A	(W29 to W20)	PWM(Ch)
1	0	1	0	(1,0,1,1,1,1,1,1,X,X)	PWM Ch2 (192/256) × Tp
MLD3	L3C	L3B	L3A	(W39 to W30)	PWM(Ch)
1	0	1	1	(1,0,0,1,1,1,1,1,X,X)	PWM Ch3 (160/256) × Tp
MLD4	L4C	L4B	L4A	(W49 to W40)	PWM(Ch)
1	1	0	0	(0,0,0,1,1,1,1,1,X,X)	PWM Ch4 (32/256) × Tp
MLD5	L5C	L5B	L5A	(W59 to W50)	PWM(Ch)
1	1	0	1	(0,0,1,1,1,1,1,1,X,X)	PWM Ch5 (64/256) × Tp
MLD6	L6C	L6B	L6A	(W69 to W60)	PWM(Ch)
1	1	1	0	(1,1,1,1,1,1,1,1,X,X)	PWM Ch6 (256/256) × Tp
MLD7	L7C	L7B	L7A	PWM(Ch)	
1	0	0	0	PWM circuit is not selected, LED is on.	
MLD8 to MLD12	LnC	LnB	LnA	State of LED Driver Outputs (LD8 to LD12)	
0	X	X	X	LED is off.	

35. (n = 8 to 12, X: Don't care)

LED Driver Waveforms

(When the PWM output is set to 512 steps by the control data WN1, WN0 = “1,0”.)

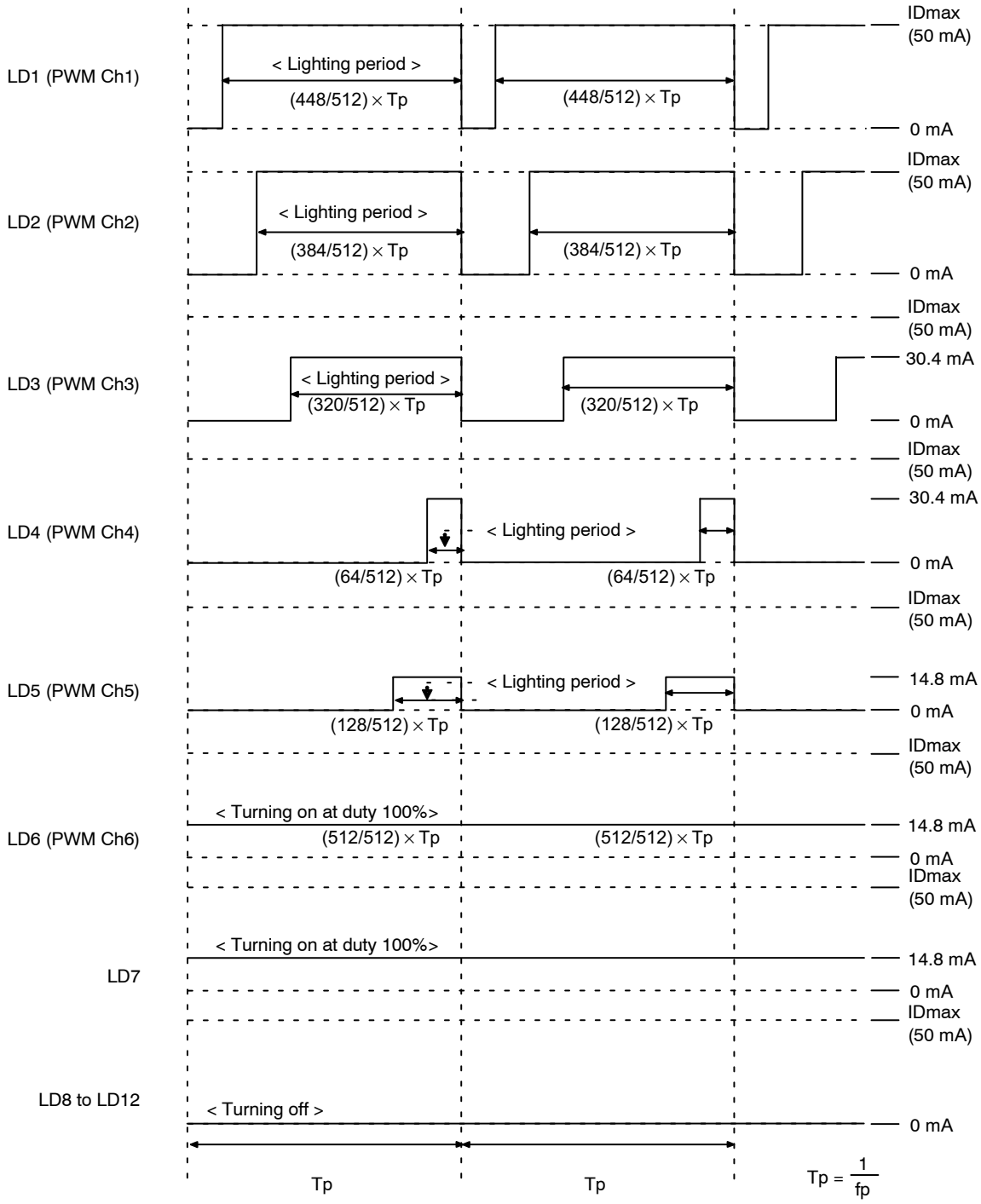


Figure 15. LED Driver Waveforms with PWM Outputs of 512 Steps

Table 8. CURRENT VALUE OF LED DRIVER OUTPUT

Control Data for LED Mask	Control Data for Current Value of the LED								State of LED Driver Output (LD1 to LD12)
MLD1	CA17	CA16	CA15	CA14	CA13	CA12	CA11	CA10	Output Current (I_D)
1	1	1	1	1	1	1	1	1	Output current (LD1): 50 × (256/256) = 50 mA
MLD2	CA27	CA26	CA25	CA24	CA23	CA22	CA21	CA20	Output Current (I_D)
1	1	1	1	1	1	1	1	1	Output current (LD2): 50 × (256/256) = 50 mA
MLD3	CA37	CA36	CA35	CA34	CA33	CA32	CA31	CA30	Output Current (I_D)
1	1	0	0	1	1	0	1	1	Output current (LD3): 50 × (156/256) = 30.4 mA
MLD4	CA47	CA46	CA45	CA44	CA43	CA42	CA41	CA40	Output Current (I_D)
1	1	0	0	1	1	0	1	1	Output current (LD4): 50 × (156/256) = 30.4 mA
MLD5	CA57	CA56	CA55	CA54	CA53	CA52	CA51	CA50	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD5): 50 × (76/256) = 14.8 mA
MLD6	CA67	CA66	CA65	CA64	CA63	CA62	CA61	CA60	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD6): 50 × (76/256) = 14.8 mA
MLD7	CA77	CA76	CA75	CA74	CA73	CA72	CA71	CA70	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD7): 50 × (76/256) = 14.8 mA
MLD8 to MLD12	CAn7	CAn6	CAn5	CAn4	CAn3	CAn2	CAn1	CAn0	Output Current (I_D)
0	X	X	X	X	X	X	X	X	Outputs (LD8 to LD12): LED is off

36. (n = 8 to 12, X: Don't care)

Table 9. LED LIGHTING TIME PER ONE FRAME OF LED DRIVER OUTPUT

Control Data for LED Mask	Data for Setting Channel for PWM Circuits			PWM Data for PWM Circuits	PWM(Ch)
MLD1	L1C	L1B	L1A	(W19 to W10)	LED Lighting Time per One Frame
1	0	0	1	(1,1,0,1,1,1,1,1,1,X)	PWM Ch1 (448/512) × Tp
MLD2	L2C	L2B	L2A	(W29 to W20)	PWM(Ch)
1	0	1	0	(1,0,1,1,1,1,1,1,1,X)	PWM Ch2 (384/512) × Tp
MLD3	L3C	L3B	L3A	(W39 to W30)	PWM(Ch)
1	0	1	1	(1,0,0,1,1,1,1,1,1,X)	PWM Ch3 (320/512) × Tp
MLD4	L4C	L4B	L4A	(W49 to W40)	PWM(Ch)
1	1	0	0	(0,0,0,1,1,1,1,1,1,X)	PWM Ch4 (64/512) × Tp
MLD5	L5C	L5B	L5A	(W59 to W50)	PWM(Ch)
1	1	0	1	(0,0,1,1,1,1,1,1,1,X)	PWM Ch5 (128/512) × Tp
MLD6	L6C	L6B	L6A	(W69 to W60)	PWM(Ch)
1	1	1	0	(1,1,1,1,1,1,1,1,1,X)	PWM Ch6 (512/512) × Tp
MLD7	L7C	L7B	L7A	PWM(Ch)	
1	0	0	0	PWM circuit is not selected, LED is on.	
MLD8 to MLD12	LnC	LnB	LnA	State of LED Driver Outputs (LD8 to LD12)	
0	X	X	X	LED is off.	

37. (n = 8 to 12, X: Don't care)

LED Driver Waveforms

(When the PWM output is set to 1024 steps by the control data WN1, WN0 = “1,1”.)

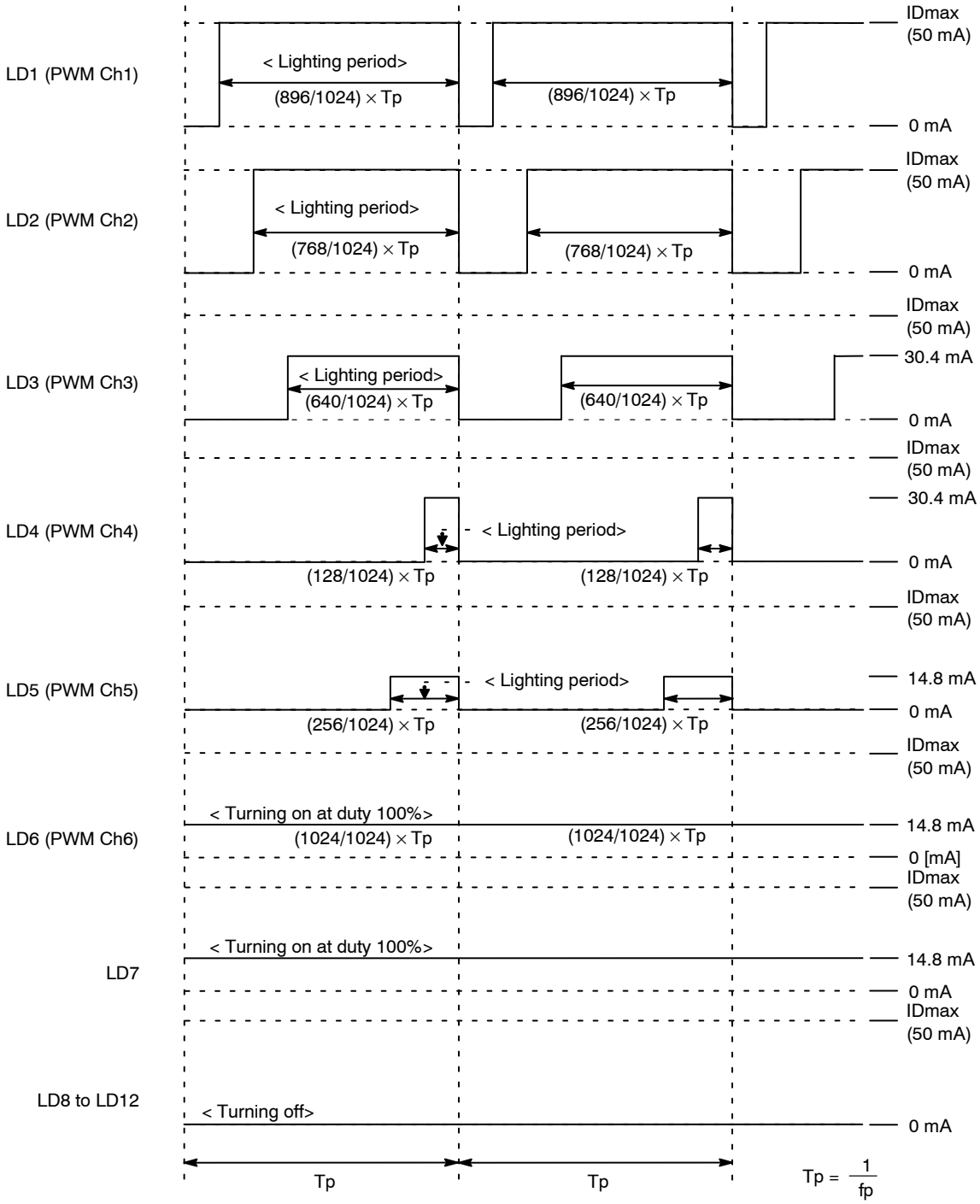


Figure 16. LED Driver Waveforms with PWM Outputs of 1024 Steps

Table 10. CURRENT VALUE OF LED DRIVER OUTPUT

Control Data for LED Mask	Control Data for Current Value of the LED								State of LED Driver Output (LD1 to LD12)
MLD1	CA17	CA16	CA15	CA14	CA13	CA12	CA11	CA10	Output Current (I_D)
1	1	1	1	1	1	1	1	1	Output current (LD1): 50 × (256/256) = 50 mA

MLD2	CA27	CA26	CA25	CA24	CA23	CA22	CA21	CA20	Output Current (I_D)
1	1	1	1	1	1	1	1	1	Output current (LD2): 50 × (256/256) = 50 mA

MLD3	CA37	CA36	CA35	CA34	CA33	CA32	CA31	CA30	Output Current (I_D)
1	1	0	0	1	1	0	1	1	Output current (LD3): 50 × (156/256) = 30.4 mA

MLD4	CA47	CA46	CA45	CA44	CA43	CA42	CA41	CA40	Output Current (I_D)
1	1	0	0	1	1	0	1	1	Output current (LD4): 50 × (156/256) = 30.4 mA

MLD5	CA57	CA56	CA55	CA54	CA53	CA52	CA51	CA50	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD5): 50 × (76/256) = 14.8 mA

MLD6	CA67	CA66	CA65	CA64	CA63	CA62	CA61	CA60	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD6): 50 × (76/256) = 14.8 mA

MLD7	CA77	CA76	CA75	CA74	CA73	CA72	CA71	CA70	Output Current (I_D)
1	0	1	0	0	1	0	1	1	Output current (LD7): 50 × (76/256) = 14.8 mA

MLD8 to MLD12	CAn7	CAn6	CAn5	CAn4	CAn3	CAn2	CAn1	CAn0	Output Current (I_D)
0	X	X	X	X	X	X	X	X	Outputs (LD8 to LD12): LED is off

38. (n = 8 to 12, X: Don't care)

Table 11. LED LIGHTING TIME PER ONE FRAME OF LED DRIVER OUTPUT

Control Data for LED Mask	Data for Setting Channel for PWM Circuits			PWM Data for PWM Circuits	PWM(Ch)
MLD1	L1C	L1B	L1A	(W19 to W10)	LED Lighting Time per One Frame
1	0	0	1	(1,1,0,1,1,1,1,1,1,1)	PWM Ch1 (896/1024) × Tp

MLD2	L2C	L2B	L2A	(W29 to W20)	PWM(Ch)
1	0	1	0	(1,0,1,1,1,1,1,1,1,1)	PWM Ch2 (768/1024) × Tp

MLD3	L3C	L3B	L3A	(W39 to W30)	PWM(Ch)
1	0	1	1	(1,0,0,1,1,1,1,1,1,1)	PWM Ch3 (640/1024) × Tp

MLD4	L4C	L4B	L4A	(W49 to W40)	PWM(Ch)
1	1	0	0	(0,0,0,1,1,1,1,1,1,1)	PWM Ch4 (128/1024) × Tp

MLD5	L5C	L5B	L5A	(W59 to W50)	PWM(Ch)
1	1	0	1	(0,0,1,1,1,1,1,1,1,1)	PWM Ch5 (256/1024) × Tp

MLD6	L6C	L6B	L6A	(W69 to W60)	PWM(Ch)
1	1	1	0	(1,1,1,1,1,1,1,1,1,1)	PWM Ch6 (1024/1024) × Tp

MLD7	L7C	L7B	L7A	PWM(Ch)
1	0	0	0	PWM circuit is not selected, LED is on.

MLD8 to MLD12	LnC	LnB	LnA	State of LED Driver Outputs (LD8 to LD12)
0	X	X	X	LED is off.

39. (n = 8 to 12, X: Don't care)

Explanation of the Operation of the Error Detection Circuit

This LSI has various error detection circuits (Temperature sensor circuit, voltage detection type reset circuit (VDET), open/short/adjacent outputs short detection circuit of the LED driver output, detection circuit of VLED voltage abnormality, detection circuit of external resister value abnormality of IREF pin and detection circuit for the fundamental clock abnormality). The controller can read a state by trasmitting the read command (Read status flag 1, Read external resistance diagnosis result, Read VLED short detection result, Read VSS short detection result, Read open detection result, Read adjacent outputs short result). In addition, it can receive the abnormality from ERR pin (open drain output) directly. When the temperature abnormality (TSD125 = “1”), or the short abnormality (SERR = “1”) of one or more LED driver output, or the open abnormality (OERR = “1”) of one or more LED driver output, or the adjacent outputs short abnormality (AERR = “1”) of one or more LED driver output, or the VLED voltage abnormality (VERR = “1”), or the external resister value abnormality (IR1,0 = “0,0”, “1,1”) or the fundamental clock abnormality (CERR = “1”), or the reset action (POR = “1”) of the system occurred, ERR pin is set to low level(VSS).

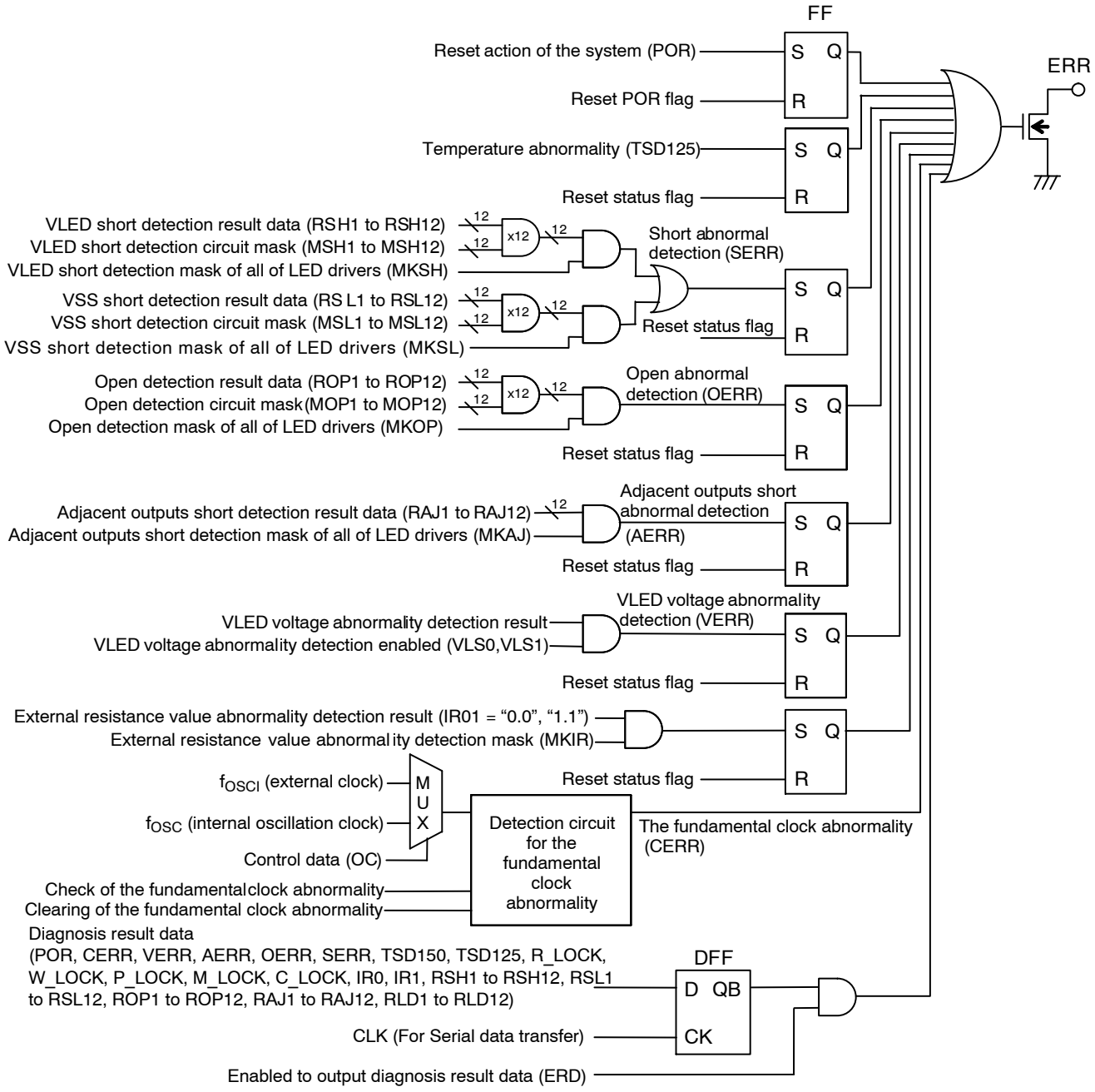


Figure 17. Equivalent Circuit of the Error Detection Circuit

Explanation of the VLED Short Detection Operation of the LED Driver Output

The VLED short detection of the LED driver output is effective, when control data (MLD1 to MLD12) for LED driver output mask is “1”, when control data (MSH1 to MSH12) for VLED short detection circuit mask is “1”, when control data (MKSH) for VLED short detection mask of all of LED driver outputs is “1” and when lighting time of the LED is more than 5 [μs].

The VLED short detection operation compares the potential difference of SENSE voltage (VSE) and the LED driver output voltage (VLDn) with the short detection voltage (VLSH1, VLSH2, VLSH3, VLSH4) by a comparator. If this potential difference is less than the short detection voltage (VLSH1, VLSH2, VLSH3, VLSH4), the LED driver output is judged the VLED short abnormality. And VLED short detection result data (RSH1 to RSH12) is set to “1” (abnormality). On the other hand, if this potential difference is more than the short detection voltage (VLSH1, VLSH2, VLSH3, VLSH4), the LED driver output is judged the normal. And VLED short detection result data (RSH1 to RSH12) is set to “0” (normal). When short abnormality of one or more LED driver output is detected, status data (SERR) of short abnormality detection is set to “1”. It is judged all with short abnormality if potential difference of SENSE voltage and the LED driver output voltage becomes less than the short detection voltage (VLSH1, VLSH2, VLSH3, VLSH4) by not only complete short abnormality but also incomplete short abnormality.

The controller can receive VLED short detection result data (RSH1 to RSH12) by the command [Read VLED short detection result], and can receive status data (SERR) of short abnormality detection by the command [Read status flag 1]. These control data are maintained and are initialized by the command [Reset status flag].

In addition, the VLED short detection operating is possible to stop per channel by the control data (MSH1 to MSH12) of VLED short detection circuit mask of the LED driver output.

Explanation of the VSS Short Detection Operation of the LED Driver Output

The VSS short detection of the LED driver output is effective, when control data (MLD1 to MLD12) for LED driver output mask is “1” or “0”, when control data (MSL1 to MSL12) for VSS short detection circuit mask is “1”, when control data (MKSL) for VSS short detection mask of all of LED driver outputs is “1” and when unlighting time of the LED is more than 5 [μs].

The VSS short detection operation compares the LED driver output voltage (VLDn) with the open detection voltage (VLOP) by a comparator. If the LED driver output voltage (VLDn) is less than the open detection voltage (VLOP), the LED driver output is judged the VSS short abnormality. And VSS short detection result data (RSL1 to RSL12) is set to “1” (abnormality). On the other hand, if the LED driver output voltage (VLDn) is more than the open detection voltage (VLOP), the LED driver output is judged the normal. And VSS short detection result data (RSL1 to RSL12) is set to “0” (normal). When VSS short abnormality of one or more LED driver output is detected, status data (SERR) of short abnormality detection is set to “1”. It is judged all with short abnormality if the LED driver output voltage (VLDn) becomes less than the open detection voltage (VLOP) by not only complete short abnormality but also incomplete short abnormality.

The controller can receive VSS short detection result data (RSL1 to RSL12) by the command [Read VSS short detection result], and can receive status data (SERR) of short abnormality detection by the command [Read status flag 1]. These control data are maintained and are initialized by the command [Reset status flag].

In addition, the VSS short detection operating is possible to stop per channel by the control data (MSL1 to MSL12) of VSS short detection circuit mask of the LED driver output.

Explanation of the Open Detection Operation of the LED Driver Output

The open detection of the LED driver output is effective, when control data (MLD1 to MLD12) for LED driver output mask is “1”, when control data (MOP1 to MOP12) for open detection circuit mask is “1”, when control data (MKOP) for open detection mask of all of LED driver outputs is “1” and when lighting time of the LED is more than 5 [μs].

The open detection operation compares the LED driver output voltage (VLDn) with the open detection voltage (VLOP) by a comparator. If the LED driver output voltage (VLDn) becomes less than the open detection voltage (VLOP), the LED driver output is judged the open abnormality. And open detection result data (ROP1 to ROP12) is set to “1” (abnormality). On the other hand, if the LED driver output voltage (VLDn) becomes more than the open detection voltage (VLOP), the LED driver output is judged the normal. And open detection result data (ROP1 to ROP12) is set to “0” (normal). When open abnormality of one or more LED driver output is detected, status data (OERR) of open abnormality detection is set to “1”. It is judged all with open abnormality if the LED driver output voltage (VLDn) becomes less than the open detection voltage (VLOP) by not only complete open abnormality but also incomplete open abnormality or the voltage reduction of the pull-up power supply for LED.

The controller can receive open detection result data (ROP1 to ROP12) by the command [Read open detection result], and can receive status data (OERR) of open abnormality detection by the command [Read status flag 1]. These control data are maintained and are initialized by the command [Reset status flag].

In addition, the open detection operating is possible to stop per channel by the control data (MOP1 to MOP12) of open detection circuit mask of the LED driver output.

Explanation of the Adjacent Outputs Short Detection Operation of the LED Driver Output

The adjacent outputs short detection of the LED driver output is effective, when control data (MLD1 to MLD12) for LED driver output mask is “0” or “1”, when control data (MKAJ) for adjacent outputs short detection mask of all of LED driver outputs is “1” and when lighting time and unlighting time of the LED between adjacent outputs are different and more than 5 [μs].

The adjacent outputs short detection operation runs when the LED driver status of lighting and unlighting is different. Then it compares the potential difference of SENSE voltage (VSE) and the LED driver output voltage (VLDn) with the short detection voltage (VLSH1, VLSH2, VLSH3, VLSH4) by a comparator. If this potential difference is more than the short detection voltage (VLSH1, VLSH2, VLSH3, VLSH4), the LED driver output is judged the adjacent outputs short abnormality. And adjacent outputs short detection result data (RAJ1 to RAJ12) is set to “1” (abnormality). On the other hand, if this potential difference is less than the short detection voltage (VLSH1, VLSH2, VLSH3, VLSH4), the LED driver output is judged the normal. And adjacent outputs short detection result data (RAJ1 to RAJ12) is set to “0” (normal). When adjacent outputs short abnormality of one or more LED driver output is detected, status data (AERR) of adjacent output short abnormality detection is set to “1”. It is judged all with adjacent outputs short abnormality if potential difference of SENSE voltage and the LED driver output voltage becomes more than the short detection voltage (VLSH1, VLSH2, VLSH3, VLSH4) by not only complete adjacent outputs short abnormality but also incomplete adjacent outputs short abnormality.

The controller can receive adjacent outputs short detection result data (RAJ1 to RAJ12) by the command [Read adjacent outputs short detection result], and can receive status data (AERR) of adjacent outputs short abnormality detection by the command [Read status flag 1]. These control data are maintained and are initialized by the command [Reset status flag].

In addition, the adjacent outputs short detection operating is not possible to stop per channel.

Explanation of the VLED Abnormality Detection Operation of the Pull-up Power Supply Voltage for LED

The VLED abnormality detection of the pull-up power supply voltage is effective, when control data (VLS0, VLS1) for setting VLED abnormal value is “1,0” (abnormality under VLED ≤ VSES1) or “0,1”, “1,1” (abnormality under VLED ≤ VSES2).

The VLED abnormality detection operation compares the SENSE voltage (VSE) with the LED driver supply abnormal voltage (VSES1, VSES2) by a comparator. If the SENSE voltage (VSE) is less than LED driver supply abnormal voltage (VSES1, VSES2), this LSI is judged the VLED abnormality of the pull-up supply voltage for LED. And the status data (VERR) of VLED voltage abnormality detection is set to “1” (abnormality). On the other hand, if this voltage (VSE) is more than LED driver supply abnormal voltage (VSES1,VSES2), this LSI is judged the normal. And the status data (VERR) of VLED voltage abnormality detection is set to “0” (normal).

The controller can receive status data (VERR) of VLED voltage abnormality detection by the command [Read status flag 1]. These control data are maintained and are initialized by the command [Reset status flag].

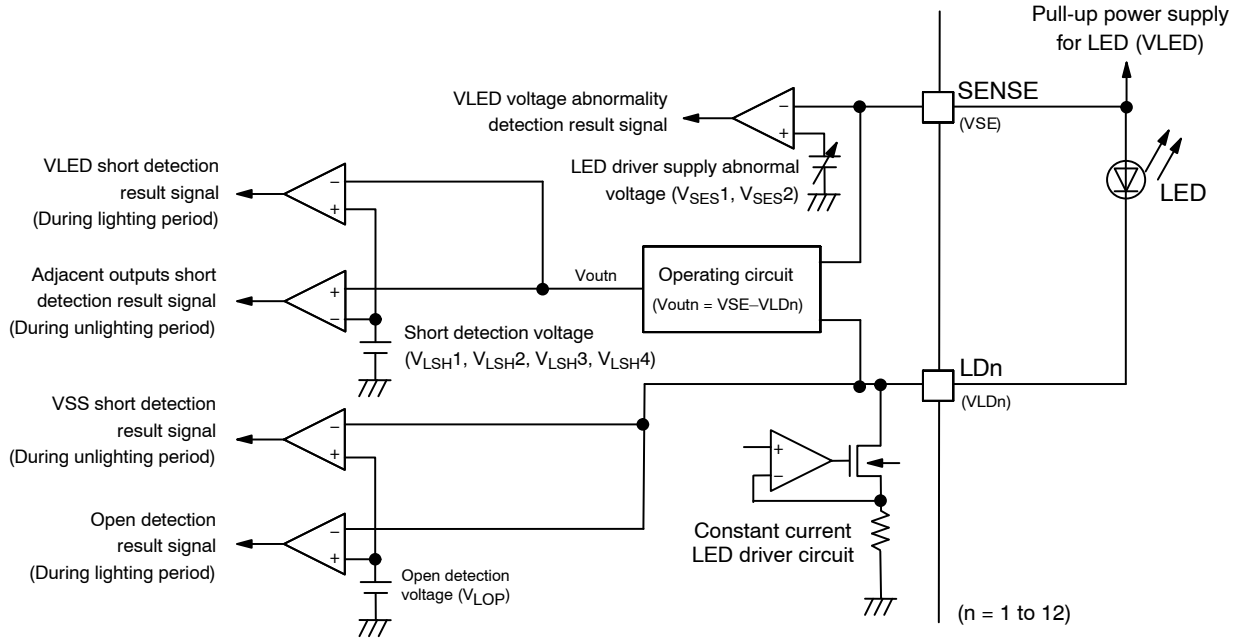
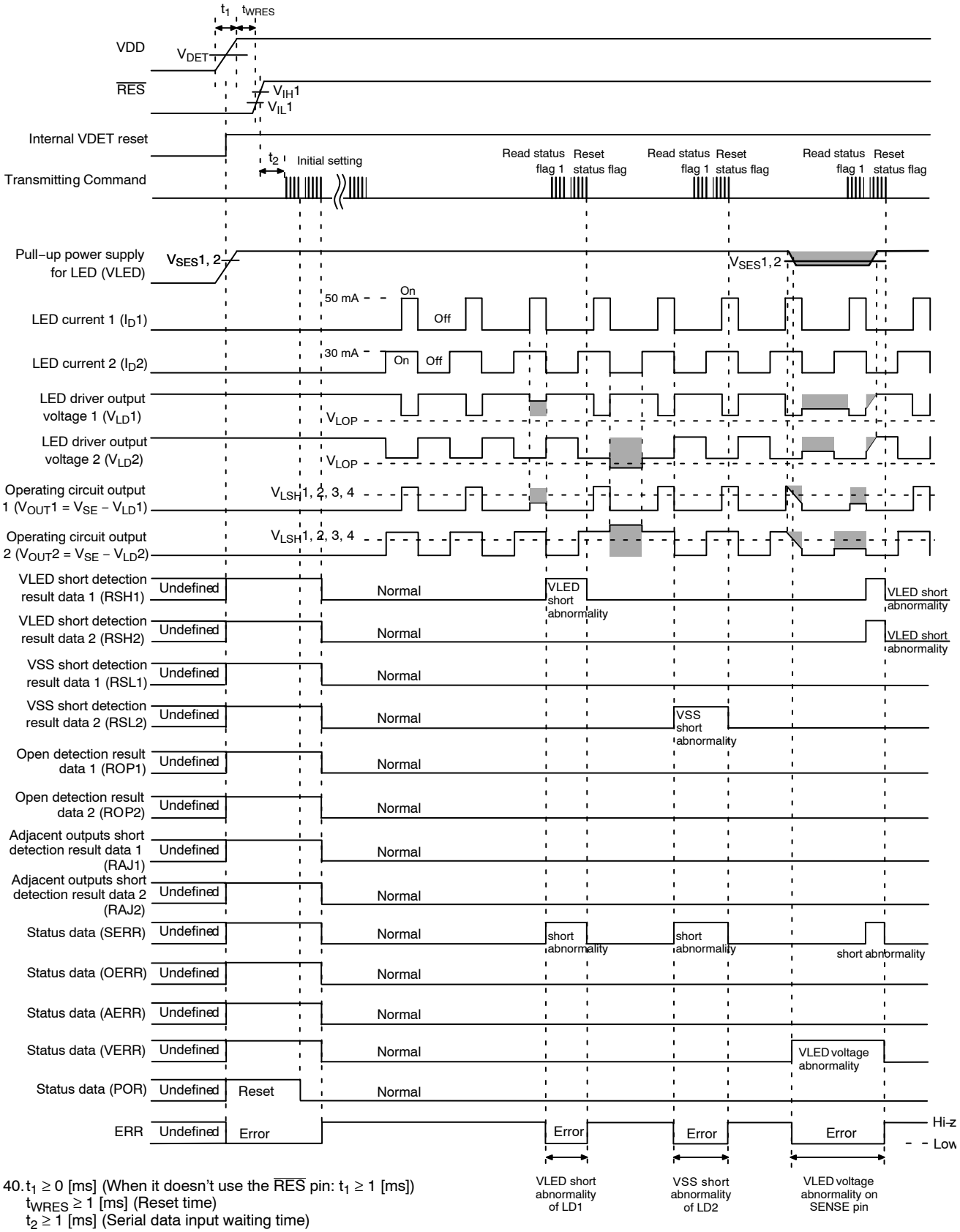
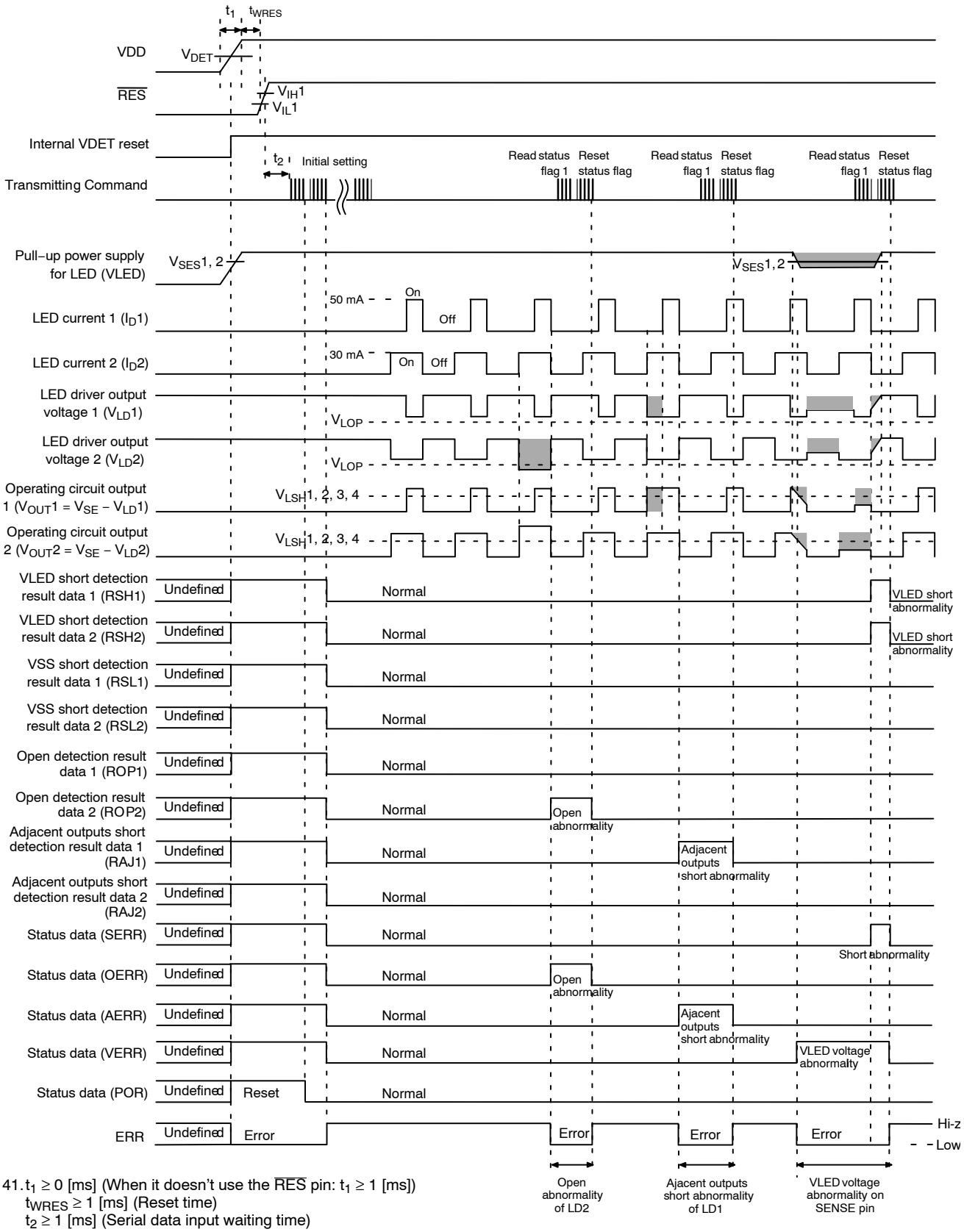


Figure 18. Open/Short Abnormality and VLED Voltage Abnormality Detection Circuit of LED Driver Outputs



40. $t_1 \geq 0$ [ms] (When it doesn't use the $\overline{RES}$ pin: $t_1 \geq 1$ [ms])
$t_{WRES} \geq 1$ [ms] (Reset time)
$t_2 \geq 1$ [ms] (Serial data input waiting time)

Figure 19. Error Detection Operating Sequence of VLED Short, VSS Short and VLED Voltage Abnormality



41. $t_1 \geq 0$ [ms] (When it doesn't use the $\overline{RES}$ pin: $t_1 \geq 1$ [ms])
$t_{WRES} \geq 1$ [ms] (Reset time)
$t_2 \geq 1$ [ms] (Serial data input waiting time)

Figure 20. Error Detection Operating Sequence of Open, Adjacent Outputs Short

About Thermal Shut Down

This LSI has a temperature sensor. When more than 125°C is detected by a temperature sensor, the status data (TSD125) is set to “1”. Furthermore, when more than 150°C is detected by a temperature sensor, the status data (TSD150) is set to “1” and operates thermal shut down. The controller can read status data TSD125 and TSD150 by the command [Read status flag 1]. Even if temperature falls, these status data is not set to “0” and are maintained until it is initialized to “0” by the command [Reset status flag].

The LED driver outputs turn off state forcibly (LD1 to LD12 = “high-impedance”) when it is the thermal shut down. When a temperature sensor falls to less than 150°C, the thermal shut down actuating is canceled.

Table 12. RELATIONS OF TEMPERATURE STATUS DATA AND THE THERMAL SHUT DOWN

TSD150	TSD125	LSI Chip Temperature	Protection Actuating
0	0	125°C or under	Normal operation
0	1	Between 125°C and 150°C	Normal operation
1	1	150°C or above	Thermal shut down actuating

After transmitting the command [Unlock of thermal shut down], it’s possible to invalidate thermal shut down by setting the control data (TSDN) of the thermal shut down to “1”. Even if thermal shut down is invalid, status data (TSD150) is usually set to “1” in the same way. The invalidation of thermal shut down is canceled by the reset action (reset by $\overline{\text{RES}}$ pin, voltage detection type reset circuit (VDET) or software reset) of the system.

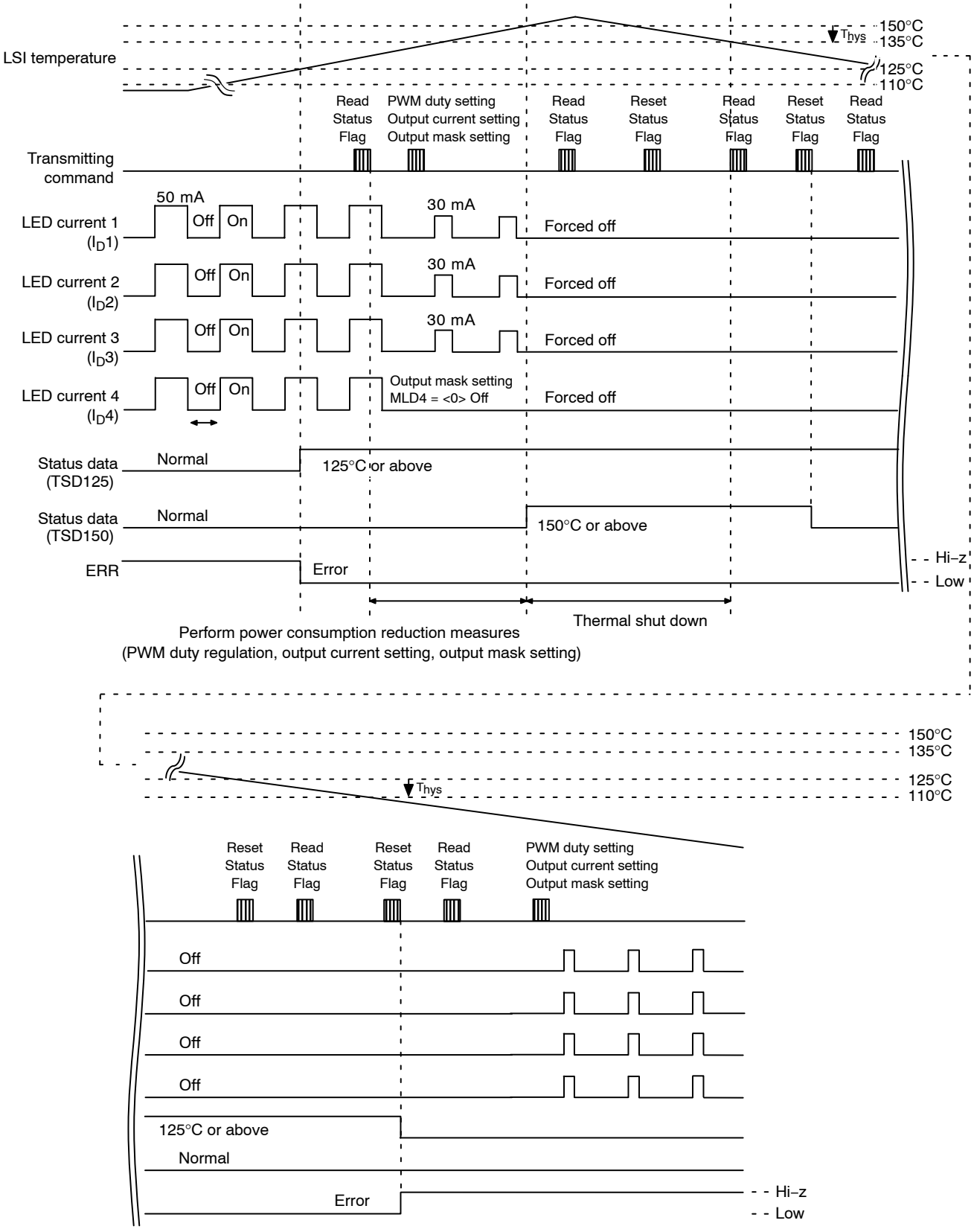


Figure 21. Sequence of the Thermal Shut Down Operating

About the Detection Circuit for the Fundamental Clock Abnormality

This LSI has a detection circuit for the fundamental clock abnormality. When it is the internal oscillator operating mode “(OC) = (0)”, the circuit can detect the internal oscillation clock abnormality. When it is the external clock operating mode “(OC) = (1)”, the circuit can detect the external clock abnormality. The detection of a fundamental clock starts at the rising edge of the LATCH signal at the command [Check of the fundamental clock abnormality]. At this time, ERR pin sets “L”(VSS) first. After detecting a fundamental clock operating, ERR pin sets “high-impedance”. (If a fundamental clock operating is not detected, ERR pin maintains “L”(VSS).) The error of the [Check of the fundamental clock abnormality] which ERR pin outputs and the status data of the fundamental clock abnormality detection (CERR) can be cleared by the command [Clearing of the fundamental clock abnormality].

The Fundamental Clock Operating	Fundamental Clock Operating Mode	The Fundamental Clock Waiting Time (twfc)
Normal	Internal oscillator operating mode “(OC) = (0)”	twfc ≤ 1/fosc
	External clock operating mode “(OC) = (1)”	twfc ≤ $1/f_{OSCI}1$ or twfc ≤ $1/f_{OSCI}2$
Abnormality	Internal oscillator operating mode “(OC) = (0)”	–
	External clock operating mode “(OC) = (1)”	–

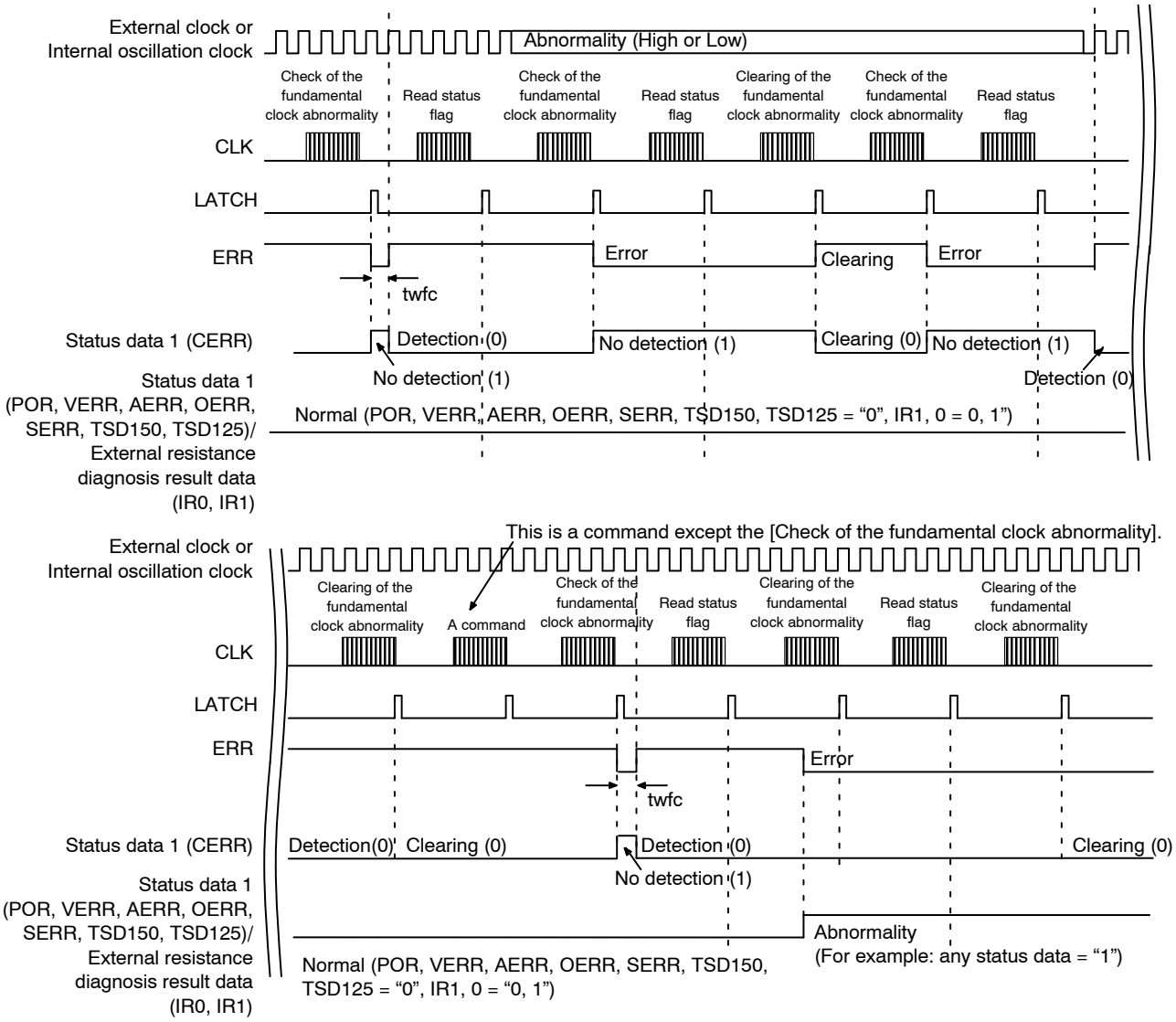


Figure 22. Operating Sequence of the Fundamental Clock Detection

About the Reset of the System

This LSI supports the system reset by $\overline{RES}$ pin, voltage detection type reset circuit (VDET), software reset command and the thermal shut down actuating. When a system reset is applied, the LED driver output (LD1 to LD12) is turned off. (This state is that an electric current does not flow.) This LSI needs to perform the following operation to prevent meaningless lighting, because the control data in the LSI is undefined at the time of the power-on. (Refer to [Figure 24] and [Figure 25]).

(1) Reset Function of the System

<Reset of the system by $\overline{RES}$ pin>

When the power is first applied with setting $\overline{RES}$ pin to "L", the LED driver outputs (LD1 to LD12) is turned off. Then status data of "POR, TSD125, TSD150, SERR, OERR, AERR, CERR and VERR" are set to "1". And the external resistance diagnosis result data of "IR1, IR0" are set to "1,1". And the LED driver state data of "RLD1 to RLD12" are set to "0".

Next, the internal oscillation clock is generated by setting $\overline{RES}$ = "H" and the status data CERR is set to "0". After transmitting the command [Reset POR flag] and [Reset status flag] from a controller, the status data of "POR, TSD125, TSD150, SERR, OERR, AERR, CERR and VERR" are set to "0". And the external resistance diagnosis result data of "IR1, IR0" are set to "0,1". And LED lighting is enabled by transmitting control data for LED display.

<Reset of the system by the voltage detection type reset circuit (VDET)>

If at least 1 [ms] is assured as the power supply voltage VDD rise time when the power is applied with setting the $\overline{RES}$ pin to "H", a system reset will be applied by the VDET output signal when the power supply voltage is brought up. Then, the LED driver outputs (LD1 to LD12) is turned off. Then status data of "POR, TSD125, TSD150, SERR, OERR, AERR, CERR and VERR" are set to "1". And the external resistance diagnosis result data of "IR1, IR0" are set to "1,1". And the LED driver state data of "RLD1 to RLD12" are set to "0". Furthermore the internal oscillation clock is generated, the status data CERR is set to "0".

Next, It maintains the $\overline{RES}$ = "H". After transmitting the command [Reset POR flag] and [Reset status flag] from a controller, the status data of "POR, TSD125, TSD150, SERR, OERR, AERR, CERR and VERR" are set to "0". And the external resistance diagnosis result data of "IR1, IR0" are set to "0,1". And LED lighting is enabled by transmitting control data for LED display.

The voltage detection type reset circuit generates an output signal and resets the system when the power is first applied and when the voltage drops, i.e., when the power supply voltage is less than or equal to the power down detection voltage VDET, which is 2.2 V (typ). To assure that this function operates reliability, a capacitor must be added to the power supply line so that the power supply voltage VDD rise time (t1) when the power is first applied and the power supply voltage VDD fall time (t3) when the voltage drops are both at least 1 [ms].

<Reset of the system by the software reset>

The LED driver outputs (LD1 to LD12) are turned off by transmitting the command [Software reset] from a controller. Then, the status data (POR) is set to "1" and the status data (TSD125, TSD150) is set to "0" or "1" depending on the state of IC again.

Next, transmit the command [Reset POR flag] from a controller. (Status data POR is set to "0".) And LED lighting is enabled by transmitting control data for LED display.

<Reset of the system by the thermal shut down actuating>

When the LSI chip temperature is more than 150°C, a reset by the thermal shut down actuating is applied and the LED driver outputs(LD1 to LD12) are turned off. When the LSI chip temperature falls to less than 150°C, the thermal shut down actuating is canceled.

Next, transmit the command [Reset POR flag] from a controller. (Status data POR is set to "0".) And LED lighting is enabled by transmitting control data for LED display.

(2) State of Each Block during the Reset Period of the System

- REFERENCE CURRENT GENERATOR
  A reset by the $\overline{RES}$ pin and the VDET are applied, and the circuit is set to the initial state. However a reset by the software reset and the thermal shut down actuating are not applied.
- LED DRIVER
  A reset by the $\overline{RES}$ pin, the VDET, the software reset and the thermal shut down actuating are applied, and all LED driver outputs (LD1 to LD12) are set to the state that an electric current does not flow forcibly, and LED is turned off.
- OPEN/SHORT DETECTION CIRCUIT
  A reset by the $\overline{RES}$ pin, the VDET, the software reset and the thermal shut down actuating are applied, and open/short/adjacent outputs short detection circuit operation of the LED driver output is set to the initial state.
- CLOCK GENERATOR
  A reset by the $\overline{RES}$ pin and the VDET are applied, and the internal oscillator stops and the accepting of external clock is stopped. However it generates forcibly the internal oscillator clock just after the end of reset period. And a reset by the software reset and the thermal shut down actuating are not applied.
- TEMPERATURE SENSOR
  A reset by the $\overline{RES}$ pin and the VDET are applied, and the circuit is set to the initial state. However a reset by the software reset and the thermal shut down actuating are not applied.

- CONTROL REGISTER
  A reset by the $\overline{\text{RES}}$ pin, the VDET, the software reset and the thermal shut down actuating are applied, and the circuit is set to the initial state. When a reset by the software reset and the thermal shut down actuating are applied, the control data (OC, EXF, ERD), the status data (SERR, OERR, AERR, CERR, VERR), various detection result data (IR1,IR0,RSH1 to RSH12, RSL1 to RSL12, ROP1 to ROP12, RAJ1 to RAJ12) and the status data of LED driver outputs (RLD1 to RLD12) are maintained same as previous contents.
- SHIFT REGISTER
  A reset by the $\overline{\text{RES}}$ pin, the VDET, the software reset and the thermal shut down actuating are applied, and the circuit is set to the initial state.
- INTERFACE CONTROLLER
  A reset by the $\overline{\text{RES}}$ pin, the VDET, the software reset and the thermal shut down actuating are applied, the circuit does not accept the input of the serial data. However it can do after the end of reset period.

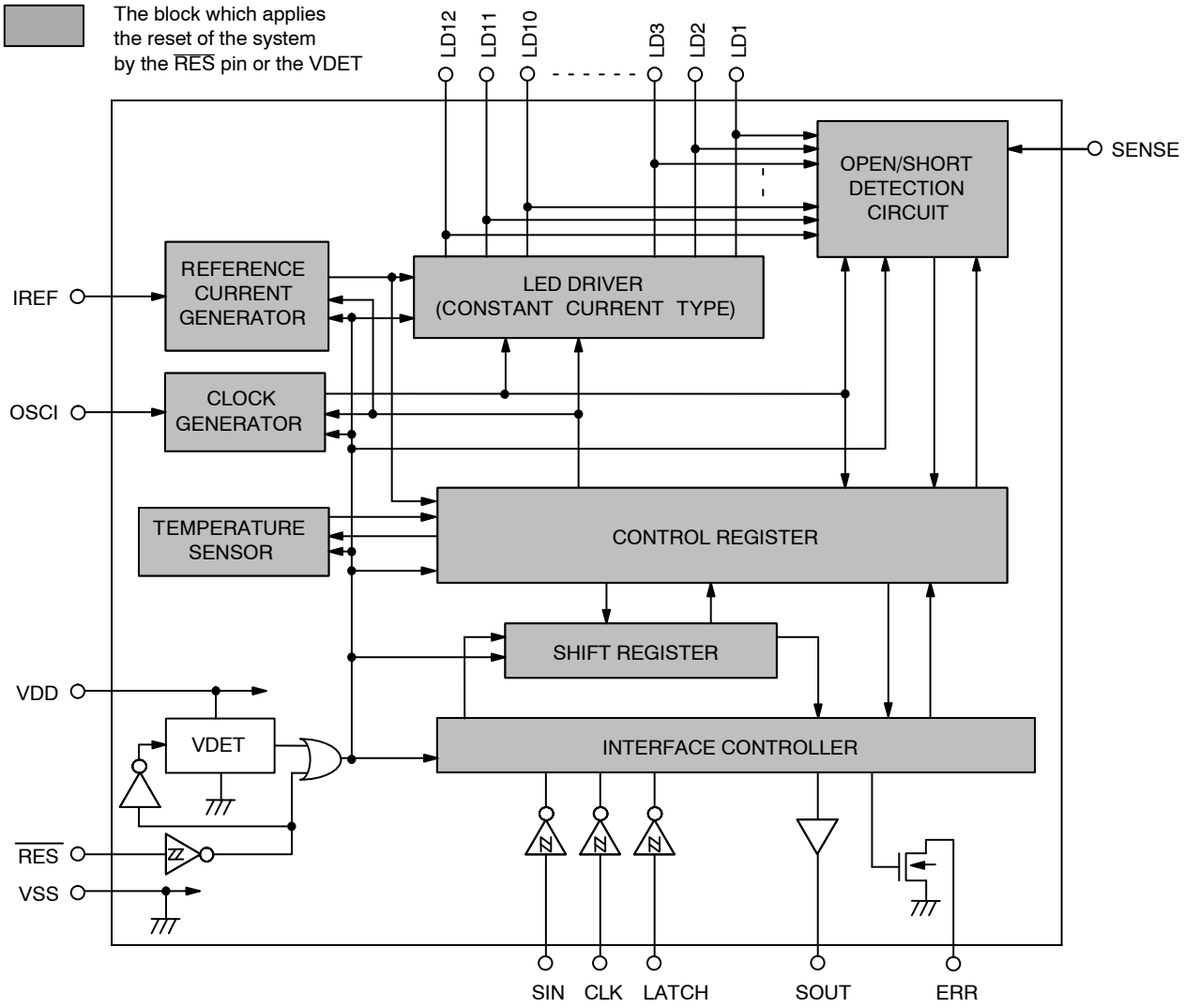


Figure 23. Block which Applies the Reset of the System

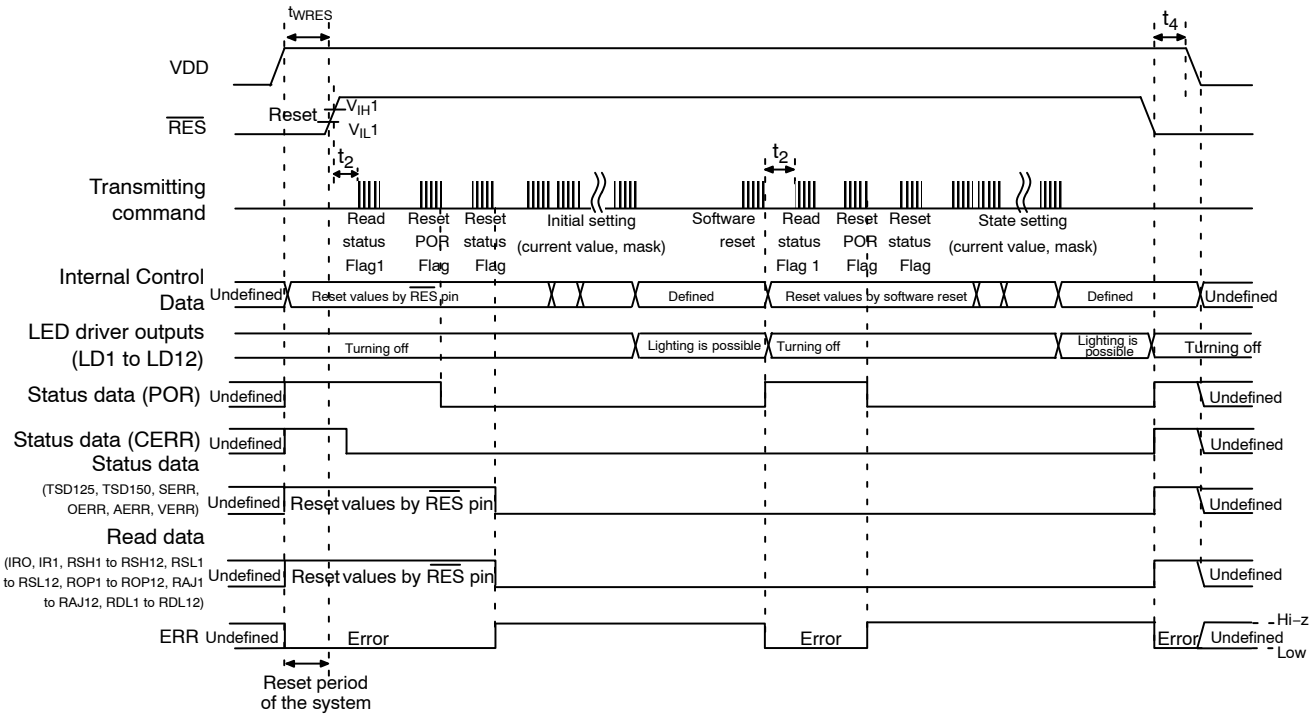
(3) Pin States during System Reset Period

Pins	States during reset of the system
LD1 to LD12	These pins are forcibly set to LED turning off. (The state that an electric current does not flow to LED.)
SOUT	“L” (VSS)
ERR	“L” (VSS)

(4) State of Each Control Register during the Reset Period

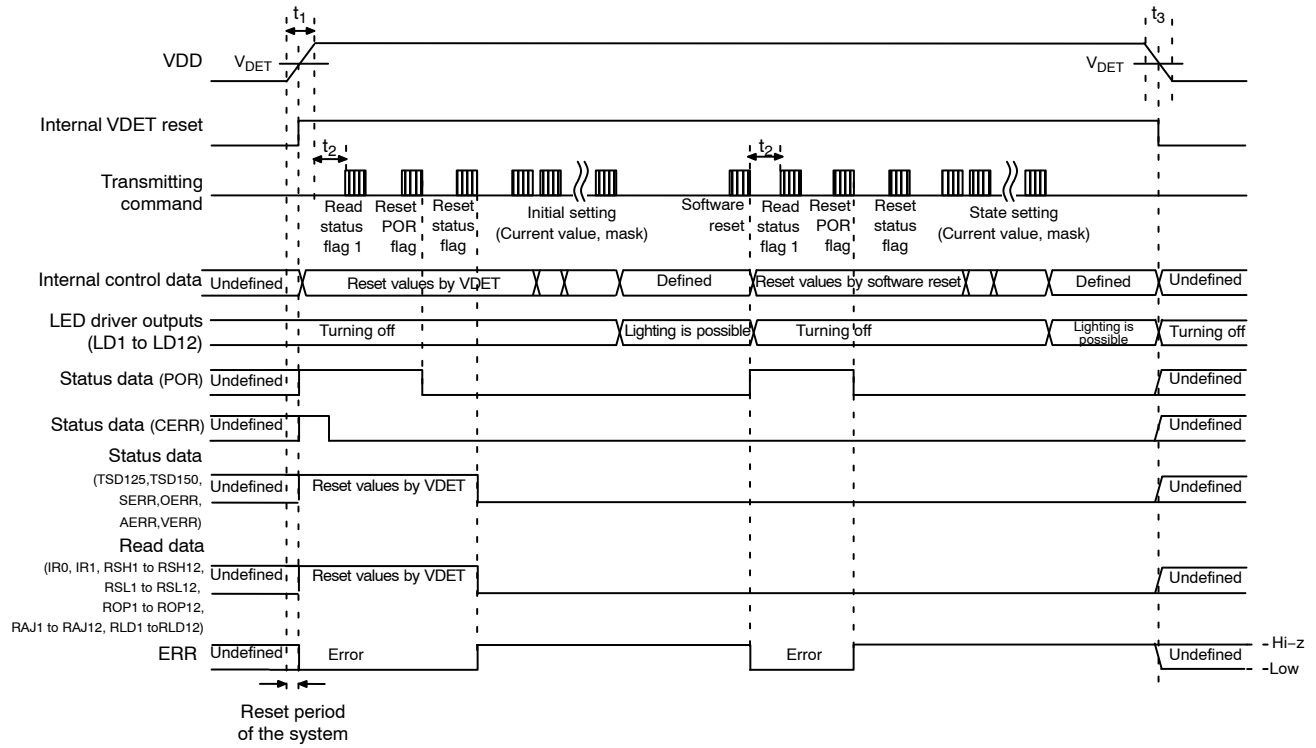
Register Name		Reset by the $\overline{RES}$ Pin or the Voltage Detection Type Reset Circuit (VDET)	Reset by the Software Reset or the Thermal Shut Down Actuating
Output current regulation (CAn7 to CAn0)		All “0,0,0,0,0,0,0,0” (The smallest current)	
PWM Ch (LnC, LnB, LnA)		All “0,0,1” (PWM ch1 is selected)	
PWM steps (WN1,WN0)		“0,0” (128 steps)	
PWM frame frequency (PF3 to PF0)		“1,0,0,0” (fosc/1024)	
PWM data (Wm9 to Wm0)		All “0,0,0,0,0,0,0,0,0,0” (The smallest lighting time)	
LED driver output mask (MLD12 to MLD1)		All “0” (LED turning off)	
VLED short detection circuit mask (MSH12 to MSH1)		All “1” (Connected a detection circuit)	
VSS short detection circuit mask (MSL12 to MSL1)		All “1” (Connected a detection circuit)	
Open detection circuit mask (MOP12 to MOP1)		All “1” (Connected a detection circuit)	
VLED short detection voltage setting (VSH12B, VSH12A to VSH1B, VSH1A)		All “0,0” (0.8 V (typ))	
PWM duty setting at the time of the 125°C detection with the temperature sensor (PLDT)		“0” (When 125°C or above were detected by a temperature sensor, the PWM outputs waveform is adjusted automatically.)	
Thermal shut down function setting (TSDN)		“0” (Thermal shut down is valid)	
Setting the internal oscillator or external clock operating mode (OC)		“0” (Internal oscillator operating mode)	A previous state is maintained.
External clock operating frequency setting (EXF)		“0” (f_{OSC}1 = 200 kHz)	A previous state is maintained.
Output current rising time setting (SR)		“0” (0.5 μs (typ))	
Enabled to output each diagnosis result data from ERR pin (ERD)		“0” (Disabled to output each diagnosis result data)	A previous state is maintained.
Setting abnormal value of LED pull-up voltage VLED (VLS1, VLS0)		“1,1” (In the case of VLED ≤ 2.4 V typ, it can detect an abnormal value)	
Setting external resistance value abnormality detection mask of IREF pin (MKIR)		“1” (It can operate the external resistance value abnormality detection of IREF pin)	
Setting VLED short detection mask of all of LED driver outputs from LD1 to LD12 (MKSH)		“1” (It can operate the VLED short detection with contents of the control data MSHn)	
Setting VSS short detection mask of all of LED driver outputs from LD1 to LD12 (MKSL)		“1” (It can operate the VSS short detection with contents of the control data MSLn)	
Setting open detection mask of all of LED driver outputs from LD1 to LD12 (MKOP)		“1” (It can operate the open detection with contents of the control data MOPn)	
Setting adjacent outputs short detection mask of all of LED driver outputs from LD1 to LD12 (MKAJ)		“1” (It can operate the adjacent outputs short detection)	
Status	125°C detection with the temperature sensor (TSD125)	“1” (Temperature abnormality)	When junction temperature is less than 125°C, it is set to “0”. (Normal) When junction temperature is or above 125°C, it is set to “1”. (Abnormality)
	150°C detection with the temperature sensor (TSD150)	“1” (Temperature abnormality)	When junction temperature is less than 150°C, it is set to “0”. (Normal) When junction temperature is or above 150°C, it is set to “1”. (Abnormality)
	Short abnormality detection (SERR)	“1” (Short abnormality is detected)	A previous state is maintained
	Open abnormality detection (OERR)	“1” (Open abnormality is detected)	A previous state is maintained
	Adjacent outputs short abnormality detection (AERR)	“1” (Adjacent outputs short abnormality is detected)	A previous state is maintained
	VLED voltage abnormality detection (VERR)	“1” (VLED voltage abnormality is detected)	A previous state is maintained
	Fundamental clock abnormality detection (CERR)	“1” (Fundamental clock abnormality is detected)	A previous state is maintained
	Reset action (POR)	“1” (Reset is executed)	
	Output current regulation lock (C_LOCK)	“0” (Output current regulation register unlock)	
	LED driver output mask/open/short lock (M_LOCK)	“0” (LED driver output mask/open/short register unlock)	
	PWM ch & PWM steps & PWM frame frequency lock (P_LOCK)	“0” (PWM ch & PWM steps & PWM frame frequency register unlock)	
	PWM data lock (W_LOCK)	“0” (PWM data register unlock)	
	Control data 1 & control data 2 lock (R_LOCK)	“0” (Control data 1 & control data 2 register unlock)	
External resistance value diagnosis (IR1, IR0)		“1,1” (62 kΩ or above is detected)	A previous state is maintained
Result data of VLED short detection (RSH12 to RSH1)		“1” (VLED Short abnormality is detected)	A previous state is maintained
Result data of VSS short detection (RSL12 to RSL1)		“1” (VSS Short abnormality is detected)	A previous state is maintained
Result data of open detection (ROP12 to ROP1)		“1” (Open abnormality is detected)	A previous state is maintained
Result data of adjacent outputs short detection (RAJ12 to RAJ1)		“1” (Adjacent outputs short abnormality is detected)	A previous state is maintained
State data of the LED driver output (RLD12 to RLD1)		“0” (OFF)	A previous state is maintained

42. (n = 1 to 12, m = 1 to 6)



43. $t_4 \geq 0$ [ms]
$t_{WRES} \geq 1$ [ms] (Reset time)
$t_2 \geq 1$ [ms] (Serial data input waiting time)

Figure 24. Reset Action Sequence (When $\overline{RES}$ Pin is Used)



44. $t_1 \geq 1$ [ms] (Power supply voltage VDD rise time)
$t_2 \geq 1$ [ms] (Serial data input waiting time)
$t_3 \geq 1$ [ms] (Power supply voltage VDD fall time)

Figure 25. Reset Action Sequence (When $\overline{RES}$ Pin is Not Used)

Start-up Sequence (Recommended Examples)

After “VDD” power activation, the internal register is reset by performing a reset action sequence ([Figure 24] or [Figure 25]), and all of LED driver outputs is turned off. After that an LED is turned on by the following sequences.

<1> Transmit the command [Read status flag 1] and confirm that it is POR = “1”. (In the case of POR = “0”, the reset action of the system is abnormality. Confirm whether a reset action sequence does not have an error.)

<2> Transmit the command [Reset POR flag], and clear status data (POR).

<3> Transmit the command [Reset status flag], and clear status data (TSD125, TSD150, SERR, OERR, AERR, VERR) and read data (IR0, IR1, RSH1 to RSH12, RSL1 to RSL12, ROP1 to ROP12, RAJ1 to RAJ12, RLD1 to RLD12).

<4> Transmit the command [Write control data 1], and set the following various control data.
(When the change from a default is necessary)

- PLDT: Control data for PWM duty setting at the time of the 125°C detection with the temperature sensor.
- TSDN: Control data for thermal shut down function setting.
- OC: Control data for switching the internal oscillator operating mode and external clock operating mode.
- EXF: Control data for setting the external clock operating frequency.
- SR: Control data for setting the output current rising time of LED driver.
- ERD: Control data for outputting each diagnosis result data from ERR pin.

<5> Transmit the command [Read control data 1], and confirm the contents of the above control data 1 register.

<6> Transmit the command [Write control data 2], and set the following various control data.
(When the change from a default is necessary)

- VLS0,1: Control data for setting abnormal value of LED pull-up voltage VLED.
- MKIR: Control data for setting external resistance value abnormality detection mask of IREF pin.
- MKSH: Control data for setting VLED short detection mask of all of LED driver outputs from LD1 to LD12.
- MKSL: Control data for setting VSS short detection mask of all of LED driver outputs from LD1 to LD12.
- MKOP: Control data for setting open detection mask of all of LED driver outputs from LD1 to LD12.
- MKAJ: Control data for setting adjacent outputs short detection mask of all of LED driver outputs from LD1 to LD12.

<7> Transmit the command [Read control data 2], and confirm the contents of the above control data 2 register.

<8> Transmit the command [Lock of control data 1 & control data 2], and lock the control data 1 register (PLDT, TSDN, OC, EXF, SR, ERD) and the control data 2 register (VLS0, VLS1, MKIR, MKSH, MKSL, MKOP, MKAJ).

<9> Transmit the command [Check of the fundamental clock abnormality], confirm that the fundamental clock (the internal oscillation clock or the external clock) is normal.

<10> Transmit the command [Write output current regulation], and set the output current value (CAn7 to CAn0) of all channel used with application.

<11> Transmit the command [Read output current regulation], and confirm the contents of the output current regulation register (CAn7 to CAn0).

<12> Transmit the command [Lock of output current regulation], and lock output current regulation register (CAn7 to CAn0).

<13> Transmit the command [Write PWM Ch], and set the PWM Ch register (LnC, LnB, LnA) of all channel used with application.

<14> Transmit the command [Read PWM Ch], and confirm the contents of the PWM Ch register (LnC, LnB, LnA).

<15> Transmit the command [Write PWM steps & PWM frame frequency], and set the PWM steps number (WN1, WN0) and frame frequency (PF3 to PF0).

<16> Transmit the command [Read PWM steps & PWM frame frequency], and confirm the contents of PWM steps register (WN1, WN0) & frame frequency register (PF3 to PF0).

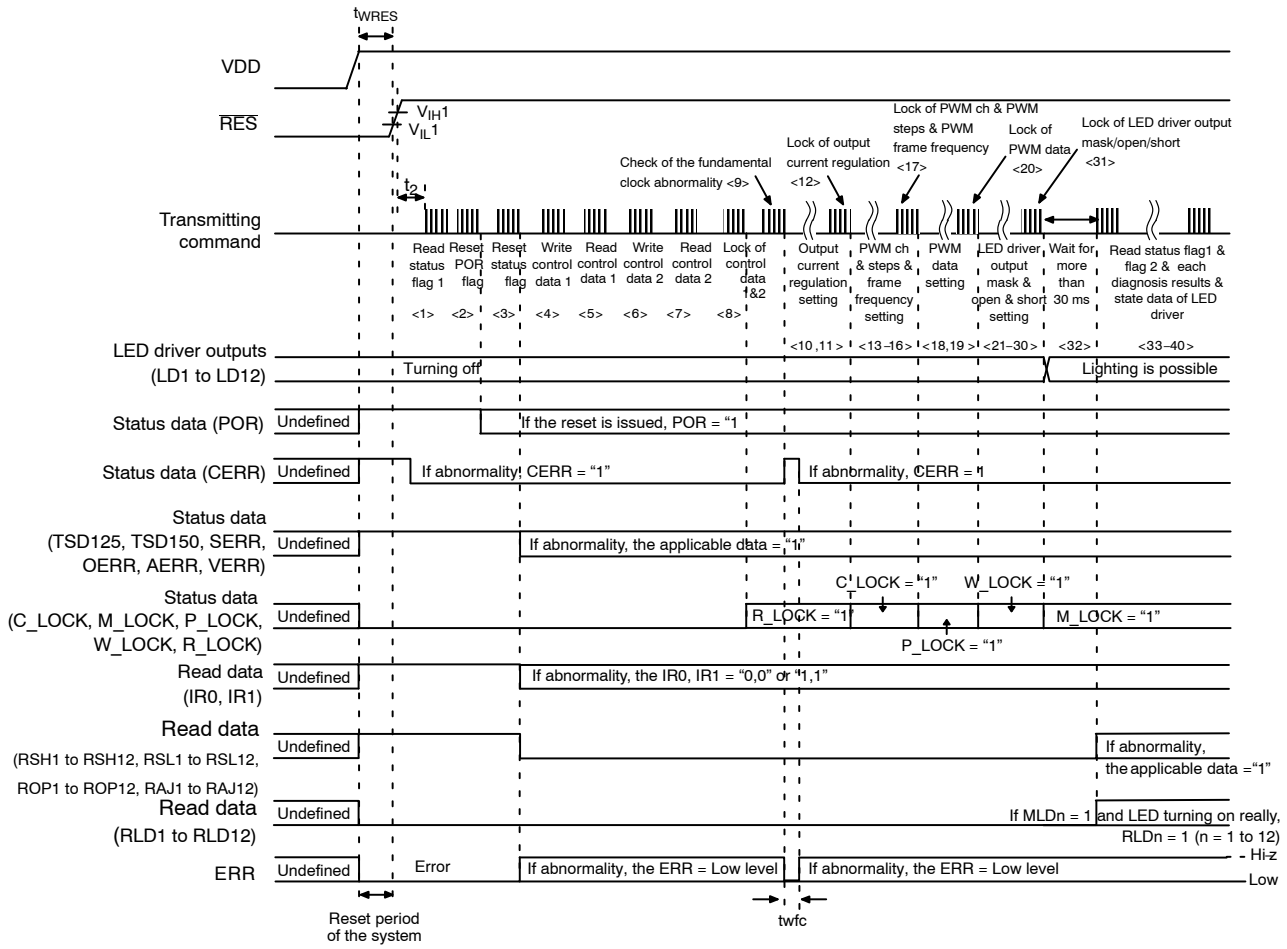
<17> Transmit the command [Lock of PWM ch & PWM steps & PWM frame frequency], and lock the PWM channel register (LnC, LnB, LnA) and the PWM steps register (WN1, WN0) and the PWM frame frequency register (PF3 to PF0).

<18> Transmit the command [Write PWM data], and set the PWM data (Wm9 to Wm0).

<19> Transmit the command [Read PWM data], and confirm the contents of PWM data register (Wm9 to Wm0).

<20> Transmit the command [Lock of PWM data], and lock the PWM data register (Wm9 to Wm0).
<21> Transmit the command [Write LED driver output mask], and set the LED driver output mask register (MLD1 to MLD12).
<22> Transmit the command [Read LED driver output mask], and confirm the contents of LED driver output mask register (MLD1 to MLD12).
<23> Transmit the command [Write VLED short detection circuit mask], and mask the VLED short detection circuit (MSH1 to MSH12).
<24> Transmit the command [Read VLED short detection circuit mask], and confirm the contents of VLED short detection circuit mask register (MSH1 to MSH12).
<25> Transmit the command [Write VSS short detection circuit mask], and mask the VSS short detection circuit (MSL1 to MSL12).
<26> Transmit the command [Read VSS short detection circuit mask], and confirm the contents of VSS short detection circuit mask register (MSL1 to MSL12).
<27> Transmit the command [Write open detection circuit mask], and mask the open detection circuit (MOP1 to MOP12).
<28> Transmit the command [Read open detection circuit mask], and confirm the contents of open detection circuit mask register (MOP1 to MOP12).
<29> Transmit the command [Write VLED short detection voltage setting], and set the VLED short detection voltage (VSHnB, VSHnA).
<30> Transmit the command [Read VLED short detection voltage setting], and confirm the contents of VLED short detection voltage setting register (VSHnB, VSHnA).
<31> Transmit the command [Lock of LED driver output mask/open/short], and lock the LED driver output mask register (MLD1 to MLD12) and the VLED short detection circuit mask register (MSH1 to MSH12) and the VSS short detection circuit mask register (MSL1 to MSL12) and the open detection circuit mask register (MOP1 to MOP12) and the VLED short detection voltage setting register (VSHnB, VSHnA). (It starts to turn on an LED.)
<32> Wait more than 30 msec.
<33> Transmit the command [Read status flag 1], and confirm the contents of status data (TSD125, TSD150, SERR, OERR, AERR, VERR). If the contents of these status data are abnormality, carry out those process from <36> to <40> as needed.
<34> Transmit the command [Read status flag 2], and confirm the contents of status data (R_LOCK, W_LOCK, P_LOCK, M_LOCK, C_LOCK). If the contents of these status data are abnormality, confirm the contents of various control data registers with regard to those lock command and set those command again.
<35> Transmit the command [Read external resistance diagnosis result], and confirm the contents of external resistance diagnosis result data (IR0, IR1).
<36> Transmit the command [Read VLED short detection result], and confirm the contents of VLED short detection result data (RSH1 to RSH12).
<37> Transmit the command [Read VSS short detection result], and confirm the contents of VSS short detection result data (RSL1 to RSL12).
<38> Transmit the command [Read open detection result], and confirm the contents of open detection result data (ROP1 to ROP12).
<39> Transmit the command [Read adjacent outputs short detection result], and confirm the contents of adjacent outputs short detection result data (RAJ1 to RAJ12).
<40> Transmit the command [Read the state data of the LED driver output], and confirm the contents of the state data of the LED driver output (RLD1 to RLD12).

NOTE: (n = 1 to 12, m = 1 to 6)



45. $t_{WRES} \geq 1$ [ms] (Reset time)
$t_2 \geq 1$ [ms] (Serial data input waiting time)
twfc ≤ 1/fosc (The fundamental clock waiting time, Internal oscillator operating mode (OC = "0"))
twfc ≤ $1/f_{OSCI}1$ or twfc ≤ $1/f_{OSCI}2$ (The fundamental clock waiting time, External clock operating mode (OC = "1"))

Figure 26. Start-up Sequence

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)†
LC75760UJA−AH	SSOP24 (225mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel

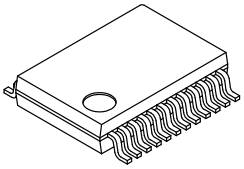
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

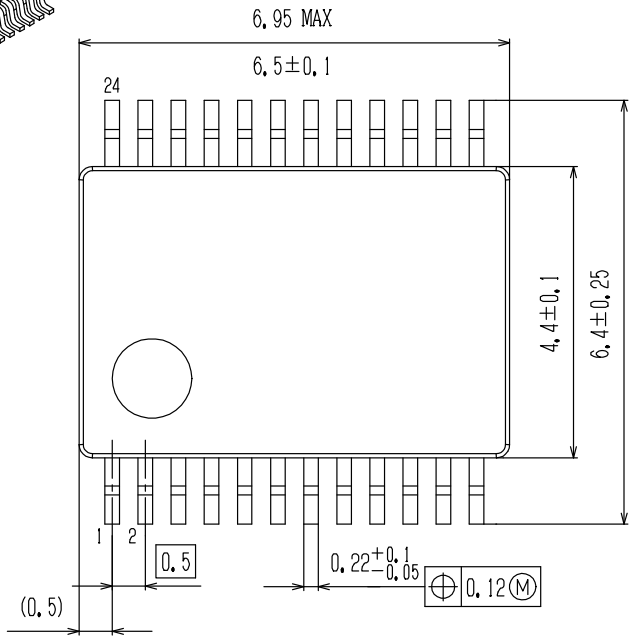
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

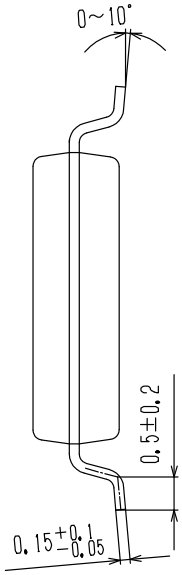
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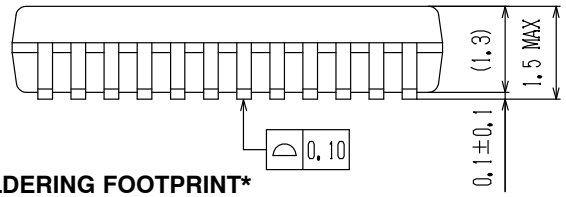
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ISSUE A

DATE 23 OCT 2013

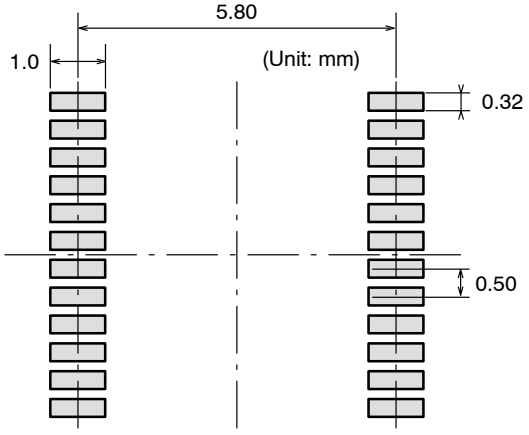








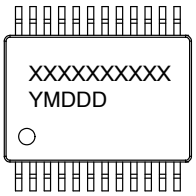
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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