MCX C141/142/242

Arm Cortex M0+ with 48 MHz 32-bit MCU, 32/64 KB Flash, 8/16 KB SRAM, USB

Rev. 4.1 — 19 August 2026 Product data sheet

- This document provides electrical specifications for MCX C141/142/241/242 family.
- For functional characteristics and the programming model, see MCX C24X Reference Manual (MCXC24XP64M48RM).

1 Introduction

Features

- ARM® Cortex®-M0+ 48 MHz with low power
- Up to 64 KB Flash, up to 16 KB SRAM, 16 KB Boot ROM
- USB FS 2.0 device without requiring an external crystal
- Embedded ROM with boot loader for flexible program upgrade
- FlexIO to support any standard and customized serial peripheral emulation
- Down to 46 µA/MHz in very low power run mode and 1.68 µA in stop mode (RAM + RTC retained)
- -40 °C to +125 °C (Tj) temperature range.

Cores

- ARM® Cortex®-M0+ core up to 48 MHz

Memories

- 32/64 KB program flash memory
- 8/16 KB SRAM
- 16 KB ROM with built-in bootloader
- 32-byte backup register

Security

- 80-bit unique identification number per chip
- Advanced flash security
- Hardware CRC module

System and clocks

- COP Software watchdog
- SWD debug interface and Micro Trace Buffer
- Bit Manipulation Engine
- 48 MHz high accuracy internal reference clock
- 8/2 MHz low power internal reference clock
- 32–40 kHz and 3–32 MHz crystal oscillator
- 1 kHz reference clock active under all low power modes (except VLLS0)

Communication Interfaces for Connectivity

- USB full-speed 2.0 device controller supporting crystal-less operation and keeping connections alive under ultralow power
- One UART module supporting ISO7816, operating up to 1.5 Mbit/s
- Two low-power UART modules supporting asynchronous operation in low-power modes
- Two I2C modules supporting up to 1 Mbit/s
- Two 16-bit SPI modules supporting up to 24 Mbit/s for SPI1 and 12 Mbit/s for SPI0
- One FlexIO module supporting emulation of additional UART, SPI, I2C, I2S, PWM and other serial modules, and so on

Analog

- One 16-bit ADC module with high accurate internal voltage reference, up to 20 channels and up to 818 ksps at equal to or less than 13-bit mode

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- High-speed analog comparator containing a 6-bit DAC for programmable reference input
- 1.2 V voltage reference (Vref)

Timers

- One 6-channel Timer/PWM module
- Two 2-channel Timer/PWM modules
- One low-power timer
- Periodic interrupt timer
- Real time clock

General-purpose input/outputs

- Up to 54 general-purpose input/output pins

Power Management

- Down to 46 µA/MHz in very low power run mode
- Down to 1.68 µA in stop mode (RAM + RTC retained)
- Six flexible static modes
- Low-leakage wakeup unit
- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range: -40 to 125 °C (Tj)

Target Applications

- Small to medium appliances
- Home security and surveillance
- Smart lighting
- Smart power socket
- DC fan

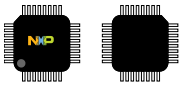
Table 1. Ordering information

Part number	Marking (Line1/ Line2)	Core Speed (MHz)	Flash (KB)	SRAM (KB)	GPIOs	USB	Package	Packing (P)
MCXC141VFM	MC141M	48	32	8	28	—	32QFN	Tray
MCXC141VLH	MCXC141VLH	48	32	8	54	—	64LQFP	Tray
MCXC242VLH	MCXC242VLH	48	64	16	51	Yes	64LQFP	Tray
MCXC142VFM	MC142M	48	64	16	28	—	32QFN	Tray
MCXC242VFM	MC242M	48	64	16	24	Yes	32QFN	Tray

All information provided in this document is subject to legal disclaimers.

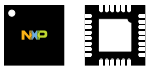
© 2026 NXP B.V. All rights reserved.

Table 2. Device isometric diagram



64 LQFP (LH)

10 x 10 x 1.6 mm 0.5 mm pitch



32 QFN (FM)

5 x 5 x 0.64 mm 0.5 mm pitch

The following figure shows the block diagram of this device:

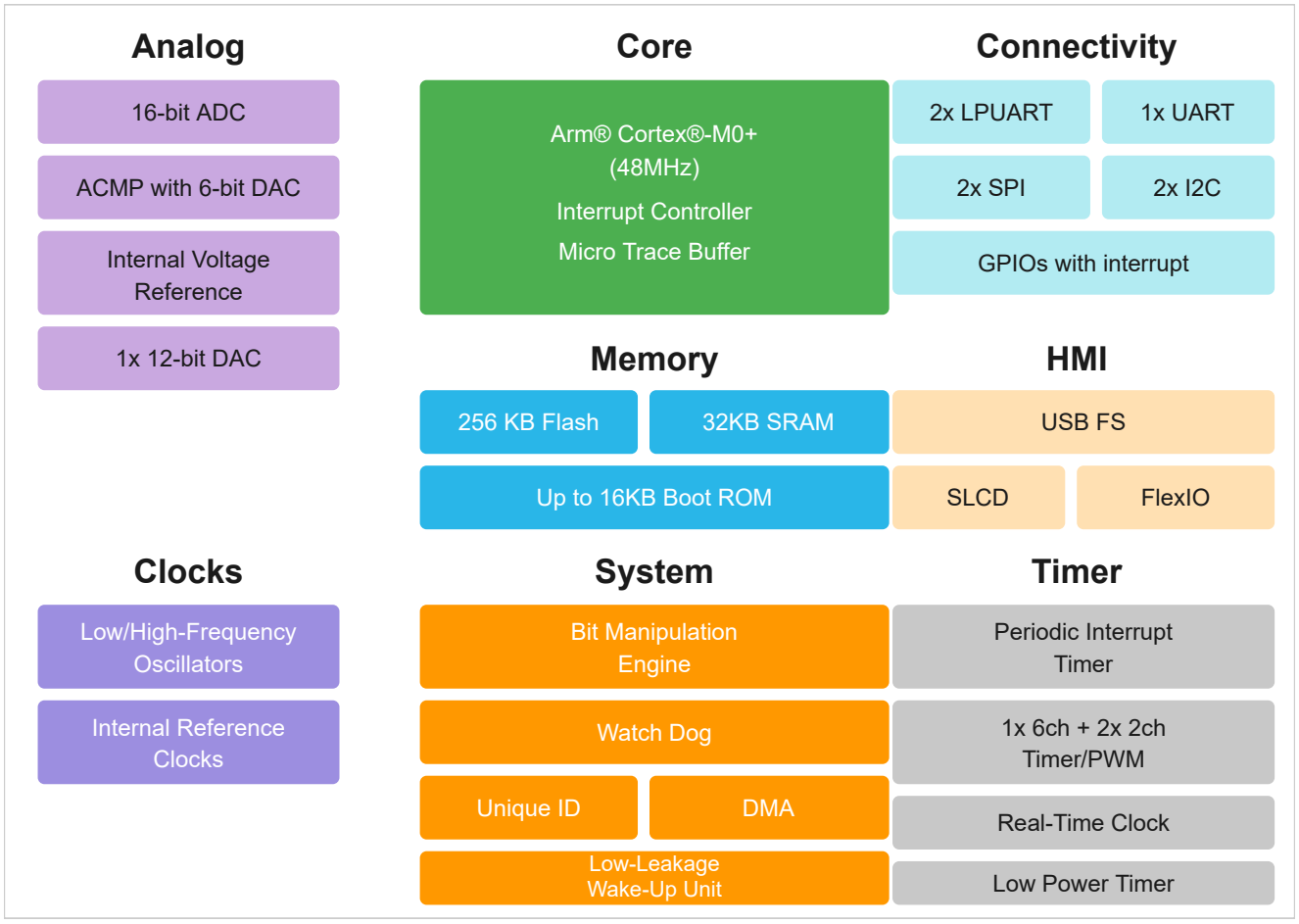


Figure 1. MCX C14x/24x/44x Block Diagram

The following figure shows the architecture diagram of this device:

© 2026 NXP B.V. All rights reserved.

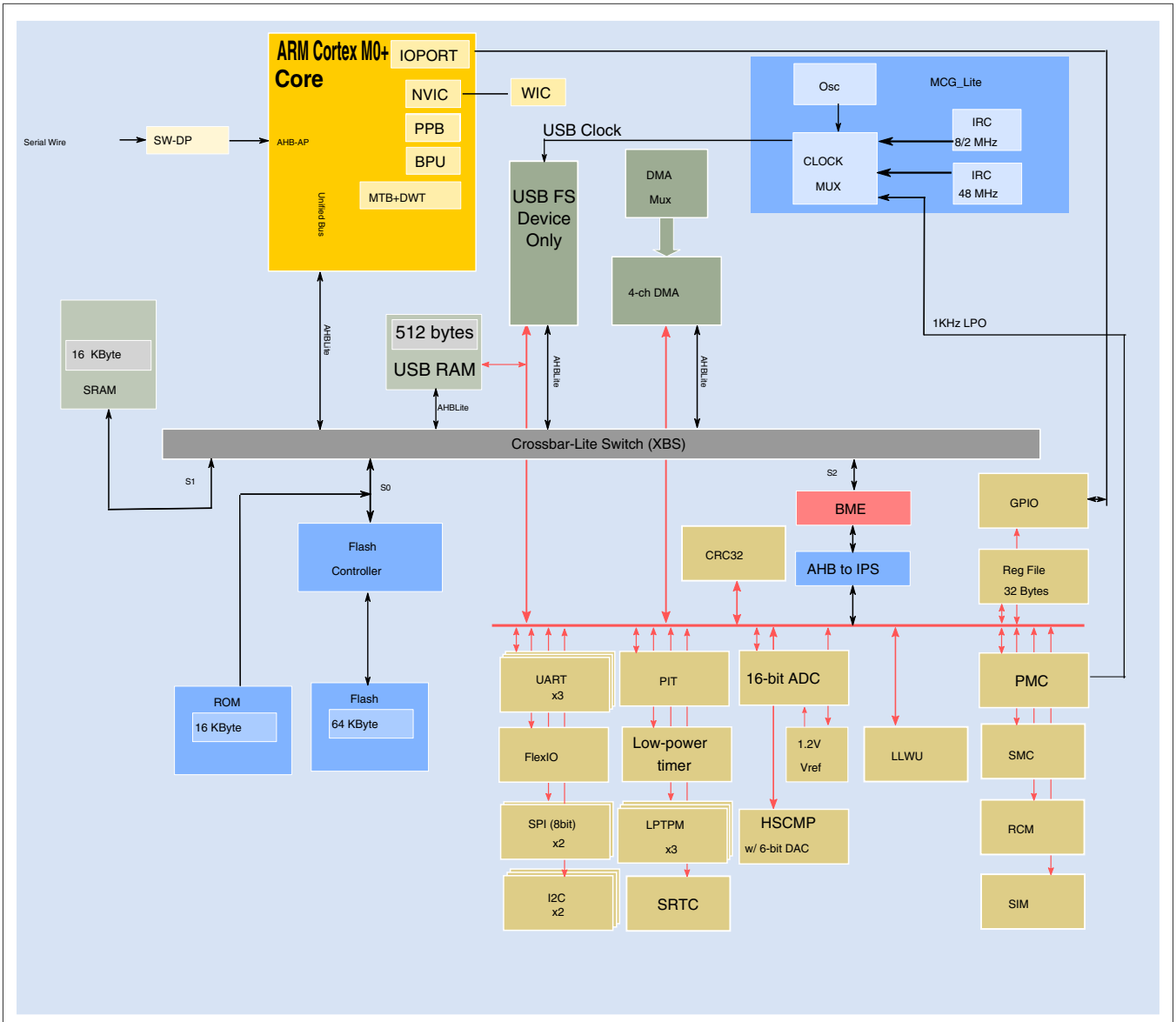


Figure 2. Architecture diagram

2 System features

The following sections describe the high-level system features.

2.1 ARM Cortex-M0+ core

The enhanced ARM Cortex M0+ is the member of the Cortex-M series of processors targeting microcontroller cores focused on very cost sensitive, low power applications. It has a single 32-bit AMBA AHB-Lite interface and includes an NVIC component. It also has hardware debug functionality including support for simple program trace capability. The processor supports the ARMv6-M instruction set (Thumb) architecture including all but three 16-bit Thumb opcodes (52 total) plus seven 32-bit instructions. It is upward compatible with other Cortex-M profile processors.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

2.2 NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 4 priority levels for interrupts. In the NVIC, each source in the IPR registers contains two bits. It also differs in number of interrupt sources and supports 32 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency to up to 15 clock cycles for Cortex-M0+. It also can be used to wake the MCU core from Wait and VLPW modes.

2.3 AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Stop and VLPS modes.

Wake-up sources are listed as below:

Table 3. AWIC stop wake-up sources

Wake-up source	Description
Available system resets	RESET pin with filter mode disabled or enabled when LPO is its clock source, COP when its clock source is enabled. COP can also work when its clock source is enabled during Stop mode.
Low-voltage detect	Power management controller—functional in Stop mode
Low-voltage warning	Power management controller—functional in Stop mode
Pin interrupts	Port control module—any enabled pin interrupt is capable of waking the system
ADC	The ADC is functional when using internal clock source or external crystal clock
CMP0	Interrupt in normal or trigger mode
I2Cx	Address match wakeup
LPUART0 , LPUART1	Any enabled interrupt can be a source as long as the module remains clocked
UART2	Active edge on RXD
RTC	Alarm or seconds interrupt
NMI	NMI pin
TPMx	Any enabled interrupt can be a source as long as the module remains clocked
LPTMR	Any enabled interrupt can be a source as long as the module remains clocked
SPIx	Slave mode interrupt
FlexIO	Any enabled interrupt can be a source as long as the module remains clocked
USB	Any enabled interrupt can be a source as long as the module remains clocked

2.4 Memory

This device has the following features:

- 8/16 KB of embedded RAM accessible (read/write) at CPU clock speed with 0 wait states.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- The non-volatile memory is divided into two arrays
  - 32/64 KB of embedded program memory
  - 16 KB ROM (built-in bootloader to support UART, I2C, USB, and SPI interfaces)

  The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 1 KB.

  The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

  The security circuitry prevents unauthorized access to RAM or flash contents from debug port.
- System register file

  This device contains a 32-byte register file that is powered in all power modes.

  Also, it retains contents during low power modes and is reset only during a power-on reset.

2.5 Reset and boot

The following table lists all the reset sources supported by this device.
Note: *In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the specific module is not reset by the corresponding Reset source.*

Table 4. Reset source

Reset sources	Descriptions	Modules								
		PMC	SIM	SMC	RCM	LLWU	Reset pin is negated	RTC	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	Y	Y	Y	Y
System resets	Low-voltage detect (LVD)	Y [1]	Y	Y	Y	Y	Y	N	Y	Y
	Low leakage wakeup (LLWU) reset	N	Y [2]	N	Y	N	Y [3]	N	N	Y
	External pin reset (RESET)	Y[1]	Y[2]	Y [4]	Y	Y	Y	N	N	Y
	Computer operating properly (COP) watchdog reset	Y[1]	Y[2]	Y[4]	Y [5]	Y	Y	N	N	Y
	Stop mode acknowledge error (SACKERR)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Software reset (SW)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Lockup reset (LOCKUP)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	MDM DAP system reset	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
Debug reset	Debug reset	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y

[1] Except PMC_LVDSC1[LVDV] and PMC_LVDSC2[LVWV]
[2] Except SIM_SOPT1
[3] Only if RESET is used to wake from VLLS mode.
[4] Except SMC_PMCTRL, SMC_STOPCTRL, SMC_PMSTAT
[5] Except RCM_RPFC, RCM_RPFW, RCM_FM

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

The CM0+ core adds support for a programmable Vector Table Offset Register (VTOR) to relocate the exception vector table after reset. This device supports booting from:

- internal flash
- boot ROM

The Flash Option (FOPT) register in the Flash Memory module (FTFA_FOPT) allows the user to customize the operation of the MCU at boot time. The register contains read-only bits that are loaded from the NVM's option byte in the flash configuration field. Below is boot flow chart for this device.

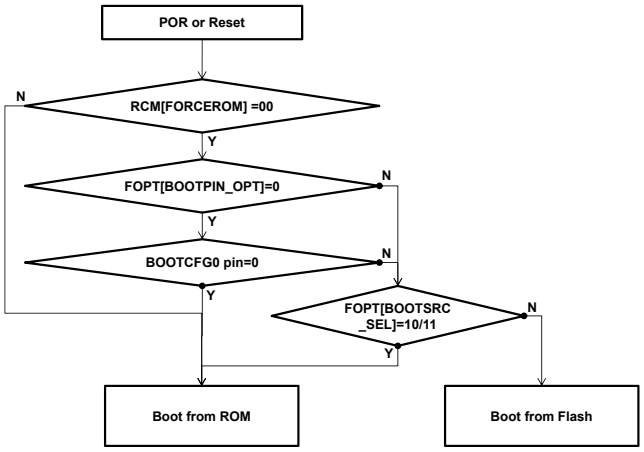


Figure 3. Boot flow chart

The blank chip is default to boot from ROM and remaps the vector table to ROM base address, otherwise, it remaps to flash address.

2.6 Clock options

This chip provides a wide range of sources to generate the internal clocks. These sources include internal resistor capacitor (IRC) oscillators, external oscillators, external clock sources, and ceramic resonators. These sources can be configured to provide the required performance and optimize the power consumption.

The IRC oscillators include the high-speed internal resistor capacitor (HIRC) oscillator, the low-speed internal resistor capacitor (LIRC) oscillator, and the low power oscillator (LPO).

The HIRC oscillator generates a 48 MHz clock and synchronizes with the USB clock in full speed mode to achieve the required accuracy.

The LIRC oscillator generates an 8 MHz or 2 MHz clock, and default to 8 MHz system clock on reset. The LIRC oscillator cannot be used in any VLLS modes.

The LPO generates a 1 kHz clock and cannot be used in VLLS0 mode.

The system oscillator supports low frequency crystals (32 kHz to 40 kHz), high frequency crystals (3 MHz to 32 MHz), and ceramic resonators (3 MHz to 32 MHz). An external clock source, DC to 48 MHz, can be used as the system clock through the EXTAL0 pin. The external oscillator also supports a low speed external clock (32.768 kHz) on the RTC_CLKIN pin for use with the RTC.

For more details on the clock operations and configurations, see Reference Manual.

The following figure is a high level block diagram of the clock generation.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

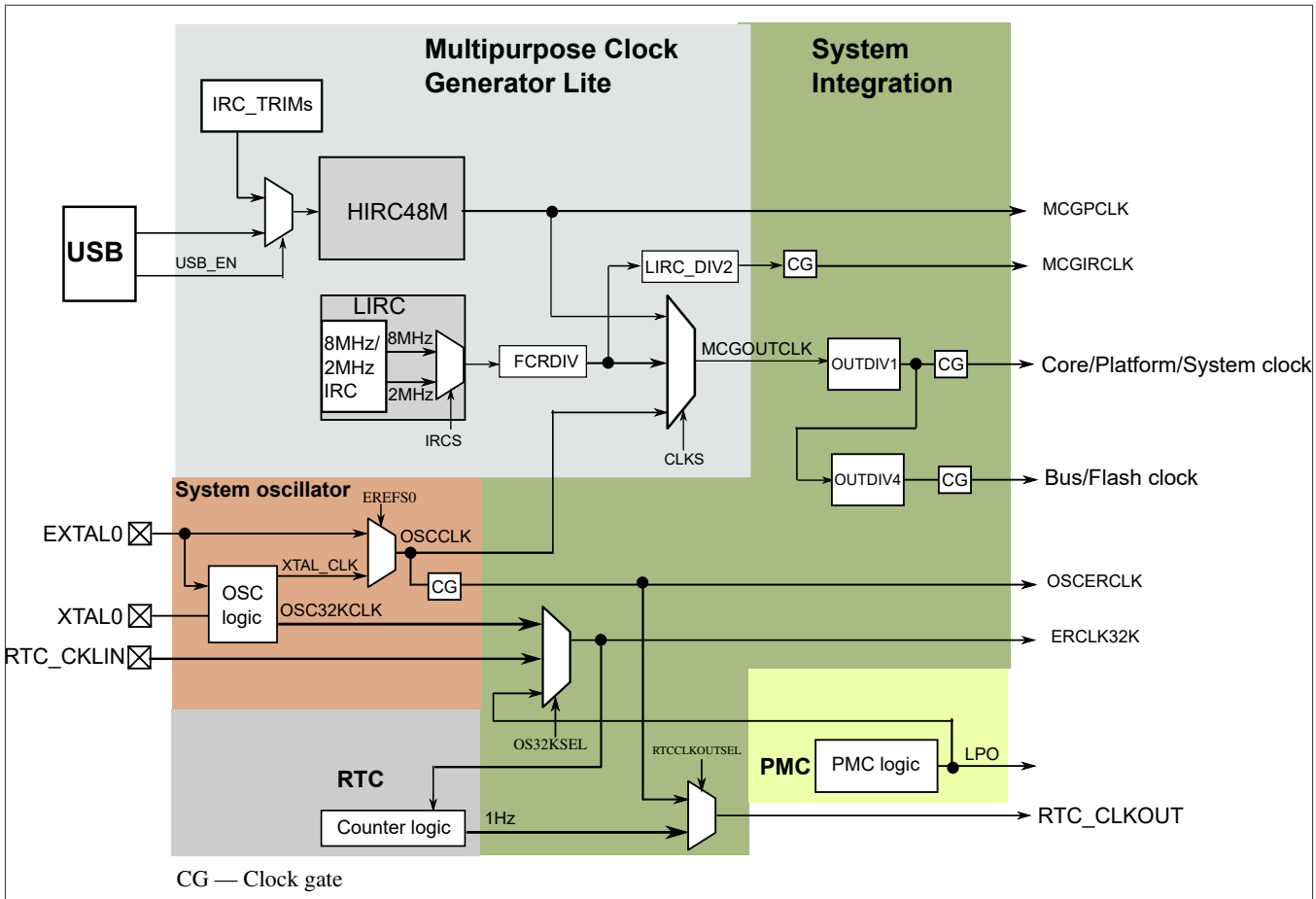


Figure 4. Clock block diagram

In order to provide flexibility, many peripherals can select from multiple clock sources for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

The following table summarizes the clocks associated with each module.

Table 5. Module clocks

Module	Bus interface clock	Internal clocks	I/O interface clocks
Core modules			
ARM Cortex-M0+ core	Platform clock	Core clock	—
NVIC	Platform clock	—	—
DAP	Platform clock	—	SWD_CLK
System modules			
DMA	System clock	—	—
DMA Mux	Bus clock	—	—

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 5. Module clocks*...continued*

Module	Bus interface clock	Internal clocks	I/O interface clocks
Port control	Bus clock	—	—
Crossbar Switch	Platform clock	—	—
Peripheral bridges	System clock	Bus clock	—
LLWU, PMC, SIM, RCM	Bus clock	LPO	—
Mode controller	Bus clock	—	—
MCM	Platform clock	—	—
COP watchdog	Bus clock	LPO, Bus Clock, MCGIRCLK, OSCERCLK	—
CRC	Bus clock	—	—
Clocks			
MCG_Lite	Bus clock	MCGOUTCLK, MCGPCLK, MCGIRCLK, OSCERCLK, ERCLK32K	—
OSC	Bus clock	OSCERCLK	—
Memory and memory interfaces			
Flash Controller	Platform clock	Flash clock	—
Flash memory	Flash clock	—	—
Analog			
ADC	Bus clock	OSCERCLK	—
CMP	Bus clock	—	—
Internal Voltage Reference (VREF)	Bus clock	—	—
Timers			
TPM	Bus clock	TPM clock	TPM_CLKIN0, TPM_CLKIN1
PIT	Bus clock	—	—
LPTMR	Bus clock	LPO, OSCERCLK, MCGPCLK, ERCLK32K	—
RTC	Bus clock	ERCLK32K	RTC_CLKOUT, RTC_CLKIN

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 5. Module clocks...*continued*

Module	Bus interface clock	Internal clocks	I/O interface clocks
Communication interfaces			
USB FS (Device Only)	System clock	USB FS clock	—
SPI0	Bus clock	—	SPI0_SCK
SPI1	System clock	—	SPI1_SCK
I2C0	System Clock	—	I2C0_SCL
I2C1	System Clock	—	I2C1_SCL
LPUART0, LPUART1	Bus clock	LPUART0 clock LPUART1 clock	—
UART2	Bus clock	—	—
FlexIO	Bus clock	FlexIO clock	—
Human-machine interfaces			
GPIO	Platform clock	—	—

2.7 Security

Security state can be enabled via programming flash configuration field (0x40e). After enabling device security, the SWD port cannot access the memory resources of the MCU, and ROM boot loader is also limited to access flash and not allowed to read out flash information via ROM boot loader commands.

Access interface	Secure state	Unsecure operation
SWD port	Cannot access memory source by SWD interface	The debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command
ROM boot loader Interface (UART/I2C/SPI/USB)	Limit access to the flash, cannot read out flash content	Send “FlashEraseAllUnsecureh" command or attempt to unlock flash security using the backdoor key

This device features 80-bit unique identification number, which is programmed in factory and loaded to SIM register after power-on reset.

2.8 Power management

The Power Management Controller (PMC) expands upon ARM’s operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM’s operational modes, See the ARM Cortex User Guide.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

The PMC provides Run (Run), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), and Very Low Leakage Stop (VLLS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC), and the Low Leakage Wake-Up Controller (LLWU) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes. The LLWU is used to wake up the MCU core from LLS and VLLSx modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, or the LLWU, please refer to the Reference Manual.

The following table provides information about the state of the peripherals in the various operational modes and the modules that can wake MCU from low power modes.

Table 6. Peripherals states in different operational modes

Core mode	Device mode	Descriptions
Run mode	Run	In Run mode, all device modules are operational.
	Very Low Power Run	In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled.
Sleep mode	Wait	In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode.
	Very Low Power Wait	In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode.
Deep sleep	Stop	In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, CMP, LPTimer, RTC, and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt.
	Very Low Power Stop	In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, TPM, FlexIO, LPUART, USB, and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt.
	Low Leakage Stop	In LLS mode, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), LLWU, LPTMR, and RTC are operational. The ADC, CRC, DMA, FlexIO, I2C, LPUART, MCG-Lite, NVIC, PIT, SPI, TPM,

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 6. Peripherals states in different operational modes...*continued*

Core mode	Device mode	Descriptions
		UART, USB, and COP are static, but retain their programming. The GPIO, and VREF are static, retain their programming, and continue to drive their previous values.
	Very Low Leakage Stop	In VLLS modes, most peripherals are powered off and will resume operation from their reset state when the device wakes up. The LLWU, LPTMR, and RTC are operational in all VLLS modes. In VLLS3, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The GPIO, and VREF are not operational but continue driving. In VLLS1, the contents of the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The GPIO, and VREF are not operational but continue driving. In VLLS0, the contents of the 32-byte system register file are retained. The PMC is operational. The GPIO is not operational but continues driving. The POR detection circuit can be enabled or disabled.

2.9 LLWU

The LLWU module is used to wake MCU from low leakage power mode (LLS and VLLSx) and functional only on entry into a low-leakage power mode. After recovery from LLS, the LLWU is immediately disabled. After recovery from VLLSx, the LLWU continues to detect wake-up events until the user has acknowledged the wake-up event.

This device uses 8 external wakeup pin inputs and 4 internal modules as wakeup sources to the LLWU module.

The following is internal peripheral and external pin inputs as wakeup sources to the LLWU module.

Table 7. Wakeup source

LLWU pin	Module source or pin name
LLWU_P5	PTB0
LLWU_P6	PTC1
LLWU_P7	PTC3
LLWU_P8	PTC4
LLWU_P9	PTC5
LLWU_P10	PTC6
LLWU_P14	PTD4
LLWU_P15	PTD6
LLWU_M0IF	LPTMR0
LLWU_M1IF	CMP0

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 7. Wakeup source*...continued*

LLWU pin	Module source or pin name
LLWU_M2IF	Reserved
LLWU_M3IF	Reserved
LLWU_M4IF	Reserved
LLWU_M5IF	RTC alarm
LLWU_M6IF	Reserved
LLWU_M7IF	RTC seconds

2.10 Debug controller

This device supports standard ARM 2-pin SWD debug port. It provides register and memory accessibility from the external debugger interface, basic run/halt control plus 2 breakpoints and 2 watchpoints.

It also supports trace function with the Micro Trace Buffer (MTB), which provides a simple execution trace capability for the Cortex-M0+ processor.

2.11 COP

The COP monitors internal system operation and forces a reset in case of failure. It can run from bus clock, LPO, 8/2 MHz internal oscillator or external crystal oscillator. Optional window mode can detect deviations in program flow or system frequency.

The COP has the following features:

- Support multiple clock input, 1 kHz clock(LPO), bus clock, 8/2 MHz internal reference clock, external crystal oscillator
- Can work in Stop/VLPS and Debug mode
- Configurable for short and long timeout values, the longest timeout is up to 262 seconds
- Support window mode

3 Peripheral features

The following sections describe the features of each peripherals of the chip.

3.1 BME

The Bit Manipulation Engine (BME) provides hardware support for atomic read-modify-write memory operations to the peripheral address space in Cortex-M0+ based microcontrollers. It reduces up to 30% of the code size and up to 9% of the cycles for bit-oriented operations to peripheral registers.

The BME supports unsigned bit field extract, load-and-set 1-bit, load-and-clear 1-bit, bit field insert, logical AND/OR/XOR operations with byte, halfword or word-sized data type.

3.2 DMA and DMAMUX

The DMA controller module enables fast transfers of data, which provides an efficient way to move blocks of data with minimal processor interaction. The DMA controller in this device implements four channels which can be routed from up to 63 DMA request sources through DMA MUX module. Some of the peripheral request sources have asynchronous DMA capability which can be used to wake MCU from Stop mode. The peripherals which have such capability include LPUART0, LPUART1, FlexIO, TPM0-TPM2, ADC0, CMP0, PORTA-PORTE. The DMA channel 0 and 1 can be periodically triggered by PIT via DMA MUX.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Main features are listed below:

- Dual-address transfers via 32-bit master connection to the system bus and data transfers in 8-, 16-, or 32-bit blocks
  - Supports programmable source and destination address and transfer size, optional modulo addressing from 16 bytes to 256 KB
  - Automatic updates of source and destination addresses
  - Auto-alignment feature for source or destination accesses allows block transfers to occur at the optimal size based on the address, byte count,and programmed size, which significantly improves the speed of block transfer
  - Automatic single or double channel linking allows the current DMA channel to automatically trigger a DMA request to the linked channels without CPU intervention

3.3 TPM

This device contains three low power TPM modules (TPM). All TPM modules are functional in Stop/VLPS mode if the clock source is enabled.

The TPM features include:

- TPM clock mode is selectable from external clock input or internal clock source, HIRC48M clock, external crystal input clock or LIRC2M/8M clock.
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- TPM includes a 16-bit counter
- Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
- Support the generation of an interrupt and/or DMA request per channel or counter overflow
- Support selectable trigger input to optionally reset or cause the counter to start or stop incrementing
- Support the generation of hardware triggers when the counter overflows and per channel

3.4 ADC

This device contains one ADC module. This ADC module supports hardware triggers from TPM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

- Linear successive approximation algorithm with up to 16-bit resolution
- Up to four pairs of differential and 17 single-ended external analog inputs
- Support selectable 16-bit, 13-bit, 11-bit, and 9-bit differential output mode, or 16-bit, 12-bit, 10-bit, and 8-bit single-ended output modes
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Selectable clock source up to four
- Operation in low-power modes for lower noise
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- Hardware average function up to 32x
- Selectable voltage reference: external or alternate
- Self-Calibration mode

3.4.1 Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see Table 59 for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031. We recommend to use internal reference voltage as ADC reference with long sample time.

3.5 VREF

The Voltage Reference (VREF) can supply an accurate voltage output (1.2 V typically) trimmed in 0.5 mV steps. It can be used in applications to provide a reference voltage to external devices or used internally as a reference to analog peripherals such as the ADC or CMP.

The VREF supports the following programmable buffer modes:

- Bandgap on only, used for stabilization and startup
- High power buffer mode
- Low-power buffer mode
- Buffer disabled

The VREF voltage output signal, bonded on VREFH for 64 LQFP packages and on PTE30 for 32 QFN, can be used by both internal and external peripherals in low and high power buffer mode. A 100 nF capacitor must always be connected between this pin and VSSA if the VREF is used. This capacitor must be as close to the VREFO pin as possible.

3.6 CMP

The device contains one high-speed comparator and two 8-input multiplexers for both the inverting and non-inverting inputs of the comparator. Each CMP input channel connects to both muxes.

The CMP includes one 6-bit DAC, which provides a selectable voltage reference for various user application cases. Besides, the CMP also has several module-to-module interconnects in order to facilitate ADC triggering, TPM triggering, and interfaces.

The CMP has the following features:

- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising or falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, digitally filtered
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels: shorter propagation delay at the expense of higher power and Low power with longer propagation delay
- DMA transfer support
- Functional in all modes of operation except in VLLS0 mode
- The filter functions are not available in Stop, VLPS, LLS, or VLLSx modes
- Integrated 6-bit DAC with selectable supply reference source and can be power down to conserve power
- Two 8-to-1 channel mux

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

3.7 RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator or clock directly from RTC_CLKIN pin.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers.

The RTC module has the following features

- 32-bit seconds counter with roll-over protection and 32-bit alarm
- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection with register lock mechanism
- 1 Hz square wave or second pulse output with optional interrupt

3.8 PIT

The Periodic Interrupt Timer (PIT) is used to generate periodic interrupt to the CPU. It has two independent channels and each channel has a 32-bit counter. Both channels can be chained together to form a 64-bit counter.

Channel 0 can be used to periodically trigger DMA channel 0, and channel 1 can be used to periodically trigger DMA channel 1. Either channel can be programmed as an ADC trigger source, or TPM trigger source. Channel 0 can be programmed to trigger DAC.

The PIT module has the following features:

- Each 32-bit timers is able to generate DMA trigger
- Each 32-bit timers is able to generate timeout interrupts
- Two timers can be cascaded to form a 64-bit timer
- Each timer can be programmed as ADC/TPM trigger source
- Timer 0 is able to trigger DAC

3.9 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
    - Hardware trigger output
    - Counter supports free-running mode or reset on compare
  - Configurable clock source for prescaler/glitch filter
  - Configurable input source for pulse counter

3.10 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

3.11 UART

This device contains a basic universal asynchronous receiver/transmitter (UART) module with DMA function supported. Generally, this module is used in RS-232, RS-485, and other communications and supports LIN slave operation and ISO7816.

The UART module has the following features:

- Full-duplex operation
- 13-bit baud rate selection with /32 fractional divide, based on the module clock frequency
- Programmable 8-bit or 9-bit data format
- Programmable transmitter output polarity
- Programmable receive input polarity
- Up to 14-bit break character transmission.
- 11-bit break character detection option
- Two receiver wakeup methods with idle line or address mark wakeup
- Address match feature in the receiver to reduce address mark wakeup ISR overhead
- Ability to select MSB or LSB to be first bit on wire
- Support for ISO 7816 protocol to interface with SIM cards and smart cards
- Receiver framing error detection
- Hardware parity generation and checking
- 1/16 bit-time noise detection
- DMA interface

3.12 LPUART

This product contains two Low-Power UART modules, both of their clock sources are selectable from IRC48M, IRC8M/2M or external crystal clock, and can work in Stop and VLPS modes. They also support 4× to 32× data oversampling rate to meet different applications.

The LPUART module has the following features:

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4× to 32×
- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods
  - Idle line wakeup
  - Address mark wakeup

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

3.13 SPI

This device contains two SPI modules. SPI modules support 8-bit and 16-bit modes. FIFO function is available only on SPI1 module.

The SPI modules have the following features:

- Full-duplex or single-wire bidirectional mode
- Programmable transmit bit rate
- Double-buffered transmit and receive data register
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8- or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed/large amounts of data transfers
- Support DMA

3.14 I2C

This device contains two I2C modules, which support up to 1 Mbits/s by dual buffer features, and address match to wake MCU from the low power mode.

I2C modules support DMA transfer, and the interrupt condition can trigger DMA request when DMA function is enabled.

The I2C modules have the following features:

- Support for system management bus (SMBus) Specification, version 2
- Software programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation and detection
- Repeated START signal generation and detection
- Acknowledge bit generation and detection

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- Bus busy detection
- General call recognition
- 10-bit address extension
- Programmable input glitch filter
- Low power mode wakeup on slave address match
- Range slave address support
- DMA support
- Double buffering support to achieve higher baud rate

3.15 USB

This device contains one USB module which implements a USB2.0 full-speed compliant peripheral and interfaces to the on-chip USBFS transceiver. It implements keep-alive feature to avoid re-enumerating when exiting from low power modes and enables HIRC48M to allow crystal-less USB operation.

The USBFS has the following features:

- USB 1.1 and 2.0 compliant full-speed device controller
- 16 bidirectional end points
- DMA or FIFO data stream interfaces
- Low-power consumption
- HIRC48 with clock-recovery is supported to eliminate the 48 MHz crystal. It is used for USB device-only implementation.
- USB keeps alive in low power mode down to VLPS and is able to wake MCU from low power mode

3.16 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to UART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/ Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation.

The FlexIO module has the following features:

- Functional in VLPR/VLPW/Stop/VLPS mode provided the clock it is using remains enabled
- Four 32-bit double buffered shift registers with transmit, receive, and data match modes, and continuous data transfer
- The timing of the shifter' shift, load and store events are controlled by the highly flexible 16-bit timer assigned to the shifter
- Two or more shifter can be concatenated to support large data transfer sizes
- Each 16-bit timers operates independently, supports for reset, enable and disable on a variety of internal or external trigger conditions with programmable trigger polarity
- Flexible pin configuration supporting output disabled, open drain, bidirectional output data and output mode
- Supports interrupt, DMA or polled transmit/receive operation

3.17 Port control and GPIO

The Port Control and Interrupt (PORT) module provides support for port control, digital filtering, and external interrupt functions. The GPIO data direction and output data registers control the direction and output data of each pin when the pin is configured for the GPIO function. The GPIO input data register displays the logic value on each pin when the pin is configured for any digital function, provided the corresponding Port Control and Interrupt module for that pin is enabled.

The following figure shows the basic I/O pad structure. This diagram applies to all I/O pins except PTA20/RESET_b and those configured as pseudo open-drain outputs.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

PTA20/RESET_b is a true open-drain pin without p-channel output driver or diode to the ESD bus. Pseudo open-drain pins have the p-channel output driver disabled when configured for open-drain operation. None of the I/O pins, including open-drain and pseudo open-drain pins, are allowed to go above VDD.

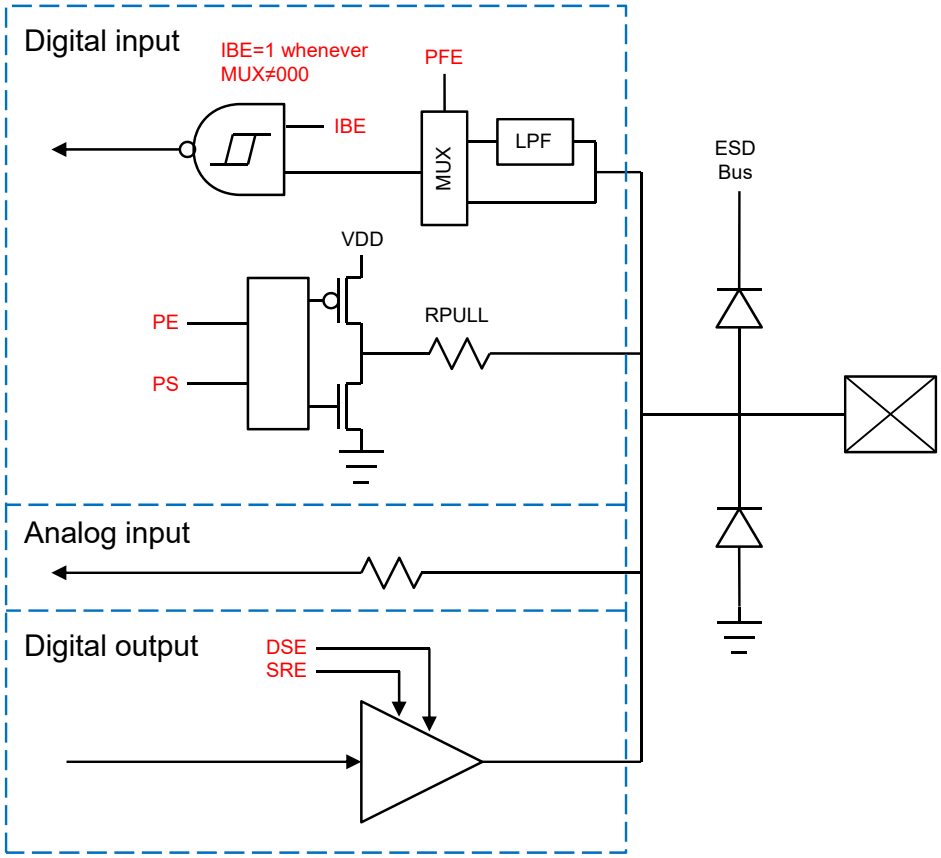


Figure 5. I/O simplified block diagram

The PORT module has the following features:

- All PIN support interrupt enable
- Configurable edge(rising,falling,both) or level sensitive interrupt type
- Support DMA request
- Asynchronous wake-up in low-power modes
- Configurable pullup, pulldown, and pull-disable on select pins
- Configurable high and low drive strength on selected pins
- Configurable fast and slow slew rates on selected pins
- Configurable passive filter on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to chip-specific digital functions
- Pad configuration fields are functional in all digital pin muxing modes.

The GPIO module has the following features:

- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- GPIO support single-cycle access via fast GPIO.

4 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. The following figure shows the system memory and peripheral locations

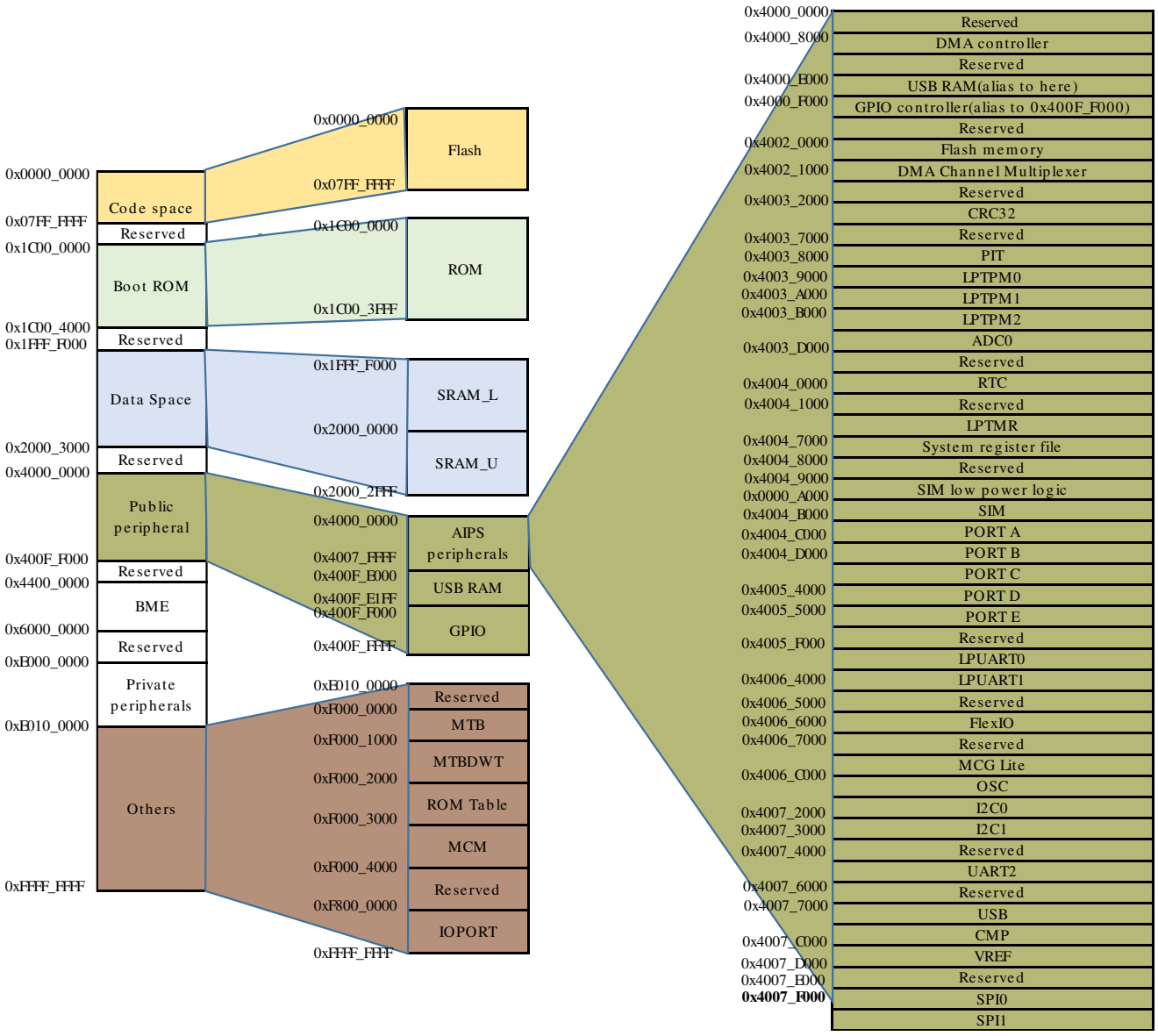


Figure 6. Memory map

5 Pinouts

© 2026 NXP B.V. All rights reserved.

5.1 Signal Multiplexing and Pin Assignments

5.1.1 MCX C24X signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 8. MCX C24X signal multiplexing and pin assignments

64LQFP	32QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	9	VREF0	VREF0_B	VREF0_B							
1	1	PTE0	DISABLED		PTE0/CLKOUT32K	SPI1_MISO	LPUART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	
2	—	PTE1	DISABLED		PTE1	SPI1_MOSI	LPUART1_RX		SPI1_MISO	I2C1_SCL	
3	—	VDD	VDD	VDD							
4	2	VSS	VSS	VSS							
5	3	USB0_DP	USB0_DP	USB0_DP							
6	4	USB0_DM	USB0_DM	USB0_DM							
7	5	USB_VDD	USB_VDD	USB_VDD							
8	6	PTE16	ADC0_DP1/ADC0_SE1	ADC0_DP1/ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_CLKIN0		FXIO0_D0	
9	—	PTE20	ADC0_DP0/ADC0_SE0	ADC0_DP0/ADC0_SE0	PTE20		TPM1_CH0	LPUART0_TX		FXIO0_D4	
10	—	PTE21	ADC0_DM0/ADC0_SE4a	ADC0_DM0/ADC0_SE4a	PTE21		TPM1_CH1	LPUART0_RX		FXIO0_D5	
11	—	PTE22	ADC0_DP3/ADC0_SE3	ADC0_DP3/ADC0_SE3	PTE22		TPM2_CH0	UART2_TX		FXIO0_D6	
12	—	PTE23	ADC0_DM3/ADC0_SE7a	ADC0_DM3/ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX		FXIO0_D7	
13	7	VDDA	VDDA	VDDA							

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 8. MCX C24X signal multiplexing and pin assignments...*continued*

64LQFP	32QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
14	7	VREFH	VREFH	VREFH							
14	—	VREFO	VREFO_A	VREFO_A							
15	8	VREFL	VREFL	VREFL							
16	8	VSSA	VSSA	VSSA							
17	—	PTE29	CMP0_IN5/ADC0_SE4b	CMP0_IN5/ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKIN0			
18	9	PTE30	ADC0_SE23/CMP0_IN4	ADC0_SE23/CMP0_IN4	PTE30		TPM0_CH3	TPM_CLKIN1	LPUART1_TX	LPTMR0_ALT1	
19	—	PTE31	DISABLED		PTE31		TPM0_CH4				
20	—	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
21	—	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
22	10	PTA0	SWD_CLK		PTA0		TPM0_CH5				SWD_CLK
23	11	PTA1	DISABLED		PTA1	LPUART0_RX	TPM2_CH0				
24	12	PTA2	DISABLED		PTA2	LPUART0_TX	TPM2_CH1				
25	13	PTA3	SWD_DIO		PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
26	14	PTA4	NMI_b		PTA4	I2C1_SDA	TPM0_CH1				NMI_b
27	—	PTA5	DISABLED		PTA5	USB_CLKIN	TPM0_CH2				
28	—	PTA12	DISABLED		PTA12		TPM1_CH0				
29	—	PTA13	DISABLED		PTA13		TPM1_CH1				
30	15	VDD	VDD	VDD							
31	16	VSS	VSS	VSS							

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 8. MCX C24X signal multiplexing and pin assignments...*continued*

64LQFP	32QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
32	17	PTA18	EXTAL0	EXTAL0	PTA18		LPUART1_RX	TPM_CLKIN0			
33	18	PTA19	XTAL0	XTAL0	PTA19		LPUART1_TX	TPM_CLKIN1		LPTMR0_ALT1	
34	19	PTA20	RESET_b		PTA20						RESET_b
35	20	PTB0/LLWU_P5	ADC0_SE8	ADC0_SE8	PTB0/LLWU_P5	I2C0_SCL	TPM1_CH0	SPI1_MOSI	SPI1_MISO		
36	21	PTB1	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	TPM1_CH1	SPI1_MISO	SPI1_MOSI		
37	—	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	TPM2_CH0				
38	—	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	TPM2_CH1				
39	—	PTB16	DISABLED		PTB16	SPI1_MOSI	LPUART0_RX	TPM_CLKIN0	SPI1_MISO		
40	—	PTB17	DISABLED		PTB17	SPI1_MISO	LPUART0_TX	TPM_CLKIN1	SPI1_MOSI		
41	—	PTB18	DISABLED		PTB18		TPM2_CH0				
42	—	PTB19	DISABLED		PTB19		TPM2_CH1				
43	—	PTC0	ADC0_SE14	ADC0_SE14	PTC0		EXTRG_IN	audioUSB_SOF_OUT	CMP0_OUT		
44	22	PTC1/LLWU_P6/RTC_CLKIN	ADC0_SE15	ADC0_SE15	PTC1/LLWU_P6/RTC_CLKIN	I2C1_SCL		TPM0_CH0			
45	23	PTC2	ADC0_SE11	ADC0_SE11	PTC2	I2C1_SDA		TPM0_CH1			
46	24	PTC3/LLWU_P7	DISABLED		PTC3/LLWU_P7	SPI1_SCK	LPUART1_RX	TPM0_CH2	CLKOUT		
47	—	VSS	VSS	VSS							
48	—	VDD	VDD	VDD							

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 8. MCX C24X signal multiplexing and pin assignments...*continued*

64LQFP	32QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
49	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	LPUART1_TX	TPM0_CH3	SPI1_PCS0		
50	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2			CMP0_OUT	
51	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN		SPI0_MISO		
52	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO	audioUSB_SOF_OUT		SPI0_MOSI		
53	—	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4				
54	—	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5				
55	—	PTC10	DISABLED		PTC10	I2C1_SCL					
56	—	PTC11	DISABLED		PTC11	I2C1_SDA					
57	—	PTD0	DISABLED		PTD0	SPI0_PCS0		TPM0_CH0		FXIO0_D0	
58	—	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1		FXIO0_D1	
59	—	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXIO0_D2	
60	—	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXIO0_D3	
61	29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4		FXIO0_D4	
62	30	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5		FXIO0_D5	
63	31	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	LPUART0_RX	I2C1_SDA	SPI1_MISO	FXIO0_D6	
64	32	PTD7	DISABLED		PTD7	SPI1_MISO	LPUART0_TX	I2C1_SCL	SPI1_MOSI	FXIO0_D7	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

5.1.2 MCX C14X signal multiplexing and pin assignments

The following table shows the signals available on each pin for the MCX C14X devices. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 9. C14 Pin Multiplexing Table

64LQFP	32QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	9	VREF0	VREF0_B	VREF0_B							
1	1	PTE0	DISABLED		PTE0/CLKOUT32K	SPI1_MISO	LPUART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	
2	2	PTE1	DISABLED		PTE1	SPI1_MOSI	LPUART1_RX		SPI1_MISO	I2C1_SCL	
3	—	VDD	VDD	VDD							
4	—	VSS	VSS	VSS							
5	3	PTE16	ADC0_DP1/ADC0_SE1	ADC0_DP1/ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_CLKIN0		FXIO0_D0	
6	4	PTE17	ADC0_DM1/ADC0_SE5a	ADC0_DM1/ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	TPM_CLKIN1	LPTMR0_ALT3	FXIO0_D1	
7	5	PTE18	ADC0_DP2/ADC0_SE2	ADC0_DP2/ADC0_SE2	PTE18	SPI0_MOSI		I2C0_SDA	SPI0_MISO	FXIO0_D2	
8	6	PTE19	ADC0_DM2/ADC0_SE6a	ADC0_DM2/ADC0_SE6a	PTE19	SPI0_MISO		I2C0_SCL	SPI0_MOSI	FXIO0_D3	
9	—	PTE20	ADC0_DP0/ADC0_SE0	ADC0_DP0/ADC0_SE0	PTE20		TPM1_CH0	LPUART0_TX		FXIO0_D4	
10	—	PTE21	ADC0_DM0/ADC0_SE4a	ADC0_DM0/ADC0_SE4a	PTE21		TPM1_CH1	LPUART0_RX		FXIO0_D5	
11	—	PTE22	ADC0_DP3/ADC0_SE3	ADC0_DP3/ADC0_SE3	PTE22		TPM2_CH0	UART2_TX		FXIO0_D6	

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 9. C14 Pin Multiplexing Table*...continued*

64LQFP	32QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
12	—	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX		FXIO0_D7	
13	7	VDDA	VDDA	VDDA							
14	7	VREFH	VREFH	VREFH							
14	—	VREFO	VREFO_A	VREFO_A							
15	8	VREFL	VREFL	VREFL							
16	8	VSSA	VSSA	VSSA							
17	—	PTE29	CMP0_IN5/ ADC0_SE4b	CMP0_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKIN0			
18	9	PTE30	ADC0_SE23/ CMP0_IN4	ADC0_SE23/ CMP0_IN4	PTE30		TPM0_CH3	TPM_CLKIN1	LPUART1_TX	LPTMR0_ALT1	
19	—	PTE31	DISABLED		PTE31		TPM0_CH4				
20	—	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
21	—	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
22	10	PTA0	SWD_CLK		PTA0		TPM0_CH5				SWD_CLK
23	11	PTA1	DISABLED		PTA1	LPUART0_RX	TPM2_CH0				
24	12	PTA2	DISABLED		PTA2	LPUART0_TX	TPM2_CH1				
25	13	PTA3	SWD_DIO		PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
26	14	PTA4	NMI_b		PTA4	I2C1_SDA	TPM0_CH1				NMI_b
27	—	PTA5	DISABLED		PTA5	USB_CLKIN	TPM0_CH2				
28	—	PTA12	DISABLED		PTA12		TPM1_CH0				

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 9. C14 Pin Multiplexing Table*...continued*

64LQFP	32QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
29	—	PTA13	DISABLED		PTA13		TPM1_CH1				
30	15	VDD	VDD	VDD							
31	16	VSS	VSS	VSS							
32	17	PTA18	EXTAL0	EXTAL0	PTA18		LPUART1_RX	TPM_CLKIN0			
33	18	PTA19	XTAL0	XTAL0	PTA19		LPUART1_TX	TPM_CLKIN1		LPTMR0_ALT1	
34	19	PTA20	RESET_b		PTA20						RESET_b
35	20	PTB0/LLWU_P5	ADC0_SE8	ADC0_SE8	PTB0/LLWU_P5	I2C0_SCL	TPM1_CH0	SPI1_MOSI	SPI1_MISO		
36	21	PTB1	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	TPM1_CH1	SPI1_MISO	SPI1_MOSI		
37	—	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	TPM2_CH0				
38	—	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	TPM2_CH1				
39	—	PTB16	DISABLED		PTB16	SPI1_MOSI	LPUART0_RX	TPM_CLKIN0	SPI1_MISO		
40	—	PTB17	DISABLED		PTB17	SPI1_MISO	LPUART0_TX	TPM_CLKIN1	SPI1_MOSI		
41	—	PTB18	DISABLED		PTB18		TPM2_CH0				
42	—	PTB19	DISABLED		PTB19		TPM2_CH1				
43	—	PTC0	ADC0_SE14	ADC0_SE14	PTC0		EXTRG_IN		CMP0_OUT		
44	22	PTC1/LLWU_P6/RTC_CLKIN	ADC0_SE15	ADC0_SE15	PTC1/LLWU_P6/RTC_CLKIN	I2C1_SCL		TPM0_CH0			
45	23	PTC2	ADC0_SE11	ADC0_SE11	PTC2	I2C1_SDA		TPM0_CH1			
46	24	PTC3/LLWU_P7	DISABLED		PTC3/LLWU_P7	SPI1_SCK	LPUART1_RX	TPM0_CH2	CLKOUT		

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 9. C14 Pin Multiplexing Table*...continued*

64LQFP	32QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
47	—	VSS	VSS	VSS							
48	—	VDD	VDD	VDD							
49	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	LPUART1_TX	TPM0_CH3	SPI1_PCS0		
50	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2			CMP0_OUT	
51	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN		SPI0_MISO		
52	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO			SPI0_MOSI		
53	—	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4				
54	—	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5				
55	—	PTC10	DISABLED		PTC10	I2C1_SCL					
56	—	PTC11	DISABLED		PTC11	I2C1_SDA					
57	—	PTD0	DISABLED		PTD0	SPI0_PCS0		TPM0_CH0		FXIO0_D0	
58	—	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1		FXIO0_D1	
59	—	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXIO0_D2	
60	—	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXIO0_D3	
61	29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4		FXIO0_D4	
62	30	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5		FXIO0_D5	
63	31	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	LPUART0_RX	I2C1_SDA	SPI1_MISO	FXIO0_D6	
64	32	PTD7	DISABLED		PTD7	SPI1_MISO	LPUART0_TX	I2C1_SCL	SPI1_MOSI	FXIO0_D7	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

5.2 Pin properties

The following table lists the pin properties.

Table 10. Pin properties

64 LQFP	32 QFN	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
—	—	PTE17	ND	Hi-Z	—	FS	N	N	Y
—	—	PTE18	ND	Hi-Z	—	FS	N	N	Y
—	9	VREF0	—	—	—	—	—	—	—
—	—	NC	—	—	—	—	—	—	—
1	1	PTE0	ND	Hi-Z	—	FS	N	N	Y
2	—	PTE1	ND	Hi-Z	—	FS	N	N	Y
3	—	VDD	—	—	—	—	—	—	—
4	2	VSS	—	—	—	—	—	—	—
5	3	USB0_DP	—	—	—	—	—	—	—
6	4	USB0_DM	—	—	—	—	—	—	—
7	5	USB_VDD	—	—	—	—	—	—	—
8	6	PTE16	ND	Hi-Z	—	FS	N	N	Y
9	—	PTE20	ND	Hi-Z	—	SS	N	N	Y
10	—	PTE21	ND	Hi-Z	—	SS	N	N	Y
11	—	PTE22	ND	Hi-Z	—	SS	N	N	Y
12	—	PTE23	ND	Hi-Z	—	SS	N	N	Y
13	7	VDDA	—	—	—	—	—	—	—
14	7	VREFH	—	—	—	—	—	—	—

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 10. Pin properties*...continued*

64 LQFP	32 QFN	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
14	—	VREFO	—	—	—	—	—	—	—
15	8	VREFL	—	—	—	—	—	—	—
16	8	VSSA	—	—	—	—	—	—	—
17	—	PTE29	ND	Hi-Z	—	SS	N	N	Y
18	9	PTE30	ND	Hi-Z	—	SS	N	N	Y
19	—	PTE31	ND	Hi-Z	—	SS	N	N	Y
20	—	PTE24	ND	Hi-Z	—	SS	N	N	Y
21	—	PTE25	ND	Hi-Z	—	SS	N	N	Y
22	10	PTA0	ND	L	PD	SS	N	N	Y
23	11	PTA1	ND	Hi-Z	—	SS	N	N	Y
24	12	PTA2	ND	Hi-Z	—	SS	N	N	Y
25	13	PTA3	ND	H	PU	FS	N	N	Y
26	14	PTA4	ND	H	PU	SS	Y	N	Y
27	—	PTA5	ND	Hi-Z	—	SS	N	N	Y
28	—	PTA12	ND	Hi-Z	—	SS	N	N	Y
29	—	PTA13	ND	Hi-Z	—	SS	N	N	Y
30	15	VDD	ND	—	—	—	—	—	—
31	16	VSS	ND	—	—	—	—	—	—
32	17	PTA18	ND	Hi-Z	—	SS	N	N	Y
33	18	PTA19	ND	Hi-Z	—	SS	N	N	Y

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 10. Pin properties...*continued*

64 LQFP	32 QFN	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
34	19	PTA20	ND	H	PU	SS	N	Y	Y
35	20	PTB0/LLWU_P5	HD	Hi-Z	—	FS	N	N	Y
36	21	PTB1	HD	Hi-Z	—	FS	N	N	Y
37	—	PTB2	ND	Hi-Z	—	SS	N	N	Y
38	—	PTB3	ND	Hi-Z	—	SS	N	N	Y
39	—	PTB16	ND	Hi-Z	—	FS	N	N	Y
40	—	PTB17	ND	Hi-Z	—	FS	N	N	Y
41	—	PTB18	ND	Hi-Z	—	SS	N	N	Y
42	—	PTB19	ND	Hi-Z	—	SS	N	N	Y
43	—	PTC0	ND	Hi-Z	—	SS	N	N	Y
44	22	PTC1/LLWU_P6/ RTC_CLKIN	ND	Hi-Z	—	SS	N	N	Y
45	23	PTC2	ND	Hi-Z	—	SS	N	N	Y
46	24	PTC3/LLWU_P7	HD	Hi-Z	—	FS	N	N	Y
47	—	VSS	—	—	—	—	—	—	—
48	—	VDD	—	—	—	—	—	—	—
49	25	PTC4/LLWU_P8	HD	Hi-Z	—	FS	N	N	Y
50	26	PTC5/LLWU_P9	ND	Hi-Z	—	FS	N	N	Y
51	27	PTC6/LLWU_P10	ND	Hi-Z	—	FS	N	N	Y
52	28	PTC7	ND	Hi-Z	—	FS	N	N	Y

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 10. Pin properties...*continued*

64 LQFP	32 QFN	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
53	—	PTC8	ND	Hi-Z	—	SS	N	N	Y
54	—	PTC9	ND	Hi-Z	—	SS	N	N	Y
55	—	PTC10	ND	Hi-Z	—	SS	N	N	Y
56	—	PTC11	ND	Hi-Z	—	SS	N	N	Y
57	—	PTD0	ND	Hi-Z	—	FS	N	N	Y
58	—	PTD1	ND	Hi-Z	—	FS	N	N	Y
59	—	PTD2	ND	Hi-Z	—	FS	N	N	Y
60	—	PTD3	ND	Hi-Z	—	FS	N	N	Y
61	29	PTD4/LLWU_P14	ND	Hi-Z	—	FS	N	N	Y
62	30	PTD5	ND	Hi-Z	—	FS	N	N	Y
63	31	PTD6/LLWU_P15	HD	Hi-Z	—	FS	N	N	Y
64	32	PTD7	HD	Hi-Z	—	FS	N	N	Y

Table 11. Pin properties descriptions

Properties	Abbreviation	Descriptions
Driver strength	ND	Normal drive
	HD	High drive
Default status after POR	Hi-Z	High impedance
	H	High level
	L	Low level

Table continues on the next page...

© 2026 NXP B.V. All rights reserved.

Table 11. Pin properties descriptions*...continued*

Properties	Abbreviation	Descriptions
Pullup/ pulldown setting after POR	PD	Pulldown
	PU	Pullup
Slew rate after POR	FS	Fast slew rate
	SS	Slow slew rate
Passive Pin Filter after POR	N	Disabled
	Y	Enabled
Open drain	N	Disabled [1]
	Y	Enabled [2]
Pin interrupt	Y	Yes

[1] When I2C module is enabled and a pin is functional for I2C, this pin is (pseudo-) open drain enabled. When UART or LPUART module is enabled and a pin is functional for UART or LPUART, this pin is (pseudo-) open drain configurable.
[2] PTA20 is a true open drain pin that must never be pulled above V_{DD}.

5.3 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

5.3.1 Core modules

Table 12. SWD signal descriptions

Chip signal name	Module signal name	Description	I/O
SWD_DIO	SWD_DIO	Serial Wire Debug Data Input/Output The SWD_DIO pin is used by an external debug tool for communication and device control. This pin is pulled up internally.	Input / Output
SWD_CLK	SWD_CLK	Serial Wire Clock This pin is the clock for debug logic when in the Serial Wire Debug mode. This pin is pulled down internally.	Input

5.3.2 System modules

Table 13. System signal descriptions

Chip signal name	Module signal name	Description	I/O
NMI	—	Non-maskable interrupt	I

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 13. System signal descriptions...*continued*

Chip signal name	Module signal name	Description	I/O
		Note: *Driving the NMI signal low forces a non-maskable interrupt, if the NMI function is selected on the corresponding pin.*	
RESET	—	Reset bidirectional signal	I/O
VDD	—	MCU power	I
VSS	—	MCU ground	I

Table 14. LLWU signal descriptions

Chip signal name	Module signal name	Description	I/O
LLWU_Pn	LLWU_Pn	Wakeup inputs (n = 5, 6, 7, 8, 9, 10, 14, 15)	I

5.3.3 Clock modules

Table 15. OSC signal descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL0	EXTAL	External clock/Oscillator input	I
XTAL0	XTAL	Oscillator output	O

5.3.4 Analog

This table presents the signal descriptions of the ADC0 module.

Table 16. ADC0 signal descriptions

Chip signal name	Module signal name	Description	I/O
ADC0_DPn	DADP3-DADP0	Differential Analog Channel Inputs	I
ADC0_DMn	DADM3-DADM0	Differential Analog Channel Inputs	I
ADC0_SEn	ADn	Single-Ended Analog Channel Inputs	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog Power Supply	I
VSSA	V_{SSA}	Analog Ground	I
EXTRG_IN	ADHWT	Hardware trigger	I

This table presents the signal descriptions of the CMP0 module.

Table 17. CMP0 signal descriptions

Chip signal name	Module signal name	Description	I/O
CMP0_IN[5:0]	IN[5:0]	Analog voltage inputs	I
CMP0_OUT	CMPO	Comparator output	O

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 18. VREF signal descriptions

Chip signal name	Module signal name	Description	I/O
VREF_OUT	VREF_OUT	Internally-generated voltage reference output	O

5.3.5 Timer Modules

Table 19. TPM0 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM0_CH[5:0]	TPM_CHn	TPM channel (n = 5 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

Table 20. TPM1 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM1_CH[1:0]	TPM_CHn	TPM channel (n = 1 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

Table 21. TPM2 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM2_CH[1:0]	TPM_CHn	TPM channel (n = 1 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

Table 22. LPTMR0 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[3:1]	LPTMR0_ALT*n*	Pulse Counter Input pin	I

Table 23. RTC signal descriptions

Chip signal name	Module signal name	Description	I/O
RTC_CLKOUT[1]	RTC_CLKOUT	1 Hz square-wave output or OSCERCLK	O

[1] RTC_CLKOUT can also be driven with OSCERCLK via SIM control bit SIM_SOPT[RCTCLKOUTSEL]

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

5.3.6 Communication interfaces

Table 24. USB FS OTG signal descriptions

Chip signal name	Module signal name	Description	I/O
USB0_DM	usb_dm	USB D- analog data signal on the USB bus.	I/O
USB0_DP	usb_dp	USB D+ analog data signal on the USB bus.	I/O
USB_CLKIN	--	Alternate USB clock input	I

Table 25. SPI0 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI0_MISO	MISO	Master Data In, Slave Data Out	I/O
SPI0_MOSI	MOSI	Master Data Out, Slave Data In	I/O
SPI0_SCLK	SPSCK	SPI Serial Clock	I/O
SPI0_PCS0	$\overline{SS}$	Slave Select	I/O

Table 26. SPI1 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI1_MISO	MISO	Master Data In, Slave Data Out	I/O
SPI1_MOSI	MOSI	Master Data Out, Slave Data In	I/O
SPI1_SCLK	SPSCK	SPI Serial Clock	I/O
SPI1_PCS0	$\overline{SS}$	Slave Select	I/O

Table 27. I^2C0 signal descriptions

Chip signal name	Module signal name	Description	I/O
I2C0_SCL	SCL	Bidirectional serial clock line of the I^2C system.	I/O
I2C0_SDA	SDA	Bidirectional serial data line of the I^2C system.	I/O

Table 28. I^2C1 signal descriptions

Chip signal name	Module signal name	Description	I/O
I2C1_SCL	SCL	Bidirectional serial clock line of the I^2C system.	I/O
I2C1_SDA	SDA	Bidirectional serial data line of the I^2C system.	I/O

Table 29. LPUART0 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART0_TX	TxD	Transmit data	I/O
LPUART0_RX	RxD	Receive data	I

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 30. LPUART1 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART1_TX	TxD	Transmit data	I/O
LPUART1_RX	RxD	Receive data	I

Table 31. UART2 signal descriptions

Chip signal name	Module signal name	Description	I/O
UART2_TX	TxD	Transmit data	O
UART2_RX	RxD	Receive data	I

Table 32. FlexIO signal descriptions

Chip signal name	Module signal name	Description	I/O
FXIO0_Dx	FXIO_Dn (n=0...7)	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O

5.3.7 Human-machine interfaces (HMI)

Table 33. GPIO signal descriptions

Chip signal name	Module signal name	Description	I/O
PTA[31:0]	PORTA31–PORTA0	General-purpose input/output	I/O
PTB[31:0]	PORTB31–PORTB0	General-purpose input/output	I/O
PTC[11:0]	PORTC11–PORTC0	General-purpose input/output	I/O
PTD[7:0]	PORTD7–PORTD0	General-purpose input/output	I/O
PTE[31:0]	PORTE31–PORTE0	General-purpose input/output	I/O

5.4 MCX C24X family pinouts

5.4.1 MCX C24X family pinouts

The figure below shows the 32 QFN pinouts:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

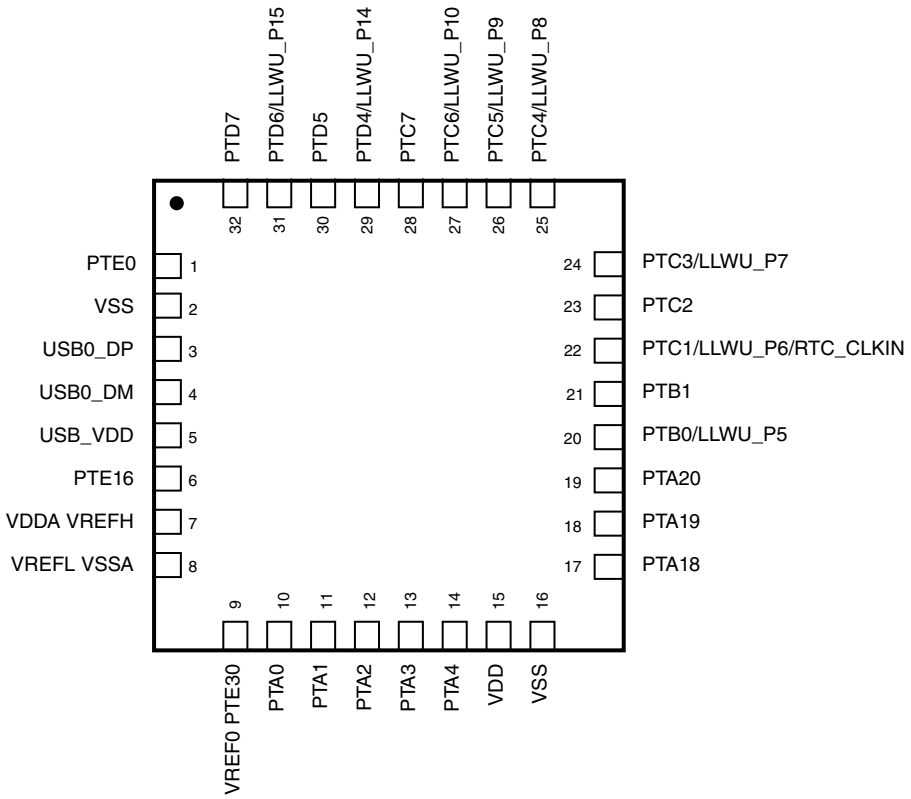


Figure 7. 32 QFN pinout diagram (transparent top view)

The figure below shows the 64 LQFP pinouts:

© 2026 NXP B.V. All rights reserved.

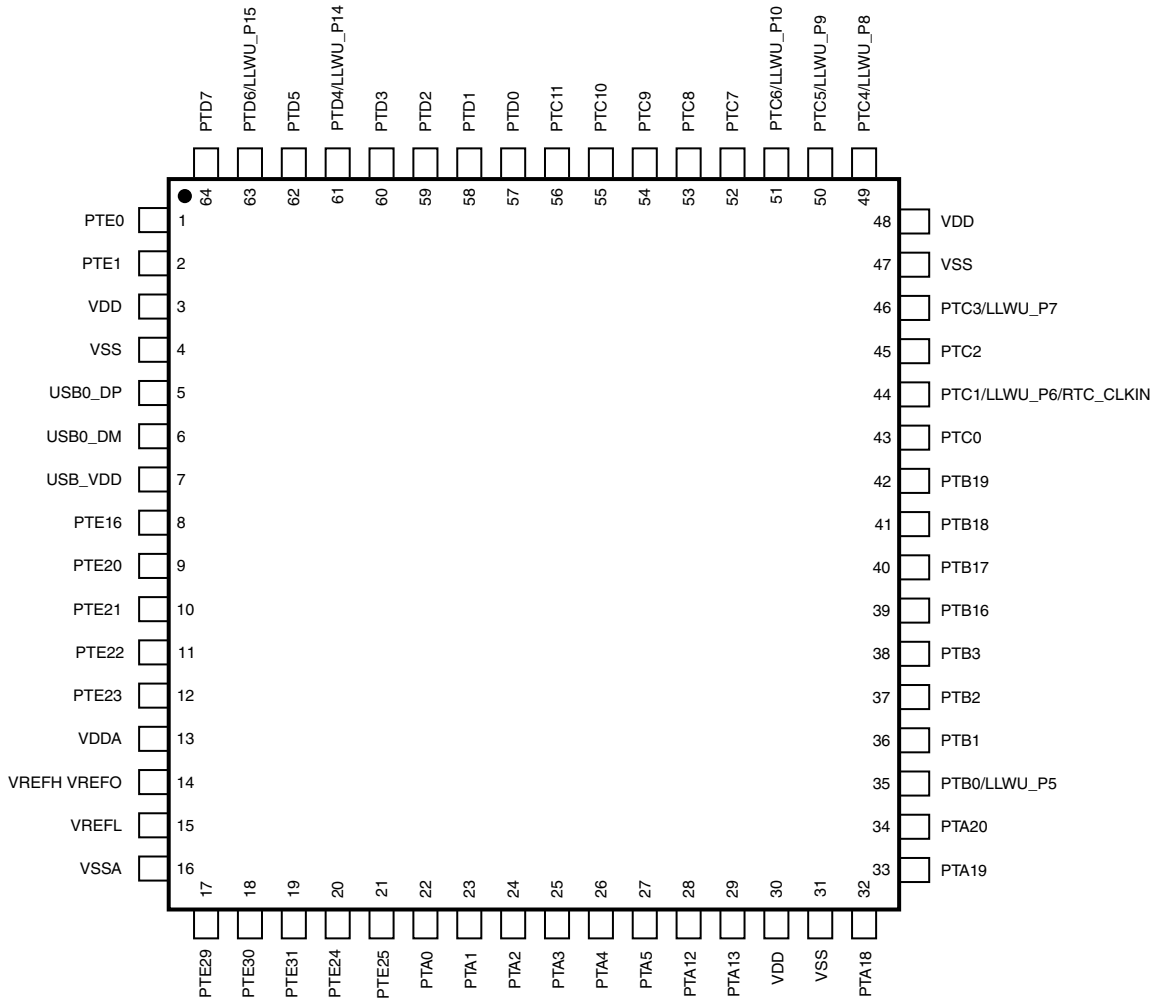


Figure 8. 64 LQFP pinout diagram (top view)

5.4.2 MCX C14X family pinouts

The figure below shows the 32 QFN pinouts.

© 2026 NXP B.V. All rights reserved.

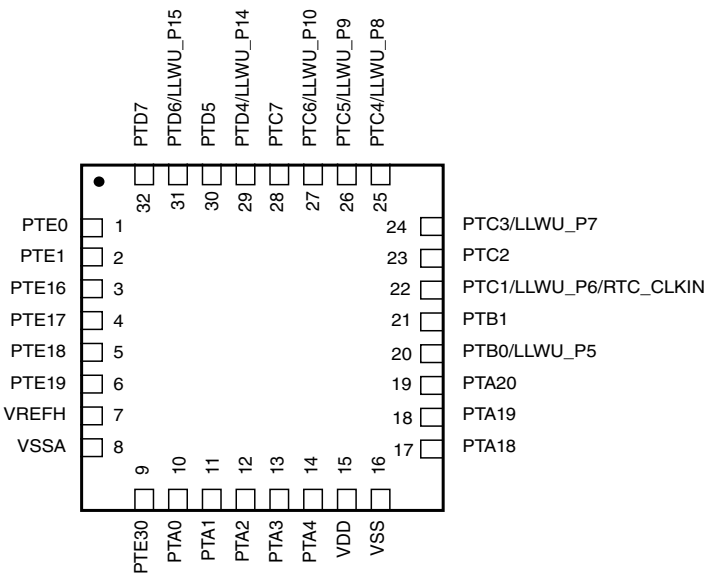


Figure 9. 32 QFN pinout diagram

The figure below shows the 64 LQFP pinouts.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

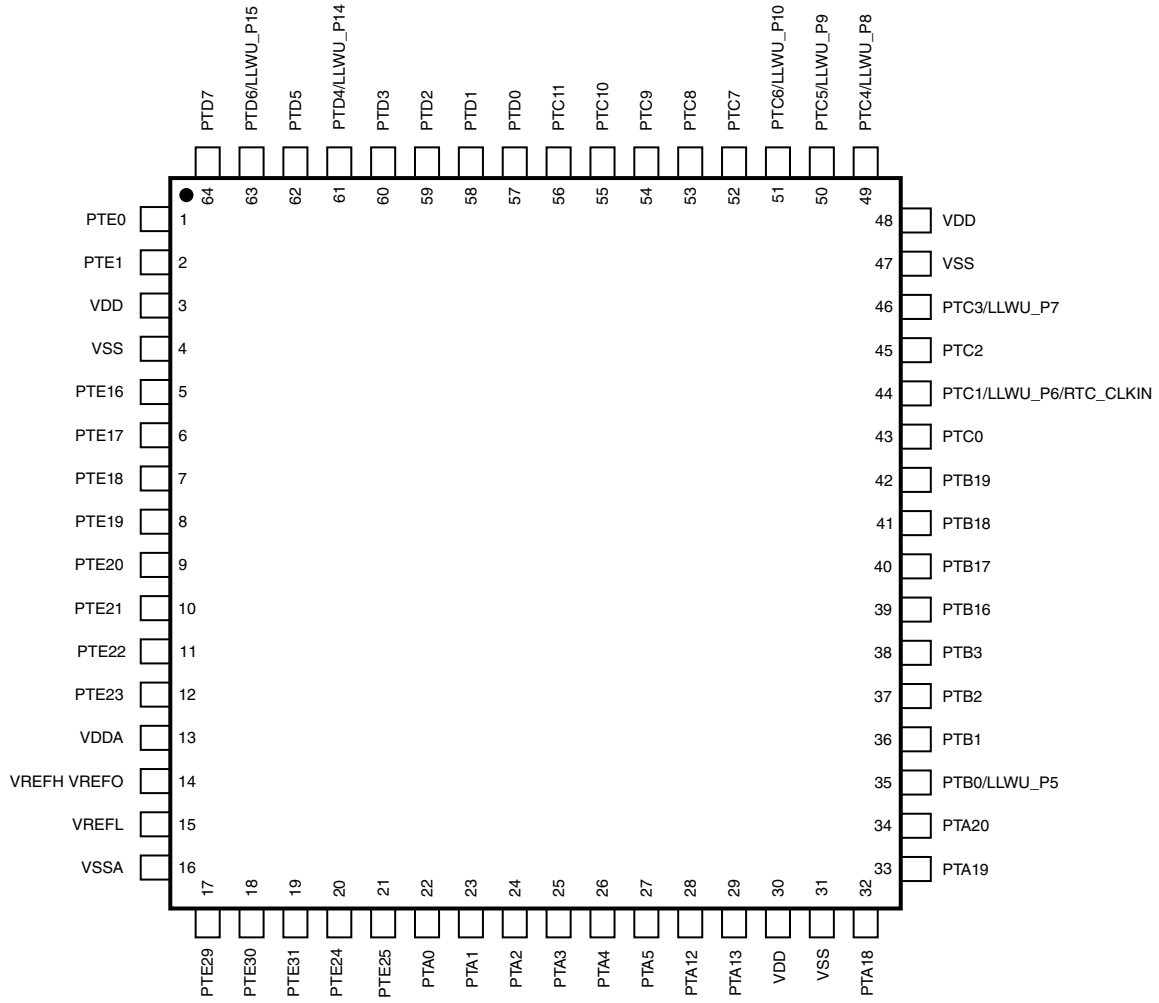


Figure 10. 64 LQFP pinout diagram

5.5 Package dimensions

The following figures show the dimensions of the package options for the devices supported by this document.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

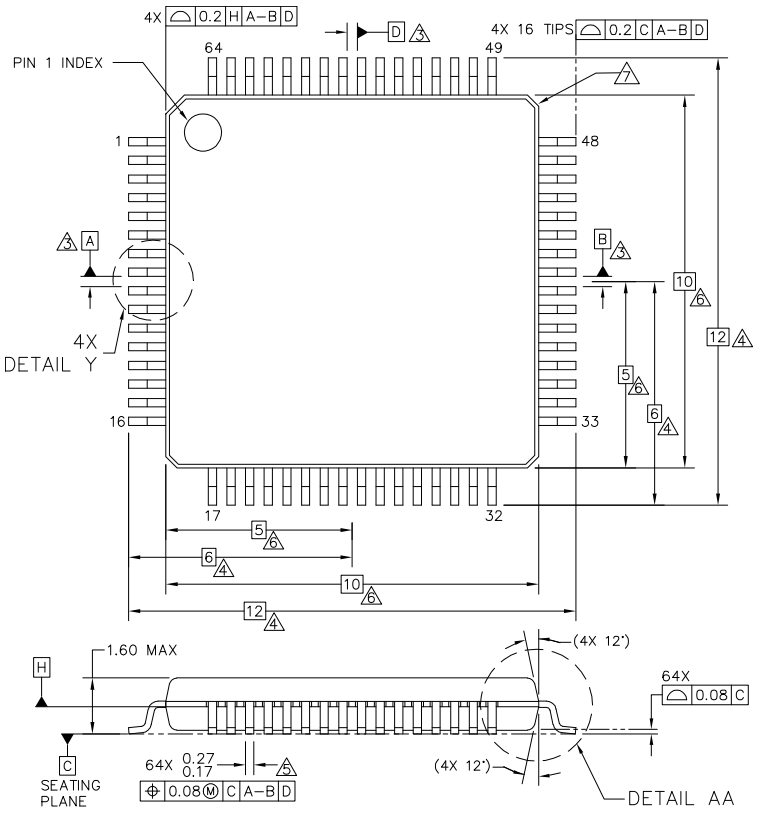
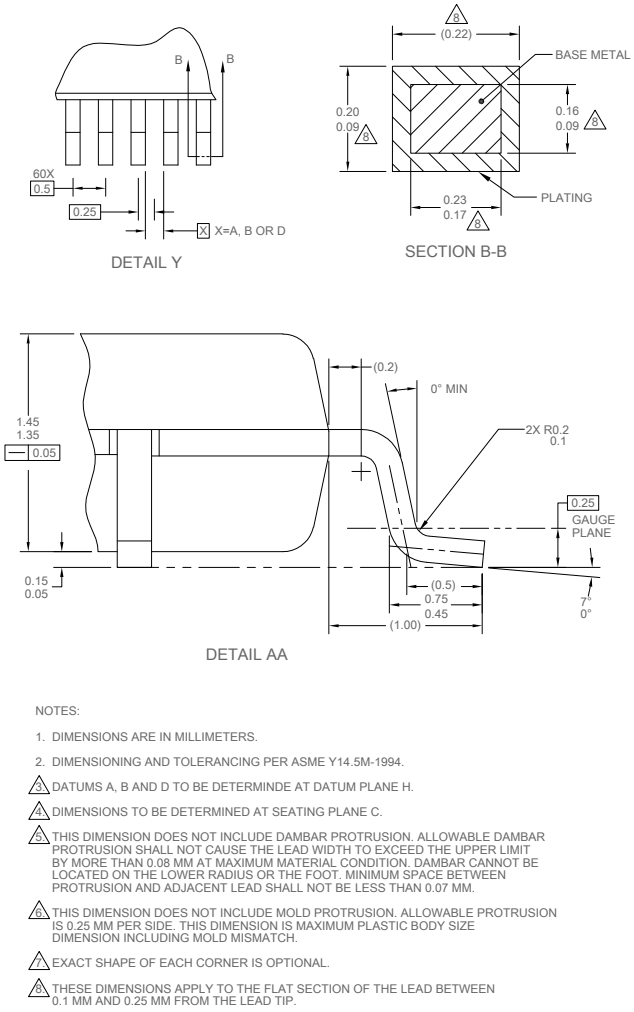


Figure 11. 64-pin LQFP package dimensions 1

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINDE AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

Figure 12. 64-pin LQFP package dimensions 2

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

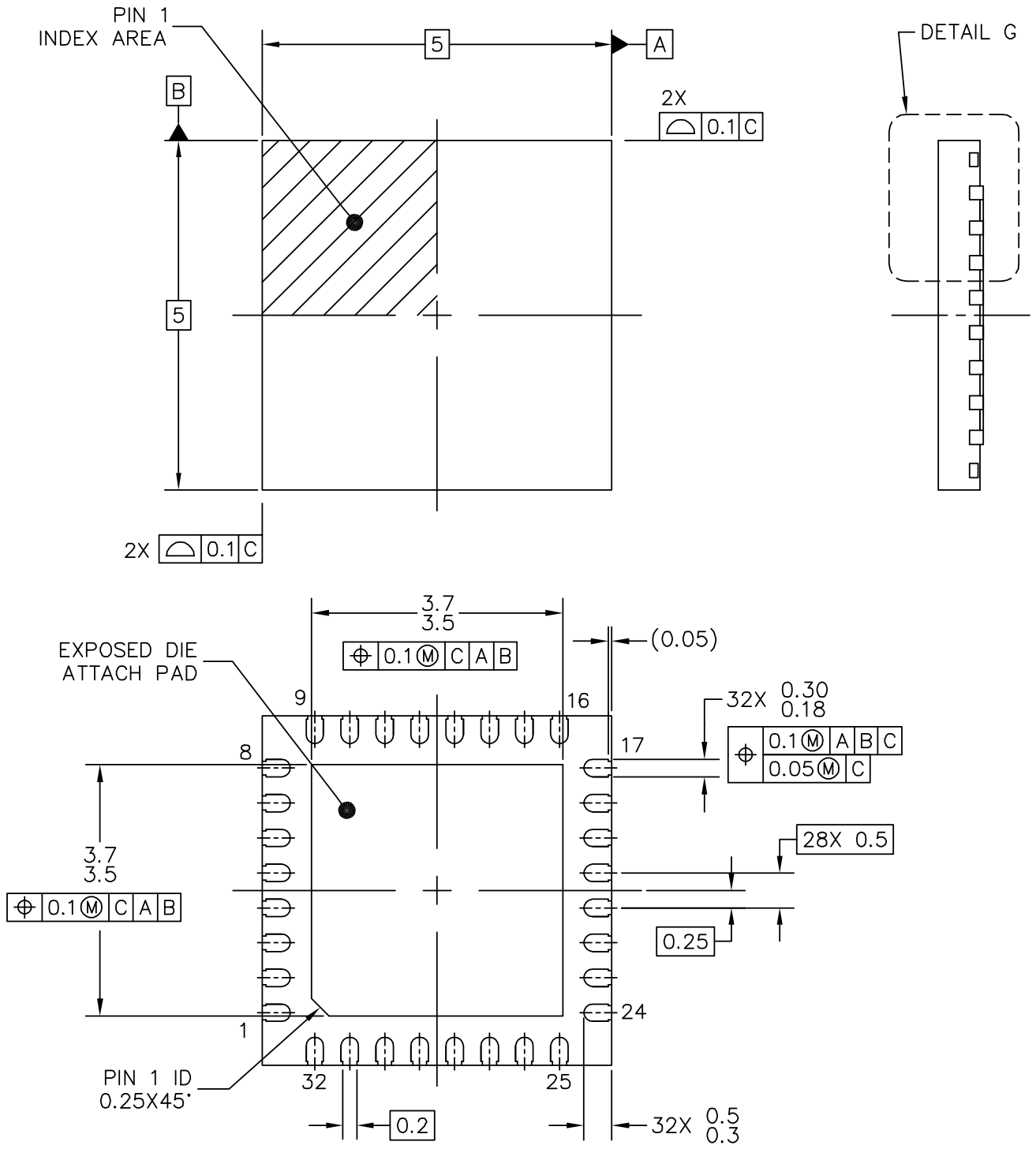
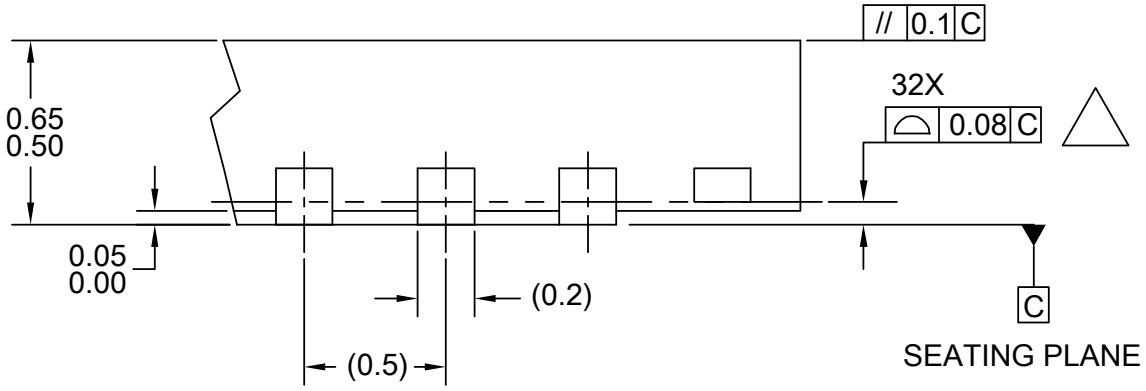


Figure 13. 32-pin QFN package dimension 1

© 2026 NXP B.V. All rights reserved.



DETAIL G
VIEW ROTATED 90°CW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

Figure 14. 32-pin QFN package dimension 2

6 Electrical characteristics

6.1 Ratings

6.1.1 Thermal handling ratings

Table 34. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	[1]
T_{SDR}	Solder temperature, lead-free	—	260	°C	[2]

[1] Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life.*
[2] Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices* .

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

6.1.2 Moisture handling ratings

Table 35. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	[1]

[1] Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.1.3 ESD handling ratings

Table 36. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	[1]
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	[2]
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	[3]

[1] Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
[2] Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
[3] Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

6.1.4 Voltage and current absolute operating ratings

Table 37. Voltage and current absolute operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} - 0.3	V_{DD} + 0.3	V
V_{USB_DP}	USB_DP input voltage	–0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	–0.3	3.63	V

6.2 General

6.2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

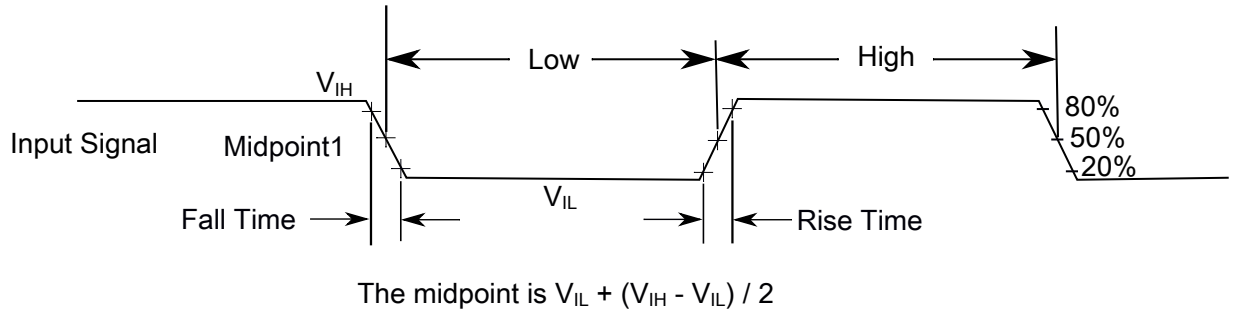


Figure 15. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L = 30 pF loads
- Slew rate disabled
- Normal drive strength

6.2.2 Nonswitching electrical specifications

6.2.2.1 Voltage and current operating requirements

Table 38. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	—
USB_V_{DD}	Supply voltage	3.0	3.6	V	—
V_{DDA}	Analog supply voltage	1.71	3.6	V	—
V_{DD} – V_{DDA}	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	—
V_{SS} – V_{SSA}	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	—
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	0.7 × V_{DD} 0.75 × V_{DD}	— —	V V	—
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	— —	0.35 × V_{DD} 0.3 × V_{DD}	V V	—
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	—
I_{ICIO}	IO pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-3	—	mA	[1]

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 38. Voltage and current operating requirements...*continued*

Symbol	Description	Min.	Max.	Unit	Notes
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	—
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	[2]
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	—

[1] All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|.

[2] Open drain outputs must be pulled to V_{DD}.

6.2.2.2 LVD and POR operating requirements

Table 39. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
V_{LVW1H} V_{LVW2H} V_{LVW3H} V_{LVW4H}	Low-voltage warning thresholds — high range • Level 1 falling (LVWV = 00) • Level 2 falling (LVWV = 01) • Level 3 falling (LVWV = 10) • Level 4 falling (LVWV = 11)	2.62 2.72 2.82 2.92	2.70 2.80 2.90 3.00	2.78 2.88 2.98 3.08	V V V V	[1]
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV = 00)	1.54	1.60	1.66	V	—
V_{LVW1L} V_{LVW2L} V_{LVW3L} V_{LVW4L}	Low-voltage warning thresholds — low range • Level 1 falling (LVWV = 00) • Level 2 falling (LVWV = 01) • Level 3 falling (LVWV = 10) • Level 4 falling (LVWV = 11)	1.74 1.84 1.94 2.04	1.80 1.90 2.00 2.10	1.86 1.96 2.06 2.16	V V V V	[1]
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 39. V_{DD} supply LVD and POR operating requirements...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	—

[1] Rising thresholds are falling threshold + hysteresis voltage

6.2.2.3 Voltage and current operating behaviors

Table 40. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — normal drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -2.5 mA	V_{DD} - 0.5 V_{DD} -0.5	— —	V V	[1]
V_{OH}	Output high voltage — high drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} -10 mA	V_{DD} - 0.5 V_{DD} - 0.5	— —	V V	[1]
I_{OHT}	Output high current total for all ports	—	100	mA	—
V_{OL}	Output low voltage — normal drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	— —	0.5 0.5	V V	[1]
V_{OL}	Output low voltage — high drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	— —	0.5 0.5	V V	[1]
I_{OLT}	Output low current total for all ports	—	100	mA	—
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	[2]
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	[2]
I_{IN}	Input leakage current (total all pins) for full temperature range	—	64	µA	[2]
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	—
R_{PU}	Internal pullup resistors	20	50	kΩ	[3]
R_{PD}	Internal pulldown resistors	20	50	kΩ	[4]

[1] PTB0, PTB1, PTC3, PTC4, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
[2] Measured at V_{DD}= 3.6 V
[3] Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

[4] Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{DD}

6.2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

Table 41. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	—
	• VLLS0 → RUN	—	152	166	µs	—
	• VLLS1 → RUN	—	152	166	µs	—
	• VLLS3 → RUN	—	93	104	µs	—
	• LLS → RUN	—	7.5	8	µs	—
	• VLPS → RUN	—	7.5	8	µs	—
	• STOP → RUN	—	7.5	8	µs	—

6.2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Note: *The while (1) test is executed with flash cache enabled.*

Table 42. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	[1]
I_{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, VDD = 3.0 V	—	—	—	—	[2]
	• at 25 °C	—	4.79	4.98	mA	—
	• at 105 °C	—	4.94	5.14		
I_{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, VDD = 3.0 V	—	—	—	—	—

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 42. Power consumption operating behaviors...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 25 °C	—	2.73	2.87	mA	—
	• at 105 °C	—	2.9	3.05		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, VDD = 3.0 V	—	—	—	—	[2]
	• at 25 °C	—	5.45	5.67	mA	—
	• at 105 °C	—	5.6	5.82		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, VDD = 3.0 V	—	—	—	—	[2]
	• at 25 °C	—	3.41	3.55	mA	—
	• at 105 °C	—	3.56	3.70		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, VDD = 3.0 V	—	—	—	—	[2]
	• at 25 °C	—	2.37	2.49	mA	—
	• at 105 °C	—	2.52	2.65		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, VDD = 3.0 V	—	—	—	—	[2]
	• at 25 °C	—	7.05	7.33	mA	—
	• at 105 °C	—	7.2	7.49		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	3.39	3.53	mA	
	• at 105 °C	—	3.57	3.71		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	2.36	2.48	mA	
	• at 105 °C	—	2.53	2.66		
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	1.84	1.93	mA	
	• at 105 °C	—	2	2.1		

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 42. Power consumption operating behaviors...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	4.98	5.18	mA	
	• at 105 °C	—	5.16	5.37		
I_{DD_VLPRCO}	Very-low-power run core mark in flash in compute operation mode— 8 MHz LIRC mode, 4 MHz core/1 MHz flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	710	752.6	µA	
I_{DD_VLPRCO}	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	251	376.5	µA	
I_{DD_VLPRCO}	Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	115	143.75	µA	
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	91	136.5	µA	
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	34	51	µA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 4 MHz core / 1 MHz flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	212	318	µA	
I_{DD_VLPR}	Very-low-power run mode current—8 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 4 MHz core / 1 MHz flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	302	392.6	µA	
I_{DD_WAIT}	Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	1.81	2.12	mA	

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 42. Power consumption operating behaviors...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_WAIT}	Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	1.27	1.46	mA	
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	156	193.2	µA	
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, VDD = 3.0 V	—	—	—	µA	—
	• at 25 °C	—	63	100.8		
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, VDD = 3.0 V	—	—	—	µA	—
	• at 25 °C	—	32	48		
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	1.68	2.05	mA	
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, VDD = 3.0 V	—	—	—	—	—
	• at 25 °C	—	1.05	1.26	mA	
I_{DD_STOP}	Stop mode current at 3.0 V	—	—	—	—	—
	• at 25 °C and below	—	158.1	175.81	µA	
	• at 50 °C	—	171	180.24	µA	
	• at 85 °C	—	203.8	228.64	µA	
	• at 105 °C	—	251.7	300.06	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V	—	—	—	—	—
	• at 25 °C and below	—	2.34	3.8	µA	
	• at 50 °C	—	5.04	8.03	µA	
	• at 85 °C	—	20.48	31.97	µA	
	• at 105 °C	—	42.34	65.78	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 1.8 V	—	—	—	—	—
	• at 25 °C and below	—	2.33	3.8	µA	
	• at 50 °C	—	4.95	7.94	µA	

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 42. Power consumption operating behaviors...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 85 °C	—	20.18	31.57	µA	
	• at 105 °C	—	41.93	65.17	µA	
I_{DD_LLS}	Low-leakage stop mode current, all peripheral disable, at 3.0 V	—	—	—	—	—
	• at 25 °C and below	—	1.71	1.96	µA	
	• at 50 °C	—	2.59	3.3	µA	
	• at 70 °C	—	4.46	7.06	µA	
	• at 85 °C	—	7.55	10.15	µA	
	• at 105 °C	—	17.03	22.67	µA	
I_{DD_LLS}	Low-leakage stop mode current with RTC current, at 3.0 V	—	—	—	—	[3]
	• at 25 °C and below	—	2.27	2.52	µA	
	• at 50 °C	—	3.1	3.81	µA	
	• at 70 °C	—	4.99	7.59	µA	
	• at 85 °C	—	8.1	10.7	µA	
	• at 105 °C	—	17.32	22.96	µA	
I_{DD_LLS}	Low-leakage stop mode current with RTC current, at 1.8 V	—	—	—	—	[3]
	• at 25 °C and below	—	2.1	2.35	µA	
	• at 50 °C	—	2.89	3.6	µA	
	• at 70 °C	—	4.65	7.25	µA	
	• at 85 °C	—	7.61	10.21	µA	
	• at 105 °C	—	16.38	22.02	µA	
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V	—	—	—	—	—
	• at 25 °C and below	—	1.43	1.58	µA	
	• at 50 °C	—	2.06	2.52	µA	
	• at 70 °C	—	3.51	5.2	µA	
	• at 85 °C	—	5.91	7.6	µA	
	• at 105 °C	—	13.36	17.08	µA	
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V	—	—	—	—	[3]
	• at 25 °C and below	—	1.83	1.98	µA	
	• at 50 °C	—	2.47	2.93	µA	
	• at 70 °C	—	3.96	5.65	µA	

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 42. Power consumption operating behaviors...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 85 °C	—	6.44	8.13	µA	
	• at 105 °C	—	13.84	17.56	µA	
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V	—	—	—	—	[3]
	• at 25 °C and below	—	1.68	1.83	µA	
	• at 50 °C	—	2.27	2.73	µA	
	• at 70 °C	—	3.66	5.35	µA	
	• at 85 °C	—	5.97	7.66	µA	
	• at 105 °C	—	12.92	16.64	µA	
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V	—	—	—	—	—
	• at 25 °C and below	—	0.84	1.06	µA	
	• at 50°C	—	1.19	1.33	µA	
	• at 70°C	—	2.03	2.62	µA	
	• at 85°C	—	3.54	4.13	µA	
	• at 105 °C	—	8.53	9.98	µA	
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V	—	—	—	—	[3]
	• at 25 °C and below	—	1.26	1.48	µA	
	• at 50°C	—	1.61	1.75	µA	
	• at 70°C	—	2.5	3.09	µA	
	• at 85°C	—	4.07	4.66	µA	
	• at 105 °C	—	9	10.45	µA	
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V	—	—	—	—	[3]
	• at 25 °C and below	—	1.08	1.3	µA	
	• at 50°C	—	1.42	1.56	µA	
	• at 70°C	—	2.21	2.8	µA	
	• at 85°C	—	3.59	4.18	µA	
	• at 105 °C	—	8.02	9.47	µA	
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V	—	—	—	—	—
	• at 25 °C and below	—	262	360	nA	

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 42. Power consumption operating behaviors...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 50 °C	—	593	725	nA	
	• at 70 °C	—	1430	2014	nA	
	• at 85 °C	—	2930	3514	nA	
	• at 105 °C	—	7930	9895	nA	
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V	—	—	—	—	[4]
	• at 25 °C and below	—	87	185	nA	
	• at 50 °C	—	417	549	nA	
	• at 70 °C	—	1230	1230	nA	
	• at 85 °C	—	2720	3304	nA	
	• at 105 °C	—	7780	9745	nA	

[1] The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module specification for its supply current.
[2] MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR with optimization level high, optimized for balanced.
[3] RTC uses external 32 kHz crystal as clock source, and the current includes ERCLK32K power consumption.
[4] No brownout

Table 43. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IRC8MHz}$	8 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 8 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	77	77	77	77	77	77	µA
$I_{IRC2MHz}$	2 MHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 2 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	25	25	25	25	25	25	µA
$I_{EREFSTEN4MHz}$	[C:] External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	224	230	238	245	253	µA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	—	—	—	—	—	—	—
	• VLLS1	440	490	540	560	570	580	nA
	• VLLS3	440	490	540	560	570	580	nA
	• LLS	490	490	540	560	570	680	nA
	• VLPS	510	560	560	560	610	680	nA

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 43. Low power mode peripheral adders — typical value*...continued*

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	• STOP	510	560	560	560	610	680	nA
I_{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.—	30	30	30	85	100	200	nA
$I_{USBKPALV}$	IDD adder measured by placing the device in VLPS mode with USB connection kept alive.	—	1.353	—	—	—	—	mA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	16	16	16	16	16	16	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	430	500	500	530	530	760	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.	—	—	—	—	—	—	µA
	• IRC8M (8 MHz internal reference clock)	96	96	96	96	96	96	µA
	• IRC2M (2 MHz internal reference clock)	31	31	31	31	31	31	µA
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	—	—	—	—	—	—	µA
	• IRC8M (8 MHz internal reference clock)	130	130	130	130	130	130	µA
	• IRC2M (2 MHz internal reference clock)	40	40	40	40	40	40	µA
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	320	320	320	320	320	320	µA

6.2.2.5.1 Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- No GPIOs toggled

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

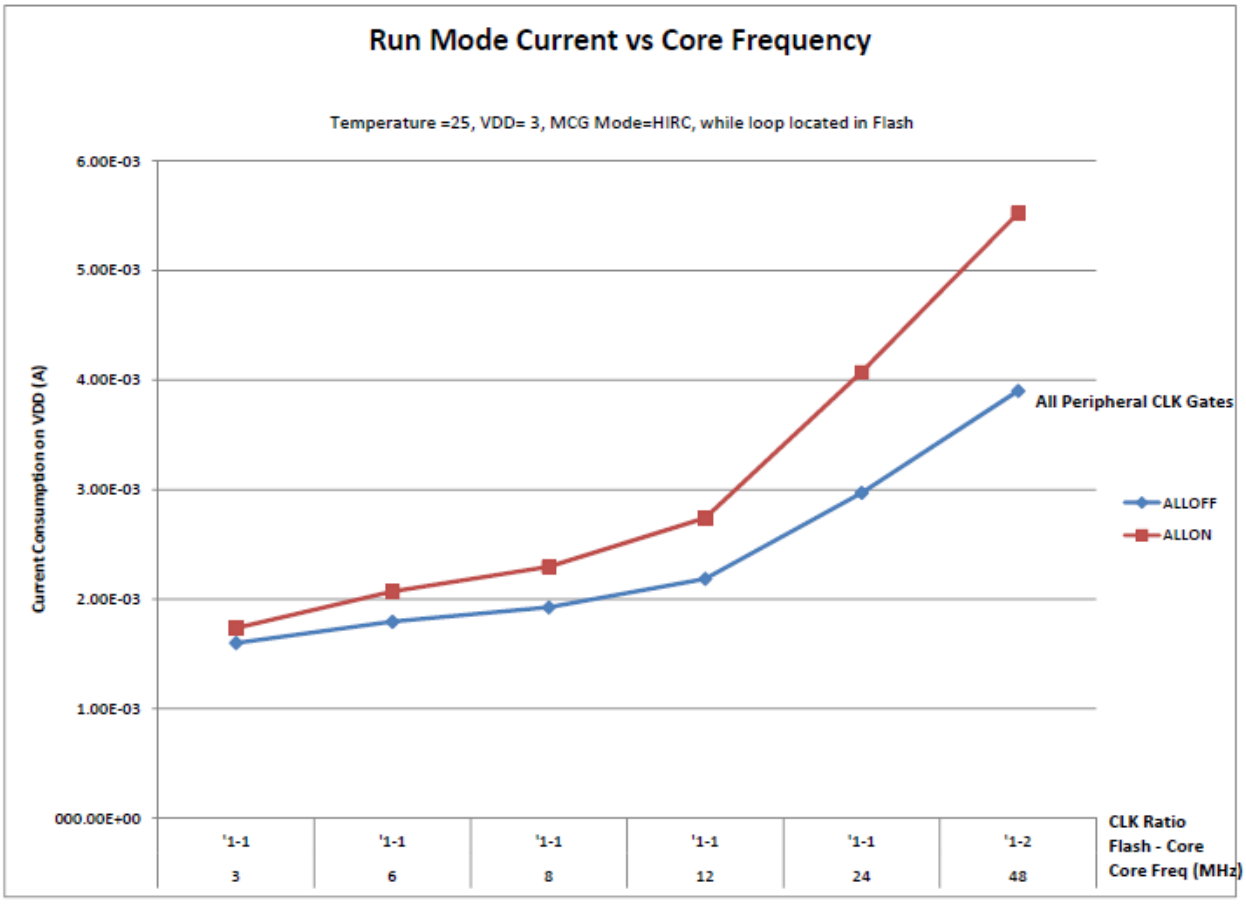


Figure 16. Run mode supply current vs. core frequency 1

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

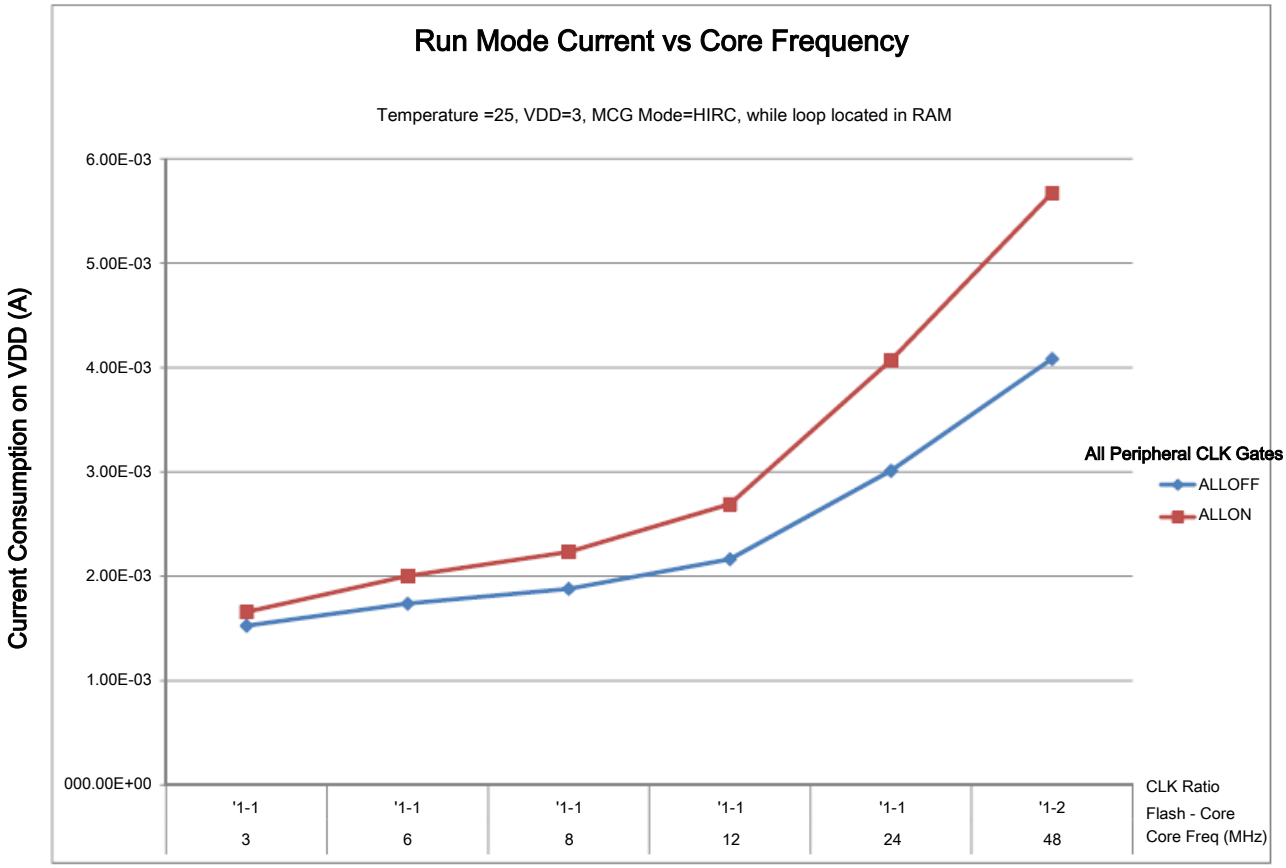


Figure 17. Run mode supply current vs. core frequency 2

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

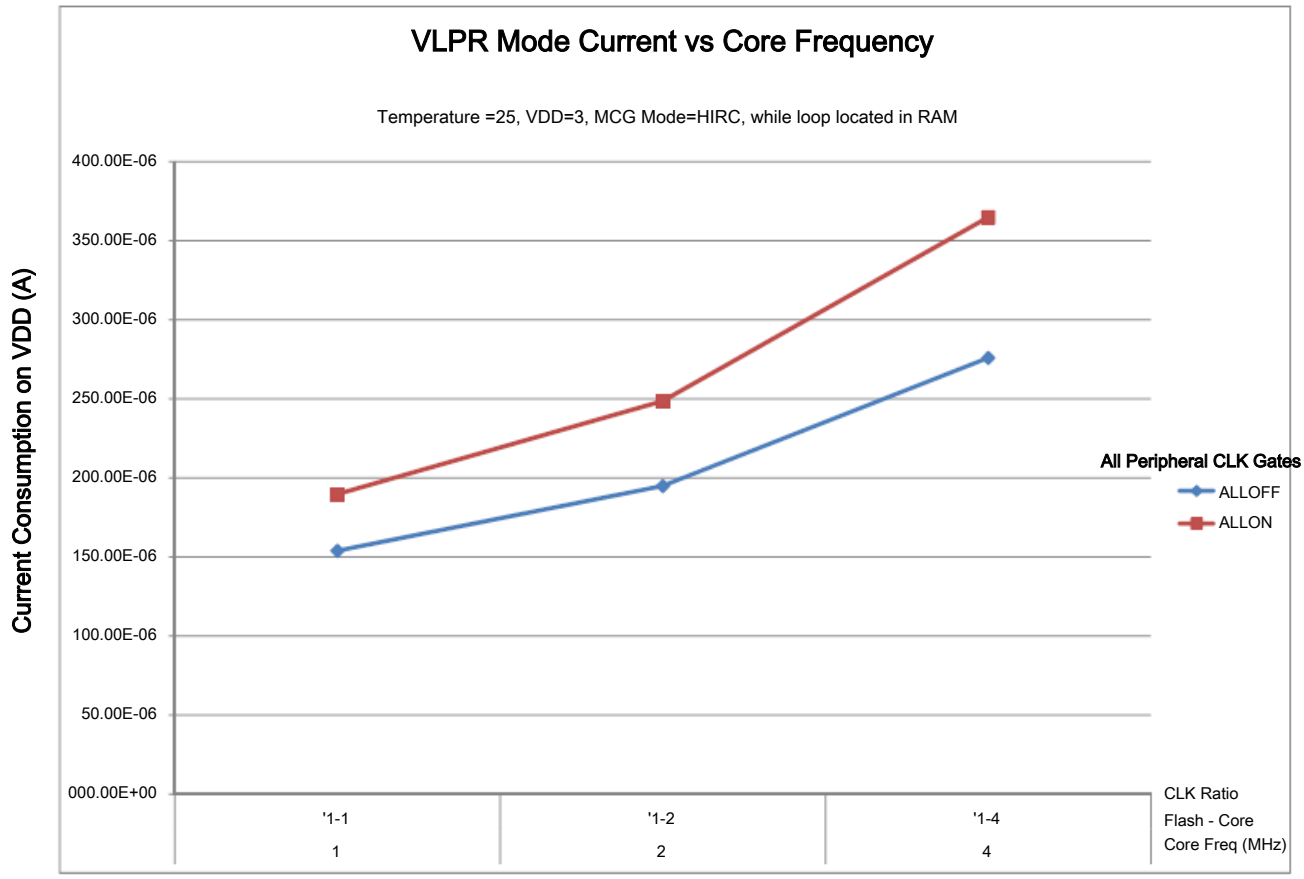


Figure 18. VLPR mode current vs. core frequency

6.2.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following NXP applications notes, available on nxp.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

6.2.2.7 Capacitance attributes

Table 44. Capacitance attributes

Symbol	Description	Min.	Max.
C_{IN}	Input capacitance	—	7 pF

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

6.2.3 Switching specifications

6.2.3.1 Device clock specifications

Table 45. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock [1]	—	48	MHz
f_{BUS}	Bus clock[1]	—	24	MHz
f_{FLASH}	Flash clock[1]	—	24	MHz
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes [2]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock [3]	—	24	MHz
f_{ERCLK}	External reference clock	—	16	MHz
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE] = 1x)	—	16	MHz
f_{TPM}	TPM asynchronous clock	—	8	MHz
f_{UART0}	UART0 asynchronous clock	—	8	MHz

[1] The maximum value of system clock, core clock, bus clock, and flash clock under normal run mode can be 3% higher than the specified maximum frequency when IRC 48MHz is used as the clock source.
[2] The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
[3] The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

6.2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 46. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	[1]

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 46. General switching specifications...*continued*

Description	Min.	Max.	Unit	Notes
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	[2]
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	[2]
Port rise and fall time	—	36	ns	[3]

[1] The synchronous and asynchronous timing must be met.
[2] This is the shortest pulse that is guaranteed to be recognized.
[3] 75 pF load

6.2.4 Thermal specifications

6.2.4.1 Thermal operating requirements

Table 47. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	—
T_A	Ambient temperature	–40	125	°C	[1], [2]

[1] Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.
[2] The device operating specification is not guaranteed beyond 125 °C TJ.

6.2.4.2 Thermal attributes

Table 48. Thermal attributes

Board type	Symbol	Description	32 QFN	64 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	101	71	°C/W	[1], [2], [3]
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	33	53	°C/W	[1], [2], [3], [4]
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	84	60	°C/W	[1], [4], [5]
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	28	47	°C/W	[1], [4], [5]
—	$R_{\theta JB}$	Thermal resistance, junction to board	13	35	°C/W	[6]
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.7	21	°C/W	[7]
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	5	°C/W	[8]

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 48. Thermal attributes*...continued*

Board type	Symbol	Description	32 QFN	64 LQFP	Unit	Notes
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom (natural convection)	—	—	°C/W	[9]

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[2] Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
[3] Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
[4] Per JEDEC JESD51-6 with the board horizontal.
[5] Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
[6] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[7] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
[8] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
[9] Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

6.3 Peripheral operating requirements and behaviors

6.3.1 Core modules

6.3.1.1 SWD electrical specifications

Table 49. SWD full voltage range electrical specifications

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

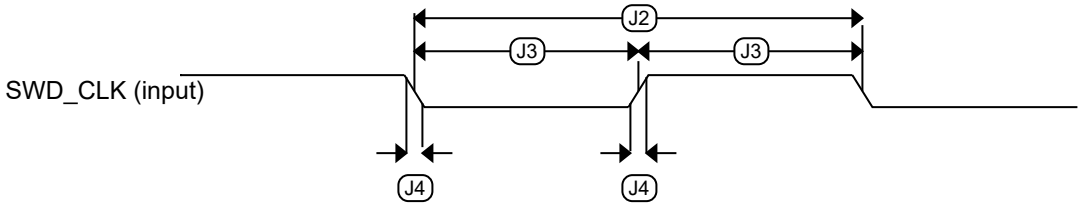


Figure 19. Serial wire clock input timing

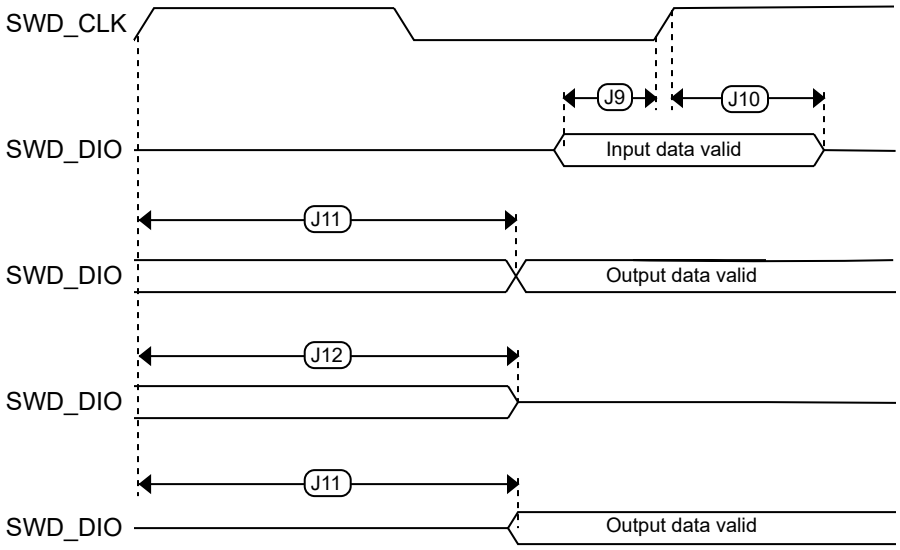


Figure 20. Serial wire data timing

6.3.2 System modules

There are no specifications necessary for the device's system modules.

6.3.3 Clock modules

6.3.3.1 MCG-Lite specifications

Table 50. IRC48M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD48M}	Supply current	—	400	500	µA	—
f_{irc48m}	Internal reference frequency	—	48	—	MHz	—
$\Delta f_{irc48m_ol_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD = 1.71 V-1.89 V) over temperature	—	± 0.5	± 1.5	$\%f_{irc48m}$	[1]

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 50. IRC48M specification...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$\Delta f_{irc48m_ol_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD = 1.89 V-3.6 V) over temperature	—	± 0.5	± 1.0	$\%f_{irc48m}$	[1]
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	[2]
T_{cyc_irc48m}	Period jitter (RMS)	—	35	150	ps	—
$T_{irc48mst}$	Startup time	—	2	3	µs	[3]

[1] The maximum value represents characterized results equivalent to mean plus or minus three times the standard deviation (mean +/-3sigma).
[2] Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN] = 1,USB_CLK_RECOVER_IRC_EN[IRC_EN] = 1).
[3] IRC48M startup time is defined as the time between clock enablement and clock availability for system use. See reference manual for details.

Table 51. IRC8M/2M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_2M}	Supply current in 2 MHz mode	—	14	17	µA	—
I_{DD_8M}	Supply current in 8 MHz mode	—	30	35	µA	—
f_{IRC_2M}	Output frequency	—	2	—	MHz	—
f_{IRC_8M}	Output frequency	—	8	—	MHz	—
$f_{IRC_T_2M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	—
$f_{IRC_T_8M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	—
T_{su_2M}	Startup time	—	—	12.5	µs	—
T_{su_8M}	Startup time	—	—	12.5	µs	—

6.3.3.2 Oscillator electrical specifications

6.3.3.2.1 Oscillator DC electrical specifications

Table 52. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO = 0) • 32 kHz	—	500	—	nA	[1]
	• 4 MHz	—	200	—	µA	

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 52. Oscillator DC electrical specifications*...continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• 8 MHz (RANGE = 01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO = 1) • 32 kHz	—	25	—	nA	[1]
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE = 01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		[2] [3]
C_y	XTAL load capacitance	—	—	—		[2], [3]
R_F	Feedback resistor — low-frequency, low-power mode (HGO = 0)	—	—	—	MΩ	[2], [4]
	Feedback resistor — low-frequency, high-gain mode (HGO = 1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO = 0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO = 1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO = 0)	—	—	—	kΩ	—
	Series resistor — low-frequency, high-gain mode (HGO = 1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO = 0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO = 1)	—	0	—	kΩ	

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 52. Oscillator DC electrical specifications*...continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO = 0)	—	0.6	—	V	[5]
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO = 1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO = 0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO = 1)	—	V_{DD}	—	V	

[1] V_{DD} =3.3 V, Temperature =25 °C
[2] See crystal or resonator manufacturer's recommendation.
[3] C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
[4] When low power mode is selected, R_F is integrated and must not be attached externally.
[5] The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2.2 Oscillator frequency specifications

Table 53. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE] = 00)	32	—	40	kHz	—
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE] = 01)	3	—	8	MHz	—
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE] = 1x)	8	—	32	MHz	—
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	[1] [2]
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	—
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO = 0)	—	750	—	ms	[3] [4]
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO = 1)	—	250	—	ms	

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 53. Oscillator frequency specifications*...continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE] = 01), low-power mode (HGO = 0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE] = 01), high-gain mode (HGO = 1)	—	1	—	ms	

[1] Other frequency limits may apply when external clock is being used as a reference for the FLL.
[2] When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
[3] Proper PC board layout procedures must be followed to achieve specifications.
[4] Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

6.3.4 Memories and memory interfaces

6.3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.3.4.1.1 Flash timing specifications - program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 54. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	[1]
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	[1]

[1] Maximum time based on expectations at cycling end-of-life.

6.3.4.1.2 Flash timing specifications - commands

Table 55. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	[1]
t_{pgmchk}	Program Check execution time	—	—	45	µs	[1]
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	[1]
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	[2]

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 55. Flash command timing specifications*...continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	[1]
t_{rdonce}	Read Once execution time	—	—	25	µs	[1]
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	70	575	ms	[2]
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	[1]
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	70	575	ms	[2]

[1] Assumes 25 MHz flash clock frequency.
[2] Maximum times for erase parameters based on expectations at cycling end-of-life.

6.3.4.1.3 Flash high voltage current behaviors

Table 56. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5 mA	6.0 mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5 mA	4.0 mA

6.3.4.1.4 Reliability specifications

Table 57. NVM reliability specifications

Symbol	Description	Min.	Typ. [1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	[2]

[1] Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
[2] Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

6.3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.3.6 Analog

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

6.3.6.1 ADC electrical specifications

Using differential inputs can achieve better system accuracy than using single-end inputs.

6.3.6.1.1 16-bit ADC operating conditions

Table 58. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. [1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
Δ_{VDDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	[2]
Δ_{VSSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	[2]
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	V_{REFL} V_{REFL}	— —	31/32 × V_{REFH} V_{REFH}	V	—
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance	—	—	2	5	kΩ	—
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK}	—	—	5	kΩ	[3]
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	[4]
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	[4]
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	ksps	—
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	—

[1] Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
[2] DC potential difference.
[3] This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
[4] To use the maximum ADC conversion clock frequency, CFG1[ADLPC] must be clear.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

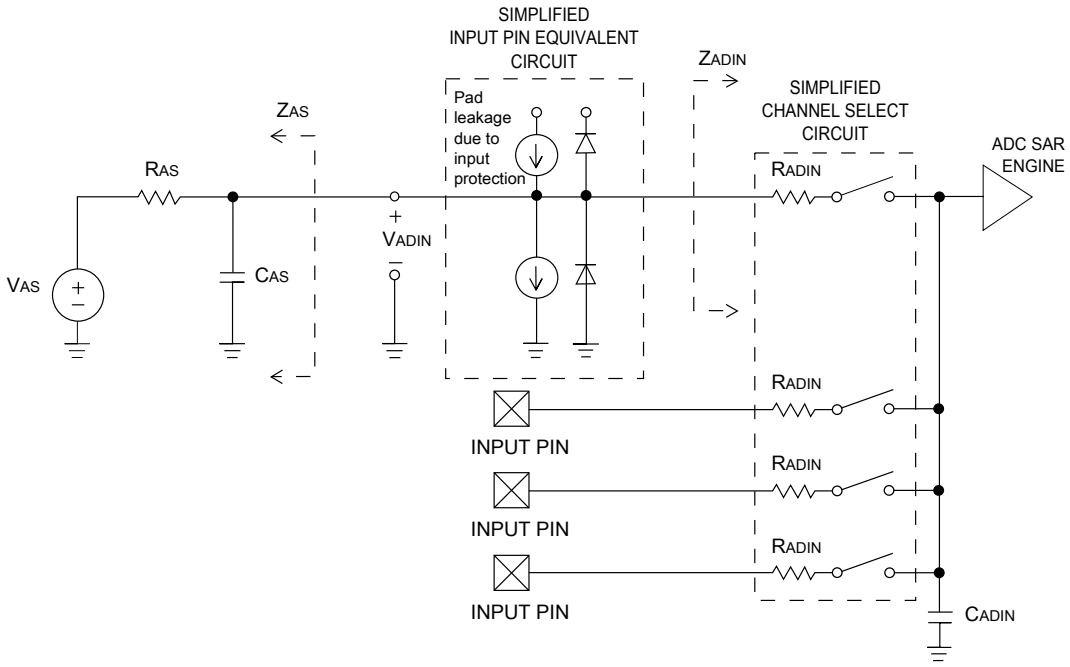


Figure 21. ADC input impedance equivalency diagram

6.3.6.1.2 16-bit ADC electrical characteristics

Table 59. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit	Notes
I_{DDA_ADC}	Supply current	—	0.215	—	1.7	mA	
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = $1/f_{ADACK}$
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes	—	±2	±6.8	LSB [1]	[2]
		• <12-bit modes	—	±1.4	±2.1	LSB[1]	
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	–1.1 to +1.9	LSB[1]	[2]
		• <12-bit modes	—	±0.2	–0.3 to 0.5	LSB[1]	

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 59. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA} *...continued*

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit	Notes
INL	Integral non-linearity	• 12-bit modes	—	±0.9	–2.7 to +1.9	LSB[1]	[2]
		• <12-bit modes	—	±0.5	–0.7 to +0.5	LSB[1]	
E_{FS}	Full-scale error	• 12-bit modes	—	–4	–5.4	LSB[1]	V_{ADIN} = V_{DDA} [2]
		• <12-bit modes	—	–1.4	–1.8	LSB[1]	
E_Q	Quantization error	• 16-bit modes	—	–1 to 0	—	LSB[1]	—
		• ≤13-bit modes	—	—	±0.5	LSB[1]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32	12.8	14.5	—	bits	[3]
		• Avg = 4	11.9	13.8	—	bits	
		16-bit single-ended mode • Avg = 32	12.2	13.9	—	bits	
		• Avg = 4	11.4	13.1	—	bits	
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	—
THD	Total harmonic distortion	16-bit differential mode • Avg = 32	—	-94	—	dB	[4]
		16-bit single-ended mode • Avg = 4	—	-85	—	dB	
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32	82	95	—	dB	[4]
		16-bit single-ended mode • Avg = 32	78	90	—	dB	
E_{IL}	Input leakage error	—	I_{In} × R_{AS}			mV	I_{In} (refer to the MCU's voltage and current

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 59. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA} *...continued*

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit	Notes
							operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	[5]
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	[5]

[1] 1 LSB = (V_{REFH} - V_{REFL})/2^N
[2] ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11).
[3] Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
[4] Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
[5] ADC conversion clock < 3 MHz.

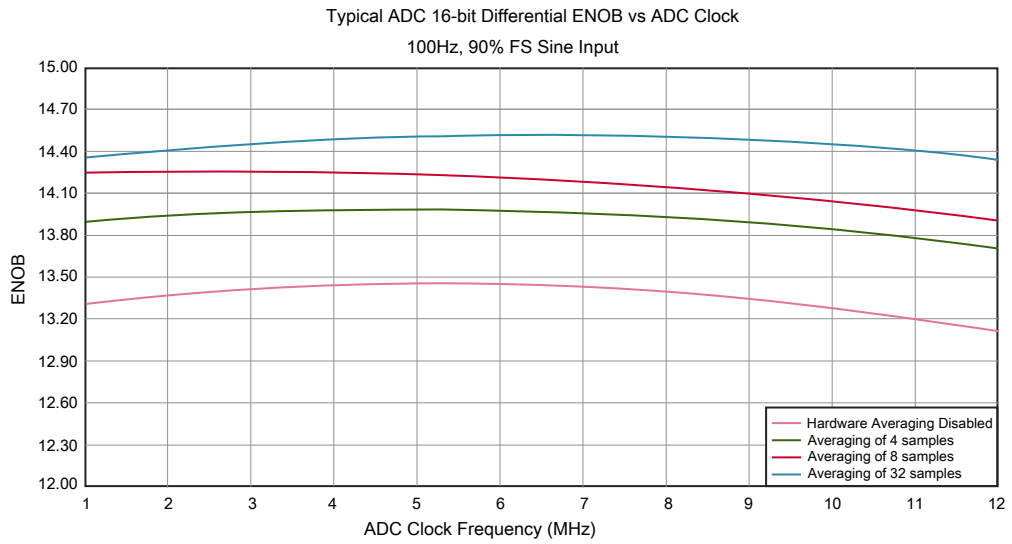


Figure 22. Typical ENOB vs. ADC_CLK for 16-bit differential mode

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

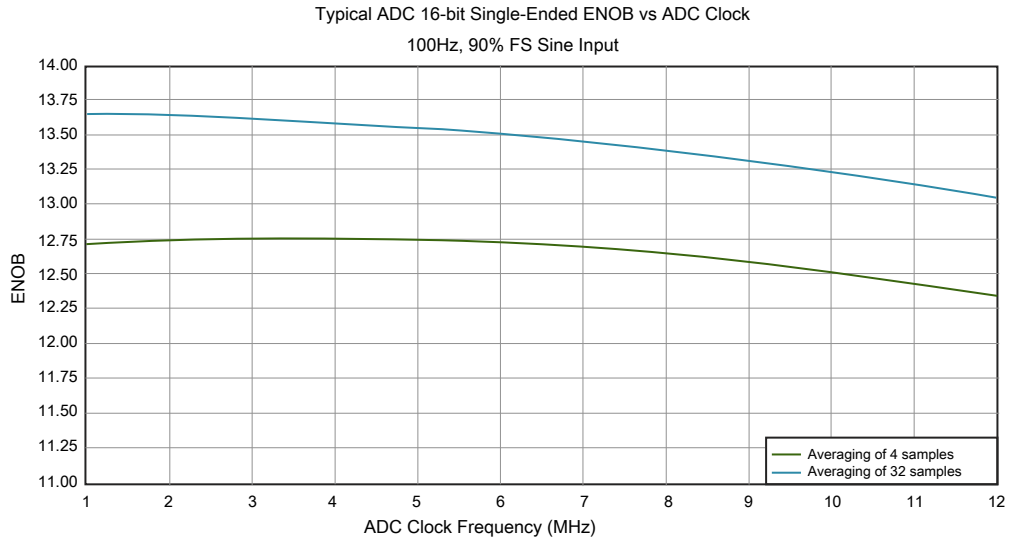


Figure 23. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.3.6.2 Voltage reference electrical specifications

Table 60. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	—
T_A	Temperature	Operating temperature range of the device		°C	—
C_L	Output load capacitance	100		nF	[1], [2]

[1] C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
[2] The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 61 is tested under the condition of setting VREF_TRM[CHOPEN], VREF_SC[REGEN] and VREF_SC[ICOMPEN] bits to 1.

Table 61. VREF full-range (-40 - 105 °C) operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA}	1.1915	1.195	1.1977	V	[1]
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	[1]
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	[1]
V_{step}	Voltage reference trim step	—	0.5	—	mV	[1]
I_{bg}	Bandgap only current	—	—	80	µA	[1]

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 61. VREF full-range (-40 - 105 °C) operating behaviors...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{hp}	High-power buffer current	—	—	1	mA	[1]
Δ_{VLOAD}	Load regulation	—	200	—	µV	[1], [2]
T_{stup}	Buffer startup time	—	—	100	µs	—
$T_{chop_osc_stup}$	Internal bandgap start-up delay with chop oscillator enabled	—	—	35	ms	—
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	[1]

[1] See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
[2] Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load.

Table 62. VREF limited-range (0 - 50°C) operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	—

6.3.6.3 CMP and 6-bit DAC electrical specifications

Table 63. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN = 1, PMODE = 1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} - 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis [1] • CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} - 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 63. Comparator and 6-bit DAC electrical specifications...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit
t_{DHS}	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	250	600	ns
	Analog comparator initialization delay [2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB [3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

[1] Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD} - 0.6 V.
[2] Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
[3] 1 LSB = $V_{reference}/64$

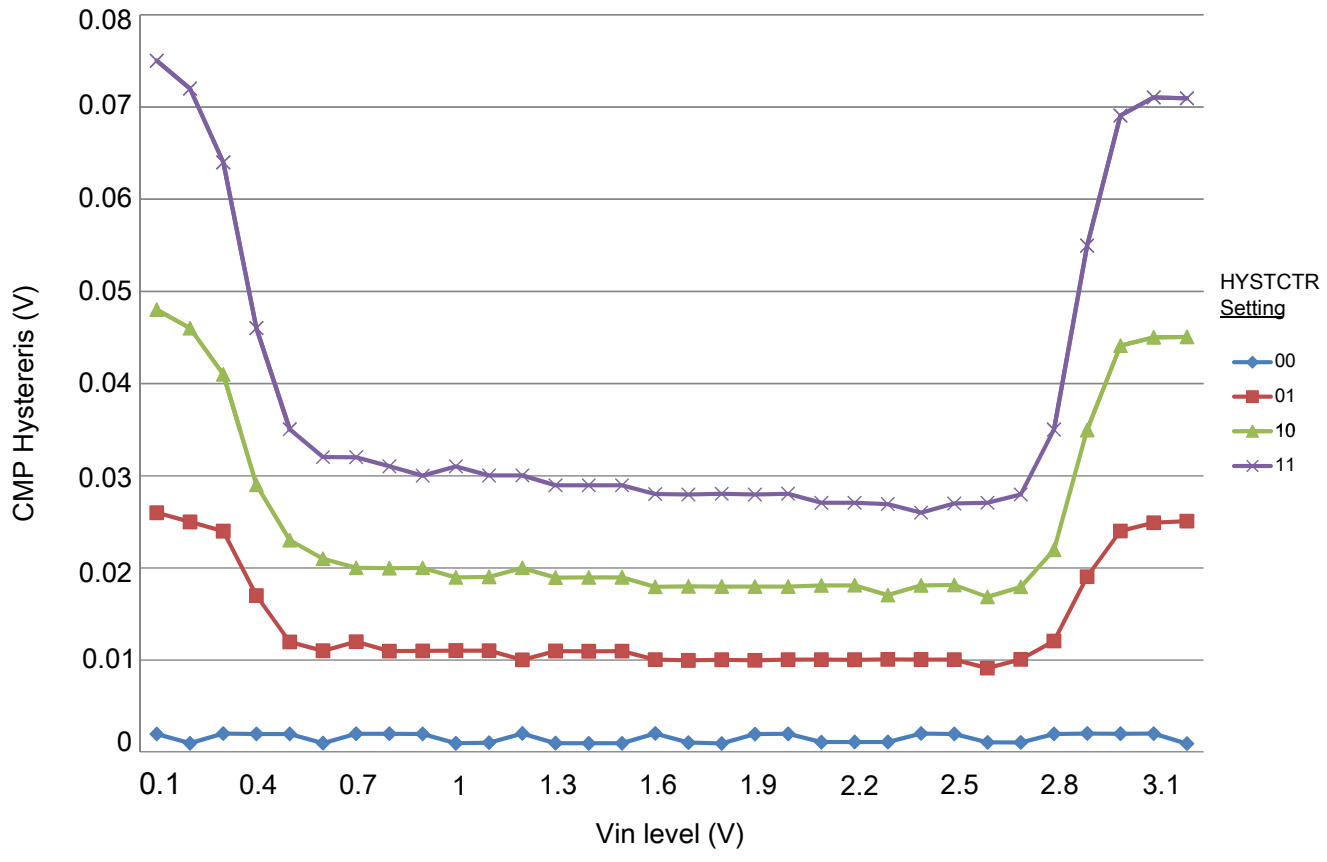


Figure 24. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

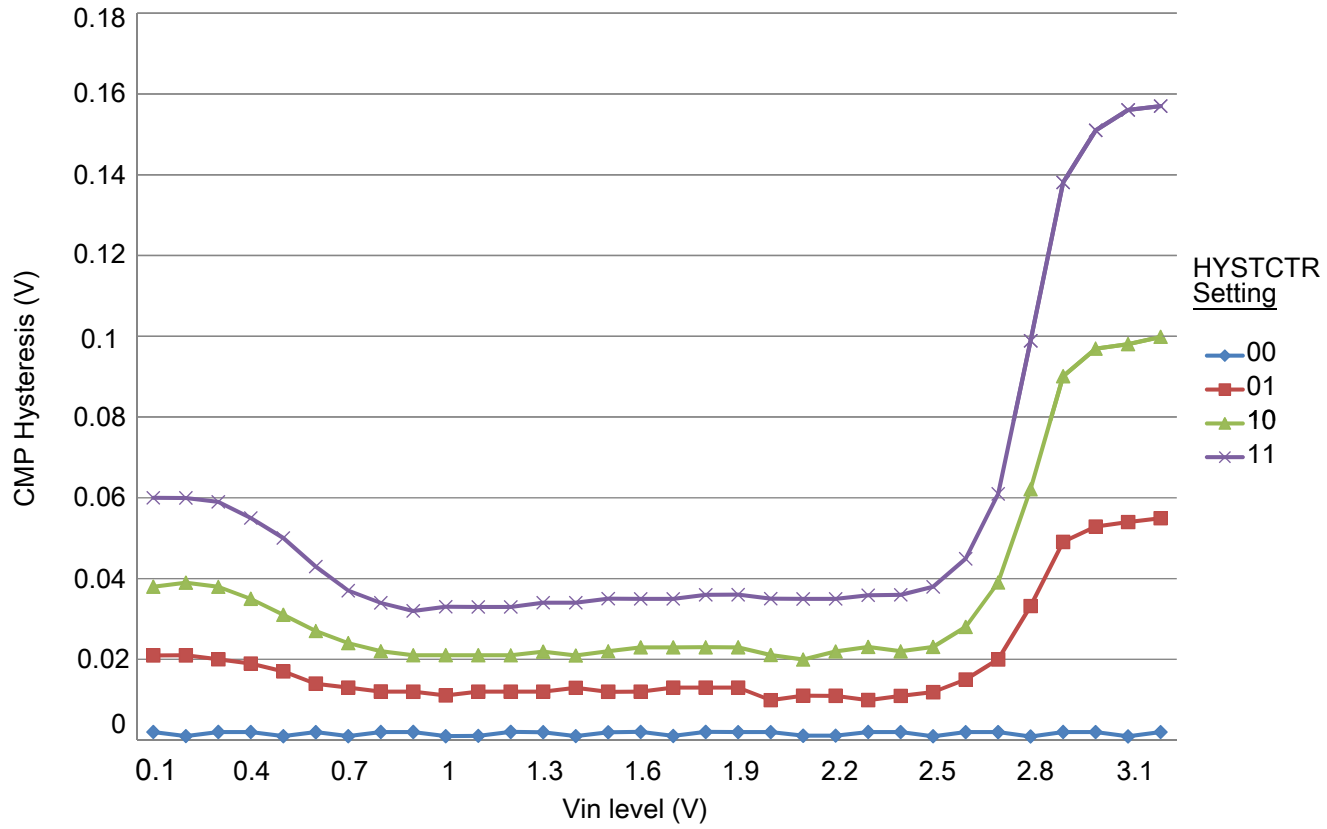


Figure 25. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.3.7 Timers

See General switching specifications.

6.3.8 Communication interfaces

6.3.8.1 USB electrical specifications

The USB electrical for the USB device module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

Note:

The IRC48M meets the USB jitter specifications for certification in Device mode when the USB clock recovery mode is enabled.

This device cannot support Host mode operation.

6.3.8.2 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with controller and target operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 64. SPI controller mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

Table 65. SPI controller mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	52	ns	—

Table continues on the next page...

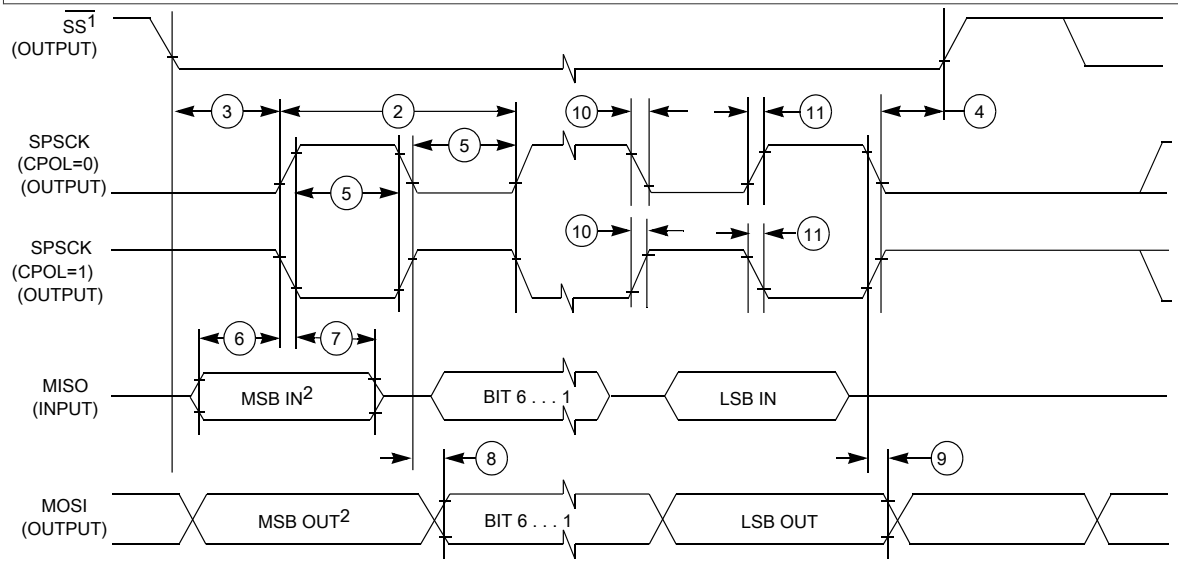
All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 65. SPI controller mode timing on slew rate enabled pads...*continued*

Num.	Symbol	Description	Min.	Max.	Unit	Note
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph}- 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

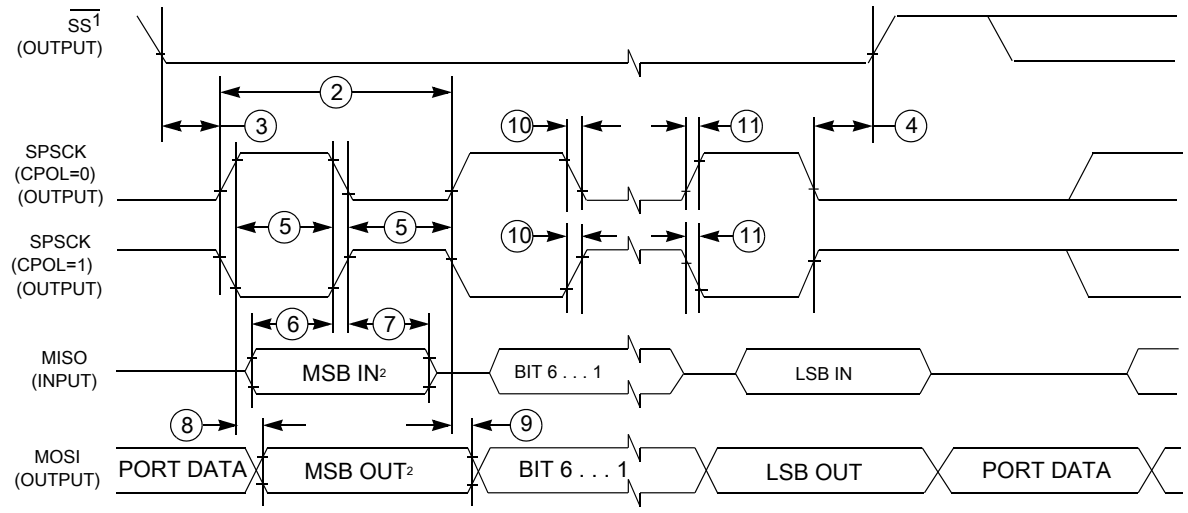
Figure 26. SPI controller mode timing (CPHA = 0)



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 27. SPI controller mode timing (CPHA = 1)

Table 66. SPI target mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	f_{periph} / 4	Hz	[1]
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	[2]
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Target access time	—	t_{periph}	ns	[3]
9	t_{dis}	Target MISO disable time	—	t_{periph}	ns	[4]
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph}- 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

[1] For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
[2] $t_{periph} = 1/f_{periph}$

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

[3] Time to data active from high-impedance state
[4] Hold time to high-impedance state

Table 67. SPI target mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	f_{periph} / 4	Hz	
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Target access time	—	t_{periph}	ns	
9	t_{dis}	Target MISO disable time	—	t_{periph}	ns	
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph}- 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

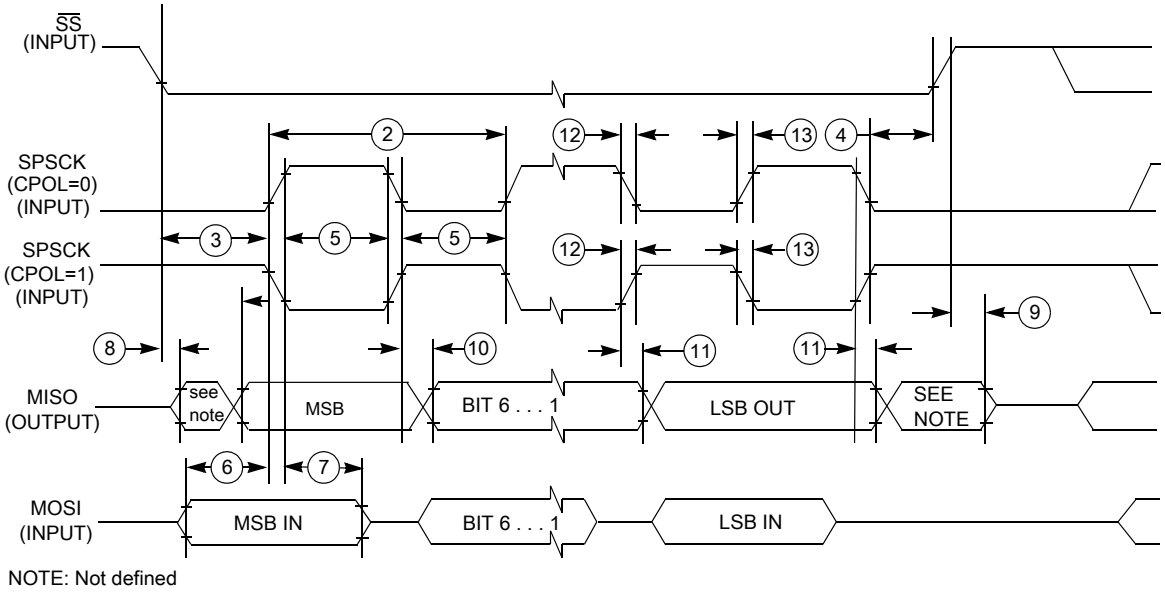


Figure 28. SPI target mode timing (CPHA = 0)

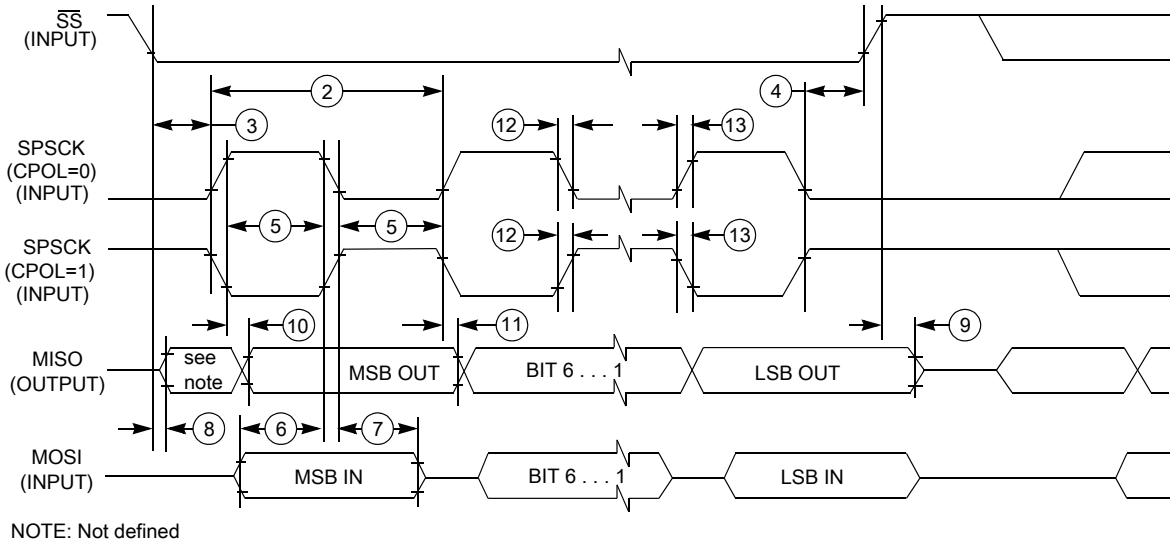


Figure 29. SPI target mode timing (CPHA = 1)

6.3.8.3 Inter-Integrated Circuit Interface (I2C) timing

Table 68. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400 [1]	kHz

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 68. I2C timing...*continued*

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus device	t_{HD}; DAT	0 [2]	3.45 [3]	0 [4]	0.9[2]	µs
Data set-up time	t_{SU}; DAT	250 [5]	—	100[3] , [6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 + 0.1C_b [7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b [6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

[1] The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the high drive pins across the full voltage range and when using the normal drive pins and VDD ≥ 2.7 V.
[2] The controller mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no target acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
[3] The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
[4] Input signal Slew = 10 ns and Output Load = 50 pF
[5] Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
[6] A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\ DAT}$ ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + $t_{SU;\ DAT}$= 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
[7] C_b = total capacitance of the one bus line in pF.

To achieve 1MHz I^2C clock rates, consider the following recommendations:

- To counter the effects of clock stretching, the I^2C baud rate select bits can be configured for faster than desired baud rate.
- Use high drive pad and DSE bit should be set in PORTx_PCRn register.
- Minimize loading on the I^2C SDA and SCL pins to ensure fastest rise times for the SCL line to avoid clock stretching.
- Use smaller pull up resistors on SDA and SCL to reduce the RC time constant.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 69. I²C 1 Mbit/s timing

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f_{SCL}	0	1 [1]	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	0.26	—	µs
LOW period of the SCL clock	t_{LOW}	0.5	—	µs
HIGH period of the SCL clock	t_{HIGH}	0.26	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	0.26	—	µs
Data hold time for I²C bus devices	t_{HD}; DAT	0	—	µs
Data set-up time	t_{SU}; DAT	50	—	ns
Rise time of SDA and SCL signals	t_r	20 +0.1C_b	120	ns
Fall time of SDA and SCL signals	t_f	20 +0.1C_b [2]	120	ns
Set-up time for STOP condition	t_{SU}; STO	0.26	—	µs
Bus free time between STOP and START condition	t_{BUF}	0.5	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

[1] The maximum SCL clock frequency of 1 Mbit/s can support maximum bus loading when using the high drive pins across the full voltage range.
[2] C_b = total capacitance of one bus line in pF.

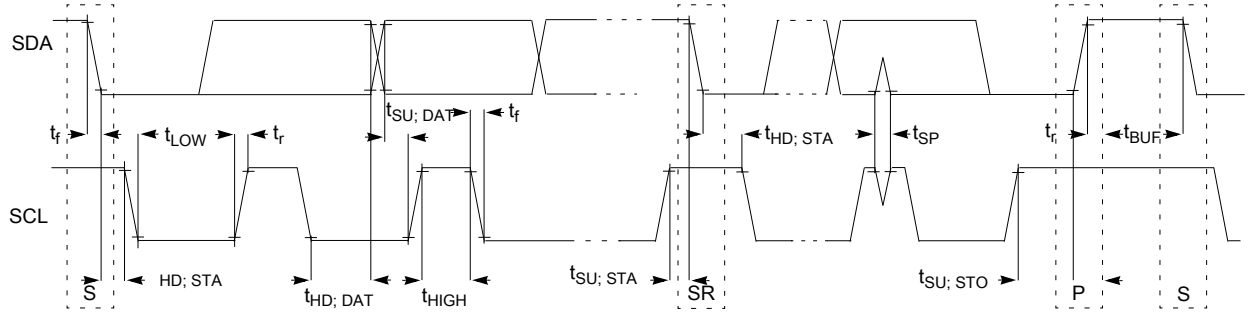


Figure 30. Timing definition for devices on the I²C bus

6.3.8.4 UART

See General switching specifications.

7 Design considerations

7.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7.1.1 Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP packages; and solder the exposed pad (EP) to ground directly under QFN packages.

7.1.2 Power delivery system

Consider the following items in the power delivery system:

- Use a plane for ground.
- Use a plane for MCU VDD supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10 µF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDD/VSS pair, including VDDA/VSSA and VREFH/VREFL.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as near as possible to the package supply pins.
- The USB_VDD voltage range is 3.0 V to 3.6 V. It is recommended to include a filter circuit with one bulk capacitor (no less than 2.2 µF) and one 0.1 µF capacitor at the USB_VDD pin to improve USB performance.
- Take special care to minimize noise levels on the VREFH/VREFL inputs. An option is to use the internal reference voltage (output 1.2 V typically) as the ADC reference.

Note: *The internal reference voltage output (VREFO) is bonded to the VREFH pin on some packages and to PTE30 on other packages. When the VREFO output is used, a 0.1 µF capacitor is required as a filter. Do not connect any other supply voltage to the pin that has VREFO activated.*

7.1.3 Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be RAS max if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.

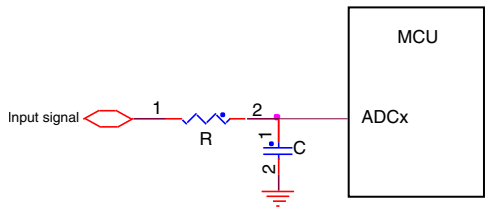


Figure 31. RC circuit for ADC input

High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown in the following figure. The voltage divider formed by R1-R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. Since the ADC pins do not have diodes to VDD, external clamp diodes must be included to protect against transient over-voltages.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

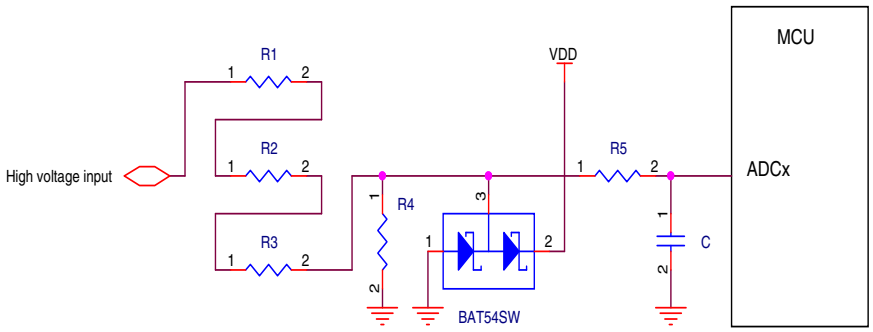


Figure 32. High voltage measurement with an ADC input

7.1.4 Digital design

Ensure that all I/O pins cannot get pulled above VDD (Max I/O is VDD + 0.3 V).

Caution: Do not provide power to I/O pins prior to VDD, especially the RESET_b pin.

- RESET_b pin

  The RESET_b pin is an open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

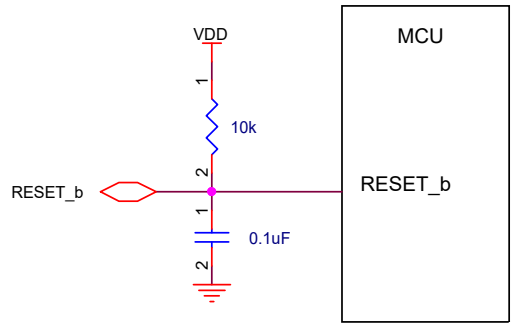


Figure 33. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin. The series resistor value (RS) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

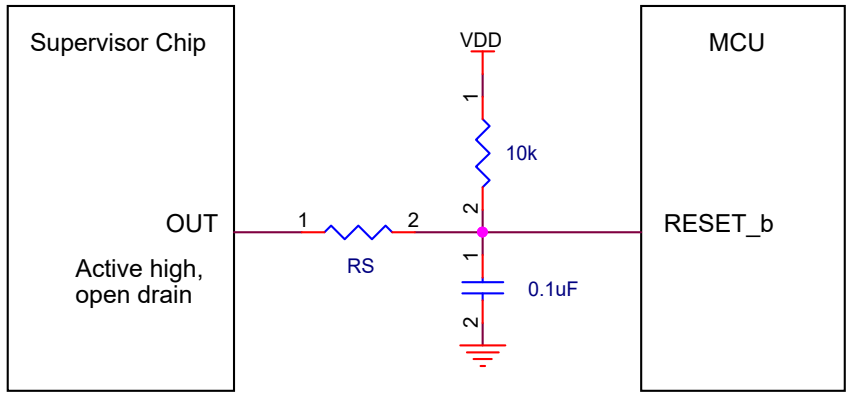


Figure 34. Reset signal connection to external reset chip

- NMI pin

  Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

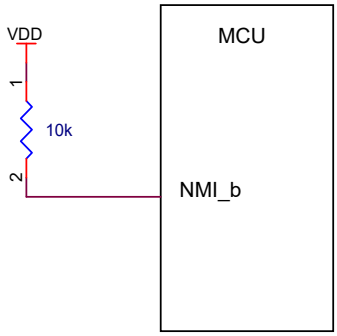


Figure 35. NMI pin biasing

- Debug interface

  This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

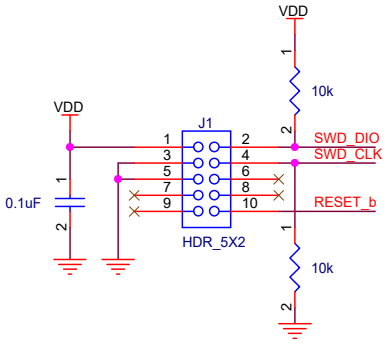


Figure 36. SWD debug interface

- Low leakage stop mode wakeup

  Select low leakage wakeup pins (LLWU_Px) to wake the MCU from one of the low leakage stop modes (LLS/VLLSx). See Signal Multiplexing and Pin Assignments.

- Unused pin

  Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

  If the USB module is not used, leave the USB data pins (USB0_DP, USB0_DM) floating. Connect USB_VDD to ground through a 10 kΩ resistor if the USB module is not used.

7.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO = 1) mode.

The series resistor, RS, is required in high gain (HGO = 1) mode when the crystal or resonator frequency is below 2 MHz. Otherwise, the low power oscillator (HGO=0) must not have any series resistance; and the high frequency, high gain oscillator with a frequency above 2 MHz does not require any series resistance.

Internal load capacitors (Cx, Cy) are provided in the low frequency (32.768 kHz) mode. Use the SCxP bits in the OSC0_CR register to adjust the load capacitance for the crystal. Typically, values of 10 pF to 16 pF are sufficient for 32.768 kHz crystals that have a 12.5 pF CL specification. The internal load capacitor selection must not be used for high frequency crystals and resonators.

Table 70. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768 kHz), low power	Diagram 1
Low frequency (32.768 kHz), high gain	Diagram 2, Diagram 4
High frequency (1-32 MHz), low power	Diagram 3
High frequency (1-32 MHz), high gain	Diagram 4

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

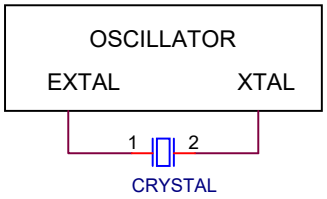


Figure 37. Crystal connection - Diagram 1

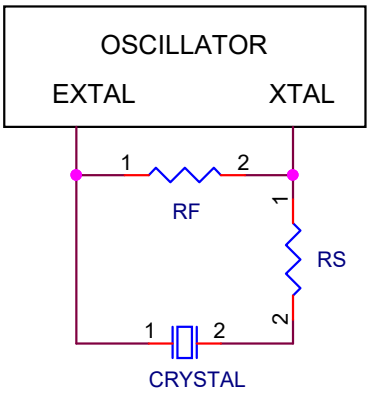


Figure 38. Crystal connection - Diagram 2

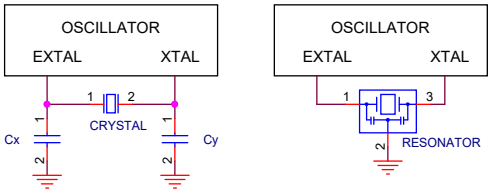


Figure 39. Crystal connection - Diagram 3

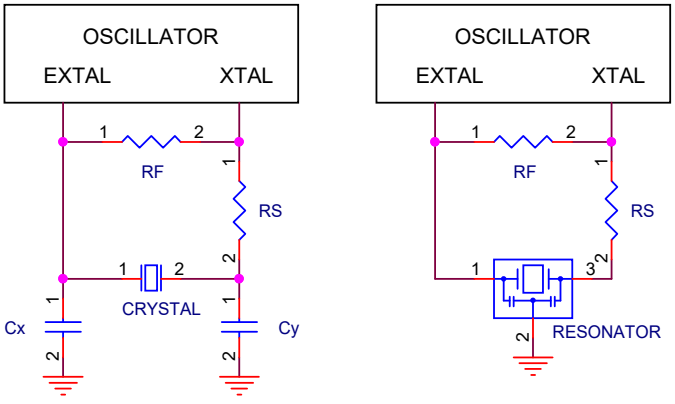


Figure 40. Crystal connection - Diagram 4

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

8 Part identification

8.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

8.2 Format

Part numbers for this device have the following format:

B PS F D FS T PG SR PT

8.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 71. Part number fields description

Field	Description	Values
B	Brand	• MCX
PS	Product series name	• C
F	Family	• 0 = Entry • 1 = Baseline • 2 = Baseline Enhance • 3 = Reserved • 4 = HMI
C	Core Features	• 4 = 48 MHz
FS	Flash Size	• 1 = 32 KB • 2 = 64 KB • 3 = 128 KB • 4 = 256 KB
T	Junction Temperature range	• V = -40 to 125 °C
PG	Package	• FG = 16QFN 3x3x0.65 mm • FK = 24QFN 4x4x0.65 mm • FM = 32QFN 5x5x0.5 mm • FT = 48QFN: 7x7x0.5 mm • LH = 64LQFP 10x10x1.6 mm • MP = 64MAPBGA: 5x5x1.23 mm
SR	Silicon Revision	• A = Initial Mask set • B = 1st Major spin

Table continues on the next page...

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 71. Part number fields description...*continued*

Field	Description	Values
PT	Package Type	• R = Tape and Reel • T = Tray

8.4 Example

This is an example part number:

MCXC242VLH

9 Revision history

The following table provides a revision history for this document.

Table 72. Revision history

Document ID	Released date	Descriptions
MCXC24XP64M48SF2 v4.1	19 August 2026	• Updated Table 1 • Added Table 2
MCXC24XP64M48SF2 v4.0	11 May 2025	• Added a row and footnote to Voltage and current operating behaviors. • Replaced -40 for die junction temperature with " - " and added -40 in row for Ambient temperature in Thermal operating requirements
MCXC24XP64M48SF2 v3.0	March 2025	Updated the footnote 4 for table 16-bit ADC operating conditions.
MCXC24XP64M48SF2 v2.0	July 2024	Initial release.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

NXP — wordmark and logo are trademarks of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Contents

1 Introduction....2
2 System features....5
2.1 ARM Cortex-M0+ core....5
2.2 NVIC....6
2.3 AWIC....6
2.4 Memory....6
2.5 Reset and boot....7
2.6 Clock options....8
2.7 Security....11
2.8 Power management....11
2.9 LLWU....13
2.10 Debug controller....14
2.11 COP....14
3 Peripheral features....14
3.1 BME....14
3.2 DMA and DMAMUX....14
3.3 TPM....15
3.4 ADC....15
3.4.1 Temperature sensor....16
3.5 VREF....16
3.6 CMP....16
3.7 RTC....17
3.8 PIT....17
3.9 LPTMR....17
3.10 CRC....17
3.11 UART....18
3.12 LPUART....18
3.13 SPI....19
3.14 I2C....19
3.15 USB....20
3.16 FlexIO....20
3.17 Port control and GPIO....20
4 Memory map....22
5 Pinouts....22
5.1 Signal Multiplexing and Pin Assignments....23
5.1.1 MCX C24X signal multiplexing and pin assignments....23
5.1.2 MCX C14X signal multiplexing and pin assignments....27
5.2 Pin properties....31
5.3 Module Signal Description Tables....35
5.3.1 Core modules....35
5.3.2 System modules....35
5.3.3 Clock modules....36
5.3.4 Analog....36
5.3.5 Timer Modules....37
5.3.6 Communication interfaces....38
5.3.7 Human-machine interfaces (HMI)....39
5.4 MCX C24X family pinouts....39
5.4.1 MCX C24X family pinouts....39
5.4.2 MCX C14X family pinouts....41
5.5 Package dimensions....43
6 Electrical characteristics....47
6.1 Ratings....47
6.1.1 Thermal handling ratings....47
6.1.2 Moisture handling ratings....48
6.1.3 ESD handling ratings....48
6.1.4 Voltage and current absolute operating ratings....48
6.2 General....48
6.2.1 AC electrical characteristics....48
6.2.2 Nonswitching electrical specifications....49
6.2.2.1 Voltage and current operating requirements....49
6.2.2.2 LVD and POR operating requirements....50
6.2.2.3 Voltage and current operating behaviors....51
6.2.2.4 Power mode transition operating behaviors....52
6.2.2.5 Power consumption operating behaviors....52
6.2.2.6 EMC performance....62
6.2.2.7 Capacitance attributes....62
6.2.3 Switching specifications....63
6.2.3.1 Device clock specifications....63
6.2.3.2 General switching specifications....63
6.2.4 Thermal specifications....64
6.2.4.1 Thermal operating requirements....64
6.2.4.2 Thermal attributes....64
6.3 Peripheral operating requirements and behaviors....65
6.3.1 Core modules....65
6.3.1.1 SWD electrical specifications....65
6.3.2 System modules....66
6.3.3 Clock modules....66
6.3.3.1 MCG-Lite specifications....66
6.3.3.2 Oscillator electrical specifications....67
6.3.4 Memories and memory interfaces....70
6.3.4.1 Flash electrical specifications....70
6.3.5 Security and integrity modules....71
6.3.6 Analog....71
6.3.6.1 ADC electrical specifications....72
6.3.6.2 Voltage reference electrical specifications....76
6.3.6.3 CMP and 6-bit DAC electrical specifications....77
6.3.7 Timers....79
6.3.8 Communication interfaces....79
6.3.8.1 USB electrical specifications....79
6.3.8.2 SPI switching specifications....79
6.3.8.3 Inter-Integrated Circuit Interface (I2C) timing....84
6.3.8.4 UART....86
7 Design considerations....86
7.1 Hardware design considerations....86
7.1.1 Printed circuit board recommendations....87
7.1.2 Power delivery system....87
7.1.3 Analog design....87

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7.1.4 Digital design....88
7.1.5 Crystal oscillator....90
8 Part identification....92
8.1 Description....92
8.2 Format....92
8.3 Fields....92
8.4 Example....93
9 Revision history....93
Legal information....94

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2026 NXP B.V. All rights reserved.

For more information, please visit: https://www.nxp.com

Date of release: 19 August 2026
Document identifier: MCXC24XP64M48SF2