MP2720

2.5A, Single-Cell, I²C-Controlled NVDC Buck Charger

DESCRIPTION

The MP2720 is a highly integrated, 2.5A, switch-mode battery management device for single-cell Li-ion or Li-polymer batteries. The narrow-voltage DC (NVDC) power management structure provides a low impedance power path, that optimizes charging efficiency, reduces battery charging time, and extends battery life during discharging.

The device's input source type identification algorithm supports USB battery charging specification 1.2 (BC1.2) and non-standard adapter detection.

The I²C interface offers complete operating control, including charging parameter configurations and status/interrupt monitoring.

The MP2720 supports a fully customizable JEITA profile with configurable temperature windows and actions.

The MP2720 is available in a QFN-22 (2.5mmx3.5mm) package.

FEATURES

- Supports USB BC1.2 and Non-Standard Adapters
- 26V Sustainable Input Voltage (V_{IN})
- Configurable 80mA to 2.5A Charge Current (I_{CC}) via I²C
- Configurable 100mA to 3.2A Input Current Limit (I_{IN_LIM}) via I²C
- Minimum V_{IN} Loop for Maximum Adapter Power Tracking
- Comprehensive Safety Features:
  - Fully Customizable JEITA Profile
  - Additional Negative Temperature Coefficient (NTC) Thermistor Input
  - Configurable Die Temperature Regulation from 60°C to 120°C
  - Complete Charge and Pre-Charge Safety Timers
  - Watchdog Safety Timer
  - Lockable Registers for Charging Parameters
- Configurable 750kHz to 1.5MHz Switching Frequency (f_{SW})
- Integrated 15mΩ Low-$R_{DS(ON)}$ Battery MOSFET with Shipping and Reset Modes
- Ultra-Low 8.5μA Battery Discharge Current in Shipping Mode
- Down to 30mA Termination Current Settings for Wearable Applications
- I²C Port for Flexible System Parameter Setting and Status Reporting
- Configurable Boost Converter for Source Mode and USB On-The-Go (OTG):
  - Configurable Output Current Limit Loop Up to 3A
  - Output Over-Current Protection (OCP)
  - Ability to Power into Large Capacitive Loads Up to 2mF
  - Configurable 5V to 5.35V Output Voltage
- Accuracy:
  - ±0.5% Battery Regulation Voltage (V_{BATT_REG})
  - ±5% I_{CC}
  - ±5% I_{IN_LIM}
  - Remote Battery Sensing for Fast Charge
  - ±2% Output Regulation in Boost Mode
- Available in a Small QFN-22 (2.5mmx3.5mm) Package

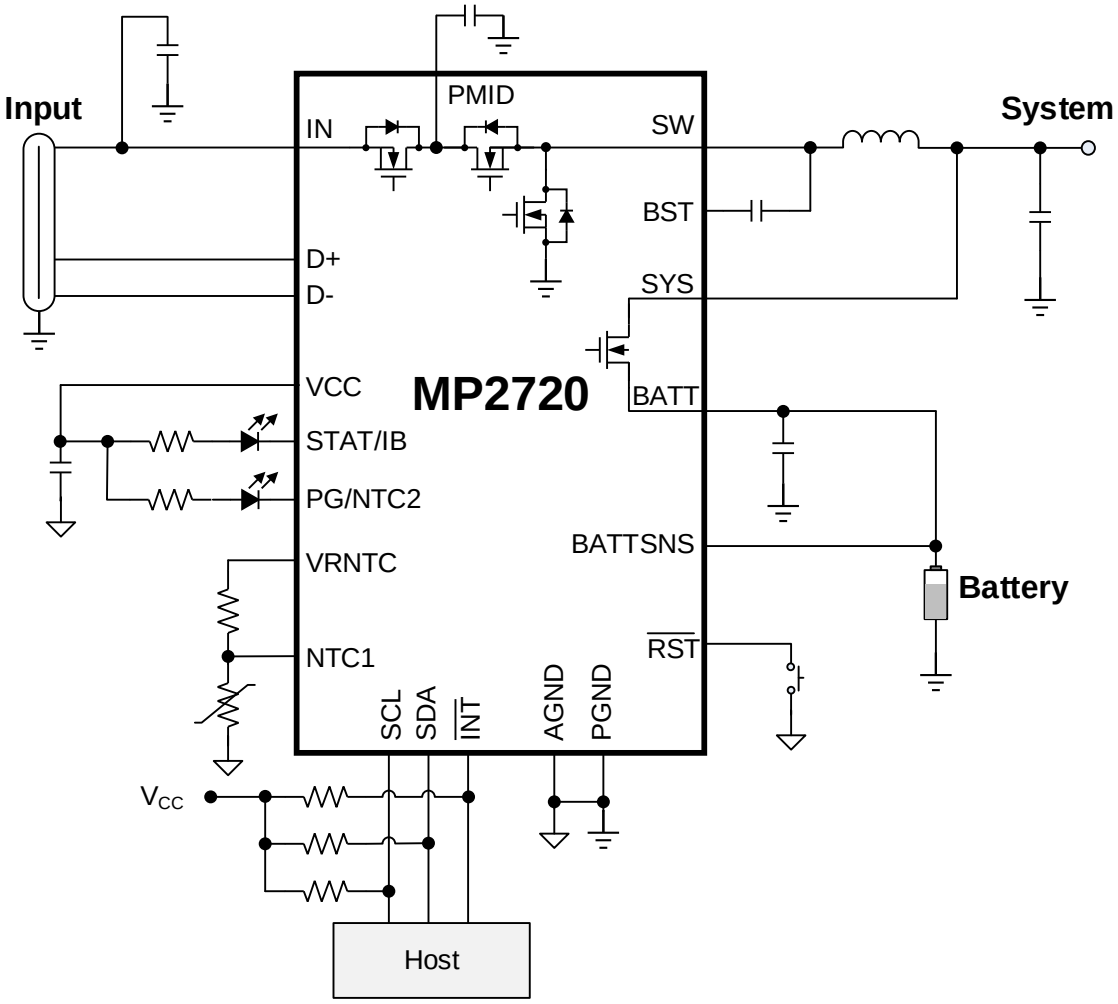
APPLICATIONS

- General ≤15W USB Applications
- Bluetooth Headphones
- Bluetooth Speakers
- Point-of-Sale (POS) Terminals
- Portable Cameras

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2720GRH-xxxx**	QFN-22 (2.5mmx3.5mm)	*See Below*	1
EVKT-MP2720	Evaluation kit	-	-

* For Tape & Reel, add suffix -Z (e.g. MP2720GRH-xxxx-Z).

** "xxxx" is the register setting option. The factory default code is "0000". This content can be viewed in the I²C register map. Contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

BVU
YWW
LLL

BVU: Product code of MP2720GRH-xxxx
Y: Year code
WW: Week code
LLL: Lot number

EVALUATION KIT EVKT-MP2720

EVKT-MP2720 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2720-RH-00A	MP2720 evaluation board	1
2	EVKT-USBI2C-02 bag	Includes one USB to I²C communication interface device, one USB cable, and one ribbon cable	1
3	Online resources	Include the datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

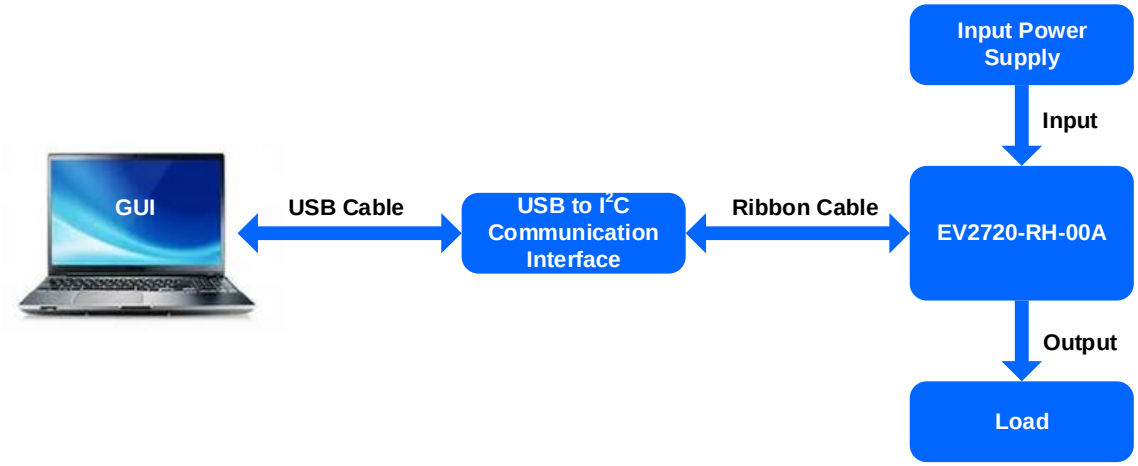
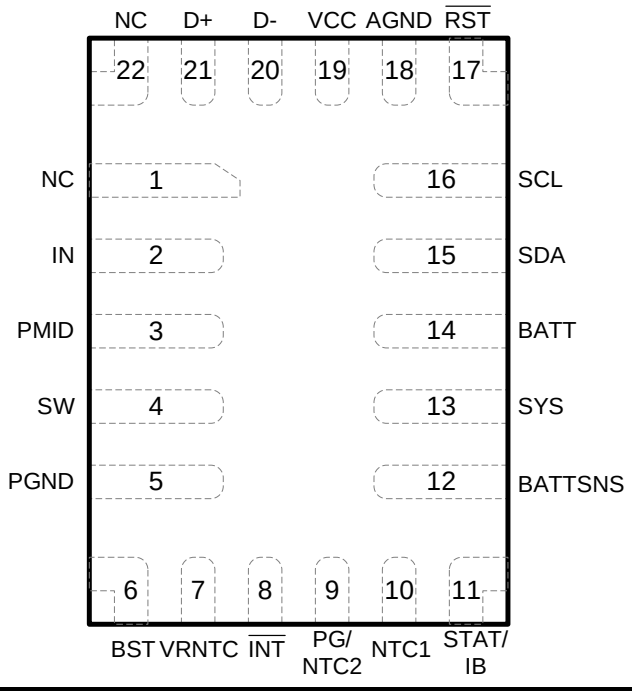


Figure 1: EVKT-MP2720 Evaluation Kit Set-Up

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PACKAGE REFERENCE



QFN-22 (2.5mmx3.5mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Type (1)	Description
2	IN	P	**Power input.** Connect a 1µF ceramic capacitor from the IN pin to PGND.
3	PMID	P	**Decoupling node for the power stage.** Bypass the PMID pin with a minimum 10µF ceramic capacitor connected from PMID to PGND, and placed as close to the IC as possible with the shortest possible route.
4	SW	P	**Switching node.** Connect the SW pin to the inductor.
6	BST	P	**Bootstrap power.** Connect a 22nF capacitor between the BST and SW pins to form a floating supply for the high-side MOSFET (HS-FET) driver.
13	SYS	P	**System power output.** Connect a minimum 20µF ceramic capacitor from the SYS pin to PGND.
14	BATT	P	**Battery positive terminal.** The internal narrow-voltage DC (NVDC) battery MOSFET is connected between the SYS and BATT pins. Place a minimum 20µF ceramic capacitor from BATT to PGND.
5	PGND	P	**Power ground.** Short the PGND pin to AGND on the PCB.
18	AGND	P	**Analog ground.** Short the AGND pin to PGND on the PCB.
19	VCC	P	**Internal circuit power supply.** Connect a 4.7µF ceramic capacitor from the VCC pin to AGND, placed as close to the IC as possible.
12	BATTSNS	AI	**Battery voltage-sense pin for battery voltage regulation.** Connect the BATTSNS pin as close as possible to the battery pack's positive terminal.
8	$\overline{\text{INT}}$	DO	**Open-drain interrupt output.** This pin generates an active low 256µs pulse when the IC has a status or fault report. Pull this pin up to VCC or another logic rail with a 10kΩ resistor.
16	SCL	DI	**I²C interface clock.** Pull the SCL pin up to VCC or another logic rail with a 10kΩ resistor.
15	SDA	DIO	**I²C interface data.** Pull the SDA pin up to VCC or another logic rail with a 10kΩ resistor.
1, 22	NC	-	**No connection.** The NC pin can be left open or shorted to AGND.
21	D+	AIO	**Positive line of the USB data line pair.** USB charger type detection is based on BC1.2. Non-standard adapter detection can also be implemented.
20	D-	AIO	**Negative line of the USB data line pair.** USB charger type detection is based on BC1.2. Non-standard adapter detection can also be implemented.
17	$\overline{\text{RST}}$	DI	**Battery MOSFET reset input.** During shipping mode, pull this pin to logic low for a set time ($t_{SHIPMODE}$) to wake up the IC from shipping mode. When the input voltage (V_{IN}) is not present, setting this pin to logic low for a set time (t_{RST}) resets the SYS power by turning the battery MOSFET off for a set time (t_{SYS_RST}). Then the battery MOSFET is re-enabled. This pin is internally pulled up by a 200kΩ resistor. Float this pin if it is not used.
7	VRNTC	AO	**Voltage output for powering up the NTC.** The VRNTC pin is powered up to the same voltage as VCC when the buck or boost converter operates.
10	NTC1	AI	**Temperature-sense input 1.** Connect the NTC1 pin to a negative temperature coefficient (NTC) thermistor. Connect a resistor divider from VRNTC to NTC1 to AGND. NTC1 supports a JEITA profile.
9	PG/NTC2	DO/AI	**Open-drain power good (PG) indicator.** Pull the PG/NTC2 pin up with a 10kΩ resistor. This pin is active low when the VIN_GD bit = 1, and it can be configured to act as temperature-sense input 2.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PIN FUNCTIONS *(continued)*

Pin #	Name	Type (1)	Description
11	STAT/IB	DO/AO	**Charge status open-drain output.** Pull the STAT/IB pin up with a 10kΩ resistor. This pin goes low to indicate when charging is in progress; it goes high to indicate when charging is complete or not in progress. It blinks at a frequency of 1Hz if a fault occurs. This pin can also be configured for battery current indication (IB). The IB pin sources a current that is proportional to the battery's charge or discharge current. Connect a resistor from IB to AGND for the battery current information.

Note:

1) AI = analog input, AO = analog output, AIO = analog input output, DI = digital input, DO = digital output, DIO = digital input output, P = power.

ABSOLUTE MAXIMUM RATINGS (2)

IN to PGND .....-0.3V to +26V
PMID to PGND .....-0.3V to +26V
SW to PGND.....-0.3V (-2V for 20ns) to +24V
PMID to IN .....-0.3V to +12V
BATT, SYS to PGND .....-0.3V to +6.5V
BST to SW…….....-0.3V to +5V
All other pins to AGND.....-0.3V to +5V
Continuous power dissipation (T_A = 25°C) (3) 2W
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature…….. -65°C to +150°C

ESD Ratings

Human body model (HBM) (4)..... 2000V
Charged device model (CDM) (5)..... 250V

Recommended Operating Conditions (7)

Supply voltage (V_{IN}) .....3.9V to 6.3V
Input current (I_{IN}).....Up to 3.2A
System current (I_{SYS}).....Up to 5A
Charge current (I_{CC}) .....Up to 2.5A
Discharge current (I_{DISCHG}) .....Up to 8A
Battery voltage (V_{BATT}) .....Up to 4.6V
Operating junction temp (T_J)….-40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-22 (2.5mmx3.5mm)..... 50 ..... 12....°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per ANSI/ESDA/JEDEC JS-001, all pins.
5) Per ANSI/ESDA/JEDEC JS-002, all pins.
6) Measured on JESD51-7, 4-layer PCB.
7) The device is not guaranteed to function outside of its operating conditions.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Quiescent Current						
Battery discharge current in shipping mode	I_{BATT_SHIP}	V_{BATT} = 4V, V_{IN} = 0V, BATTFET disabled, T_A = -40°C to +85°C		8.5	12	µA
Battery discharge current in idle mode	I_{BATT_IDLE}	V_{BATT} = 4V, V_{IN} = 0V, BATTFET enabled, T_A = -40°C to +85°C		44	64	µA
USB suspend mode current	I_{IN_SUSP}	V_{IN} = 5V, EN_BUCK = 0		0.8		mA
Power-On/Off						
Input operating range	V_{IN_OP}		3.9		6.3	V
Input under-voltage lockout (UVLO) threshold	V_{IN_UV}	V_{IN} falling, V_{BATT} = 0V	3.1	3.25	3.45	V
Input UVLO hysteresis	$V_{IN_UV_HYS}$	V_{IN} rising, V_{BATT} = 0V		250		mV
Input debounce time	t_{DEB}	V_{IN} debounce to set VIN_GD		15		ms
Hold-off timer	t_{HOLD}	VIN_GD = 1 to D+ and D- detection starts		250		ms
Input vs. battery voltage headroom threshold	V_{HDRM}	V_{IN} - V_{BATT}, V_{BATT} = 4V, V_{IN} rising	135	240	340	mV
		V_{IN} - V_{BATT}, V_{BATT} = 4V, V_{IN} falling	10	80	175	mV
Input over-voltage protection (OVP) threshold	V_{IN_OV}	V_{IN} rising	6.1	6.3	6.55	V
Input OVP hysteresis	$V_{IN_OV_HYS}$	V_{IN} falling		250		mV
BATT UVLO threshold	V_{BATT_UV}	V_{IN} = 0V, V_{BATT} falling	2.4	2.5	2.6	V
BATT UVLO hysteresis	$V_{BATT_UV_HYS}$	V_{IN} = 0V, V_{BATT} rising		400		mV
Power Path						
System regulation voltage	V_{SYS_REG}	V_{BATT} < V_{SYS_MIN}, SYS_MIN = 100	3.7	3.82	3.94	V
Blocking FET on resistance	R_{ON_RBFET}	T_A = 25°C		15		mΩ
High-side MOSFET (HS-FET) on resistance	R_{ON_HS}	T_A = 25°C		25		mΩ
Low-side MOSFET (LS-FET on resistance	R_{ON_LS}	T_A = 25°C		25		mΩ
Battery MOSFET on resistance	R_{ON_BFET}	T_A = 25°C		14		mΩ
Battery MOSFET forward voltage in supplement mode	V_{FWD}			30		mV
Charge (T_A = 0°C to 70°C)						
Charge voltage configuration range	V_{BATT_RANGE}		3.6		4.6	V
Charge voltage step	V_{BATT_STEP}			25		mV
Battery charge voltage regulation	V_{BATT_REG}	VBATT = 4.2V	4.179	4.2	4.221	V
		VBATT = 4.35V	4.328	4.35	4.372	V
Charge current regulation range	I_{CC_RANGE}		0		2500	mA
Charge current step	I_{CC_STEP}			80		mA
Fast charge current	I_{CC}	ICC = 1040mA, V_{BATT} = 3.8V	0.98	1.04	1.15	A
		ICC = 2000mA, V_{BATT} = 3.8V	1.9	2	2.1	A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

T_A = -40°C to +125°C, T_A = 25°C and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Pre-charge to fast charge threshold	V_{BATT_PRE}	V_{BATT} rising, VPRE = 3V	2.9	3	3.1	V
Pre-charge to fast charge threshold hysteresis		V_{BATT} falling, VPRE = 3V		250		mV
Pre-charge current	I_{PRE}	IPRE = 240mA, V_{BATT} = 2.5V	207.5	240	277.5	mA
Charge termination current threshold	I_{TERM}	ITERM = 120mA	90	120	150	mA
		ITERM = 30mA	18	30	42	mA
Trickle charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising	1.9	2	2.1	V
Trickle charge to pre-charge threshold hysteresis		V_{BATT} falling		200		mV
Trickle charge current	I_{TC}	V_{BATT} = 1V, ITRICKLE = 128mA	100	128	160	mA
Auto-recharge battery voltage threshold	V_{RECH}	V_{BATT} falling, VRECHG = 100mV	45	90	135	mV
		V_{BATT} falling, VRECHG = 200mV	135	190	245	mV
Input Regulation (T_A = 0°C to 70°C)						
Input minimum voltage regulation	V_{IN_LIM}	VIN_LIM = 3.88V, V_{BATT} = 3.3V	3.758	3.88	4.002	V
		VIN_LIM = 4.36V, V_{BATT} = 3.3V	4.236	4.36	4.484	V
Input minimum voltage regulation tracking battery	$V_{IN_LIM_BATT}$	VIN_LIM = 3.88V, V_{BATT} = 4V	70	165	285	mV
Input current limit	I_{IN_LIM}	IIN_LIM = 500mA	415	450	500	mA
		IIN_LIM = 1.5A	1.34	1.41	1.5	A
		IIN_LIM = 3A	2.7	2.84	3	A
Battery Over-Voltage Protection (OVP)						
Battery OVP threshold	V_{BATT_OVP}	V_{BATT} rising, percentage of V_{BATT_REG}	103	105	106.5	%
Battery OVP hysteresis				1.7		%
Thermal						
Junction temperature regulation (8)	T_{J_REG}	TREG = 80°C		80		°C
		TREG = 120°C		120		°C
Thermal shutdown rising junction temperature (8)	T_{J_SHDN}	Temperature rising		150		°C
Thermal shutdown hysteresis (8)	T_{SHDN_HYS}			30		°C
JEITA NTC Monitor (T_A = 0°C to 70°C)						
NTC cold temperature rising threshold	V_{COLD}	As a percentage of V_{VRNTC}, VCOLD = 74.2% (0°C)	73.9	74.5	75.1	%
NTC cold temperature rising threshold hysteresis		As a percentage of V_{VRNTC}		1.4		%
NTC cool temperature rising threshold	V_{COOL}	As a percentage of V_{VRNTC}, VCOOL = 64.8% (10°C)	64.3	64.9	65.5	%
NTC cool temperature rising threshold hysteresis		As a percentage of V_{VRNTC}		1.4		%

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
NTC warm temperature falling threshold	V_{WARM}	As a percentage of V_{VRNTC}, VWARM = 32.6% (45°C)	31.9	32.5	33.1	%
NTC warm temperature falling threshold hysteresis		As a percentage of V_{VRNTC}		1.4		%
NTC hot temperature falling threshold	V_{HOT}	As a percentage of V_{VRNTC}, VHOT = 23% (60°C)	22.7	23.3	23.9	%
NTC hot temperature falling threshold hysteresis		As a percentage of V_{VRNTC}		1.4		%
BATTFET Over-Current Protection (OCP)						
BATTFET over-current (OC) threshold	I_{BATT_OCP}		7			A
PWM Converter						
Switching frequency	f_{SW}	SW_FREQ = 750kHz	630	750	895	kHz
		SW_FREQ = 1000kHz	900	1050	1280	kHz
		SW_FREQ = 1250kHz	1060	1250	1450	kHz
		SW_FREQ = 1500kHz	1260	1475	1680	kHz
Boost						
Boost regulation voltage	V_{PMID_REG}	VBOOST = 5.15V, T_A = -40°C to +85°C	5.08	5.15	5.22	V
BATT_LOW comparator falling threshold	V_{BATT_LOW}	BATT_LOW = 3V	2.88	3	3.12	V
		BATT_LOW = 3.3V	3.20	3.33	3.46	V
BATT_LOW comparator hysteresis				200		mV
BATT_LOW comparator debounce time	$t_{D_BATT_LOW}$			10		ms
Boost output current limit	I_{BST_LIM}	OLIM = 500mA, T_A = 0°C to 70°C	500		615	mA
		OLIM = 1.5A, T_A = 0°C to 70°C	1500		1700	mA
Boost OVP threshold	V_{BST_OVP}	Boost mode, V_{IN} rising	5.5	5.8	6.1	V
VCC LDO						
VCC output voltage	V_{VCC}	V_{IN} = 5V, I_{VCC} = 5mA		3.65		V
IB Output (T_A = 0°C to 70°C)						
IB current output gain	I_{IB}	I_{IB}, charging, I_{BATT} = 100mA	1.1	2	2.8	µA
		I_{IB}, charging, I_{BATT} = 1A	18.2	20	22.1	µA
		I_{IB}, discharging, I_{BATT} = 100mA	1.1	2	2.8	µA
		I_{IB}, discharging, I_{BATT} = 1A	18.2	20	22.1	µA
Impedance Test						
Input impedance test current	I_{VIN_SRC}	IVIN_SRC = 10µA	6	10	14	µA
		IVIN_SRC = 40µA	28	40	52	µA
		IVIN_SRC = 320µA	240	320	405	µA
Input impedance test voltage threshold	V_{VIN_TEST}	VIN_TEST = 0.5V	0.46	0.5	0.54	V
		VIN_TEST = 1.5V	1.4	1.5	1.6	V

Notes:

8) Guaranteed by design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

T_A = -40°C to +125°C, T_A = 25°C and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Logic I/O for SCL, SDA, INT, RST, STAT						
Logic input low voltage	V_{IL}				0.4	V
Logic input high voltage	V_{IH}		1.3			V
Open-drain output low voltage	V_{OL}	I_{SINK} = 10mA			0.2	V
RST pull-up resistor	R_{PULL_UP}			200		kΩ
D+/D- Detection						
DCD D+ pull up current	I_{DP_SRC}		7	10	13	μA
DCD D- pull low resistance	R_{DM_DWN}		16	20	24	kΩ
D+D- source voltage low	V_{SRC_L}		550	600	650	mV
D+D- source voltage high	V_{SRC_H}		3.1	3.3	3.5	V
D+D- sink current	I_{SNK}		50	100	150	μA
Data detect voltage	V_{DAT_REF}		300	350	400	mV
Non-standard 1.2V window	V_{1P2_TH}	Low threshold	0.95	1	1.05	V
		High threshold	1.33	1.4	1.47	V
Non-standard 2V window	V_{2P0_TH}	Low threshold	1.73	1.8	1.87	V
		High threshold	2.17	2.25	2.33	V
Non-standard 2.7V window	V_{2P7_TH}	Low threshold	2.3	2.4	2.5	V
		High threshold	2.9	3.0	3.1	V
Timing						
Battery Charger						
Charge termination deglitch time	t_{TERM_DGL}			250		ms
Charge timer	t_{CHG_TMR}	CHG_TIMER = 10hr	8	10	12	hr
Top-off timer	t_{TOP_OFF}	TOPOFF_TIMER = 30min	24	30	36	min
Battery auto-recharge deglitch time	t_{RECH_DGL}			100		ms
RST Timing						
RST low time to exit shipping mode	$t_{SHIPMODE}$		0.9	1.1	1.3	sec
RST low time to reset BATTFET	t_{RST}		8	10	12	sec
BATTFET reset time	t_{SYS_RST}		250	330	400	ms
Enter shipping mode delay	t_{SHIP_DLY}		10	12	15	sec
Watchdog and Clock						
Watchdog timer	t_{WDT}	WATCHDOG = 40s		40		sec
I²C clock	f_{SCL}				400	kHz

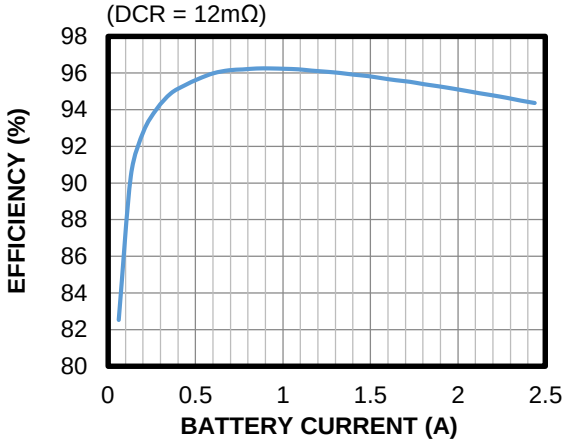
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1040mA, I_{IN_LIM} = 3A, V_{IN_MIN} = 4.36V, L = 1µH (DCR = 12mΩ), T_A = 25°C, unless otherwise noted.

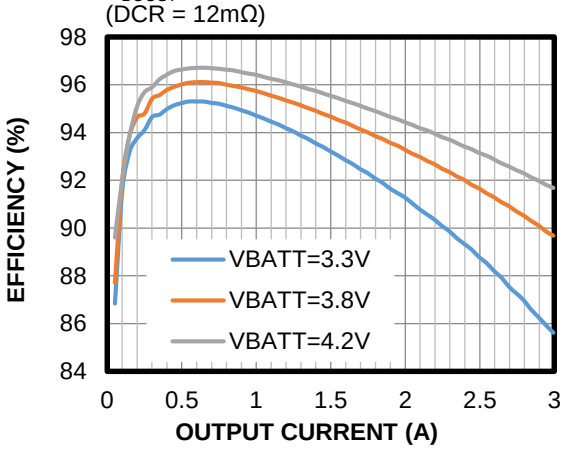
Charge Efficiency

V_{IN} = 5V, V_{BATT} = 3.8V, L = 1µH (DCR = 12mΩ)



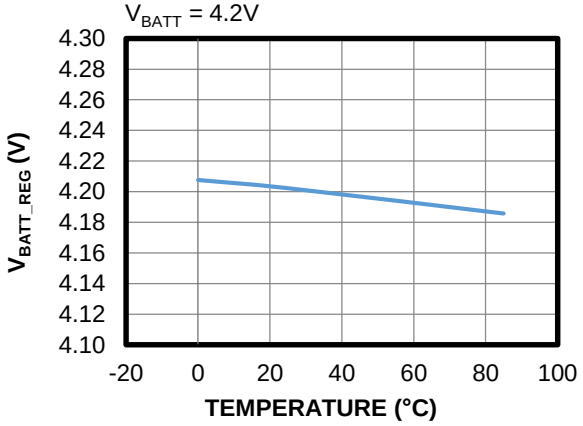
Boost Efficiency

V_{BOOST} = 5.15V, L = 1µH (DCR = 12mΩ)



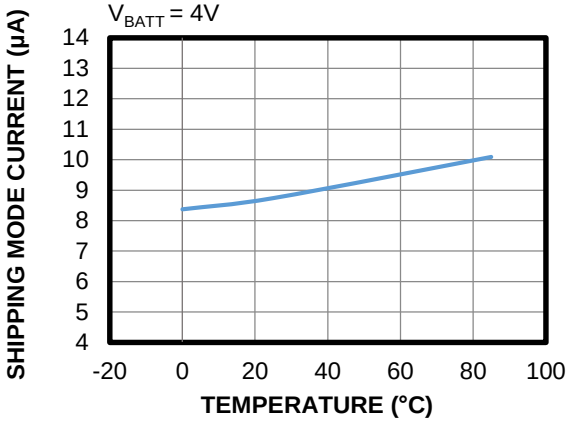
Battery Regulation Voltage vs.Temperature

V_{BATT} = 4.2V



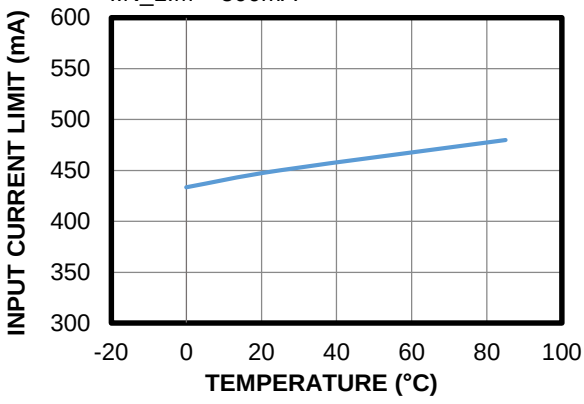
Shipping Mode Current vs. Temperature

V_{BATT} = 4V



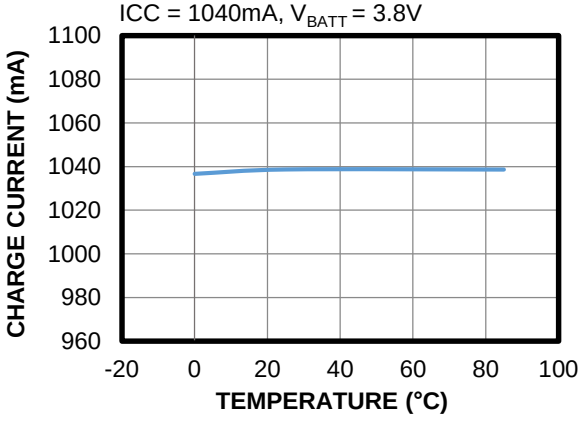
Input Current Limit vs. Temperature

IIN_LIM = 500mA



Charge Current vs. Temperature

ICC = 1040mA, V_{BATT} = 3.8V



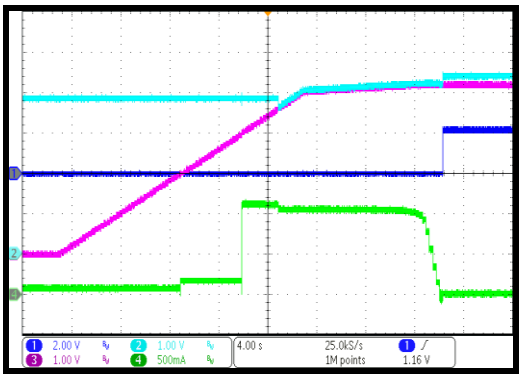
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1040mA, I_{IN_LIM} = 3A, V_{IN_MIN} = 4.36V, L = 1µH (DCR = 12mΩ), T_A = 25°C, unless otherwise noted.

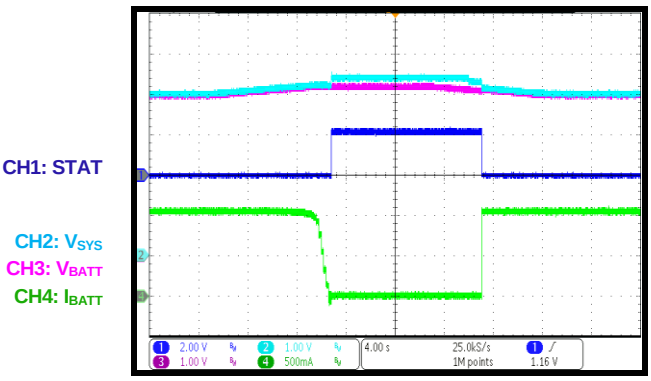
Battery Charge Profile

V_{IN} = 5V, I_{CC} = 1040mA, I_{SYS} = 0A



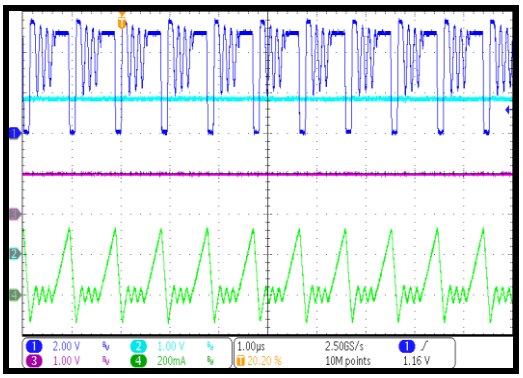
Auto-Recharge

V_{IN} = 5V, I_{CC} = 1040mA, I_{SYS} = 0A



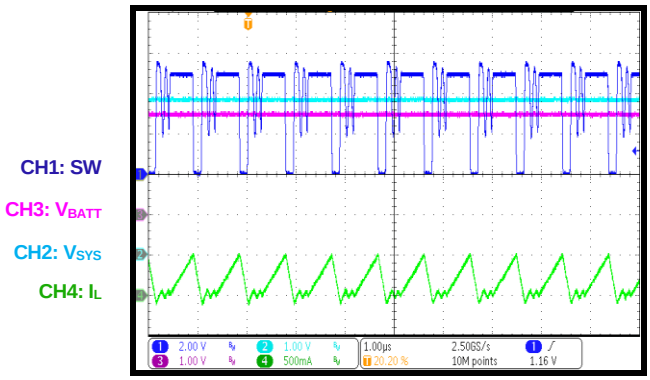
Trickle Charge

V_{IN} = 5V, V_{BATT} = 1V, I_{TRI} = 64mA, I_{SYS} = 0A



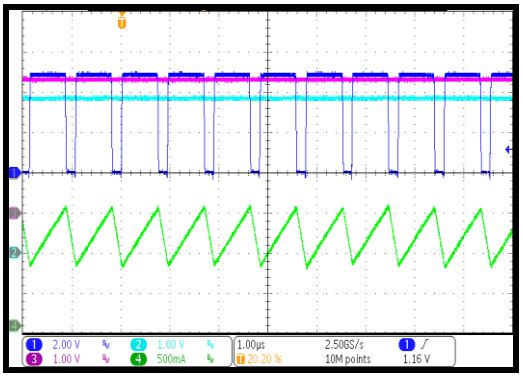
Pre-Charge

V_{IN} = 5V, V_{BATT} = 2.5V, I_{PRE} = 160mA, I_{SYS} = 0A



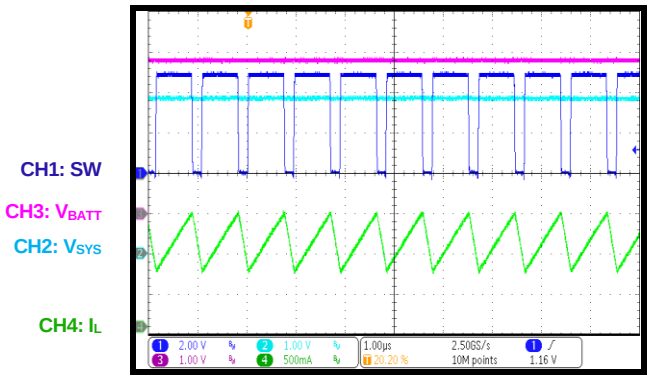
Linear CC Charge

V_{IN} = 5V, V_{BATT} = 3.3V, I_{CC} = 1040mA, I_{SYS} = 0A



Switching CC Charge

V_{IN} = 5V, V_{BATT} = 3.8V, I_{CC} = 1040mA, I_{SYS} = 0A



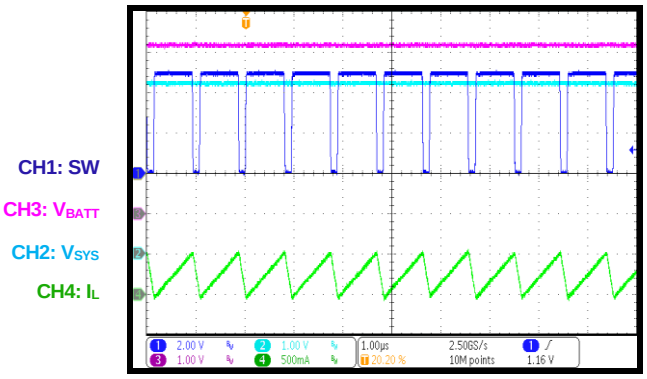
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1040mA, I_{IN_LIM} = 3A, V_{IN_MIN} = 4.36V, L = 1µH (DCR = 12mΩ), T_A = 25°C, unless otherwise noted.

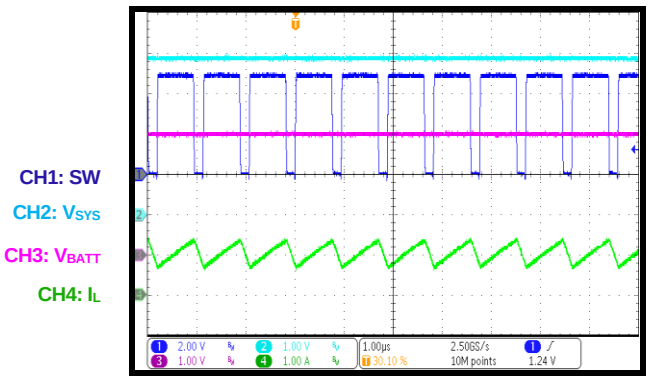
Constant Voltage Charge

V_{IN} = 5V, V_{BATT} = 4.185V, I_{SYS} = 0A



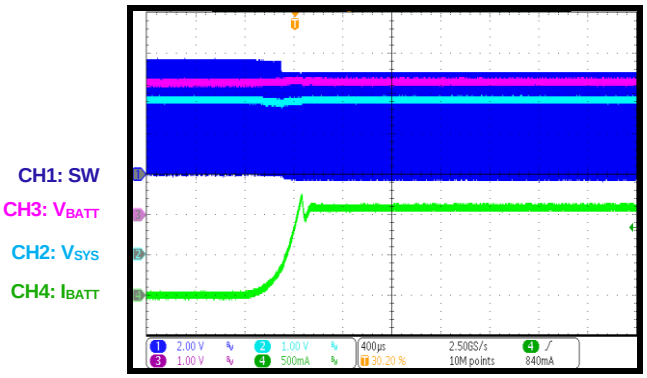
Charge Disabled Steady State

V_{IN} = 5V, V_{BATT} = 3V, I_{SYS} = 1A



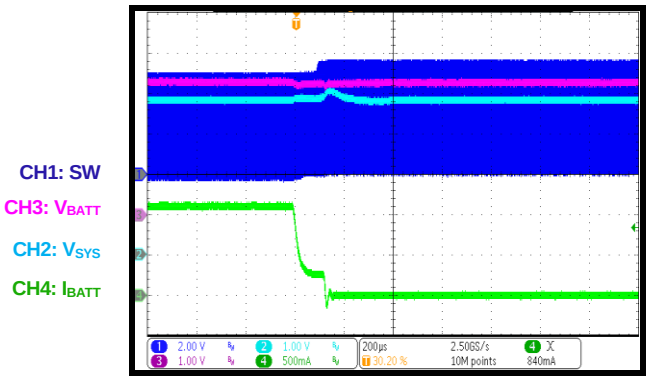
Charging Enabled

V_{IN} = 5V, V_{BATT} = 3.3V, I_{CC} = 1040mA, I_{SYS} = 0A



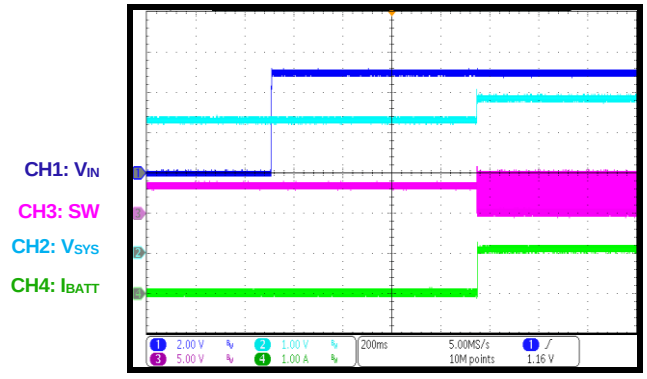
Charging Disabled

V_{IN} = 5V, V_{BATT} = 3.3V, I_{CC} = 1040mA, I_{SYS} = 0A



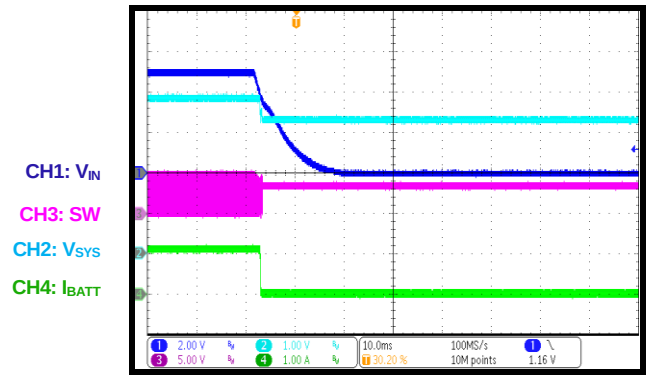
Start-Up

V_{IN} = 5V, V_{BATT} = 3.3V, I_{CC} = 1040mA, I_{SYS} = 0A



Shutdown

V_{IN} = 5V, V_{BATT} = 3.3V, I_{CC} = 1040mA, I_{SYS} = 0A



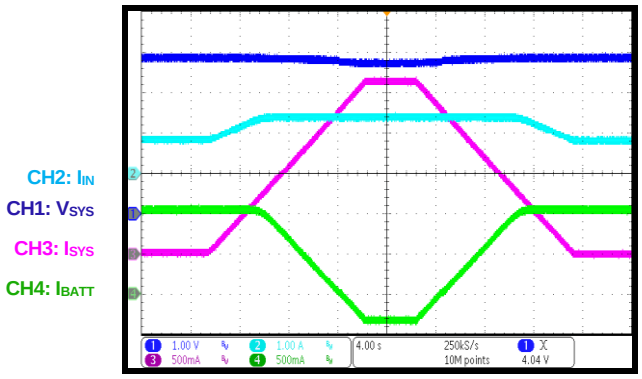
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1040mA, I_{IN_LIM} = 3A, V_{IN_MIN} = 4.36V, L = 1µH (DCR = 12mΩ), T_A = 25°C, unless otherwise noted.

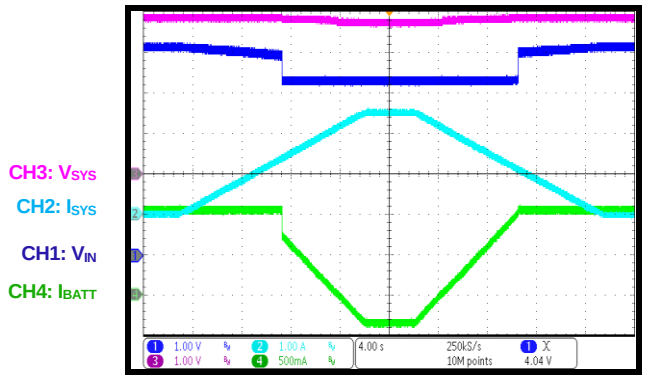
Input Current Limit

V_{IN} = 5V, I_{IN_LIM} = 1500mA, V_{BATT} = 3.8V, I_{CC} = 1040mA



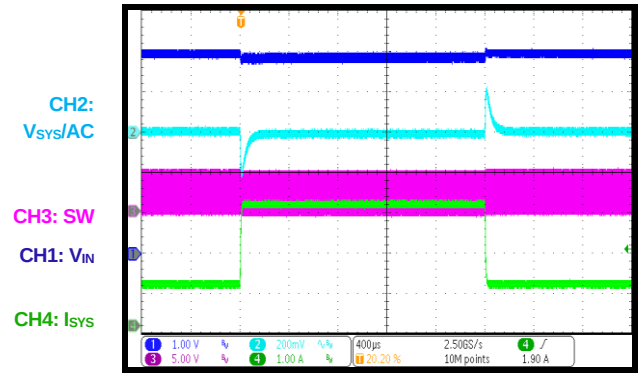
Input Voltage Limit

V_{IN} = 5V (2A), I_{IN_LIM} = 3000mA, V_{BATT} = 3.8V, I_{CC} = 1040mA



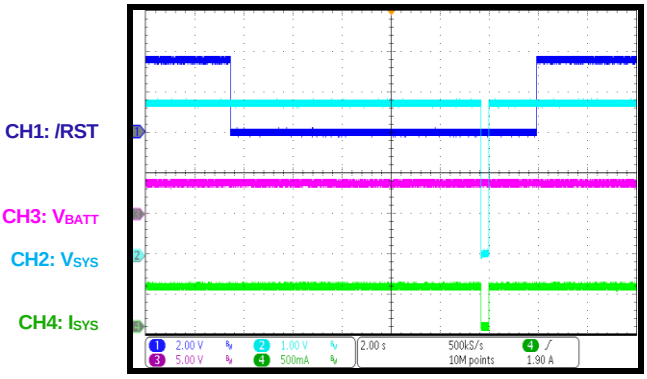
SYS Load Transient

V_{IN} = 5V, V_{BATT} = 3.3V, charge disabled, I_{SYS} = 1A to 3A



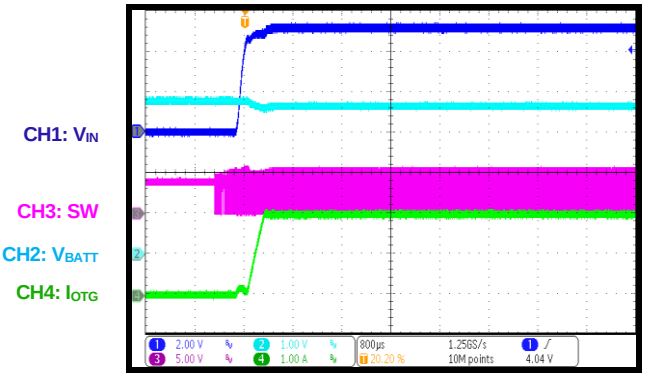
BATTFET Reset

V_{BATT} = 3.8V, I_{SYS} = 0.5A



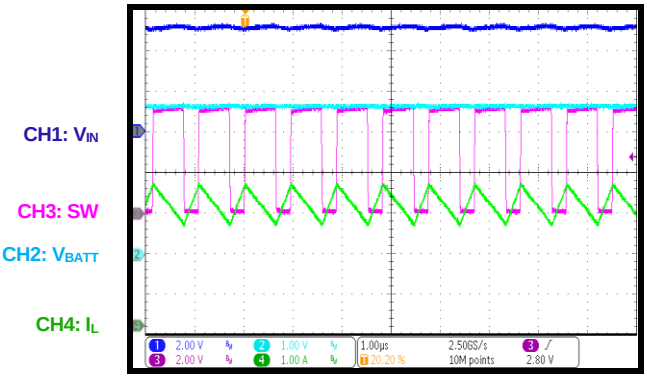
OTG Mode On

V_{BATT} = 3.8V, V_{BOOST} = 5.15V, I_{OTG} = 2A



OTG Steady State Operation

V_{BATT} = 3.8V, V_{BOOST} = 5.15V, I_{OTG} = 2A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

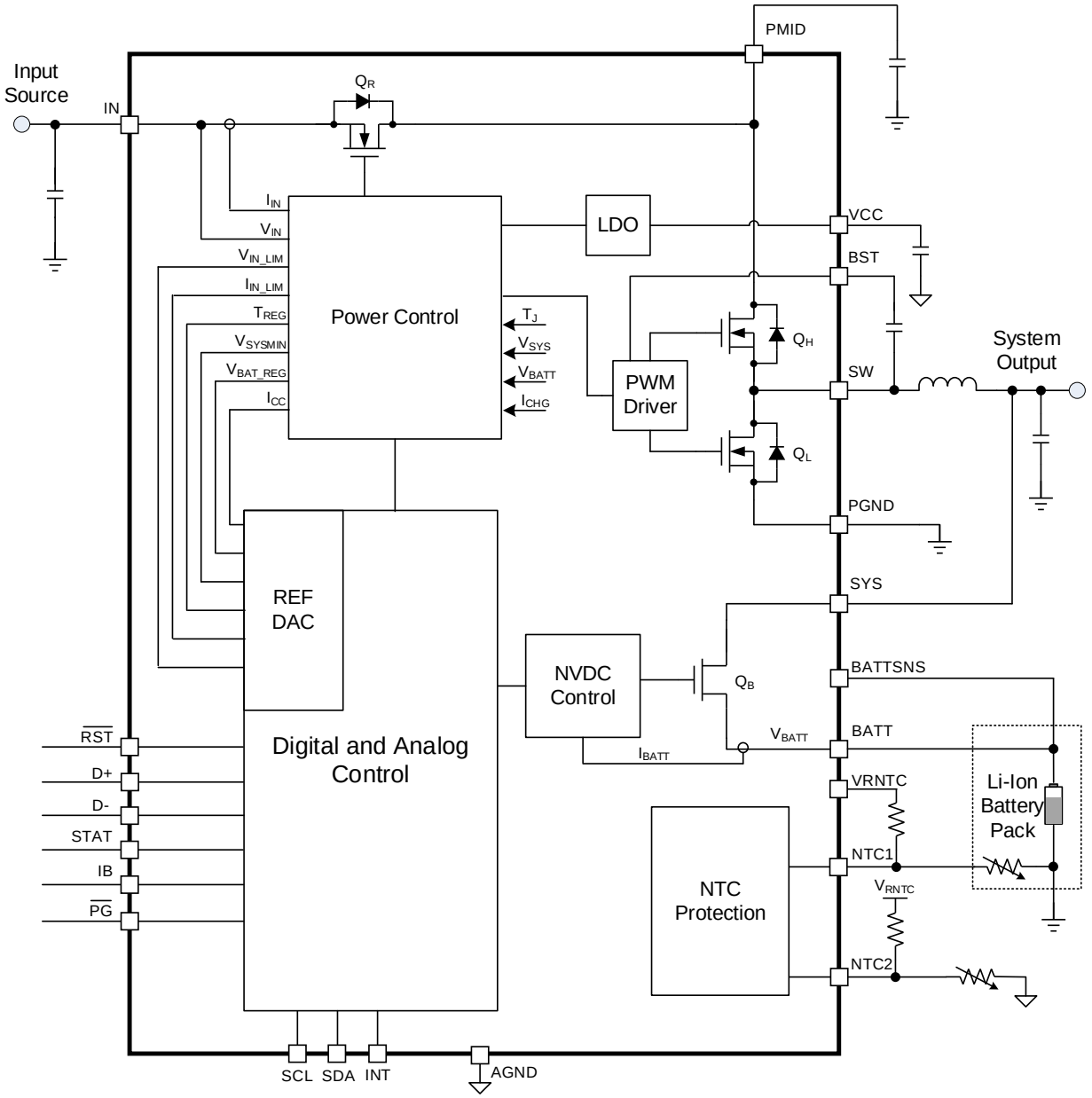


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

OPERATION

The MP2720 is a highly integrated, I²C-controlled, switch-mode battery charger IC with narrow-voltage DC (NVDC) power path management for the single-cell lithium-ion or lithium-polymer battery applications. The MP2720 integrates the reverse blocking MOSFET (RB-FET, Q_R), high-side switching MOSFET (HS-FET, Q_H), low-side switching MOSFET (LS-FET, Q_L), and battery MOSFET (BATTFET, Q_B).

VCC Regulator

The VCC regulator is powered from the higher voltage between the BATT and PMID pins. The VCC pin requires an external 4.7µF bypass capacitor. The VCC pin provides power for the internal circuits and the gate drivers. When the VCC pin voltage (V_{CC}) exceeds the VCC under-voltage lockout (UVLO) threshold (V_{VCC_UV}), the I²C interface is ready for communication, and all of the registers are reset to their default values. The VCC pin can be used for external logic pull-up, but is not recommended for excess loads.

Battery Power-On

If an input source is not available, the battery is connected, and the battery voltage (V_{BATT}) exceeds the BATT UVLO threshold (V_{BATT_UV}), the BATTFET turns on and powers up the system. The low quiescent current and low voltage drop on BATTFET minimize battery consumption and maximize the battery runtime. The BATTFET's discharge current is monitored. If the system is overloaded or shorted to ground ($I_{BATT} > I_{BATT_OCP}$), the device turns off BATTFET immediately and sets the BATTFET_DIS bit to 1. The BATTFET can be re-enabled following the methods described in the Exit Shipping Mode section on page 20.

Input Power-On

When an input source is plugged in, the IC detects the input source type and sets the input current limit (I_{IN_LIM}) before the buck converter starts. The start-up sequence from the input source is described in detail below:

1. The input voltage (V_{IN}) is detected.
2. The hold-off timer (about 250ms) runs.
3. Input source type detection starts.
4. I_{IN_LIM} is set.
5. If EN_BUCK = 1, the buck converter starts.
6. If EN_CHG = 1, charging starts.

Hold-Off Timer

When a valid input source is detected, the IC runs a hold-off timer (t_{HOLD}, typically about 250ms) before detecting the input source type. t_{HOLD} can be bypassed by setting the HOLDOFF_TMR bit to 0.

Input Source Type Detection

The IC runs D+/D- detection when all of the following conditions are met:

- V_{IN} exceeds V_{IN_UV}
- V_{IN} is below V_{IN_OV}
- VIN_GD = 1
- t_{HOLD} ends
- AUTODPDM = 1, or FORCEDPDM is set

D+/D- detection includes USB Battery Charging Specification 1.2 (BC1.2) and non-standard adapter detection. BC1.2 detection begins with data contact detection (DCD). If DCD is successful, the standard downstream port (SDP), dedicated charging port (DCP), and charging downstream port (CDP) are distinguished by primary and secondary detection. If the DCD timer expires, then non-standard adapter detection is initiated. Table 1 lists the criteria for non-standard adapter detection.

Table 1: Non-Standard Adapter Detection

Adapter Type	D+ Voltage (V_{D+})	D- Voltage (V_{D-})
Divider 1	V_{D+} within V_{2P0_TH}	V_{D-} within V_{2P7_TH}
Divider 2	V_{D+} within V_{2P7_TH}	V_{D-} within V_{2P0_TH}
Divider 3	V_{D+} within V_{2P7_TH}	V_{D-} within V_{2P7_TH}
Divider 4	V_{D+} within V_{1P2_TH}	V_{D-} within V_{1P2_TH}
Divider 5	V_{D+} within V_{2P7_TH}	$V_{D-} > V_{2P7_TH}$

If AUTODPDM = 0, then D+/D- detection is bypassed and the DPDM_STAT bits remain set to 0000.

Table 2 on page 17 lists the I_{IN_LIM} settings from D+/D- detection.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Table 2: Input Current Limit Setting by D+/D- Detection

D+/D- Detection	Input Current Limit
Not started	500mA
USB SDP	500mA
USB DCP	2A
USB CDP	1.5A
Divider 1	1A
Divider 2	2.1A
Divider 3	2.4A
Divider 4	2A
Divider 5	3A
Unknown	500mA

Input Current Limit (I_{IN_LIM}) Setting

After input source type detection finishes, the following actions are executed:

- The DPDM_STAT bits are updated
- I_{IN_LIM} is updated
- The VIN_RDY bit is set to 1

When the VIN_RDY bit is set, an INT pulse asserts and I_{IN_LIM} is updated. The host can overwrite the IIN_LIM registers to modify I_{IN_LIM}.

If the FORCEDPDM bit is written to 1, then D+/D- detection restarts. After D+/D- detection finishes, the DPDM_STAT bits and I_{IN_LIM} update. An INT pulse follows this action.

Input Voltage Limit (V_{IN_LIM}) Setting

The MP2720 supports a configurable input voltage limit (V_{IN_LIM}). If V_{IN} drops to V_{IN_LIM} due to the input source capability or a cable voltage drop, then the duty cycle is limited to prevent V_{IN} from dropping further. This reduces the converter's total output current.

If the EN_VIN_TRK bit is set to 0, then the absolute V_{IN_LIM} is set by the VIN_LIM register. If the EN_VIN_TRK bit is set to 1, then V_{IN_LIM} is the maximum value between the VIN_LIM register's setting and (V_{BATT} + 165mV).

Buck Converter and Charger Start-Up

After the VIN_RDY bit is set to 1, the buck converter soft starts if EN_BUCK = 1. The buck converter's switching frequency (f_{SW}) can be set between 750kHz and 1.5MHz.

Peak current control mode is adopted to regulate the system voltage (V_{SYS}), battery charge current, battery regulation voltage (V_{BATT_REG}), I_{IN_LIM}, V_{IN_LIM}, and the device die temperature loops.

If the EN_CHG bit is set to 1, the device automatically starts charging.

NVDC Battery MOSFET (BATTFET)

Using the NVDC structure, the BATTFET separates the system from the battery and controls the battery charging and discharging. With power path management, the device prioritizes the system (SYS) output by utilizing the input source, battery, or both.

When the input source is absent, the BATTFET turns fully on to pass the battery power to the system via the ultra-low impedance path. When the input source is present and the buck converter has started up, the system output is related to V_{BATT} in the following ways:

1. When V_{BATT} is below the minimum system voltage setting (V_{SYS_MIN}), V_{SYS} is regulated to (V_{SYS_MIN} + V_{TRACK}), where V_{TRACK} is typically 150mV. Depending on V_{BATT}, the BATTFET works in linear mode to charge the battery with a trickle-charge, pre-charge, or fast charge current.
2. Once V_{BATT} exceeds V_{SYS_MIN}, the BATTFET turns on fully and the voltage difference between V_{SYS} and V_{BATT} is the BATTFET resistive voltage drop.
3. When charging is disabled or terminated, V_{SYS} is always regulated to V_{TRACK} plus the higher value between V_{SYS_MIN} and V_{BATT}. In this scenario, V_{TRACK} is typically 100mV.

The status register VSYS_STAT indicates whether the system is in V_{SYS_MIN} regulation.

Figure 3 on page 18 shows V_{SYS} regulation as V_{BATT} changes.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

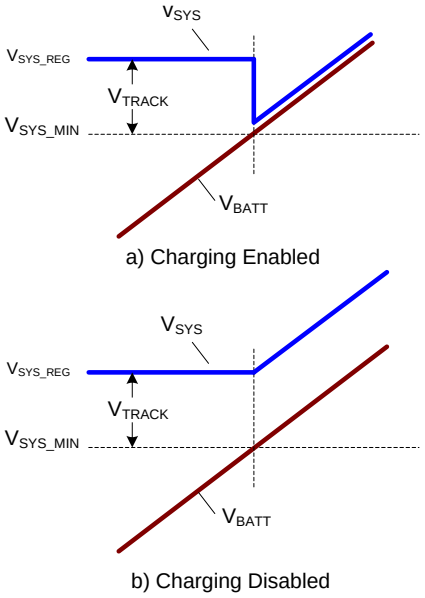


Figure 3: V_{SYS} Regulation with V_{BATT}

Dynamic Power Management

During buck converter operation, the MP2720 continuously monitors the input current (I_{IN}) and V_{IN}. When the input current limit or input voltage limit is reached, the charge current is reduced to prevent the input source from being overloaded.

If the charge current drops to zero, V_{SYS} starts to drop due to the input power limitation. Once V_{SYS} falls below V_{BATT}, the IC automatically enters supplement mode.

If the converter operates in the input current loop or input voltage limit loop, the IINDPM_STAT or VINDPM_STAT bit is set to 1, respectively. This is followed by a maskable INT pulse.

Supplement Mode

When V_{SYS} falls below V_{BATT}, the BATTFET turns on to prevent V_{SYS} from dropping further. In this scenario, the buck converter and the battery work together to provide power for the system.

Battery Charging

The MP2720 can autonomously run a charging cycle without host involvement. The host can also control the charging operations and parameters via the registers.

A new charge cycle starts when all of the below conditions are met:

- The buck converter has started up
- The NTC pin's (NTC1 and NTC2) voltages are within the acceptable ranges
- BATTFET is on (BATTFET_DIS = 0)
- Charging is enabled (EN_CHG = 1)

Charging Profile

The MP2720 detects V_{BATT} to provide four main charging phases: trickle-charge, pre-charge, constant-current charge and constant-voltage charge (see Table 3).

Table 3: Charge Current Setting

Battery Voltage (V_{BATT})	Charge Current	Default Value	CHG_ STAT
$V_{BATT} < V_{BATT_TC}$	$I_{TRICKLE}$	64mA	001
$V_{BATT_TC} \le V_{BATT} < V_{BATT_PRE}$	I_{PRE}	160mA	010
$V_{BATT_PRE} \le V_{BATT} < V_{BATT_REG}$	I_{CC}	1040mA	011
$V_{BATT} = V_{BATT_REG}$	$< I_{CC}$	-	100

Throughout the charging process, the actual charge current may be below the register setting due to other regulation loops, such as the input current loop, input voltage loop, or thermal regulation. In this scenario, charge termination is blocked and the charge timer counts at half of its usual speed if EN_TMR2X = 1. Figure 4 shows the battery charge profile.

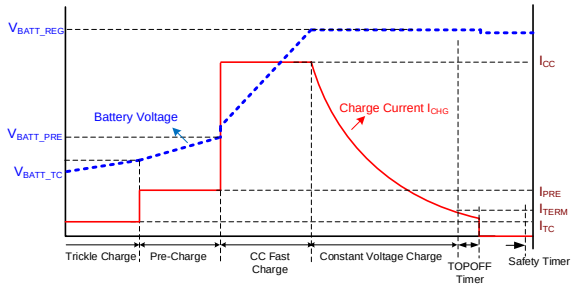


Figure 4: Battery Charging Profile

Charge Termination

If all the following conditions are met, charging is terminated:

- Termination is enabled (EN_TERM = 1)
- The charge current is below the termination threshold for t_{TEC_DGL} (about 250ms)
- The device is charging in the constant-voltage phase

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

- The device is not in an input current or input voltage loop
- The device is not in thermal regulation

After termination, the status register CHG_STAT is set to 101, the STAT pin indicator goes high, and an INT pulse is generated.

To restart a new charge cycle once charging terminates, re-plug in the input source or toggle the EN_CHG bit.

To fully charge the battery, a top-off timer can be applied after termination is detected. The TOPOFF_TIMER bits set the top-off timer. The TOPOFF_ACTIVE bit is 1 when the top-off timer is active. A maskable INT pulse is generated when entering and exiting the top-off time. During top-off timer operation, charging continues, while the CHG_STAT bits and the STAT pin both indicate that charging is done.

The top-off timer can be reset by any of the conditions listed below:

- Charging changes from disabled to enabled
- Recharging begins
- The REG_RST bit is set

Automatic Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged due to system supplement mode or self-discharge. When V_{BATT} discharges to the recharge threshold, the MP2720 automatically starts a new charging cycle without requiring a manual charge cycle restart, as long as the input power is valid. There is a deglitch timer (t_{RECH_DGL}, about 100ms) to detect whether V_{BATT} is below the recharge threshold. An INT pulse asserts when automatic recharging starts.

JEITA Thermistor Qualification

The device supports the JEITA profile to manage the charging parameters by continuously monitoring the NTC1 and NTC2 pin voltages. Two independent negative temperature coefficient (NTC) thermistors with temperature sensing and flexible configurations are provided. The NTC1 and NTC2 pins can be enabled and disabled by setting the NTC1_ACTION and NTC2_ACTION bits, respectively.

The EN_PG_NTC2 bit should be set to 1 to enable the NTC2 channel. When the EN_PG_NTC2 bit is set to 0, there is only one NTC monitor.

If the corresponding NTC channel is enabled, the voltage on the NTC pin must be within the V_{HOT} to V_{COLD} range to initiate a charge cycle. If the NTC pin voltage is outside the V_{HOT} to V_{COLD} range, then the MP2720 suspends charging and waits for the NTC voltage to return to the standard range.

In the cool temperature range (V_{COLD} to V_{COOL}), the charge current and/or charge voltage are reduced according to the COOL_ACT, JEITA_ISET, and JEITA_VSET settings.

In the warm temperature range (V_{WARM} to V_{HOT}), the charge voltage and/or charge current are reduced according to the WARM_ACT, JEITA_ISET, and JEITA_VSET settings.

The V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds all have four configurable percentage levels.

The temperature conditions can be read in NTC1_FAULT and/or NTC2_FAULT bits. An INT pulse is generated when the NTC1 or NTC2 condition changes.

The NTC1 pin and NTC2 pin share the same configurable thresholds. Table 4 shows the detection priority when the detection results between the two NTC inputs are different.

Table 4: JEITA Detection Priority

NTC2 \ NTC1	Hot	Warm	Normal	Cool	Cold
Hot	Hot	Hot	Hot	Hot	Hot
Warm	Hot	Warm	Warm	Warm	Cold
Normal	Hot	Warm	Normal	Cool	Cold
Cool	Hot	Warm	Cool	Cool	Cold
Cold	Hot	Cold	Cold	Cold	Cold

For battery temperature protection during boost mode, if the NTC1_ACTION or NTC2_ACTION bit is set to 1, the device compares the NTC1 and/or NTC2 pin voltage with the V_{COLD} and V_{HOT} thresholds. If the NTC pin voltage is outside the V_{COLD} to V_{HOT} range, then boost mode is suspended. The NTC1_FAULT or NTC2_FAULT bit is also set to report the condition.

The preset hot, cold, warm, and cool voltage thresholds are defined for a β = 3435 thermistor.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

It is recommended to use a pull-up resistor with a value that matches the thermistor's resistance at 25°C.

Figure 5 shows the JEITA voltage/current regulations with the following set-up: NTC1_ACTION = 1, NTC2_ACTION = 0, WARM_ACT = 01, COOL_ACT = 10, JEITA_VSET = 00, and JEITA_ISET = 00.

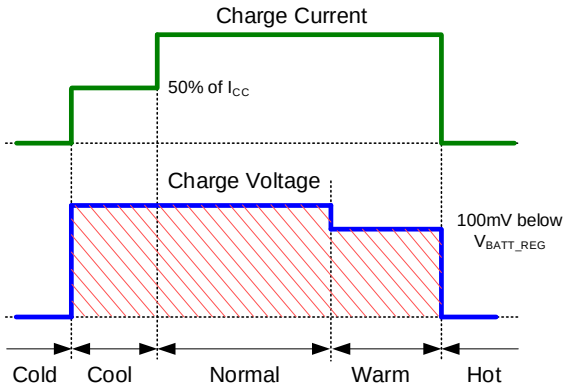


Figure 5: NTC Window under JEITA Control

Charging Safety Timer

The device has a built-in safety timer to prevent an extended charging cycle due to abnormal battery conditions. When V_{BATT} is below the V_{BATT_PRE} threshold, the safety timer is fixed to 2 hours. When V_{BATT} exceeds the V_{BATT_PRE} threshold, the safety timer is configured by the CHG_TIMER bits. When the CHG_TIMER bits are set to 00, both the pre-charge timer and the fast-charge timer are disabled.

Charging is disabled after the safety timer expires. Then the fault register's CHG_FAULT bit is set to 10, and an INT pulse is generated.

During an input current, input voltage, thermal regulation, or JEITA cool/warm conditions (when charge current reduction is enabled), the charge timer counts at half of its usual rate. This halved clock rate function can be disabled by setting the EN_TMR2X bit to 0.

The charging safety timer resets if any of the following conditions are met:

- The input source is unplugged
- EN_BUCK or EN_CHG is toggled
- The REG_RST bit is set

Remote Battery Voltage Sense

To minimize the parasitic trace resistance during charging, the BATTSNS pin can be connected to the actual battery pack's positive terminal. Remote sensing of the battery voltage accelerates the charging speed by helping the charger stay in constant-current charge mode for longer.

Shipping Mode

Entering Shipping Mode

When the host sets the BATTFET_DIS bit to 1, the MP2720 turns off the BATTFET immediately or after a set delay time (t_{SHIP_DLY}), configured by the BATTFET_DLY bit.

Exiting Shipping Mode

When the MP2720 is in shipping mode (BATTFET_DIS = 1), either of the below events can wake up the BATTFET:

- An input source is applied
- The $\overline{RST}$ pin pulls low for $t_{SHIPMODE}$

BATTFET Reset

When the input source is absent, the system is powered by the battery through the BATTFET. The system can be forced to have a hardware power-on reset (POR) by changing the BATTFET status from on to off, then back to on.

For this function, the $\overline{RST}$ pin can be connected to the device's push-button. The $\overline{RST}$ pin is pulled up internally.

If the $\overline{RST}$ pin is driven low for t_{RST} while the input source is not plugged in and BATTFET_DIS = 0, the BATTFET turns off for t_{SYS_RST}, then it is enabled again (see Figure 6).

This function can be disabled by setting the BATTFET_RST_EN bit to 0.

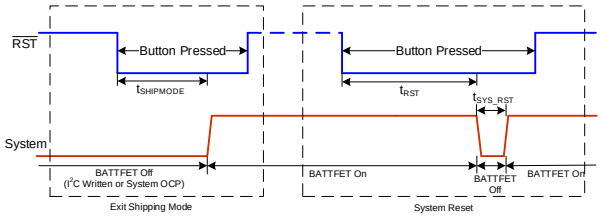


Figure 6: $\overline{RST}$ Timing

Power Good (PG) Indication

When EN_PG_NTC2 is set to 0, the PG/NTC2 pin acts as the power good (PG) indicator.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

This pin goes low to indicate a good input source when all of the following conditions are met:

- V_{IN} exceeds V_{IN_UV}
- V_{IN} is below V_{IN_OV}
- The 15ms debounce timer has passed

STAT and IB Indication

When the EN_STAT_IB bit is set to 0, the charging status is indicated on the open-drain STAT/IB pin (see Table 5).

Table 5: STAT Indication

Charging State	STAT
Charging	Low
Charging is complete, top-off timer, boost mode, charging is disabled	High
Charging is suspended (due to battery OVP, input OVP, timer fault, or an NTC fault), boost mode is suspended (due to an NTC fault, OTP, or BATT_LOW)	Blinks at 1Hz

When EN_STAT_IB is set to 1, the STAT/IB pin acts as an analog current source output that indicates the value of the battery current flowing into or out of the battery. The current's direction can be read via the BFET_STAT bit. Connect a resistor load between the STAT/IB pin and AGND to sense the IB current. If IB_EN is set to 1, the IB output is always on. If IB_EN is set to 0, the IB output is only on when the device is switching.

The IB output voltage ranges between 0V and V_{CC}. The host can measure the IB voltage to make a software fuel gauge or monitor the peak discharge current.

Interrupts (INT)

A 256µs interrupt pulse is generated on the open-drain INT pin if any of the interrupt events occur. See the Interrupt List section on page 36 for more details.

Watchdog Functions (Bark and Bite)

After the first battery or V_{IN} start-up, the MP2720 operates with the default set-up. The watchdog timer is expired by default when WATCHDOG_FAULT = 1. Writing 1 to WATCHDOG_RST starts the watchdog timer.

The watchdog timer has a bark function that generates an INT pulse when the watchdog timer is 3/4 of the way through its timer. The host can distinguish this condition by reading the WATCHDOG_BARK bit.

To maintain custom settings after the watchdog timer starts, write 1 to the WATCHDOG_RST bit before the watchdog timer expires. If the watchdog timer expires, the registers are reset according to the register table. After the watchdog timer expires, an INT pulse is sent and the WATCHDOG_FAULT bit is set to 1.

The watchdog timer can be disabled by setting the WATCHDOG bit to 00. If the watchdog timer is disabled, the registers keep their values until a POR.

Boost Mode

By boosting from the battery, the MP2720 can supply a regulated output at the IN pin. Boost mode starts once all of the following conditions are met:

- V_{IN} is below V_{IN_UV}
- The EN_BOOST bit is set to 1
- The voltages on the NTC pins (NTC1 and NTC2) are within the acceptable range
- V_{BATT} exceeds V_{BATT_UV}
- If BOOST_STP = 1, V_{BATT} must exceed V_{BATT_LOW}

The boost PWM's switching frequency is the same as the buck converter's setting.

The boost voltage loop regulates the PMID pin voltage at the value set by the VBOOST bits.

The boost output current loop limits the output current at the value set by OLIM bits for the $V_{IN} > V_{BATT} + V_{HDRM}$ range.

The boost mode start-up sequence follows the steps below:

1. The converter soft starts and regulates the PMID voltage.
2. The blocking FET (Q_R) soft starts and regulates the discharge current from PMID to IN.
3. Once the IN pin starts up successfully, the boost is controlled to regulate the PMID voltage and the output current sensed through Q_R.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

The boost converter's soft-start function allows the device to power into large capacitive loads on the IN pin.

Forced Input Current Limit

When an input source is plugged in during sink mode, the MP2720 runs the start-up sequence and initiates input source type detection. After detection finishes, I_{IN_LIM} is automatically generated. The I_{IN_LIM} result is returned by the IIN_LIM bits.

If the host does not want to use the automatically generated I_{IN_LIM}, there are two ways to set I_{IN_LIM} to different values via configuring either the IIN_MODE or IIN_LIM bits.

If the IIN_MODE bits are set to 000, the MP2720 runs with the automatically generated I_{IN_LIM} (returned by the IIN_LIM bits). However, once the VIN_RDY bit is set, the host can override the IIN_LIM bits to set I_{IN_LIM} to any value. This requires host involvement every time the converter starts up.

If the IIN_MODE bits are set to other values, I_{IN_LIM} is forced and fixed. For example, if the IIN_MODE bits are set to 101, the device always runs with a fixed 2000mA I_{IN_LIM}, ignoring the input source type detection.

Input Impedance Test

The MP2720 supports an input impedance testing function. By sourcing a current on the IN pin, the device can detect the impedance on the connecter receptacle (water detection).

The host can write 1 to the VIN_SRC_EN bit to turn on the input impedance test by sourcing a current to the IN pin. The testing current can be configured via the IVIN_SRC bits. If V_{IN} rises to the threshold configured via the VIN_TEST bit, then VIN_TEST_HIGH is set to 1 and latched. This is followed by an INT pulse.

The host can write 0 to the VIN_SRC_EN bit to turn off the test current source and clear the VIN_TEST_HIGH bit.

The VIN_SRC_EN bit can only be effective when neither the buck nor boost is operating, and the current source's maximum pull-up voltage is 2.5V. If $V_{IN} > V_{IN_UV}$ is detected during the test, then the VIN_SRC_EN and VIN_TEST_HIGH bits are reset to 0 and the test ends immediately. If boost mode is enabled during the test, then the VIN_SRC_EN and VIN_TEST_HIGH bits are reset to 0 and the test ends immediately.

Lock Function

The MP2720 supports a lock function that limits the value of some key parameters (prevents accidental I²C writing). The battery regulation voltage, constant-current charge current, pre-charge current, and JEITA voltage/current settings are some of these parameters.

To enable the lock function, the host can set the above parameters to a target value, then write the LOCK_CHG bit to 1. After these operations, these parameters can only be rewritten when their values are being decreased.

Any of the following events can unlock the parameters:

- The host writes the LOCK_CHG bit to 0
- The host writes the REG_RST bit to 0
- The device shuts down

Protections

Battery Under-Voltage Protection (UVP)

If the battery is discharged below V_{BATT_UV} when the input source is absent, then the BATTFET turns off and all registers reset.

BATTFET Over-Current Protection (OCP)

The MP2720 monitors the BATTFET's current. If SYS is overloaded or experiences a short and the battery discharge current reaches the I_{BATT_OCP} threshold, then the BATTFET turns off and latches. In addition, the BATTFET_DIS bit is set to 1. To release the latch, apply one of the methods described in the Exiting Shipping Mode section on page 20.

Input Over-Voltage Protection (OVP)

The MP2720 provides input over-voltage protection (OVP) with a rising threshold of 6.3V. If the IN pin senses a voltage above the V_{IN_OV} threshold, the buck converter stops working, the CHG_FAULT bits are set to 01, and an INT pulse is generated.

When V_{IN} returns to the normal range, the device runs the start-up sequence again and resumes normal operation. The CHG_FAULT bits are also cleared.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Battery Over-Voltage Protection (OVP)

The battery OVP threshold is 104% of V_{BATT_REG}. If a battery OV condition is detected, charging is disabled. Meanwhile, the fault register's CHG_FAULT bits are set to 11, and an INT pulse asserts.

Thermal Regulation and Thermal Shutdown

If the internal junction temperature reaches to the thermal regulation limit (T_{J_REG}) configured via the TREG bits (60°C to 120°C) during battery charging, then the charge current is reduced, charge termination is blocked, and the charge timer runs at half rate. The status register's THERM_STAT bit is set to 1, followed by a maskable INT pulse.

If the internal junction temperature rises to the shutdown threshold (T_{J_SHDN}, about 150°C) at any time, both the converter and BATTFET turn off and all registers are reset. Once the junction temperature returns to T_{SHDN_HYS} (about 30°C) below T_{J_SHDN} (150°C), the MP2720 starts up again and resumes normal operation.

Boost Over-Voltage Protection (OVP)

If V_{IN} exceeds the regulation target and V_{BST_OVP} during boost operation, the device stops switching immediately. The BOOST_FAULT bits are set to 010, and an INT pulse is generated. Boost operation recovers once V_{IN} returns to its normal range.

Boost Overload Protection

If V_{IN} drops below the (V_{BATT} + V_{HDRM}) or V_{IN_UV} threshold due to a heavy load or short during boost operation, the blocking FET turns off and restarts after 500ms. If a total of 8 restarts are not successful, the boost converter stops and latches off. Then the BOOST_FAULT bits are set to 001 and an INT pulse is generated.

If the IN pin is shorted to GND before the boost converter starts, the blocking FET also restarts 8 times. If this is not successful, the boost converter stops and latches off.

Set the EN_BOOST bit to 0 to clear the BOOST_FAULT bits.

Boost Battery Low Protection

The MP2720 can protect the battery from being over-drained and prevent a system shutdown during boost operation. If the BOOST_STP_EN bit is set to 1 and V_{BATT} falls below the BATT_LOW setting, boost operation automatically turns off and the MP2720 latches. The BOOST_FAULT bits are set to 100 and generate a maskable INT pulse. The BATTFET continues operating to provide power to SYS.

The battery low comparator has a 10ms de-bounce time. Change the EN_BOOST bit to 0 to clear the BOOST_FAULT bits.

Boost Over-Temperature Protection

The MP2720 provides protection from over-temperature conditions in boost mode. If the BOOST_OTP_EN bit is set to 1 and the internal junction temperature rises to the thermal regulation limit (T_{J_REG}, configured via the TREG bits), then boost operation stops and the MP2720 latches. The BOOST_FAULT bits are set to 011, followed by an INT pulse. In this scenario, the BATTFET continues operating to provide power to SYS.

Change the EN_BOOST bit to 0 to clear the BOOST_FAULT bits.

Serial Interface

The MP2720 uses an I²C-compatible interface to flexibly set charging parameters and instantaneously report the device status. The I²C is a two-wire serial interface with two required bus lines: a serial data line (SDA) and a serial clock line (SCL). Both the SDA and SCL lines are open drains that must be connected to the positive supply voltage with a pull-up resistor.

The IC operates as a slave device and receives control inputs from the master device, such as a microcontroller (MCU). The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100kbps) and fast mode (up to 400kbps).

All transactions begin with a start (S) command and are terminated by a stop (P) command. Start and stop commands are always generated by the master. A start command is defined as a high-to-low transition on the SDA line while SCL is high. A stop command is defined as a low-to-high transition on the SDA line when the SCL is high (see Figure 7 on page 24).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

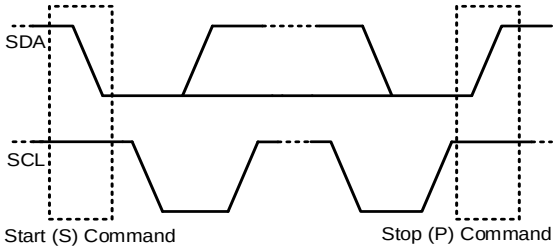


Figure 7: Start and Stop Commands

For data validity, the data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 8). Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

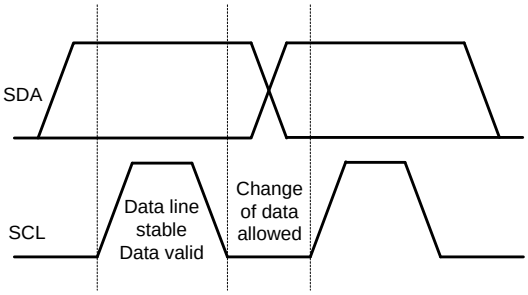


Figure 8: Bit Transfer on the I²C Bus

Each byte must be followed by an acknowledge (ACK) bit. The ACK bit is generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal is defined as when the transmitter releases the SDA line during the acknowledge clock pulse. This allows the receiver to pull the SDA line low, which remains low during the high period of the 9th clock pulse.

If the SDA line is high during the 9th clock pulse, this is considered a not acknowledge (NACK) signal. The master can then generate either a stop command to abort the transfer or a repeated start (Sr) command to start a new transfer.

A slave address is sent after the start command. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 9 shows the address bit arrangement.

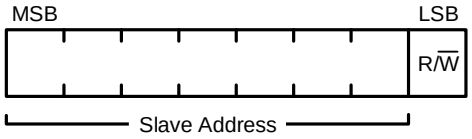


Figure 9: 7-Bit Addressing

Figure 10 shows a data transfer on the I²C bus. Figure 11 shows a single write sequence. Figure 12 on page 25 shows a single read sequence. Figure 13 on page 25 shows a multi-write sequence. Figure 14 on page 25 shows a multi-read sequence.

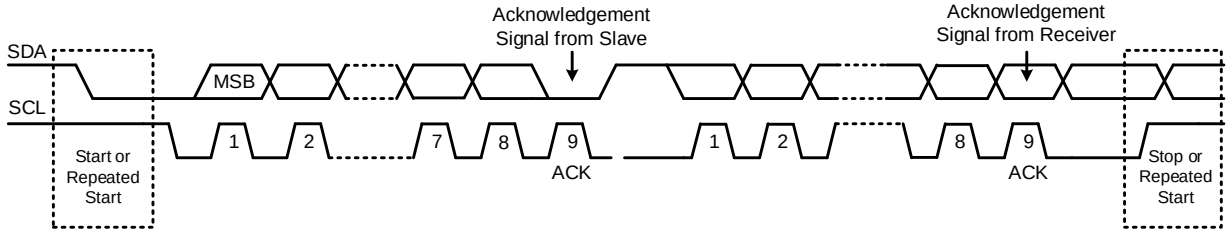


Figure 10: Data Transfer on the I²C Bus

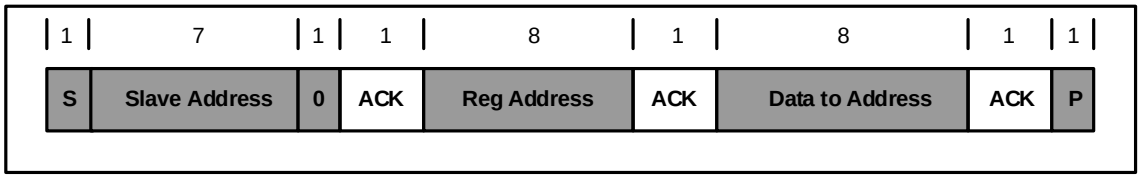


Figure 11: Single Write Sequence

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

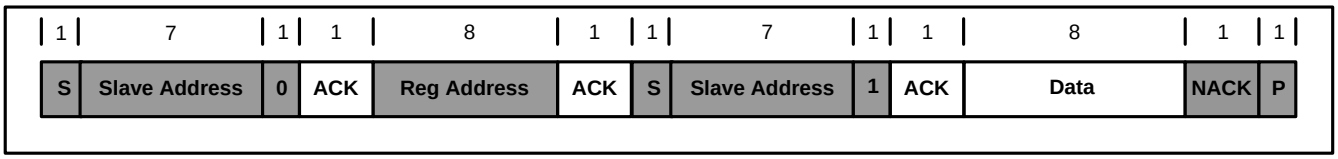


Figure 12: Single Read Sequence

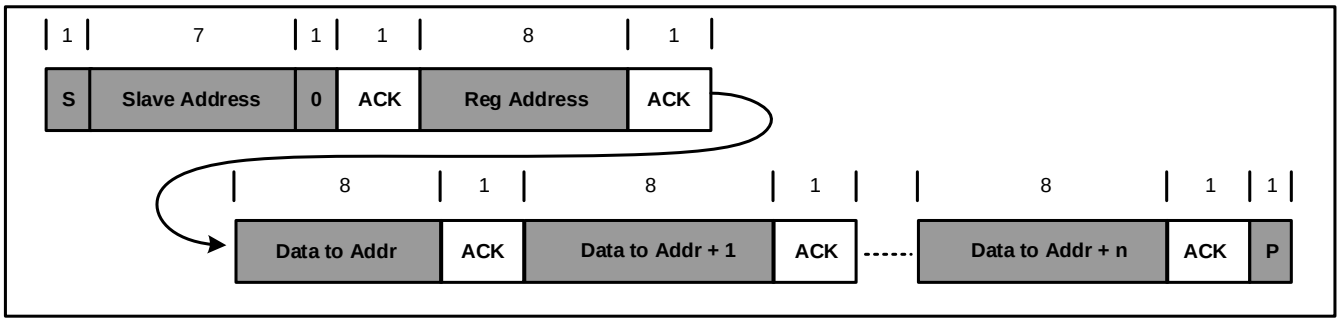


Figure 13: Multi-Write Sequence



Figure 14: Multi-Read Sequence

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REGISTER MAP

I²C Slave Address: 3Fh

Configuration Bytes: 00h~10h

Status Bytes: 11h~16h

CONFIGURATION BYTES (00h~10h)

Legend: POR = default value; WTD = watchdog; R/W = read/write; R = read-only, OTP-configurable = the register's default value can be configured via the OTP

REG00h

Bits	Name	POR	WTD Reset	Type	Description	Comments
7	REG_RST	0	-	R/W	Resets the register. 0: Keep the current setting 1: Reset the registers to their default values	This bit returns to 0 after it is written to 1.
6	EN_STAT_IB	0	No	R/W	0: The STAT/IB pin is configured as an open-drain status indicator (STAT) 1: The STAT/IB pin is configured as a battery current indicator (IB)	OTP-configurable.
5	EN_PG_NTC2	0	No	R/W	0: The PG/NTC2 pin is configured as an open-drain power good indicator (PG) 1: The PG/NTC2 pin is configured as a second thermistor input (NTC2)	To enable the NTC2 channel, this bit must be set to 1. OTP-configurable.
4	LOCK_CHG	0	No	R/W	0: Not locked 1: The VBATT[5:0], ICC[4:0], IPRE[2:0], JEITA_VSET[1:0], and JEITA_ISET[1:0] values are locked	After this bit is set to 1, any future writes to VBATT[4:0], ICC[2:0], IPRE[3:0], JEITA_VSET[1:0], and JEITA_ISET[1:0] can only reduce the set values.
3	HOLDOFF_TMR	1	Yes	R/W	0: Disable the hold-off timer 1: Enable the hold-off timer	OTP-configurable.
2	SW_FREQ[1]	0	No	R/W	00: 750kHz 01: 1MHz 10: 1.25MHz 11: 1.5MHz	Configures both the buck and boost operating frequencies. Default: 1MHz (01) OTP-configurable.
1	SW_FREQ[0]	1	No	R/W		
0	EN_VIN_TRK	1	No	R/W	0: V_{IN_LIM} is fixed 1: V_{IN_LIM} also tracks V_{BATT}	When this bit is set to 0, the VIN_LIM register sets the absolute input voltage limit (V_{IN_LIM}) value. When this bit is set to 1, V_{IN_LIM} is the maximum value between VIN_LIM[3:0] and (V_{BATT} + 165mV).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG01h

Bits	Name	POR	WTD Reset	Type	Description	Comments
7	IIN_MODE[2]	0	No	R/W	000: Follow the IIN_LIM setting 001: Force I_{IN_LIM} to 100mA 010: Force I_{IN_LIM} to 500mA 011: Force I_{IN_LIM} to 900mA 100: Force I_{IN_LIM} to 1500mA 101: Force I_{IN_LIM} to 2000mA 110: Force I_{IN_LIM} to 3000mA	When setting these bits to 000, the input current limit (I_{IN_LIM}) follows the automatically generated I_{IN_LIM} value in IIN_LIM[4:0]. When setting these bits to other values, I_{IN_LIM} is fixed. Default: 000 OTP-configurable.
6	IIN_MODE[1]	0	No	R/W		
5	IIN_MODE[0]	0	No	R/W		
4	IIN_LIM[4]	0	No	R/W	1600mA.	Sets I_{IN_LIM}. Range: 100mA to 3.2A Offset:100mA Default: 500mA (00100) This is automatically updated after input source type detection. The host can overwrite the I_{IN_LIM} value.
3	IIN_LIM[3]	0	No	R/W	800mA.	
2	IIN_LIM[2]	1	No	R/W	400mA.	
1	IIN_LIM[1]	0	No	R/W	200mA.	
0	IIN_LIM[0]	0	No	R/W	100mA.	

REG02h

Bits	Name	POR	WTD Reset	Type	Description	Comments
7	VPRE[1]	1	No	R/W	00: 2.4V 01: 2.6V 10: 2.8V 11: 3V	Sets the pre-charge to fast charge battery voltage threshold. Default: 3V (11)
6	VPRE[0]	1	No	R/W		
5	RESERVED	0	Yes	R	Reserved.	
4	ICC[4]	0	Yes	R/W	1280mA.	Sets the fast charge current. Default: 1040mA (01101) OTP-configurable.
3	ICC[3]	1	Yes	R/W	640mA.	
2	ICC[2]	1	Yes	R/W	320mA.	
1	ICC[1]	0	Yes	R/W	160mA.	
0	ICC[0]	1	Yes	R/W	80mA.	

REG03h

Bits	Name	POR	WTD Reset	Type	Description	Comments
7	RESERVED	0	Yes	R	Reserved.	
6	IPRE[2]	0	Yes	R/W	160mA.	Sets the pre-charge current. Range: 80mA to 360mA Offset: 80mA Default: 160mA (010) OTP-configurable.
5	IPRE[1]	1	Yes	R/W	80mA.	
4	IPRE[0]	0	Yes	R/W	40mA.	
3	ITERM[3]	0	Yes	R/W	240mA.	Sets the termination current. Range: 30mA to 480mA Offset: 30mA Default: 60mA (0001) OTP-configurable.
2	ITERM[2]	0	Yes	R/W	120mA.	
1	ITERM[1]	0	Yes	R/W	60mA.	
0	ITERM[0]	1	Yes	R/W	30mA.	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG04h

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	VRECHG	0	Yes	R/W	0: 100mV 1: 200mV	Sets the recharge threshold. Default: 100mV
6	ITRICKLE[2]	0	Yes	R/W	128mA.	Sets the trickle charge current. Range: 32mA to 256mA Offset: 32mA Default: 64mA (001) OTP-configurable.
5	ITRICKLE[1]	0	Yes	R/W	64mA.	
4	ITRICKLE[0]	1	Yes	R/W	32mA.	
3	VIN_LIM[3]	0	No	R/W	640mV.	Sets the input voltage limit (V_{IN_LIM}) threshold. Range: 3.88V to 5.08V Offset:3.88V Default:4.36V (0110)
2	VIN_LIM[2]	1	No	R/W	320mV.	
1	VIN_LIM[1]	1	No	R/W	160mV.	
0	VIN_LIM[0]	0	No	R/W	80mV.	

REG05h

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	TOPOFF_TMR[1]	0	Yes	R/W	00: Disabled 01: 15 minutes 10: 30 minutes 11: 45 minutes	Sets the timer to stop charging after charge termination.
6	TOPOFF_TMR[0]	0	Yes	R/W		
5	VBATT[5]	0	No	R/W	800mV.	Sets the battery regulation voltage (V_{BATT_REG}). Values above 101000 (4.6V) are clamped to 101000. Range:3.6V to 4.6V Offset: 3.6V Default: 4.2V (011000) OTP-configurable.
4	VBATT[4]	1	No	R/W	400mV.	
3	VBATT[3]	1	No	R/W	200mV.	
2	VBATT[2]	0	No	R/W	100mV.	
1	VBATT[1]	0	No	R/W	50mV.	
0	VBATT[0]	0	No	R/W	25mV.	

REG06h

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	RESERVED	0	No	R	Reserved.	
6	RESERVED	0	No	R	Reserved.	
5	SYS_MIN[2]	1	No	R/W	000: 2.975V 001: 3.15V 010: 3.325V 011: 3.5V 100: 3.588V 101: 3.675V 110: 3.763V	Sets the system minimum regulation voltage (V_{SYS_MIN}). The actual system regulation voltage is this value plus V_{TRACK} = 150mV. Default: 3.588V (100) OTP-configurable.
4	SYS_MIN[1]	0	No	R/W		
3	SYS_MIN[0]	0	No	R/W		
2	TREG[2]	1	Yes	R/W	000: 60°C 001: 70°C 010: 80°C 011: 90°C 100: 100°C 101: 110°C 110: 120°C	Sets the thermal regulation threshold for charge mode, as well as the thermal protection threshold for boost mode. Default: 100°C (100)
1	TREG[1]	0	Yes	R/W		
0	TREG[0]	0	Yes	R/W		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG07h

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	IB_EN	0	Yes	R/W	0: IB outputs when the switcher is on 1: IB outputs all the time	Enables IB when only the battery is present, which uses about 3μA of battery current. Default: 0
6	WATCHDOG_RST	0	-	R/W	1: Reset the watchdog timer	After writing this bit to 1, the watchdog timer is reset, and this bit returns to 0.
5	WATCHDOG[1]	0	Yes	R/W	00: Disable timer 01: 40s 10: 80s 11: 160s	Default: 40s (01) OTP-configurable.
4	WATCHDOG[0]	1	Yes	R/W		
3	EN_TERM	1	Yes	R/W	0: Disable termination 1: Enable termination	Default: Enable termination (1)
2	EN_TMR2X	1	Yes	R/W	0: Disable 2x timer 1: Enable 2x timer	Default: Enable 2x timer (1)
1	CHG_TIMER[1]	1	Yes	R/W	00: Disable timer 01: 5hrs 10: 10hrs 11: 15hrs	Sets the charge safety timer. Default: 10hrs (10)
0	CHG_TIMER[0]	0	Yes	R/W		

REG08h

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	BATTFET_DIS	0	No	R/W	0: Allow BATTFET to remain on 1: Turn off BATTFET	Shipping mode or OCP. Writing to this bit controls whether the BATTFET is on or off. Reading this bit indicates the BATTFET's status.
6	BATTFET_DLY	1	No	R/W	0: Turn off BATTFET immediately 1: Turn off BATTFET after a 10s delay	Sets the delay after BATTFET_DIS is set to 1. Default: Turn off BATTFET after a 10s delay (1)
5	BATTFET_RST_EN	1	Yes	R/W	0: Disable the BATTFET reset function 1: Enable the BATTFET reset function	Default: Enable the BATTFET reset function (1)
4	OLIM[1]	1	Yes	R/W	00: 500mA 01: 1.5A 10: 2.1A 11: 3A	Sets the boost output current limit. Default: 3A (11)
3	OLIM[0]	1	Yes	R/W		
2	VBOOST[2]	1	No	R/W	011: 5.35V 010: 5.3V 001: 5.25V 000: 5.2V 111: 5.15V 110: 5.1V 101: 5.05V 100: 5V	Sets the boost output voltage. Default: 5.15V (111) OTP-configurable.
1	VBOOST[1]	1	No	R/W		
0	VBOOST[0]	1	No	R/W		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG09h

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	RESERVED	0	No	R	Reserved.	
6	RESERVED	1	Yes	R	Reserved.	
5	RESERVED	0	Yes	R	Reserved.	
4	RESERVED	1	Yes	R	Reserved.	
3	RESERVED	0	Yes	R	Reserved.	
2	EN_BOOST	0	Yes	R/W	0: Boost disabled 1: Boost enabled	
1	EN_BUCK	1	Yes	R/W	0: Buck disabled 1: Buck allowed	Set this bit to 0 to force the buck converter off.
0	EN_CHG	1	Yes	R/W	0: Charging disabled 1: Charging allowed	Set this bit to 0 to force charging off.

REG0Ah

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	RESERVED	0	No	R	Reserved.	
6	RESERVED	0	No	R	Reserved.	
5	AUTODPDM	1	Yes	R/W	0: D+/D- detection starts manually 1: D+/D- detection automatically starts after VIN_GD = 1 and the hold-off timer ends	Default: 1 OTP-configurable.
4	FORCEDPDM	0	-	R/W	0: Normal 1: Force D+/D- detection	This bit returns to 0 after it is written to 1. This bit is only effective when an input source is applied.
3	RESERVED	0	Yes	R	Reserved.	
2	RESERVED	0	Yes	R	Reserved.	
1	RESERVED	1	Yes	R	Reserved.	
0	RESERVED	1	Yes	R	Reserved.	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG0Ch

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	RESERVED	0	No	R	Reserved.	
6	NTC1_ ACTION	1	No	R/W	0: Only generate INT when the NTC1 status changes 1: NTC1 is fully functional	Default: 1 OTP-configurable.
5	NTC2_ ACTION	0	No	R/W	0: Only generate INT when the NTC2 status changes 1: NTC2 is fully functional	Default: 0 OTP-configurable.
4	BATT_OVP_ EN	1	Yes	R/W	0: Battery OVP is neglected 1: Battery OVP is enabled	Default: 1
3	BATT_LOW[1]	0	No	R/W	00: 3V falling 01: 3.1V falling 10: 3.2V falling 11: 3.3V falling	If V_{BATT} falls below BATT_LOW, an INT pulse is generated with a 10ms debounce. Default: 3V (00)
2	BATT_LOW[0]	0	No	R/W		
1	BOOST_STP_ EN	0	Yes	R/W	0: The BATT_LOW comparator only generates INT 1: The BATT_LOW comparator turns off boost operation and latches	Default: 0 OTP-configurable.
0	BOOST_OTP_ EN	1	Yes	R/W	0: Boost over-temperature protection is ignored 1: Boost over-temperature protection occurs at TREG	Default: 1 OTP-configurable.

REG0Dh

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	WARM_ ACT[1]	0	No	R/W	00: No action during an NTC warm condition 01: Reduce V_{BATT_REG} during an NTC warm condition 10: Reduce I_{CC} during an NTC warm condition 11: Reduce both V_{BATT_REG} and I_{CC} during an NTC warm condition	If both the NTC1_ACTION and NTC2_ACTION bits are set to 1, see Table 4 on page 19 for more details. Default: 01
6	WARM_ ACT[0]	1	No	R/W		
5	COOL_ACT[1]	1	No	R/W	00: No action during an NTC cool condition 01: Reduce V_{BATT_REG} during an NTC cool condition 10: Reduce I_{CC} during an NTC cool condition 11: Reduce both V_{BATT_REG} and I_{CC} during an NTC cool condition	If both the NTC1_ACTION and NTC2_ACTION bits are set to 1, see Table 4 on page 19 for more details. Default: 10
4	COOL_ACT[0]	0	No	R/W		
3	JEITA_ VSET[1]	0	Yes	R/W	00: V_{BATT_REG} - 100mV 01: V_{BATT_REG} - 150mV 10: V_{BATT_REG} - 200mV 11: V_{BATT_REG} - 250mV	Default: 00
2	JEITA_ VSET[0]	0	Yes	R/W		
1	JEITA_ISET[1]	0	Yes	R/W	00: 50% of I_{CC} 01: 33% of I_{CC} 10: 20% of I_{CC}	Default: 00
0	JEITA_ISET[0]	0	Yes	R/W		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG0Eh

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	VHOT[1]	1	Yes	R/W	00: 29.1% (50°C) 01: 25.9% (55°C) 10: 23% (60°C) 11: 20.4% (65°C)	Sets the hot falling threshold, as a percentage of V_{VRNTC}. Default: 23% (10)
6	VHOT[0]	0	Yes	R/W		
5	VWARM[1]	0	Yes	R/W	00: 36.5% (40°C) 01: 32.6% (45°C) 10: 29.1% (50°C) 11: 25.9% (55°C)	Sets the warm falling threshold, as a percentage of V_{VRNTC}. Default: 32.6% (01)
4	VWARM[0]	1	Yes	R/W		
3	VCOOL[1]	1	Yes	R/W	00: 74.2% (0°C) 01: 69.6% (5°C) 10: 64.8% (10°C) 11: 59.9% (15°C)	Sets the cool rising threshold, as a percentage of V_{VRNTC}. Default: 64.8% (10)
2	VCOOL[0]	0	Yes	R/W		
1	VCOLD[1]	0	Yes	R/W	00: 78.4% (-5°C) 01: 74.2% (0°C) 10: 69.6% (+5°C) 11: 64.8% (+10°C)	Sets the cold rising threshold, as a percentage of V_{VRNTC}. Default: 74.2% (01)
0	VCOLD[0]	1	Yes	R/W		

REG0Fh

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	RESERVED	0	No	R	Reserved.	
6	VIN_SRC_EN	0	Yes	R/W	0: Normal 1: Source current to the IN pin	Enables the input impedance test.
5	IVIN_SRC[3]	0	Yes	R/W	0000: 5μA 0001: 10μA 0010: 20μA 0011: 40μA 0100: 80μA 0101: 160μA 0110: 320μA 0111: 640μA 1000: 1280μA	Configures the input impedance test current source.
4	IVIN_SRC[2]	0	Yes	R/W		
3	IVIN_SRC[1]	0	Yes	R/W		
2	IVIN_SRC[0]	0	Yes	R/W		
1	VIN_TEST[1]	0	Yes	R/W	00: 0.3V 01: 0.5V 10: 1V 11: 1.5V	Configures the input impedance test comparator threshold.
0	VIN_TEST[0]	0	Yes	R/W		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG10h

Bits	Name	POR	WTD Reset	Type	Description	Comment
7	RESERVED	0	No	R	Reserved.	
6	RESERVED	1	No	R	Reserved.	
5	MASK_ THERM	0	No	R/W	0: Enable the THERM_STAT INT pulse 1: Mask the THERM_STAT INT pulse	OTP-configurable.
4	MASK_DPM	0	No	R/W	0: Enable the VINDPM and IINDPM INT pulses 1: Mask the VINDPM and IINDPM INT pulses	
3	MASK_ TOPOFF	0	No	R/W	0: Enable the TOPOFF timer INT pulse 1: Mask the TOPOFF timer INT pulse	
2	RESERVED	1	No	R	Reserved.	
1	MASK_BATT_ LOW	0	No	R/W	0: Enable the BATT_LOW INT pulse 1: Mask the BATT_LOW INT pulse	
0	RESERVED	0	No	R	Reserved.	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

STATUS BYTES (11h~16h)

Legend: POR = default value; R/W = read/write; R = read-only; INT = interrupt; YM = the interrupt can be masked

REG11h

Bits	Name	POR	R/W	INT	Description
7	DPDM_STAT[3]	-	R	No	Returns the input source D+/D- detection result. 0000: Not started (500mA) 0001: USB SDP (500mA) 0010: USB DCP (2A) 0011: USB CDP (1.5A) 0100: Divider 1 (1A) 0101: Divider 2 (2.1A) 0110: Divider 3 (2.4A) 0111: Divider 4 (2A) 1000: Unknown (500mA) 1001: USB DCP (2A) 1110: Divider 5 (3A)
6	DPDM_STAT[2]	-	R	No	
5	DPDM_STAT[1]	-	R	No	
4	DPDM_STAT[0]	-	R	No	
3	RESERVED	-	R	No	Reserved.
2	RESERVED	-	R	No	Reserved.
1	VINDPM_STAT	-	R	YM	0: Not in VINDPM 1: In VINDPM
0	IINDPM_STAT	-	R	YM	0: Not in IINDPM 1: In IINDPM

REG12h

Bits	Name	POR	R/W	INT	Description
7	RESERVED	-	R	No	Reserved.
6	VIN_GD	-	R	Yes	When $V_{VIN_UV} < V_{IN} < V_{VIN_OV}$ in buck mode, this bit is set to 1 and the PG pin is driven low (after a 15ms debounce time). 0: The input source is not valid 1: The input source is good
5	VIN_RDY	-	R	Yes	Indicates whether input source type detection has finished. IIN_LIM[4:0] is updated. 0: V_{IN} is not ready to charge 1: V_{IN} is ready to charge
4	RESERVED	-	R	No	Reserved.
3	THERM_STAT	-	R	YM	0: Not in thermal regulation 1: In thermal regulation
2	VSYS_STAT	-	R	No	0: $V_{BATT} < V_{SYS_MIN}$ 1: $V_{BATT} > V_{SYS_MIN}$
1	WATCHDOG_ FAULT	-	R	Yes	0: Normal 1: The watchdog timer has expired
0	WATCHDOG_ BARK	-	R	Yes	0: Normal 1: The 3/4 watchdog timer has expired

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REG13h

Bits	Name	POR	R/W	INT	Description
7	CHG_STAT[2]	-	R	No	000: Not charging 001: Trickle charge 010: Pre-charge 011: Fast charge 100: Constant-voltage charge 101: Charging is done
6	CHG_STAT[1]	-	R	No	
5	CHG_STAT[0]	-	R	No	
4	BOOST_ FAULT[2]	-	R	Yes	000: Normal 001: An IN overload or short (latch-off) has occurred 010: Boost over-voltage protection (OVP) (not latch) has occurred 011: Boost over-temperature protection (latch-off) has occurred 100: The boost has stopped due to BATT_LOW (latch-off)
3	BOOST_ FAULT[1]	-	R	Yes	
2	BOOST_ FAULT[0]	-	R	Yes	
1	CHG_FAULT[1]	-	R	Yes	00: Normal 01: Input OVP 10: The charge timer has expired 11: Battery OVP
0	CHG_FAULT[0]	-	R	Yes	

REG14h

Bits	Name	POR	R/W	INT	Description
7	NTC_MISSING	-	R	Yes	0: Normal 1: NTC is missing (V_{NTC} > 95% of V_{VRNTC})
6	BATT_MISSING	-	R	Yes	0: Normal 1: The battery is missing (2 terminations detected within 3 seconds)
5	NTC1_FAULT[2]	-	R	Yes	000: Normal 001: Warm 010: Cool 011: Cold 100: Hot
4	NTC1_FAULT[1]	-	R	Yes	
3	NTC1_FAULT[0]	-	R	Yes	
2	NTC2_FAULT[2]	-	R	Yes	000: Normal 001: Warm 010: Cool 011: Cold 100: Hot
1	NTC2_FAULT[1]	-	R	Yes	
0	NTC2_FAULT[0]	-	R	Yes	

REG16h

Bits	Name	POR	R/W	INT	Description
7	RESERVED	-	R	No	Reserved.
6	TOPOFF_ACTIVE	-	R	YM	0: The top-off timer is not counting 1: The top-off timer is counting
5	BFET_STAT	-	R	No	0: The battery is charging or disabled 1: The battery is discharging
4	BATT_LOW_STAT	-	R	YM	The hysteresis = 200mV. 0: V_{BATT} is greater than BATT_LOW[1:0] 1: V_{BATT} is below BATT_LOW[1:0]
3	RESERVED	-	R	No	Reserved.
2	VIN_TEST_HIGH	-	R	Yes	0: V_{IN} is below the VIN_TEST threshold 1: V_{IN} has reached the VIN_TEST threshold
1	RESERVED	-	R	No	Reserved.
0	RESERVED	-	R	No	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

INTERRUPT LIST

INT Name	Related Registers	Can be Masked	Event
VIN_GD	VIN_GD changes	No	A good input source has been detected.
DPDM_DET_DONE	DPDM_STAT[3:0] changes	No	DPDM detection is finished.
VIN_RDY	VIN_RDY: 0 to 1	No	The input current limit has been updated; the buck converter starts.
CHG_DONE	CHG_STAT[2:0]: any value to 101	No	Charging has terminated.
RECHARGE	CHG_STAT[2:0] exits 101 and enters the CC/CV charge	No	Recharging has been initiated.
THERM_STAT	THERM_STAT: 0 to 1	Yes	The IC has entered charge thermal regulation.
WATCHDOG_FAULT	WATCHDOG_FAULT: 0 to 1	No	A watchdog timeout has occurred.
WATCHDOG_BARK	WATCHDOG_BARK: 0 to 1	No	A watchdog bark has occurred.
CHG_FAULT	CHG_FAULT[1:0]: • 00 to 01 • 00 to 10 • 00 to 11	No	One of the following charge faults has occurred: input OVP, battery OVP, or the charge timer has expired.
NTC_MISSING	NTC_MISSING changes	No	NTC is missing.
BATT_MISSING	BATT_MISSING changes	No	BATT is missing.
BOOST_FAULT	BOOST_FAULT[2:0]: • 000 to 001 • 000 to 010 • 010 to 000 • 000 to 011 • 000 to 100	No	One of the following boost fault has occurred: IN overload or short, boost OVP, boost OTP, the boost has stopped due to BATT_LOW.
NTC_FAULT	NTC1_FAULT[2:0] or NTC2_FAULT[2:0] changes	No	The NTC status has changed.
VINDPM_STAT	VINDPM_STAT: 0 to 1	Yes	The V_{IN} regulation loop has been entered.
IINDPM_STAT	IINDPM_STAT: 0 to 1		The I_{IN} regulation loop has been entered.
TOPOFF_TMR	TOPOFF_ACTIVE changes	Yes	The TOPOFF timer has started and ended.
BATT_LOW	BATT_LOW_STAT: 0 to 1	Yes	V_{BATT} has dropped to the BATT_LOW threshold.
VIN_TEST_HIGH	VIN_TEST_HIGH: 0 to 1	No	V_{IN} has reached the VIN_TEST threshold during the input impedance test.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ONE-TIME PROGRAMMABLE (OTP) MAP

The MP2720 has a one-time programmable (OTP) function to configure the default values for certain registers. The OTP map below shows the OTP-configurable commands.

#	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
00h	N/A	EN_STAT_IB	EN_PG_ NTC2	N/A	HOLDOFF_ TMR	SW_FREQ[1:0]		N/A
01h	IIN_MODE			N/A	N/A	N/A	N/A	N/A
02h	N/A	N/A	N/A	ICC[4:0]				
03h	N/A	IPRE[2:0]		ITERM[3:0]				
04h	N/A	ITRICKLE[2:0]		N/A				
05h	N/A	N/A	VBATT[5:0]					
06h	N/A	N/A	SYS_MIN[2:0]			N/A	N/A	N/A
07h	N/A	N/A	WATCHDOG[1:0]		N/A	N/A	N/A	N/A
08h	N/A	N/A	N/A	N/A	N/A	VBOOST[2:0]		
0Ah	N/A	N/A	AUTODPDM	N/A	N/A	N/A	N/A	N/A
0Ch	N/A	NTC1_ ACTION	NTC2_ ACTION	N/A	N/A	N/A	BOOST_ STP_EN	BOOST_ OTP_EN
10h	N/A	N/A	MASK_ THERM	N/A	N/A	N/A	N/A	N/A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ONE-TIME PROGRAMMABLE (OTP) DEFAULT

OTP Items	Default
EN_STAT_IB	0: STAT
EN_PG_NTC2	0: PG
HOLDOFF_TMR	1: Enable the hold-off timer
SW_FREQ[1:0]	01: 1MHz
IIN_MODE[2:0]	000: Follow the IIN_LIM setting
ICC[4:0]	01101: 1040mA
IPRE[2:0]	010: 160mA
ITERM[3:0]	0001: 60mA
ITRICKLE[2:0]	001: 64mA
VBATT[5:0]	011000: 4.2V
SYS_MIN[2:0]	100: 3.588V
WATCHDOG[1:0]	01: 40s
VBOOST[2:0]	111: 5.15V
AUTODPDM	1: D+/D- detection automatically starts after VIN_GD = 1 and the hold-off timer ends
NTC1_ACTION	1: Active
NTC2_ACTION	0: INT only
BOOST_STP_EN	0: The BATT_LOW comparator only generates INT
BOOST_OTP_EN	1: Boost operation stops if over-temperature protection occurs
MASK_THERM	0: Allow INT

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

APPLICATION INFORMATION

Selecting the Inductor

Inductor selection is a tradeoff between cost, size, and efficiency. A lower-value inductor corresponds to a smaller size, but also results in a higher current ripple, higher magnetic hysteretic losses, and higher output capacitances. A higher-value inductor results in a lower ripple current and smaller output filter capacitors, but it also results in higher inductor DC resistance (DCR) loss.

Estimate the required inductance with Equation (1):

$$L = \frac{V_{IN} - V_{SYS}}{\Delta I_{L_MAX}} \times \frac{V_{SYS}}{V_{IN} \times f_{SW}} \quad (1)$$

Where V_{IN} is the input voltage, V_{SYS} is the converter's output voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum peak-to-peak inductor current, which is typically designed to be 20% to 40% of the maximum load current.

Choose an inductor that does not saturate under the worst-case load condition, calculated with Equation (2):

$$I_{SAT} > I_{LOAD} + \frac{\Delta I_{L_MAX}}{2} \quad (2)$$

Where I_{SAT} is the inductor saturation current, and I_{LOAD} is the buck converter's maximum load.

Selecting the PMID Capacitor (C_{PMID})

The PMID capacitor (C_{PMID}) decouples the switching buck converter and absorbs the switching ripple current. Select C_{PMID} based on the demand for the PMID current ripple. The input current ripple can be calculated with Equation (3):

$$I_{RMS_MAX} = I_{LOAD} \times \frac{\sqrt{V_{SYS} \times (V_{IN} - V_{SYS})}}{V_{IN}} \quad (3)$$

Use low-ESR ceramic capacitors with an X7R or X5R rating for C_{PMID}. This capacitor should be placed as close to the PMID and PGND pins as possible. The capacitor's voltage rating must exceed V_{IN}, and it is recommended to consider the plug-in overshoot voltage. A capacitor rated for at least 25V is recommended for applications with a 15V V_{IN}. Generally, a capacitance of 10µF is considered a sufficient starting value.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PCB Layout Guidelines

PCB layout is important to meet specified noise, efficiency, and stability requirements. For the best results, refer to Figure 15 and follow the guidelines below:

1. Place the PMID capacitor as close as possible to the PMID and PGND pins using a short copper plane connection. Place the PMID capacitor on the same layer as the IC.
2. Minimize the high-frequency current path loop between the PMID capacitor and the buck converter power MOSFETs (from the PMID pin to the capacitor to ground).
3. Place the inductor's input terminal as close as possible to the SW pin.
4. Minimize the copper area of the inductor's input terminal trace to reduce electrical and magnetic field radiation, but ensure that the trace is wide enough to carry the charging current.
5. Minimize parasitic capacitance from the inductor input terminal to any other trace or plane.
6. Place decoupling capacitors (e.g. the VCC pin capacitor) as close as possible to the IC pins, and make the connection as short as possible.
7. Connect the IC's power pin to as many copper planes as possible to conduct heat away from the IC.
8. Ensure that the number and physical size of the vias are sufficient for a current path.

Figure 15 shows a high-frequency current path. In this figure, the high-frequency path (the high-side MOSFET, low-side MOSFET and the PMID capacitor) must be minimized.

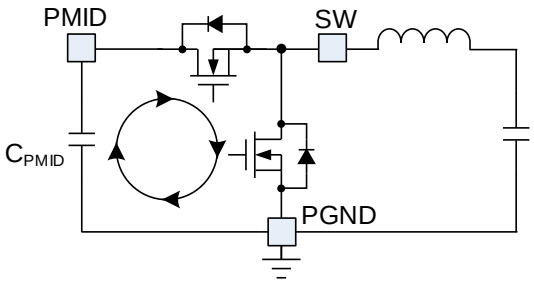


Figure 15: High-Frequency Current Path

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

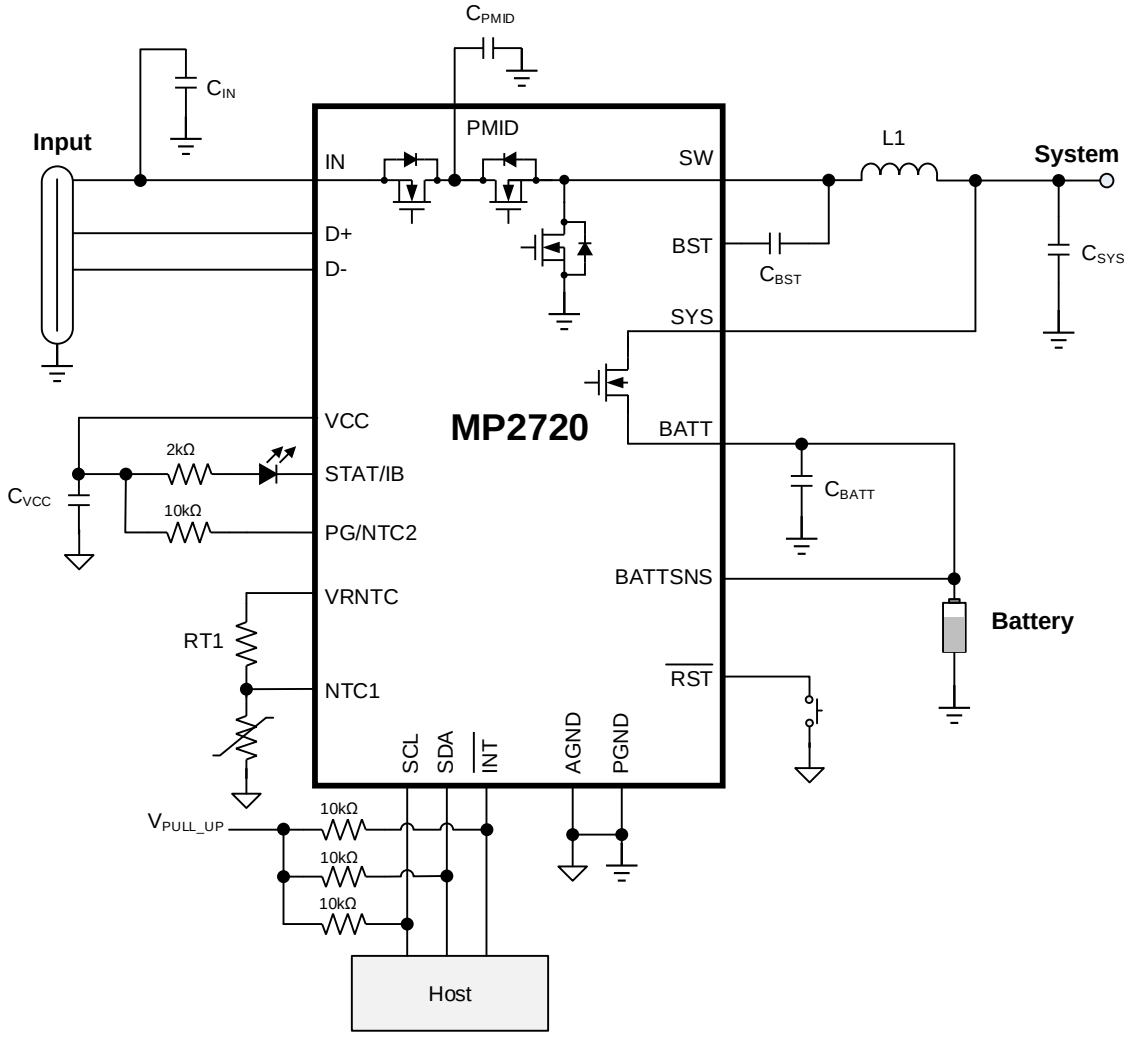


Figure 16: Typical Application Circuit

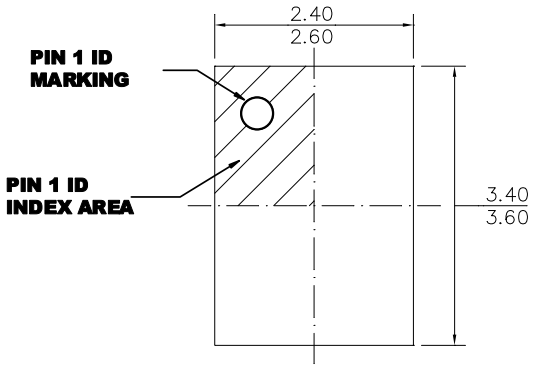
Table 6: Key BOM for Figure 16

Qty	Ref	Value	Description	Package	Manufacturer
1	C_{IN}	1µF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	C_{PMID}	10µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
2	C_{SYS}	10µF x 2	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C_{BATT}	10µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C_{VCC}	4.7µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
1	C_{BST}	22nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	L1	1µH	Inductor, 1µH, low DCR	SMD	Any
1	RT1	10kΩ	Film resistor, 1%, same value as the NTC resistance at 25°C	0603	Any

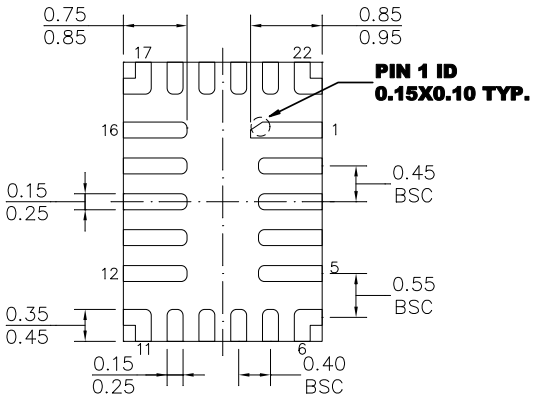
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PACKAGE INFORMATION

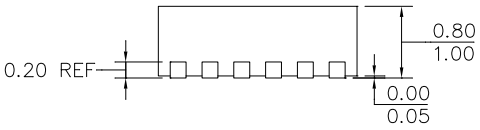
QFN-22 (2.5mmx3.5mm)



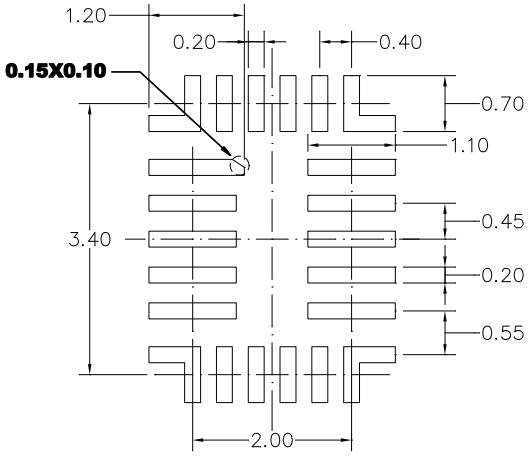
TOP VIEW



BOTTOM VIEW



SIDE VIEW



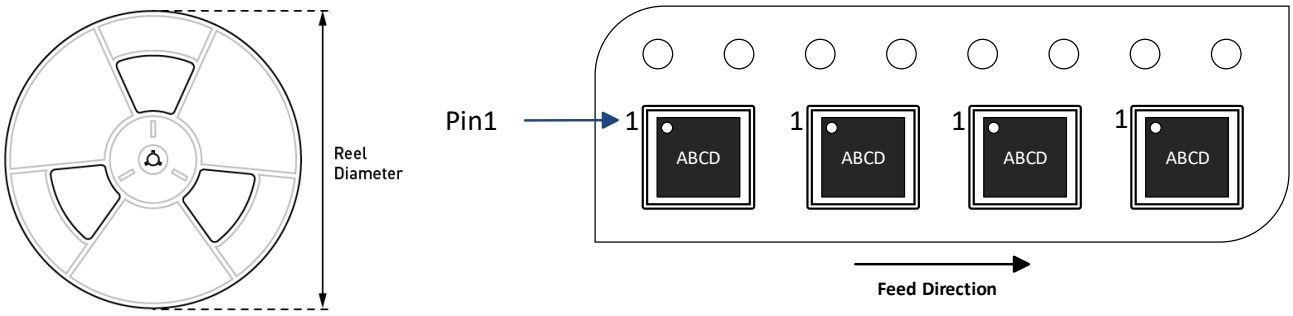
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2720GRH-xxxx-Z	QFN-22 (2.5mmx3.5mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/4/2022	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.