OPA165x SoundPlus™ 低噪声和低失真通用 FET 输入音频运算放大器

1 特性

- 低噪声：
  4.5nV/√Hz（频率为 1kHz 时）
  3.8nV/√Hz（频率为 10kHz 时）
- 低失真：1kHz 时为 0.00005%
- 低静态电流：
  每通道 2mA
- 低输入偏压电流：10pA
- 压摆率： 10V/μs
- 宽增益带宽：18MHz (G = 1)
- 单位增益稳定
- 轨到轨输出
- 宽电源电压范围：
  ±2.25V 至 ±18V 或 4.5V 至 36V
- 可提供双通道和四通道版本
- 小型封装：
  双通道：小外形尺寸 (SO)-8 和微型小外形尺寸 (MSOP)-8
  四通道：小外形尺寸 (SO)-14 和薄型小外形尺寸 (TSSOP)-14

2 应用

- 模拟和数字混音器
- 音效处理器
- 乐器
- A/V接收器
- DVD和 蓝光(Blu-Ray)™播放器
- 车载音频系统

3 说明

OPA1652（双通道）和 OPA1654（四通道）FET 输入运算放大器在 1kHz 时可实现 4.5nV/√Hz 的低噪声密度和 0.00005% 的超低失真。OPA1652 和 OPA1654 运算放大器在 2kΩ 负载条件下提供摆幅在 800mV 以内的轨到轨输出，这有助于提高余量并实现动态范围的最大化。此外，这些器件还具有 ±30mA 高输出驱动能力。

这些器件可在 ±2.25V 至 ±18V，或者 4.5V 至 36V 的极宽电源电压范围内运行，每通道电源电流仅为 2mA。OPA1652与OPA1654系列运算放大器单位增益稳定并且可在较宽的负载范围内提供出色的动态性能。

它们还采用完全独立的电路系统，可将串扰降到最低，即便在过驱动或过载时也不受通道间相互作用而带来的干扰。

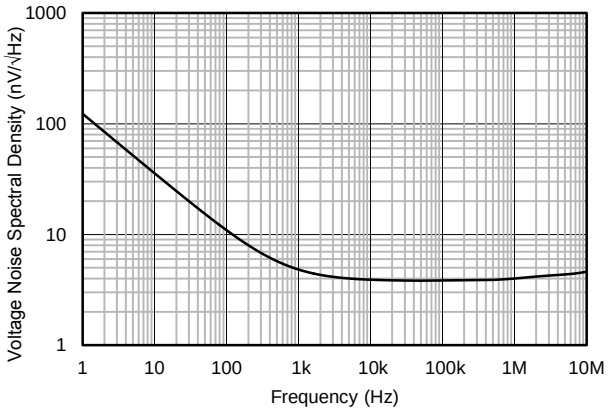
OPA1652与OPA1654 额定温度范围为 –40°C 至 +85°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA1652	SOIC (8)	4.90mm x 3.91mm
	VSSOP (8)	3.00mm × 3.00mm
	WSON (8)	3.00mm × 3.00mm
OPA1654	SOIC (14)	8.65mm x 3.91mm
	TSSOP封装(14)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

输入电压噪声频谱密度



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

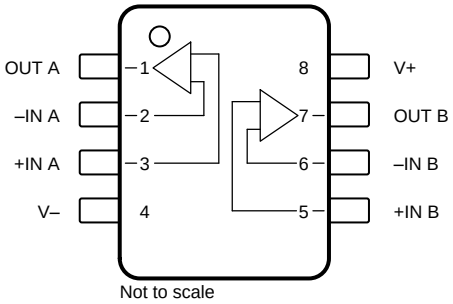
Changes from Revision A (August 2016) to Revision B **Page**

- 已添加 向*器件信息* 表添加了 SON 封装和封装尺寸的新信息 ... 1
- Added new pinout drawing for OPA1652 DRG (WSON) package ... 3
- Added thermal information for the DRG (WSON) package in the *Thermal Information* table ... 6

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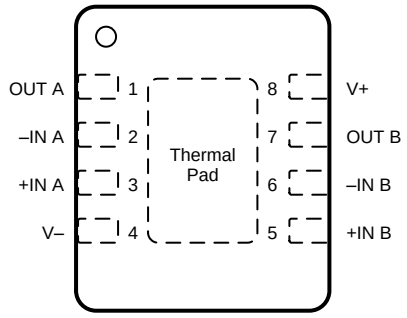
5 Pin Configuration and Functions

OPA1652 D and DGK Packages
8-Pin SOIC and VSSOP
Top View



Not to scale

OPA1652 DRG Package
8-Pin WSON With Exposed Thermal Pad
Top View



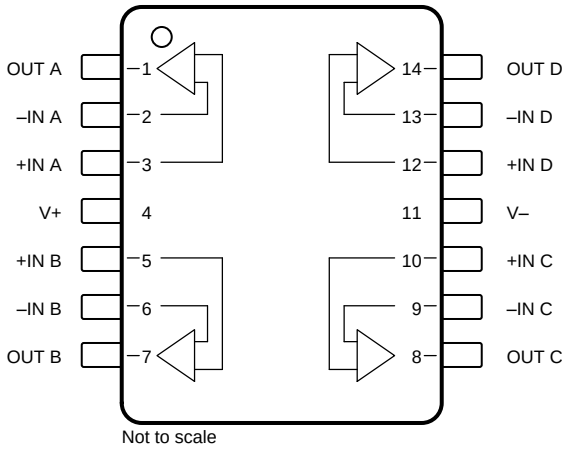
Not to scale

Pin Functions: OPA1652

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply
Thermal pad	—	—	Exposed thermal die pad on underside of DRG package; connect thermal die pad to V–. Soldering the thermal pad improves heat dissipation and provides specified performance

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OPA1654 D and PW Packages
14-Pin SOIC and TSSOP
Top View



Not to scale

Pin Functions: OPA1654

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN D	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)		40	V
	Input	(V–) – 0.5	(V+) + 0.5	V
Current	Input (all pins except power-supply pins)	–10	10	mA
	Output short-circuit(2)	Continuous		
Temperature	Operating, T_A	–55	125	°C
	Junction, T_J		200	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2 (ground in symmetrical dual supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Supply voltage	4.5 (±2.25)		36 (±18)	V
T_A	Operating temperature	–40		85	°C

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6.4 Thermal Information: OPA1652

THERMAL METRIC[1]		OPA1652			UNIT
		D (SOIC)	DGK (VSSOP)	DRG (WSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	143.6	218.9	66.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.9	78.6	54.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.8	103.7	40.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.8	14.6	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.3	101.8	40.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA1654

THERMAL METRIC[1]		OPA1654		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.1	126.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.8	46.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	58.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.9	5.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.2	57.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.6 Electrical Characteristics: V_S = ±15 V

at T_A = 25°C, R_L = 2 kΩ, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE							
THD + N	Total harmonic distortion + noise				0.00005%		
		G = 1, f = 1 kHz, V_O = 3 V_{RMS}			–126		dB
IMD	Intermodulation distortion	G = 1, V_O = 3 V_{RMS}	SMPTE and DIN Two-Tone, 4:1 (60 Hz and 7 kHz)		0.00005%		
					–126		dB
			DIM 30 (3-kHz square wave and 15-kHz sine wave)		0.00005%		
					–126		dB
			CCIF Twin-Tone (19 kHz and 20 kHz)		0.00005%		
					–126		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = 1			18		MHz
SR	Slew rate	G = –1			10		V/µs
	Full power bandwidth(1)	V_O = 1 V_P			1.6		MHz
	Overload recovery time	G = –10			1		µs
	Channel separation (dual and quad)	f = 1 kHz			–120		dB
NOISE							
e_n	Input voltage noise	f = 20 Hz to 20 kHz			4.0		μV_{PP}
	Input voltage noise density	f = 1 kHz			4.5		nV/√Hz
		f = 10 kHz			3.8		nV/√Hz
I_n	Input current noise density	f = 1 kHz			3		fA/√Hz
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±2.25 V to ±18 V			±0.5	±1.5	mV
		V_S = ±2.25 V to ±18 V, T_A = –40°C to 85°C(2)			2	8	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±2..25 V to ±18 V			3	8	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0 V			±10	±100	pA
I_{OS}	Input offset current	V_{CM} = 0 V			±10	±100	pA
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) + 0.5		(V+) – 2	V
CMRR	Common-mode rejection ratio			100	110		dB
INPUT IMPEDANCE							
	Differential				100 || 6		MΩ || pF
	Common-mode				6000 || 2		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.8 V ≤ V_O ≤ (V+) – 0.8 V, R_L = 2 kΩ		106	114		dB
OUTPUT							
V_{OUT}	Voltage output	R_L = 2 kΩ		(V–) + 0.8		(V+) – 0.8	V
I_{OUT}	Output current			See *Typical Characteristics*			mA
Z_O	Open-loop output impedance	f = 1 MHz		See *Typical Characteristics*			Ω
I_{SC}	Short-circuit current(3)				±50		mA
C_{LOAD}	Capacitive load drive				100		pF
POWER SUPPLY							
V_S	Specified voltage			±2.25		±18	V
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A			2	2.5	mA
		I_{OUT} = 0 A, T_A = –40°C to 85°C(2)				2.8	mA
TEMPERATURE							
	Specified range			–40		85	°C
	Operating range			–55		125	°C

(1) Full-power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.
(3) One channel at a time.

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6.7 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

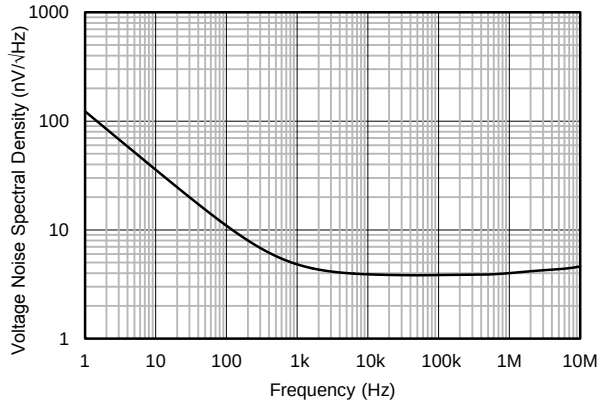


图 1. Input Voltage Noise Density vs Frequency

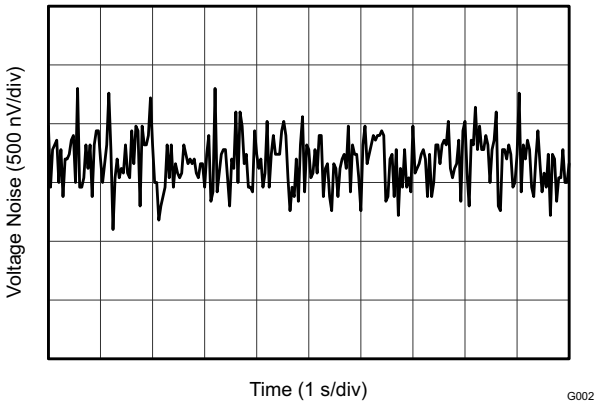


图 2. 0.1-Hz to 10-Hz Noise

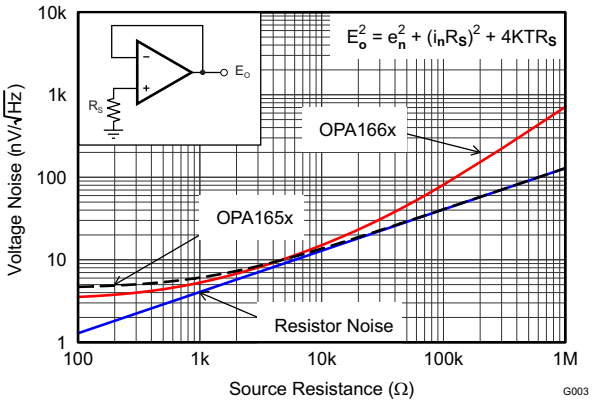


图 3. Voltage Noise vs Source Resistance

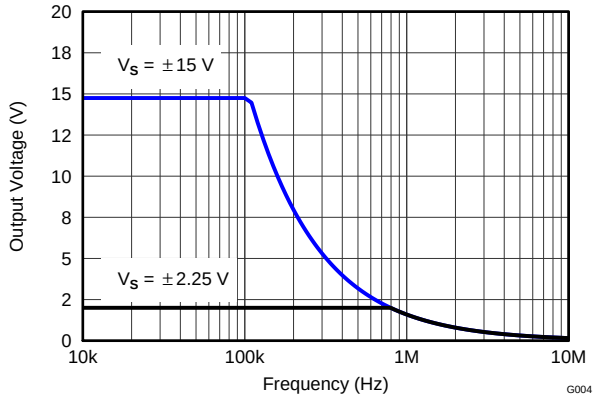


图 4. Maximum Output Voltage vs Frequency

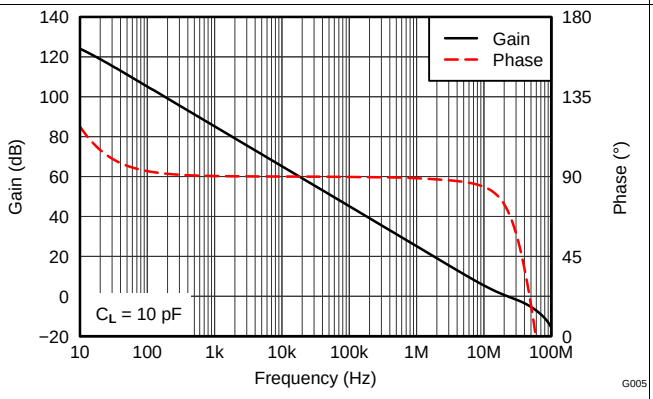


图 5. Gain and Phase vs Frequency

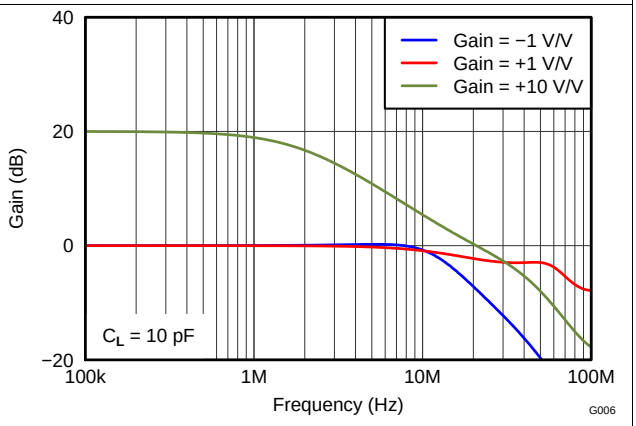


图 6. Closed-Loop Gain vs Frequency

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Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

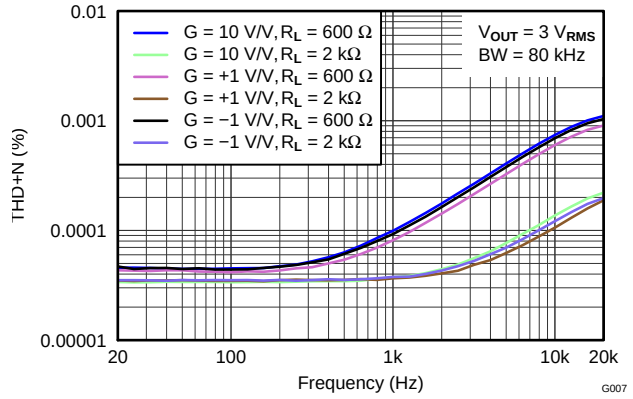


图 7. THD+N Ratio vs Frequency

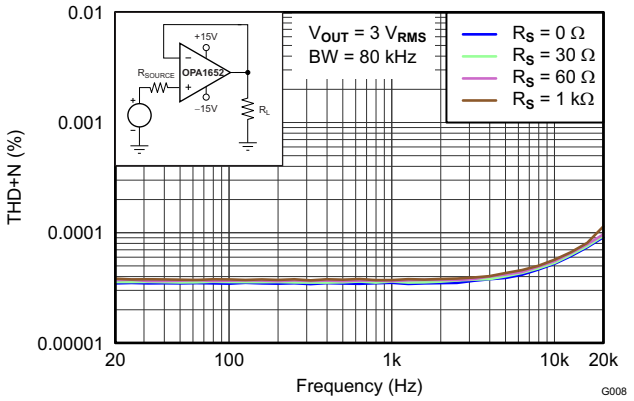


图 8. THD+N Ratio vs Frequency

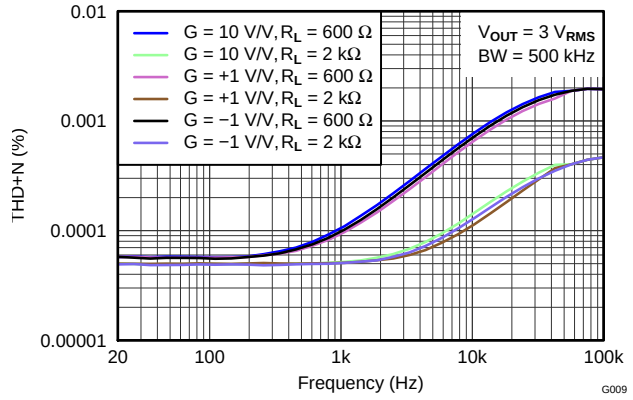


图 9. THD+N Ratio vs Frequency

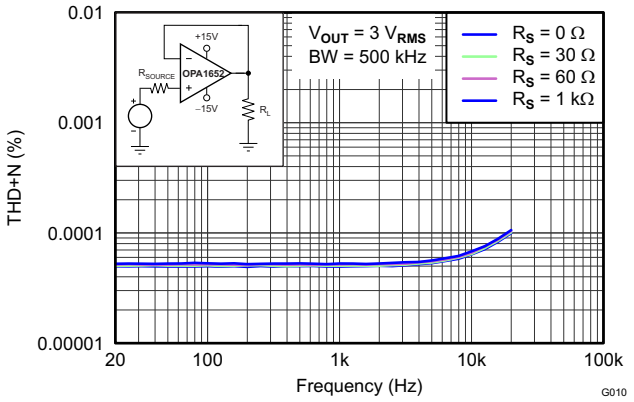


图 10. THD+N Ratio vs Frequency

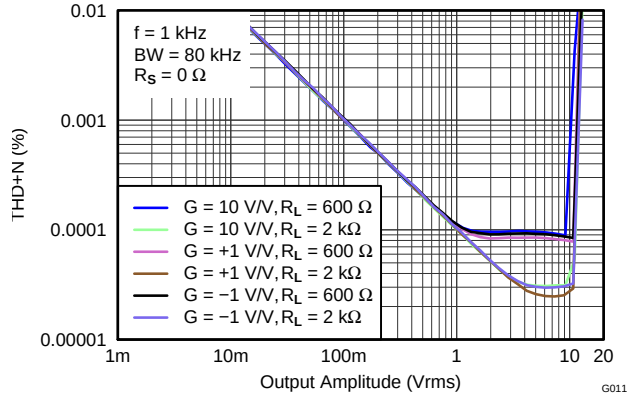


图 11. THD+N Ratio vs Output Amplitude

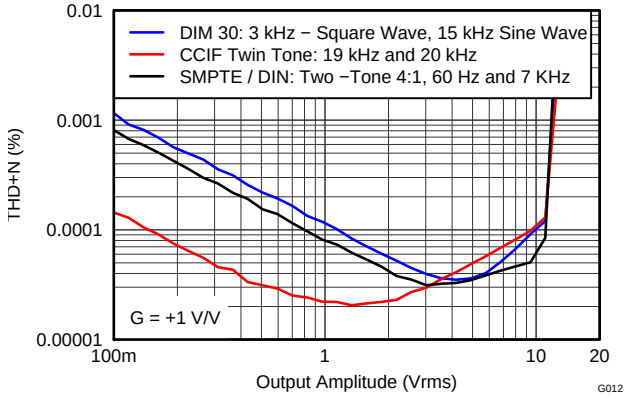


图 12. Intermodulation Distortion vs Output Amplitude

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

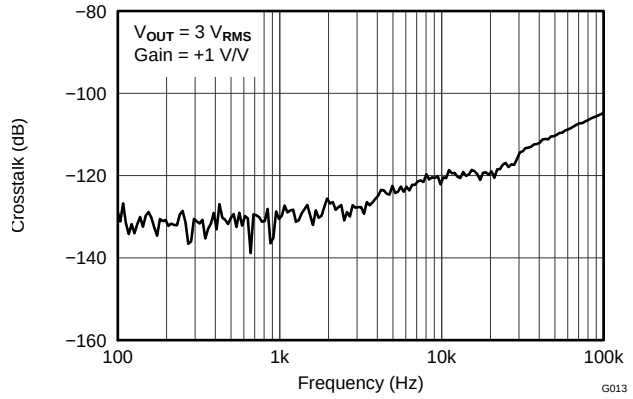


图 13. Channel Separation vs Frequency

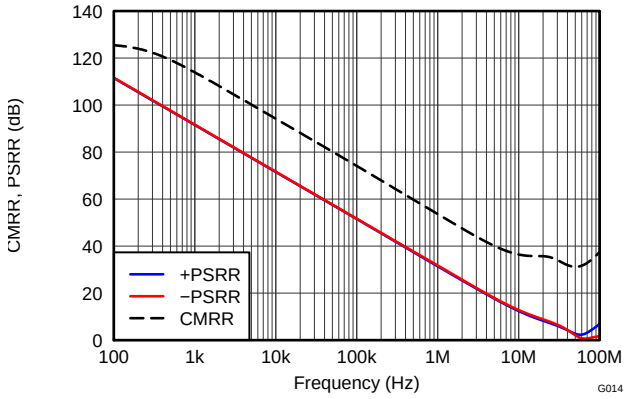


图 14. CMRR and PSRR vs Frequency (Referred to Input)

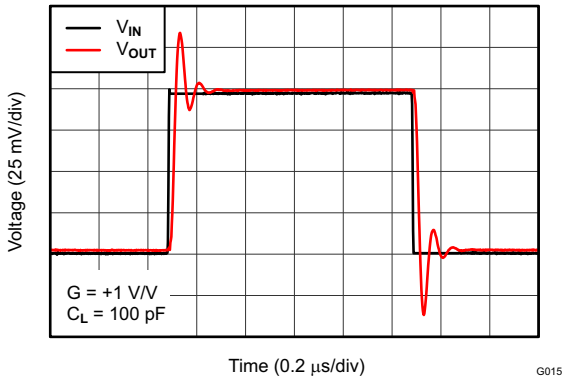


图 15. Small-Signal Step Response (100 mV)

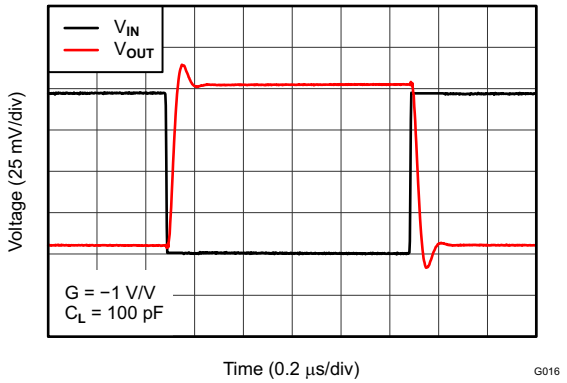


图 16. Small-Signal Step Response (100 mV)

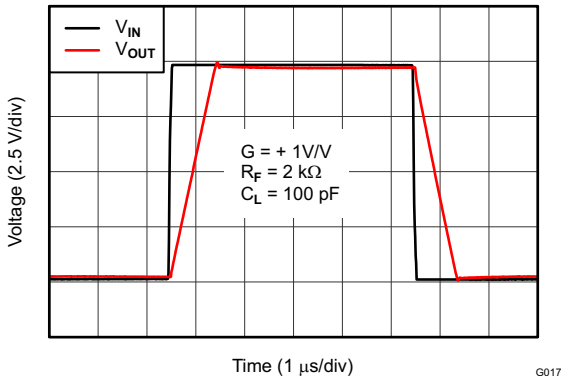


图 17. Large-Signal Step Response

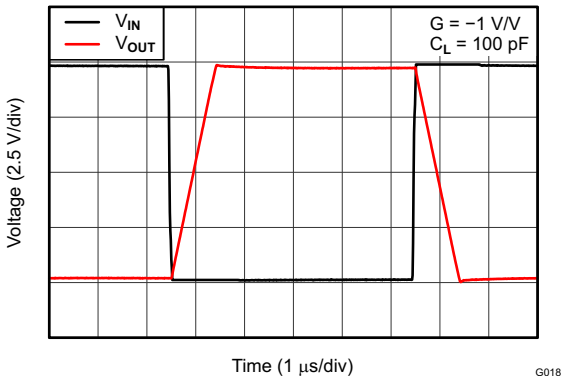


图 18. Large-Signal Step Response

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Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

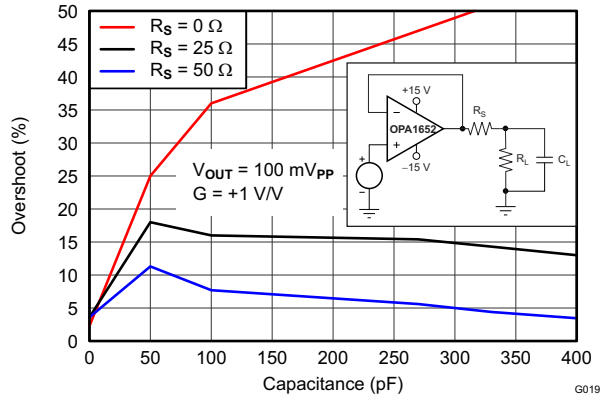


图 19. Small-Signal Overshoot vs Capacitive Load

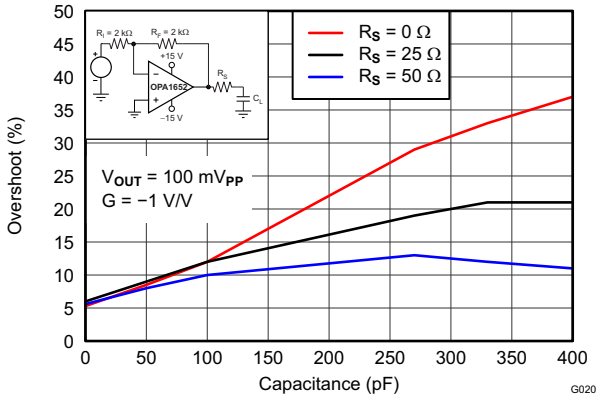


图 20. Small-Small-Signal Overshoot vs Capacitive Load

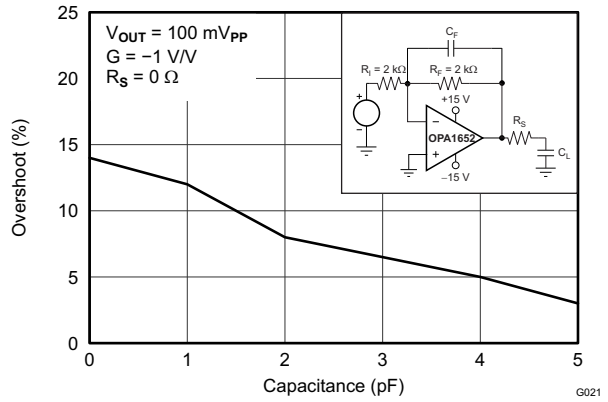


图 21. Small-Signal Overshoot vs Feedback Capacitor (100-mV Output Step)

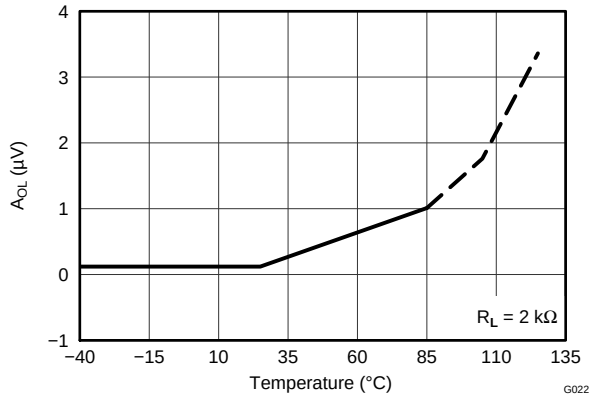


图 22. Open-Loop Gain vs Temperature

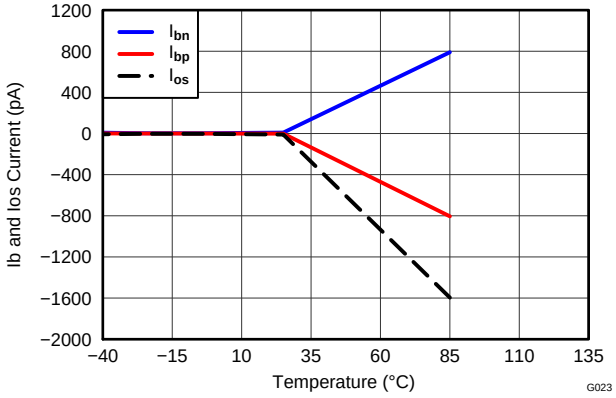


图 23. I_B and I_{OS} vs Temperature

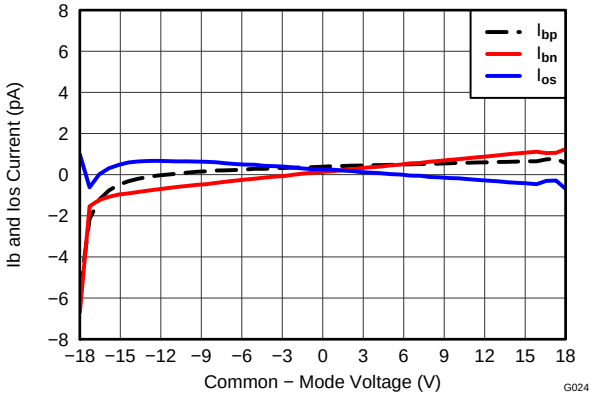


图 24. I_B and I_{OS} vs Common-Mode Voltage

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

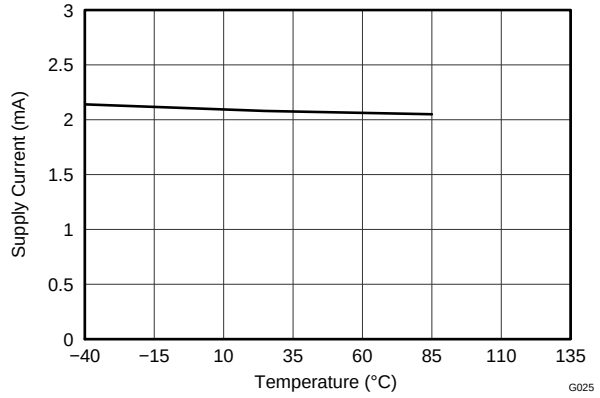


图 25. Supply Current vs Temperature

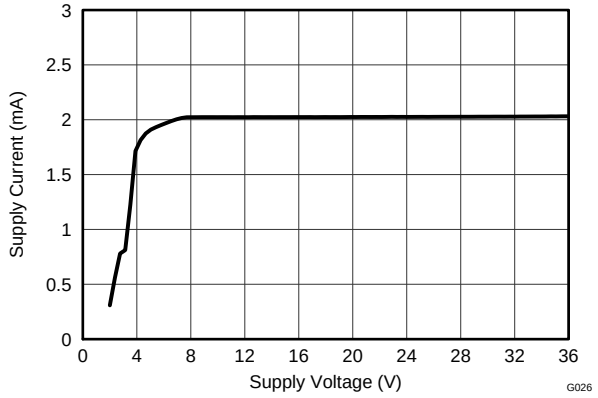


图 26. Supply Current vs Supply Voltage

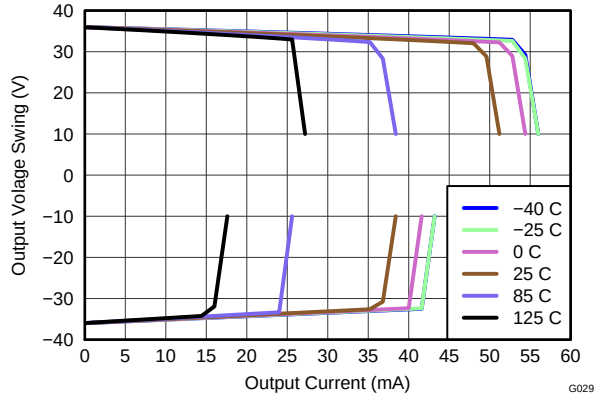


图 27. Output Voltage vs Output Current

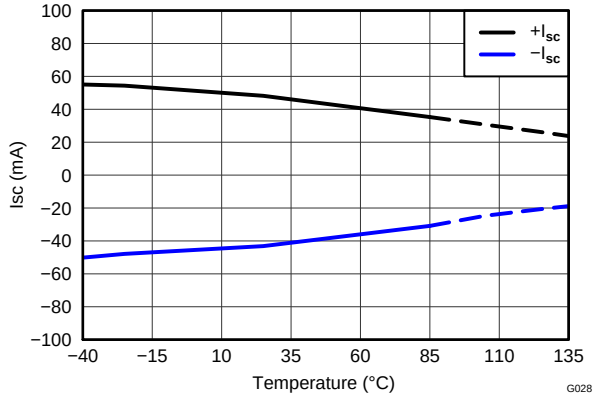


图 28. Short-Circuit Current vs Temperature

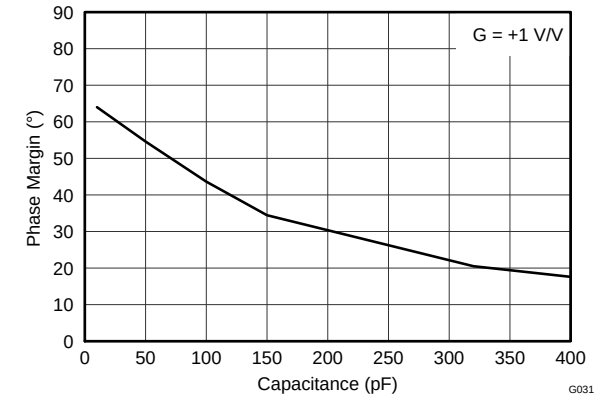


图 29. Phase Margin vs Capacitive Load

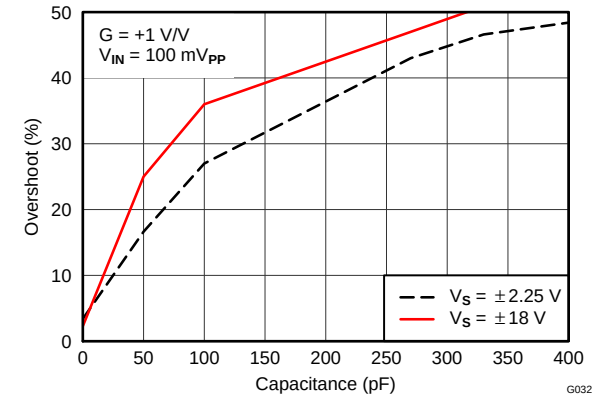


图 30. Percent Overshoot vs Capacitive Load

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Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

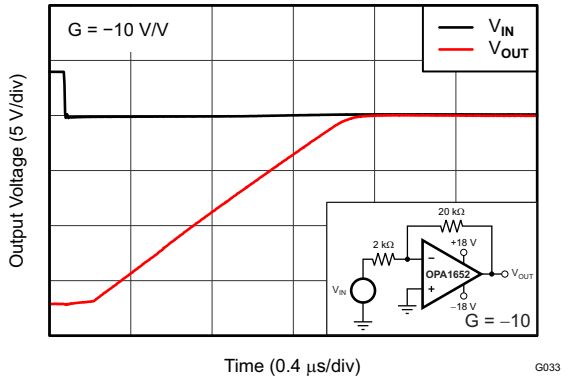


图 31. Negative Overload Recovery

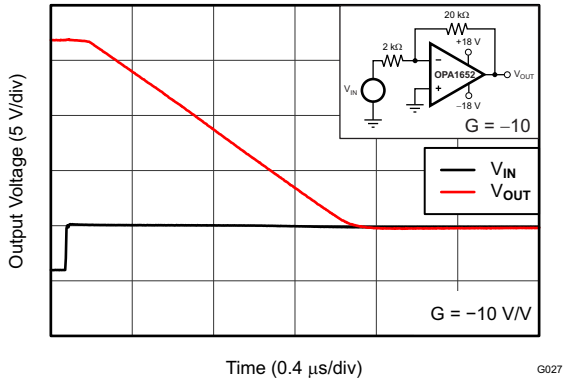


图 32. Positive Overload Recovery

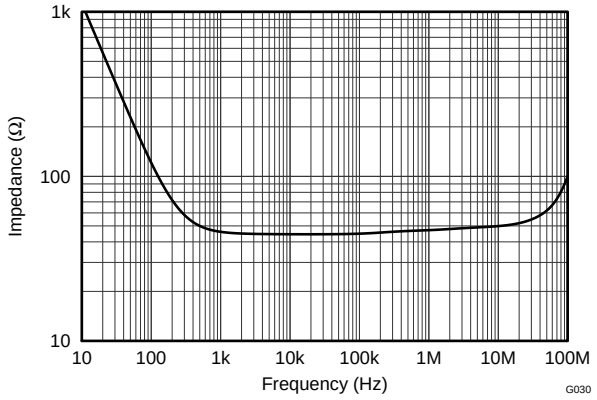


图 33. Open-Loop Output Impedance vs Frequency

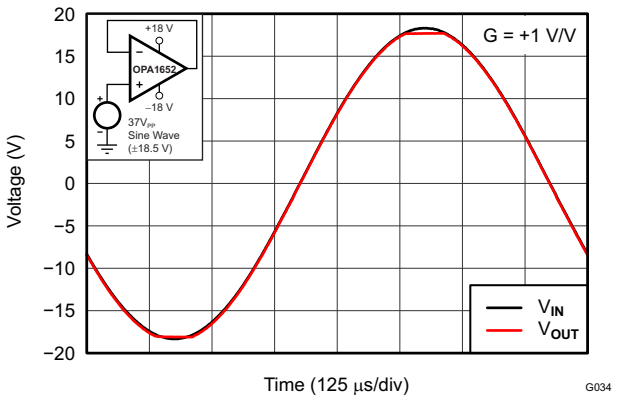


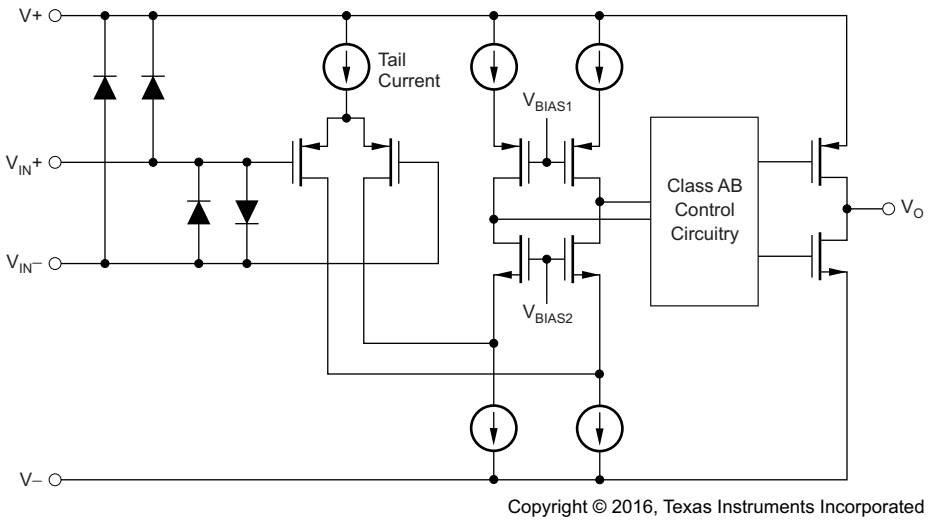
图 34. No Phase Reversal

7 Detailed Description

7.1 Overview

The OPA1652 and OPA1654 are unity-gain stable, precision dual and quad op amps with very low noise. The *Functional Block Diagram* shows a simplified schematic of the OPA165x (with one channel shown). The device consists of a very low noise input stage with a folded cascode and a rail-to-rail output stage. This topology exhibits superior noise and distortion performance across a wide range of supply voltages not previously delivered by audio operational amplifiers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Phase Reversal Protection

The OPA165x family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA165x prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in 图 35.

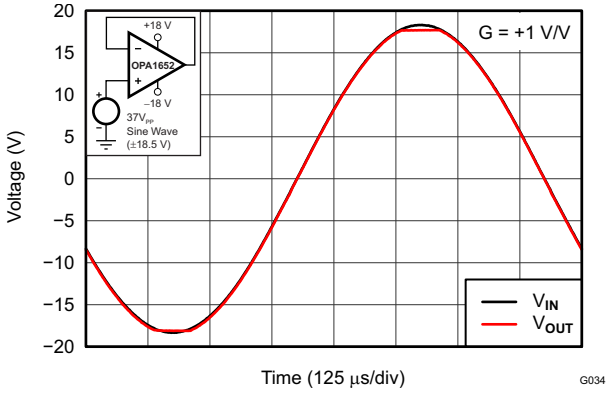


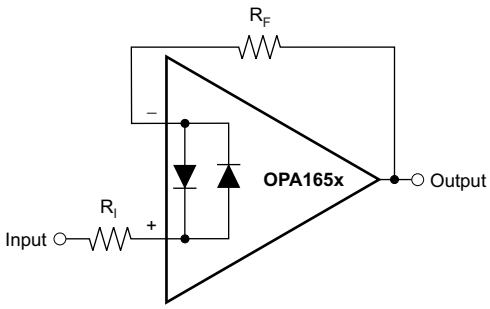
图 35. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition

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Feature Description (接下页)

7.3.2 Input Protection

The input terminals of the OPA1652 and OPA1654 are protected from excessive differential voltage with back-to-back diodes, as 图 36 illustrates. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor (R_I) or a feedback resistor (R_F) can limit the signal input current. This resistor degrades the low-noise performance of the OPA165x, and is examined in the *Noise Performance* section. 图 36 shows an example configuration when both current-limiting input and feedback resistors are used.



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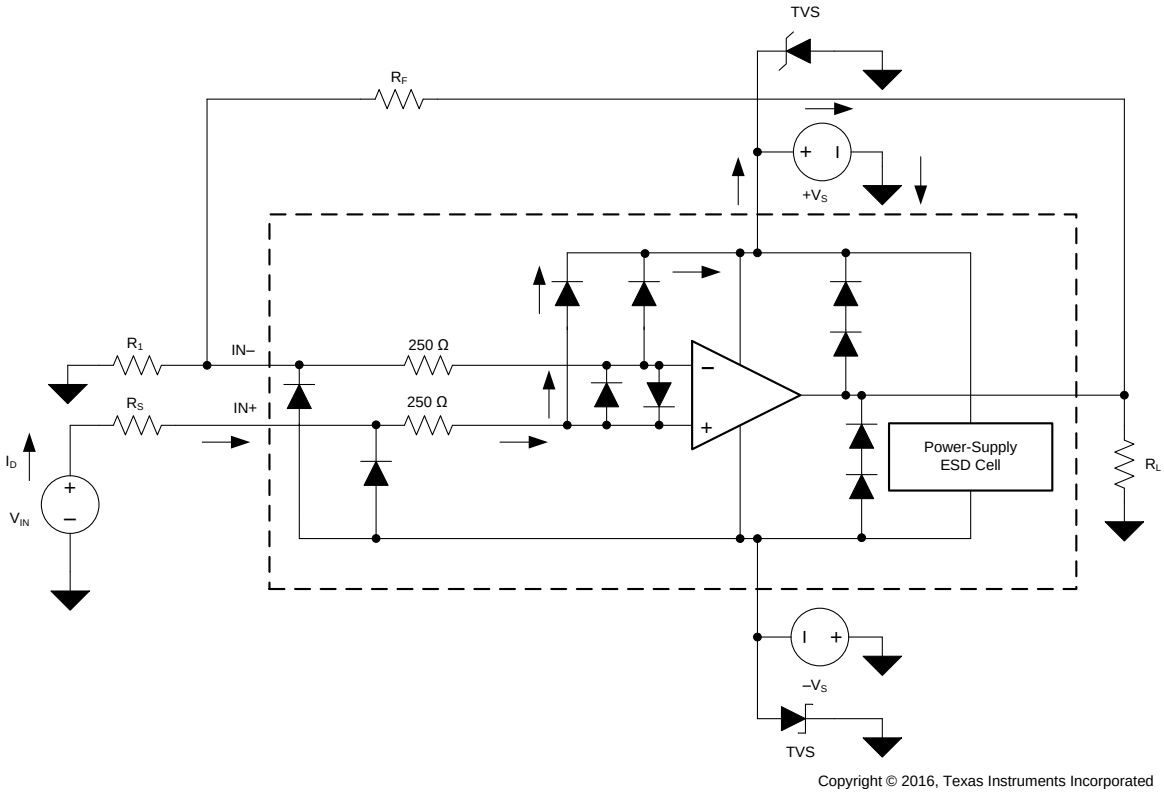
图 36. Pulsed Operation

7.3.3 Electrical Overstress

Designers typically ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 图 37 illustrates the ESD circuits contained in the OPA165x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (接下页)



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图 37. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. The absorption device activates depending on the path that the current takes. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA165x, but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (refer to 图 37), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

图 37 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} begins sourcing current to the operational amplifier, and then becomes the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the absolute maximum ratings of the operational amplifier.

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Feature Description (接下页)

Another common question explains what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. This depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are at low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see 图 37. Select the Zener voltage so the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin rises above the safe-operating, supply-voltage level.

7.4 Device Functional Modes

7.4.1 Operating Voltage

The OPA165x series op amps operate from ±2.25 V to ±18 V supplies while maintaining excellent performance. The OPA165x series can operate with as little as 4.5 V between the supplies and with up to 36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA165x series, power-supply voltages do not need to be equal. For example, the positive supply can be set to 25 V with the negative supply at –5 V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range of T_A = –40°C to +85°C. Parameters that vary significantly with operating voltage or temperature are shown in the *Typical Characteristics* section.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Noise Performance

图 38 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions).

The OPA165x (Gain bandwidth = 18 MHz, G = 1) is shown with total circuit noise calculated. The op amp contributes a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current, and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise typically dominates the total noise of the circuit. The voltage noise of the OPA165x series op amps makes the series a suitable choice for source impedances greater than or equal to 1-kΩ.

The equation in 图 38 shows the calculation of the total circuit noise, with these parameters:

- e_n = Voltage noise
- i_n = Current noise
- R_S = Source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = Temperature in Kelvins (K)

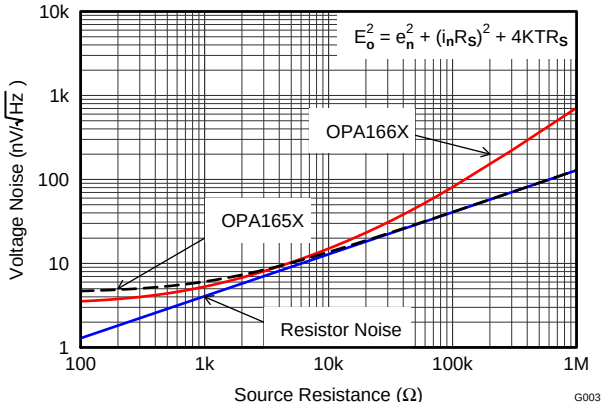


图 38. Noise Performance of the OPA165x in Unity-Gain Buffer Configuration

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

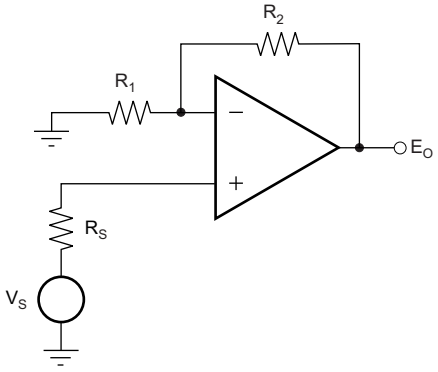
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. 图 38 plots this equation. The source impedance is typically fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

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Application Information (接下页)

图 39 illustrates both inverting (图 39 B) and noninverting (图 39 A) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors contribute noise. The current noise of the op amp reacts with the feedback resistors, creating additional noise components. The feedback resistor values can generally be selected to make these noise sources negligible. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

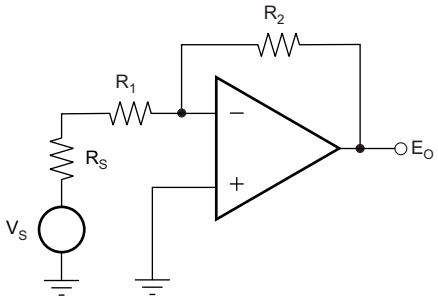
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + \left(\frac{R_2}{R_1}\right)^2 e_1^2 + e_2^2 + \left(1 + \frac{R_2}{R_1}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_1^2 + e_2^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

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Note: For the OPA165x series of op amps at 1 kHz, e_n = 4.5 nV/√Hz.

图 39. Noise Calculation in Gain Configurations

8.1.2 Total Harmonic Distortion Measurements

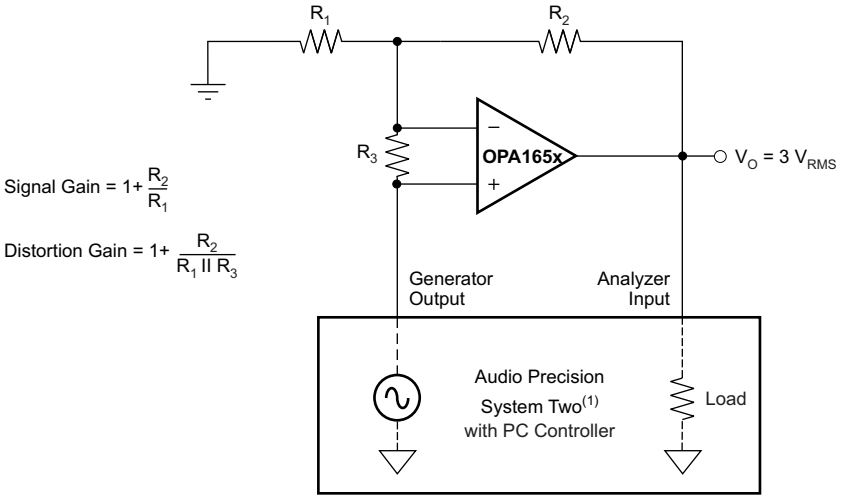
The OPA165x series op amps have excellent distortion characteristics. THD + noise is below 0.0002% (G = 1, V_O = 3 V_{RMS}, bandwidth = 80 kHz) throughout the audio frequency range, 20 Hz to 20 kHz, with a 2-kΩ load (see 图 7 for characteristic performance).

The distortion produced by the OPA165x series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as 图 40 shows) can extend the measurement capabilities.

Op amp distortion can be considered an internal error source that refers to the input. 图 40 shows a circuit that causes the op amp distortion to be gained up (refer to the table in 图 40 for the distortion gain factor for various signal gains). The addition of R_3 to the otherwise standard noninverting amplifier, configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the distortion gain factor reduces the feedback available for error connection, that extends the resolution by the same amount. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 must be kept small to minimize the effect on the distortion measurements.

Application Information (接下页)

The validity of this technique can be verified by duplicating measurements at high gain or high frequency where the distortion is within the measurement capability of the test equipment. The Audio Precision System Two distortion and noise analyzer calculated the measurements for this data sheet, which significantly simplifies repetitive measurements. Manual distortion measurement instruments performs this measurement technique.



SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
+1	101	∞	1 kΩ	10 Ω
–1	101	4.99 kΩ	4.99 kΩ	49.9 Ω
+10	110	549 Ω	4.99 kΩ	49.9 Ω

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(1) For measurement bandwidth, see 图 7 through 图 12.

图 40. Distortion Test Circuit

8.1.3 Capacitive Loads

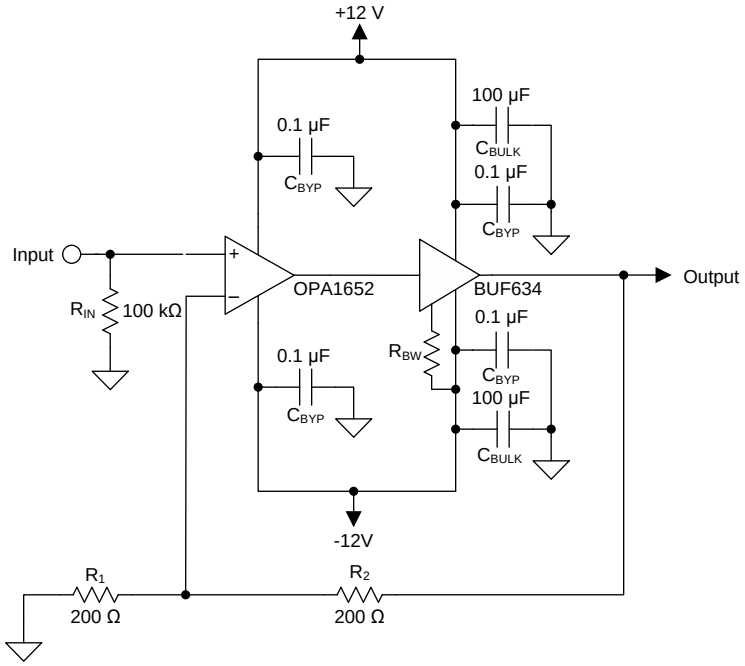
The dynamic characteristics of the OPA1652 and OPA1654 are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_S equal to 50 Ω, for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device becomes shorted. 图 19 illustrates a graph of *Small-Signal Overshoot vs Capacitive Load* for several values of R_S. For more details about analysis techniques and application circuits, see *Feedback Plots Define Op Amp AC Performance* (SBOA015), available for download from the TI website (www.ti.com).

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8.2 Typical Application

The low noise and distortion of the OPA165x family of audio operational amplifiers make them an excellent choice for a number of analog audio circuits. 图 41 illustrates a power amplifier circuit suitable for high-fidelity headphone applications.



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图 41. Composite Power Amplifier for Headphones

8.2.1 Design Requirements

- Gain: 6 dB
- Output Voltage: > 2 V_{RMS}, 32-Ω Load
- Output Impedance: < 1 Ω
- THD+N: < –110dB (1 kHz, 2 V_{RMS}, 32-Ω Load)

8.2.2 Detailed Design Procedure

The power amplifier circuit (single channel shown) features a BUF634 high-speed buffer amplifier inside the feedback loop of an OPA1652 to increase the amount of available output current. The bandwidth and power consumption of the BUF634 can be set with an external resistor (R_{BW}). For this circuit, R_{BW} uses a 0-Ω resistor that configures the BUF634 for the widest bandwidth and highest performance. Feedback resistors R_1 and R_2 (as shown in 公式 1) calculate the gain of the circuit:

$$A_V = 1 + \frac{R_2}{R_1} \tag{1}$$

To achieve the design goal of a 6-dB voltage gain (2 V/V), R_1 and R_2 must have equal values. These resistors also contribute noise thermal noise to the circuit. The voltage noise spectral density of the feedback resistors, referred to the amplifier input, is given in 公式 2:

$$e_{NR} = \sqrt{4kT\left(R_2 \,||\, R_1\right)} \tag{2}$$

Ideally, the thermal noise contributions of the resistors do not significantly degrade the noise performance of the circuit. Selecting resistor values so the resistor noise is less than one-third the input voltage noise of the op amp (公式 3) ensures that any increase in the circuit noise as a result of the feedback resistor contributions is minimal.

Typical Application (接下页)

$$e_{NR} \le \frac{e_{OA}}{3} \tag{3}$$

To calculate the required resistor values, 公式 3 is inserted into 公式 2, and the resulting equation is rearranged to solve for the parallel combination of R_1 and R_2 , as shown in 公式 4. Using a value of 3.8 nV/√Hz as the broadband voltage noise of the OPA1652 results in a value of 96.8 Ω for the parallel combination of R_1 and R_2. R_1 and R_2 use standard value 200-Ω resistors, resulting in a parallel value of 100 Ω, which is suitably close to the required value.

$$R_1 || R_2 \le \frac{{e_{OA}}^2}{36kT} \le \frac{\left(3.8\ nV/\sqrt{Hz}\right)^2}{36 \times 1.381 \times 10^{-23} \times 300} \le 96.8\ \Omega \tag{4}$$

Because of the extremely wide bandwidth and high slew rate of the BUF634, no additional components are required to maintain stability in the circuit or prevent latch-up conditions. This circuit is stable with capacitive loads over 1-nF, which is suitable for headphone applications.

8.2.3 Application Curves

The measured performance of the circuit is shown in 图 42 through 图 46. The frequency response is extremely flat over the full audio bandwidth, deviating only 0.004 dB over the audible range. The decrease in gain shown at low frequency is a result of the test equipment, and not the amplifier circuit. The amplifier output impedance, calculated from the change in gain in the loaded and unloaded conditions, is 0.036 Ω. The maximum output power (before clipping) is displayed in 图 43. For a 32-Ω load, the power amplifier delivered 781 mW before clipping. The best THD+N performance achieved with a 32-Ω load was –117.2 dB at 678 mW (1 kHz, 22-kHz measurement bandwidth). THD+N vs frequency is shown in 图 44 for a 2-V_{RMS} output level measured in a 90-kHz bandwidth. The worst-case measurement was for a 16-Ω load (250 mW), 20-kHz input frequency, –91.8 dB (0.0026%). The amplifier output spectrum for a 2-V_{RMS}, 1 kHz, fundamental into two different loads is shown in 图 45 and 图 46. All distortion harmonics are below –120 dB relative to the fundamental for both loading conditions.

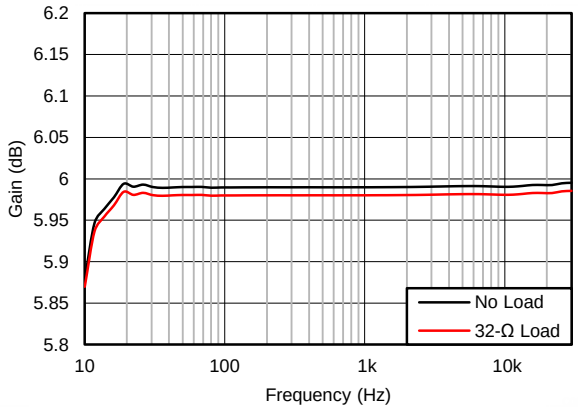


图 42. Amplifier Transfer Function

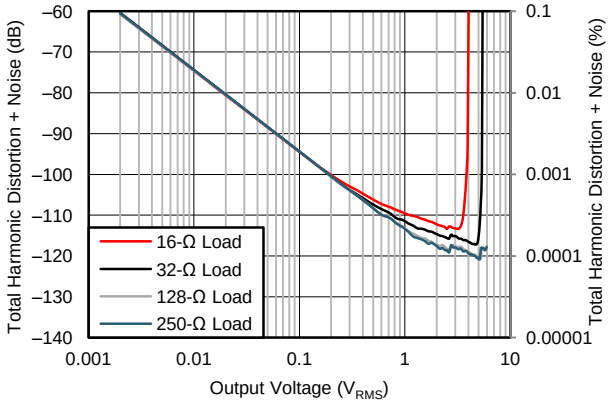
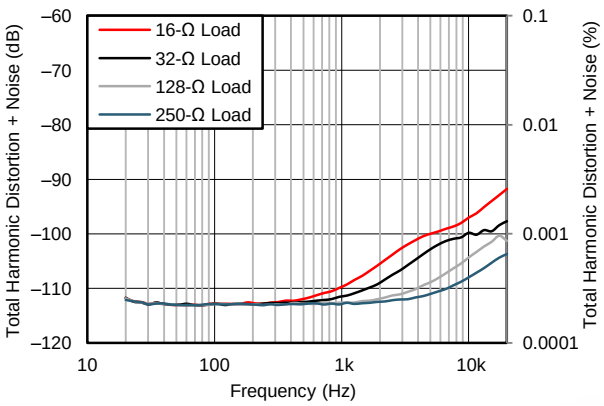


图 43. THD+N vs Frequency for Various Loads

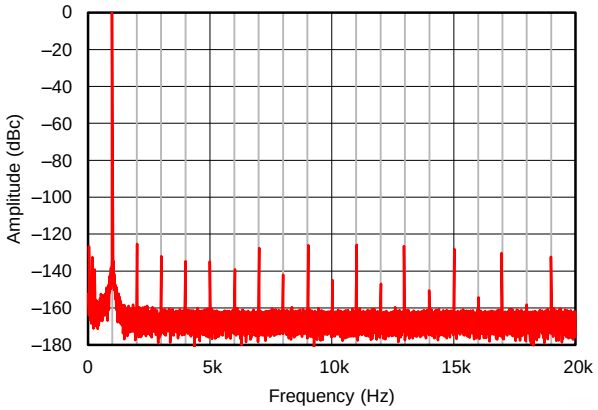
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Typical Application (接下页)



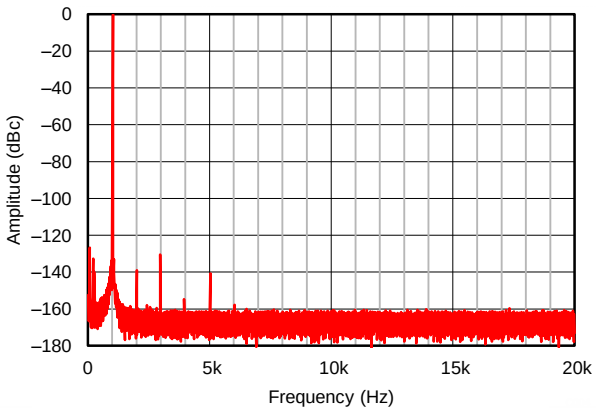
90-kHz measurement bandwidth, 2-V_{RMS} output

图 44. THD+N vs Frequency for Various Loads



1 kHz, 32-Ω load, 2-V_{RMS} output

图 45. Output Spectrum



1 kHz, 250-Ω load, 2 V_{RMS}

图 46. Output Spectrum

9 Power Supply Recommendations

The OPA165x series is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

10 Layout

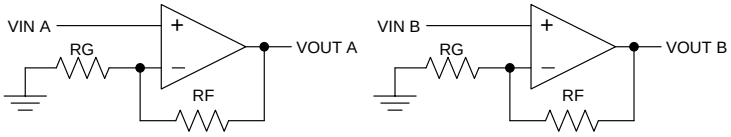
10.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Physically separate digital and analog grounds, observing the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 图 47, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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10.2 Layout Example



(Schematic Representation)

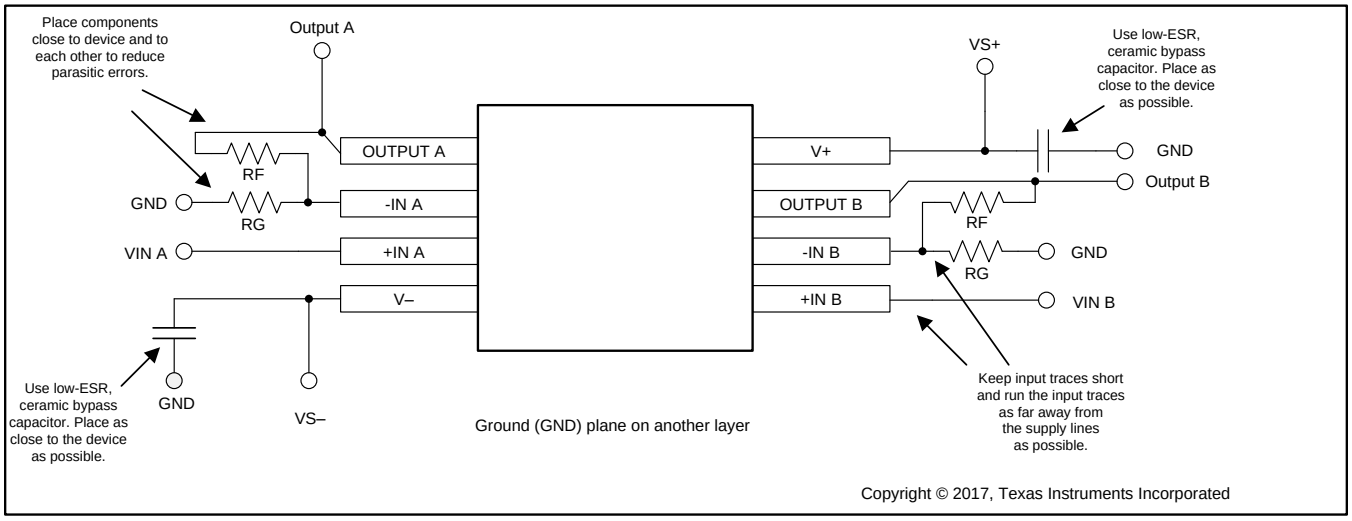


图 47. Operational Amplifier Board Layout for Noninverting Configuration

10.3 Power Dissipation

The OPA1652 and OPA1654 series op amps are capable of driving 2-kΩ loads with a power-supply voltage up to ±18 V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA165x series op amps improves heat dissipation compared to conventional materials. Circuit board layout minimizes junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise is further minimized by soldering the devices to the circuit board rather than using a socket.

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。 TINA-TI™ 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析以及其他设计功能。

TINA-TI 可从 WEBENCH® 设计中心免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 DIP 适配器 EVM

DIP 适配器 EVM 工具提供了一种针对小型表面贴装器件进行原型设计的简易低成本方法。评估工具适用于以下 TI 封装：D 或 U (SOIC-8)、PW (TSSOP-8)、DGK (VSSOP-8)、DBV（SOT23-6、SOT23-5 和 SOT23-3）、DCK（SC70-6 和 SC70-5）以及 DRL (SOT563-6)。DIP 适配器 EVM 也可搭配引脚排使用或直接与现有电路相连。

11.1.1.3 通用运算放大器评估模块 (EVM)

通用运放 EVM 是一系列通用空白电路板，可简化采用各种 IC 封装类型的电路板原型设计。借助评估模块电路板设计，可以轻松快速地构造多种不同电路。共有 5 个模型可供选用，每个模型都对应一种特定封装类型。支持 PDIP、SOIC、VSSOP、TSSOP 和 SOT-23 封装。

注

这些电路板均为空白电路板，用户必须自行提供相关器件。TI 建议您在订购通用运算放大器 EVM 时申请几个运算放大器器件样品。

11.1.1.4 智能放大器扬声器特性鉴定板评估模块

智能放大器扬声器特性鉴定板，与支持的 TI 智能放大器和 PurePath 控制台软件配合使用时，用户可测量扬声器偏移、温度和其它参数以便与 TI 智能放大器产品配合使用。

11.1.1.5 TI 高精度设计

TI 高精度设计的模拟设计方案是由 TI 公司高精度模拟实验室设计 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。

11.1.1.6 WEBENCH®滤波器设计器

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。借助WEBENCH 滤波设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源组件来打造最佳滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® 滤波器设计器。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

11.2 文档支持

11.2.1 相关文档

使用 OPA165x 时，建议参考下列相关文档。可从 www.ti.com 下载，除非另外注明。

- *《OPA1652 和 OPA1654 EMIR 抗干扰性能》*（文献编号：SBOT007）

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文档支持 (接下页)

- 《放大器源阻抗和噪声的注意事项》（文献编号：SLYT470）
- 《运算放大器的单电源运行》（文献编号：SBOA059）
- 《运算放大器性能分析》（文献编号：SBOA054）
- 《直观补偿互阻抗放大器》（文献编号：SBOA055）
- 《调整放大器》（文献编号：SBOA067）
- 《反馈曲线图定义运算放大器交流性能》（文献编号：SBOA015）
- 《专业音频的有源音量控制》（文献编号：TIDU034）

11.3 相关链接

表 1 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **1.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
OPA1652	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA1654	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.6 商标

TINA-TI, E2E are trademarks of Texas Instruments.
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WEBENCH is a registered trademark of Texas Instruments.
蓝光(Blu-Ray) is a trademark of Blu-Ray Disc Association.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA1652AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OUPI
OPA1652AIDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OUPI
OPA1652AIDGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OUPI
OPA1652AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OUPI
OPA1652AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OUPI
OPA1652AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OUPI
OPA1652AIDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OUPI
OPA1652AIDGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OUPI
OPA1652AIDGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OUPI
OPA1652AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDRGR.A	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDRGR.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDRGT.A	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1652AIDRGT.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652
OPA1654AID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654
OPA1654AID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654
OPA1654AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654
OPA1654AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA1654AIDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654
OPA1654AIDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654
OPA1654AIPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654
OPA1654AIPW.A	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654
OPA1654AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654
OPA1654AIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654
OPA1654AIPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654
OPA1654AIPWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

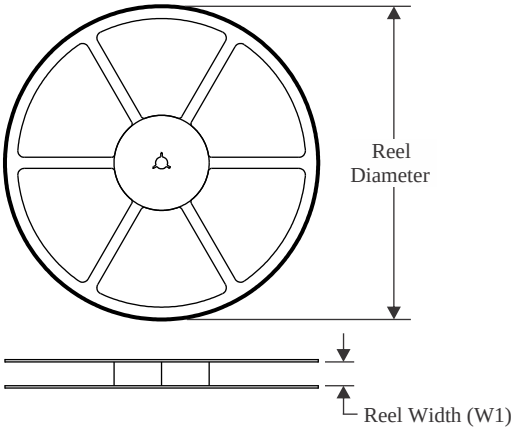
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

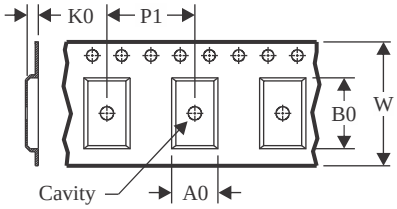
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

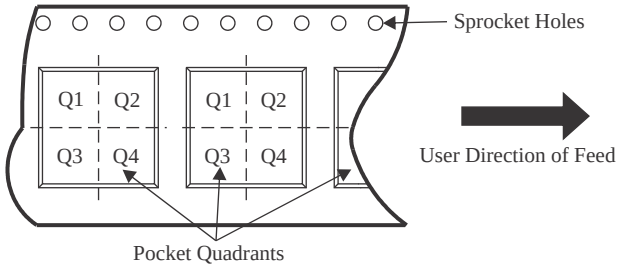


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

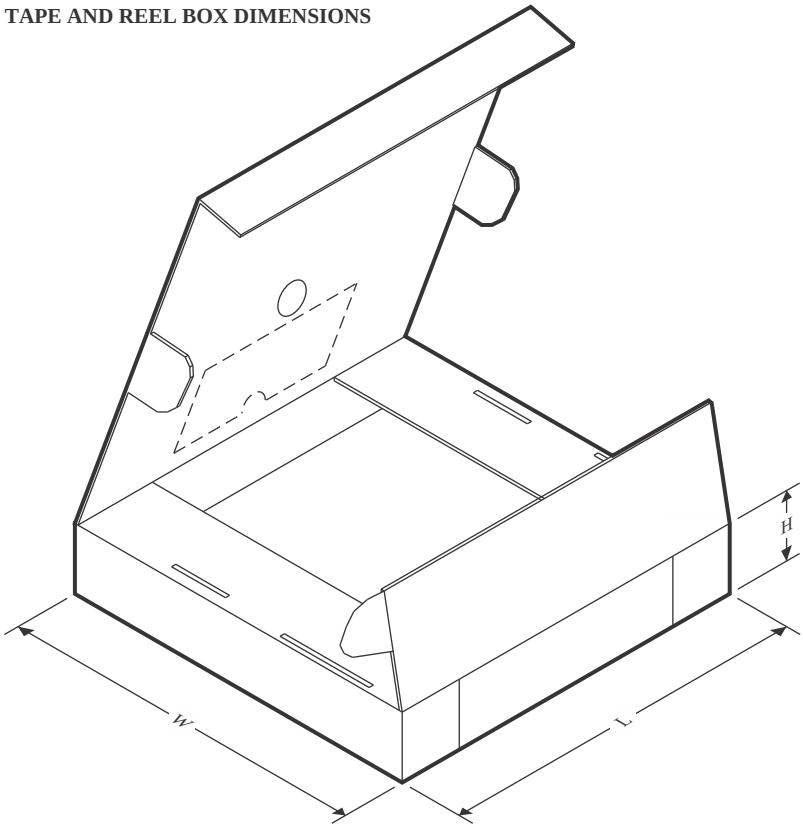
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1652AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA1652AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1652AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1652AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1652AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1652AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA1652AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA1654AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA1654AIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA1654AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA1654AIPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

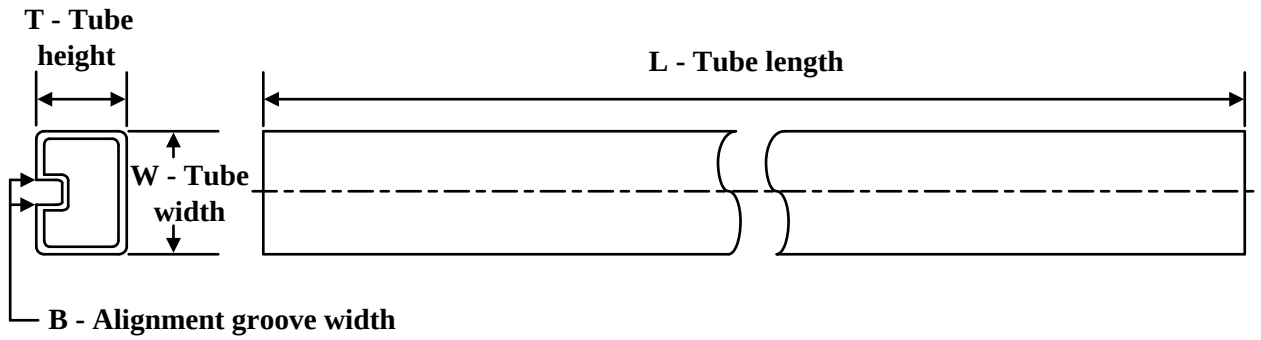
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1652AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA1652AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA1652AIDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA1652AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA1652AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA1652AIDRGR	SON	DRG	8	3000	346.0	346.0	33.0
OPA1652AIDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA1654AIDR	SOIC	D	14	2500	353.0	353.0	32.0
OPA1654AIDRG4	SOIC	D	14	2500	353.0	353.0	32.0
OPA1654AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
OPA1654AIPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

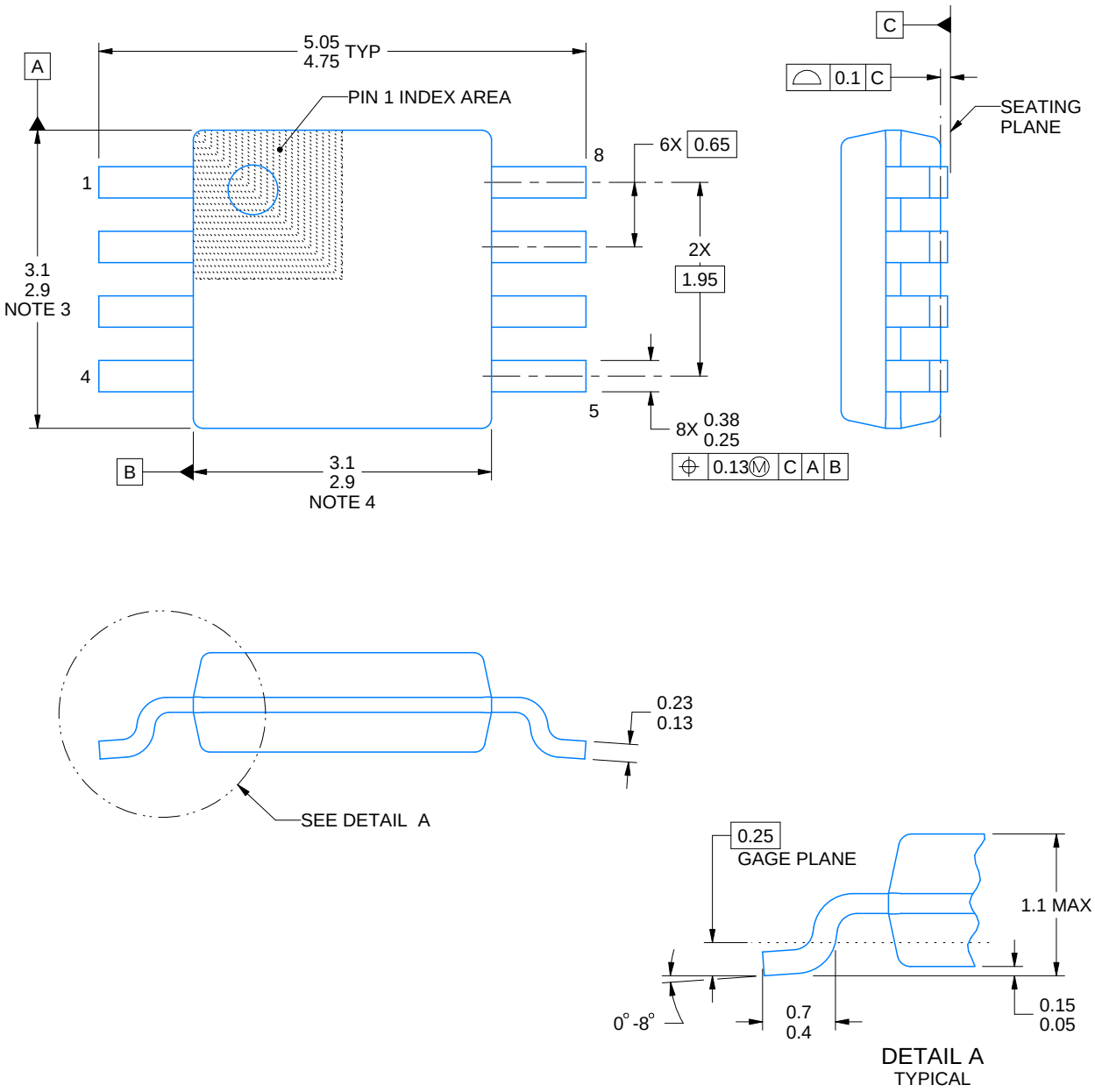
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA1652AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA1652AID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA1652AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA1652AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA1652AIDGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA1652AIDGK.B	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA1654AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA1654AID.A	D	SOIC	14	50	506.6	8	3940	4.32
OPA1654AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5
OPA1654AIPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

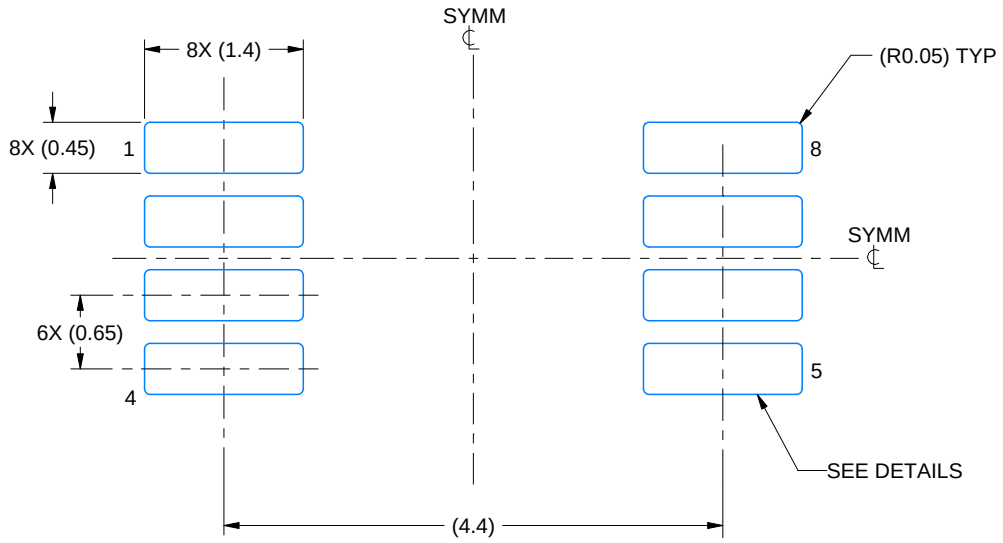
SMALL OUTLINE PACKAGE



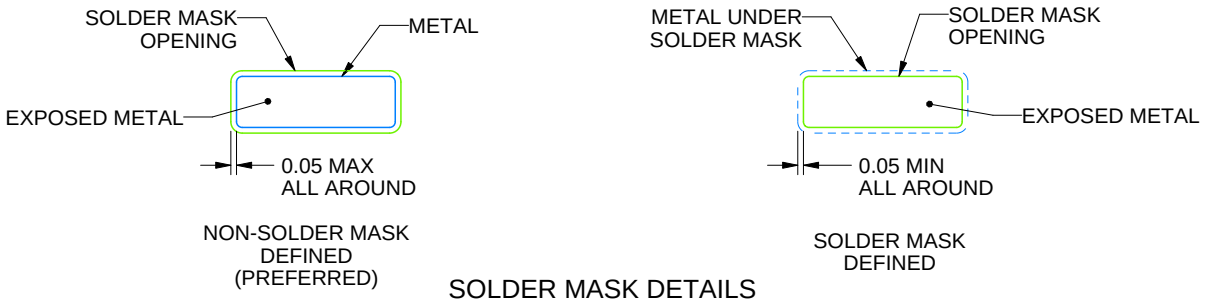
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

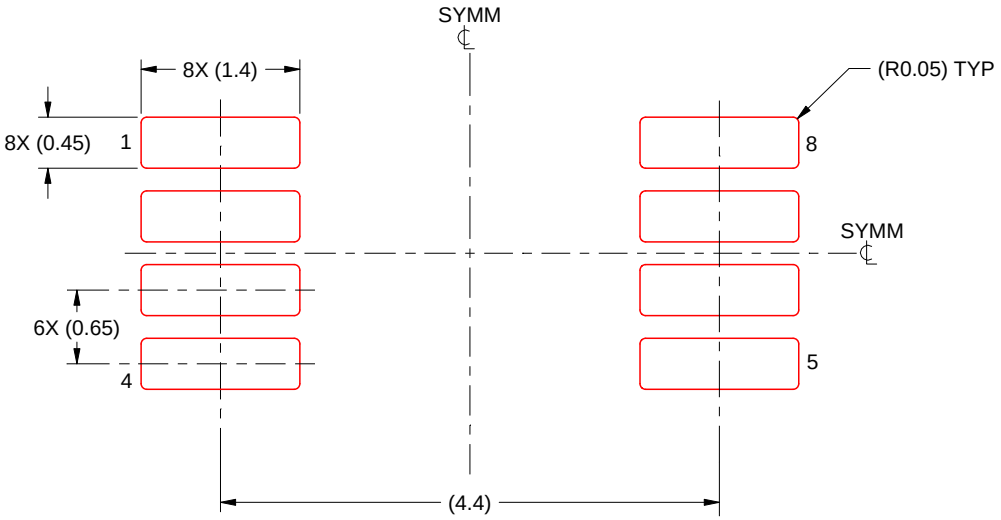


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

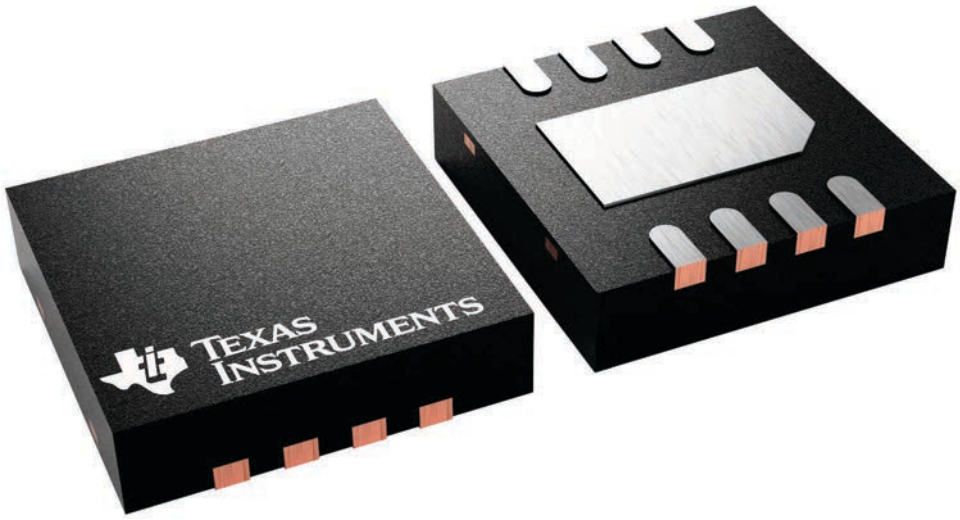
DRG 8

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



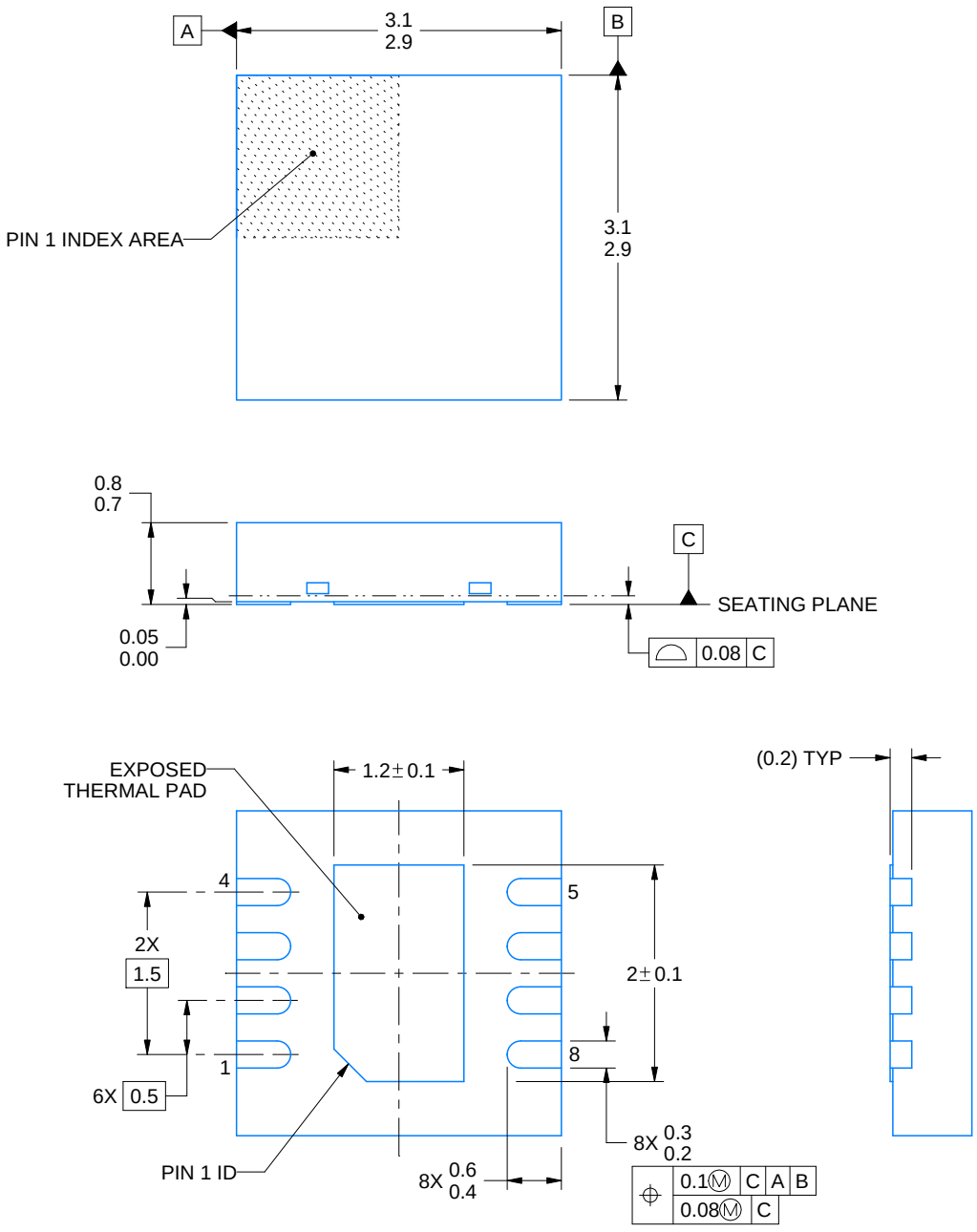
4225794/A

PACKAGE OUTLINE

DRG0008A

WSON - 0.8 mm max height

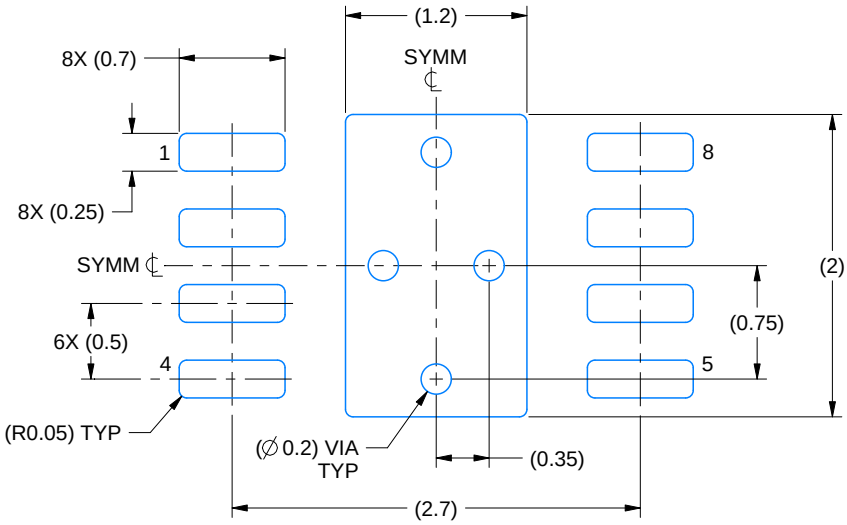
PLASTIC SMALL OUTLINE - NO LEAD



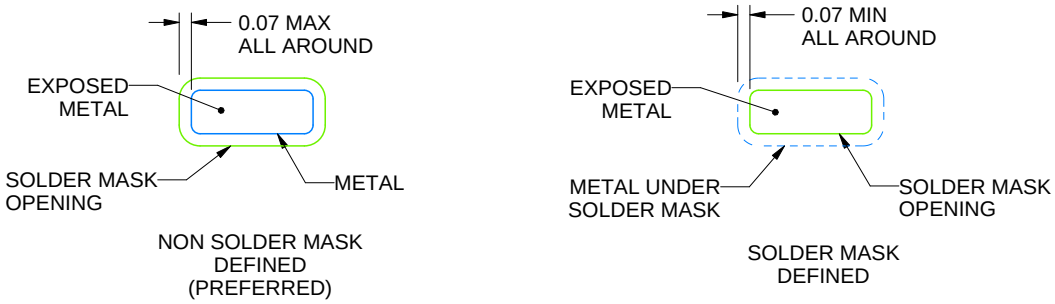
4218885/A 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

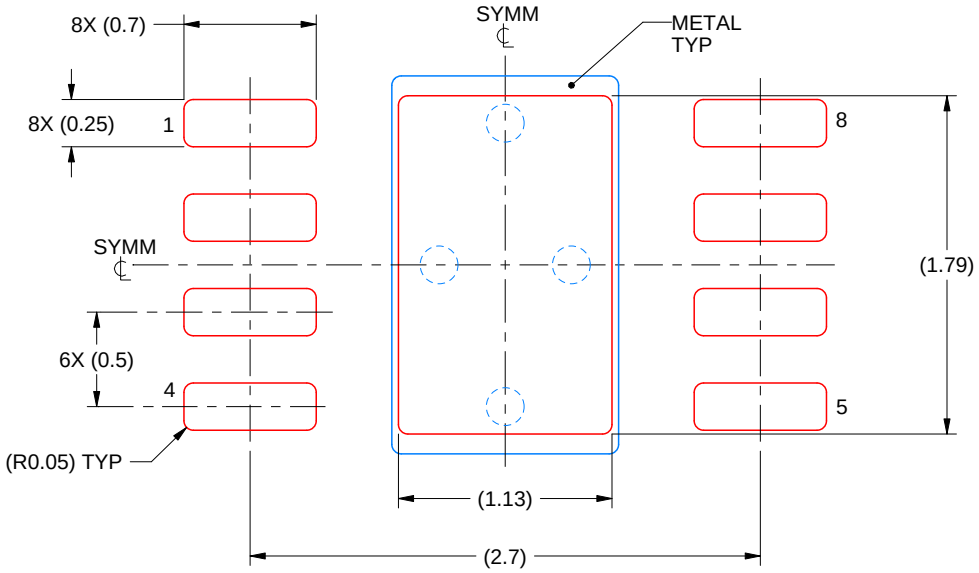


SOLDER MASK DETAILS

4218885/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



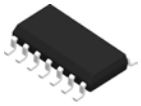
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

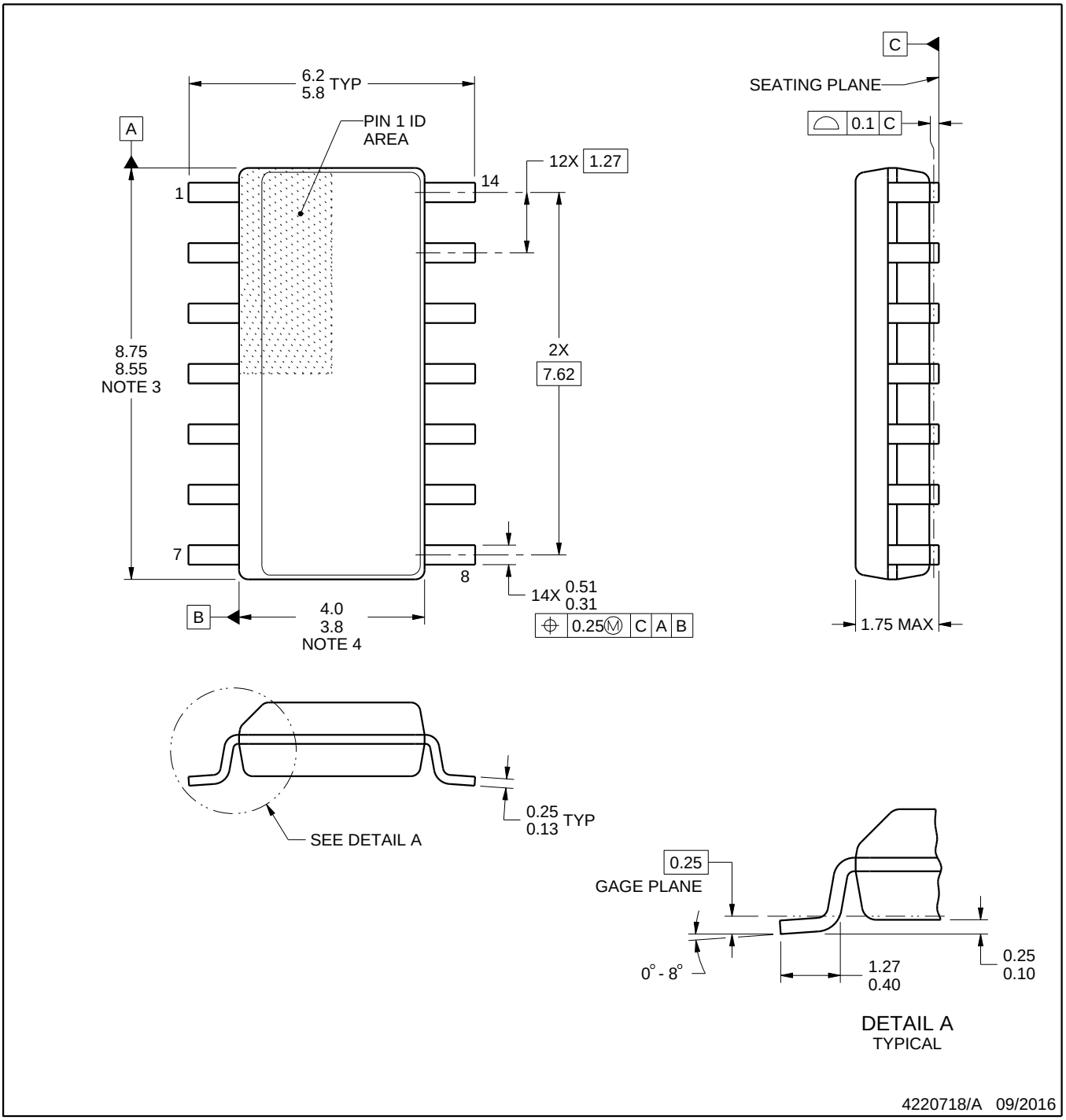


PACKAGE OUTLINE

D0014A

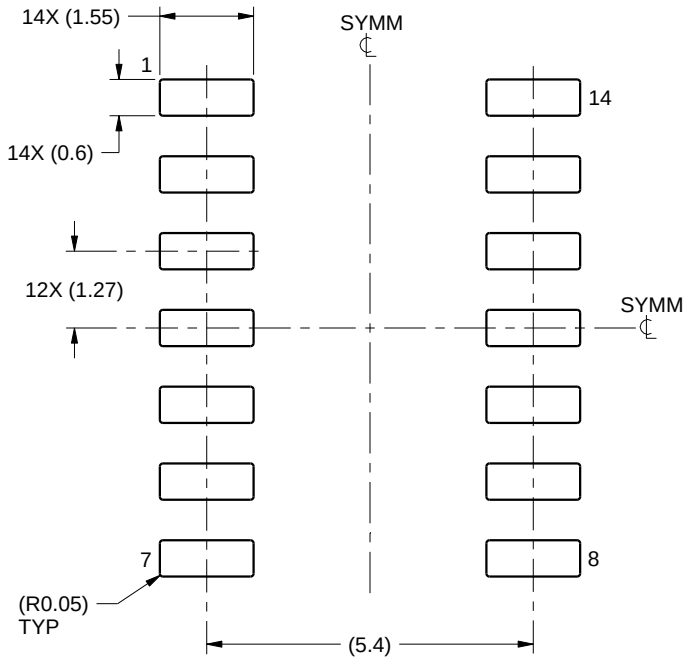
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

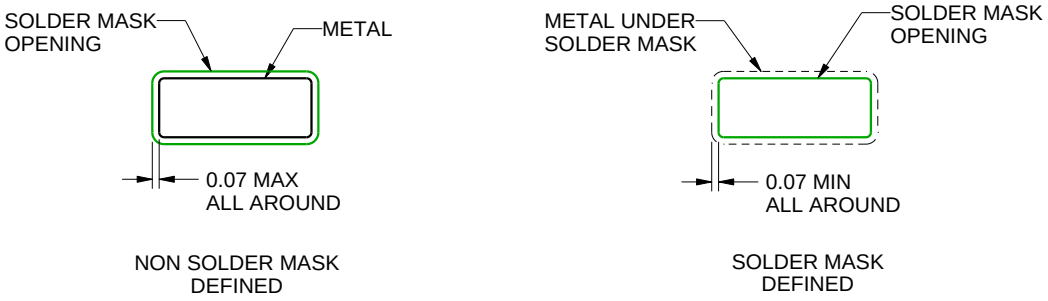


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

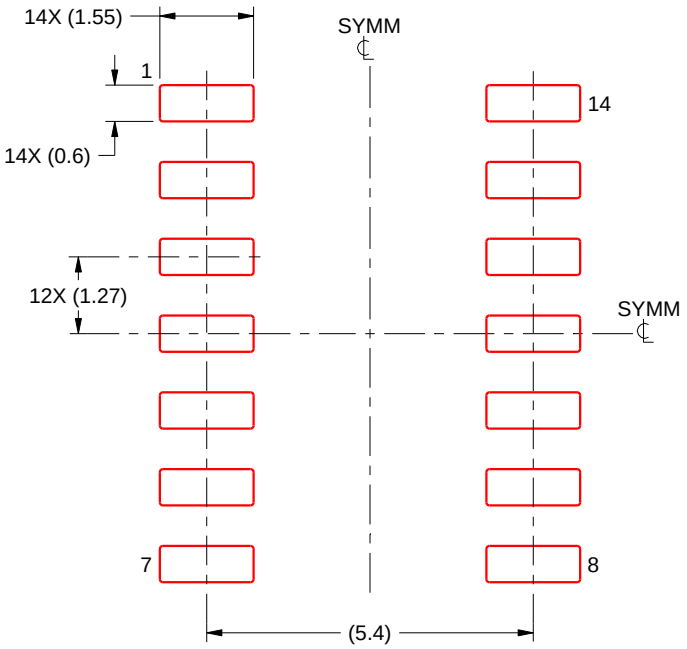
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

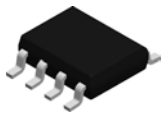


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

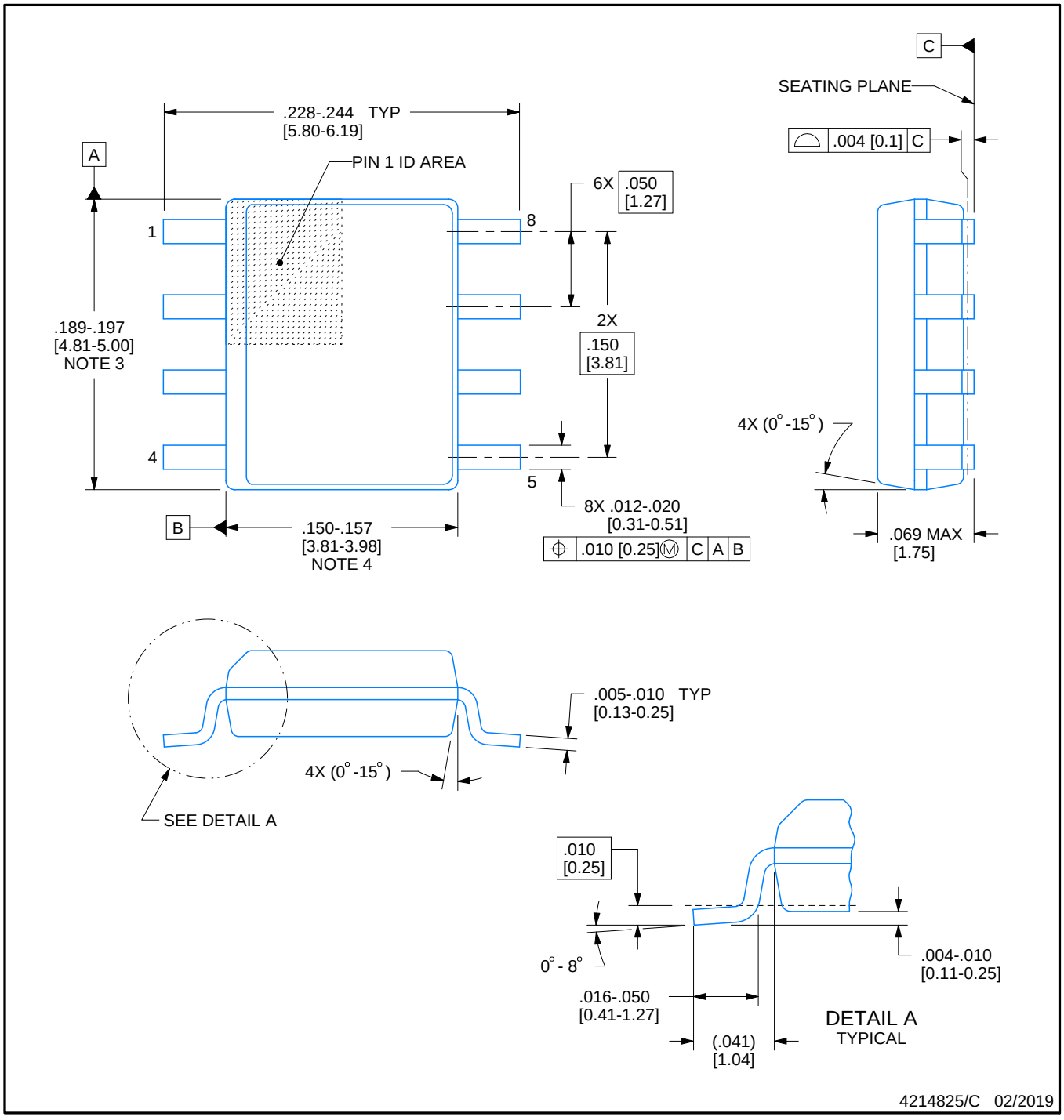


PACKAGE OUTLINE

D0008A

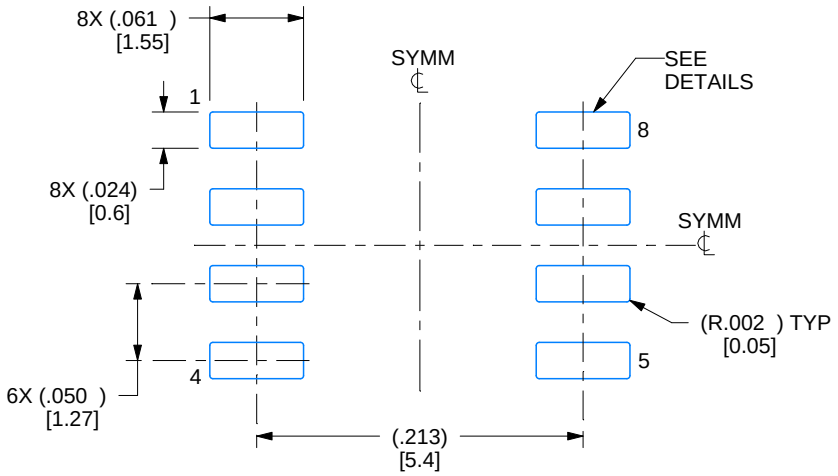
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

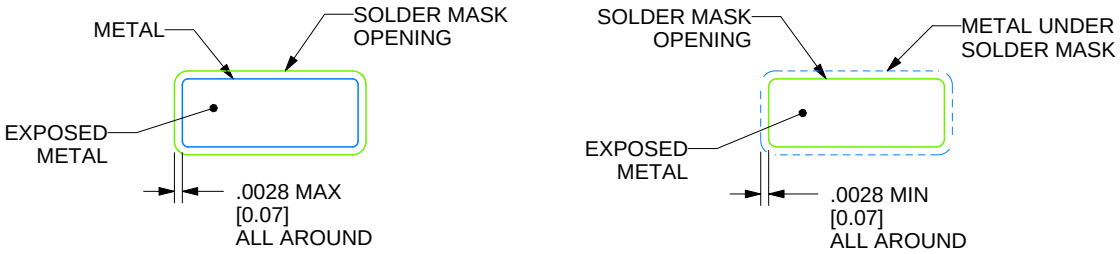


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

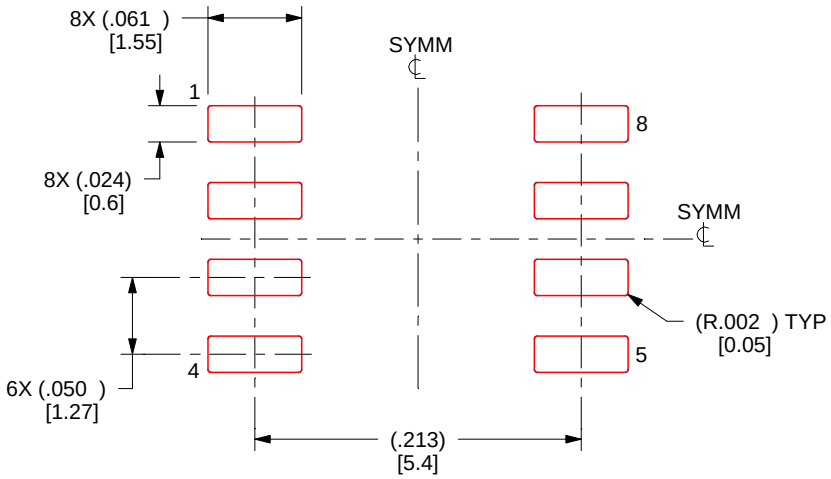
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

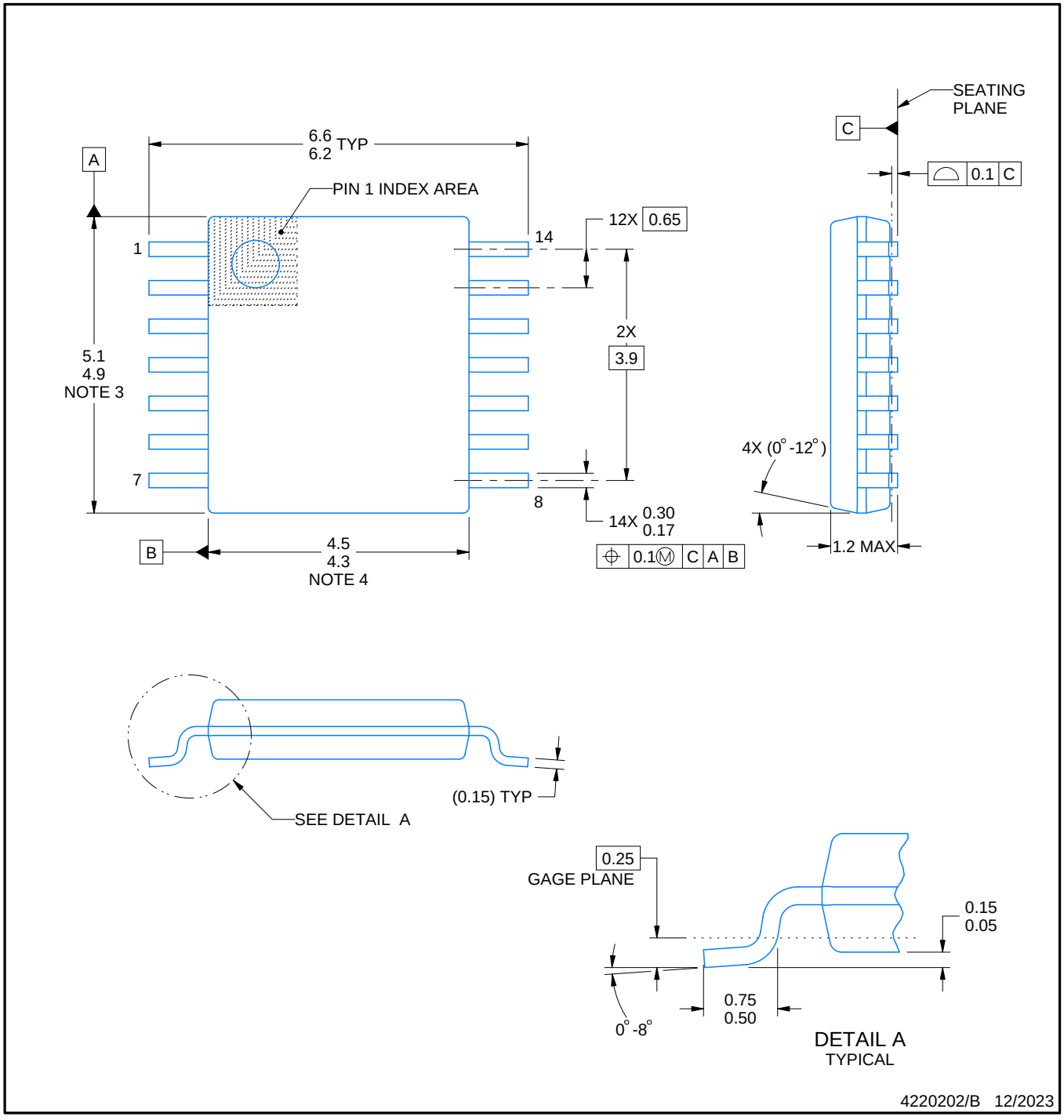
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

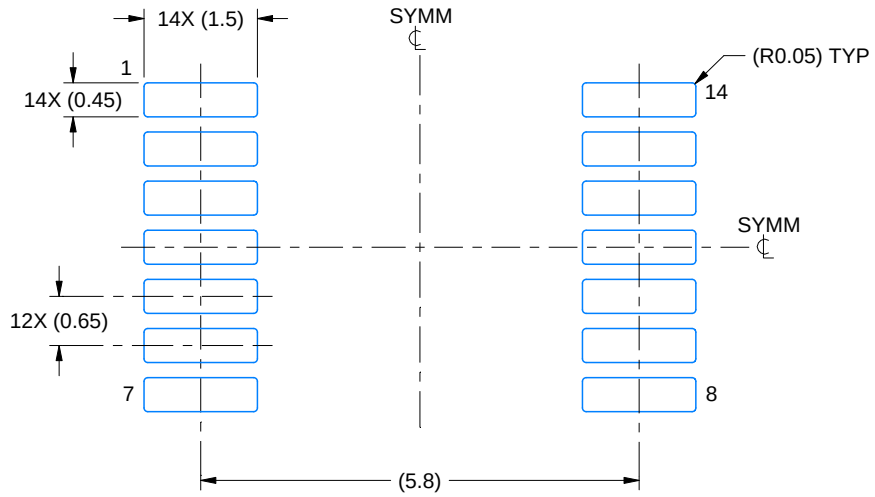
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

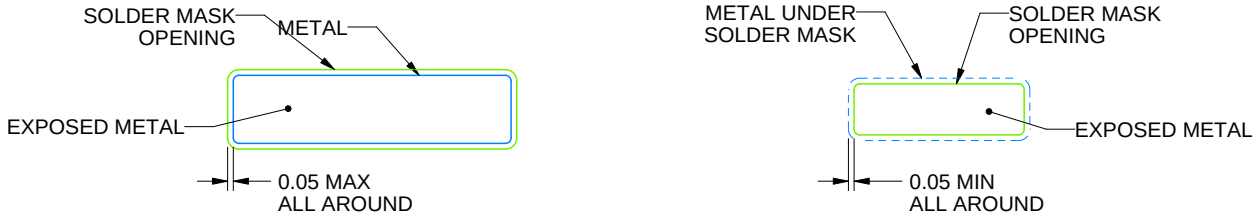


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

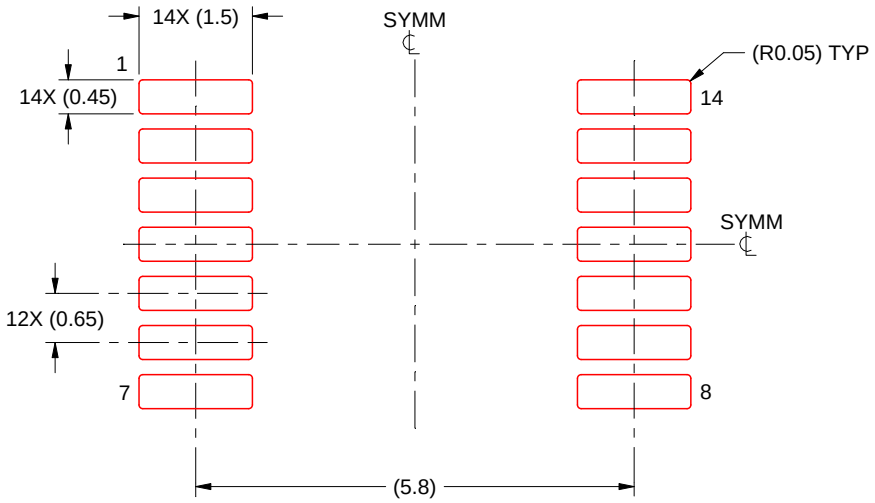


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月