20W Full-Bridge Power Stage for High-Integrated, High-Efficiency Wireless Power Transmitter

1 Descriptions

The SC5003 is a highly integrated wireless power transmitter analog front end that contains all of the analog components required to implement a WPC compliant transmitter. The SC5003 integrates a full-bridge power driver with MOSFETs, current sense amplifier, bootstrap circuit, communication demodulator and protection circuit. The SC5003 can work with transmitter controller together to create a high-performance wireless power transmitter that complies with both the WPC V1.2.4 Extended Power Profile (EPP) and Baseline Power Profile (BPP).

The system supports foreign object detection (FOD) by continuously monitoring the amount of power transferred and comparing that to the amount of received power, as reported by the receiver. In order to do this, the SC5003 measures the input DC current very accurately using a current sense amplifier. Besides, the SC5003 also supports input under-voltage lockout (UVLO), input over-voltage protection (OVLO), over-current protection (OCP) and over-temperature protection (OTP).

The SC5003 is available in a compact 4 x 4 mm QFN package.

2 Features

- Support 1V to 20V full bridge input voltage range
- Support 4V to 20V AVIN input voltage range
- Support up to 20W output power
- Integrated four low Rdson power FETs
- Integrated FET driver and bootstrap circuit
- Integrated 5V/200mA buck regulator
- Integrated voltage and current demodulation
- Integrated accurate current sense for FOD
- Integrated Q factor detection
- Single-wire digital interface
- UVLO/OVLO/OCP/OTP
- 4mm x 4mm QFN package

3 Applications

- WPC Compliant Wireless Power Transmitter
- Proprietary Wireless Chargers and Transmitter

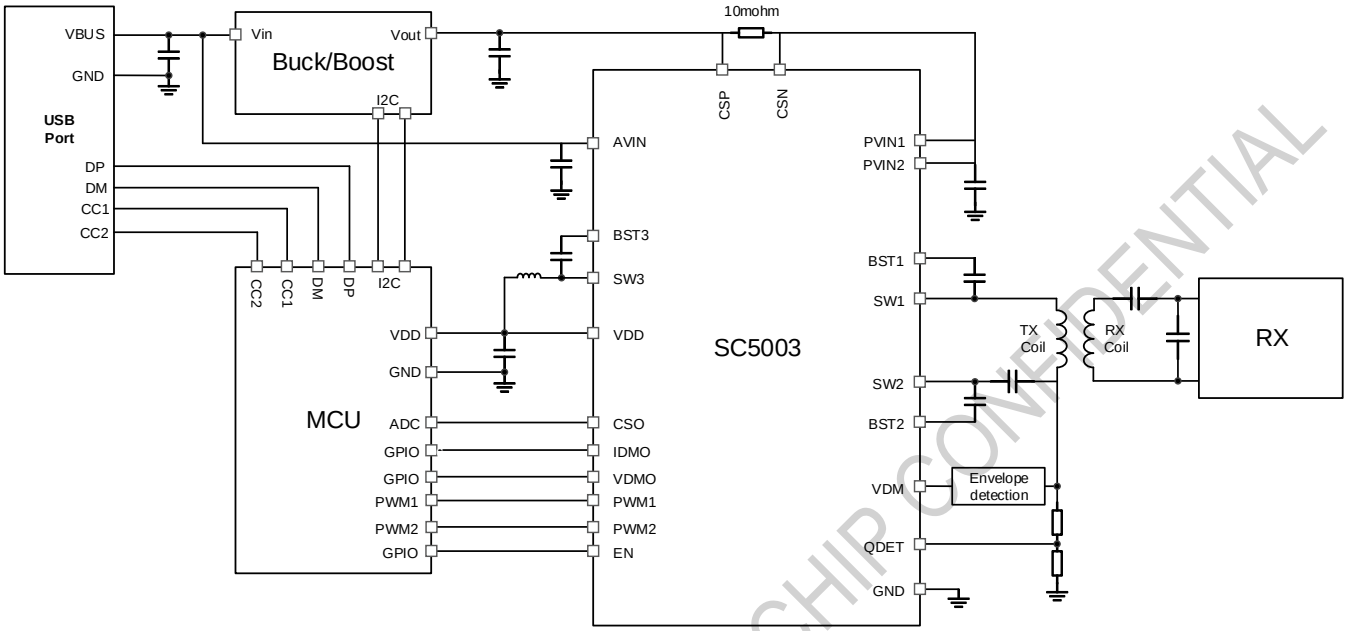
4 Device Information

Part Number	Package	Dimension
SC5003QFER	FCQFN21L	4mm x 4mm x0.75mm

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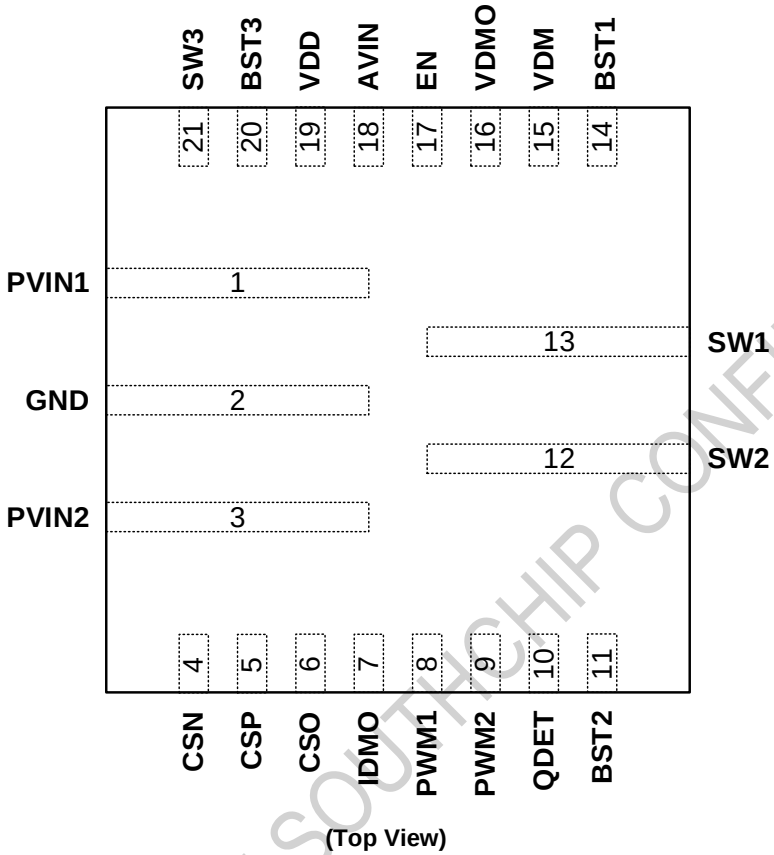
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5 Typical Application Circuit



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6 Terminal Configuration and Functions



(Top View)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	PVIN1	I	Input voltage for half-bridge MOSFET. Bypass with a 22µF ceramic capacitor to GND.
2	GND	PWR	Power ground.
3	PVIN2	I	Input voltage for half-bridge MOSFET. Bypass with a 22µF ceramic capacitor to GND.
4	CSN	I	Input current sense amplifier negative input
5	CSP	I	Input current sense amplifier positive input
6	CSO	O	Current sense amplifier output.
7	IDMO	O	Output of the demodulated 2-kHz communication signal based on current demodulation scheme.
8	PWM1	I	PWM logic input for the Q1 and Q2 as shown in the Block Diagram. Logic HIGH turns on the high-side FET Q1, and turns off the low-side FET Q2. Logic LOW turns on the low-side FET Q2 and turns off the high-side FET Q1
9	PWM2	I	PWM logic input for the Q3 and Q4 as shown in the Block Diagram. Logic HIGH turns on the high-

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			side FET Q3, and turns off the low-side FET Q4. Logic LOW turns on the low-side FET Q4 and turns off the high-side FET Q3
10	QDET	I	Quality factor detection input
11	BST2	I/O	Connect a 0.1 µF capacitor between BST2 and SW2 to bootstrap a voltage to provide the bias for high side MOSFET driver
12	SW2	O	Switch node of the half-bridge MOSFET.
13	SW1	O	Switch node of the half-bridge MOSFET.
14	BST1	I/O	Connect a 0.1 µF capacitor between BST1 and SW1 to bootstrap a voltage to provide the bias for high side MOSFET driver.
15	VDM	I	High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation.
16	VDMO	O	Output of the demodulated 2-kHz communication signal based on voltage demodulation scheme.
17	EN	I	Enable pin. Logic LOW disables the IC. Logic HIGH enables the IC.
18	AVIN	PWR	Input voltage for internal buck converter, Bypass with a 10 µF ceramic capacitor to GND.
19	VDD	I	Input power supply to internal gate drivers and control circuits. Connect a 1 µF ceramic capacitor from VDD to GND.
20	BST3	I	Connect a 0.1 µF capacitor between BST3 and SW3 to bootstrap a voltage to provide the bias for high side MOSFET driver.
21	SW3	I	Switch node of the buck converter.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	AVIN, PVIN1, PVIN2, SW1, SW2, SW3, CSP, CSN	-0.3	22	V
	PWM1, PWM2, CSO, QDET, VDM, VDMO, IDMO, VDD, EN	-0.3	6.5	V
	BST1, BST2, BST3	-0.3	SW+5	V
Temperature Range	Operating Junction, T_J	-40	125	°C
	Storage temperature range, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE(1)		QFN-21 (4mm x 4mm)	UNIT
Θ_{JA}	Junction to ambient thermal resistance	44	°C/W
Θ_{JC}	Junction to case resistance	8	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage(2)	-2000	2000	V
	Charged device model (CDM) ESD stress voltage (3)	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{PVIN1}, V_{PVIN2}	Input voltage range for full bridge	2		20	V
V_{AVIN}	Input voltage range for internal buck converter	4		20	V
C_{AVIN}, C_{PVIN1}, C_{PVIN2}	AVIN, PVIN1, PVIN2 Ceramic Capacitor		22		µF
C_{VDD}	VDD Ceramic Capacitor		1		µF
T_J	Operating junction temperature	-40		125	°C

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7.5 Electrical Characteristic

T_J= 25°C and V_{AVIN} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{AVIN}	Operating voltage		4		20	V
V_{AVIN_UVLO}	AVIN under-voltage lockout threshold	Rising edge		3.8		V
		Falling edge		3.6		V
V_{DD_UVLO}	VDD under-voltage lockout threshold	Rising edge		3.6		V
		Falling edge		3.45		V
V_{IN_OVLO}	PVIN over-voltage lockout threshold	Rising edge		22		V
		Falling edge		20.5		V
Iq	Quiescent current	EN =low (3.8V LDO is alive)			65	μA
VDD CONVERTER						
V_{DD_LDO}				3.8		V
I_{VDD_LIM}			20			mA
BUCK CONVERTER						
V_{DD_BUCK}	Output voltage	V_{AVIN} = 20V, I_{VDD} =200mA	4.8	5	5.2	V
		Trim option		4.6		V
I_{LIM}	High side MOSFET peak current limit			0.7		A
F_{sw}				1.2		Mhz
$R_{DS(on)}$	High side	V_{DD} = 5.0V		400		mΩ
	Low side	V_{DD} = 5.0V		240		mΩ
CURRENT SENSE AMPLIFIER						
G	Gain	R_{SENSE}=20mohm	0.98	1	1.02	V/A
		R_{SENSE}=10mohm	0.98	1	1.02	V/A
		R_{SENSE}=5mohm	0.97	1	1.03	V/A
V_{OO}	CSO output offset voltage	V_{CSP}=V_{CSN}, R_{SENSE}=20mohm		0.25		V
		V_{CSP}=V_{CSN}, R_{SENSE}=10mohm		0.5		
		V_{CSP}=V_{CSN}, R_{SENSE}=5mohm		1		V
POWER SWITCH						
$R_{DS(on)}$	SW1 High-side $R_{DS(on)}$	V_{DD} = 5.0V		14		mΩ
	SW1 Low-side $R_{DS(on)}$	V_{DD} = 5.0V		14		mΩ
	SW2 High-side $R_{DS(on)}$	V_{DD} = 5.0V		14		mΩ
	SW2 Low-side $R_{DS(on)}$	V_{DD} = 5.0V		14		mΩ
SHORT CIRCUIT PROTECTION						
I_{LIM}	High-side current limit threshold			10		A

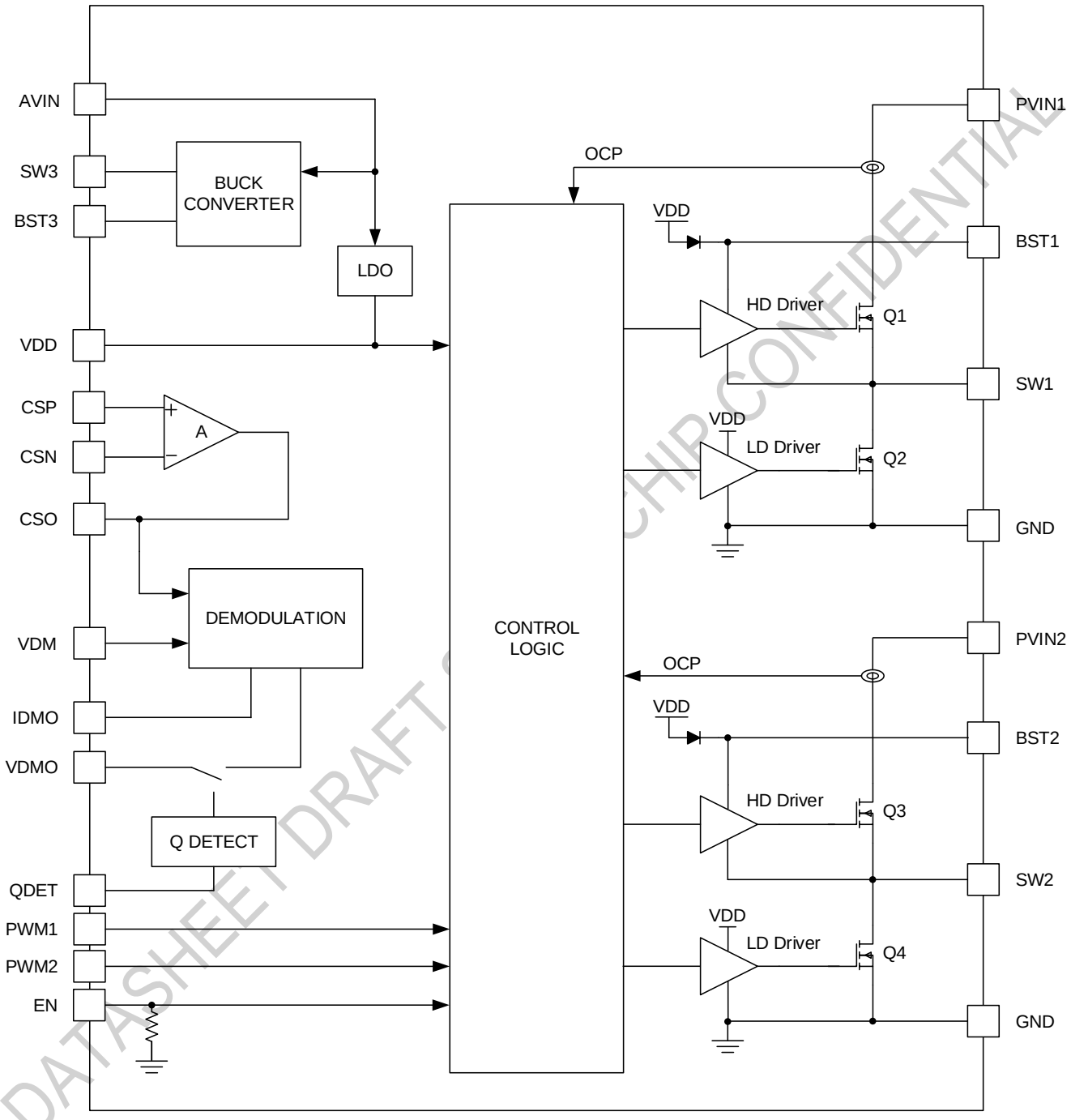
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T_p	Hiccup period		20	ms
EN				
V_{IH}	Input logic high		1.2	V
V_{IL}	Input logic low		0.4	V
R_{EN_PD}	EN internal pull-down resistance		800	kΩ
VDMO, IDMO				
V_{OH}	Output logic high		0.9* V_{DD}	V
V_{OL}	Input logic low		0.1* V_{DD}	V
Q FACTOR DETECTION				
V_{PRESET}	Preset voltage on SW1		2.5	V
V_{TH_HIGH}	High level detect voltage threshold	Configurable by EN table	200	mV
		Configurable by EN table	150	mV
		Configurable by EN table	100	mV
		Configurable by EN table	50	mV
V_{TH_LOW}	Low level detect voltage threshold	Configurable by EN table	100	mV
		Configurable by EN table	75	mV
		Configurable by EN table	50	mV
		Configurable by EN table	25	mV
TIMING				
T_{HIGH}(1)	High-level pulse duration		10	us
T_{LOW}(1)	Low-level pulse duration		10	us
$T_{D(OFF)}$ (1)	Turn-off delay time		80	us
T_{STORE}(1)	Data storage/accept time period		50	us
THERMAL SHUTDOWN				
T_{SD}	Thermal shutdown temperature		125	°C
	Thermal shutdown hysteresis		25	°C

(1) Guaranteed by design

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8 Functional Block Diagram



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9 Feature Description

9.1 Current Sense Amplifier

To support foreign object detection (FOD), the SC5003 senses the average input current to the device. The integrated current sense amplifier can be set to different voltage gain suit to different current sense resistors as Table 1.

Table1 RSENSE vs CSA gain

R_{SENSE}	CSA gain	CSO offset
5mΩ	200	1V
10mΩ	100	0.5V
20mΩ	50	0.25V

The current sense amplifier output has a voltage offset at zero input current. The offset value varies with the CSA gain. For accurate measurement of the input current, MCU need to calibrate this offset.

9.2 PWM Control

The PWM1 input controls the internal MOSFET Q1 and Q2, and the PWM2 input controls the internal MOSFET Q3 and Q4 as shown in the Block Diagram. The PWM1 and PWM2 can independently control the SW1 and SW2 duty cycle and frequency. Please be noted that dead time has already been implemented between Q1 (or Q3) and Q2 (or Q4) internally, so there is no need for dead time between external control signals PWM1 and PWM2.

9.3 Input Under-Voltage Lockout (UVLO)

The UVLO function protects the chip from operating at insufficient power supply. The chip disables all the function if AVIN input voltage is lower than 3.6V (typical) and it doesn't start up again until input voltage is higher than 3.8V (typical).

9.4 Voltage Demodulation

In order to increase the communication reliability in any load condition, the SC5003 has integrated two demodulation schemes, one based on input average current information and the other based on coil voltage information. The voltage mode envelope detector is implemented using a discrete solution as depicted on Figure1. This simple implementation achieves the envelope detector function low-pass filter as well as the DC filter function.

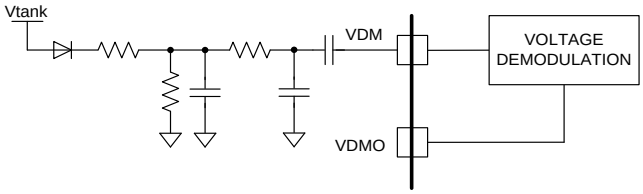


Fig1. Voltage Demodulation

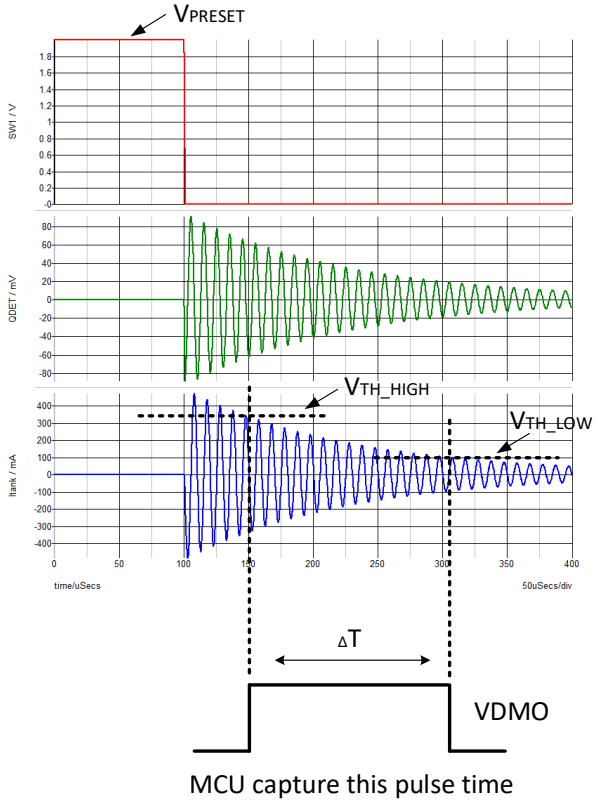
9.5 Current Demodulation

The current-mode detector takes the modulation information from the average input current. The MCU can detect the demodulation results on VDMO and IDMO pins and then implement the packet decode. The MCU can select either voltage-mode or current-mode signals depending upon which produces the best demodulated signal.

9.6 Q Factor Detection

The SC5003 integrates an accurate Q factor detection circuit to implement foreign objects detection before the selection phase.

$$Q = \frac{\Delta T * \pi}{10 * \ln \frac{V_{TH_HIGH}}{V_{TH_LOW}}}$$



MCU capture this pulse time

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9.7 Over-Current Protection (OCP)

The SC5003 integrates a hiccup mode over-current protection. Current of the SW1 high-side FET and SW2 high-side FET are sensed and compared to the current-limit threshold during every switching cycle. When the sensed current reaches the current-limit threshold, the over-current fault counter is incremented. If the over-current fault counter reaches 8 and overflows, all 4 internal FETs are turned off regardless of the PWM inputs. The IC remains in hiccup mode for a period equal to 20ms typically and then attempts to restart. The hiccup mode OCP protection can reduce the average current greatly to alleviate the thermal issue and to protect the converter. Once the OCP condition is removed, SC5003 exits hiccup mode and goes back to normal operation.

9.8 Over Temperature Protection (OTP)

The over temperature protection (OTP) prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 125℃, SC5003 is shut down. When the temperature drops below threshold (typically 100℃), the chip is enabled again.

9.9 Digital Interface (EN pin)

The digital interface is used to implement input high voltage request function and Q factor detection function. If digital interface is not required, the EN pin can also be used as a standard enable pin. Once the device is enabled, Q factor detection is not implemented. The interface counts the rising edges applied to the EN pin and enable the new function according to Table 2.

Table 2 Programming Table

Rising Edges	Function
1	VDM Vth=50mV
0/2	VDM Vth=40mV
3	VDM Vth=20mV
4	VDM Vth=10mV
0/5	Set VTH_HIGH to 200mV
6	Set VTH_HIGH to 150mV
7	Set VTH_HIGH to 100mV
8	Set VTH_HIGH to 50mV
0/9	Set VTH_LOW to 100mV
10	Set VTH_LOW to 75mV
11	Set VTH_LOW to 50mV
12	Set VTH_LOW to 25mV
13	Enable Q factor detection (When QDET enable，VDMO used as QDET output)
0/14	Disable Q factor detection (When QDET disable，VDMO used as output of demodulation)
0/15	Enable PVIN OVLO function
16	Disable PVIN OVLO function
17	High side and low side dead time=20ns
0/18	High side and low side dead time=40ns
19	High side and low side dead time=60ns
20	High side and low side dead time=80ns

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21	Driver speed slowest
22	Driver speed slow
0/23	Driver speed fast
24	Driver speed fastest
25	R_{SENSE}=20mohm
0/26	R_{SENSE}=10mohm
27	R_{SENSE}=5mohm
28	VDD=4.6V
0/29	VDD=5V
30	OCP decrease 1A
0/31	Default OCP
0/32	IDM Vth=4mV
33	IDM Vth=8mV
34	IDM Vth=16mV
35	IDM Vth=32mV

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10 Application Information

10.1 Input Current Sense

The SC5003 senses the average input current to the device. The recommended current sense resistor is 10mΩ/20mΩ. Resistor of 1% or higher accuracy and low temperature coefficient is recommended.

The resistor power rating and temperature coefficient should also be considered. The power dissipation is roughly calculated as $P=I^2R$, and I is the highest current flowing through the resistor. The resistor power rating should be higher than the calculated value.

The current sense amplifier output has a voltage offset at zero input current. The offset value varies with the CSA gain. And please be noted that this offset may vary a little from one chip to another, so when MCU is calibrating this offset, it is highly recommended to use ADC to sense this offset instead of using fixed offset showed in Table 1.

Figure 3 shows the internal current sense output (CSO) voltage over the sensed current based on different sense resistor. The input current to CSO current gain will be 1V/A.

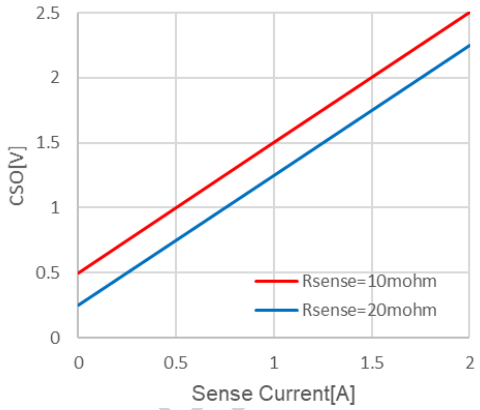


Fig3. CSO Voltage over Sense Current

10.2 Voltage/Current Demodulation

SC5003 integrates simultaneous voltage and current demodulation based on coil voltage and input average current separately. Compared with the discrete demodulation solution, SC5003 need much less number of external components.

Figure4 shows a typical circuit for voltage demodulation. D1/R15/R18/C29 is an envelope demodulation of the LC tank voltage. R14/C28 is a RC filter which can filter the high frequency switching noise while keep the 2 kHz communication signal. C27 is a DC blocking capacitor which passes through only the ac signal to the internal demodulator.

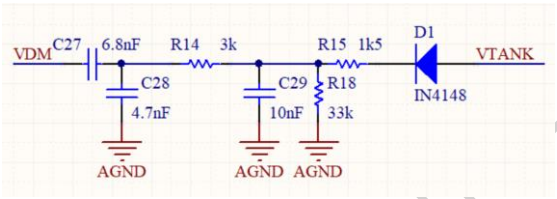


Fig4. Voltage Demodulation

Figure5 shows a typical communication packet, which is comprised of a preamble, a header, the actual message, and a checksum, as defined by the WPC standard.

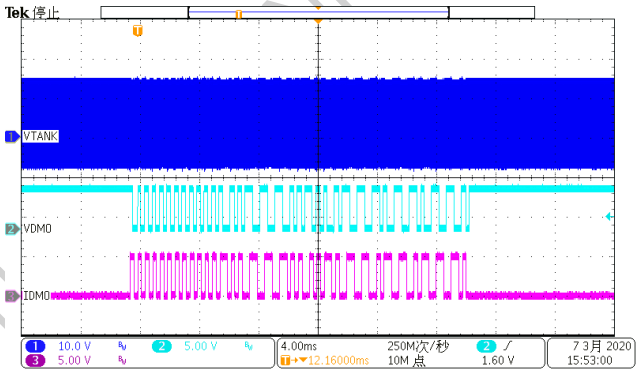


Fig5. VDMO/IDMO Demodulation Output

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11 Layout Guide

Here are the guidelines to follow:

- Make routing loop as small as possible, especially the power loop, to minimize EMI noises.
- Widen the copper between SW1, SW2 and LC tank, because high current in the LC tank can cause power losses on the traces and hence low efficiency. Moreover, the PVIN1/2 routing should be as wide as possible.
- The input current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing).
- Place small-size input capacitors as close as possible between the PVIN1/2 pins and PGND pin. These capacitors can effectively filter out high-frequency noises due to their low ESR and ESL. Please refer to C14 and C19 in Figure 6.

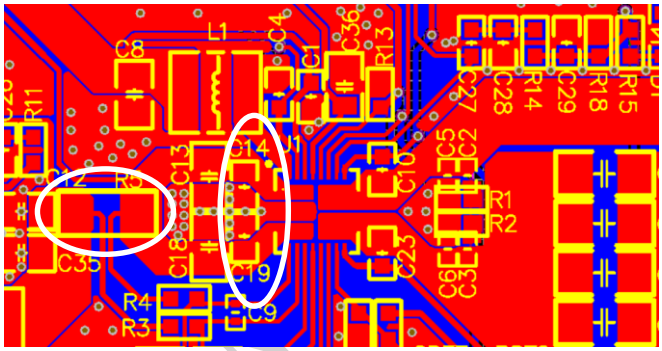
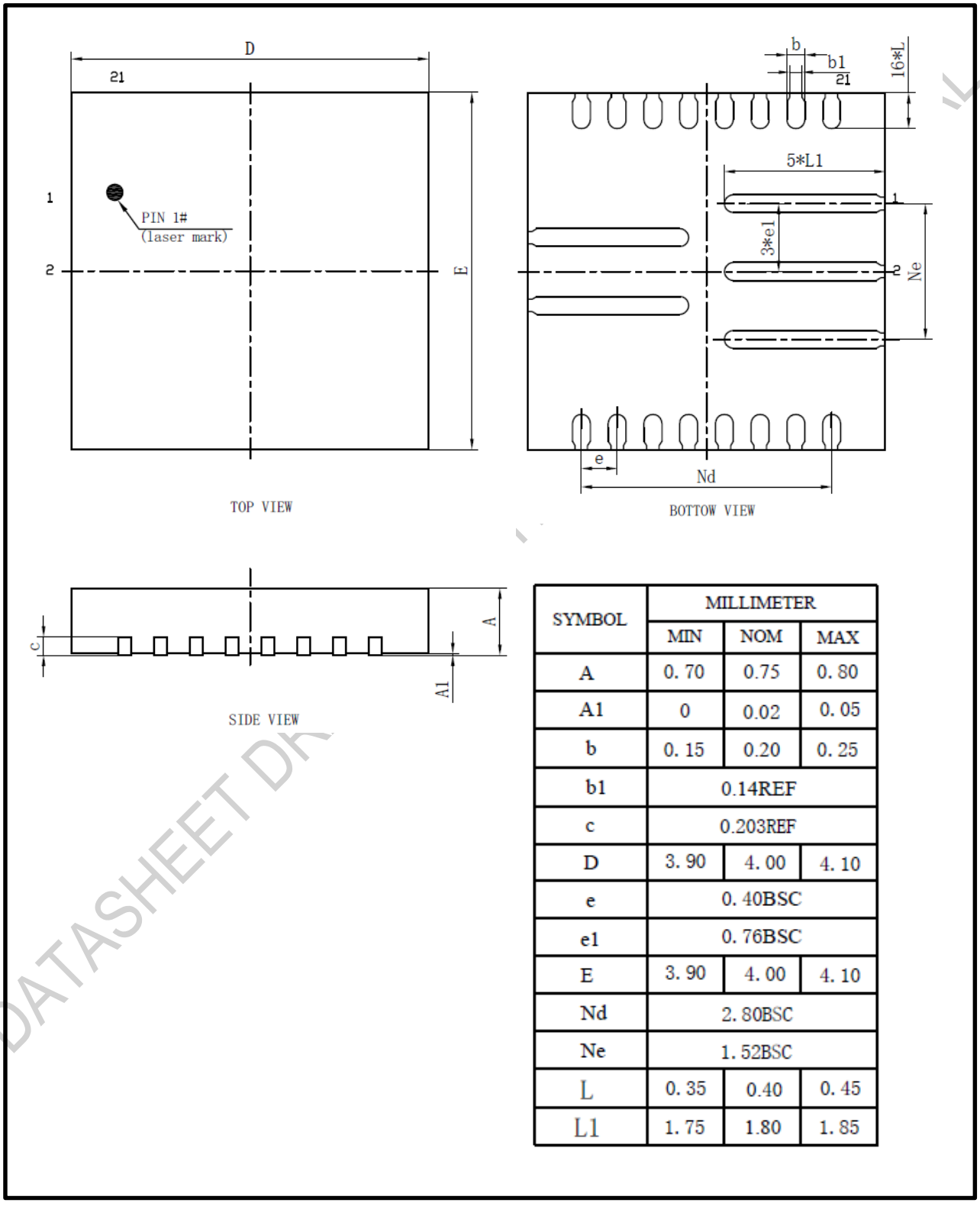


Fig6. Top Layer

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12 MECHANICAL DATA

FCQFN21L (4x4x0.75)



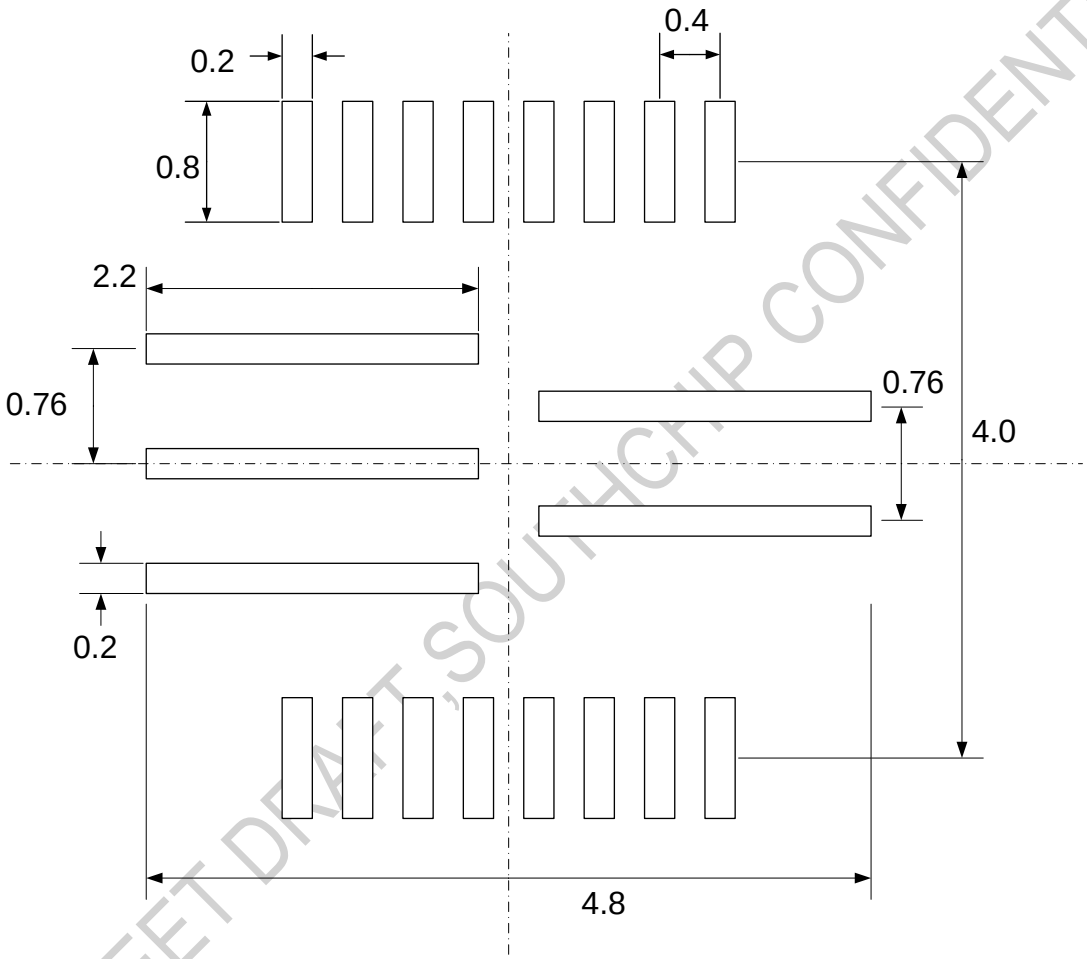
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	0	0.02	0. 05
b	0. 15	0.20	0. 25
b1	0.14REF		
c	0.203REF		
D	3. 90	4. 00	4. 10
e	0. 40BSC		
e1	0. 76BSC		
E	3. 90	4. 00	4. 10
Nd	2. 80BSC		
Ne	1. 52BSC		
L	0. 35	0.40	0. 45
L1	1. 75	1.80	1. 85

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13 RECOMMENDED FOOTPRINT

FCQFN21L (4x4x0.75)



Notes:

A: All linear dimensions are in millimeters

B: Publication IPC-7351 is recommended for alternate designs

C: Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad

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