DRV8305-Q1 集成三个分流放大器和稳压器的三相汽车智能栅极驱动器

1 特性

- 具有符合面向汽车应用的 AEC-Q100 标准
- 环境工作温度范围：
  - 温度等级 0 (E)：–40°C 至 +150°C
  - 温度等级 1 (Q)：–40°C 至 +125°C
- 4.4V 至 45V 工作电压范围
- 1.25A 和 1A 峰值栅极驱动电流
- 智能栅极驱动架构（IDRIVE 和 TDRIVE）
- 可编程高侧和低侧压摆率控制
- 支持 100% 占空比的电荷泵栅极驱动器
- 三个集成式分流放大器
- 50mA 集成型 LDO（3.3V 和 5V 选项）
- 高达 200kHz 的 3 PWM 或 6 PWM 输入控制
- 能够进行单 PWM 模式换向
- 用于器件设置和故障报告的串行外设接口 (SPI)
- 耐热增强型 48 引脚 HTQFP 封装
- 保护 功能：
  - 故障诊断和 MCU 看门狗
  - 可编程的死区时间控制
  - MOSFET 击穿保护
  - MOSFET V_{DS} 过流监视器
  - 栅极驱动器故障检测
  - 支持电池反向保护
  - 支持跛行回家模式
  - 过热警告和关断

2 应用

- 三相 BLDC 电机和 PMSM 电机
- 汽车油泵和水泵
- 汽车风扇和鼓风机

3 说明

DRV8305-Q1 器件是一款适用于三相电机驱动应用的栅极驱动器 IC。该器件提供了三个高精度半桥驱动器，每个驱动器能够驱动一个高侧和低侧 N 沟道 MOSFET。电荷泵驱动器支持占空比为 100% 的低压操作，适用于冷启动条件。该器件最高可耐受 45V 负载突降电压。

DRV8305-Q1 器件具备三个双向分流放大器，支持可变增益设置和可调节偏移基准，可精确测量低侧电流。

DRV8305-Q1 器件具有一个集成稳压器，可满足微控制器 (MCU) 或其他系统的电源要求。稳压器可与 LIN 物理接口直接相连，支持低功耗系统待机和休眠模式。

栅极驱动器在切换时使用自动握手，以防止发生电流击穿。可精确感测高侧和低侧 MOSFET 的 V_{DS}，从而防止外部 MOSFET 出现过流情况。SPI 提供详细的故障报告、诊断和器件配置，例如分流放大器的增益选项、独立的 MOSFET 过流检测和栅极驱动转换率控制。

器件选项：

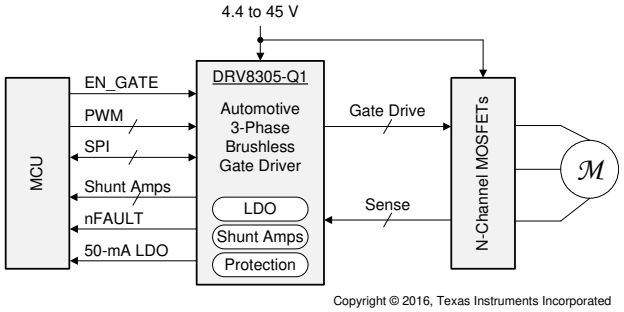
- DRV8305NQ：1 级，带有电压基准
- DRV83053Q：1 级，带有 3.3V、50mA LDO
- DRV83055Q：1 级，带有 5V、50mA LDO
- DRV8305NE：0 级，带有电压基准

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
DRV8305-Q1	HTQFP (48)	7.00mm × 7.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (September 2017) to Revision D — **Page**

- Added content to the VREG pin description ... 5
- Added ESD classification levels to the *ESD Ratings* table ... 6
- Added the *VREG Reference Voltage Input (DRV8305N)* section ... 48
- Added the *Power Supply Consideration in Generator Mode* section ... 50

Changes from Revision B (May 2016) to Revision C — **Page**

- Added transient specification for GHx, SLx, SPx, and SNx ... 6
- Changed SPx and SNx rating from -2 V to -3 V ... 6
- Changed the test condition for the V_{AVDD_UVLO}, V_{VCPH_UVFL}, V_{VCPH_UVLO2}, and $V_{VCP_LSD_UVLO2}$ parameters in the *Electrical Characteristics* table ... 11
- Changed the maximum V_{AVDD_UVLO} and V_{PVDD_UVLO2} parameters in the *Electrical Characteristics* table ... 11
- Moved the *External Components* table from the *Pin Configuration and Functions* section to the *Feature Description* section ... 18
- Added the description for latch fault reset methods to the *Undervoltage Warning (UVFL), Undervoltage Lockout (UVLO), and Overvoltage (OV) Protection* section ... 32
- Changed the description of FLIP_OTSD register bit in the *IC Operation Register Description* ... 42
- 已添加 *接收文档更新通知*部分 ... 53

Changes from Revision A (March 2016) to Revision B — **Page**

- 已更改 “产品预览”至“量产数据”并发布了完整数据手册 ... 1

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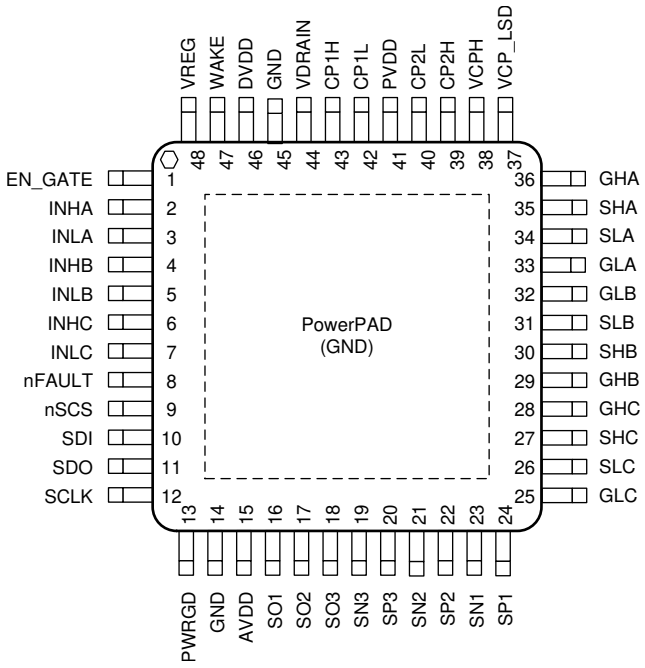
Changes from Original (May 2015) to Revision A **Page**

- 器件预览数据表更新了基本电气特性和功能描述 1
- Updated the y-axis units to µA for Figure 4 15

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5 Pin Configuration and Functions

PHP Package
48-Pin HTQFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION	
NAME	NO.			
EN_GATE	1	I	Enable gate	Enables the gate driver and current shunt amplifiers; internal pulldown.
INHA	2	I	Bridge PWM input	PWM input signal for bridge A high-side.
INLA	3	I	Bridge PWM input	PWM input signal for bridge A low-side.
INHB	4	I	Bridge PWM input	PWM input signal for bridge B high-side.
INLB	5	I	Bridge PWM input	PWM input signal for bridge B low-side.
INHC	6	I	Bridge PWM input	PWM input signal for bridge C high-side.
INLC	7	I	Bridge PWM input	PWM input signal for bridge C low-side.
nFAULT	8	OD	Fault indicator	When low indicates a fault has occurred; open drain; external pullup to MCU power supply needed (1 kΩ to 10 kΩ).
nSCS	9	I	SPI chip select	Select/enable for SPI; active low.
SDI	10	I	SPI input	SPI input signal.
SDO	11	O	SPI output	SPI output signal.
SCLK	12	I	SPI clock	SPI clock signal.
PWRGD	13	OD	Power good	VREG and MCU watchdog fault indication; open drain; external pullup to MCU power supply needed (1 kΩ to 10 kΩ).
GND	14, 45	P	Device ground	Must be connected to ground.
AVDD	15	P	Analog regulator	5-V internal analog supply regulator; bypass to GND with a 6.3-V, 1-µF ceramic capacitor.
SO1	16	O	Current amplifier output	Output of current sense amplifier 1.
SO2	17	O	Current amplifier output	Output of current sense amplifier 2.
SO3	18	O	Current amplifier output	Output of current sense amplifier 3.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION	
NAME	NO.			
SN3	19	I	Current amplifier negative input	Negative input of current sense amplifier 3.
SP3	20	I	Current amplifier positive input	Positive input of current sense amplifier 3.
SN2	21	I	Current amplifier negative input	Negative input of current sense amplifier 2.
SP2	22	I	Current amplifier positive input	Positive input of current sense amplifier 2.
SN1	23	I	Current amplifier negative input	Negative input of current sense amplifier 1.
SP1	24	I	Current amplifier positive input	Positive input of current sense amplifier 1.
GLC	25	O	Low-side gate driver	Low-side gate driver output for half-bridge C.
SLC	26	I	Low-side source connection	Low-side source connection for half-bridge C.
SHC	27	I	High-side source connection	High-side source connection for half-bridge C.
GHC	28	O	High-side gate driver	High-side gate driver output for half-bridge C.
GHB	29	O	High-side gate driver	High-side gate driver output for half-bridge B.
SHB	30	I	High-side source connection	High-side source connection for half-bridge B.
SLB	31	I	Low-side source connection	Low-side source connection for half-bridge B.
GLB	32	O	Low-side gate driver	Low side gate driver output for half-bridge B.
GLA	33	O	Low-side gate driver	Low-side gate driver output for half-bridge A.
SLA	34	I	Low-side source connection	Low-side source connection for half-bridge A.
SHA	35	I	High-side source connection	High-side source connection for half-bridge A.
GHA	36	O	High-side gate driver	High-side gate driver output for half-bridge A.
VCP_LSD	37	P	Low-side gate driver regulator	Internal voltage regulator for low-side gate driver; connect 1-µF capacitor to GND.
VCPH	38	P	High-side gate driver regulator	Internal charge pump for high-side gate driver; connect 2.2-µF capacitor to PVDD.
CP2H	39	P	Charge pump flying capacitor	Flying capacitor for charge pump; connect 0.047-µF capacitor between CP2H and CP2L.
CP2L	40	P		
PVDD	41	P	Power supply	Device power supply; minimum 4.7-µF ceramic capacitor to GND.
CP1L	42	P	Charge pump flying capacitor	Flying capacitor for charge pump; connect 0.047-µF capacitor between CP1H and CP1L.
CP1H	43	P		
VDRAIN	44	P	High-side drain	High-side MOSFET drain connection; common for all three half bridges.
DVDD	46	P	Digital regulator	3.3-V internal digital-supply regulator; bypass to GND with a 6.3-V, 1-µF ceramic capacitor.
WAKE	47	I	Wake up from sleep control pin	High voltage tolerant input pin to wake-up device from SLEEP; pin cannot be used to disable LDO; driver needs to be enabled and disabled separately.
VREG	48	P	VREG/VREF	Dual purpose pin based on part number; also supplies internal amplifier reference voltage and SDO pullup. VREG: 3.3-V or 5-V, 50-mA LDO; connect 1-µF to GND. VREF: Reference voltage; LDO disabled. If PVDD voltage is lower than VREF pin voltage, there is a current path from VREF to PVDD through the internal LDO. The current must be limited to 50 mA by the system.
GND	PPAD	P	Device ground	Must be connected to ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range with respect to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage (PVDD)		–0.3	45	V
Power supply pin voltage ramp rate (PVDD)		0	2	V/µs
High-side charge pump pin voltage (VCPH)		–0.3	PVDD + 12	V
Low-side regulator pin voltage (VCP_LSD)		–0.3	12	V
Charge pump 1 positive switching pin voltage (CP1H)		PVDD – 1.5	PVDD + 12	V
Charge pump 2 positive switching pin voltage (CP2H)		PVDD – 3	PVDD + 12	V
Charge pump negative switching pin voltage (CPxL)		–0.3	PVDD	V
High-side gate driver pin voltage (GHx)		–5	57	V
Gate-to-source voltage difference (GHx-SHx), (GLx-SLx)		–0.3	15	V
Low-side gate driver pin voltage (GLx)		–3	12	V
High-side gate driver source voltage (SHx)		–5	45	V
Transient 200-ns high-side gate driver source voltage (SHx)		–7	45	V
High-side gate driver source voltage (SHx)		–5	PVDD + 5	V
Low-side gate driver source voltage (SLx)		–3	5	V
Transient 200-ns low-side gate driver source voltage (SLx)		–5	5	V
Drain pin voltage (VDRAIN)		–0.3	45	V
Control pin voltage (INHx, INLx, EN_GATE, SCLK, SDI, SCS, SDO, nFAULT, PWRGD)		–0.3	5.5	V
Wake pin voltage (WAKE)		–0.3	45	V
Sense amplifier voltage (SPx, SNx)		–3	5	V
Transient 200-ns sense amplifier voltage (SPx, SNx)		–5	5	V
Sense amplifier output pin voltage (SOx)		–0.3	5.5	V
Externally applied reference voltage, DRV8305N (VREG)		–0.3	5.5	V
Externally applied reference sink current, DRV8305N (VREG)		0	100	µA
Internal digital regulator voltage (DVDD)		–0.3	3.6	V
Internal analog regulator voltage (AVDD)		–0.3	5.5	V
Open drain pins sink current (nFAULT, PWRGD)		0	7	mA
Wake pin sink current (WAKE) – limit current with external resistor		0	1	mA
Junction temperature, T_J	DRV8305xQPHPQ1	–40	150	°C
	DRV8305xEPHPQ1(2)(3)	–40	175	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) IC is designed to be operational up to T_J = 175°C. Internal overtemperature shutdown will be disabled by default on the DRV8305xEPHPQ1.
(3) Because lifetime degrades exponentially at higher temperatures, operation between T_J = 150°C to 175°C must be limited to transient and infrequent events. For transient events between T_J = 150°C to 175°C for a total of 10 hours over lifetime, no degradation in lifetime is expected. Contact TI for lifetime impact if the use case requires T_J = 150°C to 175°C greater than 10 hours.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM Classification Level C4A	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	MAX	UNIT
PVDD	Power supply voltage	4.4	45	V
PVDD	Power supply voltage for voltage regulator operation	4.3	45	V
VCPH	Charge pump external load current	0	30	mA
VCP_LSD	Low-side regulator external load current	0	30	mA
I_{GATE}	Total average gate drive current (HS + LS)	0	30	mA
f_{gate}	Operating switching frequency of gate driver	0	200	kHz
VREG	Voltage regulator external load current (regulator enabled device options)	0	50	mA
C_{O_OPA}	Maximum external capacitive load on shunt amplifier output (without external resistor)	0	60	pF
I_{nFAULT}	nFAULT sink current (nFAULT = 0.3 V)	0	7	mA
T_A	Operating ambient temperature, DRV8305xQPHPQ1	–40	125	°C
	Operating ambient temperature, DRV8305xEPHPQ1	–40	150	°C
T_J	Operating junction temperature, DRV8305xQPHPQ1	–40	150	°C
	Operating junction temperature, DRV8305xEPHPQ1	–40	175	°C

6.4 Thermal Information

THERMAL METRIC(1)		DRV8305-Q1 PHP (HTQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

PVDD = 4.4 to 45 V, DRV8305xQ: T_J = –40°C to 150°C, DRV8305xE: T_J = –40°C to 175°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (PVDD, DVDD, AVDD)						
V_{PVDD}	PVDD operating voltage		4.4		45	V
		Voltage regulator (VREG) operational	4.3		45	V
$I_{PVDD_Operating}$	PVDD operating supply current	EN_GATE = HIGH; VREG no load; outputs HI-Z		20		mA
$I_{PVDD_Standby}$	PVDD standby supply current	EN_GATE = LOW; VREG no load		5		mA
I_{PVDD_Sleep}	PVDD sleep supply current	EN_GATE = LOW; Sleep Mode; T_J = –40 to 150 °C		60	200	μA
		EN_GATE = LOW; Sleep Mode; T_J = 150 to 175 °C			250	uA
V_{AVDD}	Internal regulator voltage	PVDD = 5.3 to 45 V	4.85	5	5.15	V
		PVDD = 4.4 to 5.3 V	PVDD – 0.4	PVDD		V
V_{DVDD}	Internal regulator voltage			3.3		V
VOLTAGE REGULATOR (3.3-V or 5-V VREG)						
V_{VREG}	VREG DC output voltage	PVDD = 5.4 to 45 V	VREG × 0.97	VREG	VREG × 1.03	V
		PVDD = 4.4 to 5.3 V; 5-V VREG	PVDD – 0.4		PVDD	V
		PVDD = 4.4 to 5.3 V; 3.3-V VREG	VREG × 0.97	VREG	VREG × 1.03	V
$V_{LineReg}$	Line regulation	5.3 V ≤ V_{IN} ≤ 12 V; I_O = 1 mA		20		mV
$V_{LoadReg}$	Load regulation	100 μA ≤ I_{OUT} ≤ 50 mA; 5-V VREG		50	150	mV
		100 μA ≤ I_{OUT} ≤ 50 mA; 3.3-V VREG		30	100	mV
LOGIC-LEVEL INPUTS (INHx, INLx, EN_GATE, SCLK, nSCS)						
V_{IL}	Input logic low voltage		0		0.8	V
V_{IH}	Input logic high voltage		2		5	V
R_{PD}	Internal pulldown resistor	To GND		100		kΩ
CONTROL OUTPUTS (nFAULT, SDO, PWRGD)						
V_{OL}	Output logic low voltage	nFAULT; SDO; PWRGD; I_O = 5 mA			0.5	V
V_{OH}	Output logic high voltage	SDO; I_O = 5 mA	VREG – 0.9			V
I_{OH}	Output logic high leakage	V_O = 3.3 V	–1		1	μA
HIGH VOLTAGE TOLERANT LOGIC INPUT (WAKE)						
V_{IL_WAKE}	Output logic low voltage		1.1		1.45	V
V_{IH_WAKE}	Output logic high voltage		1.46		1.8	V
GATE DRIVE OUTPUT (GHx, GLx)						
V_{GHS}	High-side gate driver Vgs voltage	V_{PVDD} = 8 to 45 V; I_{GATE} < 30 mA	9	10	10.7	V
		V_{PVDD} = 5.5 to 8 V; I_{GATE} < 10 mA	7		10.7	V
		V_{PVDD} = 4.4 to 5.5 V; I_{GATE} < 5 mA	5		9	V
V_{GLS}	Low-side gate driver Vgs voltage	V_{PVDD} = 8 to 45 V; I_{GATE} < 30 mA	9	10	10.7	V
		V_{PVDD} = 5.5 to 8 V; I_{GATE} < 10 mA	9		10.7	V
		V_{PVDD} = 4.4 to 5.5 V; I_{GATE} < 5 mA	8		10.7	V
PEAK CURRENT DRIVE TIMES (GHx, GLx)						
t_{DRIVE}	Peak sink or source current drive time	TDRIVEP = 00; TDRIVEN = 00		220		ns
		TDRIVEP = 01; TDRIVEN = 01		440		ns
		TDRIVEP = 10; TDRIVEN = 10		880		ns
		TDRIVEP = 11; TDRIVEN = 11		1780		ns

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Electrical Characteristics (continued)

PVDD = 4.4 to 45 V, DRV8305xQ: T_J = –40°C to 150°C, DRV8305xE: T_J = –40°C to 175°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-SIDE PEAK CURRENT GATE DRIVE (GHx)						
I_{DRIVEP_HS}	High-side peak source current	IDRIVEP_HS = 0000		0.01		A
		IDRIVEP_HS = 0001		0.02		A
		IDRIVEP_HS = 0010		0.03		A
		IDRIVEP_HS = 0011		0.04		A
		IDRIVEP_HS = 0100		0.05		A
		IDRIVEP_HS = 0101		0.06		A
		IDRIVEP_HS = 0110		0.07		A
		IDRIVEP_HS = 0111		0.125		A
		IDRIVEP_HS = 1000		0.25		A
		IDRIVEP_HS = 1001		0.5		A
		IDRIVEP_HS = 1010		0.75		A
		IDRIVEP_HS = 1011		1		A
		IDRIVEP_HS = 1100, 1101, 1110, 1111		0.05		A
I_{DRIVEN_HS}	High-side peak sink current	IDRIVEN_HS = 0000		0.02		A
		IDRIVEN_HS = 0001		0.03		A
		IDRIVEN_HS = 0010		0.04		A
		IDRIVEN_HS = 0011		0.05		A
		IDRIVEN_HS = 0100		0.06		A
		IDRIVEN_HS = 0101		0.07		A
		IDRIVEN_HS = 0110		0.08		A
		IDRIVEN_HS = 0111		0.25		A
		IDRIVEN_HS = 1000		0.5		A
		IDRIVEN_HS = 1001		0.75		A
		IDRIVEN_HS = 1010		1		A
		IDRIVEN_HS = 1011		1.25		A
		IDRIVEN_HS = 1100, 1101, 1110, 1111		0.06		A
LOW-SIDE PEAK CURRENT GATE DRIVE (GLx)						
I_{DRIVEP_LS}	Low-side peak source current	IDRIVEP_LS = 0000		0.01		A
		IDRIVEP_LS = 0001		0.02		A
		IDRIVEP_LS = 0010		0.03		A
		IDRIVEP_LS = 0011		0.04		A
		IDRIVEP_LS = 0100		0.05		A
		IDRIVEP_LS = 0101		0.06		A
		IDRIVEP_LS = 0110		0.07		A
		IDRIVEP_LS = 0111		0.125		A
		IDRIVEP_LS = 1000		0.25		A
		IDRIVEP_LS = 1001		0.5		A
		IDRIVEP_LS = 1010		0.75		A
		IDRIVEP_LS = 1011		1		A
		IDRIVEP_LS = 1100, 1101, 1110, 1111		0.05		A

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Electrical Characteristics (continued)

PVDD = 4.4 to 45 V, DRV8305xQ: T_J = –40°C to 150°C, DRV8305xE: T_J = –40°C to 175°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRIVEN_LS}	Low-side peak sink current	IDRIVEN_LS = 0000		0.02		A
		IDRIVEN_LS = 0001		0.03		A
		IDRIVEN_LS = 0010		0.04		A
		IDRIVEN_LS = 0011		0.05		A
		IDRIVEN_LS = 0100		0.06		A
		IDRIVEN_LS = 0101		0.07		A
		IDRIVEN_LS = 0110		0.08		A
		IDRIVEN_LS = 0111		0.25		A
		IDRIVEN_LS = 1000		0.5		A
		IDRIVEN_LS = 1001		0.75		A
		IDRIVEN_LS = 1010		1		A
		IDRIVEN_LS = 1011		1.25		A
		IDRIVEN_LS = 1100, 1101, 1110, 1111		0.06		A
PASSIVE GATE PULLDOWN (GHx, GLx)						
R_{SLEEP_PD}	Gate pulldown resistance, sleep mode	EN_GATE = LOW; GHx to GND;		1000		Ω
		EN_GATE = LOW; GLx to GND;		500		Ω
$R_{STANDBY_PD}$	Gate pulldown resistance, standby mode	EN_GATE = LOW; GHx to GND;		1000		Ω
		EN_GATE = LOW; GLx to GND;		500		Ω
ACTIVE GATE PULLDOWN (GHx, GLx)						
I_{HOLD}	Gate pulldown current, holding	EN_GATE = HIGH; GHx to SHx; GLx to SLx		50		mA
I_{STRONG}	Gate pulldown current, strong	EN_GATE = HIGH; GHx to SHx; GLx to SLx		1.25		A
GATE TIMING						
$t_{pd_lf\text{-}O}$	Positive input falling to GHS_x falling	PVDD = 12 V; CL = 1 nF; 50% to 50%		200		ns
$t_{pd_lr\text{-}O}$	Positive input rising to GHS_x rising	PVDD = 12 V; CL = 1 nF; 50% to 50%		200		ns
t_{d_min}	Minimum dead time after hand shaking			280		ns
t_{dtp}	Dead time in addition to t_{d_min}	DEAD_TIME = 000		35		ns
		DEAD_TIME = 001		52		ns
		DEAD_TIME = 010		88		ns
		DEAD_TIME = 011		440		ns
		DEAD_TIME = 100		880		ns
		DEAD_TIME = 101		1760		ns
		DEAD_TIME = 110		3520		ns
		DEAD_TIME = 111		5280		ns
t_{PD_MATCH}	Propagation delay matching between high-side and low-side			50		ns
t_{DT_MATCH}	Dead-time matching			50		ns

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Electrical Characteristics (continued)

PVDD = 4.4 to 45 V, DRV8305xQ: T_J = –40°C to 150°C, DRV8305xE: T_J = –40°C to 175°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SHUNT AMPLIFIER						
G_{CSA}	Current sense amplifier gain	GAIN_CSx = 00		10		V/V
		GAIN_CSx = 01		19.9		V/V
		GAIN_CSx = 10		39.8		V/V
		GAIN_CSx = 11		78.8		V/V
G_{ERR}	Current sense amplifier gain error	Input differential > 0.025 V; T_J = –40 to 150 °C	–3.5		3.5	%
		Input differential > 0.025 V; T_J = 150 to 175 °C	–4		4	%
$t_{SETTLING}$	Current sense amplifier settling time	Settling time to 1%; no blanking; G_{CSA} = 10; Vstep = 0.46 V		300		ns
		Settling time to 1%; no blanking; G_{CSA} = 20; Vstep = 0.46 V		600		ns
		Settling time to 1%; no blanking; G_{CSA} = 40; Vstep = 0.46 V		1.2		µs
		Settling time to 1%; no blanking; G_{CSA} = 80; Vstep = 0.46 V		2.4		µs
V_{IOS}	DC input offset	G_{CSA} = 10; input shorted; RTI	–4		4	mV
V_{VREF_ERR}	Reference buffer error (DC)	Internal or external VREF; VREF_SCALE = 01	–3		3	%
		Internal or external VREF; VREF_SCALE = 10	–4		4	%
		Internal or external VREF; VREF_SCALE = 11	–10		10	%
$V_{DRIFTOS}$	Input offset error drift	G_{CSA} = 10; input shorted; RTI		10		µV/C
I_{BIAS}	Input bias current	VIN_COM = 0; SOx open			100	µA
I_{OFFSET}	Input bias current offset	IBIAS (SNx-SPx); VIN_COM = 0; SOx open		1		µA
V_{IN_COM}	Common input mode range		–0.15		0.15	V
V_{IN_DIFF}	Differential input range		–0.48		0.48	V
CMRR	Common mode rejection ration	External input resistance matched; DC; GCSA = 10	60	80		dB
		External input resistance matched; 20 kHz; GCSA = 10	60	80		dB
PSRR	Power supply rejection ratio	DC (<120 Hz); GCSA = 10		150		dB
		20 kHz; GCSA = 10		90		dB
V_{SWING}	Output voltage swing	PVDD > 5.3 V	0.3		4.7	V
V_{SLEW}	Output slew rate	GCSA = 10; R_L = 0 Ω; CL = 60 pF	5.2	10		V/µs
I_{VO}	Output short circuit current	SOx shorted to ground		20		mA
UGB	Unity gain bandwidth product	GCSA = 10		2		MHz
VOLTAGE PROTECTION						
V_{AVDD_UVLO}	AVDD undervoltage fault	AVDD falling, relative to GND	3.3		3.7	V
V_{VREG_UV}	VREG undervoltage fault	VREG_UV_LEVEL = 00			VREG × 0.9	V
		VREG_UV_LEVEL = 01			VREG × 0.8	V
		VREG_UV_LEVEL = 10			VREG × 0.7	V
		VREG_UV_LEVEL = 11			VREG × 0.7	V
$V_{VREG_UV_DGL}$	VREG undervoltage monitor deglitch time		1.5		2	µs

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Electrical Characteristics (continued)

PVDD = 4.4 to 45 V, DRV8305xQ: T_J = –40°C to 150°C, DRV8305xE: T_J = –40°C to 175°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PVDD_UVFL}	Undervoltage protection warning, PVDD	PVDD falling	7.7		8.1	V
		PVDD rising	7.9		8.3	V
V_{PVDD_UVLO1}	Undervoltage protection lock out, PVDD	PVDD falling			4.1	V
		PVDD rising			4.3	V
V_{PVDD_UVLO2}	Undervoltage protection fault, PVDD	PVDD falling	4.2		4.4	V
		PVDD rising	4.4		4.7	V
V_{PVDD_OVFL}	Overvoltage protection warning, PVDD	PVDD falling	33.5		36	V
		PVDD rising	32.5		35	V
V_{VCPH_UVFL}	Charge pump undervoltage protection warning, VCPH	VCPH falling, relative to PVDD			8	V
V_{VCPH_UVLO2}	Charge pump undervoltage protection fault, VCPH	VCPH falling, relative to PVDD, SET_VCPH_UV = 0	4.6		5.3	V
		VCPH falling, relative to PVDD, SET_VCPH_UV = 1	4.3		5	V
$V_{VCP_LSD_UVLO2}$	Low-side regulator undervoltage fault, VCP_LSD	VCP_LSD falling, relative to GND	6.4		7.5	V
V_{VCPH_OVLO}	Charge pump overvoltage protection fault, VCPH	Relative to PVDD	14		18	V
$V_{VCPH_OVLO_ABS}$	Charge pump overvoltage protection fault, VCPH	Relative to GND		60		V
TEMPERATURE PROTECTION						
OTW_CLR	Junction temperature-to clear overtemperature (OTW) warning(1)		100	130	150	°C
OTW_SET	Junction temperature for overtemperature (OTW) warning(1)		135	160	185	°C
OTSD_CLR	Junction temperature-to-clear overtemperature shutdown (OTSD)(1)		125	155	180	°C
OTSD_SET(2)	Junction temperature for overtemperature shutdown (OTSD)(1)		160	185	210	°C
TEMP_FLAG1	Junction temperature flag setting 1(1)			105		°C
TEMP_FLAG2	Junction temperature flag setting 2(1)			125		°C
TEMP_FLAG3	Junction temperature flag setting 3(1)			135		°C
TEMP_FLAG4	Junction temperature flag setting 4(1)			185		°C
PROTECTION CONTROL						
$t_{pd,E-L}$	Delay, error event to all gates low	TBLANK = 00; TVDS = 00		1		µs
$t_{pd,E-SD}$	Delay, error event to nFAULTx low	TBLANK = 00; TVDS = 00		1		µs

(1) Specified by design.
(2) Overtemperature shutdown (OTSD) is disabled by default for DRV8305xEPHPQ1 and may only be re-enabled through control register.

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Electrical Characteristics (continued)

PVDD = 4.4 to 45 V, DRV8305xQ: T_J = –40°C to 150°C, DRV8305xE: T_J = –40°C to 175°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FET CURRENT PROTECTION (VDS SENSING)						
V_{DS_TRIP}	Drain-source voltage protection limit	VDS_LEVEL = 00000		0.06		V
		VDS_LEVEL = 00001		0.068		V
		VDS_LEVEL = 00010		0.076		V
		VDS_LEVEL = 00011		0.086		V
		VDS_LEVEL = 00100		0.097		V
		VDS_LEVEL = 00101		0.109		V
		VDS_LEVEL = 00110		0.123		V
		VDS_LEVEL = 00111		0.138		V
		VDS_LEVEL = 01000		0.155		V
		VDS_LEVEL = 01001		0.175		V
		VDS_LEVEL = 01010		0.197		V
		VDS_LEVEL = 01011		0.222		V
		VDS_LEVEL = 01100		0.25		V
		VDS_LEVEL = 01101		0.282		V
		VDS_LEVEL = 01110		0.317		V
		VDS_LEVEL = 01111		0.358		V
		VDS_LEVEL = 10000		0.403		V
		VDS_LEVEL = 10001		0.454		V
		VDS_LEVEL = 10010		0.511		V
		VDS_LEVEL = 10011		0.576		V
		VDS_LEVEL = 10100		0.648		V
		VDS_LEVEL = 10101		0.73		V
		VDS_LEVEL = 10110		0.822		V
		VDS_LEVEL = 10111		0.926		V
		VDS_LEVEL = 11000		1.043		V
		VDS_LEVEL = 11001		1.175		V
		VDS_LEVEL = 11010		1.324		V
		VDS_LEVEL = 11011		1.491		V
		VDS_LEVEL = 11100		1.679		V
		VDS_LEVEL = 11101		1.892		V
		VDS_LEVEL = 11110		2.131		V
		VDS_LEVEL = 11111		2.131		V
t_{VDS}	VDS sense deglitch time	TVDS = 00		0		µs
		TVDS = 01		1.75		µs
		TVDS = 10		3.5		µs
		TVDS = 11		7		µs
t_{BLANK}	VDS sense blanking time	TBLANK = 00		0		µs
		TBLANK = 01		1.75		µs
		TBLANK = 10		3.5		µs
		TBLANK = 11		7		µs
t_{WARN_PULSE}	nFAULT pin warning pulse length			56		µs
PHASE SHORT PROTECTION						
V_{SNSOCP_TRIP}	Phase short protection limit	Fixed voltage		2		V

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6.6 SPI Timing Requirements (Slave Mode Only)

			MIN	NOM	MAX	UNIT
t_{SPI_READY}	SPI read after power on	PVDD > V_{PVDD_UVLO1}		5	10	ms
t_{CLK}	Minimum SPI clock period		100			ns
t_{CLKH}	Clock high time		40			ns
t_{CLKL}	Clock low time		40			ns
t_{SU_SDI}	SDI input data setup time		20			ns
t_{HD_SDI}	SDI input data hold time		30			ns
t_{D_SDO}	SDO output data delay time, CLK high to SDO valid	C_L = 20 pF			20	ns
t_{HD_SDO}	SDO output hold time		40			ns
t_{SU_SCS}	SCS setup time		50			ns
t_{HD_SCS}	SCS hold time		50			ns
t_{HI_SCS}	SCS minimum high time before SCS active low		400			ns
tACC	SCS access time, SCS low to SDO out of high impedance			10		ns
t_{DIS}	SCS disable time, SCS high to SDO high impedance			10		ns

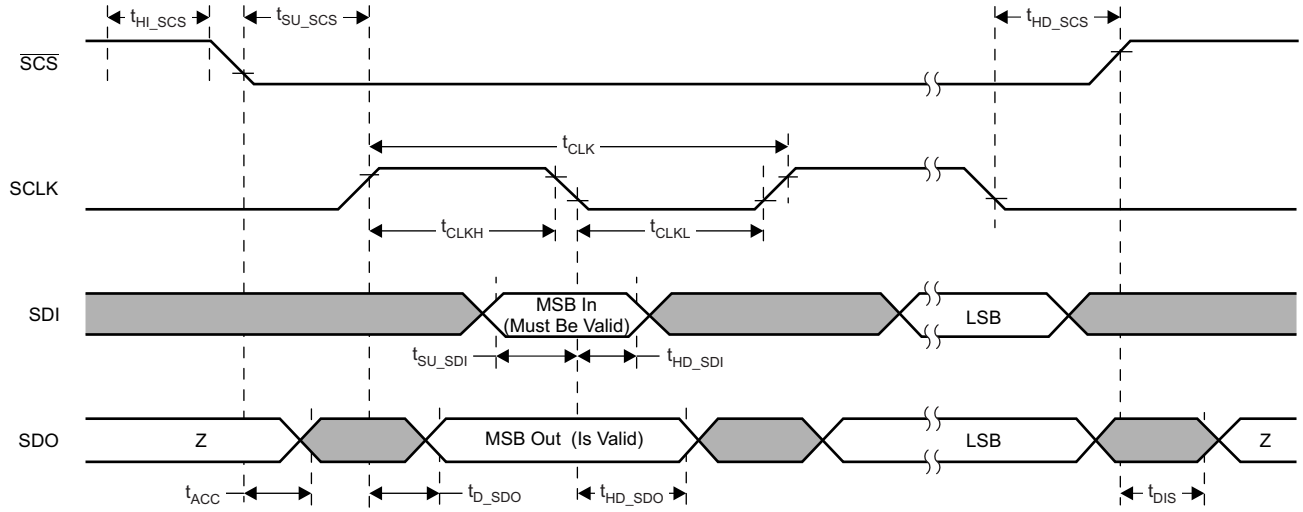


Figure 1. SPI Slave Mode Timing Definition

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6.7 Typical Characteristics

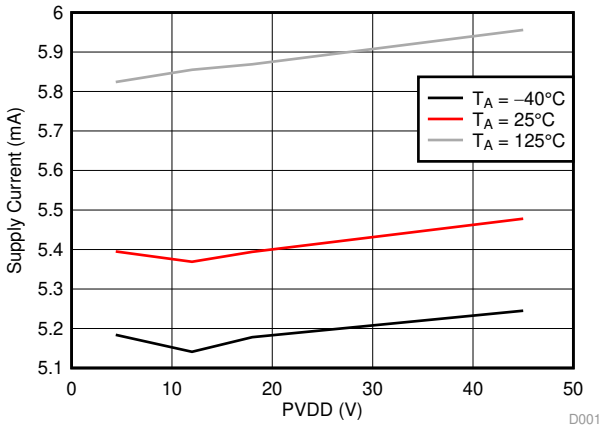


Figure 2. Standby Current

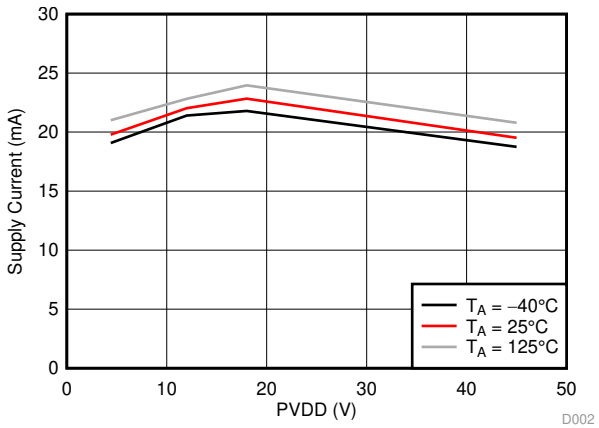


Figure 3. Operating Current

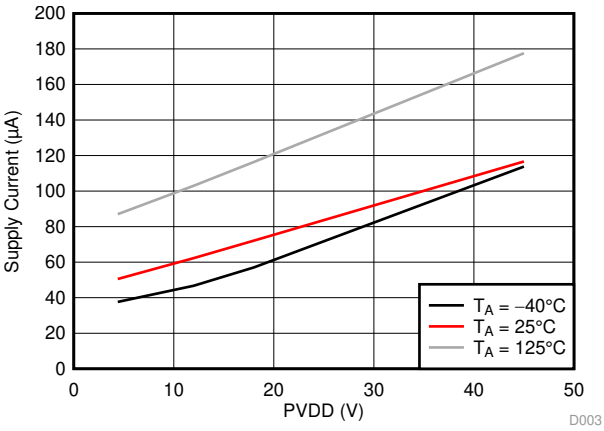


Figure 4. Sleep Current

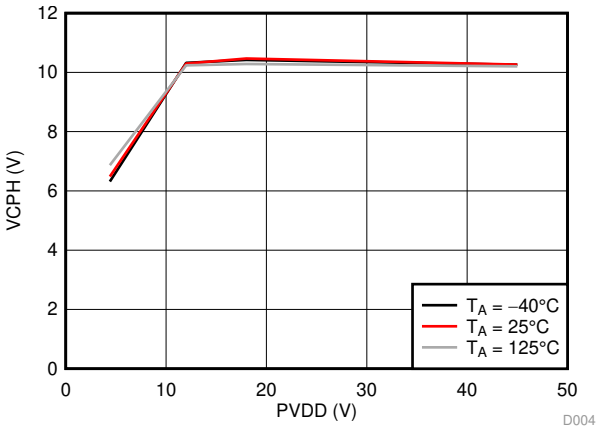


Figure 5. VCPH Voltage

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7 Detailed Description

7.1 Overview

The DRV8305-Q1 is a 4.4-V to 45-V automotive gate driver IC for three-phase motor driver applications. This device reduces external component count in the system by integrating three half-bridge drivers, charge pump, three current shunt amplifiers, an uncommited 3.3-V or 5-V, 50-mA LDO, and a variety of protection circuits. The DRV8305-Q1 provides overcurrent, shoot-through, overtemperature, overvoltage, and undervoltage protection. Fault conditions are indicated by the nFAULT pin and specific fault information can be read back from the SPI registers. The protection circuits are highly configurable to allow adaptation to different applications and support limp home operation.

The gate driver uses a tripler charge pump to generate the appropriate gate-to-source voltage bias for the external, high-side N-channel power MOSFETs during low supply conditions. A regulated 10-V LDO derived from the charge pump supplies the gate-to-source voltage bias for the low-side N-channel MOSFET. The high-side and low-side peak gate drive currents are adjustable through the SPI registers to finely tune the switching of the external MOSFETs without the need for external components. An internal handshaking scheme is used to prevent shoot-through and minimize the dead time when transitioning between MOSFETs in each half-bridge. Multiple input methods are provided to accommodate different control schemes including a 1-PWM mode which integrates a six-step block commutation table for BLDC motor control.

V_{DS} sensing of the external power MOSFETs allows for the DRV8305-Q1 to detect overcurrent conditions and respond appropriately. Integrated blanking and deglitch timers are provided to prevent false trips related to switching or transient noise. Individual MOSFET overcurrent conditions are reported through the SPI status registers and nFAULT pin. A dedicated VDRAIN pin is provided to accurately sense the drain voltage of the high-side MOSFET.

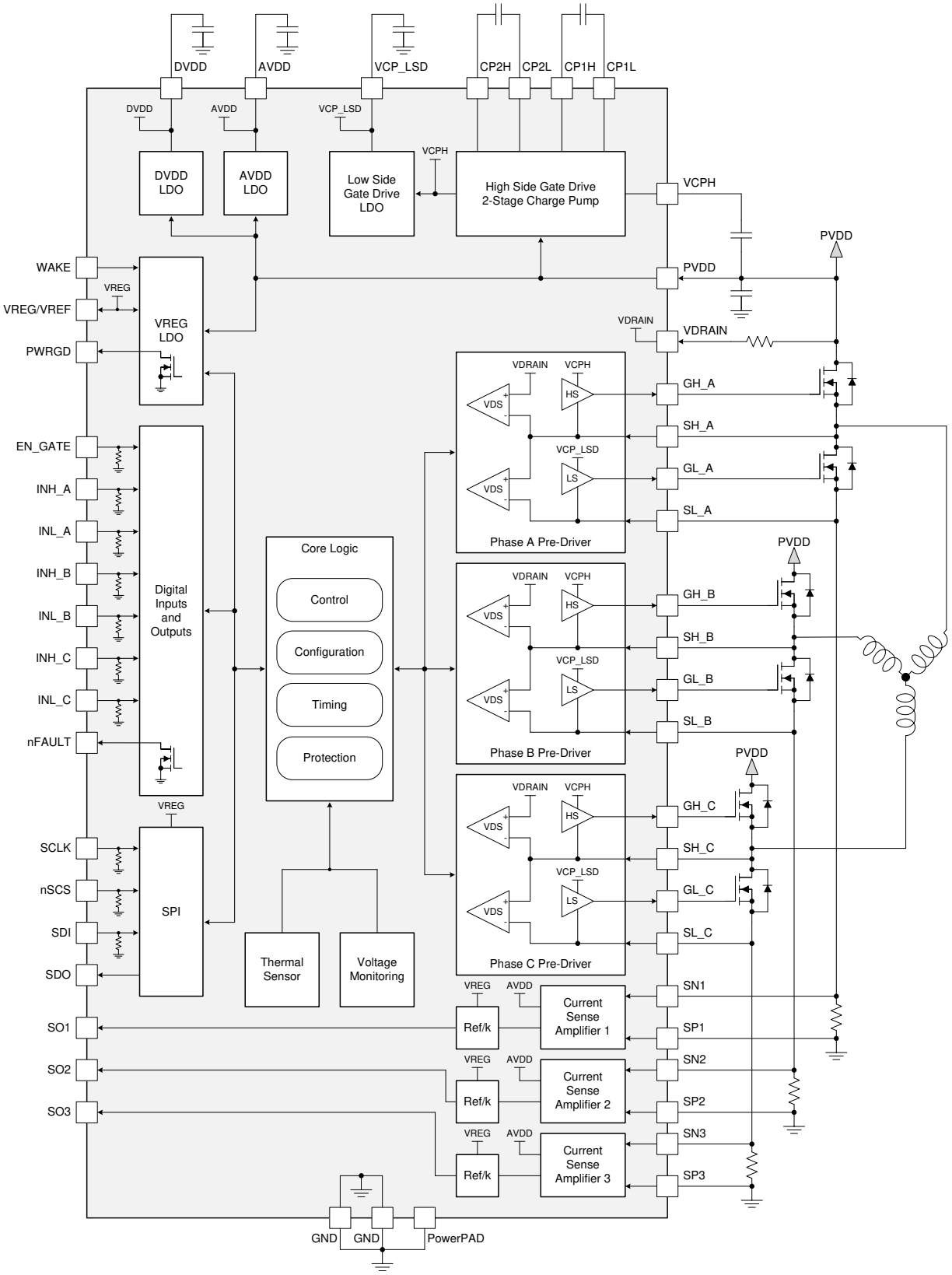
The three internal current shunt amplifiers allow for the implementation of common motor control schemes that require sensing of the half-bridge currents through a low-side current shunt resistor. The amplifier gain, reference voltage, and blanking are adjustable through the SPI registers. A calibration method is providing to minimize inaccuracy related to offset voltage.

Three versions of the DRV8305-Q1 are available with separate part numbers for the different devices options:

- DRV8305NQ: VREG pin has the internal LDO disabled and is only used as a voltage reference input for the amplifiers and SDO pullup. Grade 1.
- DRV83053Q: VREG is a 3.3-V, 50-mA LDO output pin. Grade 1.
- DRV83055Q: VREG is a 5-V, 50-mA LDO output pin. Grade 1.
- DRV8305NE: VREG pin has the internal LDO disabled and is only used as a voltage reference input for the amplifiers and SDO pullup. Grade 0.

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7.2 Functional Block Diagram



7.3 Feature Description

Table 1 lists the recommended values of the external components for the DRV8305-Q1.

Table 1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{PVDD}	PVDD	GND	4.7-µF ceramic capacitor rated for PVDD(1)
C_{AVDD}	AVDD	GND	1-µF ceramic capacitor rated for 6.3 V(1)
C_{DVDD}	DVDD	GND	1-µF ceramic capacitor rated for 6.3 V(1)
C_{VCPH}	VCPH	PVDD	2.2-µF ceramic capacitor rated for 16 V(1)
C_{VCP_LSD}	VCP_LSD	GND	1-µF ceramic capacitor rated for 16 V(1)
C_{CP1}	CP1H	CP1L	0.047-µF ceramic capacitor rated for PVDD(1)
C_{CP2}	CP2H	CP2L	0.047-µF ceramic capacitor rated for PVDD × 2(1)
C_{VREG}	VREG	GND	1-µF ceramic capacitor rated for 6.3 V(1)
R_{VDRAIN}	VDRAIN	PVDD	100-Ω series resistor between VDRAIN and HS MOSFET DRAIN
R_{nFAULT}	nFAULT	VCC(2)	1-10 kΩ pulled up the MCU power supply
R_{PWRGD}	PWRGD	VCC(2)	1-10 kΩ pulled up the MCU power supply

(1) The effective capacitance of ceramic capacitors varies with DC operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50% at the extremes of the operating voltage. The system designer must review the capacitor characteristics and select the component accordingly.
(2) VCC is not a pin on the DRV8305-Q1, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD.

7.3.1 Integrated Three-Phase Gate Driver

The DRV8305-Q1 is a completely integrated three-phase gate driver. It provides three N-channel MOSFET half-bridge gate drivers, multiple input modes, high-side and low-side gate drive supplies, and a highly configurable gate drive architecture. The DRV8305-Q1 is designed to support automotive applications by incorporating a wide operating voltage range, wide temperature range, and array of protection features. The configurability of device allows for it to be used in a broad range of applications.

7.3.2 INHx/INLx: Gate Driver Input Modes

The DRV8305-Q1 can be operated in three different inputs modes to support various commutation schemes.

- Table 2 shows the truth table for the 6-PWM input mode. This mode allows for each half-bridge to be placed in one of three states, either High, Low, or Hi-Z, based on the inputs.

Table 2. 6-PWM Truth Table

INHx	INLx	GHx	GLx
1	1	L	L
1	0	H	L
0	1	L	H
0	0	L	L

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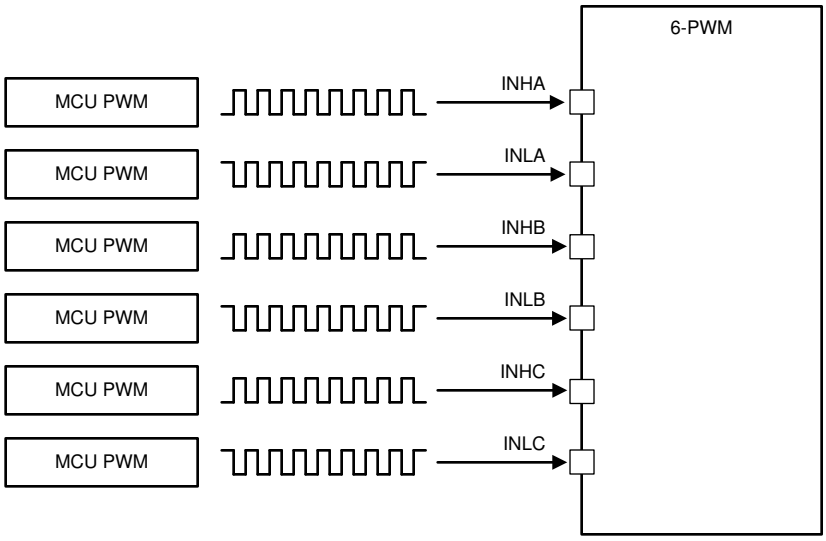


Figure 6. 6-PWM Mode

- Table 3 shows the truth table for the 3-PWM input mode. This mode allows for each half-bridge to be placed in one of two states, either High or Low, based on the inputs. The three high-side inputs (INHx) are used to control the state of the half-bridge with the complimentary low-side signals being generated internally. Dead time can be adjusted through the internal setting (DEAD_TIME) in the SPI registers. In this mode all activity on INLx is ignored.

Table 3. 3-PWM Truth Table

INHx	INLx	GHx	GLx
1	X	H	L
0	X	L	H

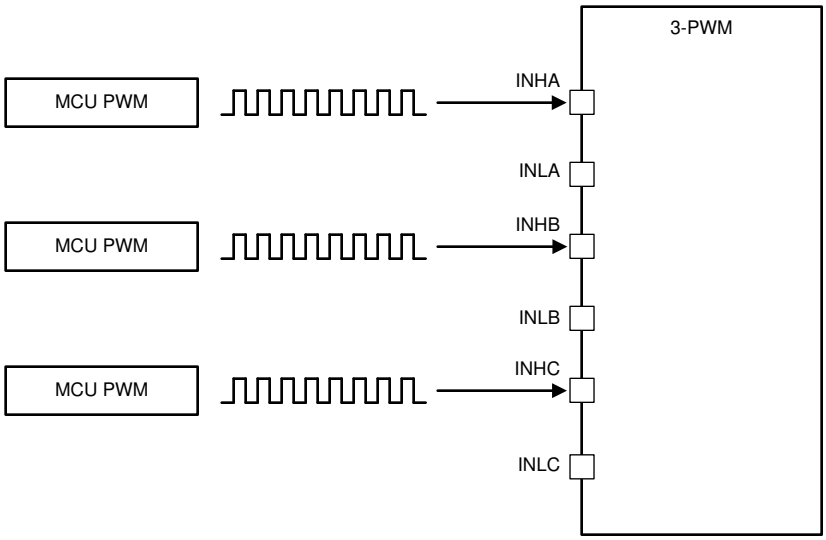


Figure 7. 3-PWM Mode

- Table 4 and Table 5 show the truth tables for the 1-PWM input mode. The 1-PWM mode uses an internally stored 6-step block commutation table to control the outputs of the three half-bridge drivers based on one PWM and three GPIO inputs. This mode allows the use of a lower cost microcontroller by requiring only one PWM resource. The PWM signal is applied on pin INHA (PWM_IN) to set the duty cycle of the half-bridge outputs along with the three GPIO signals on pins INLA (PHC_0), INHB (PHC_1), INLB (PHC_2) that serve to

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set the value of a three bit register for the commutation table. The PWM may be operated from 0-100% duty cycle. The three bit register is used to select the state for each half-bridge for a total of eight states including an align and stop state.

An additional and optional GPIO, INHC (DWELL) can be used to facilitate the insertion of *dwell states* or *phase current overlap* states between the six commutation steps. This may be used to reduce acoustic noise and improve motion through the reduction of abrupt current direction changes when switching between states. INHC must be high when the state is changed and the dwell state will exist until INHC is taken low. If the dwell states are not being used, the INHC pin can be tied low.

In 1-PWM mode all activity on INLC is ignored.

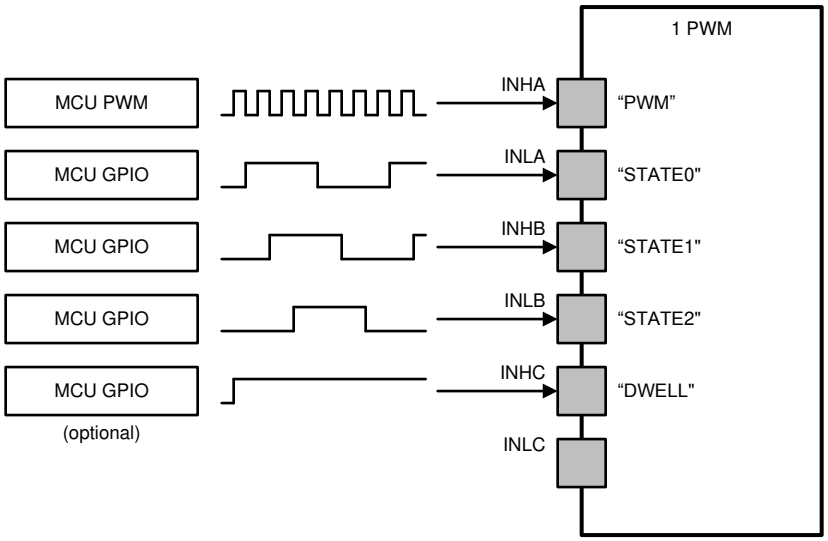


Figure 8. 1-PWM Mode

The method of freewheeling can be selected through an SPI register (COMM_OPTION). Diode freewheeling is when the phase current is carried by the body diode of the external power MOSFET during periods when the MOSFET is reverse biased (current moving from source to drain). In active freewheeling, the power MOSFET is enabled during periods when the MOSFET is reverse biased. This allows the system to improve efficiency due to the typically lower impedance of the MOSFET conduction channel as compared to the body diode. Table 4 shows the truth table for active freewheeling. Table 5) shows the truth table for diode freewheeling.

Table 4. 1-PWM Active Freewheeling

STATE	INLA:INHB:INLB:INHC	GHA	GLA	GHB	GLB	GHC	GLC
AB	0110	PWM	!PWM	LOW	HIGH	LOW	LOW
AB_CB	0101	PWM	!PWM	LOW	HIGH	PWM	!PWM
CB	0100	LOW	LOW	LOW	HIGH	PWM	!PWM
CB_CA	1101	LOW	HIGH	LOW	HIGH	PWM	!PWM
CA	1100	LOW	HIGH	LOW	LOW	PWM	!PWM
CA_BA	1001	LOW	HIGH	PWM	!PWM	PWM	!PWM
BA	1000	LOW	HIGH	PWM	!PWM	LOW	LOW
BA_BC	1011	LOW	HIGH	PWM	!PWM	LOW	HIGH
BC	1010	LOW	LOW	PWM	!PWM	LOW	HIGH
BC_AC	0011	PWM	!PWM	PWM	!PWM	LOW	HIGH
AC	0010	PWM	!PWM	LOW	LOW	LOW	HIGH
AC_AB	0111	PWM	!PWM	LOW	HIGH	LOW	HIGH
Align	1110	PWM	!PWM	LOW	HIGH	LOW	HIGH
Stop	0000	LOW	LOW	LOW	LOW	LOW	LOW

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Table 5. 1-PWM Diode Freewheeling

STATE	INLA:INHB:INLB:INHC	GHA	GLA	GHB	GLB	GHC	GLC
AB	0110	PWM	LOW	LOW	HIGH	LOW	LOW
AB_CB	0101	PWM	LOW	LOW	HIGH	PWM	LOW
CB	0100	LOW	LOW	LOW	HIGH	PWM	LOW
CB_CA	1101	LOW	HIGH	LOW	HIGH	PWM	LOW
CA	1100	LOW	HIGH	LOW	LOW	PWM	LOW
CA_BA	1001	LOW	HIGH	PWM	LOW	PWM	LOW
BA	1000	LOW	HIGH	PWM	LOW	LOW	LOW
BA_BC	1011	LOW	HIGH	PWM	LOW	LOW	HIGH
BC	1010	LOW	LOW	PWM	LOW	LOW	HIGH
BC_AC	0011	PWM	LOW	PWM	LOW	LOW	HIGH
AC	0010	PWM	LOW	LOW	LOW	LOW	HIGH
AC_AB	0111	PWM	LOW	LOW	HIGH	LOW	HIGH
Align	1110	PWM	LOW	LOW	HIGH	LOW	HIGH
Stop	0000	LOW	LOW	LOW	LOW	LOW	LOW

7.3.3 VCPH Charge Pump: High-Side Gate Supply

The DRV8305-Q1 uses a charge pump to generate the proper gate-to-source voltage bias for the high-side N-channel MOSFETs. Similar to the often used bootstrap architecture, the charge pump generates a floating supply voltage used to enable the MOSFET. When enabled, the gate of the external MOSFET is connected to VCPH through the internal gate drivers. The charge pump of the DRV8305-Q1 regulates the VCPH supply to PVDD + 10-V in order to support both standard and logic level MOSFETs. As opposed to a bootstrap architecture, the charge pump supports 0 to 100% duty cycle operation by eliminating the need to refresh the bootstrap capacitor. The charge pump also removes the need for bootstrap capacitors to be connected to the switch-node of the half-bridge.

In order to support automotive cold crank transients on the battery which require the system to be operational to as low as 4.4 V, a regulated triple charge pump scheme is used to create sufficient V_{GS} to drive standard and logic level MOSFETs during the low voltage transient. Between 4.4 to 18 V the charge pump regulates the voltage in a tripler mode. Beyond 18 V and until the max operating voltage, it switches over to a doubler mode in order to improve efficiency. The charge pump is disabled until EN_GATE is set high to reduce unneeded power consumption by the IC. After EN_GATE is set high, the device will go through a power up sequence to enable the gate drivers and gate drive supplies. 1 ms should be allocated after EN_GATE is set high to allow the charge pump to reach its regulation voltage.

The charge pump is continuously monitored for undervoltage and overvoltage conditions to prevent underdriven or overdriven MOSFET scenarios. If an undervoltage or overvoltage condition is detected the appropriate actions is taken and reported through the SPI registers.

7.3.4 VCP_LSD LDO: Low-Side Gate Supply

The DRV8305-Q1 uses a linear regulator to generate the proper gate-to-source voltage vias for the low-side N-channel MOSFETs. The linear regulator generates a fixed 10-V supply voltage with respect to GND. When enabled, the gate of the external MOSFET is connected to VCPH_LSD through the internal gate drivers. In order to support automotive cold crank transients the input voltage for the VCP_LSD linear regulator is taken from the VCPH charge pump. This allows the DRV8305-Q1 to provide sufficient V_{GS} to drive standard and logic level MOSFETs during the low voltage transient.

The low-side regulator is disabled until EN_GATE is set high to reduce unneeded power consumption by the IC. After EN_GATE is set high, the device will go through a power up sequence for the gate drivers and gate drive supplies. 1 ms should be allocated after EN_GATE is set high to allow the low-side regulator to reach its regulation voltage. The VCP_LSD regulator is continuously monitored for undervoltage conditions to prevent underdriven MOSFET scenarios. If an undervoltage condition is detected the appropriate actions is taken and reported through the SPI registers.

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7.3.5 GHx/GLx: Half-Bridge Gate Drivers

The DRV8305-Q1 gate driver uses a complimentary push-pull topology for both the high-side and the low-side gate drivers. Both the high-side (GHx to SHx) and the low-side (GLx to SLx) are implemented as floating gate drivers in order to tolerate switching transients from the half-bridges. The high-side and low-side gate drivers use a highly adjustable current control scheme in order to allow the DRV8305-Q1 to adjust the V_{DS} slew rate of the external MOSFETs without the need for additional components. The scheme also incorporates a mechanism for detecting issues with the gate drive output to the power MOSFETs during operation. This scheme and its application benefits are outlined below as well as in the *Understanding IDRIVE and TDRIVE in TI Motor Gate Drivers* application report.

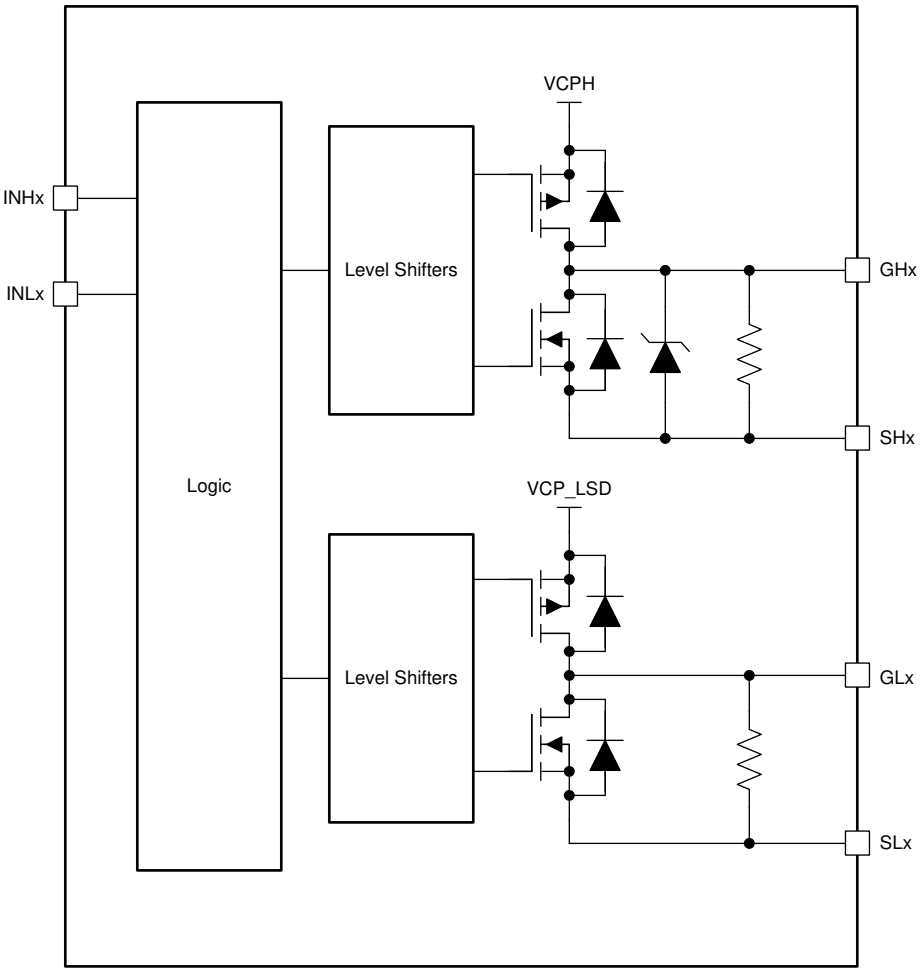


Figure 9. DRV8305-Q1 Gate Driver Architecture

7.3.5.1 Smart Gate Drive Architecture: IDRIVE

The first component of the gate drive architecture implements adjustable current control for the gates of the external power MOSFETs. This feature allows the gate driver to control the V_{DS} slew rate of the MOSFETs by adjusting the gate drive current. This is realized internally to reduce the need for external components inline with the gates of the MOSFETs. The DRV8305-Q1 provides 12 adjustable source and sink current levels for the high-side (the high-sides of all three phases share the same setting) and low-side gate drivers (the low-sides of all three phases share the same settings). The gate drive levels are adjustable through the SPI registers in both the standby and operating states. This flexibility allows the system designer to tune the performance of the driver for different operating conditions through software alone.

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The gate drivers are implemented as temperature compensated, constant current sources up to the 80-mA (sink)/70-mA (source) current settings in order to maintain the accuracy required for precise slew rate control. The current source architecture helps eliminate the temperature, process, and load-dependent variation associated with internal and external series limiting resistors. Beyond that, internal switches are adjusted to create the desired settings up to the 1.25-A (sink)/1-A (source) settings. For higher currents, internal series switches are used to minimize the power losses associated with mirroring such large currents.

Control of the gate current during the MOSFET Miller region is a key component for adjusting the MOSFET V_{DS} rise and fall times. MOSFET V_{DS} slew rates are a critical parameter for optimizing emitted radiations, energy and duration of diode recovery spikes, dV/dt related turn on leading to shoot-through, and voltage transients related to parasitics.

When a MOSFET is enhanced, three different charges must be supplied to the MOSFET gate. The MOSFET drain to source voltage will slew primarily during the Miller region. By controlling the rate of charge to the MOSFET gate (gate drive current strength) during the Miller region, it is possible to optimize the VDS slew rate for the reasons mentioned.

1. Q_{GS} = Gate-to-source charge
2. Q_{GD} = Gate-to-drain charge (Miller charge)
3. Remaining Q_G

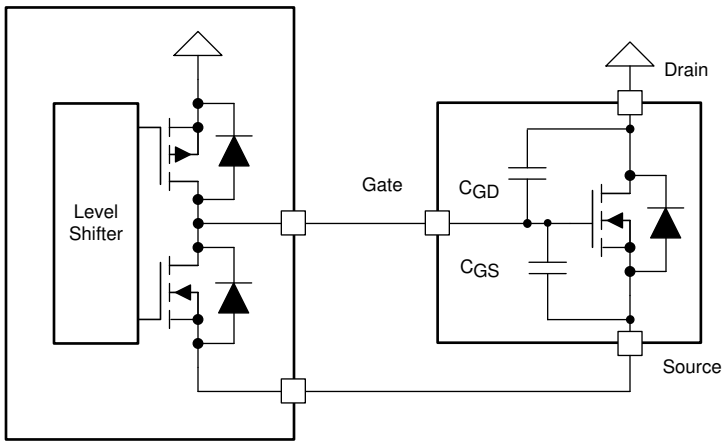


Figure 10. MOSFET Charge Example

7.3.5.2 Smart Gate Drive Architecture: TDRIVE

The DRV8305-Q1 gate driver uses an integrated state machine (TDRIVE) in the gate driver to protect against excessive current on the gate drive outputs, shoot-through in the external MOSFET, and dV/dt turn on due to switching on the phase nodes. The TDRIVE state machine allows for the design of a robust and efficient motor drive system with minimal overhead.

The state machine incorporates internal handshaking when switching from the low to the high-side external MOSFET or vice-versa. The handshaking is designed to prevent the external MOSFETs from entering a period of cross conduction, also known as shoot-through. The internal handshaking uses the V_{GS} monitors of the DRV8305-Q1 to determine when one MOSFET has been disabled and the other can be enabled. This allows the gate driver to insert an optimized dead time into the system without the risk of cross conduction. Any dead time added externally through the MCU or SPI register will be inserted after the handshake process.

The state machine also incorporates a gate drive timer to ensure that under abnormal circumstances such as a short on the MOSFET gate or the inadvertent turn on of a MOSFET V_{GS} clamp, the high peak current through the DRV8305-Q1 and MOSFET is limited to a fixed duration. This concept is visualized in the figure below. First, the DRV8305-Q1 receives a command to enable or disable the MOSFET through INHx or INLx inputs. Second, the gate driver is enabled and a strong current is applied to the MOSFET gate and the gate voltage begins to

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change. If the gate voltage has not changed to the desired level after the t_{DRIVE} period (indicating a short circuit or overcurrent condition on the MOSFET gate), the DRV8305-Q1 signals a gate drive fault and the gate drive is disabled to help protect the external MOSFET and DRV8305-Q1. If the MOSFET does successfully enable or disable, after the t_{DRIVE} period the DRV8305-Q1 will enable a lower hold current to ensure the MOSFET remains enabled or disabled and improve efficiency of the gate drive.

Select a t_{DRIVE} time that is longer than the time needed to charge or discharge the gate capacitances of the external MOSFETs. The TDRIVE SPI registers should be configured so that the MOSFET gates are charged completely within t_{DRIVE} during normal operation. If t_{DRIVE} is too low for a given MOSFET, then the MOSFET may not turn on completely. It is suggested to tune these values in-system with the required external MOSFETs to determine the best possible setting for the application. A good starting value is a t_{DRIVE} period that is 2x the expected rise or fall times of the external MOSFET gates. Note that TDRIVE will not increase the PWM time and will simply terminate if a PWM command is received while it is active.

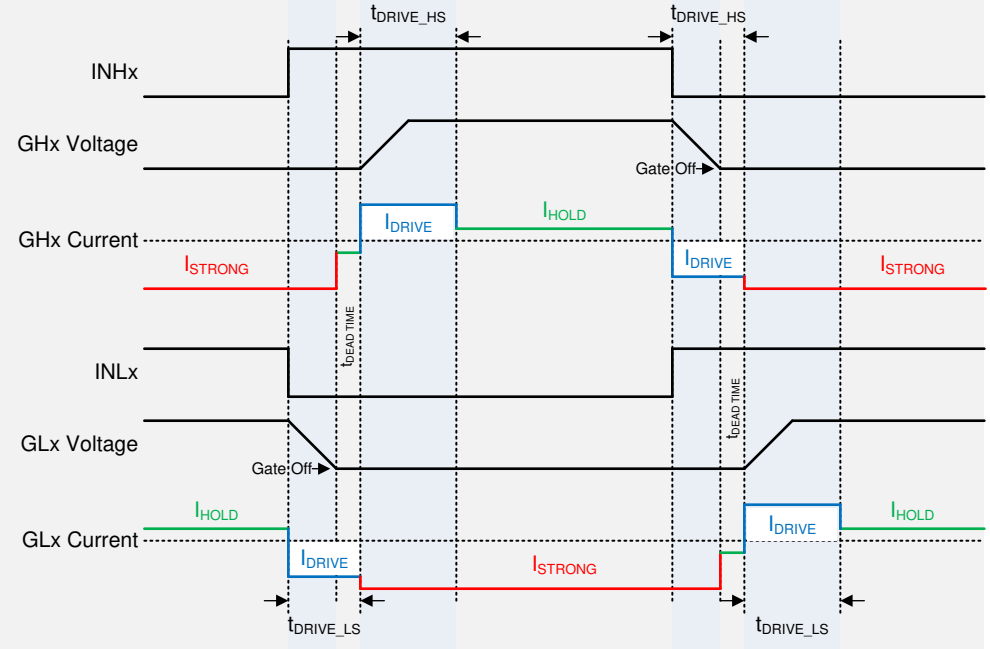


Figure 11. TDRIVE Gate Drive State Machine

7.3.5.3 CSAs: Current Shunt Amplifiers

The DRV8305-Q1 includes three high performance low-side current shunt amplifiers for accurate current measurement utilizing low-side shunt resistors in the external half-bridges. They are commonly used to measure the motor phase current to implement overcurrent protection, external torque control, or external commutation control through the application MCU.

The current shunt amplifiers have the following features:

- Each of the three current sense amplifiers can be programmed and calibrated independently.
- Can provide output bias up to 2.5 V to support bidirectional current sensing.
- May be used for either individual or total current shunt sensing.
- Four programmable gain settings through SPI registers (10, 20, 40 and 80 V/V).
- Reference voltage for output bias provided from voltage regulator VREG for DRV83053Q and DRV83055Q.
- Reference voltage for output bias provided from externally applied voltage on VREG pin for DRV8305NQ and DRV8305NE.
- Programmable output bias scaling. The scaling factor k can be programmed through SPI registers (1/2 or 1/4).
- Programmable blanking time (delay) of the amplifier outputs. The blanking time is implemented from any rising or falling edge of gate drive outputs. The blanking time is applied to all three current sense amplifiers equally. In case the current sense amplifiers are already being blanked when another gate driver rising or

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falling edge is seen, the blanking interval will be restarted at the edge. Note that the blanking time options do not include delay from internal amplifier loading or delays from the trace or component loads on the amplifier output. The programmable blanking time may be overridden to have no delay (default value).

- Minimize DC offset and drift through temperature with DC calibrating through SPI register. When DC calibration is enabled, device will short input of current shunt amplifier and disconnect the load. DC calibrating can be done at anytime, even when the MOSFET is switching because the load is disconnected. For best result, perform the DC calibrating during switching off period when no load is present to reduce the potential noise impact to the amplifier.

The output of current shunt amplifier can be calculated as:

$$V_O = \frac{V_{VREF}}{k} - G \times (SN_X - SP_X) \quad (1)$$

where

- VREF is the reference voltage from the VREG pin.
- G is the gain setting of the amplifier.
- k = 2, 4, or 8
- SN_x and SP_x are the inputs of channel x.
- SP_x should connect to the low-side (ground) of the sense resistor for the best common mode rejection.
- SN_x should connect to the high-side (LS MOSFET source) of the sense resistor.

Figure 12 shows current amplifier simplified block diagram.

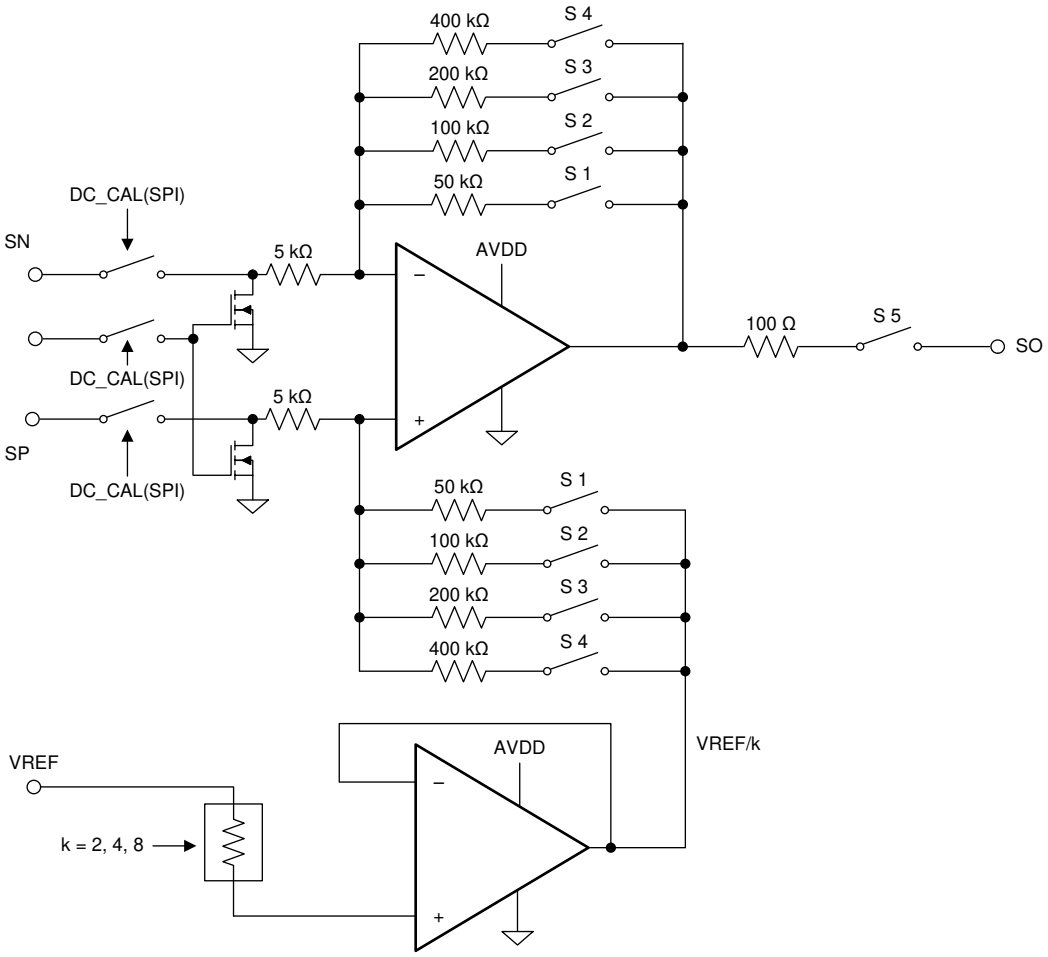


Figure 12. Current Shunt Amplifier Simplified Block Diagram

7.3.6 DVDD and AVDD: Internal Voltage Regulators

The DRV8305-Q1 has two internal regulators, DVDD and AVDD, that power internal circuitry. These regulators cannot be used to drive external loads and may not be supplied externally.

DVDD is the voltage regulator for the internal logic circuits and is maintained at a value of 3.3 V through the entire operating range of the device. DVDD is derived from the PVDD power supply. DVDD should be bypassed externally with a 1-µF capacitor to GND.

AVDD is the voltage regulator that provides the voltage rail for the internal analog circuit blocks including the current sense amplifiers and is maintained at a value 5 V. AVDD is derived from the PVDD voltage power supply. AVDD should be bypassed externally with a 1-µF capacitor to GND.

Because the allowed PVDD operating range of the device permits operation below the nominal value of AVDD, this regulator operates in two regimes: namely a linear regulating regime and a dropout region. In the dropout region, the AVDD will simply track the PVDD voltage minus a voltage drop.

If the device is expected to operate within the dropout region, take care while selecting current sense amplifier components and settings to accommodate the reduced voltage rail.

7.3.7 VREG: Voltage Regulator Output

The DRV8305-Q1 integrates a 50-mA, LDO voltage regulator (VREG) that is dedicated for driving external loads such as an MCU directly. The VREG regulator also supplies the reference for the SDO output of the SPI bus and the voltage reference for the amplifier output bias. The three different DRV8305-Q1 device versions provide different configurations for the VREG output. For the DRV83053Q, the VREG output is regulated at 3.3 V. For the DRV83055Q, the VREG output is regulated at 5 V. For the DRV8305NQ and DRV8305NE, the VREG voltage regulator is disabled (VREG pin used for reference voltage) and the reference voltage for SDO and the amplifier output bias must be supplied from an external supply to the VREG pin.

The DRV8305-Q1 VREG voltage regulator also features a PWRGD pin to protect against brownouts on externally driven devices. The PWRGD pin is often tied to the reset pin of a microcontroller to ensure that the microcontroller is always reset when the VREG output voltage is outside of its recommended operation area.

When the voltage output of the VREG regulator drops or exceeds the set threshold (programmable).

- The PWRGD pin will go low for a period of 56 µs.
- After the 56-µs period has expired, the VREG voltage will be checked and PWRGD will be held low until the VREG voltage has recovered.

The voltage regulator also has undervoltage protection implemented for both the input voltage (PVDD) and output voltage (VREG).

7.3.8 Protection Features

7.3.8.1 Fault and Warning Classification

The DRV8305-Q1 integrates extensive error detection and monitoring features. These features allow the design of a robust system that can protect against a variety of system related failure modes. The DRV8305-Q1 classifies error events into two categories and takes different device actions dependent on the error classification.

The first error class is a *Warning*. There are several types of conditions that are classified as warning only. Warning errors are report only and the DRV8305-Q1 will take no other action effecting the gate drivers or other blocks. When a warning condition occurs it will be reported in the corresponding SPI status register bit and on the nFAULT pin with a repeating 56-µs pulse low followed by a 56-µs pulse high. A warning error can be cleared by an SPI read to the corresponding status register bit. The same warning will not be reported through the nFAULT pin again unless that warning or condition passes and then reoccurs.

- A warning error is reported on the nFAULT pin with a repeating 56-µs pulse low followed by a 56-µs pulse high.
- The warning is reported on the nFAULT pin until a SPI read to the corresponding status register.
- The SPI read will clear the nFAULT report, but the SPI register will remain asserted until the condition has passed.
- The nFAULT pin will report a new warning if the condition clears and then occurs again.

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The second error class is a *Fault*. Fault errors will trigger a shutdown of the gate driver with its major blocks and are reported by holding nFAULT low with the corresponding status register asserted. Fault errors are latched until the appropriate recovery sequence is performed.

- A fault error is reported by holding the nFAULT pin low and asserting the FAULT bit in register 0x1.
- The error type will also be asserted in the SPI registers.
- A fault error is a latched fault and must be cleared with the appropriate recovery sequence.
- If a fault occurs during a warning error, the fault error will take precendence, latch nFAULT low and shutdown the gate driver.
- The output MOSFETs will be placed into their high impedance state in a fault error event.
- To recover from a fault type error, the condition must be removed and the CLR_FLTs bit asserted in register 0x9, bit D1 or an EN_GATE reset pulse issued.
- The CLR_FLTS bit self clears to 0 after fault status reset and nFAULT pin is released.

There are two exceptions to the fault and warning error classes. The first exception is the temperature flag warnings (TEMP_FLAGX). A Temperature Flag warning will not trigger any action on the nFAULT pin and the corresponding status bit will be updated in real time. See the overtemperature section for additional information. The second exception is the *MCU Watchdog* and *VREG Undervoltage (VREG_UV)* faults. These are reported on the PWRGD pin to protect the system from lock out and brownout conditions. See their corresponding sections for additional information.

Note that nFAULT is an open-drain signal and must be pulled up through an external resistor.

7.3.8.2 MOSFET Shoot-Through Protection (TDRIVE)

DRV8305-Q1 integrates analog handshaking and digital dead time to prevent shoot-through in the external MOSFETs.

- An internal handshake through analog comparators is performed between each high-side and low-side MOSFET switching transaction (see *Smart Gate Drive Architecture: TDRIVE*). The handshake monitors the voltage between the gate and source of the external MOSFET to ensure the device has reached its cutoff threshold before enabling the opposite MOSFET.
- A minimum dead time (digital) of 40 ns is always inserted after each successful handshake. This digital dead time is programmable through the DEAD_TIME SPI setting in register 0x7, bits D6-D4 and is in addition to the time taken for the analog handshake.

7.3.8.3 MOSFET Overcurrent Protection (VDS_OCP)

To protect the system and external MOSFET from damage due to high current events, V_{DS} overcurrent monitors are implemented in the DRV8305-Q1.

The V_{DS} sensing is implemented for both the high-side and low-side MOSFETs through the pins below:

- High-side MOSFET: V_{DS} measured between VDRAIN and SHx pins.
- Low-side MOSFET: V_{DS} measured between SHx and SLx pins.

Based on the $R_{DS(on)}$ of the power MOSFETs and the maximum allowed I_{DS}, a voltage threshold can be calculated, which when exceeded, triggers the V_{DS} overcurrent protection feature. The voltage threshold level (VDS_LEVEL) is programmable through the SPI VDS_LEVEL setting in register 0xC, bits D7-D3 and may be changed during gate driver operation if needed.

The V_{DS} overcurrent monitors implement adjustable blanking and deglitch times to prevent false trips due to switching voltage transients. The V_{DS} blanking time (t_{BLANK}) is inserted digitally and programmable through the SPI TBLANK setting in register 0x7, bits D3-D2. The t_{BLANK} time is inserted after each switch ON transistion (LOW to HIGH) of the output gate drivers is commanded. During the t_{BLANK} time, the V_{DS} comparators are not being monitored in order to prevent false trips when the MOSFET first turns ON. After the t_{BLANK} time expires the overcurrent monitors will begin actively watching for an overcurrent event.

The V_{DS} deglitch time (t_{VDS}) is inserted digitally and programmable through the SPI TVDS setting in register 0x7, bits D1-D0. The t_{VDS} time is a delay inserted after the V_{DS} sensing comparators have tripped to when the protection logic is informed that a V_{DS} event has occurred. If the overcurrent event does not persist through t_{VDS} delay then it will be ignored by the DRV8305-Q1.

Note that the dead time and blanking time are overlapping timers as shown in Figure 13.

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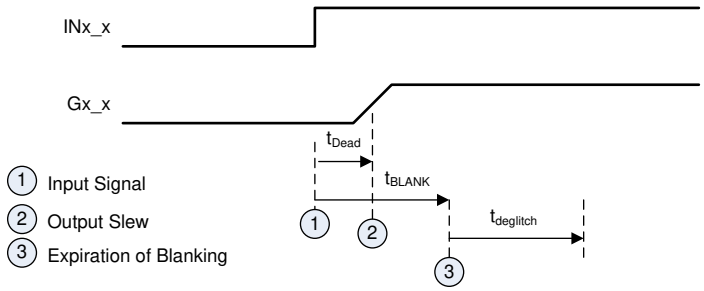


Figure 13. V_{DS} Deglitch and Blank Diagram

The DRV8305-Q1 has three possible responses to a V_{DS} overcurrent event. This response is set through the SPI VDS_MODE setting in register 0xC, bits D2-D0.

- **V_{DS} Latched Shutdown Mode:**
  When a V_{DS} overcurrent event occurs, the device will pull all gate drive outputs low in order to put all six external MOSFETs into high impedance mode. The fault will be reported on the nFAULT pin with the specific MOSFET in which the overcurrent event was detected in reported through the SPI status registers.
- **V_{DS} Report Only Mode:**
  In this mode, the device will take no action related to the gate drivers. When the overcurrent event is detected the fault will be reported on the nFAULT pin with the specific MOSFET in which the overcurrent event was detected in reported through the SPI status registers. The gate drivers will continue to operate normally.
- **V_{DS} Disabled Mode:**
  The device ignores all the V_{DS} overcurrent event detections and does not report them.

7.3.8.3.1 MOSFET dV/dt Turn On Protection (TDRIVE)

The DRV8305-Q1 gate driver implements a strong pulldown scheme during turn on of the opposite MOSFET for preventing parasitic dV/dt turn on. Parasitic dV/dt turn on can occur when charge couples into the gate of the low-side MOSFET during a switching event. If the charge induces enough voltage to cross the threshold of the low-side MOSFET shoot-through can occur in the half-bridge. To prevent this the *Smart Gate Drive Architecture: TDRIVE* state machine turns on a strong pulldown during switching. After the switching event has completed, the gate driver switches back to a lower hold off pulldown to improve efficiency.

7.3.8.3.2 MOSFET Gate Drive Protection (GDF)

The DRV8305-Q1 uses a multilevel scheme to protect the external MOSFET from V_{GS} voltages that could damage it. The first stage uses integrated V_{GS} clamps that will turn on when the GHx voltage exceeds the SHx voltage by a value that could be damaging to the external MOSFETs.

The second stage relies on the TDRIVE state machine to detect when abnormal conditions are present on the gate driver outputs. After the TDRIVE timer has expired the gate driver performs a check of the gate driver outputs against the commanded input. If the two do not match a gate drive fault (FETXX_VGS) is reported. This can be used to detected gate short to ground or gate short to supply event. The TDRIVE timer is adjustable for the high-side and low-side gate drive outputs through the TDRIVEN setting in register 0x5, bits D9-D8 and the TDRIVEP setting in register 0x6, bits D9-D8. The gate fault detection through TDRIVE can be disabled through the DIS_GDRV_FAULT setting in register 0x9, bit D8.

The third stage uses undervoltage monitors for the low-side gate drive regulator (VCP_LSD_UVLO2) and high-side gate drive charge pump (VCPH_UVLO2) and an overvoltage monitor for high-side charge pump (VCPH_OVLO). These monitors are used to detect if any of the power supplies to the gate drivers have encountered an abnormal condition.

7.3.8.4 Low-Side Source Monitors (SNS_OCP)

In additional to the V_{DS} monitors across each MOSFET, the DRV8305-Q1 directly monitors the voltage on the SLx pins with respect to ground. If high current events such phase shorts cause the SLx pin voltage to exceed 2 V, the DRV8305-Q1 will shutdown the gate driver, put the external MOSFETs into a high impedance state, and report a SNS_OCP fault error on the nFAULT pin and corresponding SPI status bit in register 0x2, bits D2-D0.

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7.3.8.5 Fault and Warning Operating Modes

Table 6. Fault and Warning Operating Modes(1)

NAME	CONDITION	GATE DRIVE OUTPUTS	GATE DRIVE SUPPLIES	INTERNAL LOGIC	DEVICE ACTION
PVDD Undervoltage Fault (PVDD_UVLO)	PVDD < V_{PVDD_UVLO1}	PL	D	D	-
	PVDD < V_{PVDD_UVLO2}	PL	D	E	SPI nFAULT Latch
PVDD Undervoltage Warning (PVDD_UVFL)	PVDD < V_{PVDD_UVFL}	E	E	E	SPI nFAULT Toggle
PVDD Overvoltage Warning (PVDD_OVFL)	PVDD > V_{PVDD_OVFL}	E	E	E	SPI nFAULT Toggle
Charge Pump Undervoltage Warning (VCPH_UVFL)	VCPH < V_{VCPH_UVFL}	E	E	E	SPI nFAULT Toggle
Charge Pump Undervoltage Fault (VCPH_UVLO2)	VCPH < V_{VCPH_UVLO2}	PL	D	E	SPI nFAULT Latch
LS Gate Supply Undervoltage Fault (VCP_LSD_UVLO2)	VCP_LSD < $V_{VCP_LSD_UVLO2}$	PL	D	E	SPI nFAULT Latch
Charge Pump Overvoltage Fault (VCPH_OVLO)	VCPH > V_{VCPH_OVLO}	PL	D	E	SPI nFAULT Latch
	VCPH > $V_{VCPH_OVLO_ABS}$	PL	D	E	SPI nFAULT Latch
AVDD Undervoltage Fault (AVDD_UVLO)	AVDD < V_{AVDD_UVLO}	PL	D	E	SPI nFAULT Latch
Temperature Flag Warning (TEMP_FLAGX)	T_J > T_{TEMP_FLAGX}	E	E	E	SPI
Overtemperature Warning (OTW)	T_J > T_{OTW}	E	E	E	SPI nFAULT Toggle
Overtemperature Shutdown Fault (OTSD)	T_J > T_{OTSD}	PL	D	E	SPI nFAULT Latch
MOSFET Overcurrent Fault (VDS_OCP)	Latched Shutdown V_{DS} > V_{VDS_LEVEL}	PL	E	E	SPI nFAULT Latch
	Report Only V_{DS} > V_{VDS_LEVEL}	E	E	E	SPI nFAULT Toggle
	Disabled V_{DS} > V_{VDS_LEVEL}	E	E	E	-
LS Overcurrent Fault (SNS_OCP)	SLx > V_{SNS_OCP}	PL	E	E	SPI nFAULT Latch
Gate Drive Fault (GDF)	See TDRIVE	PL	D	E	SPI nFAULT Latch
MCU Watchdog Fault (WD_FAULT)	$t_{INTERVAL}$ > t_{WD_DLY}	PL	E	E	SPI PWRGD nFAULT Latch
VREG Undervoltage Fault (VREG_UV)	VREG < V_{VREG_UV}	PL	E	E	SPI PWRGD nFAULT Latch

(1) E - Enabled, PL = Pulled Low, D = Disabled

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7.3.9 Undervoltage Warning (UVFL), Undervoltage Lockout (UVLO), and Overvoltage (OV) Protection

The DRV8305-Q1 implements undervoltage and overvoltage monitors on its system supplies to protect the system, prevent brownout conditions, and prevent unexpected device behavior. Undervoltage is monitored for on the PVDD, AVDD, VREF, VCPH, and VCP_LSD power supplies. Overvoltage is monitored for on the PVDD and VCPH power supplies. The values for the various undervoltage and overvoltage levels are provided in the *Electrical Characteristics* table under the voltage protection section.

The monitors for the main power supply, PVDD, incorporates several additional features:

- Undervoltage warning (PVDD_UVFL) level. Device operation is not impacted, report only indication.
- PVDD_UVFL is warning type error indicated on the nFAULT pin and the PVDD_UVFL status bit in register 0x1, bit D7.
- Independent UVLO levels for the gate driver (PVDD_UVLO2) and VREG LDO regulator (PVDD_UVLO1). PVDD_UVLO2 will trigger a shutdown of the gate driver.
- PVDD_UVLO2 is a fault type error indicated on the nFAULT pin and corresponding status bit in register 0x3, bit D10.
- PVDD_UVLO2 may be disabled through the DIS_VPVDD_UVLO setting in register 0x9, bit D9. The fault will still be reported in the status bit in register 0x3, bit D10.
- Overvoltage detection to monitor for load dump or supply pumping conditions. Device operation is not impacted, report only indication.
- PVDD_OV is a warning type error indicated on the nFAULT pin and the PVDD_OV bit in register 0x1, bit D6.

The monitors for the high-side charge pump supply, VCPH, and low-side supply (VCP_LSD) incorporate several additional features:

- VCPH relative (VCPH_OVLO) and absolute overvoltage (VCPH_OVLO_ABS) detection. The DRV8305-Q1 monitors VCPH for overvoltage conditions with respect to PVDD and GND.
- VCPH_OVLO and VCPH_OVLO_ABS are fault type errors reported on nFAULT and the corresponding status bit in register 0x3, bits D1-D0.
- VCPH undervoltage (VCPH_UVLO2) is monitored to prevent underdriven MOSFET conditions. VCPH_UVLO2 will trigger a shutdown of the gate driver.
- VCPH_UVLO2 is a fault type error indicated on the nFAULT pin and corresponding status bit in register 0x3, bit D2.
- VCP_LSD undervoltage (VCP_LSD_UVLO2) is monitored to prevent underdriven MOSFET conditions. VCP_LSD_UVLO2 will trigger a shutdown of the gate driver.
- VCP_LSD_UVLO2 is a fault type error indicated on the nFAULT pin and corresponding status bit in register 0x3, bit D4.
- Undervoltage protection for VCPH and VCP_LSD may not be disabled in the operating state.

7.3.9.1 Overtemperature Warning (OTW) and Shutdown (OTSD) Protection

A multi-level temperature detection circuit is implemented in the DRV8305-Q1.

- Flag Level 1 (TEMP_FLAG1): Level 1 overtemperature flag. No warning reported on nFAULT. Real-time flag indicated in SPI register 0x1, bit D3.
- Flag Level 2 (TEMP_FLAG2): Level 2 overtemperature flag. No warning reported on nFAULT. Real-time flag indicated in SPI register 0x1, bit D2.
- Flag Level 3 (TEMP_FLAG3): Level 3 overtemperature flag. No warning reported on nFAULT. Real-time flag indicated in SPI register 0x1, bit D1.
- Flag Level 4 (TEMP_FLAG4): Level 4 overtemperature flag. No warning reported on nFAULT. Real-time flag indicated in SPI register 0x1, bit D8.
- Warning Level (OTW): Overtemperature warning only. Warning reported on nFAULT. Real-time flag indicated in SPI register 0x1, bit D0.
- Fault Level (OTSD): Overtemperature fault and latched shut down of the device. Fault reported on nFAULT and in SPI register 0x3, bit D8.

SPI operation is still available and register settings will be retained in the device during OTSD operation as long as PVDD is within operation range. An OTSD fault can be cleared when the device temperature has dropped below the fault level and a CLR_FLTS is issued.

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7.3.9.2 Reverse Supply Protection

The DRV8305-Q1 is designed to support an external reverse supply protection scheme. The VCPH high-side charge pump is able to supply an external load up to 10 mA. This feature allows implementation of an external reverse battery protection scheme using a MOSFET and a BJT. The MOSFET gate and BJT can be driven through VCPH with a current limiting resistor. The current limiting resistor must be sized not to exceed the maximum external load on VCPH.

The VDRAIN sense pin may also be protected against reverse supply conditions by use of a current limiting resistor. The current limit resistor must be sized not to exceed the maximum current load on the VDRAIN pin. 100 Ω is recommended between VDRAIN and the drain of the external high-side MOSFET.

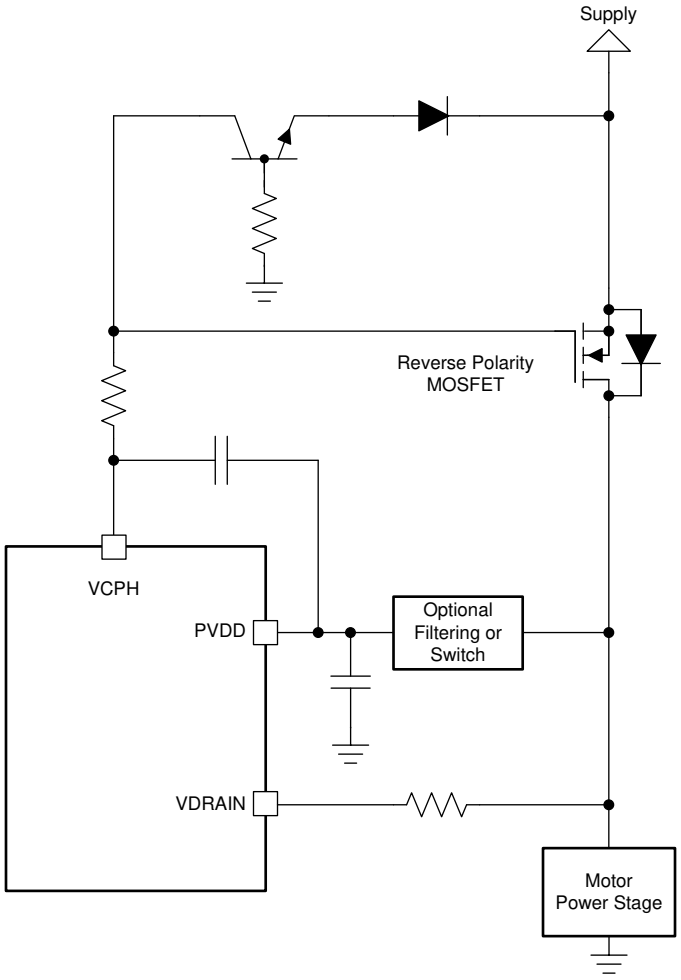


Figure 14. Typical Scheme for Reverse Battery Protection Using VCPH

7.3.9.3 MCU Watchdog

The DRV8305-Q1 incorporates an MCU watchdog function to ensure that the external controller that is instructing the device is active and not in an unknown state. The MCU watchdog function may be enabled by writing a 1 to the WD_EN setting in the SPI register 0x9, bit D3. The default setting for the device is with the watchdog disabled. When the watchdog is enabled, an internal timer starts to countdown to the interval set by the WD_DLY setting in the SPI register 0x9, bits D6-D5. To restart the watchdog timer, the address 0x1 (status register) must be read by the controller within the interval set by the WD_DLY setting. If the watchdog timer is allowed to expire without the address 0x1 being read, a watchdog fault will be enabled.

Response to a watchdog fault is as follows:

- A latched fault occurs on the DRV8305-Q1 and the gate drivers are put into a safe state. An appropriate recovery sequence must then be performed.

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- The PWRGD pin is taken low for 56 µs and then back high in order to reset the controller or indicate the watchdog fault.
- The nFAULT pin is asserted low, the WD_EN bit is cleared, and the WD_FAULT set high in register 0x3, bit D9.
- It is recommended to read the status registers as part of the recovery or power-up routine in order to determine whether a WD_FAULT had previously occurred.

Note that the watchdog fault results in a clearing of the WD_EN setting and it will have to be set again to resume watchdog functionality.

7.3.9.4 VREG Undervoltage (VREG_UV)

The DRV8305-Q1 has an undervoltage monitor on the VREG output regulator to ensure the external controller does not experience a brownout condition. The undervoltage monitor will signal a fault if the VREG output drops below a set threshold from its set point. The VREG output set point is configured for two different levels, 3.3 V or 5 V, depending on the DRV8305-Q1 device options (DRV83053Q and DRV83055Q). The VREG undervoltage level can be set through the SPI setting VREG_UV_LEVEL in register 0xB, bits D1-D0. The VREG undervoltage monitor can be disabled through the SPI setting DIS_VREG_PWRGD in register 0xB, bit D2.

Response to a VREG undervoltage fault is as follows:

- A latched fault occurs on the DRV8305-Q1 and the gate drivers are put into a safe state. An appropriate recovery sequence must then be performed.
- The PWRGD is taken low until the undervoltage condition is removed and for at least a minimum of 56 µs.
- The nFAULT pin is asserted low and the VREG_UV bit set high in register 0x3, bit D6.
- The fault can be cleared after the VREG undervoltage condition is removed with CLR_FLTS or an EN_GATE reset pulse.

Note that the VREG undervoltage monitor is disabled on the no regulator (VREF) device option (DRV8305NQ and DRV8305NE).

7.3.9.5 Latched Fault Reset Methods

A latched fault can be cleared after the fault condition is removed by either setting the CLR_FLTS register bit in register 0x09 to 1 or by issuing an EN_GATE reset pulse to the DRV8305-Q1. The CLR_FLTS register bit will automatically reset back to 0 have the fault has been cleared.

The secondary method through the EN_GATE pin requires a high-low-high pulse on the pin to clear the latched fault. The low duration of the pulse should be greater than or equal to 1µs.

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7.4 Device Functional Modes

7.4.1 Power Up Sequence

The DRV8305-Q1 has an internal state machine to ensure proper power up and power down sequencing of the device. When PVDD power is applied the device will remain inactive until PVDD cross the digital logic threshold. At this point, the digital logic will become active, VREG will enable (if 3.3-V or 5-V device option is used), the passive gate pulldowns will enable, and nFAULT will be driven low to indicate that the device has not reached the V_{PVDD_UVLO2} threshold. nFAULT will remain driven low until PVDD crosses the PVDD_UVLO threshold. At this point the device will enter its standby state.

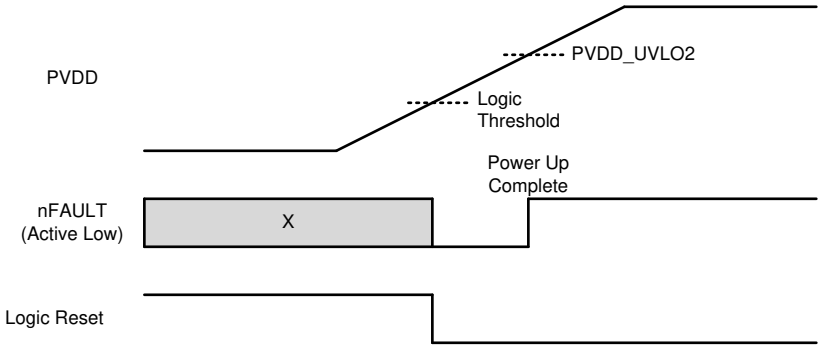


Figure 15. Power-Up Sequence

7.4.2 Standby State

After the power up sequence is completed and the PVDD voltage is above V_{PVDD_UVLO2} threshold, the DRV8305-Q1 will indicate successful and fault free power up of all circuits by releasing the nFAULT pin. At this point the DRV8305-Q1 will enter its standby state and be ready to accept inputs from the external controller. The DRV8305-Q1 will remain in or re-enter its standby state anytime EN_GATE = LOW or a fault type error has occured. In this state the major gate driver blocks are disabled, but the passive gate pulldowns are still active to maintain the external MOSFETs in their high-impedence state. It is recommended, but not required to perform all device configurations through SPI in the standby state.

7.4.3 Operating State

After reaching the standby state and then taking EN_GATE from LOW to HIGH, the DRV8305-Q1 will enter its operating state. The operating state enables the major gate driver and current shunt amplifier blocks for normal operation. 1 ms should be allowed after EN_GATE is taken HIGH to allow the charge pump supply for the high-side gate drivers to reach its steady state operating point. If at any point in its operating state a fault type error occurs, the DRV8305-Q1 will immediately re-enter the standby state.

7.4.4 Sleep State

The sleep state can be entered by issuing a sleep command through the SLEEP bit in SPI register 0x9, bit D2 with the device in its standby state (EN_GATE = LOW). The device will not respond to a sleep command in its operating state. After the sleep command is received, the gate drivers and output regulator (VREG) will safely power down after a programmable delay set in the SPI register 0xB, bits D4-D3. The device can then only be enabled through the WAKE pin which is a high-voltage tolerant input pin. For the DRV8305-Q1 to be brought out of sleep, the WAKE pin must be at a voltage greater than 3 V. This allows the wake pin to be driven, for example, directly by the battery through a switch, through the inhibit pin (INH) on a standard LIN interface, or through standard digital logic. The WAKE pin will only react to a wake up command if PVDD > V_{PVDD_UVLO2}. After the DRV8305-Q1 is out of SLEEP mode, all activity on the WAKE pin is ignored. The sleep state erases all values in the SPI control registers and it is not recommended to write through SPI in the sleep state.

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Device Functional Modes (continued)

7.4.5 Limp Home or Fail Code Operation

The DRV8305-Q1 enables the adoption of secondary limp-home or fail code software through configurable fault mode handling. The following device features may be configured during the operating state without stopping the motor.

- IDRIVE Gate Current Output (IDRIVEN_HS, IDRIVEP_HS, IDRIVEN_LS, IDRIVEP_LS): All four IDRIVEX settings may be adjusted during normal operation without issue. This features allows the software to change the slew rate, switching characteristics of the external MOSFETs on the fly if required without having to stop the motor rotation. The IDRIVEX settings are located in the SPI registers 0x5 (high-side) and 0x6 (low-side).
- VDS Fault Mode (VDS_MODE): The V_{DS} overcurrent monitors may be changed from latched shutdown (VDS_MODE = b'000) or report only (VDS_MODE = b'001) modes to disabled (VDS_MODE = b'010) mode to allow operation of the external MOSFETs past normal operating conditions. This is the only VDS_MODE change allowed in the operating state. The VDS_MODE setting is located in the SPI register 0xC, bits D2-D0.
- VDS Comparator Thresholds (VDS_LEVEL): The V_{DS} overcurrent monitor threshold (VDS_LEVEL) may be changed at any time during operation to allow for higher than standard operating currents. The VDS_LEVEL setting is located in the SPI register 0xC.
- VGS Fault Mode (DIS_GDRV_FAULT): The V_{GS} fault detection monitors can be disabled through the SPI register 0x9, bit D8. Reporting in SPI will also be disabled as a result.
- SNS_OCP Fault Mode (DIS_SNS_OCP): The sense amplifier overcurrent monitors can be disabled through the SPI register 0x9, bit D4. Reporting in SPI will also be disabled as a result.
- PVDD Undervoltage Lockout (DIS_VPVDD_UVLO2): The main power supply undervoltage lockout can be disabled through the SPI register 0x9, but D9. Reporting in SPI will also be disabled as a result.
- OTSD Overtemperature Shutdown (FLIP_OTS): The overtemperature shutdown can be disabled through the SPI register 0x9, bit D10. Reporting in SPI will also be disabled as a result. The OTS overtemperature shutdown is disabled by default on the Grade 0, DRV8305xE device.

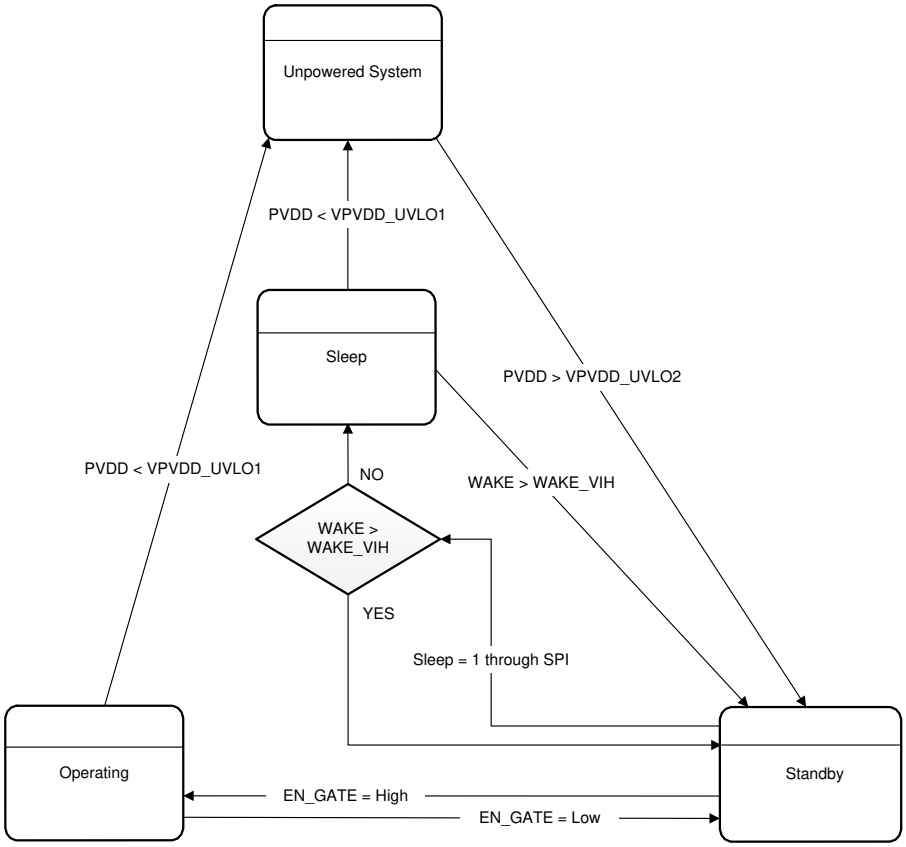


Figure 16. Operating States

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7.5 Programming

7.5.1 SPI Communication

7.5.1.1 SPI

The DRV8305-Q1 uses a SPI to set device configurations, operating parameters, and read out diagnostic information. The DRV8305-Q1 SPI operates in slave mode. The SPI input data (SDI) word consists of a 16-bit word with a 5-bit command and 11 bits of data. The SPI output data (SDO) word consists of 11 bits of register data with the first 5 bits (MSB) as don't cares.

A valid frame must meet following conditions:

- CPOL (clock polarity) = 0 and CPHA (clock phase) = 1.
- SCLK must be low when nSCS transitions.
- Full 16 SCLK cycles.
- Data is always propagated on the rising edge of SCLK.
- Data is always captured on the falling edge of SCLK.
- MSB is shifted in and out first.
- When nSCS is high, SCLK and SDI are ignored and SDO is high impedance.
- nSCS should be taken high for at least 500 ns between frames.
- If the data sent to SDI is less than or greater than 16 bits it is considered a frame error and the data will be ignored.

7.5.1.2 SPI Format

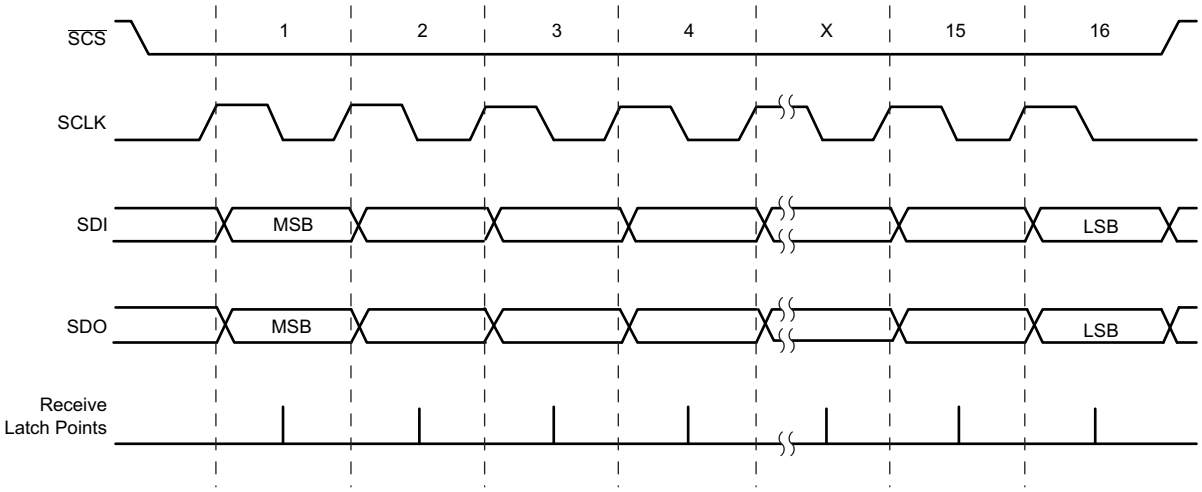


Figure 17. SPI Slave Mode Timing Diagram

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Programming (continued)

The SPI input data (SDI) control word is 16 bits long and consists of the following format:

- 1 read or write bit W [15]
- 4 address bits A [14:11]
- 11 data bits D [10:0]

The SPI output data (SDO) word response word is 11 bits long (first 5 bits are don't cares). It contains the content of the register being accessed.

The MSB of the SDI word (W0) is the read/write bit. When W0 = 0, the input data is a write command. When W0 = 1, the input data is a read command.

For a write command: The response word is the data currently in the register being written.

For a read command: The response word is the data currently in the register being read.

Table 7. SPI Input Data Control Word Format

	R/W	ADDRESS				DATA										
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	W0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 8. SPI Output Data Response Word Format

	DATA															
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	X	X	X	X	X	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

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7.6 Register Maps

Table 9. Register Map

ADDRESS	NAME	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x1	Warnings & Watchdog Reset	FAULT	*RSVD*	TEMP_FLAG4	PVDD_UVFL	PVDD_OVFL	VDS_STATUS	VCPH_UVFL	TEMP_FLAG1	TEMP_FLAG2	TEMP_FLAG3	OTW
0x2	OV/VDS Faults	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC	*RSVD*		SNS_C_OCP	SNS_B_OCP	SNS_A_OCP
0x3	IC Faults	PVDD_UVLO2	WD_FAULT	OTSD	RSVD	VREG_UV	AVDD_UVLO	VCP_LSD _UVLO2	*RSVD*	VCPH_UVLO2	VCPH_OVLO	VCPH_OVLO _ABS
0x4	VGS Faults	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC	*RSVD*				
0x5	HS Gate Drive Control	*RSVD*	TDRIVEN		IDRIVEN_HS				IDRIVEP_HS			
0x6	LS Gate Drive Control	*RSVD*	TDRIVEP		IDRIVEN_LS				IDRIVEP_LS			
0x7	Gate Drive Control	*RSVD*	COMM_OPTION	PWM_MODE		DEAD_TIME			TBLANK		TVDS	
0x8	Reserved	*RSVD*										
0x9	IC Operation	FLIP_OTSD	DIS_PVDD _UVLO2	DIS_GDRV _FAULT	EN_SNS _CLAMP	WD_DLY		DIS_SNS_OCP	WD_EN	SLEEP	CLR_FLTS	SET_VCPH_UV
0xA	Shunt Amplifier Control	DC_CAL_CH3	DC_CAL_CH2	DC_CAL_CH1	CS_BLANK		GAIN_CS3		GAIN_CS2		GAIN_CS1	
0xB	Voltage Regulator Control	*RSVD*	VREF_SCALE		*RSVD*			SLEEP_DLY		DIS_VREG _PWRGD	VREG_UV_LEVEL	
0xC	VDS Sense Control	*RSVD*			VDS_LEVEL					VDS_MODE		

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7.6.1 Status Registers

The status registers are used to report device warnings, fault conditions, and provide a means to prevent timing out of the watchdog timer. Status registers are read only registers.

7.6.1.1 Warning and Watchdog Reset (Address = 0x1)

Table 10. Warning and Watchdog Reset Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R	FAULT	0x0	Fault indication
9	R	RSVD	0x0	-
8	R	TEMP_FLAG4	0x0	Temperature flag setting for approximately 175°C
7	R	PVDD_UVFL	0x0	PVDD undervoltage flag warning
6	R	PVDD_OVFL	0x0	PVDD overvoltage flag warning
5	R	VDS_STATUS	0x0	Real time OR of all VDS overcurrent monitors
4	R	VCHP_UVFL	0x0	Charge pump undervoltage flag warning
3	R	TEMP_FLAG1	0x0	Temperature flag setting for approximately 105°C
2	R	TEMP_FLAG2	0x0	Temperature flag setting for approximately 125°C
1	R	TEMP_FLAG3	0x0	Temperature flag setting for approximately 135°C
0	R	OTW	0x0	Overtemperature warning

7.6.1.2 OV/VDS Faults (Address = 0x2)

Table 11. OV/VDS Faults Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R	VDS_HA	0x0	VDS overcurrent fault for high-side MOSFET A
9	R	VDS_LA	0x0	VDS overcurrent fault for low-side MOSFET A
8	R	VDS_HB	0x0	VDS overcurrent fault for high-side MOSFET B
7	R	VDS_LB	0x0	VDS overcurrent fault for low-side MOSFET B
6	R	VDS_HC	0x0	VDS overcurrent fault for high-side MOSFET C
5	R	VDS_LC	0x0	VDS overcurrent fault for low-side MOSFET C
4:3	R	RSVD	0x0	-
2	R	SNS_C_OCP	0x0	Sense C overcurrent fault
1	R	SNS_B_OCP	0x0	Sense B overcurrent fault
0	R	SNS_A_OCP	0x0	Sense A overcurrent fault

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7.6.1.3 IC Faults (Address = 0x3)

Table 12. IC Faults Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R	PVDD_UVLO2	0x0	PVDD undervoltage 2 fault
9	R	WD_FAULT	0x0	Watchdog fault
8	R	OTSD	0x0	Overtemperature fault
7	R	RSVD	0x0	-
6	R	VREG_UV	0x0	VREG undervoltage fault
5	R	AVDD_UVLO	0x0	AVDD undervoltage fault
4	R	VCP_LSD_UVLO2	0x0	Low-side gate supply fault
3	R	RSVD	0x0	-
2	R	VCPH_UVLO2	0x0	High-side charge pump undervoltage 2 fault
1	R	VCPH_OVLO	0x0	High-side charge pump overvoltage fault
0	R	VCPH_OVLO_ABS	0x0	High-side charge pump overvoltage ABS fault

7.6.1.4 VGS Faults (Address = 0x4)

Table 13. Gate Driver VGS Faults Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R	VGS_HA	0x0	VGS gate drive fault for high-side MOSFET A
9	R	VGS_LA	0x0	VGS gate drive fault for low-side MOSFET A
8	R	VGS_HB	0x0	VGS gate drive fault for high-side MOSFET B
7	R	VGS_LB	0x0	VGS gate drive fault for low-side MOSFET B
6	R	VGS_HC	0x0	VGS gate drive fault for high-side MOSFET C
5	R	VGS_LC	0x0	VGS gate drive fault for low-side MOSFET C
4:0	R	RSVD	0x0	-

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7.6.2 Control Registers

Control registers are used to set the device parameters for DRV8305-Q1. The default values are shown in bold.

- Control registers are read/write registers
- Do not clear on register read, CLR_FLTs, or EN_GATE resets
- Cleared to default values on power up
- Cleared to default values when the device enters SLEEP mode

7.6.2.1 HS Gate Drive Control (Address = 0x5)

Table 14. HS Gate Driver Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION			
10	R/W	RSVD	0x0	-			
9:8	R/W	TDRIVEN	0x3	High-side gate driver peak source time b'00 - 220 ns b'01 - 440 ns b'10 - 880 ns **b'11 - 1780 ns**			
7:4	R/W	IDRIVEN_HS	0x4	High-side gate driver peak sink current			
				b'0000 - 20 mA **b'0100 - 60 mA** b'1000 - 0.50 A b'1100 - 60 mA	b'0001 - 30 mA b'0101 - 70 mA b'1001 - 0.75 A b'1101 - 60 mA	b'0010 - 40 mA b'0110 - 80 mA b'1010 - 1.00 A b'1110 - 60 mA	b'0011 - 50 mA b'0111 - 0.25 A b'1011 - 1.25 A b'1111 - 60 mA
3:0	R/W	IDRIVEP_HS	0x4	High-side gate driver peak source current			
				b'0000 - 10 mA **b'0100 - 50 mA** b'1000 - 0.25 A b'1100 - 50 mA	b'0001 - 20 mA b'0101 - 60 mA b'1001 - 0.50 A b'1101 - 50 mA	b'0010 - 30 mA b'0110 - 70 mA b'1010 - 0.75 A b'1110 - 50 mA	b'0011 - 40 mA b'0111 - 0.125 A b'1011 - 1.00 A b'1111 - 50 mA

7.6.2.2 LS Gate Drive Control (Address = 0x6)

Table 15. LS Gate Driver Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION			
10	R/W	RSVD	0x0	-			
9:8	R/W	TDRIVEP	0x3	Low-side gate driver peak source time b'00 - 220 ns b'01 - 440 ns b'10 - 880 ns **b'11 - 1780 ns**			
7:4	R/W	IDRIVEN_LS	0x4	Low-side gate driver peak sink current			
				b'0000 - 20 mA **b'0100 - 60 mA** b'1000 - 0.50 A b'1100 - 60 mA	b'0001 - 30 mA b'0101 - 70 mA b'1001 - 0.75 A b'1101 - 60 mA	b'0010 - 40 mA b'0110 - 80 mA b'1010 - 1.00 A b'1110 - 60 mA	b'0011 - 50 mA b'0111 - 0.25 A b'1011 - 1.25 A b'1111 - 60 mA
3:0	R/W	IDRIVEP_LS	0x4	Low-side gate driver peak source current			
				b'0000 - 10 mA **b'0100 - 50 mA** b'1000 - 0.25 A b'1100 - 50 mA	b'0001 - 20 mA b'0101 - 60 mA b'1001 - 0.50 A b'1101 - 50 mA	b'0010 - 30 mA b'0110 - 70 mA b'1010 - 0.75 A b'1110 - 50 mA	b'0011 - 40 mA b'0111 - 0.125 A b'1011 - 1.00 A b'1111 - 50 mA

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7.6.2.3 Gate Drive Control (Address = 0x7)

Table 16. Gate Drive Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R/W	VCPH_FREQ	0x0	Reduce charge pump frequency center and spread **b'0 - Center = 518 kHz, Spread = 438 kHz - 633 kHz** b'1 - Center = 452 kHz, Spread = 419 kHz - 491 kHz
9	R/W	COMM_OPTION	0x1	Rectification control (PWM_MODE = b'10 only) b'0 - diode freewheeling **b'1 - active freewheeling**
8:7	R/W	PWM_MODE	0x0	PWM Mode **b'00 - PWM with 6 independent inputs** b'01 - PWM with 3 independent inputs b'10 - PWM with one input b'11 - PWM with 6 independent inputs
6:4	R/W	DEAD_TIME	0x1	Dead time b'000 - 35 ns b'011 - 440 ns b'110 - 3520 ns **b'001 - 52 ns** b'100 - 880 ns b'111 - 5280 ns b'010 - 88 ns b'101 - 1760 ns
3:2	R/W	TBLANK	0x1	VDS sense blanking b'00 - 0 µs **b'01 - 1.75 µs** b'10 - 3.5 µs b'11 - 7 µs
1:0	R/W	TVDS	0x2	VDS sense deglitch b'00 - 0 µs b'01 - 1.75 µs **b'10 - 3.5 µs** b'11 - 7 µs

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7.6.2.4 IC Operation (Address = 0x9)

Table 17. IC Operation Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION	
10	R/W	FLIP_OTSD	0x0	OTSD control setting	
				DRV8305xQ **b'0 - Enable OTSD** b'1 - Disable OTSD	DRV8305xE **b'0 - Disable OTSD**(1) b'1 - Enable OTSD
9	R/W	DIS_PVDD_UVLO2	0x0	Disable PVDD_UVLO2 fault and reporting **b'0 - PVDD_UVLO2 enabled** b'1 - PVDD_UVLO2 disabled	
8	R/W	DIS_GDRV_FAULT	0x0	Disable gate drive fault and reporting **b'0 - Gate driver fault enabled** b'1 - Gate driver fault disabled	
7	R/W	EN_SNS_CLAMP	0x0	Enable sense amplifier clamp **b'0 - Sense amplifier clamp is not enabled** b'1 - Sense amplifier clamp is enabled, limiting output to ~3.3 V	
6:5	R/W	WD_DLY	0x1	Watchdog delay b'00 - 10 ms **b'01 - 20 ms** b'10 - 50 ms b'11 - 100 ms	
4	R/W	DIS_SNS_OCP	0x0	Disable SNS overcurrent protection fault and reporting **b'0 - SNS OCP enabled** b'1 - SNS OCP disabled	
3	R/W	WD_EN	0x0	Watchdog enable **b'0 - Watch dog disabled** b'1 - Watch dog enabled	
2	R/W	SLEEP	0x0	Put device into sleep mode **b'0 - Device awake** b'1 - Device asleep	
1	R/W	CLR_FLTS	0x0	Clear faults **b'0 - Normal operation** b'1 - Clear faults	
0	R/W	SET_VCPH_UV	0x0	Set charge pump undervoltage threshold level **b'0 -** 4.9 V b'1 - 4.6 V	

(1) Overtemperature shutdown (OTSD) is disabled by default for DRV8305xEPHPQ1 and may only be re-enabled through this control bit.

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7.6.2.5 Shunt Amplifier Control (Address = 0xA)

Table 18. Shunt Amplifier Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R/W	DC_CAL_CH3	0x0	DC calibration of CS amplifier 3 **b'0 - Normal operation** b'1 - DC calibration mode
9	R/W	DC_CAL_CH2	0x0	DC calibration of CS amplifier 2 **b'0 - Normal operation** b'1 - DC calibration mode
8	R/W	DC_CAL_CH1	0x0	DC calibration of CS amplifier 1 **b'0 - Normal operation** b'1 - DC calibration mode
7:6	R/W	CS_BLANK	0x0	Current shunt amplifier blanking time **b'00 - 0 ns** b'01 - 500 ns b'10 - 2.5 µs b'11 - 10 µs
5:4	R/W	GAIN_CS3	0x0	Gain of CS amplifier 3 **b'00 - 10 V/V** b'01 - 20 V/V b'10 - 40 V/V b'11 - 80 V/V
3:2	R/W	GAIN_CS2	0x0	Gain of CS amplifier 2 **b'00 - 10 V/V** b'01 - 20 V/V b'10 - 40 V/V b'11 - 80 V/V
1:0	R/W	GAIN_CS1	0x0	Gain of CS amplifier 1 **b'00 - 10 V/V** b'01 - 20 V/V b'10 - 40 V/V b'11 - 80 V/V

7.6.2.6 Voltage Regulator Control (Address = 0xB)

Table 19. Voltage Regulator Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R/W	RSVD	0x0	-
9:8	R/W	VREF_SCALE	0x1	VREF Scaling b'00 - RSVD **b'01 - k = 2** b'10 - k = 4 b'11 - k = 8
7:5	R/W	RSVD	0x0	-
4:3	R/W	SLEEP_DLY	0x1	Delay to power down VREG after SLEEP b'00 - 0 µs **b'01 - 10 µs** b'10 - 50 µs b'11 - 1 ms
2	R/W	DIS_VREG_PWRGD	0x0	Disable VREG undervoltage fault and reporting **b'0 - VREG_UV enabled** b'1 - VREG_UV disabled
0:1	R/W	VREG_UV_LEVEL	0x2	VREG undervoltage set point b'00 - VREG x 0.9 b'01 - VREG x 0.8 **b'10 - VREG x 0.7** b'11 - VREG x 0.7

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7.6.2.7 VDS Sense Control (Address = 0xC)

Table 20. VDS Sense Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION			
10:8	R	RSVD	0x0	These bits are reserved for internal use for revision ID.			
7:3	R/W	VDS_LEVEL	0x19	VDS comparator threshold			
				b'00000 - 0.060 V b'00100 - 0.097 V b'01000 - 0.155 V b'01100 - 0.250 V b'10000 - 0.403 V b'10100 - 0.648 V b'11000 - 1.043 V b'11100 - 1.679 V	b'00001 - 0.068 V b'00101 - 0.109 V b'01001 - 0.175 V b'01101 - 0.282 V b'10001 - 0.454 V b'10101 - 0.730 V **b'11001 - 1.175 V** b'11101 - 1.892 V	b'00010 - 0.076 V b'00110 - 0.123 V b'01010 - 0.197V b'01110 - 0.317 V b'10010 - 0.511 V b'10110 - 0.822 V b'11010 - 1.324 V b'11110 - 2.131 V	b'00011 - 0.086 V b'00111 - 0.138 V b'01011 - 0.222 V b'01111 - 0.358 V b'10011 - 0.576 V b'10111 - 0.926 V b'11011 - 1.491 V b'11111 - 2.131 V
2:0	R/W	VDS_MODE	0x0	VDS mode **b'000 - Latched shut down when overcurrent detected** b'001 - Report only when overcurrent detected b'010 - VDS protection disabled (no overcurrent sensing or reporting)			

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

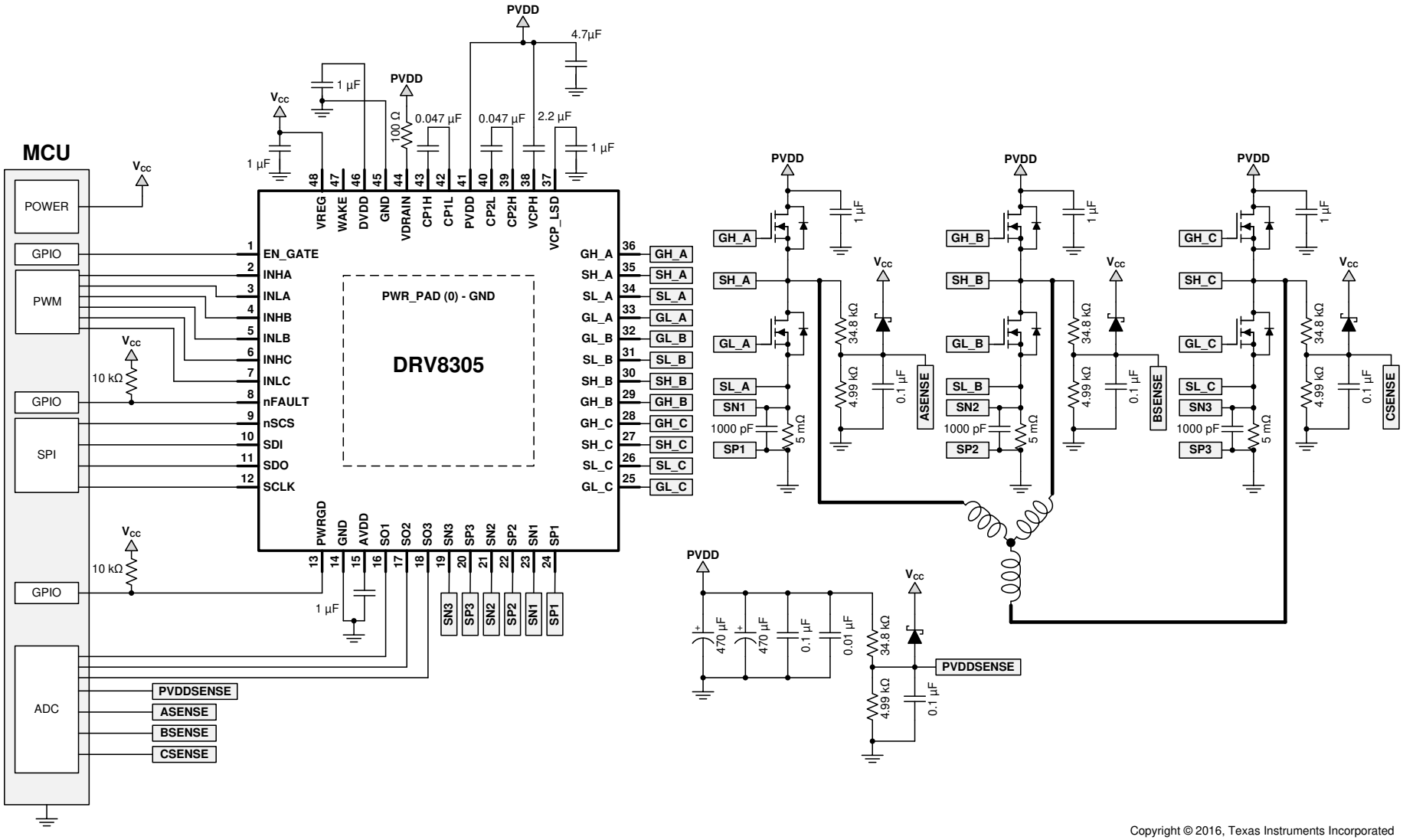
8.1 Application Information

The DRV8305-Q1 is a gate driver IC designed to drive a 3-phase BLDC motor in combination with external power MOSFETs. The device provides a high level of integration with three half-bridge gate drivers, three current shunt amplifiers, adjustable slew rate control, logic LDO, and a suite of protection features.

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8.2 Typical Application

The following design is a common application of the DRV8305-Q1.



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Figure 18. Typical Application Schematic

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8.2.1 Design Requirements

Table 21. Design Parameters

DESIGN PARAMETER	REFERENCE	VALUE
Supply voltage	PVDD	12 V
Motor winding resistance	M_R	0.5 Ω
Motor winding inductance	M_L	0.28 mH
Motor poles	M_P	16 poles
Motor rated RPM	M_{RPM}	2000 RPM
Number of MOSFETs switching	N_{SW}	6
Switching frequency	f_{SW}	45 kHz
IDRIVEP	I_{DRIVEP}	50 mA
IDRIVEN	I_{DRIVEN}	60 mA
MOSFET Q_G	Q_g	36 nC
MOSFET Q_{GD}	Q_{GD}	9 nC
MOSFET $R_{DS(on)}$	$R_{DS(on)}$	4.1 mΩ
Target full-scale current	I_{MAX}	30 A
Sense resistor	R_{SENSE}	0.005 Ω
V_{DS} trip level	V_{DS_LVL}	0.197 V
Amplifier bias	V_{BIAS}	1.65 V
Amplifier gain	Gain	10 V/V

8.2.2 Detailed Design Procedure

8.2.2.1 Gate Drive Average Current

The gate drive supply (VCP) of the DRV8305-Q1 is capable of delivering up to 30 mA (RMS) of current to the external power MOSFETs. The charge pump directly supplies the high-side N-channel MOSFETs and a 10-V LDO powered from VCP supplies the low-side N-channel MOSFETs. The designer can determine the approximate RMS load on the gate drive supply through the following equation.

$$\text{Gate Drive RMS Current} = \text{MOSFET } Q_g \times \text{Number of Switching MOSFETs} \times \text{Switching Frequency} \quad (2)$$

Example: 36 nC (Q_G) × 6 (N_{SW}) × 45 kHz (f_{SW}) = 9.72 mA

Note that this is only a first-order approximation.

8.2.2.2 MOSFET Slew Rates

The rise and fall times of the external power MOSFET can be adjusted through the use of the DRV8305-Q1 IDRIVE setting. A higher IDRIVE setting will charge the MOSFET gate more rapidly where a lower IDRIVE setting will charge the MOSFET gate more slowly. System testing requires fine tuning to the desired slew rate, but a rough first-order approximation can be calculated as shown in the following.

$$\text{MOSFET Slew Rate} = \text{MOSFET } Q_{GD} / \text{IDRIVE Setting} \quad (3)$$

Example: 9 nC (Q_{GD}) / 50 mA (IDRIVEP) = 180 ns

8.2.2.3 Overcurrent Protection

The DRV8305-Q1 provides overcurrent protection for the external power MOSFETs through the use of VDS monitors for both the high-side and low-side MOSFETs. These are intended for protecting the MOSFET in overcurrent conditions and are not for precise current regulation.

The overcurrent protection works by monitoring the VDS voltage drop of the external MOSFETs and comparing it against the internal VDS_LEVEL set through the SPI registers. The high-side VDS is measured across the VDRAIN and SH_X pins. The low-side VDS is measured across the SH_X and SL_X pins. If the VDS voltage exceeds the VDS_LEVEL value, the DRV8305-Q1 will take action according to the VDS_MODE register.

The overcurrent trip level can be determined with the MOSFET $R_{DS(on)}$ and the VDS_LEVEL setting.

$$\text{Overcurrent Trip} = \text{VDS Level (VDS_LVL)} / \text{MOSFET } R_{DS(on)} \ (R_{DS(on)}) \quad (4)$$

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Example: 0.197 V (VDS_LVL) / 4.1 mΩ ($R_{DS(ON)}$) = 48 A

8.2.2.4 Current Sense Amplifiers

The DRV8305-Q1 provides three bidirectional low-side current shunt amplifiers. These can be used to sense the current flowing through each half-bridge. If individual half-bridge sensing is not required, a single current shunt amplifier can be used to measure the sum of the half-bridge current. Use this simple procedure to correctly configure the current shunt amplifiers.

1. Determine the peak current that the motor will demand (IMAX). This demand depends on the motor parameters and the application requirements. IMAX in this example is 14 A.
2. Determine the available voltage output range for the current shunt amplifiers. This will be the ± voltage around the amplifier bias voltage (VBIAS). In this case VBIAS = 1.65 V and a valid output voltage is 0 to 3.3 V. This gives an output range of ±1.65 V.
3. Determine the sense resistor value and amplifier gain settings. The sense resistor value and amplifier gain have common tradeoffs. The larger the sense resistor value, the better the resolution of the half-bridge current. This comes at the cost of additional power dissipated from the sense resistor. A larger gain value allows for the use of a smaller resolution, but at the cost of increased noise in the output signal and a longer settling time. This example uses a 5-mΩ sense resistor and the minimum gain setting of the DRV8305-Q1 (10 V/V). These values allow the current shunt amplifiers to measure ±33 A across the sense resistor.

8.2.3 VREG Reference Voltage Input (DRV8305N)

For the DRV8305N, the VREG pin is used for a reference voltage of current sense amplifier and SDO pullup as described in *VREG: Voltage Regulator Output*. The internal LDO is disabled, but the LDO physically exists in the device, and there is a current path from the VREG pin to the PVDD pin through the internal LDO. The reference current specified in the data sheet flows to the device if PVDD voltage (V_{PVDD}) is higher than VREG pin voltage (V_{VREG}). In case V_{VREG} is higher than V_{PVDD} during power up/down sequence, TI recommends to limit the current by adding a resistor to VREG pin so that the current does not exceed 50 mA. As shown in Figure 19, a 330-Ω resistor helps limit the current to approximately 15 mA when V_{VREG} = 5 V and V_{PVDD} = 0 V. For V_{VREG} = 3.3 V, TI recommends to use 220 Ω.

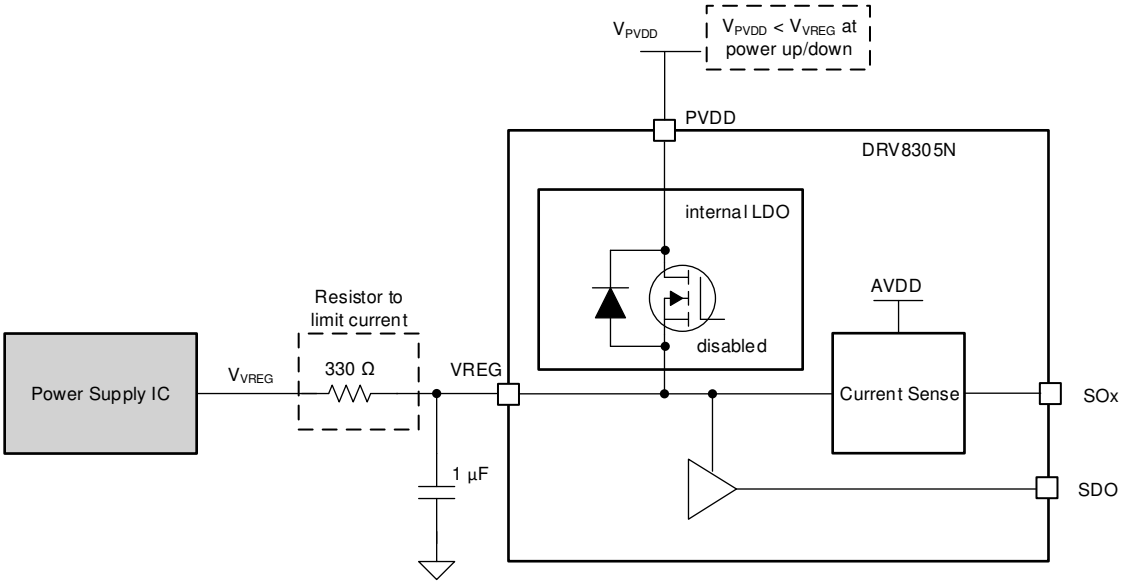


Figure 19. VREG Reference Voltage Input

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8.2.4 Application Curves

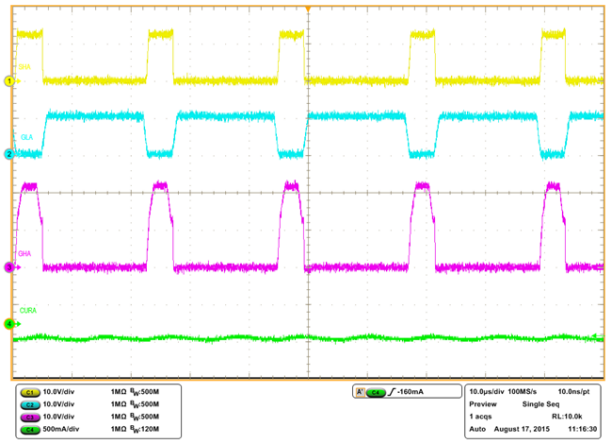


Figure 20. Gate Drive 20% Duty Cycle

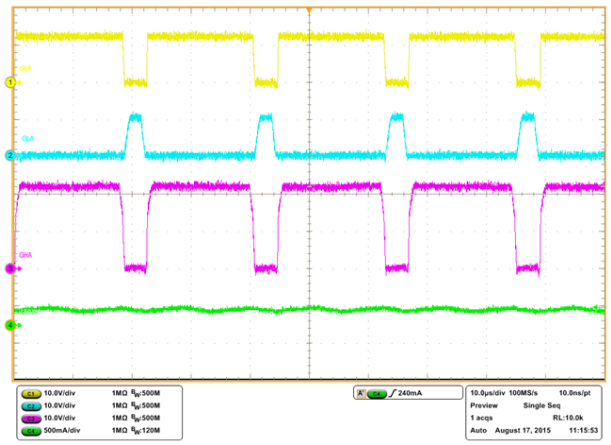


Figure 21. Gate Drive 80% Duty Cycle

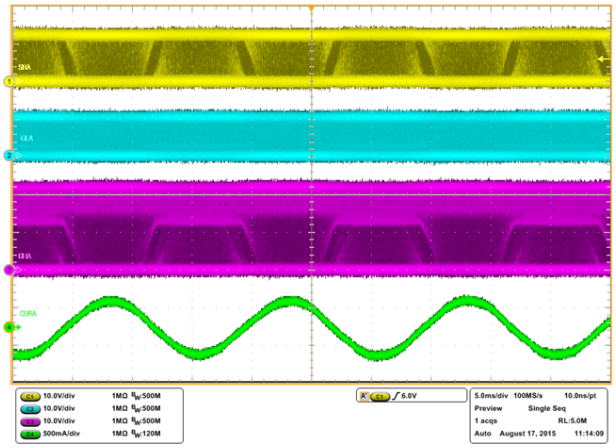


Figure 22. Motor Spinning 1000 RPM

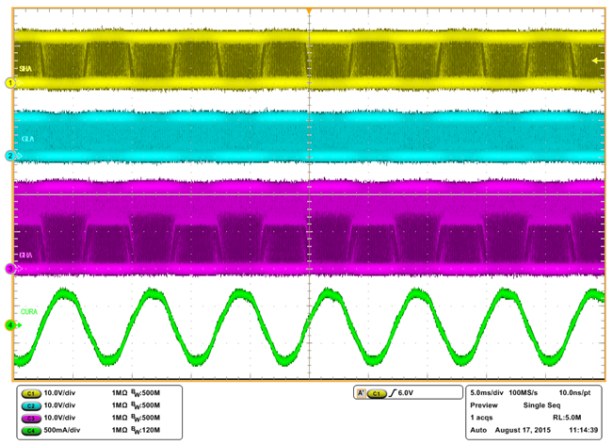


Figure 23. Motor Spinning 2000 RPM

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9 Power Supply Recommendations

9.1 Power Supply Consideration in Generator Mode

When the motor shaft of BLDC or PMSM motor is turned by an external force, the motor windings will generate a voltage on the motor inputs. This condition is known as generator mode or motor back-drive. In the generator mode, a positive voltage can be observed on SHx pins of the device. If there is a switch between VDRAIN and PVDD (SW_{VDRAIN} in Figure 24), and the following conditions exist in the system, the absolute maximum voltage of VCPH with respect to PVDD must be reviewed:

- Generator mode
- SW_{VDRAIN} is off
- PVDD and VCPH are low voltage (for example, PVDD = 0 V)

If SHx voltage (V_{SHx}) exceeds the VCPH voltage, the VCPH voltage starts following V_{SHx} because of the device internal diodes D1 and D2 (or D3). If the VCPH-PVDD voltage exceeds the absolute maximum voltage of DRV8305-Q1, the ESD diode D4 starts conducting, and results in a big current from SHx to PVDD through the diodes D2, D1, and D4. To avoid this condition, TI recommends to add an external diode D_{VDRAIN_PVDD} between VDRAIN and PVDD.

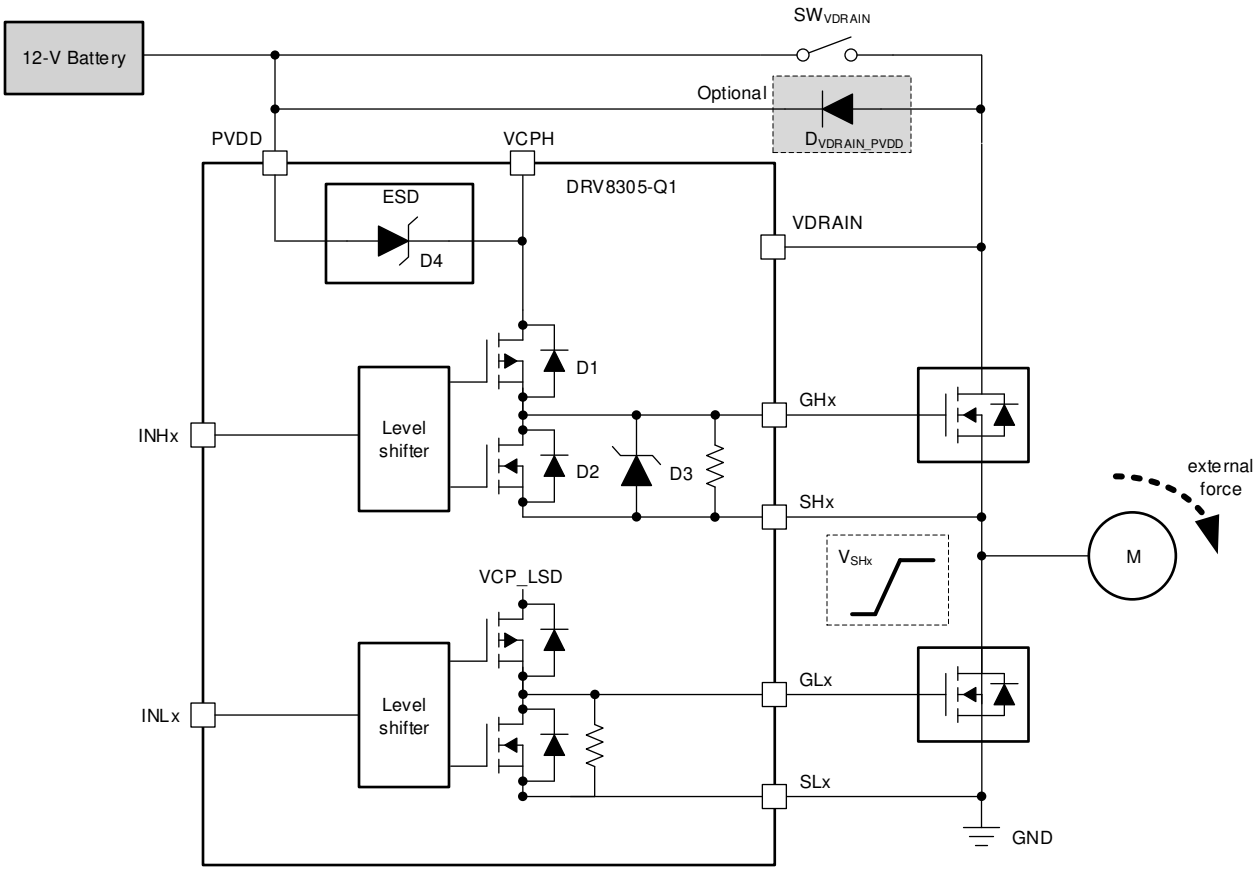


Figure 24. Power Supply Consideration in Generator Mode

9.2 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including the:

- Highest current required by the motor system
- Power supply's capacitance and ability to source or sink current

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Bulk Capacitance (continued)

- Amount of parasitic inductance between the power supply and motor system
- Acceptable voltage ripple
- Type of motor used (brushed DC, brushless DC, stepper)
- Motor braking method

The inductance between the power supply and motor drive system will limit the rate that current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate-sized bulk capacitor.

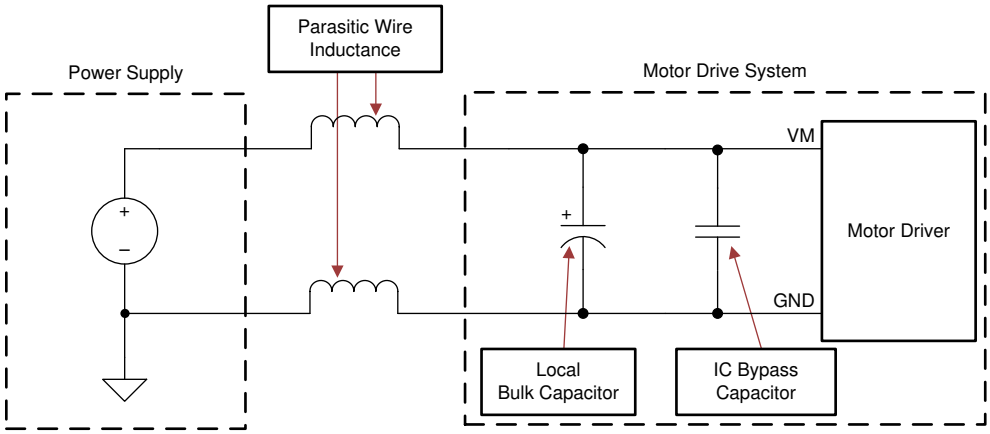


Figure 25. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

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10 Layout

10.1 Layout Guidelines

Use the following layout recommendations when designing a PCB for the DRV8305-Q1.

- The DVDD and AVDD 1-µF bypass capacitors should connect directly to the adjacent GND pin to minimize loop impedance for the bypass capacitor.
- The CP1 and CP2 0.047-µF flying capacitors should be placed directly next to the DRV8305-Q1 charge pump pins.
- The VCPH 2.2-µF and VCP_LSD 1-µF bypass capacitors should be placed close to their corresponding pins with a direct path back to the DRV8305-Q1 PVDD for VCPH and GND for VCP_LSD.
- The PVDD 4.7-µF bypass capacitor should be placed as close as possible to the DRV8305-Q1 PVDD supply pin.
- Use the proper footprint as shown in the mechanical drawing.
- Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the DRV8305-Q1 GH_X to the power MOSFET and returns through SH_X. The low-side loop is from the DRV8305-Q1 GL_X to the power MOSFET and returns through SL_X.
- The VDRAIN pin is used to sense the DRAIN voltage of the high-side MOSFETs for the V_{DS} overcurrent monitors. It should route through the 100-Ω series resistor directly to the MOSFET DRAIN, ideally at the midpoint of the half-bridge connections in order to get the most accurate sense point.

10.2 Layout Example

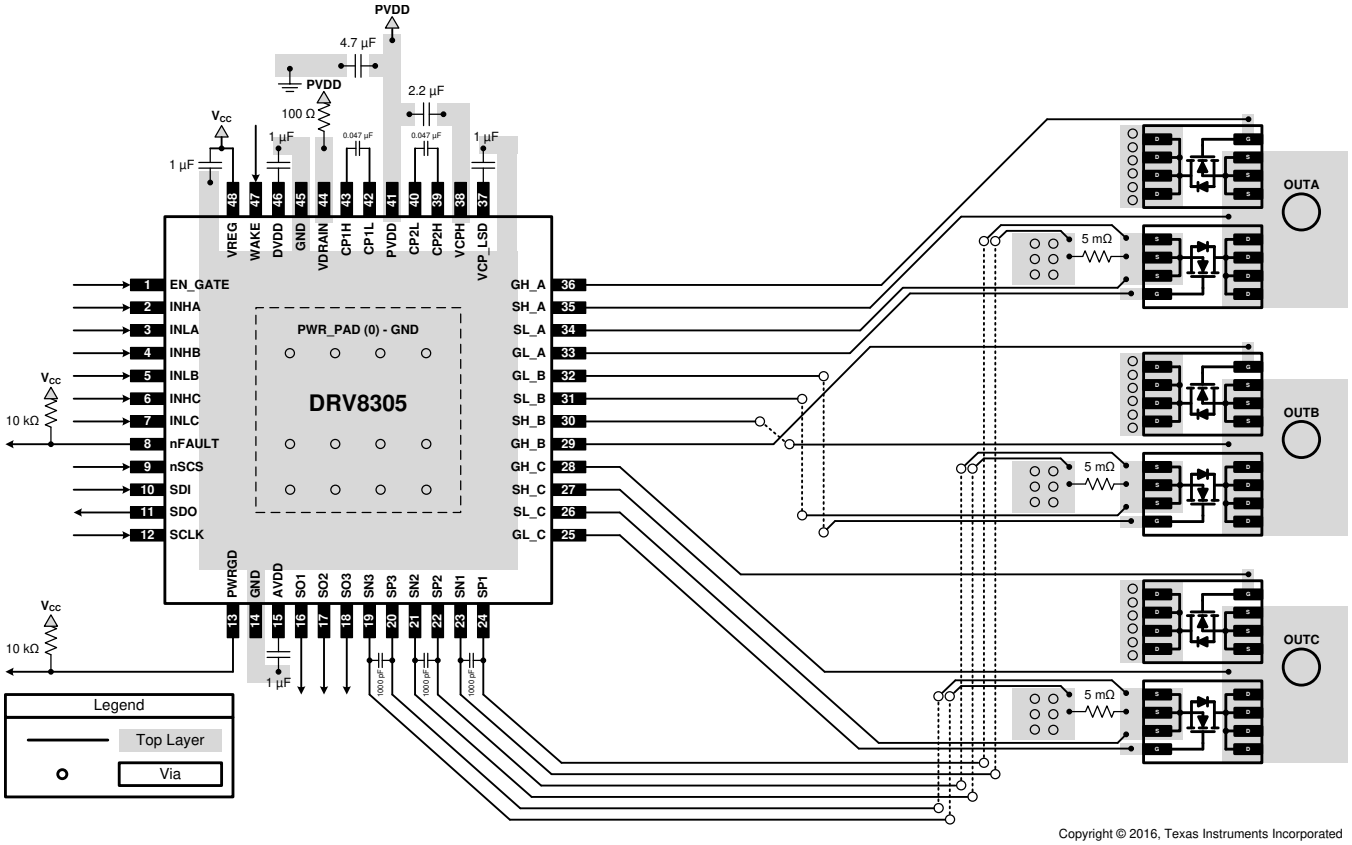


Figure 26. Layout Recommendation

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11 器件和文档支持

11.1 文档支持

请参见以下文档了解详细信息。

- 德州仪器 (TI)，*《汽车 12V 200W (20A) BLDC 电机驱动器参考设计》*
- 德州仪器 (TI)，*《汽车两轴电动座椅驱动器参考设计》*
- 德州仪器 (TI)，*《PowerPAD™ 热增强型封装》*应用报告
- 德州仪器 (TI)，*《PowerPAD™ 速成》*应用报告
- 德州仪器 (TI)，*《使用 MSP430 的传感器式三相 BLDC 电机控制》*应用报告
- 德州仪器 (TI)，*《了解 TI 电机栅极驱动器中的 IDRIVE 和 TDRIVE》*应用报告

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV83053QPHPQ1	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83053Q
DRV83053QPHPQ1.A	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83053Q
DRV83053QPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83053Q
DRV83053QPHPRQ1.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83053Q
DRV83055QPHPQ1	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83055Q
DRV83055QPHPQ1.A	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83055Q
DRV83055QPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83055Q
DRV83055QPHPRQ1.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83055Q
DRV8305NEPHPQ1	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV8305NE
DRV8305NEPHPQ1.A	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV8305NE
DRV8305NEPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV8305NE
DRV8305NEPHPRQ1.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV8305NE
DRV8305NQPHPQ1	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8305NQ
DRV8305NQPHPQ1.A	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8305NQ
DRV8305NQPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8305NQ
DRV8305NQPHPRQ1.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8305NQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF DRV8305-Q1 :

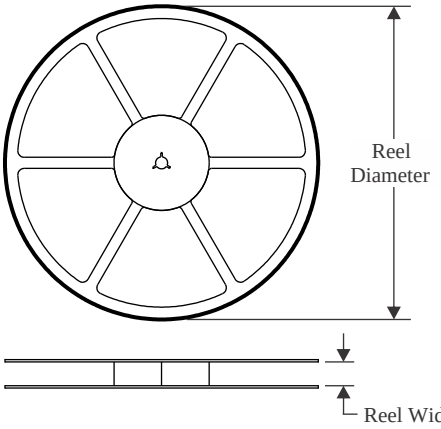
- Catalog : DRV8305

NOTE: Qualified Version Definitions:

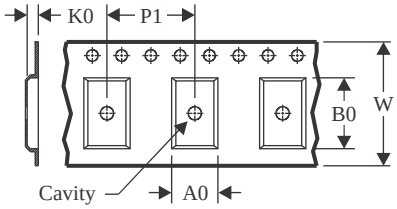
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

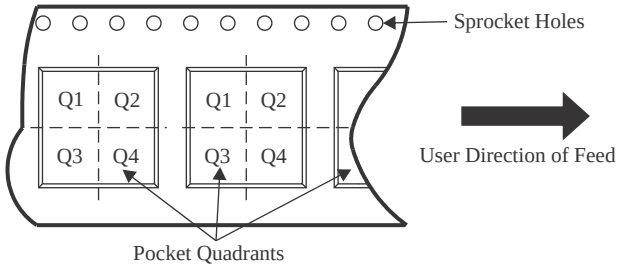


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

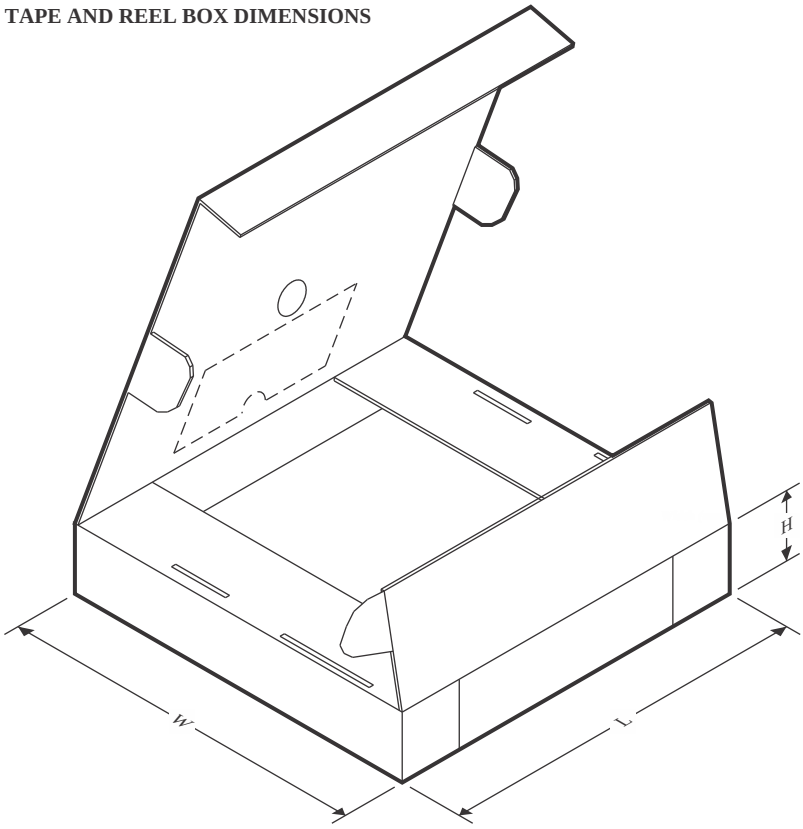
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV83053QPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DRV83055QPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DRV8305NEPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DRV8305NQPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DRV8305NQPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

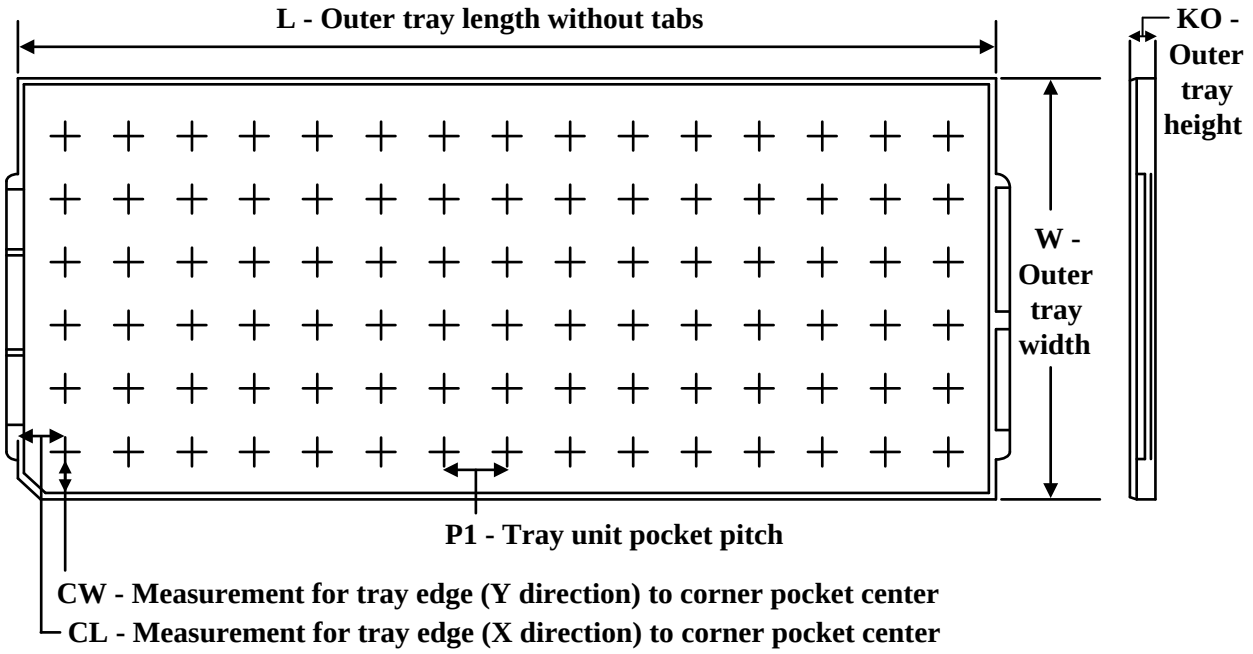
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV83053QPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0
DRV83055QPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0
DRV8305NEPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0
DRV8305NQPHPRQ1	HTQFP	PHP	48	1000	336.6	336.6	31.8
DRV8305NQPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DRV83053QPHPQ1	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DRV83053QPHPQ1.A	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DRV83055QPHPQ1	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DRV83055QPHPQ1.A	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DRV8305NEPHPQ1	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DRV8305NEPHPQ1.A	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DRV8305NQPHPQ1	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DRV8305NQPHPQ1.A	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

GENERIC PACKAGE VIEW

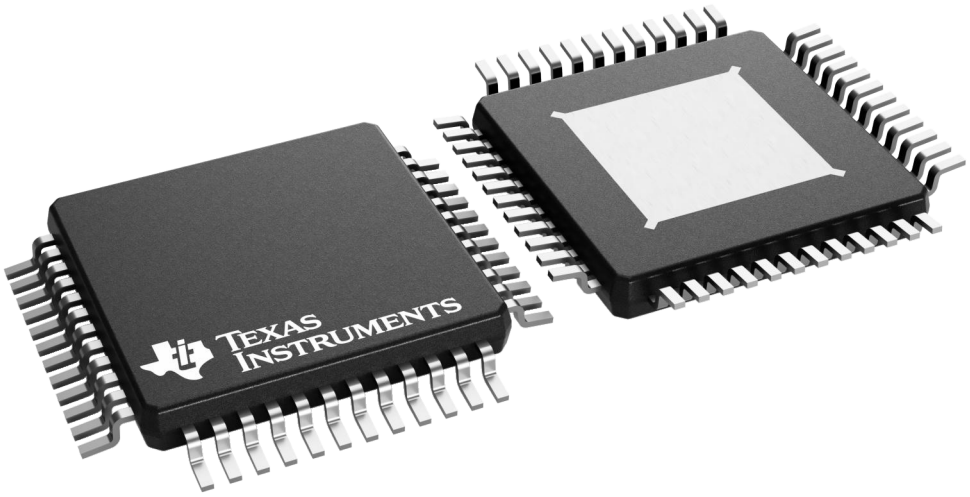
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



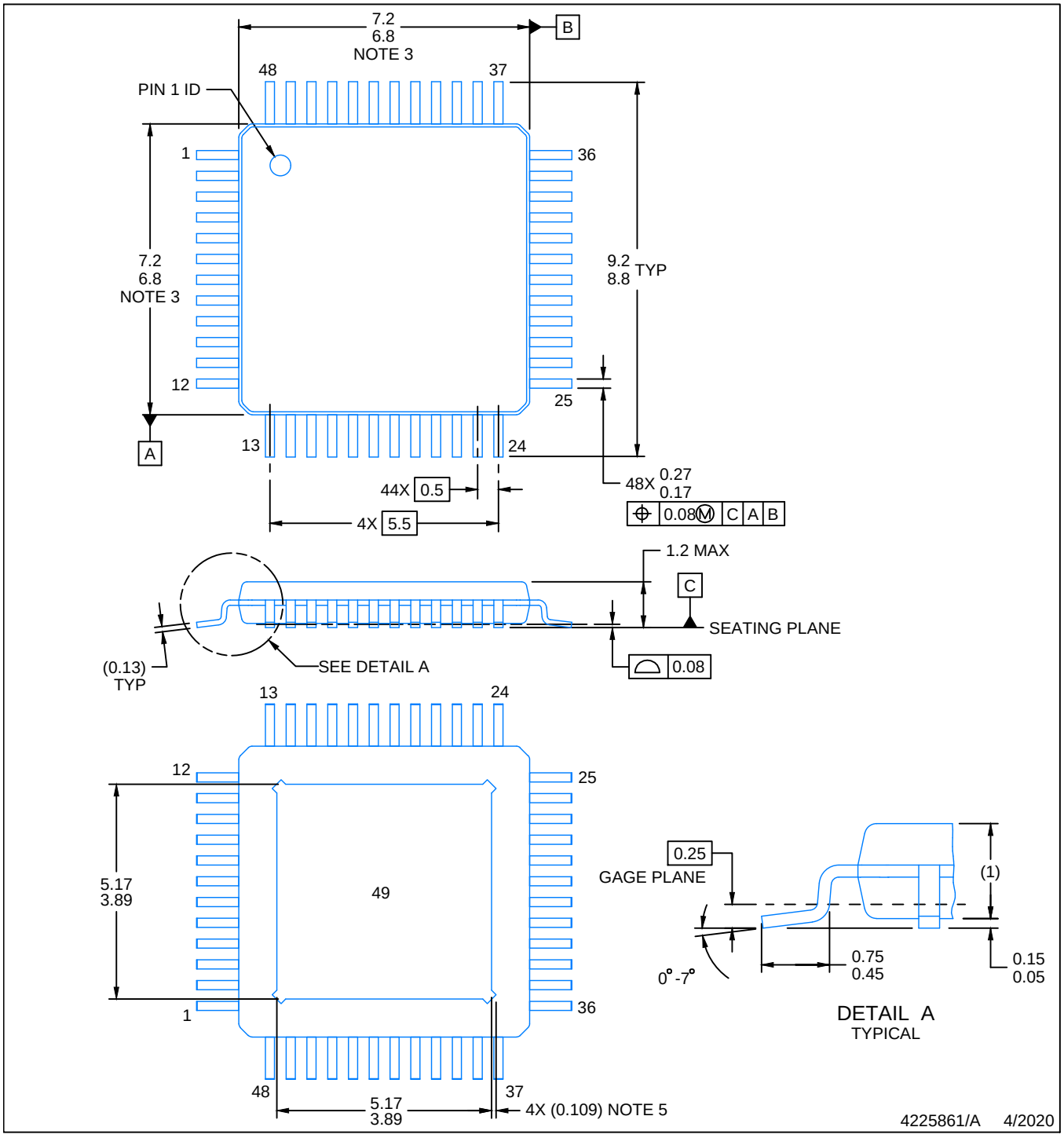
4226443/A

PACKAGE OUTLINE

PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

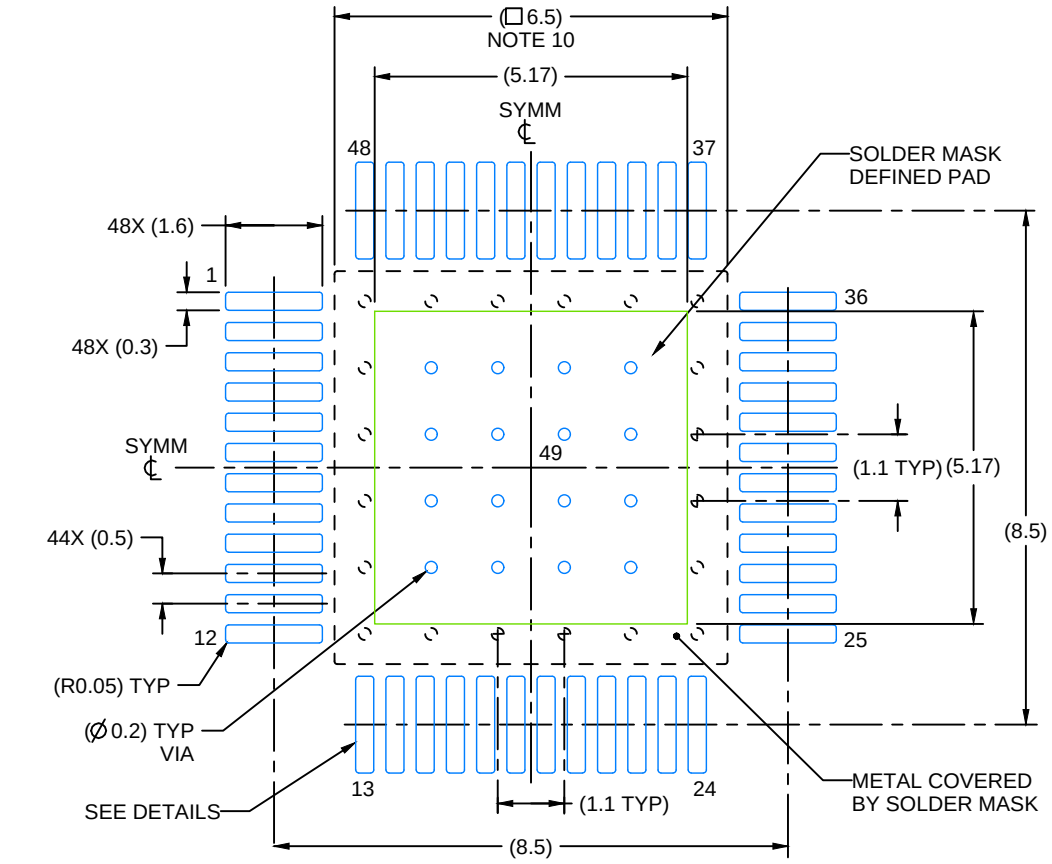
PLASTIC QUAD FLATPACK



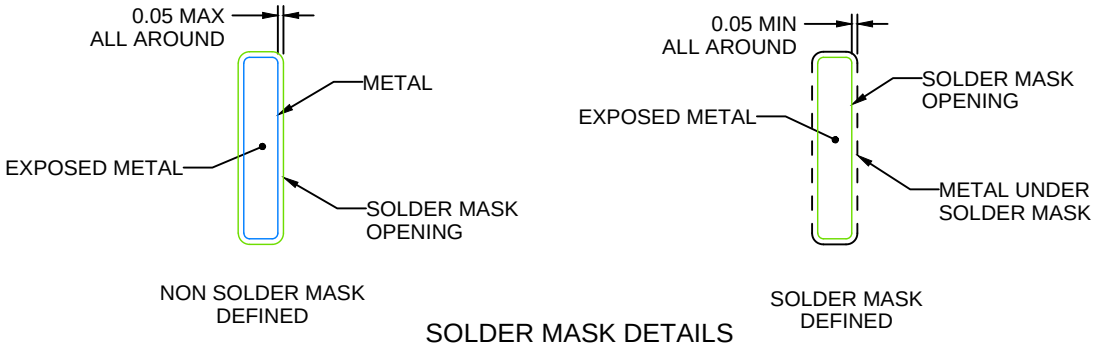
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

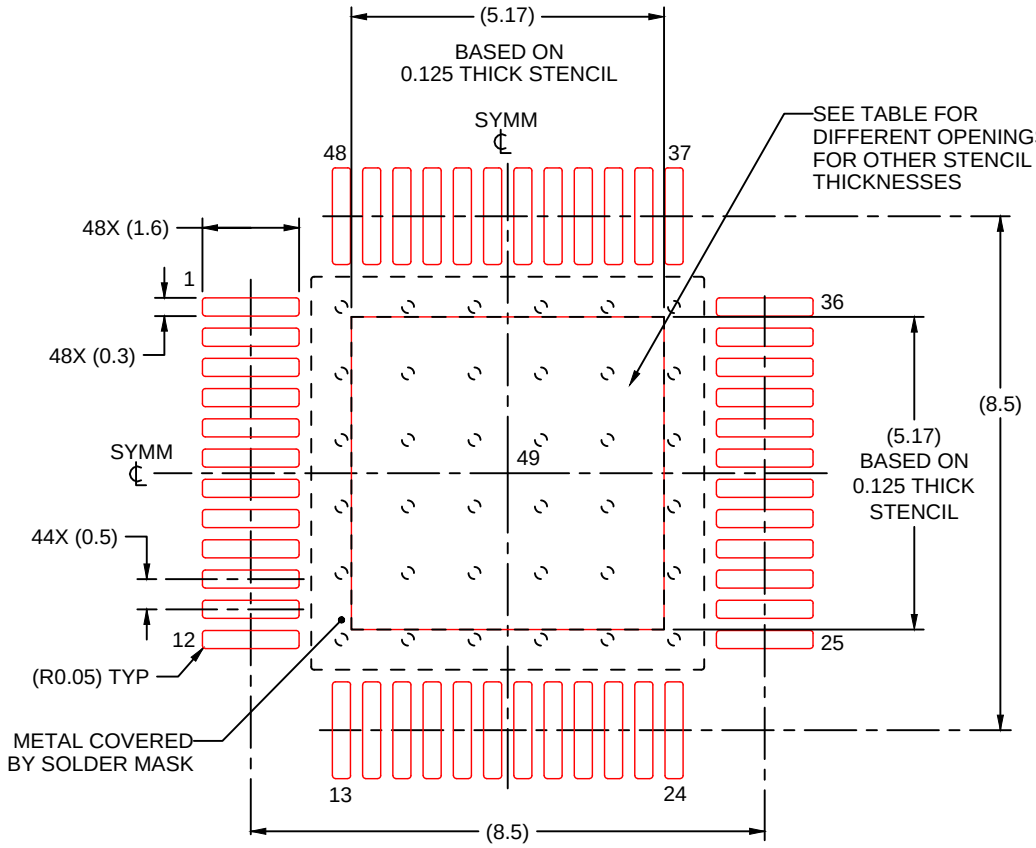


SOLDER MASK DETAILS

4225861/A 4/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

4225861/A 4/2020

NOTES: (continued)

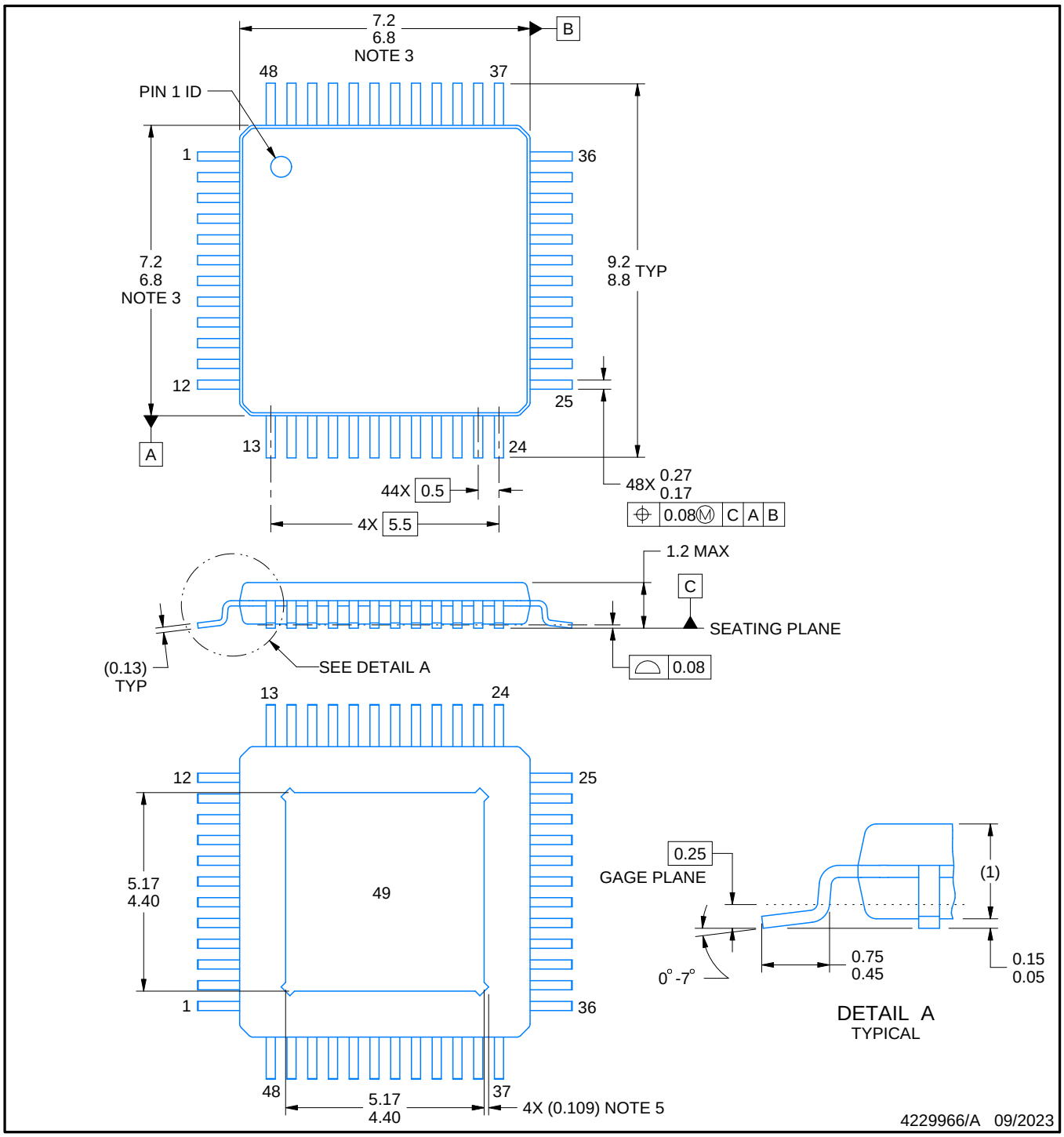
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PHP0048N

PowerPAD™ HTQFP - 1.2 mm max height

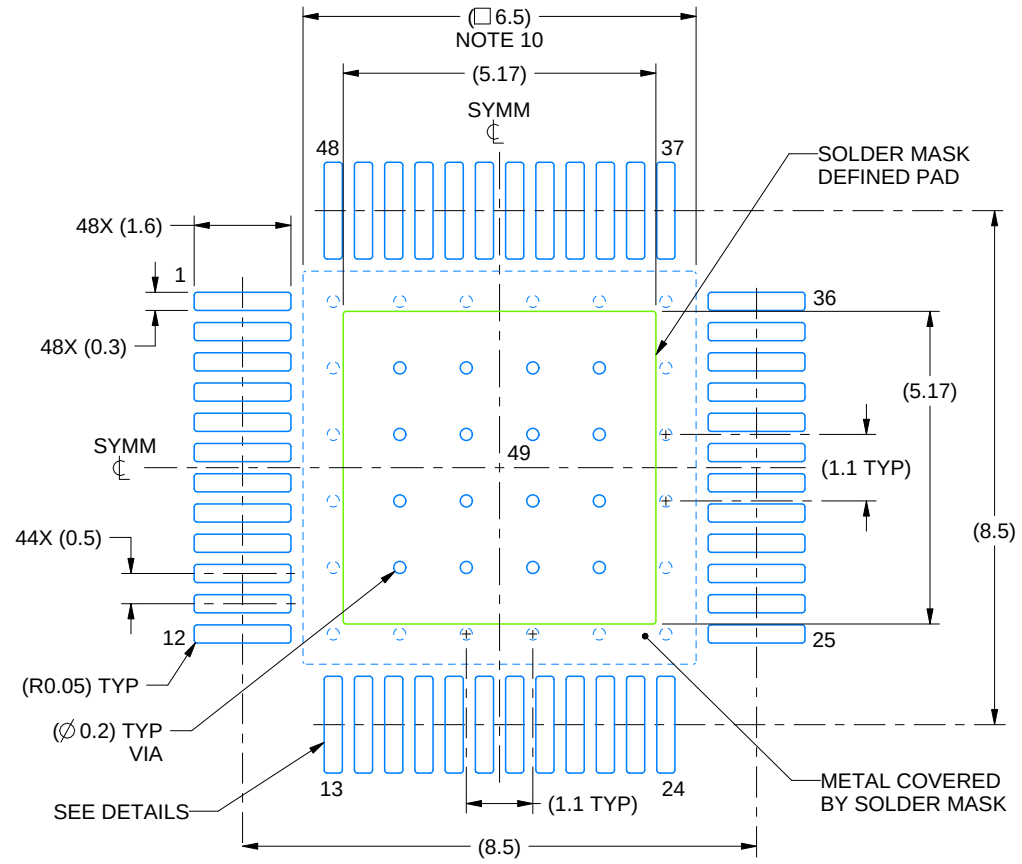
PLASTIC QUAD FLATPACK



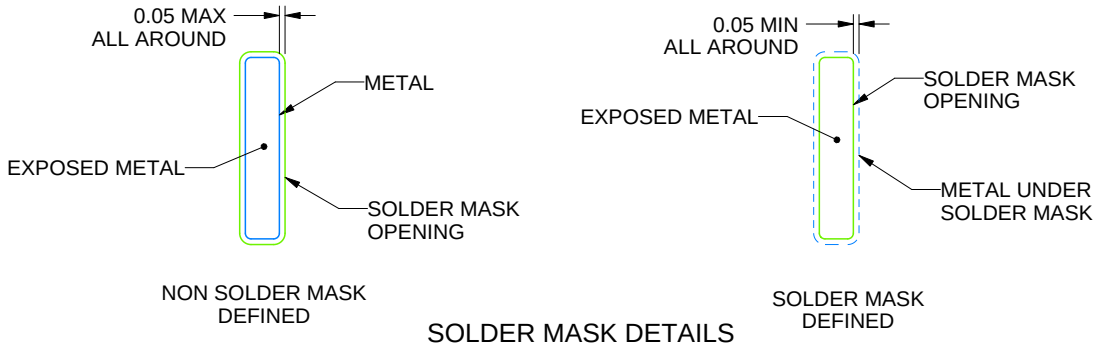
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

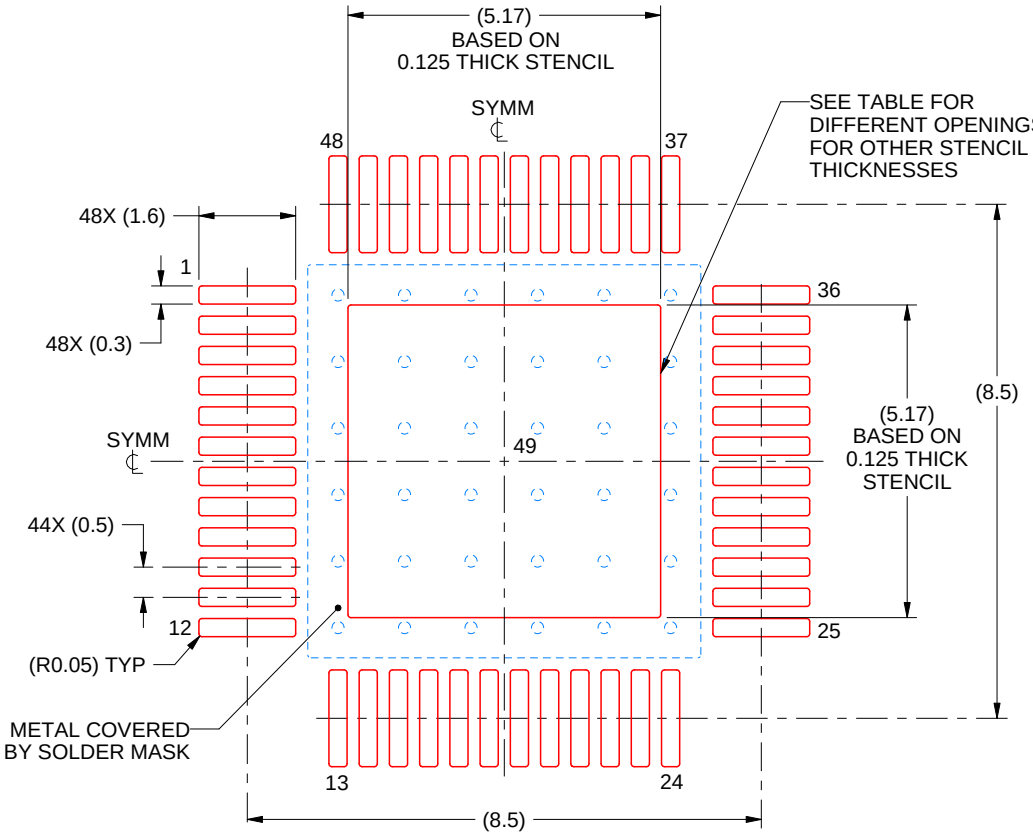


SOLDER MASK DETAILS

4229966/A 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

4229966/A 09/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月