20V, 10A, Synchronous Boost Converter with Load Disconnect Control

1 Features

- Input Voltage Range :2.7V to 20V
- Output Voltage Range: 4.5V to 20V
- Minimal Boost Ratio is down to 1.0
- Efficiency up to 96%: VIN = 7.2 V, VBUS = 16 V, IOUT = 2 A
- Two 7mΩ FETs Integrated
- Adjustable switching frequency up to 2.2MHz
- Programmable Cycle-by-Cycle Current Limit up to 15A
- Hiccup Short Protection with Load Disconnect Drive
- FCCM Operation under light load
- Input Under-Voltage Lockout
- Output Over-Voltage Protection at fixed 21V
- Over-Temperature Protection
- QFN13-FC 3*3.5 Package

2 Applications

- Portable POS terminal
- Bluetooth Speaker
- E-Cigarette
- Thunderbolt Interface
- USB Type-C Power Delivery

3 Description

The PL3050 is a 20-V synchronous Boost converter with the gate driver built-in for load disconnect. The PL3050 integrates two low on resistance power FETs: A 7-mΩ switching FET and a 7-mΩ rectifier FET.

The PL3050 uses the adaptive constant off time peak current mode control. The PL3050 operates in force continues mode to avoid audible noise under light load.

The PL3050 includes configurable features include programmable cycle-by-cycle current limit and programmable switching frequency functions.

The PL3050 could isolate the output from input side when shutdown. Once the output is shorted, it enters into the hiccup mode to lower the thermal stress and can recover automatically after the short condition releases. Additionally, the PL3050 also has OVP and thermal protection to avoid the fault operation. The PL3050 is in a 3.0-mm x 3.5-mm 13-pin VQFN package with enhanced thermal dissipation.

4 Typical Application Schematic

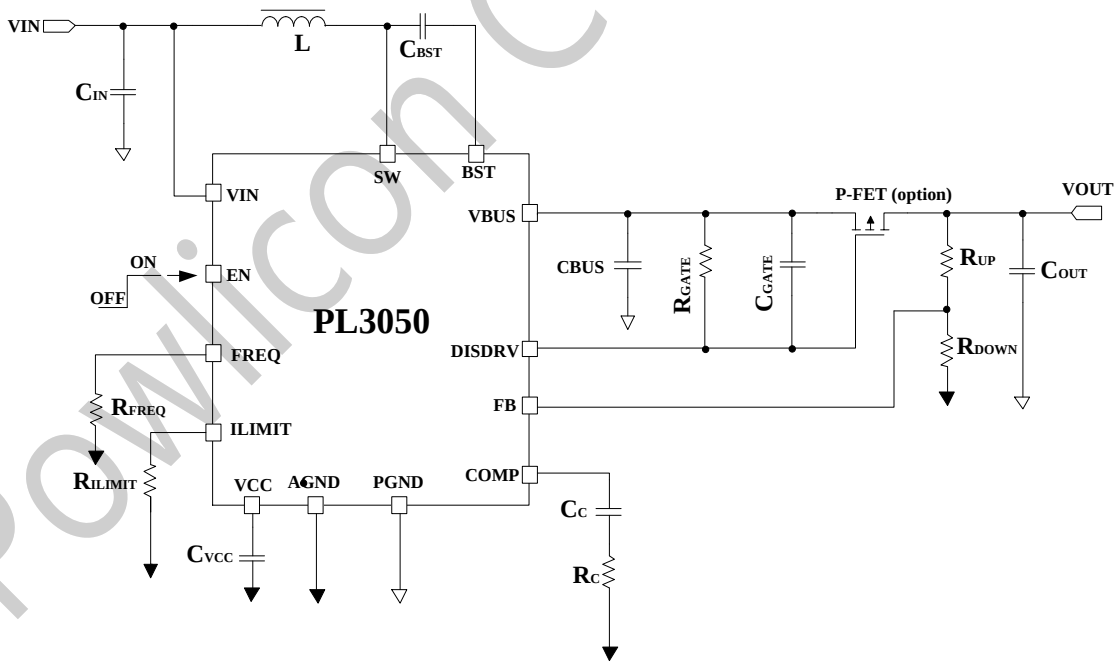


Fig. 1 Application Schematic

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5 Pin Configuration and Functions

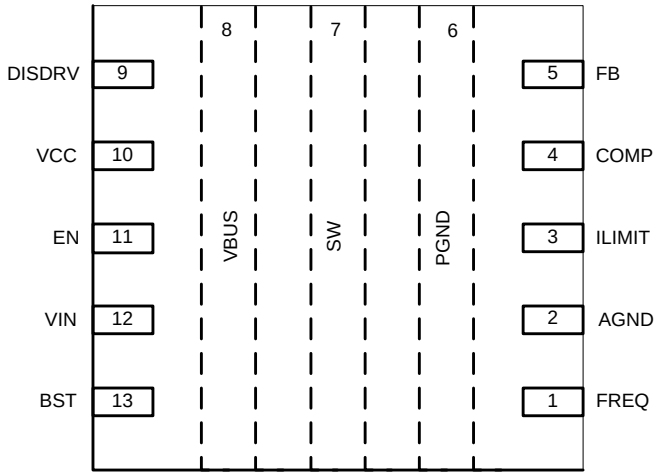


Fig. 2Pin-Function (QFN13-FC)

Pin		Description
Number	Name	
1	**FREQ**	The switching frequency is programmed by a resistor between this pin and the AGND. This pin can't be float in application.
2	**AGND**	Analog ground.
3	**ILIMIT**	A Adjustable LSFET peak current limit. Connect a resistor to AGND.
4	**COMP**	Output of internal error amplifier, loop compensation network connect to COMP and AGND .COMP is a sensitive node, keep COMP away from SW and BST pin.
5	**FB**	Feedback Input. FB senses the output voltage, connect FB with a resistor divider connected between the output and ground. FB is a sensitive node, keep FB away from SW and BST pin.
6	**PGND**	Power ground. The source of LSFET connect to PGND internally.
7	**SW**	Power switching pin of boost converter, common node of LSFET drain and HSFET source. Connect the coil to this pin and power input.
8	**VBUS**	Output pin of boost converter, connect to the drain of HSFET internally.
9	**DISDRV**	A gate drive output for the external disconnect FET. Connect the DISDRV pin to the gate of the external FET. Leave it floating if not using the load disconnect function.
10	**VCC**	Output of internal regulator, A ceramic capacitor of more than 4.7μF is required between this pin and ground.
11	**EN**	Enable pin. Pull high to turn on the IC, don't float.
12	**VIN**	Input supply pin. Bypass Vin to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors close to Vin and GND pins.
13	**BST**	Boot strap pin Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver.

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL3050	**PL3050IFQ13**	**QFNFC3.5X3-13L**	**3000**	**3050 RAAYMD**

PL3050: Part Number
RAAYMD: RAA: Lot NO.; YMD: Package Date

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7 Specifications

7.1 Absolute Maximum Ratings(Note1)

Symbol	Description	Rating	Unit
BST	BST Voltage	–0.3 to SW+6.5	V
V_{VIN}, V_{SW}, V_{DISDRV}, V_{BUS} , V_{EN}	VIN, SW, DISDRV, VBUS, EN voltage	–0.3 to +23	V
Others	FB, COMP, ILIMIT, VCC, FREQ voltage	-0.3 to +6.5	V

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+150	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model		2	kV
	CDM Charger device model		500	V

7.3 Recommended Operating Conditions (Note 2)

Symbol	Description	Rating	Unit
V_{IN}	Input Voltage	2.7 to 20	V
V_{VBUS}	Output Voltage	4.5 to 20	V
V_{BST}	BST voltage	0 to SW+5	V
V_{EN}	EN voltage	0 to VIN	V
V_{SW}, V_{DISDRV}	SW, DISDRV voltage	0 to VBUS	V
Others	FB, COMP, ILIMIT, VCC, FREQ voltage	0 to 5	V
T_A	Operating Ambient Temperature Range	-40 to +85	°C

7.4 Thermal Information(Note 3)

Symbol	Description	QFN13-FC	Unit
θ_{JA}	Junction to ambient thermal resistance	50	°C/W
θ_{JC}	Junction to case thermal resistance	10	

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

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7.5ElectricalCharacteristics

VIN = 2.7 V to 14 V and VOUT = 16 V, TJ = - 40 °C to 125 °C , Typical values are at TJ = 25 °C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Section						
V_{IN}	VIN operating range		2.7		20	V
V_{INUV}	VIN UVLO threshold voltage	when VIN < V_{INUV}, IC turn off, falling edge		2.6		V
V_{INUV_HYS}	VIN UVLO hysteresis voltage	after VIN > V_{INUV}+ V_{INUV_HYS}, IC restore operation		0.35		V
V_{CC}	VCC regulation voltage	I_{VCC}=2mA, VIN=6V		5		V
V_{CCUV}	VCC UVLO threshold voltage	VCC falling edge		2.1		V
V_{CCUV_HYS}	VCC UVLO hysteresis voltage			0.1		V
I_{Q_VIN}	Standby current into VIN pin	VIN=EN=4V, VBUS=12V, FB=1.3V, no Ext. FET		23		uA
I_{Q_VBUS}	Standby current into VBUS pin	VIN=EN=4V, VBUS=12V, FB=1.3V, no Ext. FET		280		uA
I_{SD_VIN}	Shutdown current	EN=0V, VIN=4V		2		uA
VBUS Section						
V_{BUS}	VBUS operating range		4.5		20	V
V_{OVP}	VBUS OVP threshold voltage	Rising edge	20.5	21	21.5	V
V_{OVP_HYS}	VBUS OVP hysteresis voltage	Falling below V_{OVP}		0.5		V
V_{FB}	Reference voltage at FB pin		1.182	1.2	1.218	V
I_{FB}	FB pin leakage current	FB=1.2V	-50		50	nA
Error Amplifier Section						
G_M	Error amplifier trans-conductance	FB=1.2V, COMP=1.5V		610		uS
I_{SOURCE}	COMP pin source current			54		uA
I_{SINK}	COMP pin sink current			54		uA
G_{CS}	COMP to current gain(Note4)			10		S
Power FET Section						
R_{ONLS}	Low side NFET on-resistance	I_{DS}=0.5A		7		mΩ
R_{ONHS}	High side NFET on-resistance	I_{DS}=0.5A		7		mΩ
I_{LKLS}	Low side FET leakage current	VSW=20V			1	uA
I_{LKHS}	High side FET leakage current	VBUS=20V, VSW=0V			1	uA
V_{BST}	High side driver supply voltage	BST-SW		5		V
ILIM Section						
V_{ILIM}	Reference voltage at ILIM			0.5		V
I_{LIM}	Peak LS NFET current limit	RLIM=100k Ohm, Ilimit=1M/RSET	8	10	12	A
		RLIM=200k Ohm, Ilimit=1M/RSET	4	5	6	A
Fsw Section						
f_{SW}	Switching frequency	R_{FREQ}=100k, Fs = 5x10^10/R_{FREQ}		500		kHz
t_{on_min}	Minimum LSFET on time(Note4)			105		ns
t_{off_min}	Minimum HSFET on time(Note4)			140		ns
EN section						
V_{EN_H}	EN high threshold voltage	EN > V_{EN_H}, enable IC after t_{EN_ON}		1.2		V
V_{EN_L}	EN low threshold voltage	EN < V_{EN_L}, shutdown IC		1.0		V
I_{EN}	EN input current	VEN=1.3V	-50		50	nA

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Electrical Characteristics(continued)

VIN = 2.7 V to 14 V and VOUT = 16 V, TJ = - 40 °C to 125 °C , Typical values are at TJ = 25 °C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Short Circuit Protect section						
I_{OCP}	LS NFET current threshold for OCP			15		A
I_{SCP}	LS NFET current threshold for SCP			20		A
V_{SCP}	FB voltage threshold for SCP			0.4		V
T_{HICCUP}	Waiting time for restart in hiccup mode			120		mS
Soft Start section						
T_{POR}	POR time			2		mS
T_{PRE_CHG}	VBUS Pre-charge time			4		mS
T_{TURN_ON}	Disconnect MOS Turn on time			4		mS
$T_{STARTUP}$	FB Soft Startup time			4		mS
OTP section						
T_{SD}	Thermal shutdown temperature			150		° C
T_{SD_HYS}	Thermal shutdown hysteresis temperature			20		° C

Note:

4) Guaranteed by design, not tested in production.

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7.6 Typical Characteristics

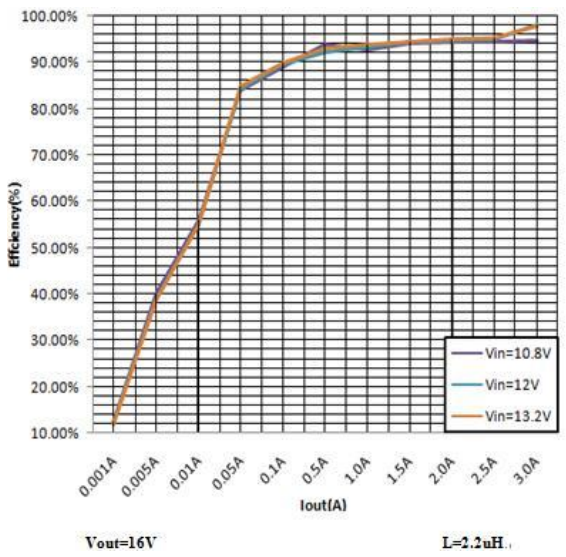


Fig. 3 Efficiency

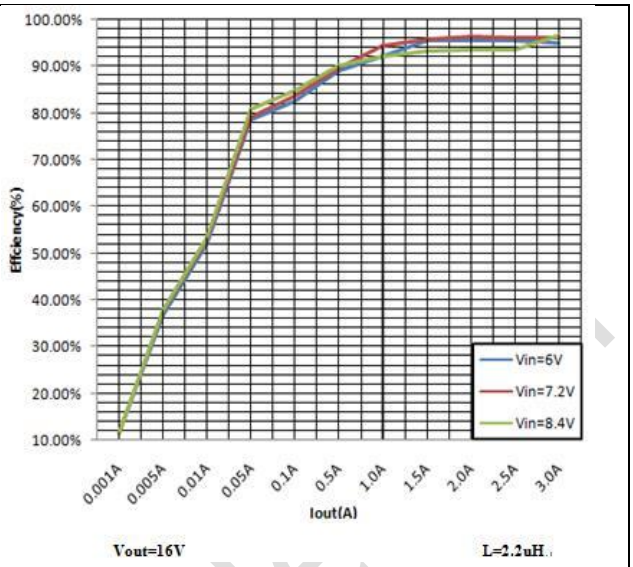
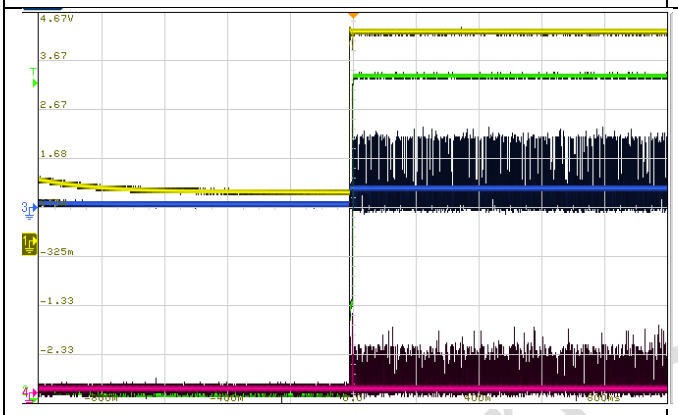


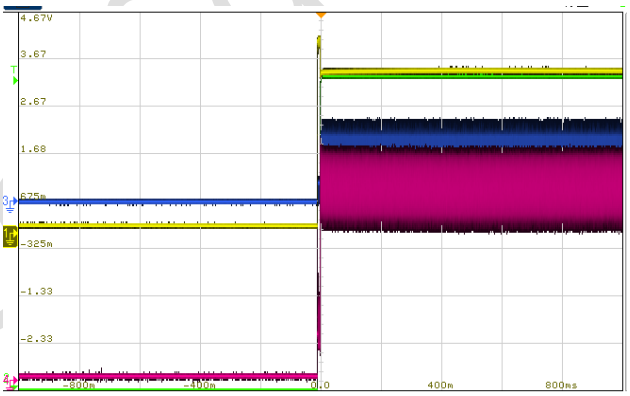
Fig. 4 Efficiency



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=3.6V Vout=14V

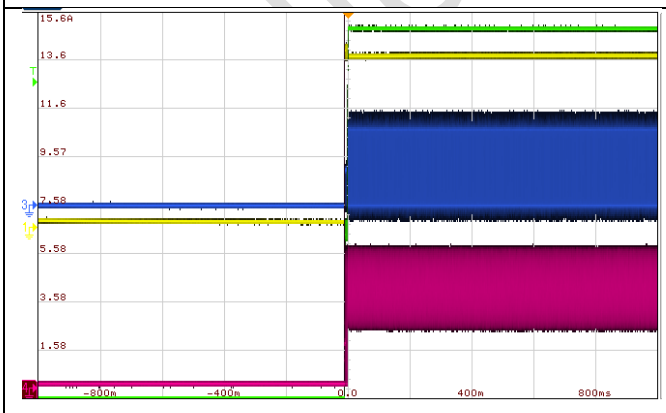
Fig.5 Startup waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=3.6V Vout=14V

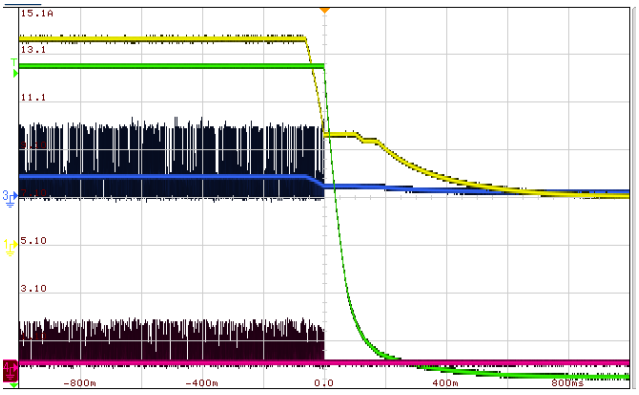
Fig.6 Startup waveform, Iout =2A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=7.2V Vout=16V

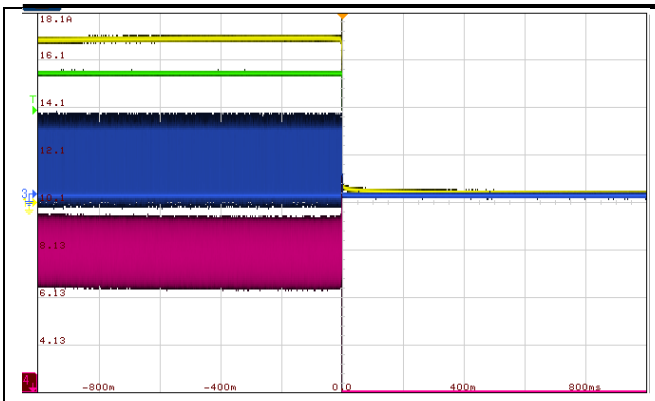
Fig.7 Startup waveform, Iout =2A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=3.6V Vout=14V

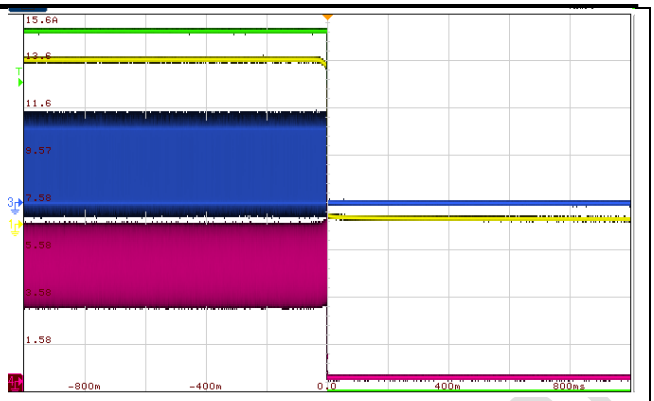
Fig.8 Shutdown waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=3.6V Vout=14V

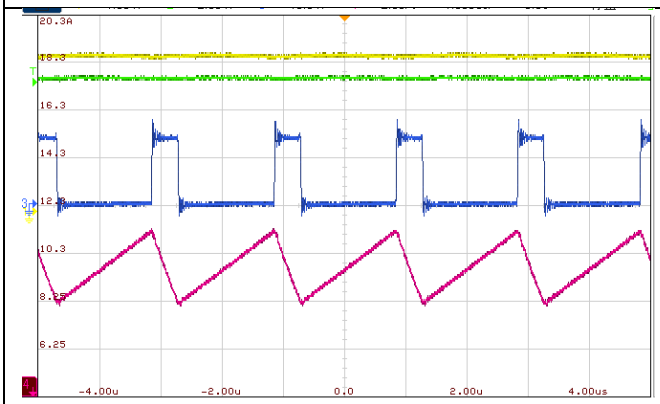
Fig.9 Shutdown waveform, Iout =2A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=7.2V Vout=16V

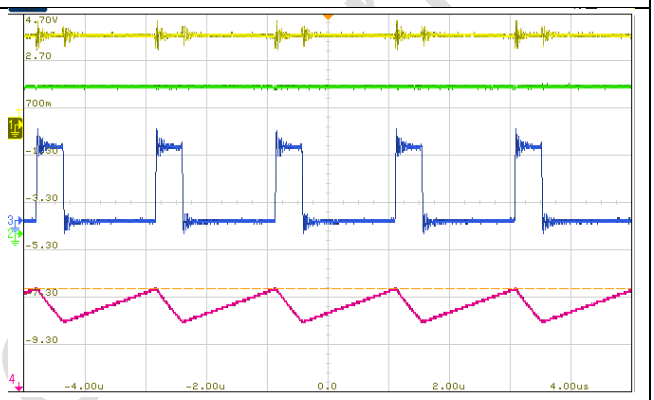
Fig.10 Shutdown waveform, Iout =2A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=3.6V Vout=14V

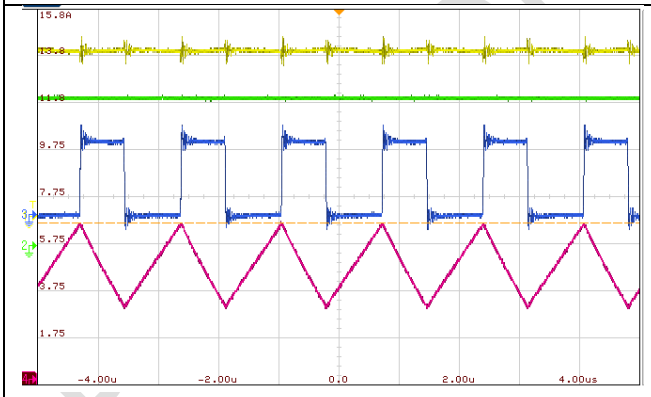
Fig.11 Steady State, Iout =2A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=3.6V Vout=16V

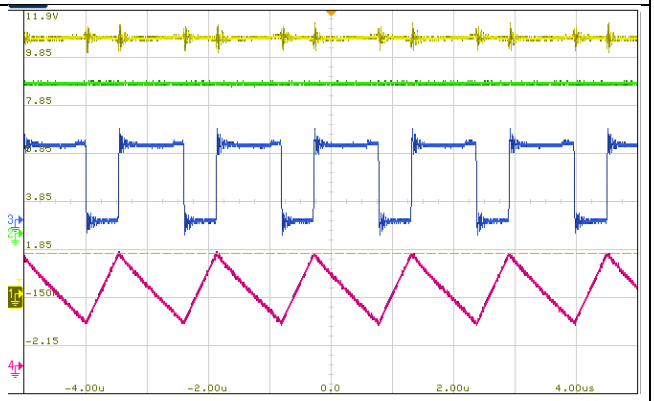
Fig.12 Steady State, Iout =2A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=7.2V Vout=16V

Fig.13 Steady State, Iout =2A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=10.8V Vout=16V

Fig.14 Steady State, Iout =2A

8. Detailed Description

8.1 Overview

The PL3050 is a synchronous boost converter designed for delivering the switch peak current up to 15A and output voltage up to 20 V. The PL3050 adopts adaptive constant off time peak current mode control operates in force continues mode to avoid audible noise under light load current. With this control scheme, the PL3050 provides the excellent line and load transient response with the minimal output capacitor. The external loop compensation brings the flexibility to use a wider range of the inductor and output capacitor combinations.

The PL3050 supports the adjustable switching frequency up to 2.2MHz. The device implements a programmable cycle-by-cycle current limit to protect the device from overload during the boost operation phase. The PL3050 triggers the hiccup short protection if the output current further increases and exceeds the short current threshold or the output voltage drops below the short threshold. And this device recovers automatically once the short condition releases.

Additionally, the PL3050 provides the gate driver for the external FET to isolate the output from input during shutdown.

8.2 Functional Block Diagram

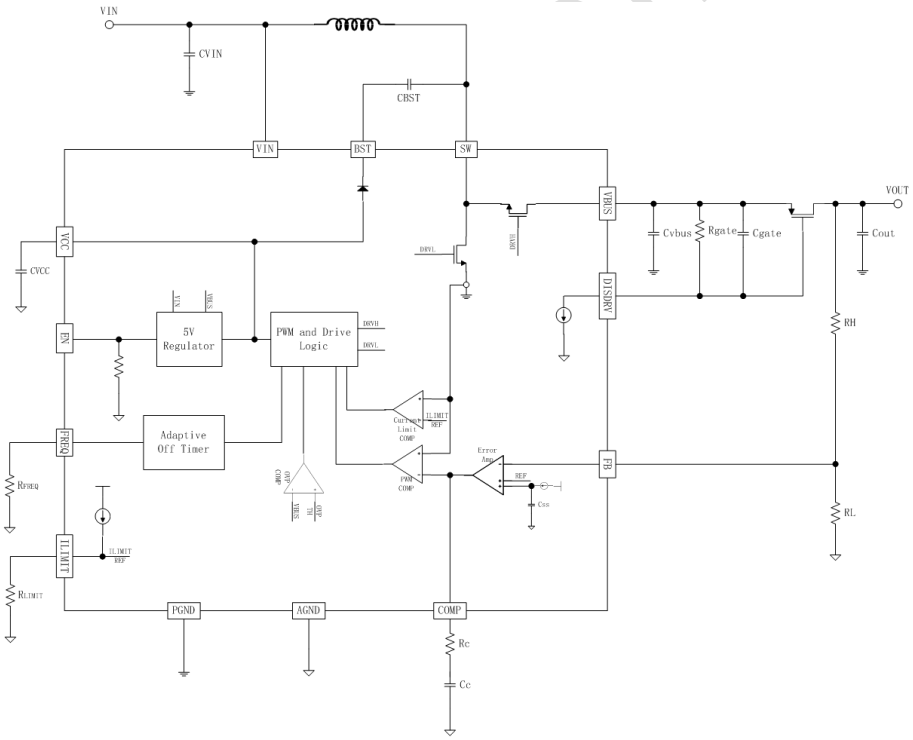


Figure 15

8.3 Feature Description

8.3.1 Under-voltage Lockout

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the UVLO threshold of 2.25 V. A hysteresis of 350 mV is added so that the device cannot be enabled again until the input voltage exceeds 2.6 V. This function is implemented in order to prevent malfunctioning of

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the device when the input voltage is between 2.25 V and 2.6 V.

8.3.2 Enable and Disable

When the input voltage is above UVLO rising threshold of 2.6 V and the EN pin is pulled high above 1.2 V, the PL3050 is enabled. When the EN pin is pulled below 1 V, the PL3050 goes into the shutdown mode and stops switching.

8.3.3 Startup

When the input voltage to the device exceeds the UVLO threshold and EN pin pulled to high as well, the PL3050 starts to ramp up the output voltage. There is a switching pre-charge phase and the output voltage is charged up to input voltage (1.0 x V_{IN}).

After the pre-charge phase ends (typical 4 ms), The PL3050 gradually turns on the external FET at the output side, which completely disconnects the output from the input during shutdown or output short happens.

After the turn-on phase ends (typical 4 ms), The PL3050 regulates the FB pin to the internal soft start voltage and results in a gradual rise of the output voltage starting from the input voltage level to the target output voltage. The soft start time is typical 4 ms, which helps the regulator to gradually reach the steady state setting point, thus reducing the startup stresses and surges.

8.3.4 Load Disconnect Gate Driver

The PL3050 device provides a DISDRV pin to drive the external FET at the output side, which completely disconnects the output from the input during shutdown or output short happens. During the device's start-up phase, the disconnect FET is controlled by the gate driver voltage of the external disconnect FET, there is an internal 55 μA (typical) sink current. The load disconnect FET connection is shown as *Figure 7.*

The driver voltage and turn on / off timing can be set via the resistor and capacitor connecting between the DISDRV pin and the source of the external FET. See the Application and Implementation section for the details of how to select the gate resistor and capacitor.

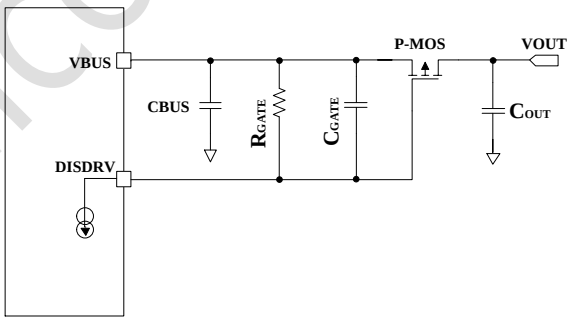


Figure 16

8.3.5 Adjustable Cycle-by-Cycle Switching Current Limit

When the PL3050 is in the normal boost switching phase, the device is prevented from the over current condition via the cycle by cycle current limit by sensing the current through the internal low-side FET. When the peak switch current triggers the current limit threshold, the low-side switch turns off to prevent the switching current further increasing.

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The peak switch current limit can be set by a resistor connecting with the I_{LIMIT} pin. The relationship between the current limit and the resistor is determined by Equation 1

$$R_{LIMIT} = \frac{1000}{I_{LIMIT}} \quad (1)$$

Where R_{LIMIT} is the resistor for setting the current limit, with the unit of kΩ, I_{LIMIT} is switching peak current limit, with the unit of A. For instance, when the resistor value is 100 kΩ, the switch peak current limit is 10 A.

8.3.6 Output Short Protection (with load disconnected FET)

In addition to the cycle-by-cycle current limiting, the PL3050 also has the output short protection. If theinductor current reaches the short protection limit threshold (typical 20A) or the output voltage drops below 30%(typical) of the normal output voltage, the device enters into the hiccup protection mode. In the hiccup mode, thedevice shuts down itself and restarts after 120ms (typical) waiting time which helps to reduce the total thermal dissipation. After the short condition releases, the device can recover automatically and restart the start-up phase.

8.3.7 Adjustable Switching Frequency

The PL3050 features of a wide adjustable switching frequency ranging up to 2.2MHz. The switching frequency is set by a resistor connecting with the FREQ pin. This pin cannot be left floating in the application. Use Equation 2to calculate the resistor value for a desired frequency.

$$Freq = \frac{50000}{R_{Freq}} \text{ kHz} \quad (2)$$

Where R_{Freq} is the resistor for setting the frequency, with the unit of kΩ, Freq is switching frequency, with the unit of kHz. For instance, when the resistor value is 100 kΩ, the switching frequency is 500 kHz.

8.3.8 Error Amplifier

The PL3050 has a trans-conductance amplifier and compares the feedback voltage with the internal voltage reference (or the internal soft start voltage during startup phase). The trans-conductance of the error amplifier is 610 μA / V typically. The loop compensation components are required to be placed between the COMP terminal and ground to balance the loop stability and the transient response time.

8.3.9 Start-up with the Output Pre-Biased

The PL3050 has been designed to prevent the low-side FET from discharging a pre-biased output. During the pre-biased startup, both high-side and low-side FETs are not allowed to be turned on until the internal soft start voltage is higher than the sensed output voltage at FB pin.

8.3.10 Bootstrap Voltage (BST)

The PL3050 has an integrated bootstrap regulator, and requires a small ceramic capacitor between the BST pin and SW pin to provide the gate drive voltage for the high-side FET. The bootstrap capacitor is charged when the BST-SW voltage is below regulation. The value of this ceramic capacitor should be above 100 nF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and DC biased voltage.

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8.3.11 Over-voltage Protection

If the voltage at the V_{BUS} pin is detected above over-voltage protection threshold, typically 21 V, the PL3050 stops switching immediately until the voltage at the V_{BUS} pin drops lower than the output over voltage protection threshold (with 500mV hysteresis). This function prevents the devices against the over-voltage and secures the circuits connected to the output from excessive over voltage.

8.3.12 Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 150°C. When the thermal shutdown is triggered, the device stops switching and recover when the junction temperature falls below 130°C(typical).

8.4 Device Functional Modes

PL3050 operates at the adaptive constant off time peak current mode control (CMCOT). At the beginning of each switching cycle, the low-side FET switch turns on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. The PWM controller turns off the low-side FET when the peak inductor current reaches a threshold level set by the error amplifier output. After the low-side FET turns off, the high-side synchronous FET is turned on after a short dead time until the adaptive off timer end or until the inductor current reaches the reverse current sense threshold.

During the portion of the switching cycle when the low-side FET is on, the input voltage is applied across the inductor and stores the energy as the inductor current ramps up. Meanwhile only the output capacitor supplies the load current. When it turns off the low-side FET, the inductor transfers the stored energy via the high-side synchronous FET to replenish the output capacitor and also supply the load current. This operation repeats every switching cycle.

9 Application and Implementation

9.1 Setting the switching Frequency

The switching frequency of the PL3050 is set at 500 kHz. Use Equation 2 to calculate the required resistor value. For a target switching frequency of 500 kHz, The calculated value is 100 kΩ.

9.2 Setting the Cycle-By-Cycle Current Limit

The current limit of the PL3050 could be programmed by an external resistor. Use Equation 1 to calculate the required resistor value. For a target current limit of 10 A, the calculated resistor value is 100 kΩ.

9.3 Setting the Output Voltage

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R1 and R2. A value between 10k and1M is recommended for both resistors. If R1=200k is chosen, then R2 can be calculated to be:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

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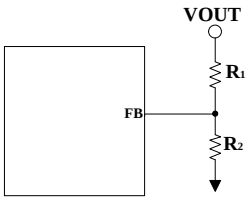


Figure 17

9.4 Selecting the Inductor

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum verage input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{0.4 \times F_{SW} \times I_{OUT_MAX}} \quad (4)$$

where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

PL3050 is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT_MIN} > \frac{V_{OUT}}{V_{IN}} \times I_{OUT_MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{2 \times F_{SW} \times L} \quad (5)$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to a chieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve a good overall efficiency.

9.5 Selecting the Output Capacitors

The Boost Output capacitor CBD and disconnection FET Output capacitor COUT are selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken in to account when selecting these capacitors. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 25V rating and more than 22uF capacitors.

9.6 Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 22-μF input capacitor is sufficient for the most applications, larger values may be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, should be

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placed between CIN and the power source lead to reduce ringing that can occur between the inductance of the power source leads and CIN.

9.7 Selecting the Disconnect FET

The PL3050 provides a gate driver to control an external FET to disconnect the output from the input at shutdown or output short conditions, shown in Figure 7.

The V_{DS}, I_{DS} and safe operation area (SOA) should be taken into consideration when selecting the FET:

• The drain-to-source voltage rating should be higher than the output max. voltage, $V_{DS_DIS_MAX} = V_{OUT}$,

• The drain-to-source RMS current rating is the maximum output current. $I_{DS_DIS_RMS} = I_{OUT}$,

• The SOA should be considered when the output short occurs, and there is heat caused by the short protection response time and surge current, SOA > Q_{SHORT}.

$$Q_{SHORT} = 0.5 \times V_{OUT} \times I_{SHORT} \times T_{SHORT} \quad (6)$$

where

• $V_{DS_DIS_Max}$ is the maximum drain-source voltage

• I_{DS_DIS} is the drain-source RMS current

• I_{SHORT} is the short current

• T_{SHORT} is the response time before the short protection triggered

• Q_{SHORT} is the heat produced for the output short

For instance: V_{OUT} = 16 V, I_{SHORT} = 20 A , T_{SHORT} = 30 μs.

SOA ≥ 4.8 mJ, $V_{DS_DIS_MAX}$ ≥ 16 V.

An additional capacitor between the gate and source of the external FET is required to slow the turn-on speed.

$$T_{ON_PFET} = \frac{V_{TH_PFET} \times C_{GS_PFET}}{I_{DIS_PFET}} \quad (7)$$

where

• T_{ON_PFET} is the on time of external FET

• V_{TH_PFET} is the gate threshold of external FET

• C_{GS_PFET} is the total gate capacitance of connected between gate and source external FET. (including the gate-source capacitance of the FET)

•I_{DIS_PFET} is the discharge current inside of PL3050, it is 55μA typically

Given 1.5 V threshold, C_{GS_PFET} is 10nF, the T_{ON_PFET} is around 300μs.Please be aware that the maximum turn on time should not exceed 4ms, and the maximum capacitance C_{GS_PFET} should be < 100nF. Otherwise, the PL3050 could not startup normally if the disconnect FET could not be turn on within the 4ms.

The gate resistor depends on the gate-source voltage of the external FET,

$$R_{GATE} = \frac{V_{GATE}}{I_{DIS_PFET}} \quad (8)$$

Given the 5-V V_{GATE}, the R_{GATE} = 100kΩ.

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9.8 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during each cycle's turn-on and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1μF to 1μF. CBST should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1μF was selected for this design example.

9.9 Selecting the VCC Capacitor

The primary purpose of the VCC capacitor is to supply the peak transient currents of the driver and bootstrap capacitor as well as provide stability for the VCC regulator. The value of CVCC should be at least 10 times greater than the value of CBST, and should be a good quality, low ESR, ceramic capacitor. CVCC should be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 4.7 μF was selected for this design example.

9.10 Design Example

9.10.1 PL3050 with 14-V Output from 2.7-V to 4.4-V Input Voltage

The Figure 18 is the typical application schematic for 2.7-V to 4.4-V input (single cell Li+ battery) to output 14-Voutput converter. The inductor can be lower to 1.8μH for the 14-V output.

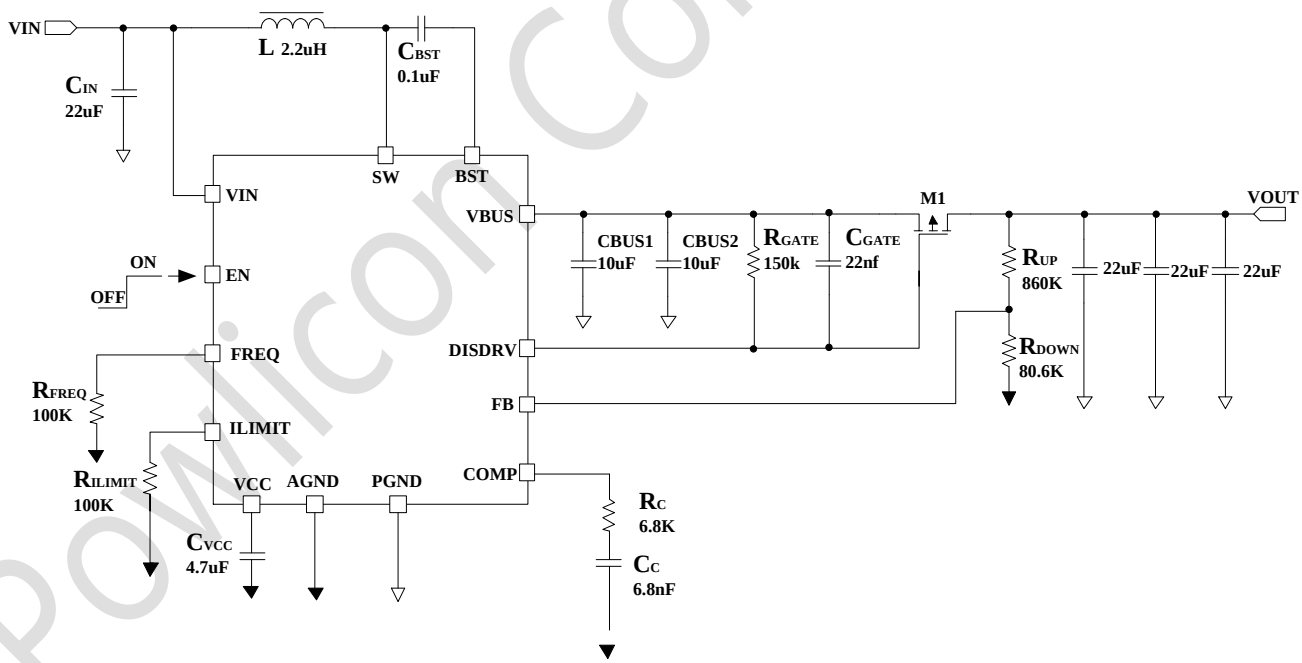


Figure 18. 14-V Output Voltage With Load Disconnect Function

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9.10.2 PL3050 Without Load Disconnect Function

The Figure 19 is the typical application schematic is for 6-V to 14-V input (2 / 3 cells Li+ battery or 12-V bus) to output 16-V output converter without load disconnect. With removing the load disconnect FET, it simplifies the design and minimizes the external components.

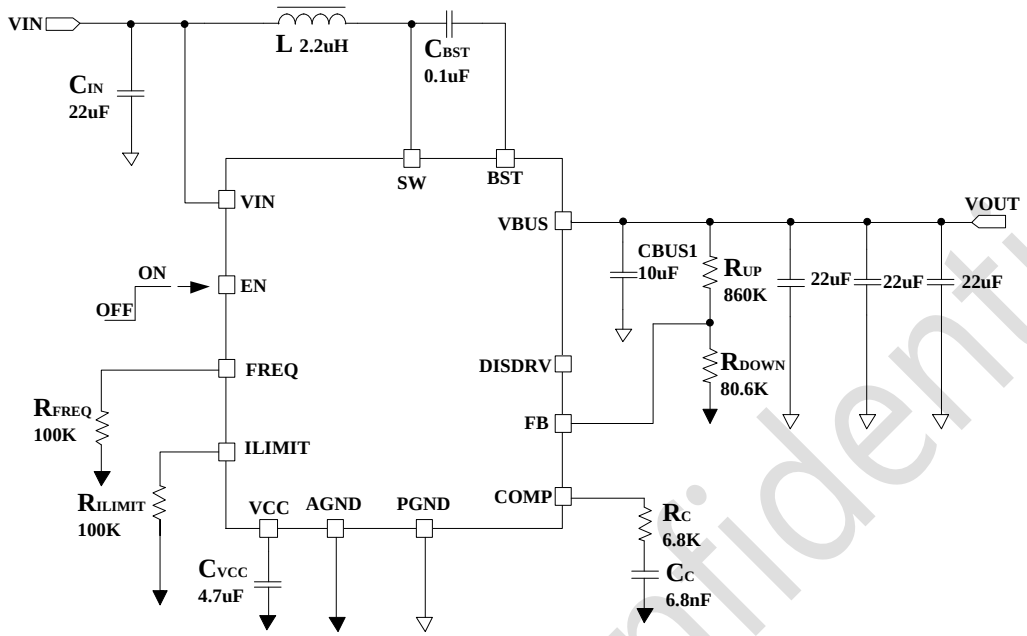


Figure 19. 14-V Output Voltage Without Load Disconnect Functio

10 PCB Layout

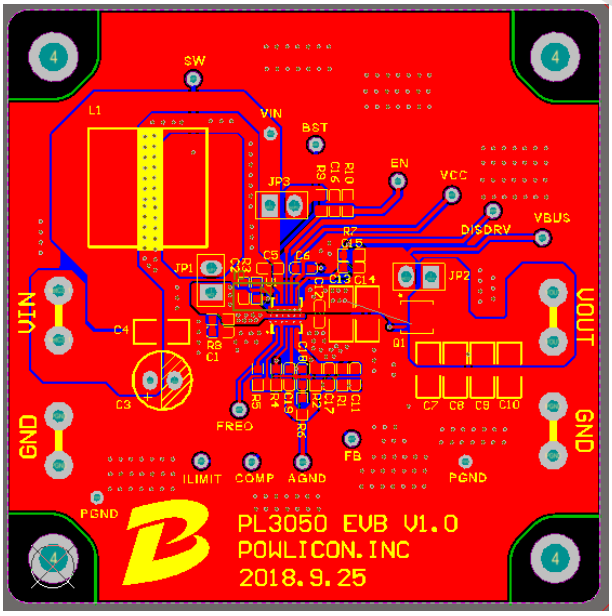


Figure 20. Top lay

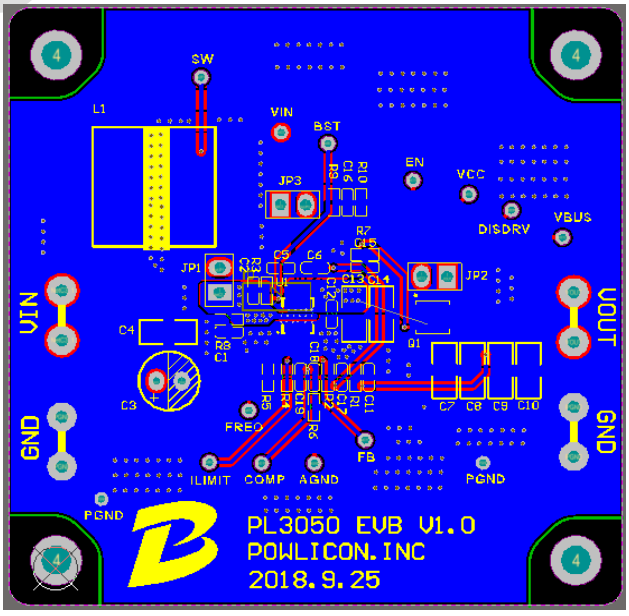
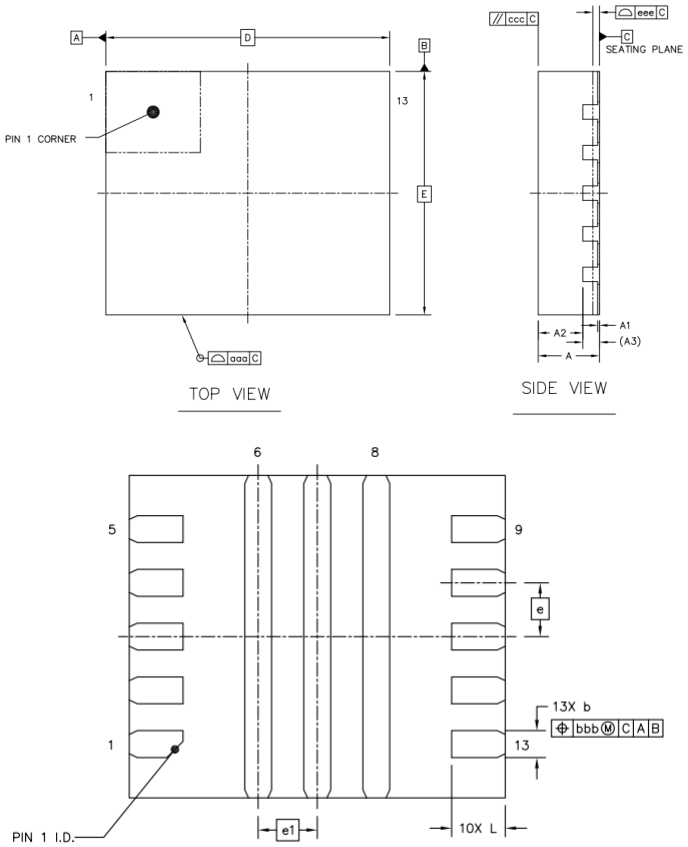


Figure 21. Bottom l

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11 Packaging Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3.5 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
		e1		0.55 BSC	
LEAD LENGTH		L	0.4	0.5	0.6
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	

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