PF3001

Power Management Integrated Circuit (PMIC) for i.MX 7 and i.MX 6 SoloLite/ SoloX/UltraLite Processors

Rev. 5.1 — 16 June 2026 Product data sheet



1 General description

The PF3001 is the power management integrated circuit (PMIC) designed primarily for use with NXP's i.MX series of multi-media application processors. It is also capable of providing full power solutions to i.MX 6SL, 6SX, 6UL, and i.MX7processors.

2 Features and benefits

This section summarizes the PF3001 features.

- Input voltage range to PMIC: 2.8 V to 4.5 V, or 3.7 V to 5.5 V [1]

– Buck regulators
  - SW1, 2.75 A; 0.7 V to 1.425 V, 1.8 V, 3.3 V
  - SW2, 1.25 A; 1.50 V to 1.85 V, or 2.50 V to 3.30 V
  - SW3, 1.5 A; 0.90 V to 1.65 V
  - Dynamic voltage scaling
  - Modes: PWM, PFM, APS
  - Programmable output voltage
  - Programmable current limit
  - Programmable PWM switching frequency

– LDOs
  - VCC_SD, 1.8 V to 1.85 V, or 2.85 V to 3.30 V, 100 mA based on SD_VSEL
  - V33, 2.85 V to 3.30 V, 350 mA
  - VLDO1, 1.8 V to 3.3 V, 100 mA
  - VLDO2, 0.80 V to 1.55 V, 250 mA
  - VLDO3, 1.8 V to 3.3 V, 100 mA
  - VLDO4, 1.8 V to 3.3 V, 350 mA

- Always ON RTC regulator/switch VSNVS 3.0 V, 1.0 mA
- Battery backed memory including coin cell charger
- I^2C interface

1 2.8 V to 4.5 V when VIN is used at input. 3.7 V to 5.5 V when VPWR is used as input.

3 Applications

- IPTV
- Set top boxes
- POS terminals
- Industrial control
- Medical monitoring
- Home automation/security/energy management

4 Ordering information

The PF3001 is available with pre-programmed OTP memory configurations. The devices are identified using the program codes from Table 1. Details of the startup programming for each device can be found in Table 4.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	Programming options	Notes
MC32PF3001A1ES	-40 °C to 85 °C (For use in consumer applications)	98ASA00933D, 48 QFN 7.0 mm x 7.0 mm WF-type (wettable flank)	1 (i.MX 7 with DDR3L)	[1] [2]
MC32PF3001A1EP				
MC32PF3001A2ES			2 (i.MX 7 with LPDDR3)	
MC32PF3001A2EP				
MC32PF3001A3ES			3 (i.MX 6SX with DDR3L)	
MC32PF3001A3EP				
MC32PF3001A4ES			4 (i.MX 6SX with DDR3)	
MC32PF3001A4EP				
MC32PF3001A5ES			5 (i.MX 6SL with LPDDR2)	
MC32PF3001A5EP				
MC32PF3001A6ES			6 (i.MX 6UL with LPDDR2)	
MC32PF3001A6EP				
MC32PF3001A7ES			7 (i.MX 6UL with DDR3L)	
MC32PF3001A7EP				
MC33PF3001A6ES	-40 °C to 105 °C (For use in automotive applications)	98ASA00933D, 48 QFN 7.0 mm x 7.0 mm WF-type (wettable flank)	6 (i.MX 6UL with LPDDR2)	[1]
MC33PF3001A7ES			7 (i.MX 6UL with DDR3L)	

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Table 1. Orderable part variations*...continued*

Part number	Temperature (T_A)	Package	Programming options	Notes
MC34PF3001A1ES	-40 °C to 105 °C (For use in Industrial applications)	98ASA00933D, 48 QFN 7.0 mm x 7.0 mm WF-type (wettable flank)	1 (i.MX 7 with DDR3L)	[1] [2]
MC34PF3001A1EP				
MC34PF3001A2ES			2 (i.MX 7 with LPDDR3)	
MC34PF3001A2EP				
MC34PF3001A3ES			3 (i.MX 6SX with DDR3L)	
MC34PF3001A3EP				
MC34PF3001A4ES			4 (i.MX 6SX with DDR3)	
MC34PF3001A4EP				
MC34PF3001A5ES			5 (i.MX 6SL with LPDDR2)	
MC34PF3001A5EP				
MC34PF3001A6ES			6 (i.MX 6UL with LPDDR2)	
MC34PF3001A6EP				
MC34PF3001A7ES			7 (i.MX 6UL with DDR3L)	
MC34PF3001A7EP				

[1] For Tape and Reel add an R2 suffix to the part number.
[2] The ~EP parts are not recommended for new designs.

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5 Internal block diagram

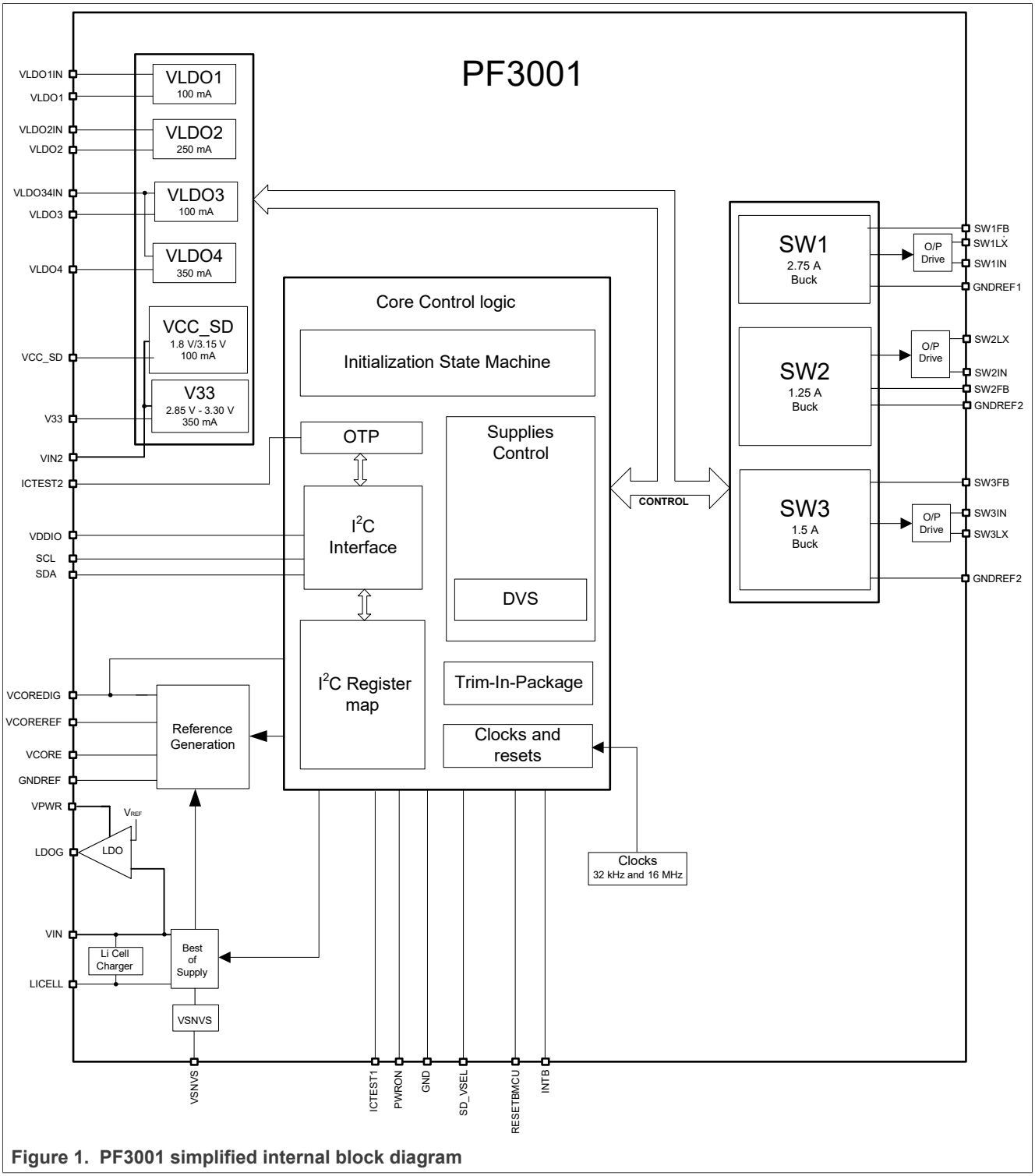


Figure 1. PF3001 simplified internal block diagram

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6 Functional block diagram

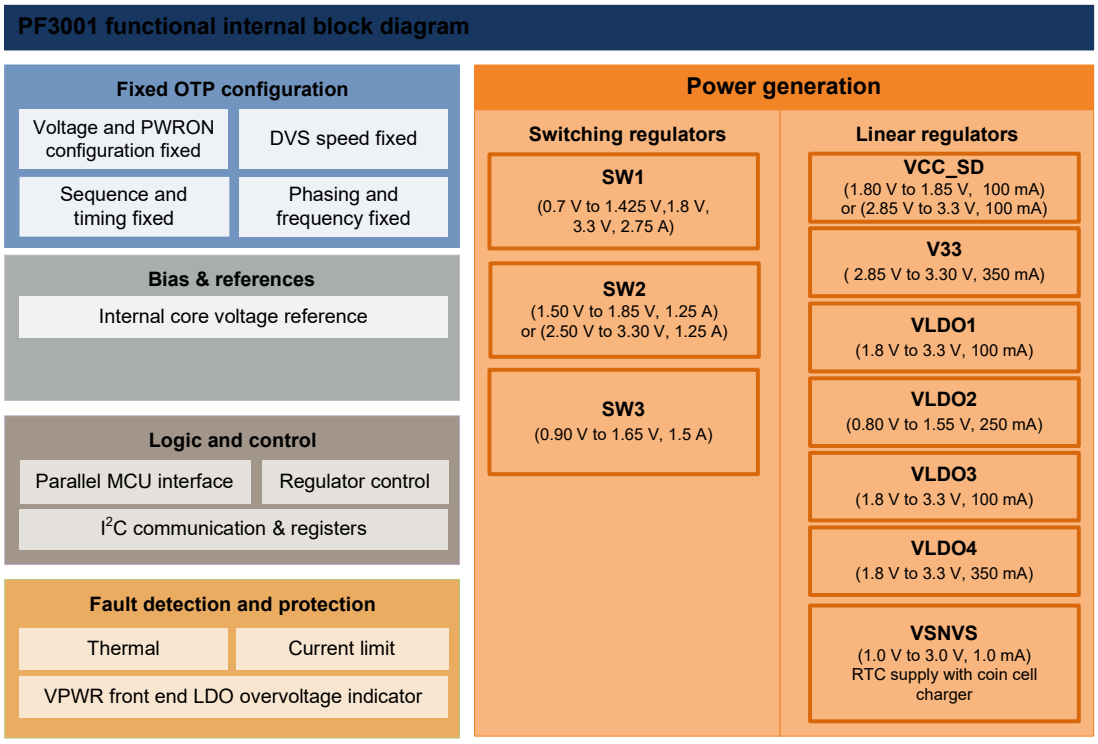


Figure 2. PF3001 functional block diagram

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7 Pinning information

7.1 Pinning diagram

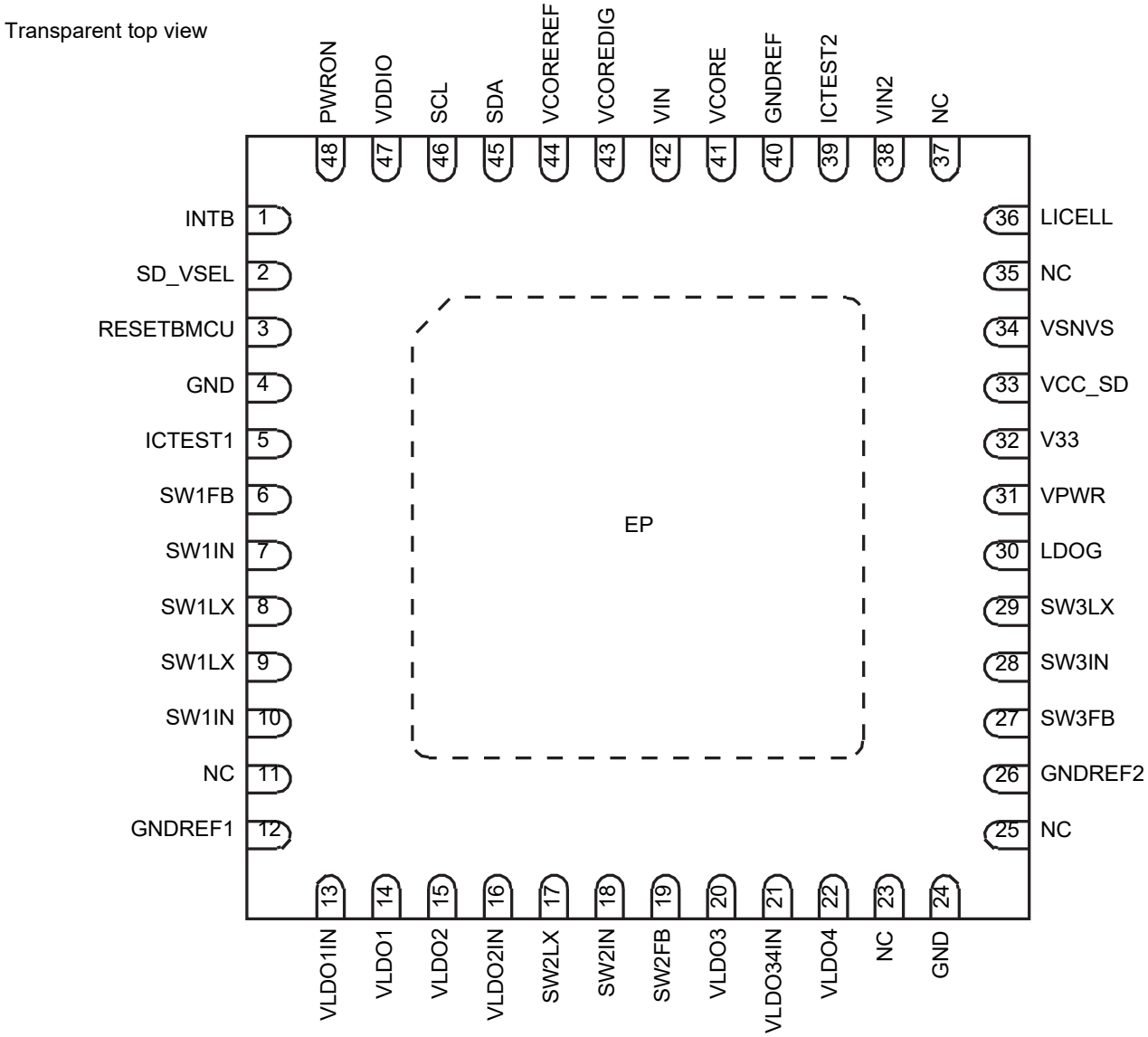


Figure 3. Pinning diagram

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7.2 Pin descriptions

Table 2. Pin descriptions

Pin number	Pin name	Pin function	Type	Definition
1	INTB	O	Digital	Open drain interrupt signal to processor
2	SD_VSEL	I/O	Digital	Input from i.MX processor to select VCC_SD regulator voltage • SD_VSEL=0, VCC_SD = 2.85 V to 3.3 V • SD_VSEL= 1, VCC_SD = 1.8 V to 1.85 V
3	RESETBMCU	O	Digital	Open drain reset output to processor
4	GND	I	GND	Ground reference. Connect to ground.
5	ICTEST1	I	Digital and Analog	Reserved pin. Connect to GND in application
6	SW1FB[1]	I	Analog	SW1 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitance or near the load, if possible for best regulation
7	SW1IN[1]	I	Analog	Input to SW1 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
8	SW1LX[1]	O	Analog	Switcher 1 switch node connection. Connect to SW1LX and connect to SW1 inductor
9	SW1LX[1]	O	Analog	Switcher 1 switch node connection. Connect to SW1LX and connect to SW1 inductor
10	SW1IN[1]	I	Analog	Input to SW1 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
11	NC	–	Reserved	Leave floating
12	GNDREF1	GND	GND	Ground reference for SW1. Connect to GND. Keep away from high current ground return paths
13	VLDO1IN	I	Analog	VLDO1 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
14	VLDO1	O	Analog	VLDO1 regulator output. Bypass with a 2.2 µF ceramic output capacitor
15	VLDO2	O	Analog	VLDO2 regulator output. Bypass with a 4.7 µF ceramic output capacitor
16	VLDO2IN	I	Analog	VLDO2 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
17	SW2LX[1]	O	Analog	Switcher 2 switch node connection. Connect to SW2 inductor
18	SW2IN[1]	I	Analog	Input to SW2 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
19	SW2FB[1]	I	Analog	SW2 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
20	VLDO3	O	Analog	VLDO3 regulator output. Bypass with a 2.2 µF ceramic output capacitor
21	VLDO34IN	I	Analog	VLDO3 and VLDO4 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
22	VLDO4	O	Analog	VLDO4 regulator output. Bypass with a 2.2 µF ceramic output capacitor
23	NC	–	Reserved	Leave floating
24	GND	GND	GND	Ground reference. Connect to ground. Keep away from high current ground return paths
25	NC	–	Reserved	Leave floating
26	GNDREF2	GND	GND	Reference ground for SW2 and SW3 regulators. Connect to GND. Keep away from high current ground return paths

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Table 2. Pin descriptions*...continued*

Pin number	Pin name	Pin function	Type	Definition
27	SW3FB[1]	I	Analog	SW3 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
28	SW3IN[1]	I	Analog	Input to SW3 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
29	SW3LX[1]	O	Analog	Switcher 3 switch node connection. Connect the SW3 inductor
30	LDOG	O	Analog	Connect to gate of front-end LDO external pass P-MOSFET. Leave floating if VPWR LDO is not used
31	VPWR	I	Analog	Input to optional front-end VPWR LDO for systems with input voltage > 4.5 V
32	V33	O	Analog	V33 regulator output. Bypass with a 4.7 µF ceramic output capacitor
33	VCC_SD	O	Analog	Output of VCC_SD regulator. Bypass with a 2.2 µF ceramic output capacitor.
34	VSNVS	O	Analog	VSNVS regulator/switch output. Bypass with 0.47 µF capacitor to ground.
35	NC	–	Reserved	Leave floating
36	LICELL	I/O	Analog	Coin cell supply input/output. Bypass with 0.1 µF capacitor. Connect to optional coin cell.
37	NC	–	Reserved	Leave floating
38	VIN2	I	Analog	Input to VCC_SD, V33 regulators. Connect to VIN rail and bypass with 10 µF capacitor
39	ICTEST2	I	Digital & Analog	Reserved pin. Connect to GND in application
40	GNDREF	GND	GND	Ground reference for IC core circuitry. Connect to ground. Keep away from high current ground return paths
41	VCORE	O	Analog	Internal analog core supply. Bypass with 1.0 µF capacitor to ground
42	VIN	I	Analog	Main IC supply. Bypass with 1.0 µF capacitor to ground. Connect to system input supply if voltage ≤ 4.5 V. Connect to drain of external PFET when VPWR LDO is used for systems with input voltage > 4.5 V
43	VCOREDIG	O	Analog	Internal digital core supply. Bypass with 1.0 µF capacitor to ground
44	VCOREREF	O	Analog	Main band gap reference. Bypass with 220 nF capacitor to ground
45	SDA	I/O	Digital	I^2C data line (open drain). Pull up to VDDIO with a 4.7 kΩ resistor
46	SCL	I	Digital	I^2C clock. Pull up to VDDIO with a 4.7 kΩ resistor
47	VDDIO	I	Analog	Supply for I^2C bus. Bypass with 0.1 µF ceramic capacitor. Connect to 1.7 V to 3.6 V supply. Ensure VDDIO is always lesser than or equal to VIN
48	PWRON	I	Digital	Power ON/OFF input from processor
–	EP	GND	GND	Expose pad. Functions as ground return for buck and boost regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation

[1] Unused switching regulators should be connected as follows: Pins SWxLX and SWxFB should be unconnected and Pin SWxIN should be connected to VIN with a 0.1 µF bypass capacitor.

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8 Functional description

8.1 Introduction

The PF3001 is a highly integrated, low quiescent current power management IC featuring three buck regulators and seven LDO regulators. The PF3001 provides all the necessary rails to power a complete system including the application processor, memory, and peripherals. The PF3001 operates from an input voltage of up to 5.5 V. Output voltage, startup sequence, and other functions are set in integrated one-time-programmable (OTP) memory.

8.2 Power generation

The buck regulators in the PF3001 provide supply to the processor cores and to other voltage domains, such as I/O and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and other circuitry.

The linear regulators in the PF3001 can be used as general purpose regulators to power peripherals and lower power processor rails. The VCC_SD LDO regulator supports the dual voltage requirement by high speed SD card readers. Depending on the system power path configuration, the LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, and Wireless LAN, and so on.

The VSNVS block behaves as an LDO, or as a bypass switch to supply the SNVS/SRTC circuitry on the i.MX processors; V_{SNVS} may be powered from V_{IN}, or from a coin cell.

To accommodate applications powered by main supplies of voltages higher than 4.5 V and up to 5.5 V, the PF3001 incorporates a front-end LDO regulator using an external pass FET to keep the maximum regulator input voltage of the regulators at 4.5 V. Applications with an input voltage lower than 4.5 V can directly power the regulators without using the front-end LDO.

Table 3 shows a summary of the voltage regulators in the PF3001.

Table 3. PF3001 power tree

Supply	Output voltage (V)	Programming step size (mV)	Maximum load current (mA)
SW1	0.7 to 1.425 1.8 and 3.3	25 (N/A)	2750
SW2	1.5 to 1.85 2.5 to 3.3	50 variable	1250
SW3	0.9 to 1.65	50	1500
VLDO1	1.8 to 3.3	50	100
VLDO2	0.8 to 1.55	50	250
VCC_SD	2.85 to 3.3 1.8 to 1.85	150 50	100
V33	2.85 to 3.3	150	350
VLDO3	1.8 to 3.3	100	100
VLDO4	1.8 to 3.3	100	350
VSNVS	3.0	NA	1.0

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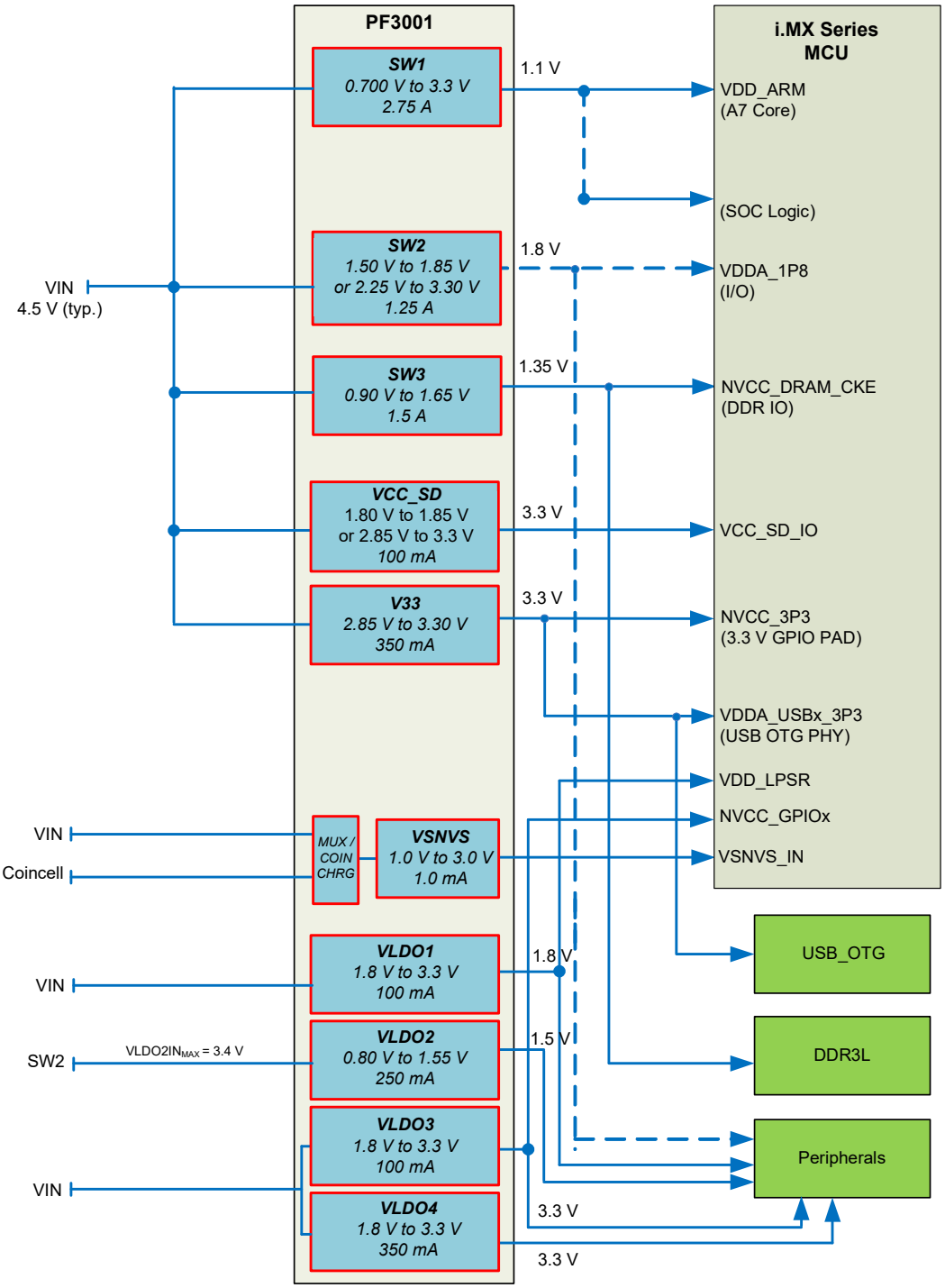


Figure 4. PF3001 typical power map

Figure 4 shows a simplified power map with various recommended options to supply the different block within the PF3001, as well as the typical application voltage domain on the i.MX Series processors. Note that each application power tree is dependent upon the system's voltage and current requirements, therefore a proper input voltage should be selected for the regulators.

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8.3 Functional description

8.3.1 Control logic and interface signals

The PF3001 is fully programmable via the I^2C interface. Additional communication is provided by direct logic interfacing including INTB, RESETBMCU, PWRON, and SD_VSEL. See Table 148 for logic levels for these pins.

8.3.1.1 PWRON

PWRON is an input signal to the IC which generates a turn-on event. A turn-on event brings the PF3001 out of OFF mode and into the ON mode. See Section 8.5 for the various modes (states) of operation of the IC. If the PWRON signal is high and VIN > UVDET, the PMIC turns on; the interrupt and sense bits, PWRONI and PWRONS respectively, are set.

8.3.1.2 RESETBMCU

RESETBMCU is an open-drain, active low output. It is deasserted 2.0 ms after the last regulator in the startup sequence is enabled. This signal can be used to bring the processor out of reset (POR), or as an indicator which all supplies have been enabled; it is only asserted during a turn-off event. The RESETBMCU signal is internal timer based and does not monitor the regulators.

8.3.1.3 INTB

INTB is an open drain, active low output. It is asserted when any fault occurs, provided the fault interrupt is unmasked. INTB is deasserted after the fault interrupt is cleared by software, which requires writing a 1 to the fault interrupt bit.

8.3.1.4 SD_VSEL

SD_VSEL is an input pin which sets the output voltage range of the VCC_SD regulator. When SD_VSEL = HIGH, the VCC_SD regulator operates in the lower output voltage range. When SD_VSEL = LOW, the VCC_SD regulator operates in the higher output voltage range. The SD_VSEL input buffer is powered by the VDDIO supply. When a valid VDDIO voltage is not present, the output of the SD_VSEL buffer defaults to a logic high thus keeping the VCC_SD regulator output in the lower voltage range.

8.3.2 Startup

The PF3001 is available in a number of pre-programmed fixed startup sequences to suit a wide variety of system configurations. See Table 4 for programming details of the different values.

Table 4. Startup configuration [1]

Registers	Pre-programmed OTP configuration						
	A1	A2	A3	A4	A5	A6	A7
Default I^2C Address	0x08	0x08	0x08	0x08	0x08	0x08	0x08
VSNVS_VOLT	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V
SW1_VOLT	1.10 V	1.10 V	1.375 V	1.375 V	1.375 V	1.4 V	1.4 V
SW1_SEQ	1	1	2	1	1	3	3
SW2_VOLT	1.8 V	1.8 V	3.3 V	3.3 V	3.15 V	3.3 V	3.3 V
SW2_SEQ	2	2	4	2	2	3	3
SW3_VOLT	1.35 V	1.2 V	1.35 V	1.5 V	1.2 V	1.2 V	1.35 V

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Table 4. Startup configuration [1] *...continued*

Registers	Pre-programmed OTP configuration						
	A1	A2	A3	A4	A5	A6	A7
SW3_SEQ	5	5	3	3	4	3	3
VLDO1_VOLT	1.8 V	1.8 V	3.3 V	1.8 V	1.8 V	3.3 V	3.3 V
VLDO1_SEQ	4	4	OFF	OFF	3	3	3
VLDO2_VOLT	1.5 V	1.5 V	1.5 V	1.2 V	1.5 V	1.5 V	1.5 V
VLDO2_SEQ	4	4	OFF	3	OFF	OFF	OFF
VLDO3_VOLT	3.3 V	3.3 V	2.5 V	1.8 V	3.1 V	1.8 V	1.8 V
VLDO3_SEQ	3	3	OFF	OFF	2	3	OFF
VLDO4_VOLT	3.3 V	3.3 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
VLDO4_SEQ	3	3	4	3	3	3	3
V33_VOLT	3.3 V	3.3 V	3.0 V	3.3 V	2.85 V	3.3 V	3.3 V
V33_SEQ	3	3	1	2	OFF	2	2
VCC_SD_VOLT	3.3 V/1.85 V	3.3 V/1.85 V	3.3 V/1.85 V	3.0 V/1.80 V	3.15 V/1.80 V	3.3 V/1.85 V	3.3 V/1.85 V
VCC_SD_SEQ	4	4	5	3	2	3	3
PU CONFIG, SEQ_ CLK_SPEED	2000 µs	2000 µs	500 µs	2000 µs	2000 µs	2000 µs	2000 µs
PU CONFIG, SWDVS_CLK	12.5 mV/µs	12.5 mV/µs	6.25 mV/µs	12.5 mV/µs	12.5 mV/µs	6.25 mV/µs	6.25 mV/µs
PU CONFIG, PWRON	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive
SW1_FREQ	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz
SW2_FREQ	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz
SW3_FREQ	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz

[1] This table specifies the default output voltage of the LDOs and SWx after start-up and/or when the LDOs and SWx are enabled. The VCC_SD voltage depends on the state of the SD_VSEL pin.

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8.3.3 Startup timing diagram

Figure 5 shows the startup timing of the regulators as determined by their OTP sequence. The trimmed 32 kHz clock controls all the startup timing.

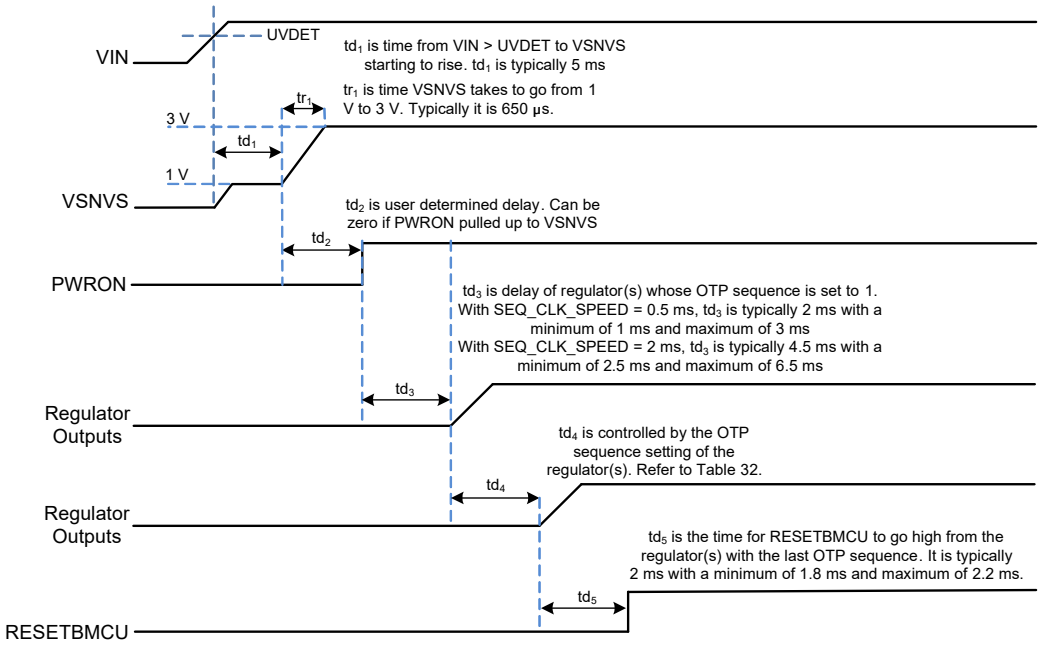


Figure 5. Startup timing diagram

8.3.4 16 MHz and 32 kHz clocks

The PF3001 incorporates two clocks: a trimmed 16 MHz RC oscillator and an untrimmed 32 kHz RC oscillator. The 32 kHz untrimmed clock is only used in the following conditions:

- V_{IN} < UVDET
- All regulators are in PFM Switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During startup, V_{IN} > UVDET

When the 16 MHz is active in the On mode, the debounce times are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and PWRONI interrupts, which are referenced to the 32 kHz untrimmed clock. Switching frequency of the switching regulators is derived from the trimmed 16 MHz clock.

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16 MHz clock, the user may add an offset as small as ±3.0 % of the nominal frequency. Contact an NXP representative for more information.

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8.3.5 Optional front-end input LDO regulator

8.3.5.1 LDO regulator description

This section describes the optional front-end LDO regulator provided by the PF3001 in order to facilitate the operation with supply voltages higher than 4.5 V and up to 5.5 V.

For non-battery operated applications, when the input supply voltage exceeds 4.5 V, the front-end LDO can be activated by populating the external PMOS pass FET MP1 in Figure 6 and connecting the VPWR pin to the main supply. Under this condition, the LDO control block self-starts with a local bandgap reference. When the VIN pin reaches UVDET rising threshold, the reference is switched to the main trimmed bandgap reference to maintain the required VIN accuracy. In applications using an input supply voltage of 4.5 V or lower, the PMOS pass FET should not be populated, the VPWR pin should be grounded externally, and the VIN pin should be used instead as the main supply input pin. The input pins of the switching regulators should always be connected to the VIN net.

The main components of the LDO regulator are an external power P-channel MOSFET and an internal differential error amplifier. One input of the amplifier monitors a fraction of the output voltage at VIN determined by the resistor ratio of R1 and R2 as shown in Figure 6. The second input to the differential amplifier is from a stable bandgap voltage reference. If the output voltage rises too high relative to the reference voltage, the gate voltage of the power FET is changed to maintain a constant output voltage.

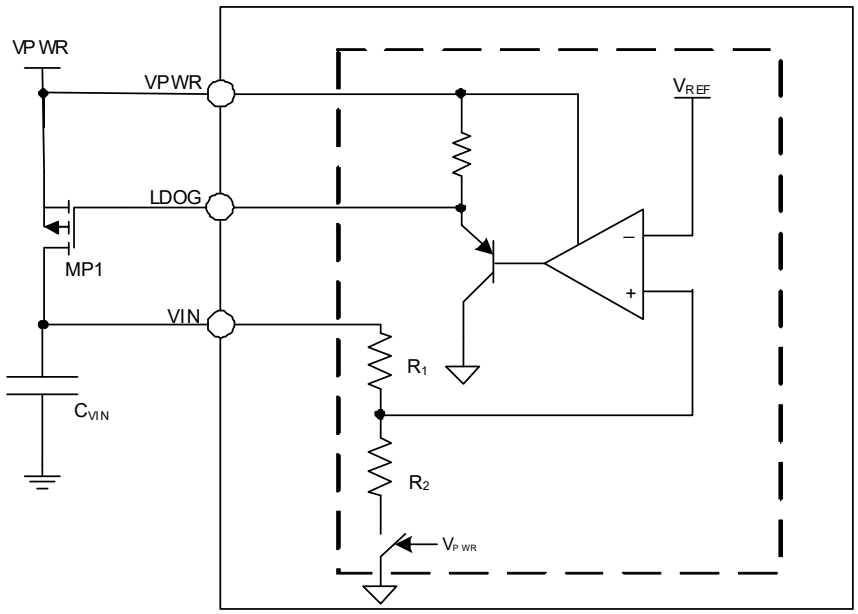


Figure 6. Front-end LDO block diagram

8.3.5.2 Undervoltage/short-circuit and overvoltage detection

Short-circuit to GND at VIN is detected using an under voltage monitor at VIN which senses excessive droop on the VIN line and consequently turns off (disable) the external PMOS pass FET. Overvoltage at VPWR is detected if VPWR exceeds the V_{PWROV} threshold (typically 6.0 V). Upon the detection of an overvoltage event an interrupt is generated and bit 2 is set in INTSTAT3 register. The INTB pin is pulled low if the VPWROVM mask bit is cleared. The interrupt is filtered using a 122 µs debouncing circuit. The VPWROV interrupt is not asserted if the overvoltage event occurs during start up. The VPWROVS bit can be read using I^2C to detect an overvoltage condition.

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8.3.5.3 External components

Table 5 lists the typical component values for the general purpose LDO regulators.

Table 5. Input LDO external components

Component	Value
Minimum output capacitor on VIN rail	100 µF[1]
MP1	Fairchild FDMA908PZ, Vishay SiA447DJ, or comparable

[1] Use X5R/X7R ceramic capacitors with a voltage rating at least two times the nominal voltage. The 100 µF capacitance is the total capacitance on the VIN rail including the capacitance at the various regulator inputs. For example, 2 x 22 µF capacitors can be used along with 10 µF capacitors at all the SWx and LDOx inputs to achieve a total of 100 µF capacitance.

8.3.6 Internal core voltages

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VCOREREF. VCOREDIG is a 1.5 V regulator powering all the digital logic in the PF3001. VCOREDIG is regulated at 1.28 V in off and coin cell modes. The VCORE supply is used to bias internal analog rails. No external DC loading is allowed on VCORE, VCOREDIG, or VCOREREF. VCOREDIG is kept powered as long as there is a valid supply and/or valid coin cell.

8.3.7 Buck regulators

The PF3001 integrates three independent buck regulators: SW1, SW2, and SW3. Each regulator has associated registers controlling its output voltage during on mode. After boot up, contents of the SWxVOLT[4:0] register can be set through I^2C to set the output voltage during On mode.

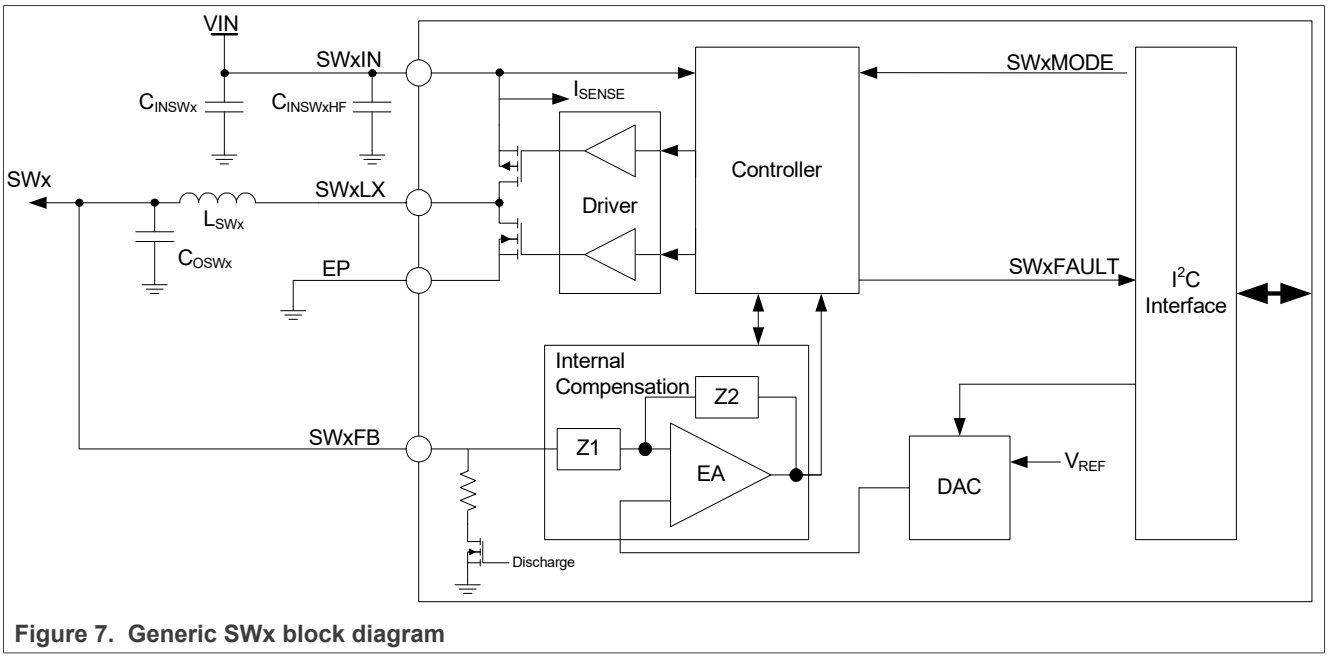


Figure 7. Generic SWx block diagram

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Table 6. SWx regulators external components

Components	Description	Values
CINSWx	SWx input capacitor	10 µF
CINSWxHF	SWx decoupling input capacitor	0.1 µF
COSWx	SWx output capacitor	2 x 22 µF (10 V or higher voltage rated capacitors) or 3 x 22 µF (6.3 V rated capacitors)
LSWx	SWx inductor	1.5 µH

Note: *Use X5R or X7R capacitors with voltage rating at least two times the nominal voltage.*

8.3.7.1 Switching modes

The buck regulators can operate in different Switching modes. Changing between switching modes can occur by I^2C programming. Available Switching modes for buck regulators are presented in Table 7.

Table 7. Switching mode description

Mode	Description
OFF	The regulator is switched off and the output voltage is discharged using an internal resistor
PFM	In this mode, the regulator operates in forced PFM mode. The main error amplifier is turned off and a hysteretic comparator is used to regulate output voltage. Use this mode for load currents less than 50 mA.
PWM	In this mode, the regulator operates in forced PWM mode.
APS	In this mode, the regulator operates in pulse skipping mode at light loads and switches over to PWM modes for heavier load conditions. This is the default mode in which the regulators power up during a turn-on event.

During soft-start of the buck regulators, the controller transitions through the PFM, APS, and PWM Switching modes. 3.0 ms after the output voltage reaches regulation, the controller transitions to the selected Switching mode. Depending on the particular switching mode selected, additional ripple may be observed on the output voltage rail as the controller transitions between switching modes. The operating mode of the regulator in On mode is controlled using the SWxMODE[3:0] bits associated with each regulator. Table 8 summarizes the Buck regulator programmability for Normal mode.

Table 8. Regulator mode control

SWxMODE[3:0]	Normal mode
0000	Off
0001	PWM
0011	PFM
1000 (default)	APS

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8.3.7.2 Dynamic voltage scaling

To reduce overall power consumption, processor core voltages can be varied depending on the mode or activity level of the processor.

Normal operation: The output voltage is selected by I^2C bits SW1[4:0] for SW1 and SW2[2:0] for SW2, and SW3[3:0] for SW3. A voltage transition initiated by I^2C is governed by the DVS stepping rate which is 25 mV per step each 4.0 µs.

The regulators have a strong sourcing and sinking capability in PWM mode, therefore the fastest rising and falling slopes are determined by the regulator in PWM mode. However, if the regulators are programmed in PFM or APS mode during a DVS transition, the falling slope can be influenced by the load. Additionally, as the current capability in PFM mode is reduced, controlled DVS transitions in PFM mode could be affected. Critically timed DVS transitions are best assured with PWM mode operation.

Figure 8 shows the general behavior for the regulators when initiated with I^2C programming. During the DVS period the overcurrent condition on the regulator should be masked.

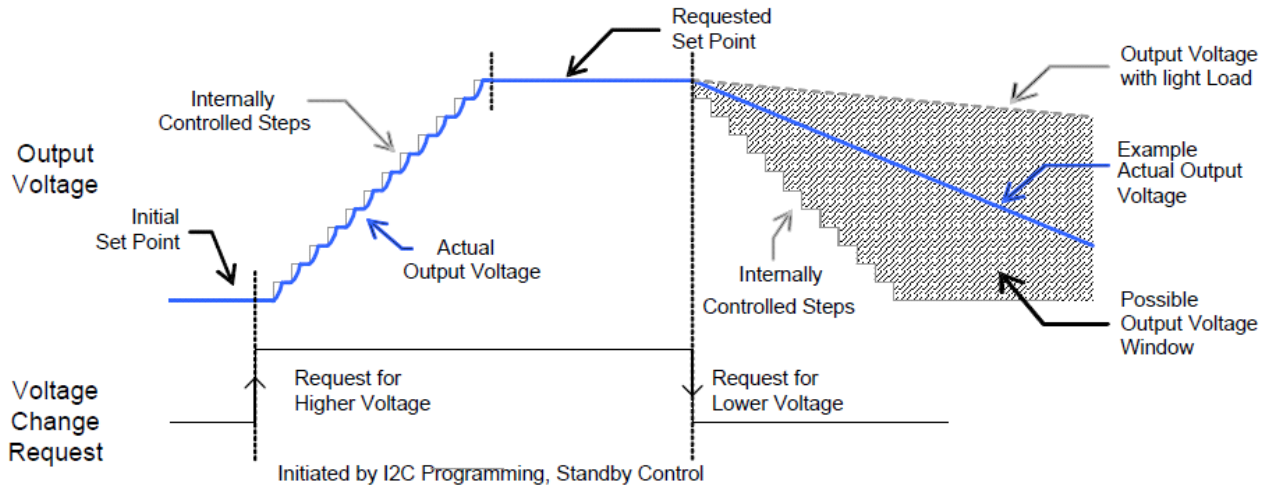


Figure 8. Voltage stepping with fixed DVS

8.3.7.3 Regulator phase clock

The SWxPHASE[1:0] bits select the phase of the regulator clock as shown in Table 9. By default, each regulator is initialized at 90 °C out of phase with respect to each other. For example, SW1 is set to 0 °C, SW2 is set to 90 °C, and SW3 is set to 180 °C by default at power up.

Table 9. Regulator phase clock selection

SWxPHASE[1:0]	Phase of clock sent to regulator (degrees)
00	0
01	90
10	180
11	270

The SWxFREQ[1:0] register is used to set the desired switching frequency for each one of the buck regulators. Table 11 shows the selectable options for SWxFREQ[1:0]. For each frequency, all phases are available, this allows regulators operating at different frequencies to have different relative switching phases. However, not

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all combinations are practical. For example, 2.0 MHz, 90 °C and 4.0 MHz, 180 °C are the same in terms of phasing. Table 10 shows the optimum phasing when using more than one switching frequency.

Table 10. Optimum phasing

Frequencies	Optimum phasing
1.0 MHz 2.0 MHz	0 °C 180 °C
1.0 MHz 4.0 MHz	0 °C 180 °C
2.0 MHz 4.0 MHz	0 °C 180 °C
1.0 MHz 2.0 MHz 4.0 MHz	0 °C 90 °C 90 °C

Table 11. Regulator frequency configuration

SWxFREQ[1:0]	Frequency
00	1.0 MHz
01	2.0 MHz (default)
10	4.0 MHz
11	Reserved

8.3.7.4 SW1

SW1 is a 2.75 A buck regulator. The SW1 output voltage is programmable from 1.5 V to 3.3 V. In this configuration, the SW1LX pins are connected together to a single inductor, providing up to 2.75 A current capability for high current applications. The feedback and all other controls are accomplished using the SW1FB pin.

8.3.7.5 SW1 setup and control registers

SW1 output voltages are programmable from 0.7 V to 1.425 V in steps of 25 mV. They can additionally be programmed at 1.8 V or 3.3 V. The output voltage set point is independently programmed for Normal mode by setting the SW1[4:0] bits respectively. Table 12 shows the output voltage coding.

Table 12. SW1 output voltage configuration

Set Point	SW1[4:0]	SW1x output (V)
0	00000	0.700
1	00001	0.725
2	00010	0.750
3	00011	0.775
4	00100	0.800
5	00101	0.825
6	00110	0.850

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Table 12. SW1 output voltage configuration*...continued*

Set Point	SW1[4:0]	SW1x output (V)
7	00111	0.875
8	01000	0.900
9	01001	0.925
10	01010	0.950
11	01011	0.975
12	01100	1.000
13	01101	1.025
14	01110	1.050
15	01111	1.075
16	10000	1.100
17	10001	1.125
18	10010	1.150
19	10011	1.175
20	10100	1.200
21	10101	1.225
22	10110	1.250
23	10111	1.275
24	11000	1.300
25	11001	1.325
26	11010	1.350
27	11011	1.375
28	11100	1.400
29	11101	1.425
30	11110	1.800
31	11111	3.300

Table 13 provides a list of registers used to configure and operate the SW1 regulator.

Table 13. SW1 register summary

Register	Address	Output
SW1VOLT	0x20	SW1 output voltage set point in normal operation
SW1MODE	0x23	SW1 switching mode selector register
SW1CONF	0x24	SW1 phase and frequency configuration

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8.3.7.6 SW2 setup and control registers

SW2 is a single phase, 1.25 A rated buck regulator. The SW2 output voltage is programmable from 1.5 V to 1.85 V in 50 mV steps if the CTL_SW2_HL bit is low or from 2.5 V to 3.3 V in 150 mV steps, if the bit CTL_SW2_HL is set high. This internal bit CTL_SW2_HL is decided by the SW2 startup voltage in the startup sequence. During normal operation, output voltage of the SW2 regulator can be changed through I^2C only within the range set by the CTL_SW2_HL bit. The output voltage set point is independently programmed for Normal mode by setting the SW2[2:0] bits, respectively. Table 14 shows the output voltage coding valid for SW2.

Table 14. SW2 output voltage configuration

Low output voltage range (CTL_SW2_HL= 0)		High output voltage range (CTL_SW2_HL=1)	
SW2[2:0]	SW2 output	SW2[2:0]	SW2 output
000	1.500	000	2.500
001	1.550	001	2.800
010	1.600	010	2.850
011	1.650	011	3.000
100	1.700	100	3.100
101	1.750	101	3.150
110	1.800	110	3.200
111	1.850	111	3.300

Setup and control of SW2 is done through the I^2C registers listed in Table 15.

Table 15. SW2 register summary

Register	Address	Description
SW2VOLT	0x35	SW2 output voltage set point on normal operation
SW2MODE	0x38	SW2 switching mode selector register
SW2CONF	0x39	SW2 phase, frequency, and ILIM configuration

8.3.7.7 SW3 setup and control registers

SW3 output voltage is programmable from 0.90 V to 1.65 V in 50 mV steps to support different types of DDR memory as listed in Table 16.

Table 16. SW3 output voltage configuration

SW3[3:0]	SW3 output (V)	SW3[3:0]	SW3 output (V)
0000	0.90	1000	1.30
0001	0.95	1001	1.35
0010	1.00	1010	1.40
0011	1.05	1011	1.45
0100	1.10	1100	1.50
0101	1.15	1101	1.55
0110	1.20	1110	1.60
0111	1.25	1111	1.65

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Table 17 provides a list of registers used to configure and operate SW3.

Table 17. SW3 register summary

Register	Address	Output
SW3VOLT	0x3C	SW3 output voltage set point on normal operation
SW3MODE	0x3F	SW3 switching mode selector register
SW3CONF	0x40	SW3 phase, frequency, and ILIM configuration

8.3.7.8 LDO regulators description

This section describes the LDO regulators provided by the PF3001. All regulators use the main bandgap as reference. When a regulator is disabled, the output discharges through an internal pull-down resistor.

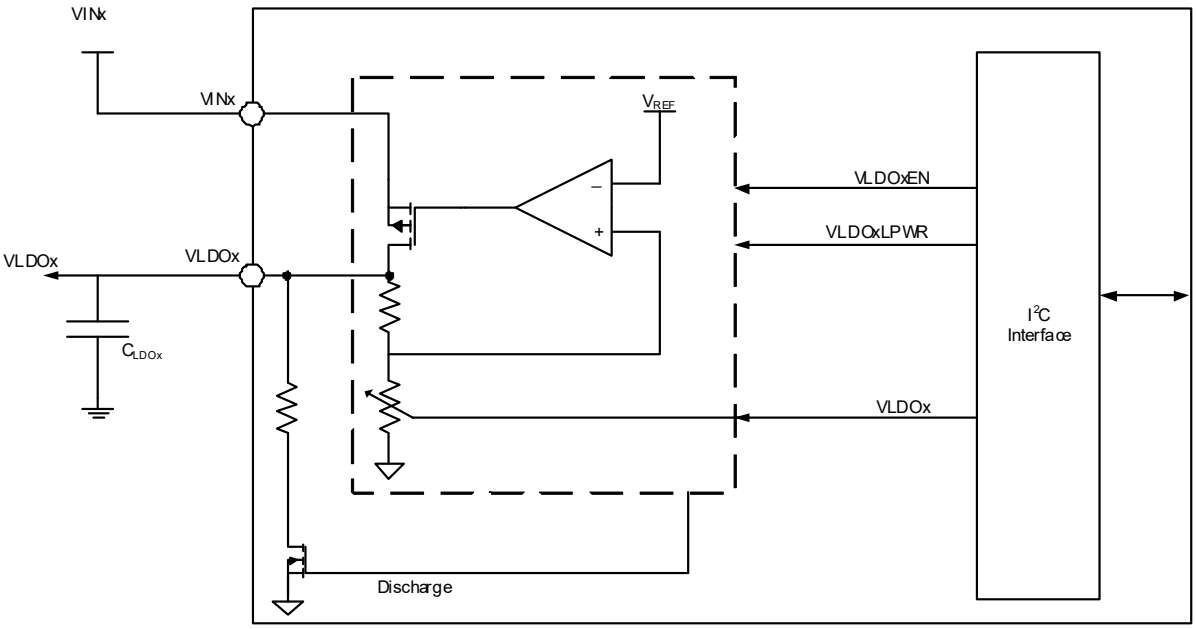


Figure 9. General LDO block diagram

8.3.7.8.1 External components

Table 18 lists the typical component values for the general purpose LDO regulators.

Table 18. LDO external components

Regulator	Output capacitor (µF)[1]
VLDO1	2.2
VLDO2	4.7
VLDO3	2.2
VLDO4	4.7
V33	4.7
VCC_SD	2.2

[1] Use X5R/X7R ceramic capacitors.

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8.3.7.8.2 Current limit protection

All the LDO regulators in the PF3001 have current limit protection. In the event of an overload condition, the regulators transitions from a voltage regulator to a current regulator which regulates output current per the current limit threshold.

Additionally, if the REGSCPEN bit in Table 79 is set, the LDO is turned off if the current limit event lasts for more than 8.0 ms. The LDO is disabled by resetting its VLDOxEN bit, while at the same time, an interrupt VLDOxFAULTI is generated to flag the fault to the system processor. The VLDOxFAULTI interrupt is maskable through the VLDOxFAULTM mask bit. By default, the REGSCPEN is not set; therefore, at startup none of the regulators is disabled if an overloaded condition occurs. A fault interrupt, VLDOxFAULTI, is generated in an overload condition regardless of the state of the REGSCPEN bit.

8.3.7.8.3 LDO voltage control

Each LDO is fully controlled through its respective VLDOxCTL register. This register enables the user to set the LDO output voltage according to Table 19 for VLDO1 and VLDO2; and uses the voltage set point on Table 20 for VLDO3 and VLDO4. Table 21 lists the voltage set points for the V33 LDO and Table 22 provides the output voltage set points for the VCC_SD LDO, based on SD_VSEL control signal.

Table 19. VLDO1, VLDO2 output voltage configuration

VLDO1[3:0] VLDO2[3:0]	VLDO1 output (V)	VLDO2 output (V)
0000	1.80	0.80
0001	1.90	0.85
0010	2.00	0.90
0011	2.10	0.95
0100	2.20	1.00
0101	2.30	1.05
0110	2.40	1.10
0111	2.50	1.15
1000	2.60	1.20
1001	2.70	1.25
1010	2.80	1.30
1011	2.90	1.35
1100	3.00	1.40
1101	3.10	1.45
1110	3.20	1.50
1111	3.30	1.55

Table 20. VLDO3, VLDO4 output voltage configuration

VLDO3[3:0] VLDO4[3:0]	VLDO3 or VLDO4 output (V)
0000	1.80
0001	1.90
0010	2.00

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Table 20. VLDO3, VLDO4 output voltage configuration*...continued*

VLDO3[3:0] VLDO4[3:0]	VLDO3 or VLDO4 output (V)
0011	2.10
0100	2.20
0101	2.30
0110	2.40
0111	2.50
1000	2.60
1001	2.70
1010	2.80
1011	2.90
1100	3.00
1101	3.10
1110	3.20
1111	3.30

Table 21. V33 output voltage configuration

V33[1:0]	V33 output (V)
00	2.85
01	3.00
10	3.15
11	3.30

Table 22. VCC_SD output voltage configuration

VCC_SD[1:0]	VCC_SD output (V) VSD_VSEL= 0	VCC_SD output (V) VSD_VSEL= 1
00	2.85	1.80
01	3.00	1.80
10	3.15	1.80
11	3.30	1.85

Along with the output voltage configuration, the LDOs can be enabled or disabled at anytime during Normal mode operation. Each regulator has associated I^2C bits for this. Table 23 presents a summary of all valid combinations of the control bits on VLDOxCTL register and the expected behavior of the LDO output.

Table 23. LDO control

VLDOxEN/ V33EN/ VCC_SDEN	VLDOxOUT/ V33OUT/ VCC_SDOUT
0	Off
1	On

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8.3.7.9 VSNVS LDO/switch

VSNVS powers the low power, SNVS/RTC domain on the processor. It derives its power from either VIN, or coin cell, and cannot be disabled. When powered by both, V_{IN} takes precedence when above the appropriate comparator threshold. When powered by V_{IN}, VSNVS is an LDO capable of supplying 3.0 V. When powered by coin cell, the VSNVS output tracks the coin cell voltage by means of a

switch, whose maximum resistance is 100 Ω. In this case, the V_{SNVS} voltage is simply the coin cell voltage minus the voltage drop across the switch, which is 100 mV at a rated maximum load current of 1000 µA.

When the coin cell is applied for the first time, VSNVS outputs 1.0 V. Only when V_{IN} is applied thereafter does V_{SNVS} transition to its default value, or programmed value if different. Upon subsequent removal of V_{IN}, with the coin cell attached, V_{SNVS} changes configuration from an LDO to a switch, provided certain conditions are met as described in Table 24.

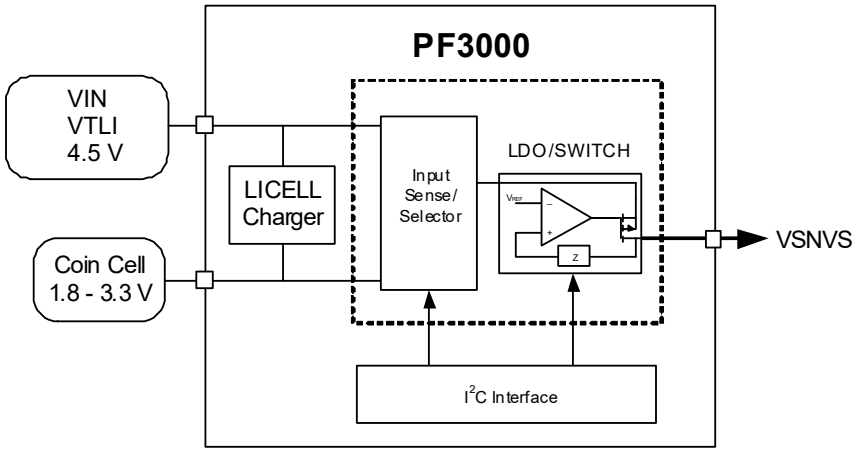


Figure 10. VSNVS supply switch architecture

Table 24 provides a summary of the V_{SNVS} operation at different input voltage V_{IN} and with or without coin cell connected to the system.

Table 24. SNVS Modes of Operation

VSNVSVOLT[2:0]	VIN	MODE
110	> VTH1	VIN LDO 3.0 V
110	< VTL1	Coin cell switch

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8.3.7.9.1 VSNVS control

The V_{SNVS} output level is configured through the VSNVSVOLT[2:0] bits on VSNVSCTL register as shown Table 25.

Table 25. Register VSNVSCTL - ADDR 0x6B

Name	Bit #	R/W	Default	Description
VSNVSVOLT	2:0	R/W	0b000	Configures VSNVS output voltage.[1] 000 = RSVD 001 = RSVD 010 = RSVD 011 = RSVD 100 = RSVD 101 = RSVD 110 = 3.0 V (default) 111 = RSVD
Unused	7:3	–	0b00000	Unused

[1] Only valid when a valid input voltage is present.

8.3.7.9.2 VSNVS external components

Table 26. VSNVS external components

Capacitor	Value (µF)
VSNVS	0.47

8.3.7.9.3 Coin cell battery backup

The LICELL pin provides for a connection of a coin cell backup battery or a “super” capacitor. If the voltage at VIN goes below the VIN threshold (VTL1), contact-bounced, or removed, the coin cell maintained logic is powered by the voltage applied to LICELL. The supply for internal logic and the VSNVS rail switches over to the LICELL pin when VIN goes below VTL1, even in the absence of a voltage at the LICELL pin, resulting in clearing of memory and turning off VSNVS. Applications concerned about this behavior can tie the LICELL pin to any system voltage between 1.8 V and 3.0 V. A 0.47 µF capacitor should be placed from LICELL to ground under all circumstances.

8.3.7.9.4 Coin cell charger control

The coin cell charger circuit functions as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The coin cell charger is enabled via the COINCHEN bit while the coin cell voltage is programmable through the VCOIN[2:0] bits on register COINCTL on Table 27. The coin cell charger voltage is programmable. In the ON state, the charger current is fixed at ICOINHI. In the OFF state, coin cell charging is not available as the main battery could be depleted unnecessarily. The coin cell charging stops when V_{IN} is below UVDET.

Table 27. Coin cell charger voltage

VCOIN[2:0]	V_{COIN} (V)[1]
000	2.50
001	2.70
010	2.80

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Table 27. Coin cell charger voltage*...continued*

VCOIN[2:0]	V_{COIN} (V)[1]
011	2.90
100	3.00
101	3.10
110	3.20
111	3.30

[1] Coin cell voltages selected based on the type of LICELL used on the system.

Table 28. Register COINCTL – ADDR 0x1A

Name	Bit #	R/W	Default	Description
VCOIN	2:0	R/W	0x00	Coin cell charger output voltage selection. See Table 27 for all options selectable through these bits.
COINCHEN	3	R/W	0x00	Enable or disable the coin cell charger
Unused	7:4	–	0x00	Unused

8.3.7.9.5 External components

Table 29. Coin cell charger external components

Component	Value	Units
LICELL bypass capacitor	100	nF

8.4 Power dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in Table 124. To optimize the thermal management and to avoid overheating, the PF3001 provides thermal protection. An internal comparator monitors the die temperature. Interrupts THERM110, THERM120, THERM125, and THERM130 is generated when the respective thresholds specified in Table 30 are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry shuts down the PF3001. This thermal protection acts above the thermal protection threshold listed in Table 30. To avoid any unwanted power downs resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured such that this protection is not tripped under normal conditions.

Table 30. Thermal protection thresholds

Parameter	Min.	Typ.	Max.	Units
Thermal 110 °C threshold (THERM110)	100	110	120	°C
Thermal 120 °C threshold (THERM120)	110	120	130	°C
Thermal 125 °C threshold (THERM125)	115	125	135	°C
Thermal 130 °C threshold (THERM130)	120	130	140	°C
Thermal warning hysteresis	2.0	–	4.0	°C

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Table 30. Thermal protection thresholds*...continued*

Parameter	Min.	Typ.	Max.	Units
Thermal protection threshold	130	140	150	°C

8.5 Modes of operation

8.5.1 State diagram

The operation of the PF3001 can be reduced to three states, or modes: On, Off, and Coin Cell. Figure 11 shows the state diagram of the PF3001, along with the conditions to enter and exit from each state.

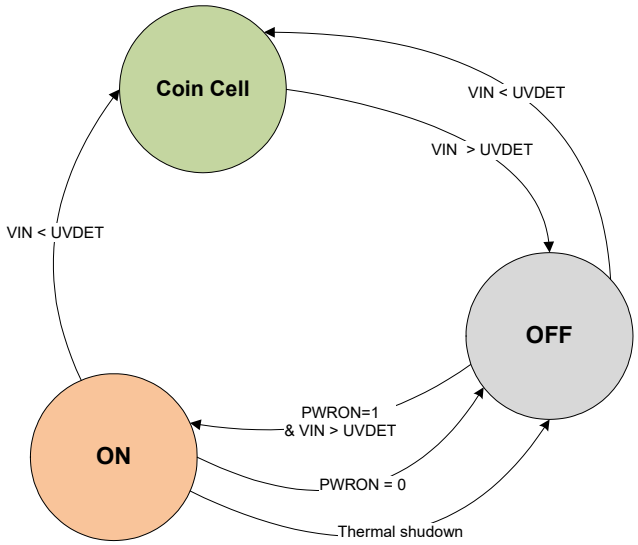


Figure 11. State diagram

To complement the state diagram in Figure 11, a description of the states is provided in following sections.

Note: *V_{IN} must exceed the rising UVDET threshold to allow a power up. See Table 150 for the UVDET thresholds. Additionally, I^2C control is not possible in the coin cell mode and the interrupt signal, INTB, is only active in the on state.*

8.5.1.1 On mode

The PF3001 enters the on mode after a turn-on event. RESETBMCU is deasserted, and pulled high via an external pull-up resistor, in this mode of operation. To enter the on mode, VIN voltage must surpass the rising UVDET threshold and PWRON must be asserted. From the on mode, when the voltage at VIN drops below the undervoltage falling threshold, UVDET, the state machine transitions to the coin cell mode.

8.5.1.2 Off mode

The PF3001 enters the Off mode after a turn-off event. Only VCOREDIG and VSNVS are powered in the mode of operation. To exit the off mode, a valid turn-on event is required. RESETBMCU is asserted, LOW, in this mode. Turn off events can be achieved using the PWRON pin, thermal protection, as described by the following.

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8.5.1.3 PWRON pin

The PWRON pin is used to power off the PF3001. The PWRON pin powers off the PMIC under conditions where the PWRON pin is low.

8.5.1.4 Thermal protection

If the die temperature surpasses a given threshold, the thermal protection circuit powers off the PMIC to avoid damage. A turn-on event does not power on the PMIC while it is in thermal protection. The part remains in off mode until the die temperature decreases below a given threshold. See Section 8.4 for more information.

8.5.1.5 Coin cell mode

In the coin cell state, the coin cell is the only valid power source to the PMIC. No turn-on event is accepted in the coin cell state. Transition to the off state requires V_{IN} surpasses the UVDET threshold. RESETBMCU is held low in this mode. If the coin cell is depleted, a complete system reset occurs. At the next application of power and the detection of a turn-on event, the system re-initializes with all I^2C bits including, those that reset on COINPORB are restored to their default states.

8.5.2 State machine flow summary

Table 31 provides a summary matrix of the PF3001 flow diagram to show the conditions needed to transition from one state to another.

Table 31. State machine flow summary

STATE		Next state		
		Off	Coin cell	On
Initial State	Off	X	V_{IN} < UVDET	PWRON = 1 and V_{IN} > UVDET
	Coin cell	V_{IN} > UVDET	X	X
	On	Thermal Shutdown	V_{IN} < UVDET	X
		PWRON = 0		

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8.5.3 Performance characteristics curves

V_{IN} = 3.6 V, $SW1_{OUT}$ = 1.0 V, $SW2_{OUT}$ = 1.8 V, $SW3_{OUT}$ = 1.0 V, Switching frequency = 2.0 MHz, Mode = APS; $LDO1_{OUT}$ = 1.8 V, $LDO2_{OUT}$ = 1.0 V, $LDO3_{OUT}$ = 1.8 V, $LDO4_{OUT}$ = 1.8 V, $V33_{OUT}$ = 3.3 V, VCC_SD_{OUT} = 3.3 V, unless otherwise noted

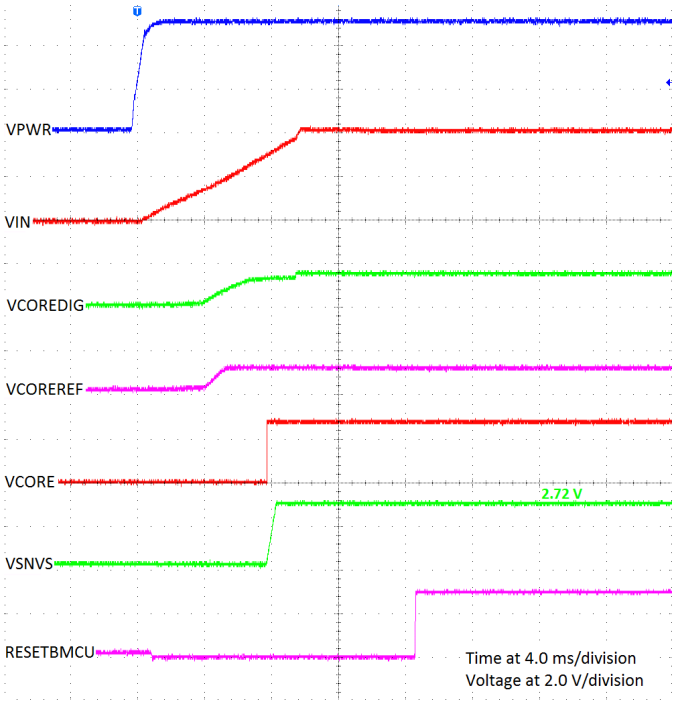


Figure 12. Startup sequence

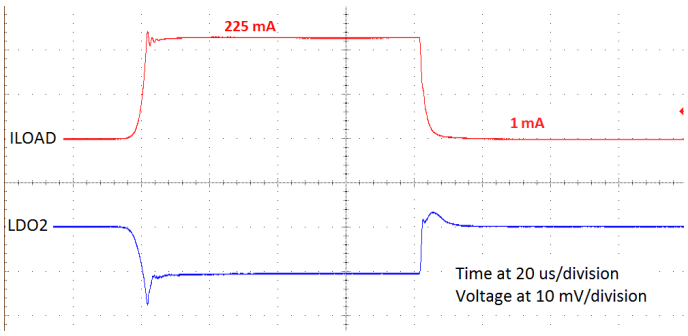


Figure 13. Load transient response – LDO2

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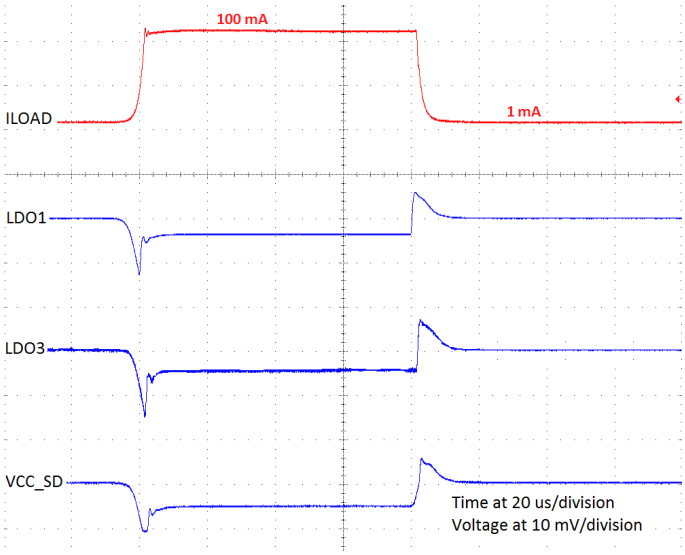


Figure 14. Load transient response – LDO1, LDO3, and VCC_SD

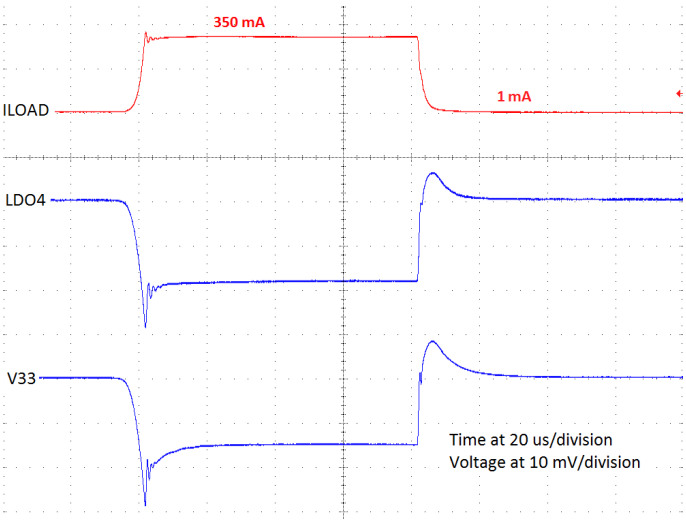


Figure 15. Load transient response – LDO4 and V33

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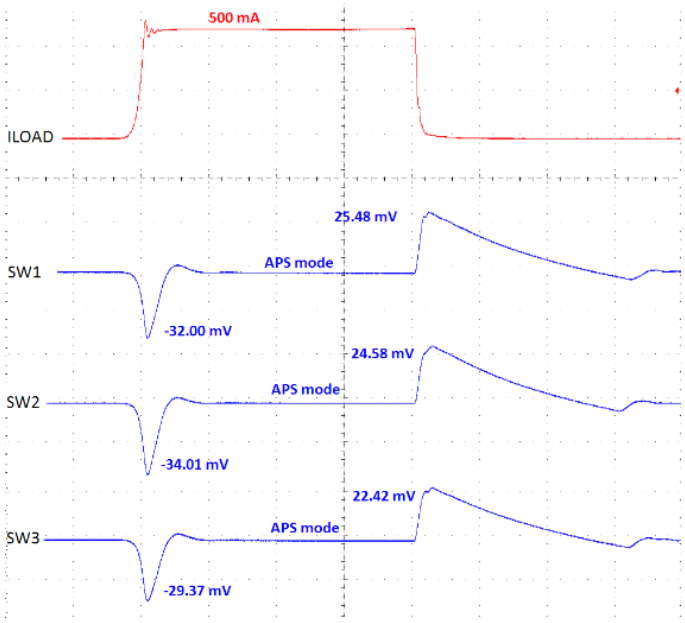


Figure 16. Load transient response – buck regulators

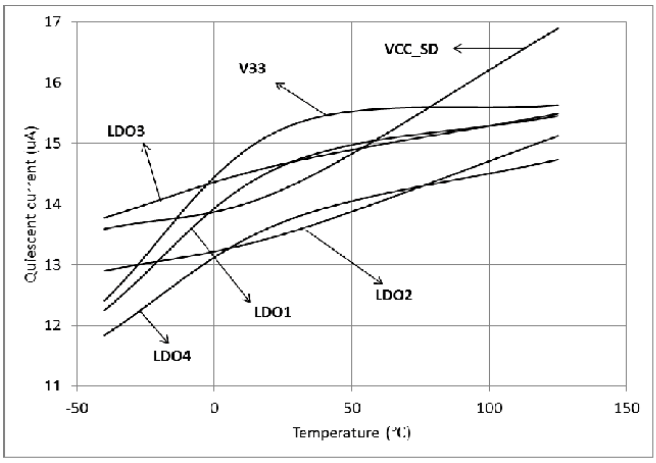


Figure 17. Quiescent current – LDOs

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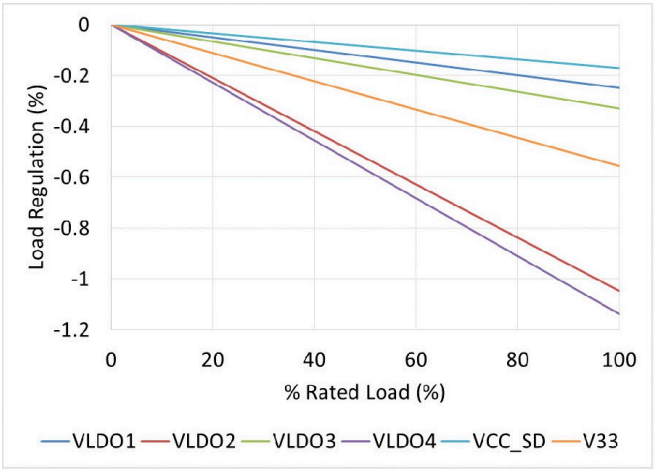


Figure 18. Load regulation – LDOs

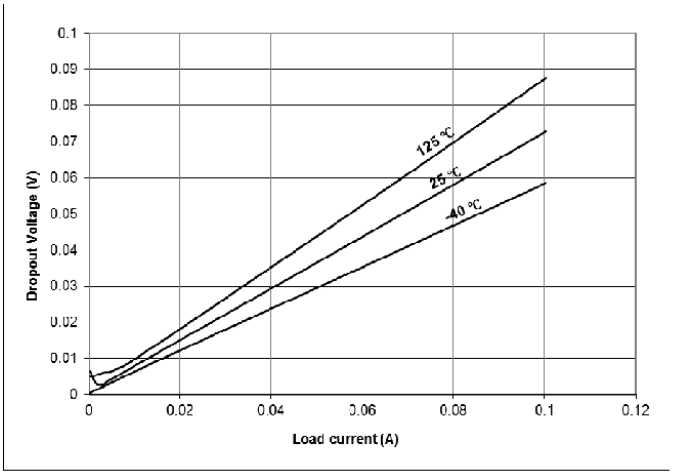


Figure 19. Dropout voltage – VLDO1, VLDO3, VCC_SD - V_{OUT} = 3.3 V

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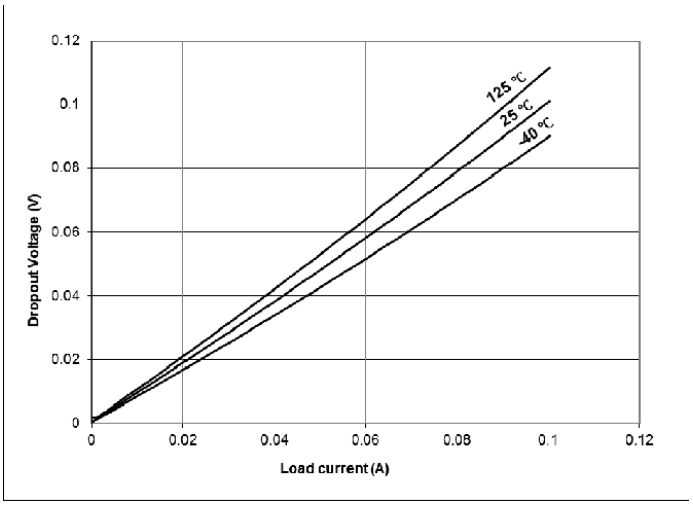


Figure 20. Dropout voltage – VLDO1, VLDO3,VCC_SD - V_{OUT} = 1.8 V

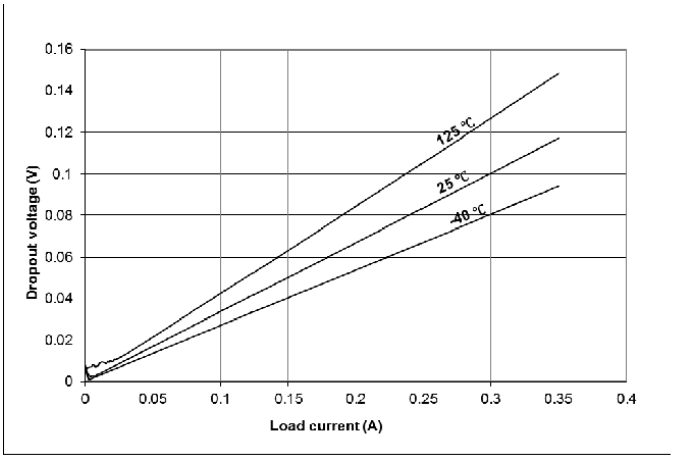


Figure 21. Dropout voltage – VLDO4, V33 - V_{OUT} = 3.3 V

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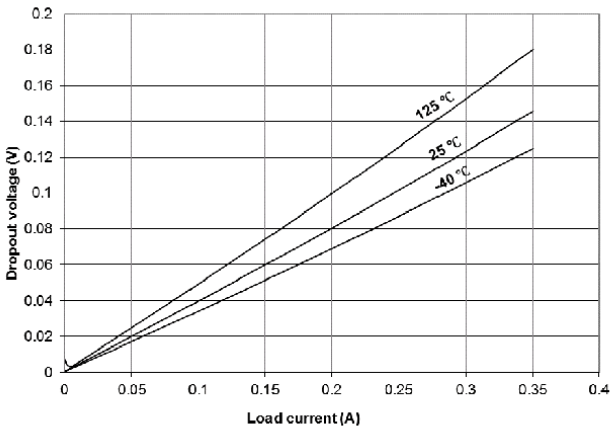


Figure 22. Dropout voltage – VLDO4 - V_{OUT} = 1.8 V

8.6 Control interface I^2C block description

The PF3001 contains an I^2C interface port which allows access by a processor, or any I^2C controller, to the register set. Via these registers the resources of the IC can be controlled. The registers also provide status information about how the IC is operating.

8.6.1 I^2C device ID

I^2C interface protocol requires a device ID for addressing the target IC on a multi-device bus. The I^2C address of the PF3001 is set to 0x08.

8.6.2 I^2C operation

The I^2C mode of the interface is implemented generally following the fast mode definition which supports up to 400 kbits/s operation (exceptions to the standard are noted to be 7-bit only addressing and no support for General Call addressing.) Timing diagrams, electrical specifications, and further details can be found in the I^2C specification, which is available for download.

I^2C read operations are also performed in byte increments separated by an ACK. Read operations also begin with the MSB and each byte is sent out unless a STOP command or NACK is received prior to completion.

The following examples show how to write and read data to and from the IC. The host initiates and terminates all communication. The host sends a controller command packet after driving the start condition. The device responds to the host if the controller command packet contains the corresponding follower address. In the following examples, the device is always shown responding with an ACK to transmissions from the host. If at any time a NACK is received, the host should terminate the current transaction and retry the transaction.

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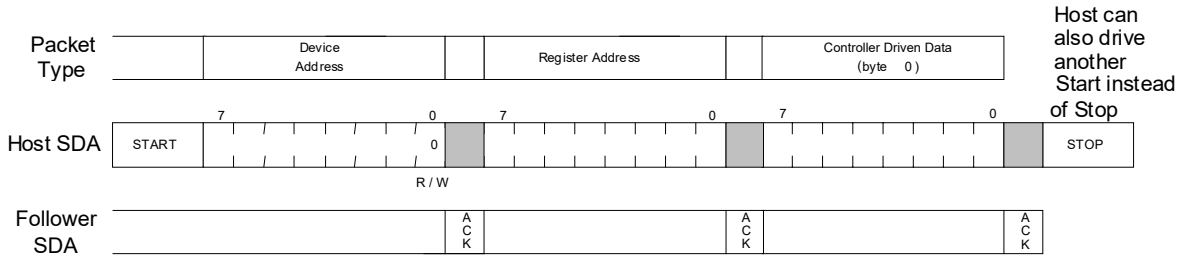


Figure 23. I²C write example

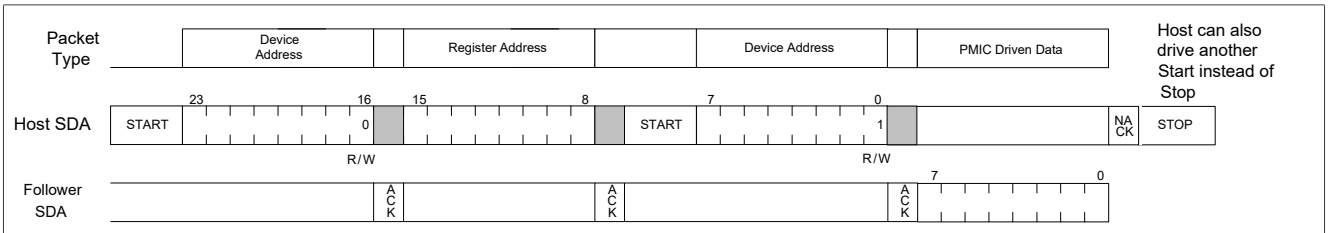


Figure 24. I²C read example

8.6.3 Interrupt handling

The system is informed about important events based on interrupts. Unmasked interrupt events are signaled to the processor by driving the INTB pin low. Each interrupt is latched so even if the interrupt source becomes inactive, the interrupt remains set until cleared. Each interrupt can be cleared by writing a 1 to the appropriate bit in the Interrupt Status register; this causes the INTB pin to go high. If there are multiple interrupt bits set the INTB pin remains low until all are either masked or cleared. If a new interrupt occurs while the processor clears an existing interrupt bit, the INTB pin remains low.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the INTB pin does not go low. A masked interrupt can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the IC. The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the INTB pin goes low after unmasking.

The sense registers contain status and input sense bits so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable. Interrupts generated by external events are debounced; therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are documented in the INT summary Table 32. Due to the asynchronous nature of the debounce timer, the effective debounce time can vary slightly.

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8.6.4 Interrupt bit summary

Table 32 summarizes all interrupt, mask, and sense bits associated with INTB control. For more detailed behavioral descriptions, refer to the related chapters.

Table 32. Interrupt, Mask, and Sense Bits

Interrupt	Mask	Sense	Purpose	Trigger	Debounce time (ms)
LOWVINI	LOWVINM	LOWVINS	Low input voltage detect Sense is 1 if below 2.70 V threshold	H to L	3.9[1]
PWRONI	PWRONM	PWRONS	Power on button event	H to L	31.25[1]
			Sense is 1 if PWRON is high	L to H	31.25
THERM110	THERM110M	THERM110S	Thermal 110 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM120	THERM120M	THERM120S	Thermal 120 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM125	THERM125M	THERM125S	Thermal 125 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM130	THERM130M	THERM130S	Thermal 130 °C threshold Sense is 1 if above threshold	Dual	3.9
SW1FAULTI	SW1FAULTM	SW1FAULTS	Regulator 1 overcurrent limit Sense is 1 if above current limit	L to H	8.0
SW2FAULTI	SW2FAULTM	SW2FAULTS	Regulator 2 overcurrent limit Sense is 1 if above current limit	L to H	8.0
SW3FAULTI	SW3FAULTM	SW3FAULTS	Regulator 3 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VLDO1FAULTI	VLDO1FAULTM	VLDO1FAULTS	VLDO1 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VLDO2FAULTI	VLDO2FAULTM	VLDO2FAULTS	VLDO2 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VCC_SDFAULTI	VCC_SDFAULTM	VCC_SDFAULTS	VCC_SD overcurrent limit Sense is 1 if above current limit	L to H	8.0
V33FAULTI	V33FAULTM	V33FAULTS	V33 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VLDO3FAULTI	VLDO3FAULTM	VLDO1FAULTS	VLDO3 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VLDO4FAULTI	VLDO4FAULTM	VLDO4FAULTS	VLDO4 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VPWROVI	VPWROVM	VPWROVS	VPWR pin overvoltage interrupt	L to H	0.122

[1] Typical debounce timing for the falling edge can be extended with PWRONDBNC[1:0].

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A full description of all interrupt, mask, and sense registers is provided in Table 33 to Table 44.

Table 33. Register INTSTAT0 – ADDR 0x05

Name	Bit #	R/W	Default	Description
PWRONI	0	R/W1C	0	Power on interrupt bit
LOWVINI	1	R/W1C	0	Low-voltage interrupt bit
THERM110I	2	R/W1C	0	110 °C thermal interrupt bit
THERM120I	3	R/W1C	0	120 °C thermal interrupt bit
THERM125I	4	R/W1C	0	125 °C thermal interrupt bit
THERM130I	5	R/W1C	0	130 °C thermal interrupt bit
Unused	7:6	–	0b00	Unused

Table 34. Register INTMASK0 – ADDR 0x06

Name	Bit #	R/W	Default	Description
PWRONM	0	R/W1C	1	Power on interrupt mask bit
LOWVINM	1	R/W1C	1	Low-voltage interrupt mask bit
THERM110M	2	R/W1C	1	110 °C thermal interrupt mask bit
THERM120M	3	R/W1C	1	120 °C thermal interrupt mask bit
THERM125M	4	R/W1C	1	125 °C thermal interrupt mask bit
THERM130M	5	R/W1C	1	130 °C thermal interrupt mask bit
Unused	7:6	–	0b00	Unused

Table 35. Register INTSENSE0 – ADDR 0x07

Name	Bit #	R/W	Default	Description
PWRONS	0	R	0	Power on sense bit 0 = PWRON low 1 = PWRON high
LOWVINS	1	R	0	Low-voltage sense bit 0 = VIN > 2.7 V 1 = VIN ≤ 2.7 V
THERM110S	2	R	0	110 °C thermal sense bit 0 = Below threshold 1 = Above threshold
THERM120S	3	R	0	120 °C thermal sense bit 0 = Below threshold 1 = Above threshold
THERM125S	4	R	0	125 °C thermal sense bit 0 = Below threshold 1 = Above threshold
THERM130S	5	R	0	130 °C thermal sense bit 0 = Below threshold 1 = Above threshold
ICTEST1S	6	R	0	0 = ICTEST1 pin is grounded 1 = ICTEST1 to VCOREDIG or greater

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Table 35. Register INTSENSE0 – ADDR 0x07*...continued*

Name	Bit #	R/W	Default	Description
ICTEST2S	7	R	0	Additional ICTEST2 voltage sense pin 0 = ICTEST2 pin is grounded 1 = ICTEST2 to VCOREDIG or greater

Table 36. Register INTSTAT1 – ADDR 0x08

Name	Bit #	R/W	Default	Description
SW1FAULTI	0	R/W1C	0	SW1 overcurrent interrupt bit
Unused	1	R/W1C	0	Unused
Unused	2	R/W1C	0	Unused
SW2FAULTI	3	R/W1C	0	SW2 overcurrent interrupt bit
SW3FAULTI	4	R/W1C	0	SW3 overcurrent interrupt bit
Unused	5	R/W1C	0	Unused
Unused	6	R/W1C	0	Unused
Unused	7	–	0	Unused

Table 37. Register INTMASK1 – ADDR 0x09

Name	Bit #	R/W	Default	Description
SW1FAULTM	0	R/W	1	SW1 overcurrent interrupt mask bit
Unused	1	R/W	1	Unused
Unused	2	R/W	1	Unused
SW2FAULTM	3	R/W	1	SW2 overcurrent interrupt mask bit
SW3FAULTM	4	R/W	1	SW3 overcurrent interrupt mask bit
Unused	5	R/W	1	Unused
Unused	6	R/W	1	Unused
Unused	7	–	0	Unused

Table 38. Register INTSENSE1 – ADDR 0x0A

Name	Bit #	R/W	Default	Description
SW1FAULTS	0	R	0	SW1 overcurrent sense bit 0 = Normal operation 1 = Above current limit
Unused	1	R	0	Unused
Unused	2	R	0	Unused
SW2FAULTS	3	R	0	SW2 overcurrent sense bit 0 = Normal operation 1 = Above current limit
SW3FAULTS	4	R	0	SW3 overcurrent sense bit 0 = Normal operation 1 = Above current limit
Unused	5	R	0	Unused

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Table 38. Register INTSENSE1 – ADDR 0x0A*...continued*

Name	Bit #	R/W	Default	Description
Unused	6	R	0	Unused
Unused	7	–	0	Unused

Table 39. Register INTSTAT3 – ADDR 0x0E

Name	Bit #	R/W	Default	Description
Unused	0	R/W1C	0	Unused
Unused	1	–	0b0	Unused
VPWROVI	2	R/W1C	0b0	High when overvoltage event is detected in the front-end LDO circuit. This bit defaults to 0b1 when VPWR is grounded and the VIN path is used to power the PF3001.
Unused	5:3	–	0b0	Unused
Unused	6	R/W1C	0b0	Unused
Unused	7	R/W1C	0	Unused

Table 40. Register INTMASK3 – ADDR 0x0F

Name	Bit #	R/W	Default	Description
Unused	0	R/W	1	Unused
Unused	1	–	0	Unused
VPWROVM	2	R/W	1	VPWR overvoltage interrupt mask bit
Unused	5:3	–	0b000	Unused
Unused	6	R/W	1	Unused
Unused	7	R/W	1	Unused

Table 41. Register INTSENSE3 – ADDR 0x10

Name	Bit #	R/W	Default	Description
Unused	0	R	0	Unused
Unused	1	–	0b0	Unused
VPWROVS	2	R	0	VPWR overvoltage interrupt sense bit
Unused	5:3	–	0b000	Unused
Unused	6	R	0	Unused
Unused	7	R	0	Unused

Table 42. Register INTSTAT4 – ADDR 0x11

Name	Bit #	R/W	Default	Description
VLDO1FAULTI	0	R/W1C	0	VLDO1 overcurrent interrupt bit
VLDO2FAULTI	1	R/W1C	0	VLDO2 overcurrent interrupt bit
VCC_SDFAULTI	2	R/W1C	0	VCC_SD overcurrent interrupt bit
V33FAULTI	3	R/W1C	0	V33 overcurrent interrupt bit

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Table 42. Register INTSTAT4 – ADDR 0x11*...continued*

Name	Bit #	R/W	Default	Description
VLDO3FAULTI	4	R/W1C	0	VLDO3 overcurrent interrupt bit
VLDO4FAULTI	5	R/W1C	0	VLDO4 overcurrent interrupt bit
Unused	7:6	–	0b00	Unused

Table 43. Register INTMASK4 – ADDR 0x12

Name	Bit #	R/W	Default	Description
VLDO1FAULTM	0	R/W	1	VLDO1 overcurrent interrupt mask bit
VLDO2FAULTM	1	R/W	1	VLDO2 overcurrent interrupt mask bit
VCC_SDFAULTM	2	R/W	1	VCC_SD overcurrent interrupt mask bit
V33FAULTM	3	R/W	1	V33 overcurrent interrupt mask bit
VLDO3FAULTM	4	R/W	1	VLDO3 Overcurrent interrupt mask bit
VLDO4FAULTM	5	R/W	1	VLDO4 Overcurrent interrupt mask bit
Unused	7:6	–	0b00	Unused

Table 44. Register INTSENSE4 – ADDR 0x13

Name	Bit #	R/W	Default	Description
VLDO1FAULTS	0	R	0	VLDO1 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VLDO2FAULTS	1	R	0	VLDO2 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VCC_SDFAULTS	2	R	0	VCC_SD overcurrent sense bit 0 = Normal operation 1 = Above current limit
V33FAULTS	3	R	0	V33 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VLDO3FAULTS	4	R	0	VLDO3 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VLDO4FAULTS	5	R	0	VLDO4 overcurrent sense bit 0 = Normal operation 1 = Above current limit
Unused	7:6	–	0b00	Unused

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8.6.5 Specific registers

8.6.5.1 IC and version identification

The IC and other version details can be read via identification bits. These are hard-wired on the chip and described in Table 45 to Table 47.

Table 45. Register DEVICEID – ADDR 0x00

Name	Bit #	R/W	Default	Description
DEVICEID	3:0	R	0x1	0001 = PF3001
Unused	7:4	–	0x3	Unused

Table 46. Register SILICON REV– ADDR 0x03

Name	Bit #	R/W	Default	Description
METAL_LAYER_REV	3:0	R	0x0	Represents the metal mask revision Pass 0.0 = 0000 … Pass 0.15 = 1111
FULL_LAYER_REV	7:4	R	0x1	Represents the full mask revision Pass 1.0 = 0001 … Pass 15.0 = 1111

Table 47. Register FABID – ADDR 0x04

Name	Bit #	R/W	Default	Description
FIN	1:0	R	0b00	Allows for characterizing different options within the same reticule
FAB	3:2	R	0b00	Represents the wafer manufacturing facility
Unused	7:4	R	0b0000	Unused

8.6.5.2 Embedded memory

There are four register banks of general purpose embedded memory to store critical data. The data written to MEMA[7:0], MEMB[7:0], MEMC[7:0], and MEMD[7:0] is maintained by the coin cell when the main battery is deeply discharged, removed, or contact-bounced. The contents of the embedded memory are reset by COINPORB. The banks can be used for any system need for bit retention with coin cell backup.

Table 48. Register MEMA – ADDR 0x1C

Name	Bit #	R/W	Default	Description
MEMA	7:0	R/W	0x00	Memory bank A

Table 49. Register MEMB – ADDR 0x1D

Name	Bit #	R/W	Default	Description
MEMB	7:0	R/W	0x00	Memory bank B

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Table 50. Register MEMC – ADDR 0x1E

Name	Bit #	R/W	Default	Description
MEMC	7:0	R/W	0x00	Memory bank C

Table 51. Register MEMD – ADDR 0x1F

Name	Bit #	R/W	Default	Description
MEMD	7:0	R/W	0x00	Memory bank D

8.6.5.3 Register descriptions

This section describes all the PF3001 registers and their individual bits. Address order is as listed in Section 8.6.6.

8.6.5.3.1 Interrupt status register 0 (INTSTAT0)

INSTAT0 is one of the four status interrupt registers. This register contains six status flags. Write a logic 1 to clear a flag.

Table 52. Status interrupt register 0 (INTSTAT0)

Address: 0x05 functional page **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W			THERM130I	THERM125I	THERM120I	THERM110I	LOWVINI	PWRONI
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

Table 53. INTSTAT0 field descriptions

Field	Description
5 THERM130I	**130 °C thermal interrupt bit** — THERM130I is set to 1 when the THERM130 threshold specified in is crossed in either direction (bidirectional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM130 threshold 1 Die temperature has crossed THERM130 threshold
4 THERM125I	**125 °C thermal interrupt bit** — THERM125I is set to 1 when the THERM125 threshold specified in is crossed in either direction (bidirectional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM125 threshold 1 Die temperature has crossed THERM125 threshold
3 THERM120I	**120 °C thermal interrupt bit** — THERM120I is set to 1 when the THERM120 threshold specified in is crossed in either direction (bidirectional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM120 threshold 1 Die temperature has crossed THERM120 threshold

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Table 53. INTSTAT0 field descriptions...*continued*

Field	Description
2 THERM110I	**110 °C thermal interrupt bit** — THERM110I is set to 1 when the THERM110 threshold specified in is crossed in either direction (bidirectional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM110 threshold 1 Die temperature has crossed THERM110 threshold
1 LOWVINI	**Low-voltage interrupt bit** — LOWVINI is set to 1 when a low-voltage event occurs on VIN. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 V_{IN} > 2.7 V (typical) 1 V_{IN} < 2.7 V (typical)
0 PWRONI	**Power-on interrupt bit** — PWRONI is set to 1 when the turn on event occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Power on has not occurred 1 Power on has occurred

8.6.5.3.2 Interrupt status mask register 0 (INTMASK0)

INTMASK0 is the mask register for the status interrupt register INTSTAT0. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 54. Interrupt status mask register 0 (INTMASK0)

Address: 0x06 functional page — **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W			THERM130M	THERM125M	THERM120M	THERM110M	LOWVINM	PWRONM
Default	0	0	1	1	1	1	1	1

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

Table 55. INTMASK0 field descriptions

Field	Description
5 THERM130M	130 °C thermal interrupt mask bit 0 THERM130I unmasked 1 THERM130I Masked
4 THERM125M	125 °C thermal interrupt mask bit 0 THERM125I unmasked 1 THERM125I masked
3 THERM120M	120 °C thermal interrupt mask bit 0 THERM120I unmasked 1 THERM120I masked
2 THERM110M	110 °C thermal interrupt mask bit 0 THERM110I unmasked 1 THERM110I masked
1 LOWVINM	Low-voltage interrupt mask bit 0 LOWVINI unmasked 1 LOWVINI masked

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Table 55. INTMASK0 field descriptions*...continued*

Field	Description
0 PWRONM	Power on interrupt mask bit 0 PWRONI unmasked 1 PWRONI masked

8.6.5.3.3 Interrupt sense register 0 (INTSENSE0)

This register has seven read-only sense bits. These sense bits reflect the actual state of the corresponding function.

Table 56. Interrupt sense register 0 (INTSENSE0)

Address: 0x07 functional page **Access: User read-only[1]**

	7	6	5	4	3	2	1	0
R	ICTEST2S		THERM130S	THERM125S	THERM120S	THERM110S	LOWVINS	PWRONS
W								
Default	X[2]	0	X[3]	X[3]	X[3]	X[3]	X[4]	X[5]

= Unimplemented or Reserved

[1] Read: Anytime
[2] Default value depends on the initial ICTEST2S pin state.
[3] Default value depends on the initial temperature of the die.
[4] Default value depends on the initial VIN voltage.
[5] Default value depends on the initial PWRON pin state.

Table 57. INTSENSE0 field descriptions

Field	Description
7 ICTEST2S	VDDOTP voltage sense bit 0 ICTEST2S grounded 1 ICTEST2S to VCOREDIG or greater
5 THERM130S	130 °C thermal interrupt sense bit 0 Die temperature below THERM130 threshold 1 Die temperature above THERM130 threshold
4 THERM125S	125 °C thermal interrupt sense bit 0 Die temperature below THERM125 threshold 1 Die temperature has crossed THERM125 threshold
3 THERM120S	120 °C thermal interrupt sense bit 0 Die temperature below THERM120 threshold 1 Die temperature has crossed THERM120 threshold
2 THERM110S	110 °C thermal interrupt sense bit 0 Die temperature below THERM110 threshold 1 Die temperature has crossed THERM110 threshold
1 LOWVINS	Low-voltage interrupt sense bit 0 V_{IN} > 2.7 V (typical) 1 V_{IN} < 2.7 V (typical)
0 PWRONS	Power-on interrupt sense bit 0 PWRON low 1 PWRON high

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8.6.5.3.4 Interrupt status register 1 (INTSTAT1)

INSTAT1 is one of the three status interrupt registers. This register contains three status flags. Write a logic 1 to clear a flag.

Table 58. Status interrupt register 1 (INTSTAT1)

	Address: 0x08 functional page						Access: User read/write[1]	
	7	6	5	4	3	2	1	0
R W				SW3 FAULTI	SW2 FAULTI			SW1 FAULTI
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

Table 59. INTSTAT1 field descriptions

Field	Description
4 SW3FAULTI	**SW3 overcurrent interrupt bit** — SW3FAULTI is set to 1 when the SW3 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 SW3 in normal operation 1 SW3 above current limit
3 SW2FAULTI	**SW2 overcurrent interrupt bit** — SW2FAULTI is set to 1 when the SW2 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 SW2 in normal operation 1 SW2 above current limit
0 SW1FAULTI	**SW1 overcurrent interrupt bit** — SW1FAULTI is set to 1 when the SW1 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 SW1 in normal operation 1 SW1 above current limit

8.6.5.3.5 Interrupt status mask register 1 (INTMASK1)

INTMASK1 is the mask register for the status interrupt register INTSTAT1. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 60. Interrupt status mask register 1 (INTMASK1)

	Address: 0x09 functional page						Access: User read/write[1]	
	7	6	5	4	3	2	1	0
R W				SW3 FAULTM	SW2 FAULTM			SW1 FAULTM
Default	0	0	0	1	1	0	1	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

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Table 61. INTMASK1 field descriptions

Field	Description
4 SW3FAULTM	SW3 overcurrent interrupt mask bit 0 SW3FAULTI Unmasked 1 SW3FAULTI Masked
3 SW2FAULTM	SW2 overcurrent interrupt mask bit 0 SW2FAULTI Unmasked 1 SW2FAULTI Masked
0 SW1FAULTM	SW1 overcurrent interrupt mask bit 0 SW1FAULTI Unmasked 1 SW1FAULTI Masked

8.6.5.3.6 Interrupt sense register 1 (INTSENSE1)

This register has three read-only sense bits. These sense bits reflect the actual state of the corresponding function.

Table 62. Interrupt sense register 1 (INTSENSE1)

Address: 0x0A functional page **Access: User read-only**[1]

	7	6	5	4	3	2	1	0
R				SW3 FAULTS	SW2 FAULTS			SW1 FAULTS
W								
Default	0	0	0	X[2]	X[2]	0	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
[2] Default value depends on the regulator initial state

Table 63. INTSENSE1 field descriptions

Field	Description
4 SW3FAULTS	SW3 overcurrent sense bit 0 SW3 in normal operation 1 SW3 above current limit
3 SW2FAULTS	SW2 overcurrent sense bit 0 SW2 in normal operation 1 SW2 above current limit
0 SW1FAULTS	SW1 overcurrent sense bit 0 SW1 in normal operation 1 SW1 above current limit

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8.6.5.3.7 Interrupt status register 3 (INTSTAT3)

INSTAT3 is one of the status interrupt registers. This register contains a status flag. Write a logic 1 to clear a flag.

Table 64. Status Interrupt Register 3 (INTSTAT3)

Address: 0x0E functional page							Access: User read/write[1]
7	6	5	4	3	2	1	0
R W						VPWROVI		
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

Table 65. INTSTAT3 field descriptions

Field	Description
2 VPWROVI	**VPWR overvoltage interrupt bit** — High when overvoltage event is detected in the front-end LDO circuit. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VPWR in normal operation range. 1 VPWR in overvoltage range.

8.6.5.3.8 Interrupt status mask register 3 (INTMASK3)

INTMASK3 is the mask register for the status interrupt register INTSTAT3. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 66. Interrupt status mask register 3 (INTMASK3)

Address: 0x0F functional page							Access: User read/write[1]
7	6	5	4	3	2	1	0
R W						VPWROVM		
Default	1	1	0	0	0	1	0	1

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

Table 67. INTMASK3 field descriptions

Field	Description
2 VPWROVM	VPWR overvoltage interrupt mask bit 0 VPWROVI Unmasked 1 VPWROVI Masked

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8.6.5.3.9 Interrupt sense register 3 (INTSENSE3)

This register has four read-only sense bits. These sense bits reflect the actual state of the corresponding function.

Table 68. Interrupt sense register 3 (INTSENSE3)

	Address: 0x10 functional page					Access: User read-only[1]		
	7	6	5	4	3	2	1	0
R						VPWROVS		
W								
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime

Table 69. INTSENSE3 field descriptions

Field	Description
2 VPWROVS	VPWR overvoltage interrupt sense bit 0 VPWR in normal operation range 1 VPWR in overvoltage range

8.6.5.3.10 Interrupt status register 4 (INTSTAT4)

INSTAT4 is one of the status interrupt registers. This register contains six status flags. Write a logic 1 to clear a flag.

Table 70. Status interrupt register 4 (INTSTAT4)

	Address: 0x11 functional page					Access: User read/write[1]		
	7	6	5	4	3	2	1	0
R W			VLDO4 FAULTI	VLDO3 FAULTI	V33FAULTI	VCC_ SDFAULTI	VLDO2 FAULTI	VLDO1 FAULTI
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

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Table 71. INTSTAT4 field descriptions

Field	Description
5 VLDO4FAULTI	**VLDO4 overcurrent interrupt bit** — VLDO4FAULTI is set to 1 when the VLDO4 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO4 in normal operation 1 VLDO4 above current limit
4 VLDO3FAULTI	**VLDO3 overcurrent interrupt bit** — VLDO3FAULTI is set to 1 when the VLDO3 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO3 in normal operation 1 VLDO3 above current limit
3 V33FAULTI	**V33 overcurrent interrupt bit** — V33FAULTI is set to 1 when the V33 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 V33 in normal operation 1 V33 above current limit
2 VCC_SDFAULTI	**VCC_SD overcurrent interrupt bit** — VCC_SDFAULTI is set to 1 when the VCC_SD regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VCC_SD in normal operation 1 VCC_SD above current limit
1 VLDO2FAULTI	**VLDO2 overcurrent interrupt bit** — VLDO2FAULTI is set to 1 when the VLDO2 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO2 in normal operation range. 1 VLDO2 above current limit
0 VLDO1FAULTI	**VLDO1 overcurrent interrupt bit** — VLDO1FAULTI is set to 1 when the VLDO1 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO1 in normal operation range. 1 VLDO1 above current limit

8.6.5.3.11 Interrupt status mask register 4 (INTMASK4)

INTMASK4 is the mask register for the status interrupt register INTSTAT4. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 72. Interrupt status mask register 4 (INTMASK4)

Address: 0x12 functional page — **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W			VLDO4 FAULTM	VLDO3 FAULTM	V33FAULTM	VCC_ SDFAULTM	VLDO2 FAULTM	VLDO1 FAULTM
Default	0	0	1	1	1	1	1	1

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

Table 73. INTMASK4 field descriptions

Field	Description
5 VLDO4FAULTM	VLDO4 overcurrent interrupt mask bit 0 VLDO4FAULTI Unmasked 1 VLDO4FAULTI Masked

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Table 73. INTMASK4 field descriptions...*continued*

Field	Description
4 VLDO3FAULTM	VLDO3 overcurrent interrupt mask bit 0 VLDO3FAULTI Unmasked 1 VLDO3FAULTI Masked
3 V33FAULTM	V33 overcurrent interrupt mask bit 0 V33FAULTI Unmasked 1 V33FAULTI Masked
2 VCC_SDFAULTM	VCC_SD overcurrent interrupt mask bit 0 VCC_SDFAULTI Unmasked 1 VCC_SDFAULTI Masked
1 VLDO2FAULTM	VLDO2 overcurrent interrupt mask bit 0 VLDO2FAULTI Unmasked 1 VLDO2FAULTI Masked
0 VLDO1FAULTM	VLDO1 overcurrent interrupt mask bit 0 VLDO1FAULTI Unmasked 1 VLDO1FAULTI Masked

8.6.5.3.12 Interrupt sense register 4 (INTSENSE4)

This register has read-only sense bits. These sense bits reflect the actual state of the corresponding function.

Table 74. Interrupt sense register 4 (INTSENSE4)

Address: 0x13 functional page **Access: User read-only**[1]

	7	6	5	4	3	2	1	0
R			VLDO4 FAULTS	VLDO3 FAULTS	V33FAULTS	VCC_ SDFAULTS	VLDO2 FAULTS	VLDO1 FAULTS
W								
Default	0	0	X[2]	X[2]	X[2]	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
[2] Default value depends on the regulator initial state

Table 75. INTSENSE4 Field Descriptions

Field	Description
5 VLDO4FAULTS	VLDO4 overcurrent sense bit 0 VLDO4 in normal operation 1 VLDO4 above current limit
4 VLDO3FAULTS	VLDO3 overcurrent sense bit 0 VLDO3 in normal operation 1 VLDO3 above current limit
3 V33FAULTS	V33 overcurrent sense bit 0 V33 in normal operation 1 V33 above current limit
2 VCC_SDFAULTS	VCC_SD overcurrent sense bit 0 VCC_SD in normal operation 1 VCC_SD above current limit

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Table 75. INTSENSE4 Field Descriptions*...continued*

Field	Description
1 VLDO2FAULTS	VLDO2 overcurrent sense bit 0 VLDO2 in normal operation 1 VLDO2 above current limit
0 VLDO1FAULTS	VLDO1 overcurrent sense bit 0 VLDO1 in normal operation 1 VLDO1 above current limit

8.6.5.3.13 Coin cell control register (COINCTL)

This register is used to control the coin cell charger.

Table 76. Coin cell control register (COINCTL)

	Address: 0x1A functional page						Access: User read/write[1]	
	7	6	5	4	3	2	1	0
R W					COINCHEN	VCOIN		
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

Table 77. COINCTL field descriptions

Field	Description
3 COINCHEN	Coin cell charger enable bit 0 Coin cell charger disabled. 1 Coin cell charger enabled.
2:0 VCOIN	**Coin cell charger output voltage selection** — This field is used to set the coin cell charging voltage from 2.50 V to 3.30 V. See Table 27 for all options selectable through these bits.

8.6.5.3.14 Power control register (PWRCTL)

Table 78. Power control register (PWRCTL)

	Address: 0x1B functional page						Access: User read/write[1]	
	7	6	5	4	3	2	1	0
R W	REG SCPEN						PWRONR STEN	RES TARTEN
Default	0	0	0	1	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

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Table 79. PWRCTL field descriptions

Field	Description
7 REGSCPEN	**Short-circuit protection enable bit** — When REGSCPEN is set to 1, whenever a current limit event occurs on a LDO regulator, this regulator is shutdown. 0 Short-circuit protection disabled 1 Short-circuit protection enabled
1 PWRONRSTEN	**PWRON reset enable bit** — When set to 1, the PF3001 can enter Off mode when the PWRON pin is held low for 4 seconds or longer. See Section 8.5.1.3 for more details. 0 Disallow Off mode after PWRON held low 1 Allow Off mode after PWRON held low
0 RESTARTEN	**Restart enable bit** — When set to 1, the PF3001 restarts automatically after a power off event generated by the PWRON (held low for 4 seconds or longer) when PWR_CFG bit = 1. 0 Automatic restart disabled 1 Automatic restart enabled

8.6.5.3.15 Embedded memory register A (MEMA)

Table 80. Embedded memory register A (MEMA)

Address: 0x1C functional page — **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W	MEMA							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

Table 81. MEMA field descriptions

Field	Description
7:0 MEMA	**Memory bank A** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

8.6.5.3.16 Embedded memory register B (MEMB)

Table 82. Embedded memory register B (MEMB)

Address: 0x1D functional page — **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W	MEMB							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

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Table 83. MEMB field descriptions

Field	Description
7:0 MEMB	**Memory bank B** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

8.6.5.3.17 Embedded memory register C (MEMC)

Table 84. Embedded Memory Register C (MEMC)

Address: 0x1E functional page **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W	MEMC							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

Table 85. MEMC field descriptions

Field	Description
7:0 MEMC	**Memory bank C** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

8.6.5.3.18 Embedded memory register D (MEMD)

Table 86. Embedded memory register D (MEMD)

Address: 0x1F functional page **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W	MEMD							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

Table 87. MEMD field descriptions

Field	Description
7:0 MEMD	**Memory bank D** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

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8.6.5.3.19 SW1 voltage control register (SW1VOLT)

This register is used to set the output voltage of the SW1 regulator in normal operation.

Table 88. SW1 voltage control register (SW1VOLT)

Address: 0x20 functional page							Access: User read/write[1]
7	6	5	4	3	2	1	0
R W				SW1			
Default	0	0	0	X[2]	X[2]	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on OTP content.

Table 89. SW1VOLT field descriptions

Field	Description
4:0 SW1	**SW1 output voltage** — See Table 12

8.6.5.3.20 SW1 switching mode selector register (SW1MODE)

This register is used to set the switching mode of the SW1 regulator.

Table 90. SW1 switching mode selector register (SW1MODE)

Address: 0x23 functional page							Access: User read/write[1]
7	6	5	4	3	2	1	0
R W				SW1MODE			
Default	0	0	0	0	X[2]	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

Table 91. SW1MODE field descriptions

Field	Description
4:0 SW1MODE	**SW1 switching mode selector** — See Table 8

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8.6.5.3.21 SW1 configuration register (SW1CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW1 regulator.

Table 92. SW1A configuration register (SW1CONF)

Address: 0x24 functional page **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W			SW1PHASE		SW1FREQ			SW1ILIM
Default	0	0	0	0	X[2]	X[2]	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on OTP content.

Table 93. SW1ACONF field descriptions

Field	Description
5:4 SW1PHASE	**SW1 phase clock bit**— SW1PHASE is used to set the phase clock for SW1. See Table 9.
3:2 SW1FREQ	**SW1 switching frequency**— SW1PHASE is used to set the desired switching frequency for SW1. See Table 11.
0 SW1ILIM	**SW1 current limiter bit**— This bit configures the current limit for SW1. 0 2.75 A (typ) 1 2.0 A (typ)

8.6.5.3.22 SW2 voltage control register (SW2VOLT)

This register is used to set the output voltage of the SW2 regulator in normal operation.

Table 94. SW2 voltage control register (SW2VOLT)

Address: 0x35 functional page **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W				SW2				
Default	0	0	0	X[2]	X[2]	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

Table 95. SW2VOLT field descriptions

Field	Description
4:0 SW2	**SW2 output voltage** — See Table 14.

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8.6.5.3.23 SW2 switching mode selector register (SW2MODE)

This register is used to set the Switching mode of the SW2 regulator.

Table 96. SW2 Switching mode selector register (SW2MODE)

Address: 0x38 functional page							Access: User read/write[1]
	7	6	5	4	3	2	1	0
R W					SW2MODE			
Default	0	0	0	0	X[2]	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

Table 97. SW2MODE field descriptions

Field	Description
3:0 SW2MODE	**SW2 switching mode selector** — See Table 8.

8.6.5.3.24 SW2 configuration register (SW2CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW2 regulator.

Table 98. SW2 configuration register (SW2CONF)

Address: 0x39 functional page							Access: User read/write[1]
	7	6	5	4	3	2	1	0
R W			SW2PHASE		SW2FREQ			SW2ILIM
Default	0	0	0	0	X[2]	X[2]	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on OTP content.

Table 99. SW2CONF field descriptions

Field	Description
5:4 SW2PHASE	**SW2 phase clock bit** — SW2PHASE is used to set the phase clock for SW2. See Table 9.
3:2 SW2FREQ	**SW2 switching frequency** — SW2PHASE is used to set the desired switching frequency for SW2. See Table 11.
0 SW2ILIM	**SW2 current limiter bit** — This bit configures the current limit for SW2. 0 2.75 A (typ) 1 2.0 A (typ)

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8.6.5.3.25 SW3 voltage control register (SW3VOLT)

This register is used to set the output voltage of the SW3 regulator in normal operation.

Table 100. SW3 voltage control register (SW3VOLT)

	Address: 0x3C functional page							Access: User read/write[1]
	7	6	5	4	3	2	1	0
R W				SW3				
Default	0	0	0	X[2]	X[2]	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

Table 101. SW3VOLT field descriptions

Field	Description
4:0 SW3	**SW3 output voltage** — See Table 16.

8.6.5.3.26 SW3 switching mode selector register (SW3MODE)

This register is used to set the Switching mode of the SW3 regulator.

Table 102. SW3 Switching mode selector register (SW3MODE)

	Address: 0x3F functional page							Access: User read/write[1]
	7	6	5	4	3	2	1	0
R W					SW3MODE			
Default	0	0	0	0	X[2]	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

Table 103. SW3MODE field descriptions

Field	Description
3:0 SW3MODE	**SW3 switching mode selector** — See Table 8.

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8.6.5.3.27 SW3 configuration register (SW3CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW3 regulator.

Table 104. SW3 configuration register (SW3CONF)

	Address: 0x40 functional page						Access: User read/write[1]	
	7	6	5	4	3	2	1	0
R W			SW3PHASE		SW3FREQ			SW3ILIM
Default	0	0	1	0	X[2]	X[2]	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on OTP content.

Table 105. SW3CONF field descriptions

Field	Description
5:4 SW3PHASE	**SW3 phase clock bit** — SW3PHASE is used to set the phase clock for SW3. See Table 9.
3:2 SW3FREQ	**SW3 switching frequency** — SW3PHASE is used to set the desired switching frequency for SW3. See Table 11.
0 SW3ILIM	**SW3 current limiter bit** — This bit configures the current limit for SW3. 0 3.0 A (typ) 1 2.25 A (typ)

8.6.5.3.28 VSNVS control register (VSNVSCTL)

This register is used to control the VSNVS supply operation.

Table 106. VSNVS control register (VSNVSCTL)

	Address: 0x6B functional page					Access: User read/write[1]		
	7	6	5	4	3	2	1	0
R W						VSNVSVOLT		
Default	0	0	0	0	0	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

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Table 107. VSNVSCTL field descriptions

Field	Description
2:0 VSNVSVOLT	**VSNVS output voltage configuration** — VSNVSVOLT is used to configure the VSNVS output voltage. Values below are typical voltages. 000 = RSVD 001 = RSVD 010 = RSVD 011 = RSVD 100 = RSVD 101 = RSVD 110 = 3.0 V (default) 111 = RSVD

8.6.5.3.29 VLDO1 control register (VLDO1CTL)

This register is used to configure Output Voltage, Normal mode operation of the VLDO1 regulator.

Table 108. VLDO1 control register (VLDO1CTL)

Address: 0x6C functional page — **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W				VLDO1EN	VLDO1			
Default	0	0	0	X[2]	X[2]	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

Table 109. VLDO1CTL field descriptions

Field	Description
4 VLDO1EN	**VLDO1 enable bit** — VLDO1EN is used to enable or disable the VLDO1 regulator. 0 VLDO1 disabled 1 VLDO1 enabled
3:0 VLDO1	**VLDO1 output voltage configuration** — See Table 19.

8.6.5.3.30 VLDO2 control register (VLDO2CTL)

This register is used to configure Output Voltage, Normal mode operation of the VLDO2 regulator.

Table 110. VLDO2 control register (VLDO2CTL)

Address: 0x6D functional page — **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W				VLDO2EN	VLDO2			
Default	0	0	0	X[2]	X[2]	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

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Table 111. VLDO2CTL field descriptions

Field	Description
4 VLDO2EN	**VLDO2 enable bit** — VLDO2EN is used to enable or disable the VLDO2 regulator. 0 VLDO2 disabled 1 VLDO2 enabled
3:0 VLDO2	**VLDO2 output voltage configuration** — See Table 19.

8.6.5.3.31 VCC_SD control register (VCC_SDCTL)

This register is used to configure Output Voltage, Normal mode operation of the VCC_SD regulator.

Table 112. CC_SD control register (VCC_SDCTL)

	Address: 0x6E functional page						Access: User read/write[1]	
	7	6	5	4	3	2	1	0
R W				VCC_SDEN			VCC_SD	
Default	0	0	0	X[2]	0	0	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

Table 113. VCC_SDCTL field descriptions

Field	Description
4 VCC_SDEN	**VCC_SD enable bit** — VCC_SDEN is used to enable or disable the VCC_SD regulator. 0 VCC_SD disabled 1 VCC_SD enabled
1:0 VCC_SD	**VCC_SD output voltage configuration** — See Table 22.

8.6.5.3.32 V33 control register (V33CTL)

This register is used to configure Output Voltage, Normal mode operation of the V33 regulator.

Table 114. V33 control register (V33CTL)

	Address: 0x6F functional page						Access: User read/write[1]	
	7	6	5	4	3	2	1	0
R W				V33EN			V33	
Default	0	0	0	X[2]	0	0	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

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Table 115. V33CTL field descriptions

Field	Description
4 V33EN	**V33 enable bit** — V33EN is used to enable or disable the VLDO2 regulator. 0 V33 disabled 1 V33 enabled
1:0 V33	**V33 output voltage configuration** — See Table 21.

8.6.5.3.33 VLDO3 control register (VLDO3CTL)

This register is used to configure Output Voltage, Normal mode operation of the VLDO3 regulator.

Table 116. VLDO3 control register (VLDO3CTL)

Address: 0x70 functional page **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W				VLDO3EN	VLDO3			
Default	0	0	0	X[2]	X[2]	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

Table 117. VLDO3CTL field descriptions

Field	Description
4 VLDO3EN	**VLDO3 enable bit** — VLDO3EN is used to enable or disable the VLDO3 regulator. 0 VLDO3 disabled 1 VLDO3 enabled
3:0 VLDO3	**VLDO3 output voltage configuration** — See Table 20.

8.6.5.3.34 VLDO4 control register (VLDO4CTL)

This register is used to configure Output Voltage, Normal mode operation of the VLDO4 regulator.

Table 118. VLDO4 control register (VLDO4CTL)

Address: 0x71 functional page **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W				VLDO4EN	VLDO4			
Default	0	0	0	X[2]	X[2]	X[2]	X[2]	X[2]

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime
[2] Default value depends on startup sequence.

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Table 119. VLDO4CTL field descriptions

Field	Description
4 VLDO4EN	**VLDO4 enable bit** — VLDO4EN is used to enable or disable the VLDO4 regulator. 0 VLDO4 disabled 1 VLDO4 enabled
3:0 VLDO4	**VLDO4 output voltage configuration** — See Table 20.

8.6.5.3.35 Page selection register

This register is used to access the extended register pages.

Table 120. Page selection register

Address: 0x7F functional page **Access: User read/write**[1]

	7	6	5	4	3	2	1	0
R W					PAGE			
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

[1] Read: Anytime
Write: Anytime

Table 121. Page register field descriptions

Field	Description
3:0 PAGE	**Register page selection** — The page field is used to select the register pages. 0000 Functional page selected

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8.6.6 Register map

The register map is only one page and its addresses and data fields are each eight bits wide. This page registers 0x00 to 0x7F are referred to as “functional”.

Registers missing in the sequence are reserved; reading from them returns a value 0x00, and writing to them has no effect. The contents of all registers are given in the tables defined in this chapter; each table is structure as follows:

Name: Name of the bit

Bit #: The bit location in the register (7-0)

R/W: Read/Write access and control

- R is read-only access
- R/W is read and write access
- RW1C is read and write access with write 1 to clear

Reset: Reset signals are color coded based on the following legend.

Bits reset by SC and VCOREDIG_PORB
Bits reset by PWRON or loaded default
Bits reset by DIGRESETB
Bits reset by PORB or RESETBMCU
Bits reset by VCOREDIG_PORB
Bits reset by POR or OFFB

Default: The value after reset, as noted in the default column of the memory map.

- Fixed defaults are explicitly declared as 0 or 1.
- “X” corresponds to Read/Write bits initialized at startup. Bits are subsequently I^2C modifiable, when their reset has been released. “X”, may also refer to bits which may have other dependencies. For example, some bits may depend on the version of the IC, or a value from an analog block, for instance the sense bits for the interrupts.

8.6.6.1 Register map

Table 122. Functional page

				BITS[7:0]							
Add	Register Name	R/W	Default	7	6	5	4	3	2	1	0
00	DeviceID	R	8'b0011_0000	–	–	–	–	DEVICE ID [3:0]			
				0	0	1	1	0	0	0	1
03	SILICO NREVI D	R	8'b0001_0000	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			
				0	0	0	1	0	0	0	0
04	FABID	R	8'b0000_0000	–	–	–	–	FAB[1:0]		FIN[1:0]	
				0	0	0	0	0	0	0	0
05	INTSTAT0	RW1C	8'b0000_0000	–	–	THERM130I	THERM125I	THERM120I	THERM110I	LOWVINI	PWRONI
				0	0	0	0	0	0	0	0
06	INTMASK0	R/W	8'b0011_1111	–	–	THERM130M	THERM125M	THERM120M	THERM110M	LOWVINM	PWRONM
				0	0	1	1	1	1	1	1
07	INTSENSE0	R	8'b00xx_xxxx	ICTEST2S	ICTESTS	THERM130S	THERM125S	THERM120S	THERM110S	LOWVINS	PWRONS
				0	0	x	x	x	x	x	x

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Table 122. Functional page...*continued*

				BITS[7:0]							
Add	Register Name	R/W	Default	7	6	5	4	3	2	1	0
08	INTSTAT1	RW1C	8'b0000_0000	–	–	–	SW3FAULTI	SW2FAULTI	–	–	SW1FAULTI
				0	0	0	0	0	x	0	0
09	INTMASK1	R/W	8'b0111_1111	–	–	–	SW3FAULTM	SW2FAULTM	–	–	SW1FAULTM
				0	1	1	1	1	1	1	1
0A	INTSENSE1	R	8'b0xxx_xxxx	–	–	–	SW3FAULTS	SW2FAULTS	–	–	SW1FAULTS
				0	x	x	x	x	x	x	x
0E	INTSTAT3	RW1C	8'b0000_0000	–	–	–	–	–	VPWROVI	–	–
				0	0	0	0	0	0	0	0
0F	INTMASK3	R/W	8'b1100_0101	–	–	–	–	–	VPWROVI	–	–
				1	1	0	0	0	1	0	1
10	INTSENSE3	R	8'b0000_000x	–	–	–	–	–	VPWROVS	–	–
				0	0	0	0	0	0	0	x
11	INTSTAT4	RW1C	8'b0000_0000	–	–	VLDO4FAULTI	VLDO3FAULTI	V33FAULTI	VCC_ SDFAUL TI	VLDO2FAULTI	VLDO1FAULTI
				0	0	0	0	0	0	0	0
12	INTMASK4	R/W	8'b0011_1111	–	–	VLDO4 FAULTM	VLDO3 FAULTM	V33 FAULTM	VCC_ SDFAUL TM	VLDO2 FAULT M	VLDO1 FAULT M
				0	0	1	1	1	1	1	1
13	INTSENSE4	R	8'b00xx_xxxx	–	–	VLDO4 FAULTS	VLDO3 FAULTS	V33 FAULTS	VCC_SD FAULTS	VLDO2 FAULTS	VLDO1 FAULTS
				0	0	x	x	x	x	x	x
1A	COINCTL	R/W	8'b0000_0000	–	–	–	–	COINCHEN	VCOIN[2:0]		
				0	0	0	0	0	0	0	0
1B	PWRCTL	R/W	8'b0001_0000	REGSCPEN	–	–		PWRONBDBNC[1:0]		PWR ONRSTE N	RESTARTEN
				0	0	0	1	0	0	0	0
1C	MEMA	R/W	8'b0000_0000	MEMA[7:0]							
				0	0	0	0	0	0	0	0
1D	MEMB	R/W	8'b0000_0000	MEMB[7:0]							
				0	0	0	0	0	0	0	0
1E	MEMC	R/W	8'b0000_0000	MEMC[7:0]							
				0	0	0	0	0	0	0	0
1F	MEMD	R/W	8'b0000_0000	MEMD[7:0]							
				0	0	0	0	0	0	0	0
20	SW1VOLT	R/W	8'b000x_xxxx	–	–	–	SW1[4:0]				
				0	0	0	–	–	–	–	–
21	SW1STBY	R/W	8'b000x_xxxx	–	–	–	–	–	–	–	–
				0	0	0	–	–	–	–	–
22	SW1OFF	R/W	8'b000x_xxxx	–	–	–	–	–	–	–	–
				0	0	0	–	–	–	–	–
23	SW1MODE	R/W	8'b0000_xxxx	–	–	–	–	SW1MODE[3:0]			
				0	0	0	x	–	–	–	–
24	SW1CONF	R/W	8'bxx00_xxx0	–	–	SW1PHASE[1:0]		SW1FREQ[1:0]		–	SW1ILIM
				x	x	0	0	x	x	x	0
2E	RSVD	R/W	8'b0000_0000	–	–	–	–				
				x	x	x	x	x	x	x	x
2F	RSVD	R/W	8'b0000_0000	–	–	–	–				
				x	x	x	x	x	x	x	x
30	RSVD	R/W	8'b0000_0000	–	–	–	–				
				x	x	x	x	x	x	x	x

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Table 122. Functional page...*continued*

				BITS[7:0]							
Add	Register Name	R/W	Default	7	6	5	4	3	2	1	0
31	RSVD	R/W	8'b0001_0000	–	–	–	–	–			
				x	x	0	–	–	–	–	–
32	RSVD	R/W	8'bx100_0000	–	–	–		–		–	–
				x	–	x	x	–	–	x	x
35	SW2VOLT	R/W	8'b0xxx_0110	–	–	–	–	SW2_HL	SW2[2:0]		
				0	x	x	x	–	–	–	–
36	SW2STBY	R/W	8'b0xxx_xxxx	–	–	–	–	–	–	–	–
				0	x	x	x	x	x	x	x
37	SW2OFF	R/W	8'b0xxx_xxxx	–	–	–	–	–	–	–	–
				0	x	x	x	x	x	x	x
38	SW2MODE	R/W	8'b0010_1000	–	–	–	–	SW2MODE[3:0]			
				0	0	0	0	1	0	0	0
39	SW2CONF	R/W	8'bxx01_xxx0	–	–	SW2PHASE[1:0]		SW2FREQ[1:0]		–	SW2ILIM
				x	x	0	1	x	x	x	0
3C	SW3VOLT	R/W	8'b0xxx_1100	–	–	–	–	SW3[3:0]			
				0	x	x	x	–	–	–	–
3D	RSVD	R/W	8'b0xxx_1100	–	–	–	–	–	–	–	–
				0	x	x	x	–	–	–	–
3E	RSVD	R/W	8'b0xxx_1100	–	–	–	–	–	–	–	–
				0	x	–	x	–	–	–	–
3F	SW3MODE	R/W	8'b0011_1000	–	–	0	–	SW3MODE[3:0]			
				0	0	1	1	1	0	0	0
40	SW3CONF	R/W	8'bxx10_xxx0	–	–	SW3PHASE[1:0]		SW3FREQ[1:0]		–	SW3ILIM
				x	–	1	0	–	–	0	0
66	RSVD	R/W	8'b0xx0_0000	–	–		–	–		–	
				0	x	x	0	x	x	x	x
69	RSVD	R/W	8'b0xxx_xxx0	–	–	–	–	–	–	–	–
				0	x	x	x	x	x	x	x
6A	RSVD	R/W	8'b000x_0000	–	–	–	–	–	–	–	–
				x	x	x	–	x	x	x	x
6B	VSNVSCTL	R/W	8'b0000_0110	–	–	–	–	–	VSNVSVOLT[2:0]		
				0	0	0	0	0	1	1	0
6C	VLDO1CTL	R/W	8'b010x_1110	–	–	–	VLDO1EN	VLDO1[3:0]			
				0	0	0	–	–	–	–	–
6D	VLDO2CTL	R/W	8'b000x_1000	–	–	–	VLDO2EN	VLDO2[3:0]			
				0	0	0	–	–	–	–	–
6E	VCC_SDCTL	R/W	8'b000x_xx10	–	–	–	VCC_SDEN	–	–	VCC_SD[1:0]	
				0	0	0	–	x	x	–	–
6F	V33CTL	R/W	8'b000x_xx10	–	–	–	V33EN	–	–	V33[1:0]	
				0	0	0	–	x	x	–	–
70	VLDO3CTL	R/W	8'b010x_0000	–	–	–	VLDO3EN	VLDO3[3:0]			
				0	0	0	–	–	–	–	–
71	VLDO4CTL	R/W	8'b000x_xxxx	–	–	–	VLDO4EN	VLDO4[3:0]			
				0	0	0	–	–	–	–	–
7F	RSVD	R/W	8'b0000_0000	–	–	–		–			
				0	0	0	0	0	0	0	0

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9 General product characteristics

9.1 Maximum ratings

Table 123. Maximum voltage ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Symbol	Description	Value	Unit	Notes
Electrical ratings				
VPWR, ICTEST1, ICTEST2, LDOG	–	-0.3 to 7.5	V	[1]
VIN, VIN2, VLDO1IN, SW1IN, SW2IN, SW3IN, SW1LX, SW2LX, SW3LX	–	-0.3 to 4.8	V	–
INTB, SD_VSEL, RESETBMCU, SW1FB, SW2FB, SW3FB, VLDO1, VLDO2IN, VLDO3, VLDO34 IN, VLDO4, V33, VCC_SD, VSNVS, LICELL, VCORE, SDA, SCL, VDDIO, PWRON	–	-0.3 to 3.6	V	–
VLDO2	VLDO2 linear regulator output	-0.3 to 2.5	V	–
VCOREDIG	Digital core supply voltage output	-0.3 to 1.65	V	–
VCOREREF	Bandgap reference voltage output	-0.3 to 1.5	V	–
V_{ESD}	ESD ratings • Human body model • Charge device model	±2000 ±500	V	[2]

[1] 7.5 V Maximum DC voltage rated.

[2] ESD testing is performed in accordance with the Human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge device model (CDM), Robotic (C_{ZAP} = 4.0 pF).

9.2 Thermal characteristics

Table 124. Thermal ratings

Symbol	Description (rating)	Min	Max	Unit	Notes
Thermal ratings					
T_A	Ambient operating temperature range • Industrial version • Consumer version	 -40 -40	 105 85	°C	–
T_J	Operating junction temperature range	-40	125	°C	[1]
T_{ST}	Storage temperature range	-65	150	°C	–
T_{PPRT}	Peak package reflow temperature	–	[2]	°C	[2][3]
QFN48 thermal resistance and package dissipation ratings					
$R\theta_{JA}$	Junction to ambient, natural convection • Four layer board (2s2p) • Eight layer board (2s6p)	 – –	 24 15	°C/W	[4][5][6]
$R\theta_{JB}$	Junction to Board	–	11	°C/W	[7]
$R\Theta_{JCBOTTOM}$	Junction to case bottom	–	1.4	°C/W	[8]

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Table 124. Thermal ratings*...continued*

Symbol	Description (rating)	Min	Max	Unit	Notes
ΨJT	Junction to package top • Natural convection	–	1.3	°C/W	[9]

[1] Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See thermal protection thresholds for thermal protection features.
[2] NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to https://www.nxp.com/, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
[3] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
[4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[5] The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
[6] Per JEDEC JESD51-6 with the board horizontal.
[7] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[8] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
[9] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters (Ψ) are not available, the thermal characterization parameter is written as Psi-JT.

9.3 Current consumption

The current consumption of the individual blocks is described in detail in Table 125.

Table 125. Current consumption summary

TA= -40 °C to 105 °C, V_{PWR}= 0 V (External pass FET is not populated), V_{IN} = 3.6 V, V_{DDIO} = 1.7 V to 3.6 V, L_{ICELL} = 1.8 V to 3.3 V, V_{SNVS} = 3.0 V, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{PWR} = 0 V, V_{DDIO} = 3.3 V, L_{ICELL} = 3.0 V, V_{SNVS} = 3.0 V and 25 °C, unless otherwise noted.

Mode	PF3001 conditions	System conditions	Typ.	Max.	Unit	Notes
Coin Cell	VSNVS from LICELL, All other blocks off, V_{IN} = 0.0 V	No load on VSNVS	4.0	7.0	µA	[1] [2]
Off	VSNVS from VIN or LICELL Wake-up from PWRON active 32 kHz RC on All other blocks off VIN ≥ UVDET	No load on VSNVS, PMIC able to wake-up	16	25	µA	[1][2]
On	VSNVS from VIN SW1 in APS SW2 in APS SW3 in APS Trimmed 16 MHz RC enabled Trimmed reference active, VLDO1-4 enabled V33 enabled VCC_SD enabled	No load on any of the regulators.	1.2	–	mA	–

[1] At 25 °C only.
[2] When V_{IN} is below the UVDET threshold, in the range of 1.8 V ≤ V_{IN} < 2.65 V, the quiescent current increases by 50 µA, typically.

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9.4 Electrical characteristics

Table 126. Electrical characteristics – front-end input LDO

All parameters are specified at T_A = -40 °C to 105 °C, V_{PWR} = 5.0 V, V_{IN} = 4.4 V, I_{VIN} = 300 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{PWR} = 5.0 V, V_{IN} = 4.4 V, I_{VIN} = 300 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Front end input LDO (VPWR LDO)						
V_{PWR}	Operating input voltage • In regulation • In dropout operation	4.6 3.7	– –	5.5 4.6	V	[1]
V_{IN}	On mode output voltage, 4.6 V < V_{PWR} < 5.5 V, 0.0 mA < I_{VIN} < 3000 mA	4.3	4.4	4.55	V	–
I_{VIN}	Operating load current at VIN, 3.7 V < V_{PWR} < 5.5 V	0.0	–	3.0	A	–
I_{LDOGQ}	ON mode quiescent current, No load,	–	5.0	10	mA	–
V_{IN}	Low Power mode output voltage, 4.6 V < V_{PWR} < 5.5 V 0.0 mA < I_{VIN} < 1.0 mA	3.7	–	4.5	V	–
$V_{PWROFFMODE}$	Off mode output voltage, (CL = 100 µF) 4.6 V < V_{PWR} < 5.5 V, 0.0 mA < I_{VIN} < 35 µA	3.2	–	4.8	V	–
V_{PWRUV}	VPWR undervoltage threshold (upon undervoltage condition the external pass FET is turned off)	3.1	–	3.7	V	–
V_{PWROV}	VPWR overvoltage threshold (upon overvoltage condition interrupt is asserted at INTB)	5.5	–	6.5	V	–
$I_{VINUVILIMIT}$	VPWR LDO current limit under VIN short-circuit (V_{IN} < UVDET)	–	–	300	mA	–
$I_{VINLEAKAGE}$	Reverse leakage current from VIN to VPWR, No external pass FET, VPWR is grounded, device is in OFF state	–	–	1.0	µA	–
$I_{VPWROFF}$	VPWR LDO Off mode quiescent current	–	–	75	µA	[2]

[1] While the front end LDO can handle spikes up to 7.5 V at VPWR for as long as 200 µs, the circuit is not expected to be continuously operated when VPWR is above 5.5 V.

[2] This specification gives the leakage current in the VPWR LDO block. Total OFF mode current includes the quiescent current from the other blocks as specified in Table 125.

Table 127. Static electrical characteristics – SW1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW1IN} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, typical external component values, f_{SW1} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW1IN} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Switch mode supply SW1						
V_{SW1IN}	Operating input voltage	2.8	–	4.5	V	[1]
V_{SW1}	Nominal output voltage	–	Table 12	–	V	–

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Table 127. Static electrical characteristics – SW1*...continued*

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW1IN} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, typical external component values, f_{SW1} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW1IN} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{SW1ACC}	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW1IN} < 4.5 V, 0 < I_{SW1} < 2.75 A 0.7 V ≤ V_{SW1} ≤ 1.2 V • PFM, APS, 2.8 V < V_{SW1IN} < 4.5 V, 0 < I_{SW1} < 2.75 A 1.225 V < V_{SW1} < 1.425 V • PFM, steady state, 2.8 V < V_{SW1IN} < 4.5 V, 0 < I_{SW1} < 150 mA 1.8 V ≤ V_{SW1} ≤ 1.425 V • PWM, APS, 2.8 V < V_{SW1IN} < 4.5 V, 0 < I_{SW1} < 2.75A 1.8 V < V_{SW1} < 3.3 V • PFM, steady state, 2.8 V < V_{SW1IN} < 4.5 V, 0 < I_{SW1} < 150 mA 1.8 V ≤ V_{SW1} ≤ 3.3 V	 -25 -25 -45 -6.0 -6.0	–	 25 25 45 6.0 6.0	 mV mV mV % %	–
I_{SW1}	Rated output load current, • 2.8 V ≤ V_{SW1IN} ≤ 4.5 V, 0.7 V < V_{SW1} < 1.425 V, 1.8 V, 3.3 V	–	–	2750	mA	–
I_{SW1Q}	Quiescent current • PFM mode • APS mode	 – –	 22 300	 – –	µA	–
I_{SW1LIM}	Current limiter peak current detection, current through inductor • SW1ILM = 0 (default) • SW1ILM = 1	 3.5 2.6	 5.5 4.0	 7.5 5.4	A	–
ΔV_{SW1}	Output ripple	–	5.0	–	mV	–
R_{SW1DIS}	Discharge resistance	–	600	–	Ω	–

[1] The maximum operating input voltage is 4.55 V when VPWR LDO is used.

Table 128. Dynamic electrical characteristics – SW1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW1IN} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, typical external component values, f_{SW1} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW1IN} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW1 (single phase)						
V_{SW1OSH}	Startup Overshoot, I_{SW1} = 0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW1IN} = 4.5 V, V_{SW1} = 1.425 V	–	–	66	mV	–
t_{ONSW1}	Turn-on time, enable to 90 % of end value, I_{SW1} = 0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW1IN} = 4.5 V, V_{SW1} = 1.425 V	–	–	500	µs	–

Table 129. Static electrical characteristics – SW2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW2						
V_{SW2IN}	Operating Input Voltage	2.8	–	4.5	V	[1] [2]

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Table 129. Static electrical characteristics – SW2*...continued*

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{SW2}	Nominal output voltage	–	Table 14	–	V	–
V_{SW2ACC}	Output voltage accuracy • PWM, APS, 2.8 V ≤ V_{SW2IN} ≤ 4.5 V, 0 ≤ I_{SW2} ≤ 1.25 A • 1.50 V ≤ V_{SW2} ≤ 1.85 V • 2.5 V ≤ V_{SW2} ≤ 3.3 V • PFM, 2.8 V ≤ V_{SW2IN} ≤ 4.5 V, 0 ≤ I_{SW2} ≤ 50 mA • 1.50 V ≤ V_{SW2} ≤ 1.85 V • 2.5 V ≤ V_{SW2} ≤ 3.3 V	 -3.0 -6.0 -6.0 -6.0	 – – – –	 3.0 6.0 6.0 6.0	%	–
I_{SW2}	Rated output load current, 2.8 V < V_{SW2IN} < 4.5 V, 1.50 V < V_{SW2} < 1.85 V, 2.5 V < V_{SW2} < 3.3 V	–	–	1250	mA	[3]
I_{SW2Q}	Quiescent current • PFM mode • APS mode (low output voltage settings, CTL_SW2_HL = 0) • APS mode (high output voltage settings, CTL_SW2_HL = 1)	 – – –	 23 145 305	 – – –	µA	–
I_{SW2LIM}	Current limiter peak current detection, current through inductor • SW2ILM = 0 (default) • SW2ILM = 1	 1.625 1.235	 2.5 1.9	 3.375 2.565	A	–
ΔV_{SW2}	Output ripple	–	5.0	–	mV	–
R_{ONSW2P}	SW2 P-MOSFET $R_{DS(on)}$ at V_{IN} = V_{SW2IN} = 3.3 V	–	215	245	mΩ	–
R_{ONSW2N}	SW2 N-MOSFET $R_{DS(on)}$ at V_{SW2IN} = V_{SW2IN} = 3.3 V	–	258	326	mΩ	–
I_{SW2PQ}	SW2 P-MOSFET leakage current, V_{IN} = V_{SW2IN} = 4.5 V	–	–	10.5	µA	–
I_{SW2NQ}	SW2 N-MOSFET leakage current, V_{IN} = V_{SW2IN} = 4.5 V	–	–	3.0	µA	–
R_{SW2DIS}	Discharge resistance during Off mode	–	600	–	Ω	–

[1] The maximum operating input voltage is 4.55 V when VPWR LDO is used.
[2] Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3001 regulator, or external system supply.
[3] The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (V_{SW2IN} - V_{SW2}) = I_{SW2}* (DCR of Inductor +R_{ONSW2P} + PCB trace resistance).

Table 130. Dynamic electrical characteristics – SW2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, ISW2 = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch Mode Supply SW2						
V_{SW2OSH}	Startup overshoot, I_{SW2} = 0.0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW2IN} = 4.5 V	–	–	66	mV	–

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Table 130. Dynamic electrical characteristics – SW2*...continued*

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, ISW2 = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{ONSW2}	Turn-on time, enable to 90 % of end value, I_{SW2} = 0.0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW2IN} = 4.5 V	–	–	500	µs	–

Table 131. Static electrical characteristics – SW3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW3						
V_{SW3IN}	Operating input voltage	2.8	–	4.5	V	[1]
V_{SW3}	Nominal output voltage	–	Table 16	–	V	–
V_{SW3ACC}	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 1.5 A, 0.9 V < V_{SW3} < 1.65 V • PFM, steady state (2.8 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 50 mA), 0.9 V < V_{SW3} < 1.65 V	 -3.0 -6.0	 – –	 -3.0 -6.0	%	–
I_{SW3}	Rated output load current, 2.8 V < V_{SW3IN} < 4.5 V, 0.9 V < V_{SW3} < 1.65 V, PWM, APS mode	–	–	1500	mA	[2]
I_{SW3Q}	Quiescent current • PFM mode • APS mode	 – –	 50 150	 – –	µA	–
I_{SW3LIM}	Current limiter peak current detection, current through inductor • SW3ILIM = 0 (default) • SW3ILIM = 1	 1.95 1.45	 3.0 2.25	 4.05 3.05	A	–
ΔV_{SW3}	Output ripple	–	5.0	–	mV	–
R_{ONSW3P}	SW3 P-MOSFET $R_{DS(on)}$ at V_{IN} = V_{SW3IN} = 3.3 V	–	205	235	mΩ	–
R_{ONSW3N}	SW3 N-MOSFET $R_{DS(on)}$ at V_{IN} = V_{SW3IN} = 3.3 V	–	250	315	mΩ	–
I_{SW3PQ}	SW3 P-MOSFET leakage current, V_{IN} = V_{SW3IN} = 4.5 V	–	–	12	µA	–
I_{SW3NQ}	SW3 N-MOSFET leakage current, V_{IN} = V_{SW3IN} = 4.5 V	–	–	4.0	µA	–
R_{SW3DIS}	Discharge resistance during off mode	–	600	–	Ω	–

[1] The maximum operating input voltage is 4.55 V when VPWR LDO is used.

[2] The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (V_{SW3IN} - V_{SW3}) = I_{SW3}* (DCR of Inductor +R_{ONSW3P} + PCB trace resistance).

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Table 132. Dynamic Electrical Characteristics – SW3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{SW3OSH}	Startup overshoot, I_{SW3} = 0.0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW3IN} = 4.5 V	–	–	66	mV	–
t_{ONSW3}	Turn-on time, enable to 90% of end value, I_{SW3} = 0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW3IN} = 4.5 V	–	–	500	µs	–

Table 133. Static electrical characteristics – VSNVS

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VSNVS						
V_{IN}	Operating input voltage • Valid coin cell range • Valid V_{IN}	 1.8 2.25	 – –	 3.3 4.5	V	[1]
I_{SNVS}	Operating load current, V_{INMIN} < V_{IN} < V_{INMAX}	1.0	–	1000	µA	–
V_{SNVS}	Output voltage • 5.0 µA < I_{SNVS} < 1000 µA (OFF), 3.20 V < V_{IN} < 4.5 V • 5.0 µA < I_{SNVS} < 1000 µA (ON), 3.20 V < V_{IN} < 4.5 V • 5.0 µA < I_{SNVS} < 1000 µA (coin cell mode), 2.84 V < V_{COIN} < 3.3 V	 -5.0 -5.0 V_{COIN} -0.10	 3.0 3.0 –	 7.0 5.0 V_{COIN}	 % % V	–
$V_{SNVSDROP}$	Dropout voltage, 2.85 V < V_{IN} < 2.9 V, 1.0 µA < I_{SNVS} < 1000 µA	–	–	110	mV	–
$I_{SNVSLIM}$	Current limit, V_{IN} > V_{TH1}	1100	–	6750	µA	–
VSNVS DC, switch						
V_{LICELL}	Operating input voltage, valid coin cell range	1.8	–	3.3	V	–
I_{SNVS}	Operating load current	1.0	–	1000	µA	–
$R_{DSONSNVS}$	Internal switch $R_{DS(on)}$, V_{COIN} = 2.6 V	–	–	100	Ω	–

[1] The maximum operating input voltage is 4.55 V when VPWR LDO is used.

Table 134. Dynamic electrical characteristics – VSNVS

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{SNVS} =3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VSNVS						
$V_{SNVSTON}$	Turn-on time (load capacitor, 0.47 µF), from V_{IN} = V_{TH1} to 90 % of V_{SNVS}, V_{COIN} = 0.0 V, I_{SNVS} = 5.0 µA	–	–	24	ms	[1][2]
$V_{SNVSOSH}$	Startup overshoot, I_{SNVS} = 5.0 µA	–	40	70	mV	–

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Table 134. Dynamic electrical characteristics – VSNVS*...continued*

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{SNVS} =3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$V_{SNVSLOTR}$	Transient load response, 3.2 < V_{IN} ≤ 4.5 V, I_{SNVS} = 100 to 1000 µA	2.8	–	–	V	–
V_{TL1}	V_{IN} falling threshold (V_{IN} powered to coin cell powered)	2.45	2.70	3.05	V	–
V_{TH1}	V_{IN} rising threshold (coin cell powered to V_{IN} powered)	2.50	2.75	3.10	V	–
V_{HYST1}	V_{IN} threshold hysteresis for V_{TH1}-V_{TL1}	5.0	–	–	mV	–
$V_{SNVSCROSS}$	Output voltage during crossover, V_{COIN} > 2.9 V, switch to LDO: V_{IN} > V_{TH1}, I_{SNVS} = 100 µA, LDO to switch: V_{IN} < V_{TL1}, I_{SNVS} = 100 µA	2.45	–	–	V	–

[1] The startup of V_{SNVS} is not monotonic. It first rises to 1.0 V and then settles to 3.0 V.
[2] From coin cell insertion to V_{SNVS} = 1.0 V, the delay time is typically 400 ms.

Table 135. Static electrical characteristics – VLDO1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO1 linear regulator						
V_{LDO1IN}	Operating input voltage • 1.8 V ≤ $V_{LDO1NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO1NOM}$ ≤ 3.3 V	2.8 $V_{LDO1NOM}$ +0.250	– –	4.5 4.5	V	[1][2]
$V_{LDO1NOM}$	Nominal output voltage	–	Table 19	–	V	–
I_{LDO1}	Operating load current	0.0	–	100	mA	–
$V_{LDO1TOL}$	Output voltage tolerance, $V_{LDO1INMIN}$ < V_{LDO1IN} < 4.5 V, 0.0 mA < I_{LDO1} < 100 mA, VLDO1 = 1.8 V to 3.3 V	-3.0	–	3.0	%	–
I_{LDO1Q}	Quiescent current, no load, change in I_{VIN}, when VLDO1 enabled	–	13	–	µA	–
$I_{LDO1LIM}$	Current limit, I_{LDO1} when V_{LDO1} is forced to $V_{LDO1NOM}$/2	122	167	280	mA	–

[1] The maximum operating input voltage is 4.55 V when VPWR LDO is used.
[2] Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3001 regulator, or external system supply.

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Table 136. Dynamic electrical characteristics – VLDO1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO1 linear regulator						
$PSRR_{VLDO1}$	PSRR, I_{LDO1} = 75 mA, 20 Hz to 20 kHz • VLDO1 = 1.8 V to 3.3 V, V_{LDO1IN} = $V_{LDO1INMIN}$ + 100 mV • VLDO1 = 1.8 V to 3.3 V, V_{LDO1IN} = $V_{LDO1NOM}$ + 1.0 V	35 52	40 60	– –	dB	–
$NOISE_{VLDO1}$	Output noise density, V_{LDO1IN} = $V_{LDO1INMIN}$, I_{LDO1} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	– – –	-114 -129 -135	-102 -123 -130	dBV/√Hz	–
t_{ONLDO1}	Turn-on time, enable to 90 % of end value, V_{LDO1IN} = $V_{LDO1INMIN}$ to 4.5 V, I_{LDO1} = 0.0 mA, all output voltage settings	60	–	500	µs	–
$t_{OFFLDO1}$	Turn-off time, disable to 10 % of initial value, V_{LDO1IN} = $V_{LDO1INMIN}$, I_{LDO1} = 0.0 mA	–	–	10	ms	–
$LDO1_{OSHT}$	Startup overshoot, V_{LDO1IN} = $V_{LDO1INMIN}$ to 4.5 V, I_{LDO1} = 0.0 mA	–	1.0	2.0	%	–

Table 137. Static electrical characteristics – VLDO2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO2 linear regulator						
V_{LDO2IN}	Operating input voltage	1.75	–	3.40	V	–
$V_{LDO2NOM}$	Nominal output voltage	–	Table 19	–	V	–
I_{LDO2}	Operating load current	0.0	–	250	mA	–
$V_{LDO2TOL}$	Output voltage tolerance, 1.75 V < V_{LDOIN1} < 3.40 V, 0.0 mA < I_{LDO2} < 250 mA, V_{LDO2} = 0.8 V to 1.55 V	-3.0	–	3.0	%	–
I_{LDO2Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO2IN}$, When V_{LDO2} enabled	–	16	–	µA	–
$I_{LDO2LIM}$	Current limit, I_{LDO2} when V_{LDO2} is forced to $V_{LDO2NOM}$/2	333	417	612	mA	–

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Table 138. Dynamic electrical characteristics – VLDO2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO2 linear regulator						
$PSRR_{VLDO2}$	PSRR, I_{LDO2} = 187.5 mA, 20 Hz to 20 kHz • VLDO2 = 0.8 V to 1.55 V • VLDO2 = 1.1 V to 1.55 V	 50 37	 60 45	 – –	dB	–
$NOISE_{VLDO2}$	Output noise density, V_{LDO2IN} = 1.75 V, I_{LDO2} = 187.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -108 -118 -124	 -100 -108 -112	dBV/√Hz	–
t_{ONLDO2}	Turn-on time, enable to 90 % of end value, V_{LDO2IN} = 1.75 V to 3.4 V, I_{LDO2} = 0.0 mA	60	–	500	µs	–
$t_{OFFLDO2}$	Turn-off time, disable to 10 % of initial value, V_{LDO2IN} = 1.75 V, I_{LDO2} = 0.0 mA	–	–	10	ms	–
$LDO2_{OSHT}$	Startup overshoot, V_{LDO2IN} = 1.75 V to 3.4 V, I_{LDO2} = 0.0 mA	–	1.0	2.0	%	–

Table 139. Static electrical characteristics – VCC_SD

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{CC_SD} = 1.85 V, I_{VCC_SD} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{CC_SD} = 1.85 V, I_{VCC_SD} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCC_SD linear regulator						
V_{IN}	Operating input voltage	2.8	–	4.5	V	[1][2][3]
V_{CC_SDNOM}	Nominal output voltage	–	Table 22	–	V	–
I_{VCC_SD}	Operating load current	0.0	–	100	mA	–
V_{CC_SDTOL}	Output voltage accuracy, 2.8 V < V_{IN} < 4.5 V, 0.0 mA < I_{VCC_SD} < 100 mA, VCC_SD[1:0] = 00 to 11	-3.0	–	3.0	%	–
I_{VCC_SDQ}	Quiescent current, no load, change in I_{VIN} and I_{VIN2}, when V_{CC_SD} enabled	–	13	–	µA	–
I_{VCC_SDLIM}	Current limit, I_{VCC_SD} when V_{CC_SD} is forced to $V_{CC_SDNOM}/2$	122	167	280	mA	–

[1] When the LDO output voltage is set above 2.6 V, the minimum allowed input voltage needs to be at least the output voltage plus 0.25 V.
[2] The maximum operating input voltage is 4.55 V when VPWR LDO is used.
[3] Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3001 regulator, or external system supply.

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Table 140. Dynamic electrical characteristics – VCC_SD

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{CC_SD} = 1.85 V, I_{VCC_SD} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{CC_SD} = 1.85 V, I_{VCC_SD} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCC_SD linear regulator						
$PSRR_{VCC_SD}$	PSRR, I_{VCC_SD} = 75 mA, 20 Hz to 20 kHz • VCC_SD[1:0] = 00 - 10, V_{IN} = 2.8 V + 100 mV • VCC_SD[1:0] = 10 - 11, V_{IN} = V_{CC_SDNOM} + 1.0 V	 35 52	 40 60	 – –	dB	–
$NOISE_{VCC_SD}$	Output noise density, V_{IN} = 2.8V, I_{VCC_SD} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	–
t_{ONVCC_SD}	Turn-on time, enable to 90 % of end value, V_{IN} = 2.8 V to 4.5 V, I_{VCC_SD} = 0.0 mA	60	–	500	µs	–
t_{OFFVCC_SD}	Turn-off time, disable to 10 % of initial value, V_{IN} = 2.8 V, I_{VCC_SD} = 0.0 mA	–	–	10	ms	–
V_{CC_SDOSHT}	Startup overshoot, V_{IN} = 2.8 V to 4.5 V, I_{VCC_SD} = 0.0 mA	–	1.0	2.0	%	–

Table 141. Static electrical characteristics – V33

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V33 = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator						
V_{IN}	Operating input voltage, 2.9 V ≤ V_{33NOM} ≤ 3.6 V	2.8	–	4.5	V	[1][2][3]
V_{33NOM}	Nominal output voltage	–	Table 21	–	V	–
I_{V33}	Operating load current	0.0	–	350	mA	–
V_{33TOL}	Output voltage tolerance, 2.8 V < V_{IN} < 4.5 V, 0.0 mA < I_{V33} < 350 mA, V_{33}[1:0] = 00 to 11	-3.0	–	3.0	%	–
I_{V33Q}	Quiescent current, no load, change in I_{VIN}, when V_{33} enabled	–	13	–	µA	–
I_{V33LIM}	Current limit, I_{V33} when V_{33} is forced to V_{33NOM}/2	435	584.5	950	mA	–

[1] When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
[2] The maximum operating input voltage is 4.55 V when VPWR LDO is used.
[3] Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3001 regulator, or external system supply.

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Table 142. Dynamic electrical characteristics – V33

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator						
$PSRR_{V33}$	PSRR, I_{V33} = 262.5 mA, 20 Hz to 20 kHz, V_{33}[1:0] = 00 - 11, V_{IN} = V_{33NOM} + 1.0 V	52	60	–	dB	[1]
$NOISE_{V33}$	Output noise density, VI_N = 2.8 V, I_{V33} = 262.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	–
t_{ONV33}	Turn-on time, enable to 90 % of end value, V_{IN} = 2.8 V, to 4.5 V, I_{V33} = 0.0 mA	60	–	500	µs	–
t_{OFFV33}	Turn-off time, disable to 10 % of initial value, V_{IN} = 2.8 V, I_{V33} = 0.0 mA	–	–	10	ms	–
V_{33OSHT}	Startup overshoot, V_{IN} = 2.8 V to 4.5 V, I_{V33} = 0.0 mA	–	1.0	2.0	%	–

[1] When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.

Table 143. Static electrical characteristics – VLDO3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO3 linear regulator						
$V_{LDO34IN}$	Operating input voltage • 1.8 V ≤ $V_{LDO3NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO3NOM}$ ≤ 3.3 V	2.8 $V_{LDO3NOM}$ +0.250	– –	3.6 3.6	V	[1]
$V_{LDO3NOM}$	Nominal output voltage	–	Table 20	–	V	–
I_{LDO3}	Operating load current	0.0	–	100	mA	–
$V_{LDO3TOL}$	Output voltage tolerance, $V_{LDO34INMIN}$ < $V_{LDO34IN}$ < 4.5 V, 0.0 mA < I_{LDO3} < 100 mA, V_{LDO3} = 1.8 V to 3.3 V	-3.0	–	3.0	%	–
I_{LDO3Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO34IN}$, When V_{LDO3} enabled	–	13	–	µA	–
$I_{LDO3LIM}$	Current limit, I_{LDO3} when V_{LDO3} is forced to $V_{LDO3NOM}$/2	122	167	280	mA	–

[1] Beyond VLDO34IN rating, the ESD protection can be sensitive to voltage transients.

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Table 144. Dynamic electrical characteristics – VLDO3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO3 linear regulator						
$PSRR_{VLDO3}$	PSRR, I_{LDO3} = 75 mA, 20 Hz to 20 kHz • VLDO3 = 1.8 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ + 100 mV • VLDO3 = 1.8 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO3NOM}$ + 1.0 V	35 52	40 60	– –	dB	–
$NOISE_{VLDO3}$	Output noise density, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, I_{LDO3} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	– – –	-114 -129 -135	-102 -123 -130	dBV/√Hz	–
t_{ONLDO3}	Turn-on time, enable to 90 % of end value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ to 4.5 V, I_{LDO3} = 0.0 mA	60	–	500	µs	–
$t_{OFFLDO3}$	Turn-off time, disable to 10 % of initial value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, I_{LDO3} = 0.0 mA	–	–	10	ms	–
$LDO3_{OSHT}$	Startup overshoot, $V_{LDO34IN}$ = $V_{LDO34IN2MIN}$ to 4.5 V, I_{LDO3} = 0.0 mA	–	1.0	2.0	%	–

Table 145. Static electrical characteristics – VLDO4

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO4} = 3.3 V, I_{LDO4} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO4} = 3.3 V, I_{LDO4} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO4 linear regulator						
$V_{LDO34IN}$	Operating input voltage • 1.8 V ≤ $V_{LDO4NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO4NOM}$ ≤ 3.3 V	2.8 $V_{LDO4NOM}$ +0.250	– –	3.6 3.6	V	[1]
$V_{LDO4NOM}$	Nominal output voltage	–	Table 20	–	V	–
I_{LDO4}	Operating load current	0.0	–	350	mA	–
$V_{LDO4TOL}$	Output voltage tolerance, $V_{LDO34INMIN}$ < $V_{LDO34IN}$ < 4.5 V, 0.0 mA < ILDO3 < 100 mA, V_{LDO4} = 1.9 V to 3.3 V	-3.0	–	3.0	%	–
I_{LDO4Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO34IN}$, When V_{LDO4} enabled	–	13	–	µA	–
$I_{LDO4LIM}$	Current limit, I_{LDO4} when V_{LDO4} is forced to $V_{LDO4NOM}$/2	435	584.5	950	mA	–
$PSRR_{VLDO4}$	PSRR, I_{LDO4} = 262.5 mA, 20 Hz to 20 kHz • VLDO4 = 1.9 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ + 100 mV • VLDO4 = 1.9 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO4NOM}$ + 1.0 V	35 52	40 60	– –	dB	–

[1] Beyond VLDO34IN rating, the ESD protection can be sensitive to voltage transients.

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Table 146. Dynamic electrical characteristics – VLDO4

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO4} = 3.3 V, I_{LDO4} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO4} = 3.3 V, I_{LDO4} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO4 linear regulator						
$NOISE_{VLDO4}$	Output noise density, $V_{LDO34IN2}$ = $V_{LDO34INMIN}$, I_{LDO4} = 262.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	–
t_{ONLDO4}	Turn-on time, enable to 90 % of end value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, 4.5 V, I_{LDO4} = 0.0 mA	60	–	500	µs	–
$t_{OFFLDO4}$	Turn-off time, disable to 10 % of initial value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, I_{LDO4} = 0.0 mA	–	–	10	ms	–
$LDO4_{OSHT}$	Startup overshoot, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, 4.5 V, I_{LDO4} = 0.0 mA	–	1.0	2.0	%	–

Table 147. Static electrical characteristics – Coin Cell

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, typical external component values, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Coin cell						
$V_{COINACC}$	Charge voltage accuracy	-100	–	-100	mV	–
$I_{COINACC}$	Charge current accuracy	-30	–	30	%	–
I_{COIN}	Coin cell charge current • I_{COINHI} (in On mode) • I_{COINLO} (in On mode)	 – –	 60 10	 – –	µA	–

Table 148. Static electrical characteristics – Digital I/O

All parameters are specified at T_A = -40 °C to 105 °C, V_{DDIO} = 1.7 V to 3.6 V, V_{PWR} = 0 V (external FET not populated), and typical external component values and full load current range, unless otherwise noted.

Pin Name	Parameter	Load condition	Min.	Max.	Unit	Notes
PWRON	• V_L • V_H	– –	0.0 0.8 * V_{SNVS}	0.2 * V_{SNVS} 3.6	V	–
RESETBMCU	• V_{OL} • V_{OH}	-2.0 mA Open Drain	0.0 0.7 * V_{DDIO}	0.4 * V_{DDIO} V_{DDIO}	V	–
SCL	• V_L • V_H	– –	0.0 0.8 * V_{DDIO}	0.2 * V_{DDIO} 3.6	V	–
SDA	• V_L • V_H • V_{OL} • V_{OH}	– – -2.0 mA Open Drain	0.0 0.8 * V_{DDIO} 0.0 0.7 * V_{DDIO}	0.2 * V_{DDIO} 3.6 0.4 * V_{DDIO} V_{DDIO}	V	–

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Table 148. Static electrical characteristics – Digital I/O*...continued*

All parameters are specified at T_A = -40 °C to 105 °C, V_{DDIO} = 1.7 V to 3.6 V, V_{PWR} = 0 V (external FET not populated), and typical external component values and full load current range, unless otherwise noted.

Pin Name	Parameter	Load condition	Min.	Max.	Unit	Notes
INTB	• V_{OL} • V_{OH}	-2.0 mA Open Drain	0.0 0.7 * V_{DDIO}	0.4 * V_{DDIO} V_{DDIO}	V	–
SD_VSEL	• V_L • V_H	– –	0.0 0.8 * V_{DDIO}	0.2 * V_{DDIO} 3.6	V	–

Table 149. Static electrical characteristics – Internal supplies

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 2.8 V to 4.5 V, LICELL = 1.8 V to 3.3 V, and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCOREDIG (digital core supply)						
$V_{COREDIG}$	Output voltage • On mode • Coin cell mode and Off mode	 – –	 1.5 1.3	 – –	V	[1]
VCORE (analog core supply)						
V_{CORE}	Output voltage • On mode and charging • Coin cell mode and Off mode	 – –	 2.775 0.0	 – –	V	[1]
VCOREREF (bandgap regulator reference)						
$V_{COREREF}$	Output voltage at 25 °C	–	1.2	–	V	[1]
$V_{COREREFACC}$	Absolute trim accuracy	–	0.5	–	%	–
$V_{COREREFTACC}$	Temperature drift	–	0.25	–	%	–

[1] 3.1 V < V_{IN} < 4.5 V, no external loading on VCOREDIG, VCORE, or VCOREREF.

Table 150. Static electrical characteristics – UVDET threshold

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 2.8 V to 4.5 V, LICELL = 1.8 V to 3.3 V, and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{IN} UVDET threshold						
VUVDET	• Rising • Falling	– 2.5	– –	3.1 –	V	–

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10 Typical applications

10.1 Application diagram

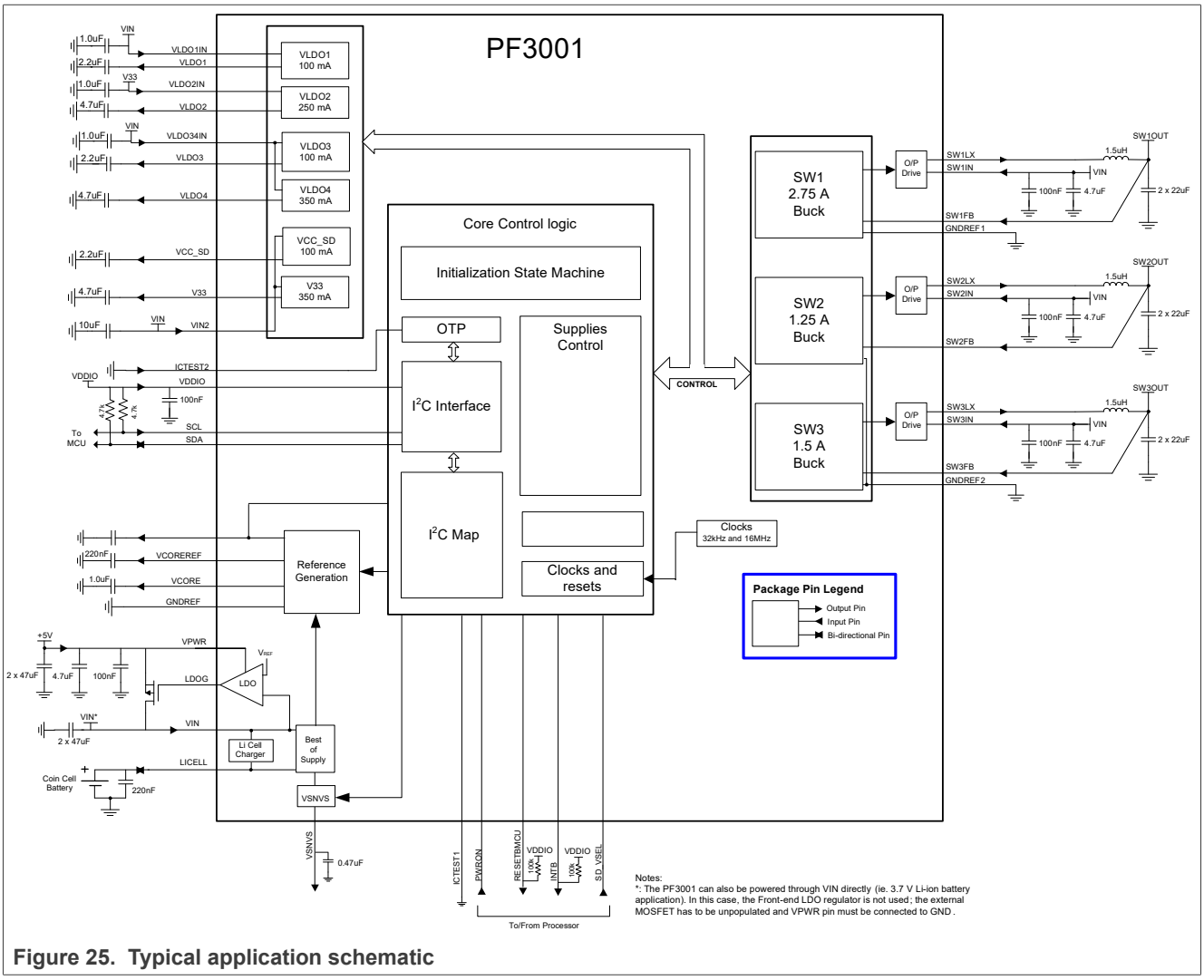


Figure 25. Typical application schematic

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11 Thermal information

11.1 Rating data

The thermal rating data of the packages has been simulated with the results listed in Table 124. Junction-to-ambient thermal resistance nomenclature: the JEDEC specification reserves the symbol $R\theta_{JA}$ or θJA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1 s test board in natural convection environment. $R\theta_{JMA}$ or θJMA (Theta-JMA) is used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1 s and 2s2p test boards. It is anticipated the generic name, Theta-JA, continues to be commonly used. The JEDEC standards can be consulted at https://www.jedec.org/

11.2 Estimation of junction temperature

An estimation of the chip junction temperature T_J can be obtained from the equation:

$T_J = T_A + (R\theta_{JA} \times P_D)$

with:

T_A = Ambient temperature for the package in °C

$R\theta_{JA}$ = Junction to ambient thermal resistance in °C/W

P_D = Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value providing a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board $R\theta_{JA}$ and the value obtained on a four layer board $R\theta_{JMA}$. Actual application PCBs show a performance close to the simulated four layer board value although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

At a known board temperature, the junction temperature T_J is estimated using the following equation

$T_J = T_B + (R\theta_{JB} \times P_D)$ with

TB = Board temperature at the package perimeter in °C

$R\theta_{JB}$ = Junction to board thermal resistance in °C/W

P_D = Power dissipation in the package in W

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made.

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12 Bill of materials

Table 151 provides a complete list of the recommended components on a full featured system using the PF3001 Critical components are provided with a recommended part number; but equivalent components may be used.

Table 151. Bill of materials for -40 °C to 85 °C applications [1]

Value	Qty	Description	Part#	Manufacturer	Component/pin
PMIC					
N/A	1	Power management IC	PF3001	NXP	IC
Buck regulators					
1.5 µH	3	IND PWR 1.5 µH at 1.0 MHz 2.9 A 20 % 2016	DFE252012P-1R5M	Toko Inc.	SW1, SW2, SW3 inductors
		IND PWR 1.5 µH at 1.0 MHz 2.2 A 20 % 1210	BRL3225T1R5M	Taiyo Yuden	Alternate for low power applications
4.7 µF	3	CAP CER 4.7 µF 10 V 20 % X5R 0402	GRM155R61A475MEAA	Murata	SW1, SW2, SW3 input capacitors
0.1 µF	3	CAP CER 0.1 µF 10 V 20 % X5R 0603	GRM033R61A104ME84	Murata	SW1, SW2, SW3 input capacitors (optional)
22 µF	6	CAP CER 22 µF 10 V 20 % X5R 0201	GRM188R61A226ME15	Murata	SW1, SW2, SW3 output capacitors
Linear regulators					
1.0 µF	3	CAP CER 1.0 µF 10 V 20 % X5R 0201	GRM033R61A105ME44	Murata	VLDO1, VLDO2, VLDO3, and VLDO4 input capacitors
2.2 µF	3	CAP CER 2.2 µF 10 V 20 % X5R 0201	GRM033R61A225ME47	Murata	VLDO1, VLDO3, VCC_SD output capacitors
10 µF	1	CAP CER 10 µF 10 V 20 % X7R 0402	GRM155R61A106ME11	Murata	V33 and VCC_SD input capacitor
4.7 µF	3	CAP CER 4.7 µF 10 V 20 % X5R 0402	GRM155R61A475MEAA	Murata	VLDO2, VLDO4, V33 output capacitors
Miscellaneous					
1.0 µF	4	CAP CER 1.0 µF 10 V 20 % X5R 0201	GRM033R61A105ME44	Murata	VCORE, VCOREDIG, capacitors
0.22 µF	2	CAP CER 0.22 µF 10 V 20 % X5R 0201	GRM033R61A224ME90	Murata	VCOREREF and coin cell output capacitors
47 µF	4	CAP CER 47 µF 10 V 20 % X5R 0805	GRM21BR61A476ME15	Murata	Front-end LDO capacitors for VIN and VPWR
2.2 µF	1	CAP CER 2.2 µF 10 V 20 % X5R 0201	GRM033R61A225ME47	Murata	VIN Input Capacitor when not using front-end LDO
0.1 µF	4	CAP CER 0.1 µF 10 V 10 % X5R 0201	GRM033R61A104KE84	Murata	VPWR, VIN Input capacitors (optional)
N/A	1	TRAN PMOS 11 A 12 V 12 SOT-1220	PMPB15XP	NXP	External MOSFET
100 k	2	RES MF 100 K 1/16 W 1 % 0402	RC0402FR-07100KL	Yageo America	Pullup resistor
4.7 k	2	RES MF 4.70 K 1/20 W 1 % 0201	RC0201FR-074K7L	Yageo America	Pullup resistor

[1] NXP does not assume liability, endorse, or warrant components from external manufacturers are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

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Table 152. Bill of materials for -40 °C to 105 °C applications [1]

Value	Qty	Description	Part#	Manufacturer	Component/pin
PMIC					
N/A	1	Power management IC	PF3000	NXP	IC
Buck regulators					
1.5 µH	3	IND PWR 1.5 µH@1 MHz 2.9 A 20 % 2016	DFE201610E-1R5M	Toko Inc.	SW1, SW2, SW3 inductors
		IND PWR 1.5 µH@1 MHz 2.2 A 20 % 1210	BRL3225T1R5M	Taiyo Yuden	Alternate for low power applications
4.7 µF	3	CAP CER 4.7 µF 10 V 10 % X7S 0603	GRM188C71A475KE11	Murata	SW1, SW2, SW3 input capacitors
0.1 µF	3	CAP CER 0.1 µF 10 V 10 % X7S 0201	GRM033C71A104KE14	Murata	SW1, SW2, SW3 input capacitors (optional)
22 µF	6	CAP CER 22 µF 10 V 20 % X7T 0805	GRM21BD71A226ME44	Murata	SW1, SW2, SW3 output capacitors
Linear regulators					
1.0 µF	3	CAP CER 1.0 µF 10 V 10 % X7S 0402	GRM155C71A105KE11	Murata	VLDO1, VLDO2, VLDO3 and VLDO4 input capacitors
2.2 µF	3	CAP CER 2.2 µF 10 V 10 % X7S 0402	GRM155C71A225KE11	Murata	VLDO1, VLDO3, VCC_SD output capacitors
10 µF	1	CAP CER 10 µF 10 V 20 % X7T 0603	GRM188D71A106MA73	Murata	V33 and VCC_SD input capacitor
4.7 µF	3	CAP CER 4.7 µF 10 V 10 % X7S 0603	GRM188C71A475KE11	Murata	VLDO2, VLDO4, V33 output capacitors
1.0 µF	4	CAP CER 1.0 µF 10 V 10 % X7R 0402	GRM155C71A105KE11	Murata	VCORE, VCOREDIG capacitors
0.22 µF	2	CAP CER 0.22 µF 10 V 10 % X7R 0402	GRM155R71A224KE01	Murata	VCOREREF and coin cell output capacitors
47 µF	4	CAP CER 47 µF 10 V 20 % X7R 1210	GRM32ER71A476ME15	Murata	Front-end LDO capacitors for VIN and VPWR.
2.2 µF	1	CAP CER 2.2 µF 10 V 10 % X7S 0402	GRM155C71A225KE11	Murata	VIN Input Capacitor when not using front-end LDO
0.1 µF	4	CAP CER 0.1 µF 10 V 10 % X7S 0201	GRM033C71A104KE14	Murata	VPWR, VIN input capacitors (optional)
N/A	1	TRAN PMOS 11 A 12 V 12 SOT-1220	PMPB15XP	NXP	External MOSFET
100 k	2	RES MF 100 K 1/16 W 1 % 0402	RC0402FR-07100KL	Yageo America	Pull-up resistors
4.7 k	2	RES MF 4.70 K 1/20 W 1 % 0201	RC0201FR-074K7L	Yageo America	I^2C pull-up resistors

[1] NXP does not assume liability, endorse, or warrant components from external manufacturers are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

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13 Simplified application diagram

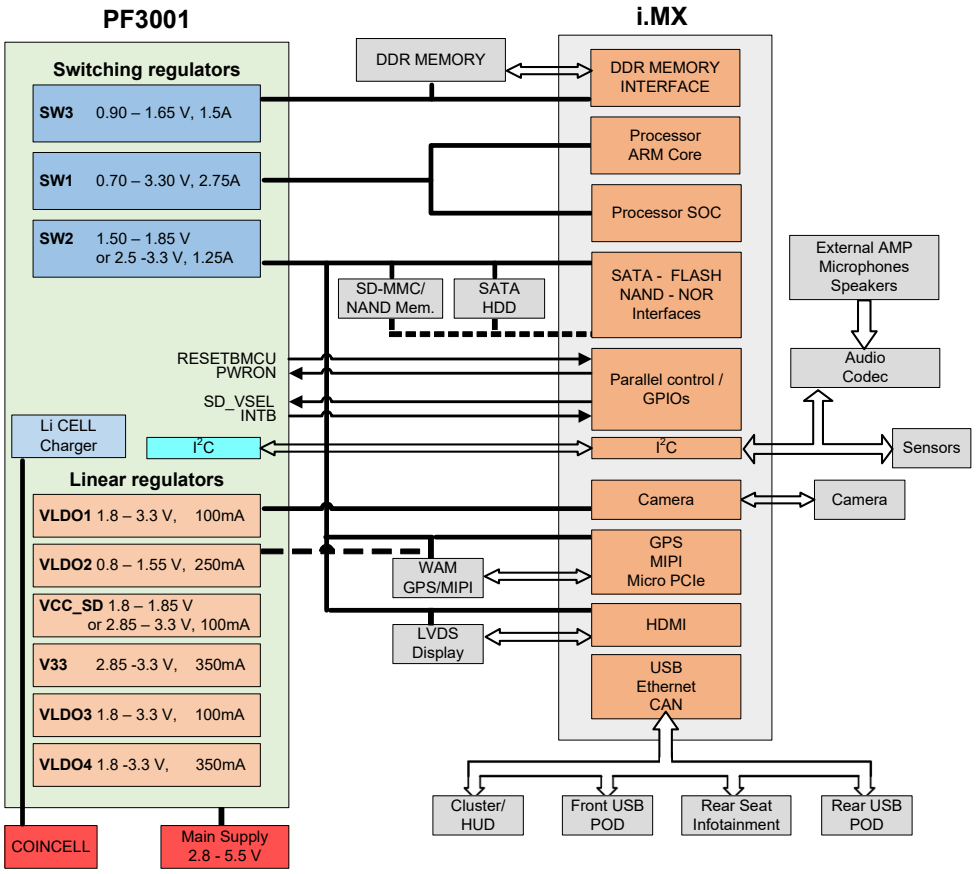


Figure 26. PF3001 simplified application diagram

14 Package information

14.1 Package outline

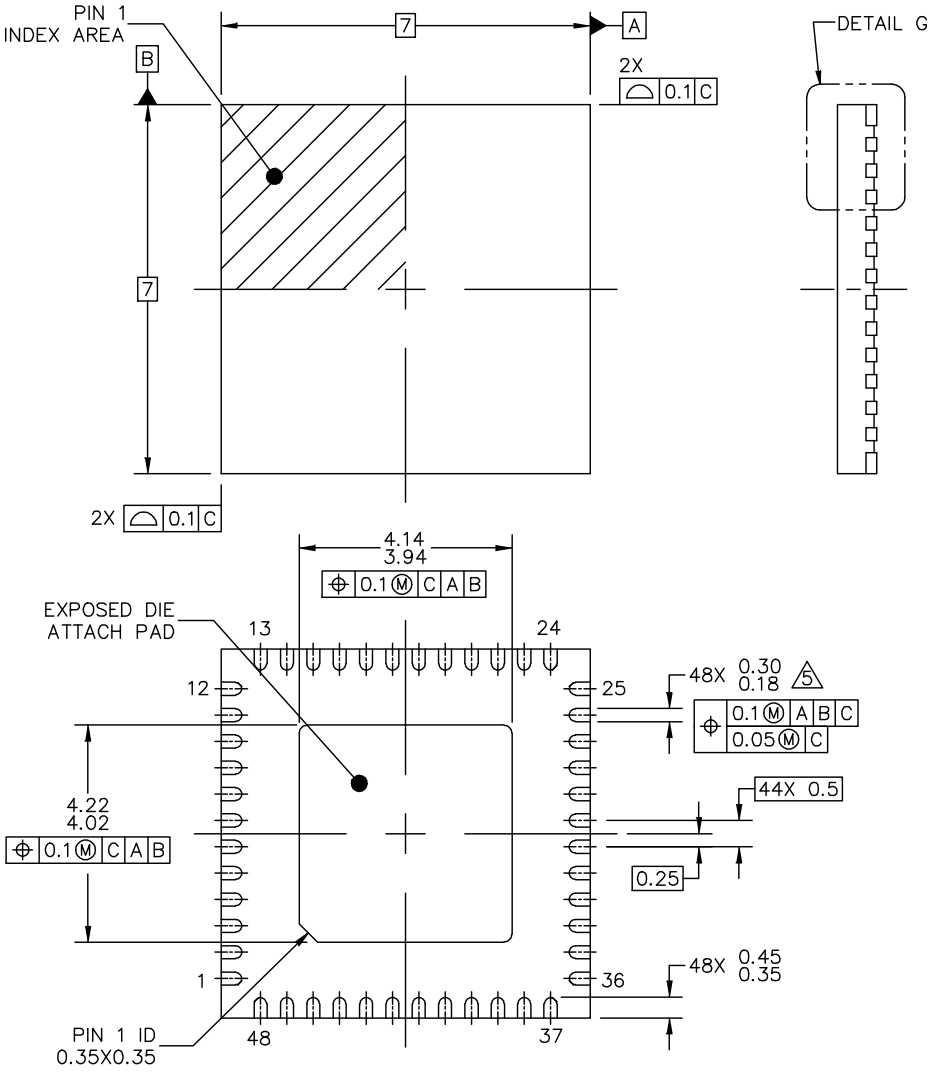
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to https://www.nxp.com/ and perform a keyword search for the drawing's document number. See Section 9.2 for specific thermal characteristics for each package.

Table 153. Package drawing information

Package	Suffix	Package outline drawing number
48-pin QFN 7.0 mm X 7.0 mm - 0.5 mm pitch	EP	98ASA00719D
48 QFN 7.0 mm x 7.0 mm WF-type (wettable flank)	ES	98ASA00933D

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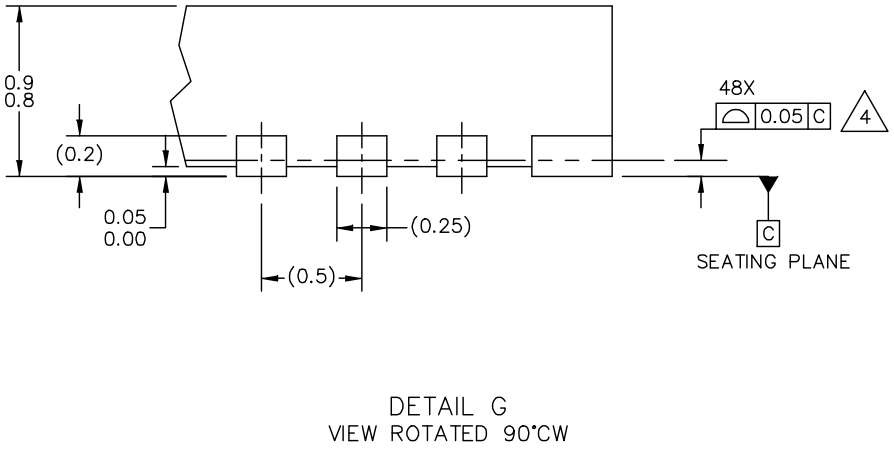


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Figure 27. SOT619-18 (98ASA00719D)

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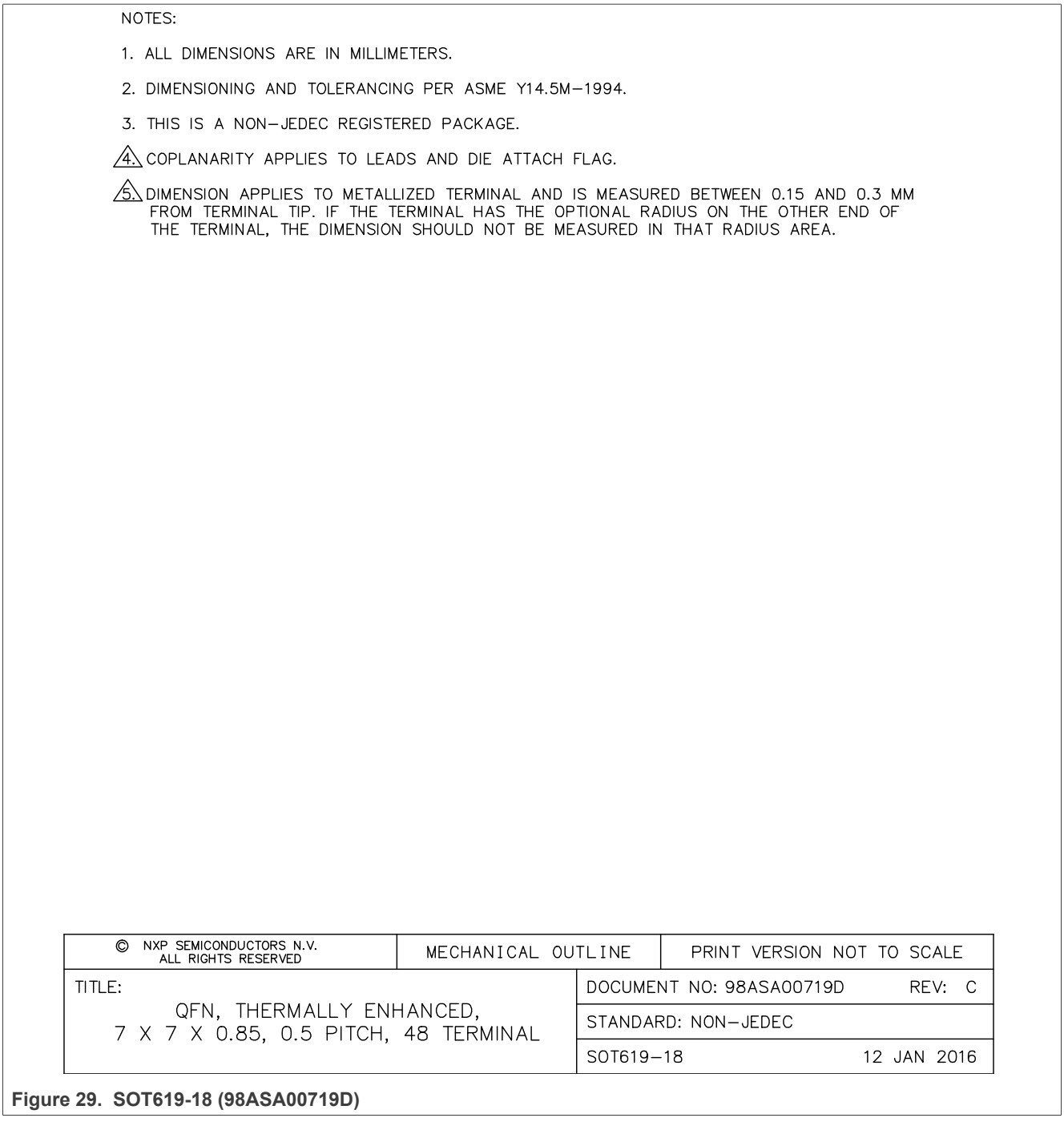
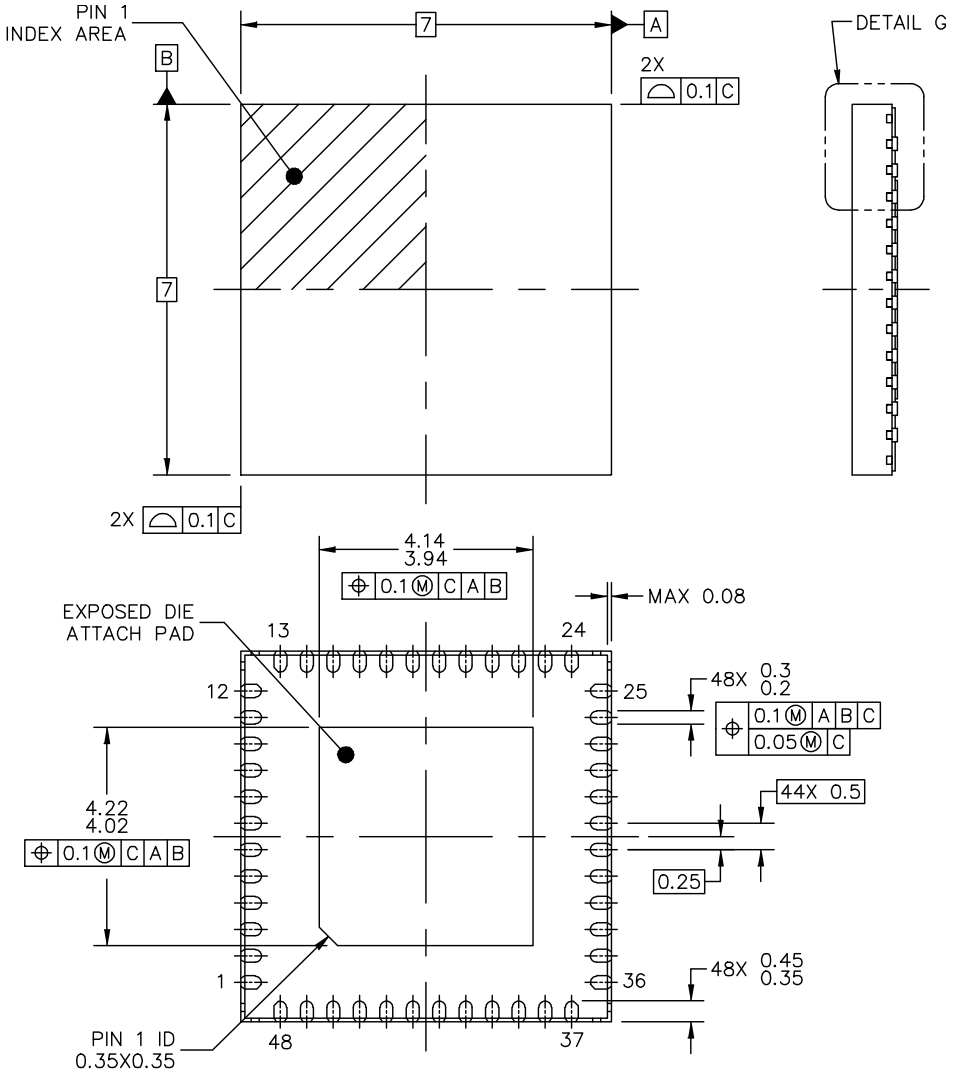


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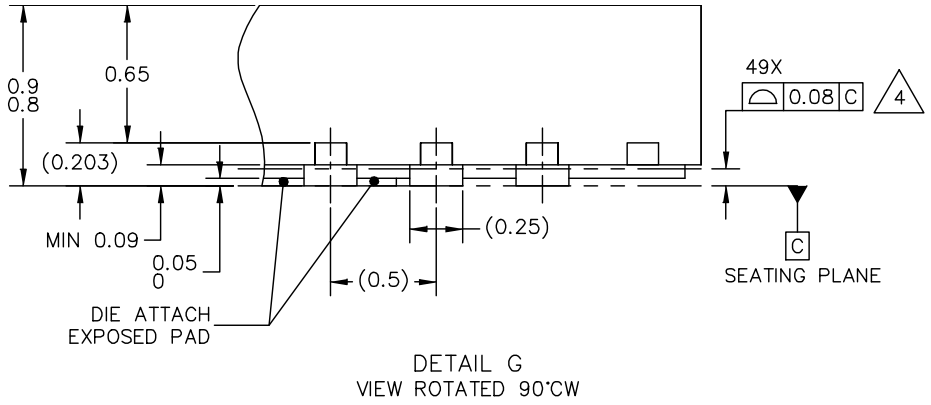


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Figure 30. SOT619-23 (98ASA00933D)

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Figure 31. SOT619-23 (98ASA00933D)

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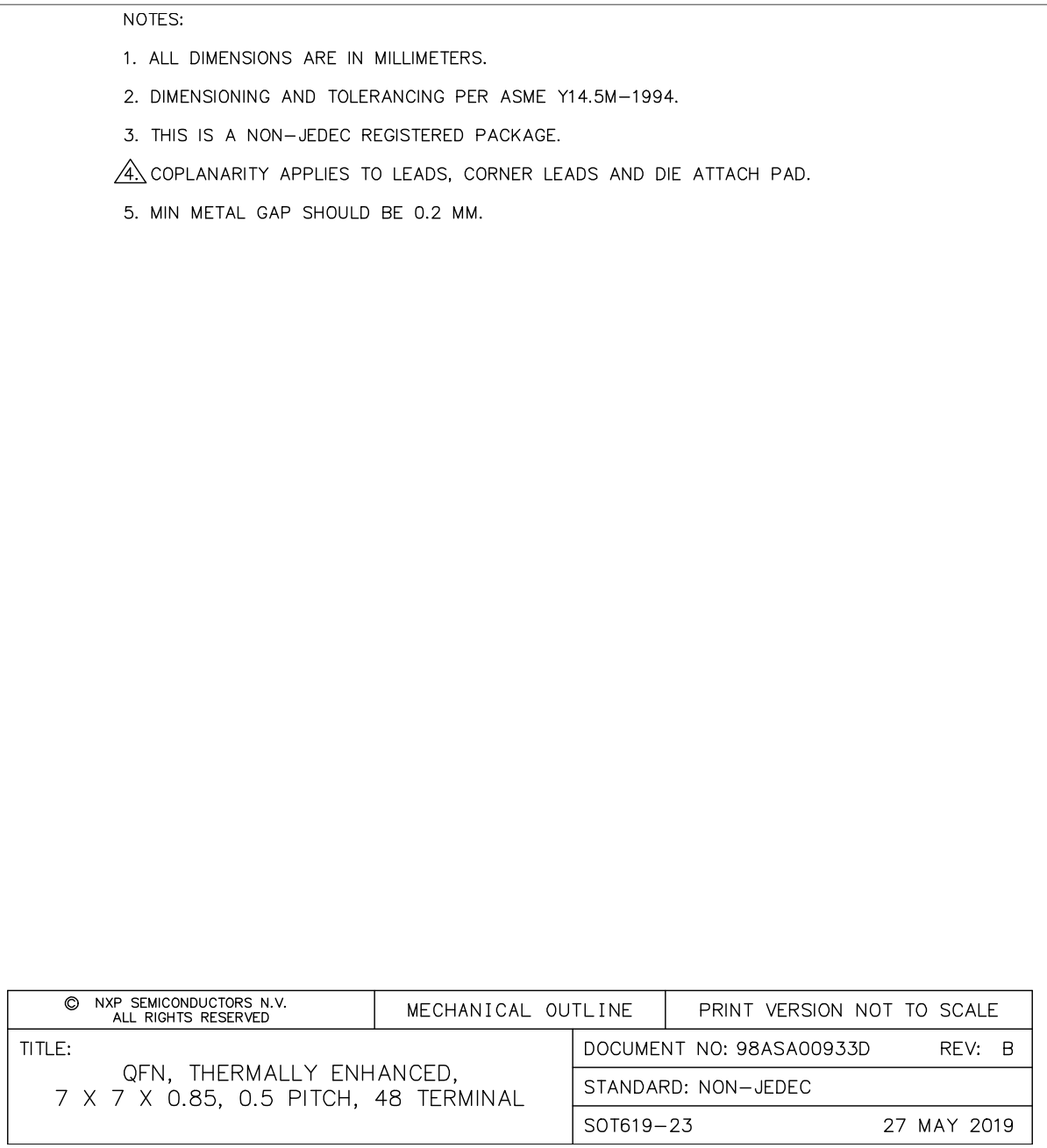


Figure 32. SOT619-23 (98ASA00933D)

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15 Revision history

Table 154. Revision history

Document ID	Release date	Description
PF3001 v.5.1	16 June 2026	• Added back ~EP parts in Table 1 • Added footnote [2] in Table 1 • Added back ~EP package information and drawings in Package outline
PF3001 v.5.0	05 March 2026	• Updated as per Device Migration 202603034DM01 • Updated template to meet our new standards • Replaced master for controller • Replaced slave for follower • Updated Table 1 • Removed EP in Table 153 • Updated package drawings in Section 14.1
4.0	8/2017	• Updated footnotes [1] in Table 144 and [1] in Table 146 as per CIN 201707041I
3.0	4/2017	• Corrected typo in Figure 26 • Updated Table 35 (changed default value to 1)
2.0	3/2016	• Added 98ASA00933D and the page 1 package image for wettable flank • Changed Table 2, pins 7, 10, 18, and 28, from Bypass with at least a 10 µF to Bypass with at least a 4.7 µF • Added PC33PF3001A6ES and PC33PF3001A7ES to Table 1
		• Changed PC33PF3001A6ES and PC33PF3001A7ES to MC parts in Table 1
1.0	8/2015	• Initial release
	9/2015	• Corrected package image on page 1

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Tables

Tab. 1. Orderable part variations 2
Tab. 2. Pin descriptions 7
Tab. 3. PF3001 power tree 9
Tab. 4. Startup configuration 11
Tab. 5. Input LDO external components 15
Tab. 6. SWx regulators external components 16
Tab. 7. Switching mode description 16
Tab. 8. Regulator mode control 16
Tab. 9. Regulator phase clock selection 17
Tab. 10. Optimum phasing 18
Tab. 11. Regulator frequency configuration 18
Tab. 12. SW1 output voltage configuration 18
Tab. 13. SW1 register summary 19
Tab. 14. SW2 output voltage configuration 20
Tab. 15. SW2 register summary 20
Tab. 16. SW3 output voltage configuration 20
Tab. 17. SW3 register summary 21
Tab. 18. LDO external components 21
Tab. 19. VLDO1, VLDO2 output voltage configuration 22
Tab. 20. VLDO3, VLDO4 output voltage configuration 22
Tab. 21. V33 output voltage configuration 23
Tab. 22. VCC_SD output voltage configuration 23
Tab. 23. LDO control 23
Tab. 24. SNVS Modes of Operation 24
Tab. 25. Register VSNVSCTL - ADDR 0x6B 25
Tab. 26. VSNVS external components 25
Tab. 27. Coin cell charger voltage 25
Tab. 28. Register COINCTL – ADDR 0x1A 26
Tab. 29. Coin cell charger external components 26
Tab. 30. Thermal protection thresholds 26
Tab. 31. State machine flow summary 28
Tab. 32. Interrupt, Mask, and Sense Bits 36
Tab. 33. Register INTSTAT0 – ADDR 0x05 37
Tab. 34. Register INTMASK0 – ADDR 0x06 37
Tab. 35. Register INTSENSE0 – ADDR 0x07 37
Tab. 36. Register INTSTAT1 – ADDR 0x08 38
Tab. 37. Register INTMASK1 – ADDR 0x09 38
Tab. 38. Register INTSENSE1 – ADDR 0x0A 38
Tab. 39. Register INTSTAT3 – ADDR 0x0E 39
Tab. 40. Register INTMASK3 – ADDR 0x0F 39
Tab. 41. Register INTSENSE3 – ADDR 0x10 39
Tab. 42. Register INTSTAT4 – ADDR 0x11 39
Tab. 43. Register INTMASK4 – ADDR 0x12 40
Tab. 44. Register INTSENSE4 – ADDR 0x13 40
Tab. 45. Register DEVICEID – ADDR 0x00 41
Tab. 46. Register SILICON REV– ADDR 0x03 41
Tab. 47. Register FABID – ADDR 0x04 41
Tab. 48. Register MEMA – ADDR 0x1C 41
Tab. 49. Register MEMB – ADDR 0x1D 41
Tab. 50. Register MEMC – ADDR 0x1E 42
Tab. 51. Register MEMD – ADDR 0x1F 42
Tab. 52. Status interrupt register 0 (INTSTAT0) 42
Tab. 53. INTSTAT0 field descriptions 42
Tab. 54. Interrupt status mask register 0 (INTMASK0) 43
Tab. 55. INTMASK0 field descriptions 43
Tab. 56. Interrupt sense register 0 (INTSENSE0) 44
Tab. 57. INTSENSE0 field descriptions 44
Tab. 58. Status interrupt register 1 (INTSTAT1) 45
Tab. 59. INTSTAT1 field descriptions 45
Tab. 60. Interrupt status mask register 1 (INTMASK1) 45
Tab. 61. INTMASK1 field descriptions 46
Tab. 62. Interrupt sense register 1 (INTSENSE1) 46
Tab. 63. INTSENSE1 field descriptions 46
Tab. 64. Status Interrupt Register 3 (INTSTAT3) 47
Tab. 65. INTSTAT3 field descriptions 47
Tab. 66. Interrupt status mask register 3 (INTMASK3) 47
Tab. 67. INTMASK3 field descriptions 47
Tab. 68. Interrupt sense register 3 (INTSENSE3) 48
Tab. 69. INTSENSE3 field descriptions 48
Tab. 70. Status interrupt register 4 (INTSTAT4) 48
Tab. 71. INTSTAT4 field descriptions 49
Tab. 72. Interrupt status mask register 4 (INTMASK4) 49
Tab. 73. INTMASK4 field descriptions 49
Tab. 74. Interrupt sense register 4 (INTSENSE4) 50
Tab. 75. INTSENSE4 Field Descriptions 50
Tab. 76. Coin cell control register (COINCTL) 51
Tab. 77. COINCTL field descriptions 51
Tab. 78. Power control register (PWRCTL) 51
Tab. 79. PWRCTL field descriptions 52
Tab. 80. Embedded memory register A (MEMA) 52
Tab. 81. MEMA field descriptions 52
Tab. 82. Embedded memory register B (MEMB) 52
Tab. 83. MEMB field descriptions 53
Tab. 84. Embedded Memory Register C (MEMC) 53
Tab. 85. MEMC field descriptions 53
Tab. 86. Embedded memory register D (MEMD) 53
Tab. 87. MEMD field descriptions 53
Tab. 88. SW1 voltage control register (SW1VOLT) 54
Tab. 89. SW1VOLT field descriptions 54
Tab. 90. SW1 switching mode selector register (SW1MODE) 54
Tab. 91. SW1MODE field descriptions 54
Tab. 92. SW1A configuration register (SW1CONF) 55
Tab. 93. SW1ACONF field descriptions 55
Tab. 94. SW2 voltage control register (SW2VOLT) 55
Tab. 95. SW2VOLT field descriptions 55
Tab. 96. SW2 Switching mode selector register (SW2MODE) 56
Tab. 97. SW2MODE field descriptions 56
Tab. 98. SW2 configuration register (SW2CONF) 56
Tab. 99. SW2CONF field descriptions 56
Tab. 100. SW3 voltage control register (SW3VOLT) 57
Tab. 101. SW3VOLT field descriptions 57
Tab. 102. SW3 Switching mode selector register (SW3MODE) 57

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Tab. 103. SW3MODE field descriptions 57
Tab. 104. SW3 configuration register (SW3CONF) 58
Tab. 105. SW3CONF field descriptions 58
Tab. 106. VSNVS control register (VSNVSCTL) 58
Tab. 107. VSNVSCTL field descriptions 59
Tab. 108. VLDO1 control register (VLDO1CTL) 59
Tab. 109. VLDO1CTL field descriptions 59
Tab. 110. VLDO2 control register (VLDO2CTL) 59
Tab. 111. VLDO2CTL field descriptions 60
Tab. 112. CC_SD control register (VCC_SDCTL) 60
Tab. 113. VCC_SDCTL field descriptions 60
Tab. 114. V33 control register (V33CTL) 60
Tab. 115. V33CTL field descriptions 61
Tab. 116. VLDO3 control register (VLDO3CTL) 61
Tab. 117. VLDO3CTL field descriptions 61
Tab. 118. VLDO4 control register (VLDO4CTL) 61
Tab. 119. VLDO4CTL field descriptions 62
Tab. 120. Page selection register 62
Tab. 121. Page register field descriptions 62
Tab. 122. Functional page 63
Tab. 123. Maximum voltage ratings 66
Tab. 124. Thermal ratings 66
Tab. 125. Current consumption summary 67
Tab. 126. Electrical characteristics – front-end input LDO 68
Tab. 127. Static electrical characteristics – SW1 68
Tab. 128. Dynamic electrical characteristics – SW1 69
Tab. 129. Static electrical characteristics – SW2 69
Tab. 130. Dynamic electrical characteristics – SW2 70
Tab. 131. Static electrical characteristics – SW3 71
Tab. 132. Dynamic Electrical Characteristics – SW3 72
Tab. 133. Static electrical characteristics – VSNVS 72
Tab. 134. Dynamic electrical characteristics – VSNVS 72
Tab. 135. Static electrical characteristics – VLDO1 73
Tab. 136. Dynamic electrical characteristics – VLDO1 74
Tab. 137. Static electrical characteristics – VLDO2 74
Tab. 138. Dynamic electrical characteristics – VLDO2 75
Tab. 139. Static electrical characteristics – VCC_SD 75
Tab. 140. Dynamic electrical characteristics – VCC_SD 76
Tab. 141. Static electrical characteristics – V33 76
Tab. 142. Dynamic electrical characteristics – V33 77
Tab. 143. Static electrical characteristics – VLDO3 77
Tab. 144. Dynamic electrical characteristics – VLDO3 78
Tab. 145. Static electrical characteristics – VLDO4 78
Tab. 146. Dynamic electrical characteristics – VLDO4 79
Tab. 147. Static electrical characteristics – Coin Cell 79
Tab. 148. Static electrical characteristics – Digital I/O 79
Tab. 149. Static electrical characteristics – Internal supplies 80
Tab. 150. Static electrical characteristics – UVDET threshold 80
Tab. 151. Bill of materials for -40 °C to 85 °C applications 83
Tab. 152. Bill of materials for -40 °C to 105 °C applications 84
Tab. 153. Package drawing information 85
Tab. 154. Revision history 92

Figures

Fig. 1. PF3001 simplified internal block diagram 4
Fig. 2. PF3001 functional block diagram 5
Fig. 3. Pinning diagram 6
Fig. 4. PF3001 typical power map 10
Fig. 5. Startup timing diagram 13
Fig. 6. Front-end LDO block diagram 14
Fig. 7. Generic SWx block diagram 15
Fig. 8. Voltage stepping with fixed DVS 17
Fig. 9. General LDO block diagram 21
Fig. 10. VSNVS supply switch architecture 24
Fig. 11. State diagram 27
Fig. 12. Startup sequence 29
Fig. 13. Load transient response – LDO2 29
Fig. 14. Load transient response – LDO1, LDO3, and VCC_SD 30
Fig. 15. Load transient response – LDO4 and V33 30
Fig. 16. Load transient response – buck regulators 31
Fig. 17. Quiescent current – LDOs 31
Fig. 18. Load regulation – LDOs 32
Fig. 19. Dropout voltage – VLDO1, VLDO3, VCC_SD - VOUT = 3.3 V 32
Fig. 20. Dropout voltage – VLDO1, VLDO3,VCC_SD - VOUT = 1.8 V 33
Fig. 21. Dropout voltage – VLDO4, V33 - VOUT = 3.3 V 33
Fig. 22. Dropout voltage – VLDO4 - VOUT = 1.8 V 34
Fig. 23. I2C write example 35
Fig. 24. I2C read example 35
Fig. 25. Typical application schematic 81
Fig. 26. PF3001 simplified application diagram 85
Fig. 27. SOT619-18 (98ASA00719D) 86
Fig. 28. SOT619-18 (98ASA00719D) 87
Fig. 29. SOT619-18 (98ASA00719D) 88
Fig. 30. SOT619-23 (98ASA00933D) 89
Fig. 31. SOT619-23 (98ASA00933D) 90
Fig. 32. SOT619-23 (98ASA00933D) 91

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Contents

1 General description 1
2 Features and benefits 1
3 Applications 2
4 Ordering information 2
5 Internal block diagram 4
6 Functional block diagram 5
7 Pinning information 6
7.1 Pinning diagram 6
7.2 Pin descriptions 7
8 Functional description 9
8.1 Introduction 9
8.2 Power generation 9
8.3 Functional description 11
8.3.1 Control logic and interface signals 11
8.3.1.1 PWRON 11
8.3.1.2 RESETBMCU 11
8.3.1.3 INTB 11
8.3.1.4 SD_VSEL 11
8.3.2 Startup 11
8.3.3 Startup timing diagram 13
8.3.4 16 MHz and 32 kHz clocks 13
8.3.5 Optional front-end input LDO regulator 14
8.3.5.1 LDO regulator description 14
8.3.5.2 Undervoltage/short-circuit and overvoltage detection 14
8.3.5.3 External components 15
8.3.6 Internal core voltages 15
8.3.7 Buck regulators 15
8.3.7.1 Switching modes 16
8.3.7.2 Dynamic voltage scaling 17
8.3.7.3 Regulator phase clock 17
8.3.7.4 SW1 18
8.3.7.5 SW1 setup and control registers 18
8.3.7.6 SW2 setup and control registers 20
8.3.7.7 SW3 setup and control registers 20
8.3.7.8 LDO regulators description 21
8.3.7.9 VSNVS LDO/switch 24
8.4 Power dissipation 26
8.5 Modes of operation 27
8.5.1 State diagram 27
8.5.1.1 On mode 27
8.5.1.2 Off mode 27
8.5.1.3 PWRON pin 28
8.5.1.4 Thermal protection 28
8.5.1.5 Coin cell mode 28
8.5.2 State machine flow summary 28
8.5.3 Performance characteristics curves 29
8.6 Control interface I2C block description 34
8.6.1 I2C device ID 34
8.6.2 I2C operation 34
8.6.3 Interrupt handling 35
8.6.4 Interrupt bit summary 36
8.6.5 Specific registers 41
8.6.5.1 IC and version identification 41
8.6.5.2 Embedded memory 41
8.6.5.3 Register descriptions 42
8.6.6 Register map 63
8.6.6.1 Register map 63
9 General product characteristics 66
9.1 Maximum ratings 66
9.2 Thermal characteristics 66
9.3 Current consumption 67
9.4 Electrical characteristics 68
10 Typical applications 81
10.1 Application diagram 81
11 Thermal information 82
11.1 Rating data 82
11.2 Estimation of junction temperature 82
12 Bill of materials 83
13 Simplified application diagram 85
14 Package information 85
14.1 Package outline 85
15 Revision history 92
Legal information 93

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