适用于成本优化型系统的 TLV854x 500nA RRIO 纳瓦级功率运算放大器

1 特性

- 对于成本优化型系统
- 纳瓦级功率电源电流：500nA/通道
- 失调电压：3.1mV（最大值）
- TcVos：0.8µV/°C
- 增益带宽：8kHz
- 单位增益稳定
- 低输入失调电流：100fA
- 宽电源电压范围：1.7V 至 3.6V
- 轨至轨输入和输出 (RRIO)
- 温度范围：–40°C 至 +125°C
- 行业标准封装
  - 四通道 14 引脚 TSSOP 和 SOIC 封装
  - 双通道 8 引脚 SOIC 封装
  - 单通道 5 引脚 SOT-23 封装
- 无引线封装
  - 双通道 8 引脚 X2QFN 封装

2 应用

- 使用 PIR 传感器的运动检测器 SNAA301
- 使用微波传感器的运动检测器
- 气体检测器
- 离子化烟雾报警器
- 温度调节装置
- 远程传感器、IoT（物联网）
- 有效的射频识别 (RFID) 阅读器和标签
- 便携式医疗设备
- 血糖监测

3 说明

TLV854x 超低功耗运算放大器适用于无线和低功耗有线设备中的 成本优化型 传感应用。TLV854x 系列运算放大器可最大限度地减少极其注重电池使用寿命的运动检测安全系统（如微波和 PIR 运动传感系统）等设备的功耗。此类器件的互补金属氧化物半导体 (CMOS) 输入级经过精心设计，能够实现超低飞安级失调电流，从而降低 I_{BIAS} 和 I_{OS} 误差，否则会影响敏感 应用。这些方面的示例包括带有兆欧级反馈电阻器的跨阻放大器 (TIA) 配置以及高源阻抗传感 应用。此外，内置的 EMI 保护可降低器件对手机、WiFi、无线电发射器和标签阅读器等发出的无用射频信号的敏感度。

器件信息(1)

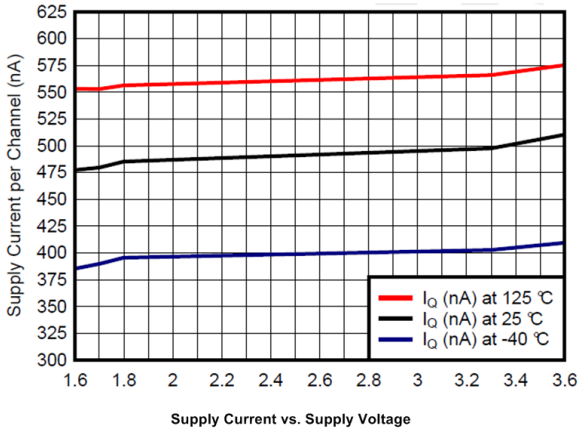
器件型号	封装	封装尺寸
TLV8544	TSSOP封装(14)	5.00mm x 4.40mm
	SOIC (14)（预览）	8.65mm × 3.91mm
TLV8542	SOIC (8)	4.9mm × 3.90mm
	X2QFN (8)（预览）	1.50mm × 1.50mm
TLV8541	SOT-23 (5)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

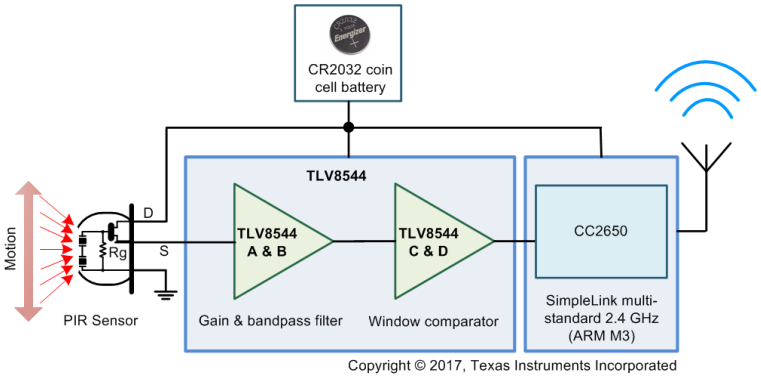
纳瓦级功率放大器系列

系列	通道数	每通道的 I_Q	V_{OS}（最大值）	V_{SUPPLY}
TLV854x	1、2、4	500nA	3.1mV	1.7 至 3.6V
TLV880x	1、2	320nA	4.5mV	1.7 至 5.5V
LPV81x	1、2	425nA	0.3mV	1.6 至 5.5V

低功耗 **PIR** 运动检测器



Supply Current vs. Supply Voltage



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4 修订历史记录

Changes from Revision C (October 2017) to Revision D — **Page**

- TLV8541 的生产数据发布 ... 1
- 为 TLV8542 添加了 8 引脚 X2QFN 封装 ... 1

Changes from Revision B (June 2017) to Revision C — **Page**

- 已更改 将 TLV8542 双通道数据表更改为生产数据 ... 1

Changes from Revision A (March 2017) to Revision B — **Page**

- 已添加 向 TLV8544 数据表中添加预告信息 TLV8542 ... 1

Changes from Original (December 2016) to Revision A — **Page**

- 已更改 将“产品预览”更改为“生产数据”发布。 ... 1

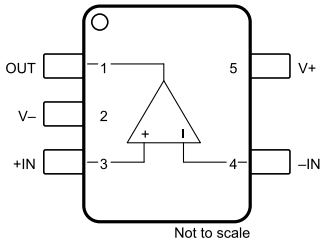
5 说明 （续）

TLV854x 运算放大器采用低至 1.7V 的单电源电压供电，并且可在 –40°C 至 +125°C 的扩展温度范围内、在低电量情况下连续运行。所有版本的额定工作温度范围均为 –40°C 至 125°C。TLV8541（单通道版本）采用 5 引脚 SOT-23 封装，而 TLV8542（双通道版本）采用 8 引脚 SOIC 封装。四通道 TLV8544（四通道版本）采用行业标准 14 引脚 TSSOP 封装。

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6 Pin Configuration and Functions

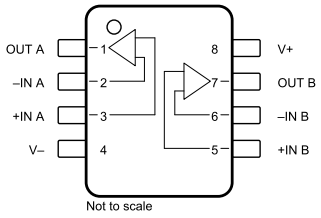
TLV8541 DBV Package
5-Pin SOT-23
Top View



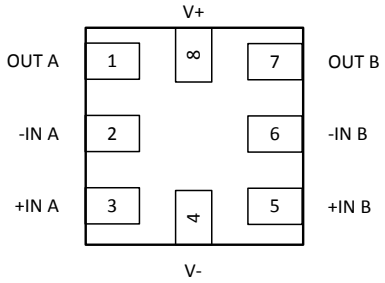
Pin Functions: TLV8541 DBV

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT	O	Output
2	V–	P	Negative (lowest) power supply
3	+IN	I	Non-Inverting Input
4	–IN	I	Inverting Input
5	V+	P	Positive (highest) power supply

TLV8542 D Package
8-Pin SOIC
Top View



TLV8542 RUG Package
8-Pin X2QFN
Top View

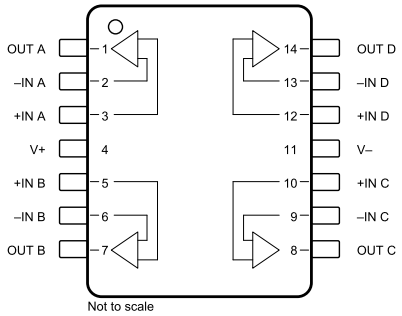


Pin Functions: TLV8542 D (X2QFN RUG Package Preview)

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT A	O	Channel A Output
2	–IN A	I	Channel A Inverting Input
3	+IN A	I	Channel A Non-Inverting Input
4	V–	P	Negative (lowest) power supply
5	+IN B	I	Channel B Non-Inverting Input
6	–IN B	I	Channel B Inverting Input
7	OUT B	O	Channel B Output
8	V+	P	Positive (highest) power supply

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TLV8544 PW and D Package
14-Pin TSSOP and SOIC
Top View



Pin Functions: TLV8544 PW (D SOIC Package Preview)

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUTA	O	Channel A output
2	–INA	I	Channel A inverting input
3	+INA	I	Channel A non-inverting input
4	V+	P	Positive (highest) power supply
5	+INB	I	Channel B non-inverting input
6	–INB	I	Channel B inverting input
7	OUTB	O	Channel B output
8	OUTC	O	Channel C output
9	–INC	I	Channel C inverting input
10	+INC	I	Channel C non-inverting input
11	V–	P	Negative (lowest) power supply
12	+IND	I	Channel D non-inverting input
13	–IND	I	Channel D inverting input
14	OUTD	O	Channel D output

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)			–0.3	4	V
Input pins	Voltage	Common mode	(V–) – 0.3	(V+) + 0.3	V
		Differential	(V–) – 0.3	(V+) + 0.3	V
Input pins	Current		–10	10	mA
Output short current (4)			Continuous	Continuous	
Operating ambient temperature			–40	125	°C
Storage temperature, T_{stg}			–65	150	°C
Junction temperature				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Short-circuit to ground.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	1.7		3.6	V
Specified ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TLV8544 PW (TSSOP) 14 PINS	TLV8542 D (SOIC) 8 PINS	TLV8541 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	141.6	244.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.7	85.7	127.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.2	84.7	79.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.3	36.3	44.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.7	84.0	78.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

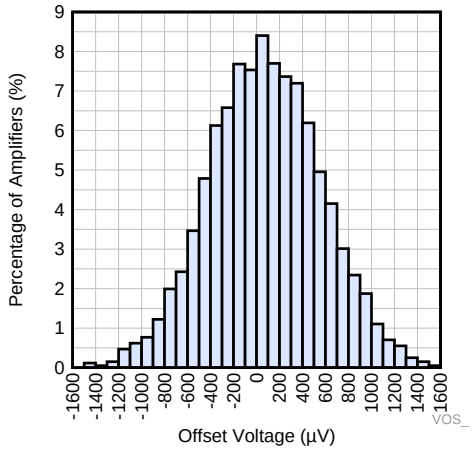
T_A = 25°C, V_S = 1.8 V to 3.3 V, V_{CM} = V_{OUT} = V_S / 2, and R_L ≥ 10 MΩ to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = V– , V_S = 1.8 V and 3.3 V	–3.1	See Plots	3.1	mV
		V_{CM} = V+, V_S = 1.8 V and 3.3 V	–3.4	See Plots	3.4	
dV_{OS}/dT	Input offset drift	V_{CM} = V–, T_A = –40°C to 125°C		0.8		µV/°C
PSRR	Power-supply rejection ratio	V_{CM} = V– , V_S =1.8 V and 3.3 V	66	90		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 3.3 V	0		3.3	V
CMRR	Common-mode rejection ratio	(V–) ≤ V_{CM} ≤ (V+), V_s = 3.3 V	60	80		dB
		(V–) ≤ V_{CM} ≤ (V+) – 1.2 V		90		
INPUT BIAS CURRENT						
I_B	Input bias current			100		fA
I_{OS}	Input offset current			100		fA
INPUT IMPEDANCE						
	Differential			2		pF
	Common mode			4		pF
NOISE						
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz		8.6		µVp–p
e_n	Input voltage noise density	f = 1 kHz		264		nV/√Hz
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.3 V ≤ V_O ≤ (V+) – 0.3 V, R_L = 100 kΩ to V^+/2		120		dB
OUTPUT						
V_{OH}	Voltage output swing from positive rail	R_L = 100 kΩ to V^+/2, V_S = 3.3 V			12	mV
V_{OL}	Voltage output swing from negative rail	R_L = 100 kΩ to V^+/2, V_S = 3.3 V			12	mV
I_{SC}	Short-circuit current	Sourcing, V_O to V–, $V_{IN(diff)}$ = 100 mV, V_S = 3.3 V		15		mA
		Sinking, V_O to V+, $V_{IN(diff)}$ = –100 mV, V_S = 3.3 V		30		
Z_O	Open loop output impedance	f = 1 kHz, I_O = 0 mA		8		kΩ
FREQUENCY RESPONSE						
GBP	Gain-bandwidth product	C_L = 20 pF, R_L = 10 MΩ		8		kHz
SR	Slew rate (10% to 90%)	G = 1, rising edge, C_L = 20 pF		3.5		V/ms
		G = 1, falling edge, C_L = 20 pF		4.5		
POWER SUPPLY						
$I_{Q–TLV8541}$	Quiescent Current	V_{CM} = V–, I_O = 0 mA, V_S = 3.3 V		550	640	nA
$I_{Q–TLV8542}$	Quiescent Current, per channel	V_{CM} = V–, I_O = 0 mA, V_S = 3.3 V		550	640	nA
$I_{Q–TLV8544}$	Quiescent current, per channel	V_{CM} = V–, I_O = 0 mA, V_S = 3.3 V		500	640	nA

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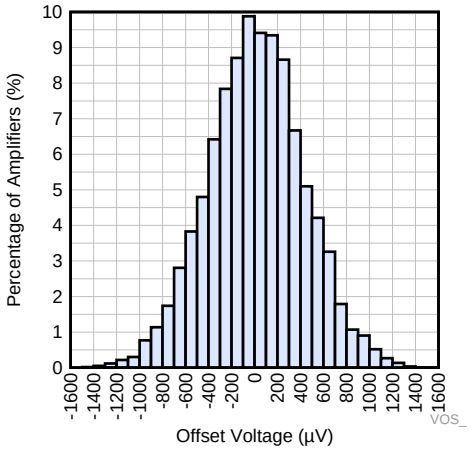
7.6 Typical Characteristics

TA = 25°C, R_L = 10 MΩ to V_S/2 ,C_L = 20 pF, V_{CM} = V_S / 2 V unless otherwise specified.



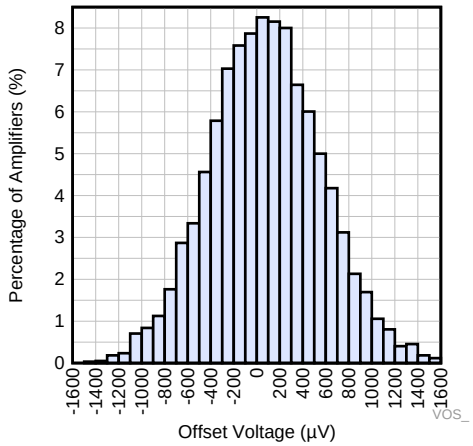
V_S = 1.8 V V_{CM} = V+ Data from 1500 4-channel devices

Figure 1. Offset Voltage Production Distribution



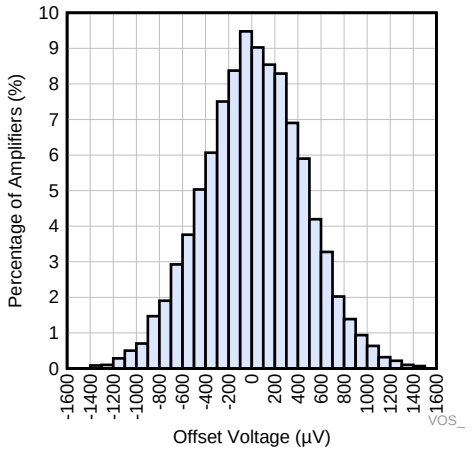
V_S = 1.8 V V_{CM} = V– Data from 1500 4-channel devices

Figure 2. Offset Voltage Production Distribution



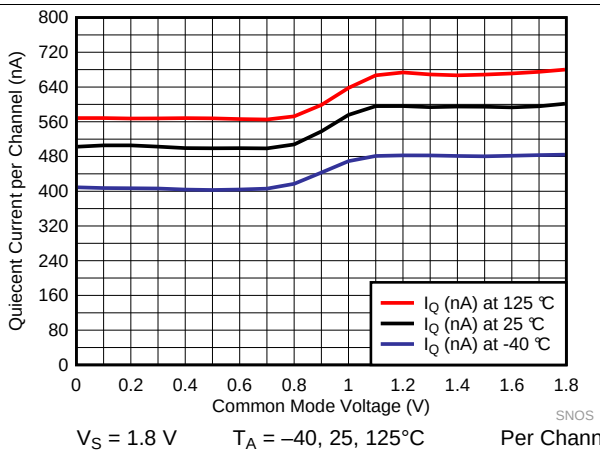
V_S = 3.3 V V_{CM} = V+ Data from 1500 4-channel devices

Figure 3. Offset Voltage Production Distribution



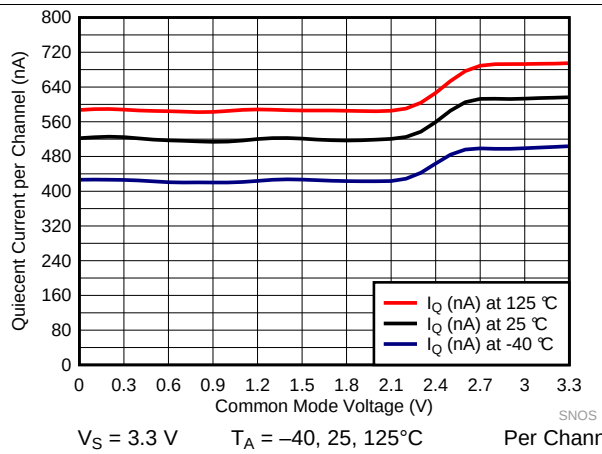
V_S = 3.3 V V_{CM} = V– Data from 1500 4-channel devices

Figure 4. Offset Voltage Production Distribution



V_S = 1.8 V T_A = –40, 25, 125°C Per Channel

Figure 5. Supply Current vs Common Mode Voltage



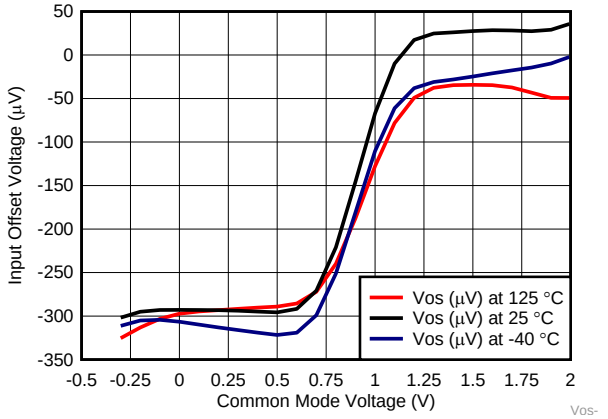
V_S = 3.3 V T_A = –40, 25, 125°C Per Channel

Figure 6. Supply Current vs Common Mode Voltage

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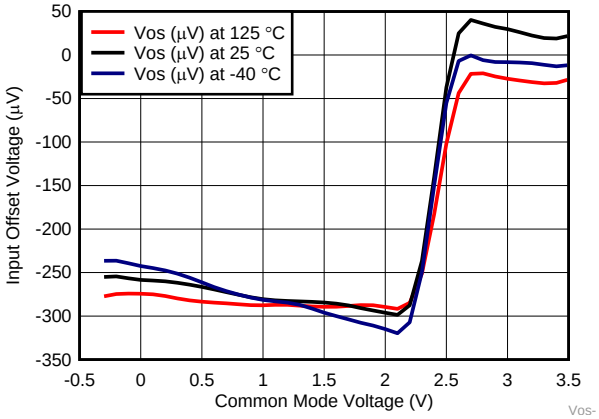
Typical Characteristics (continued)

TA = 25°C, R_L = 10 MΩ to V_S/2 ,C_L = 20 pF, V_{CM} = V_S / 2 V unless otherwise specified.



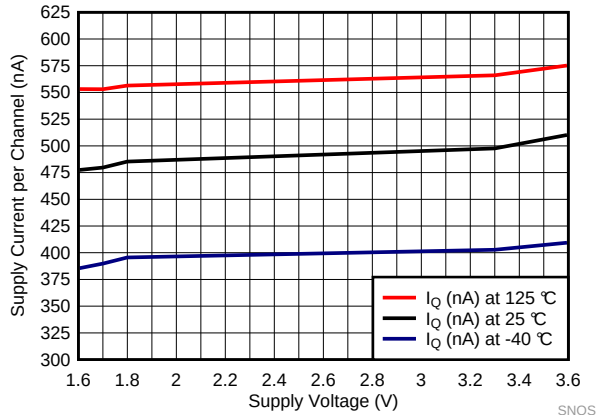
V_S = 1.8 V T_A = –40, 25, 125°C

Figure 7. Typical Offset Voltage vs Common Mode Voltage



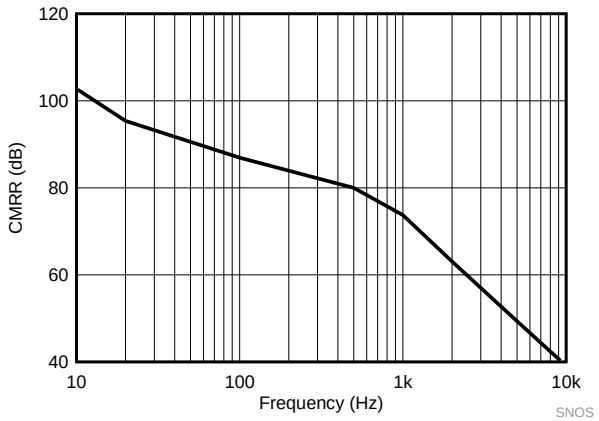
V_S = 3.3 V T_A = –40, 25, 125°C

Figure 8. Typical Offset Voltage vs Common Mode Voltage



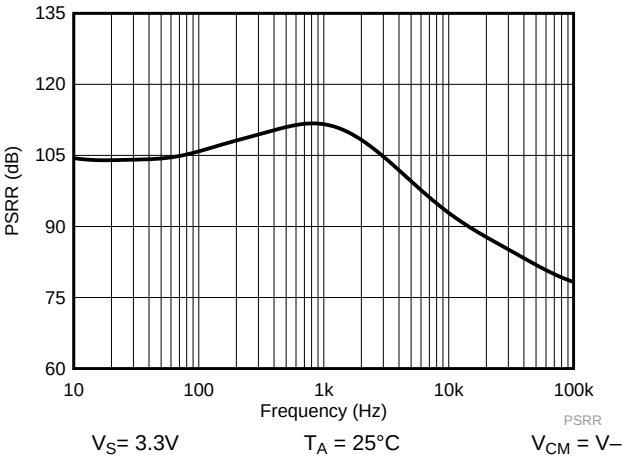
V_S = 1.6 to 3.6V T_A = –40, 25, 125°C V_{CM} = V-

Figure 9. Supply Current vs Supply Voltage, Low VCM



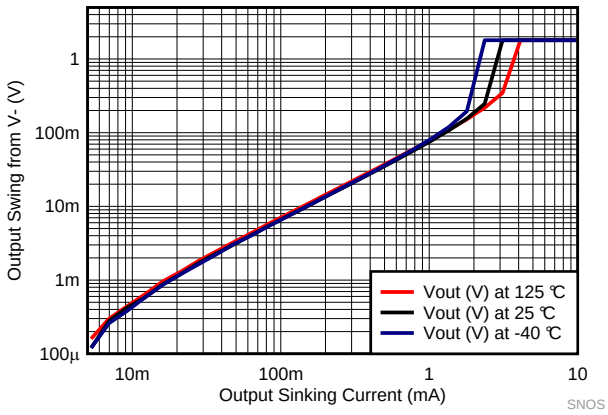
V_S= 3.3V T_A = 25°C

Figure 10. CMRR vs Frequency



V_S= 3.3V T_A = 25°C V_{CM} = V–

Figure 11. PSRR vs Frequency



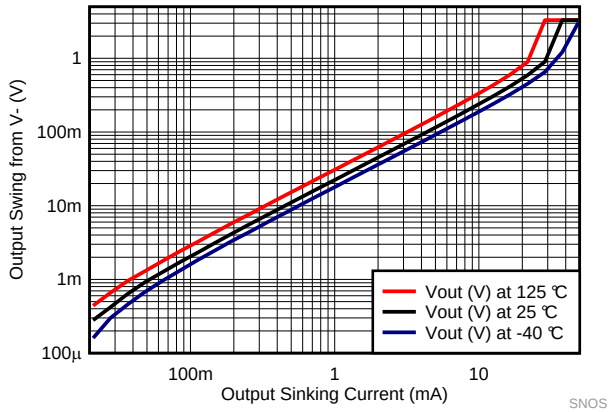
V_S = 1.8 V T_A = –40, 25, 125°C

Figure 12. Output Swing vs Sinking Current

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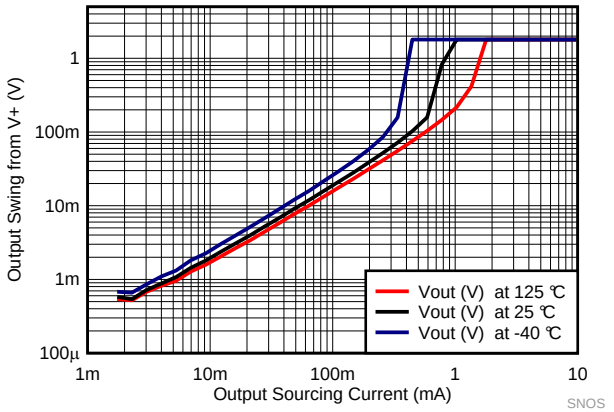
Typical Characteristics (continued)

TA = 25°C, R_L = 10 MΩ to V_S/2 ,C_L = 20 pF, V_{CM} = V_S / 2 V unless otherwise specified.



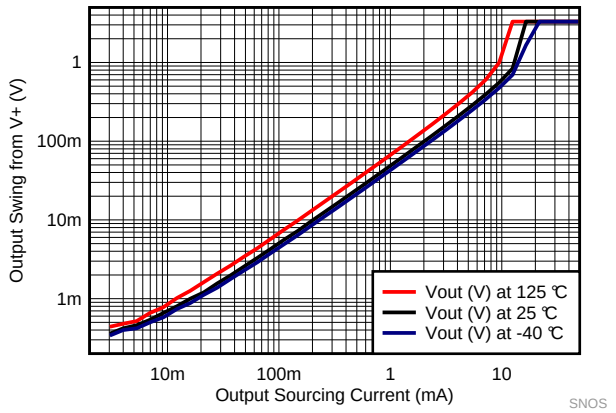
V_S = 3.3 V T_A = –40, 25, 125°C

Figure 13. Output Swing vs Sinking Current



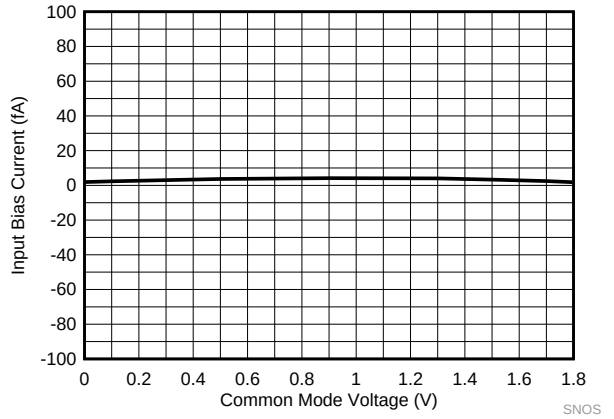
V_S = 1.8 V T_A = –40, 25, 125°C

Figure 14. Output Swing vs Sourcing Current



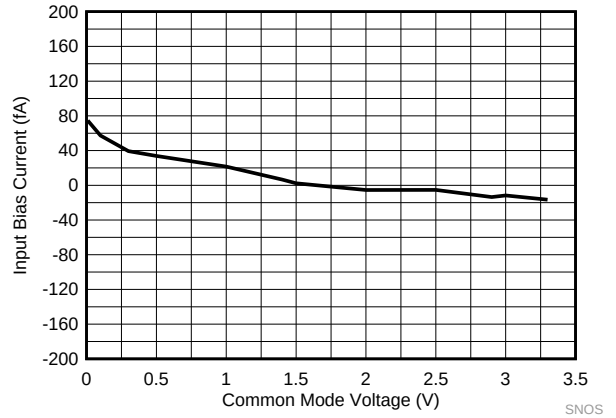
V_S = 3.3 V T_A = –40, 25, 125°C

Figure 15. Output Swing vs Sourcing Current



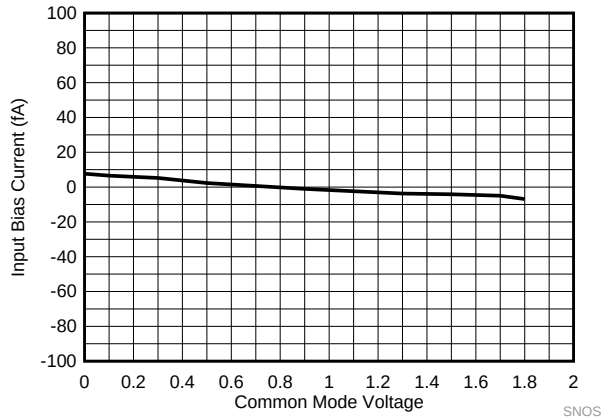
V_S = 1.8 V T_A = –40°C

Figure 16. Input Bias Current vs Common Mode Voltage



V_S = 3.3 V T_A = –40°C

Figure 17. Input Bias Current vs Common Mode Voltage



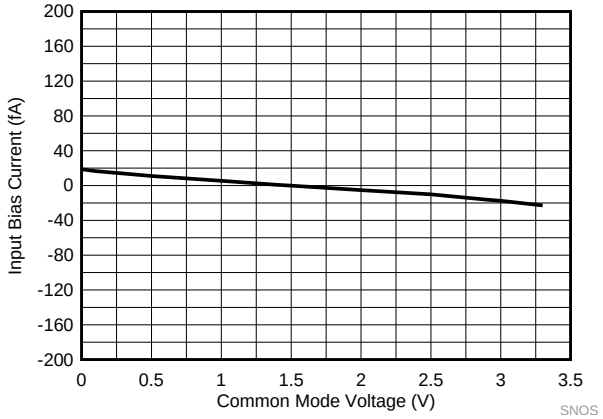
V_S = 1.8 V T_A = 25°C

Figure 18. Input Bias Current vs Common Mode Voltage

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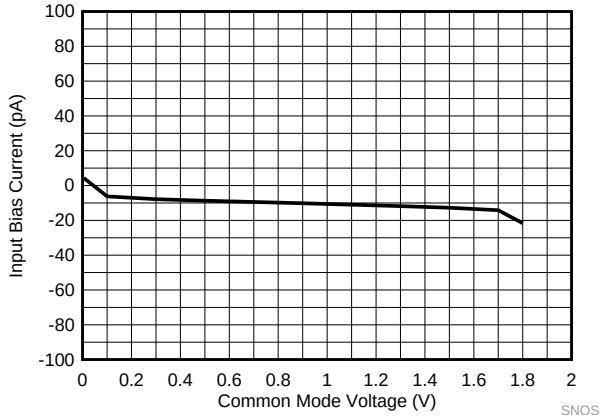
Typical Characteristics (continued)

TA = 25°C, R_L = 10 MΩ to V_S/2 ,C_L = 20 pF, V_{CM} = V_S / 2 V unless otherwise specified.



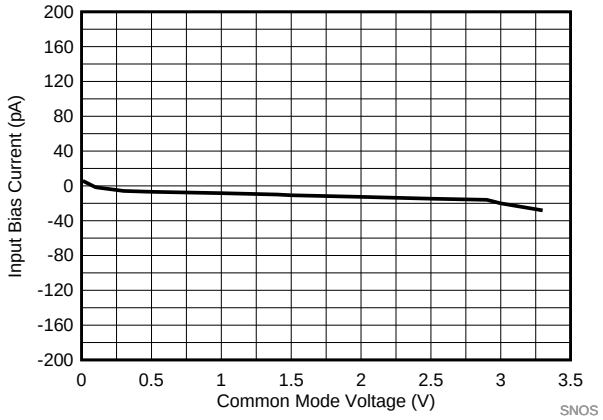
V_S = 3.3 V T_A = 25°C

Figure 19. Input Bias Current vs Common Mode Voltage



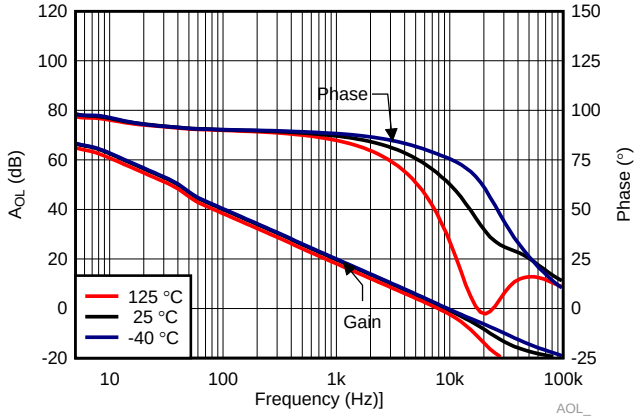
V_S= 1.8V T_A = 125°C

Figure 20. Input Bias Current vs Common Mode Voltage



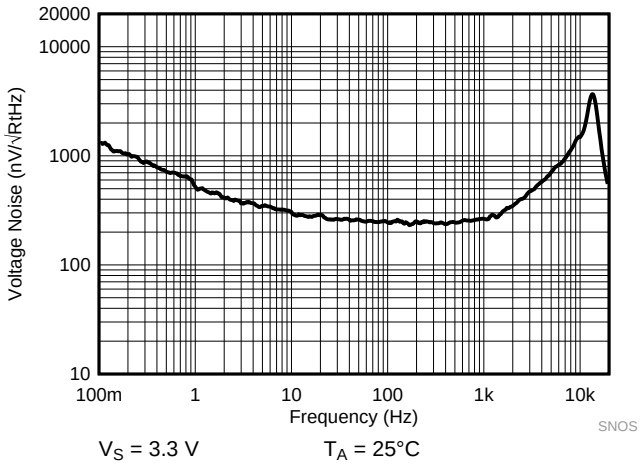
V_S = 3.3 V T_A = 125°C

Figure 21. Input Bias Current vs Common Mode Voltage



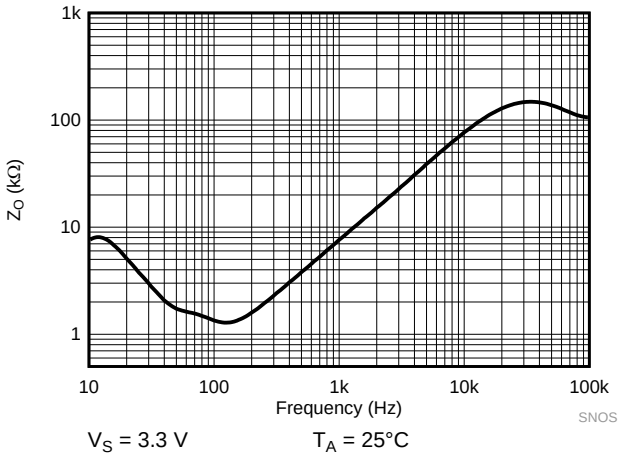
V_S = 3.3 V T_A = –40, 25, 125°C C_L = 50 pF

Figure 22. Open Loop Gain and Phase



V_S = 3.3 V T_A = 25°C

Figure 23. Input Voltage Noise vs Frequency



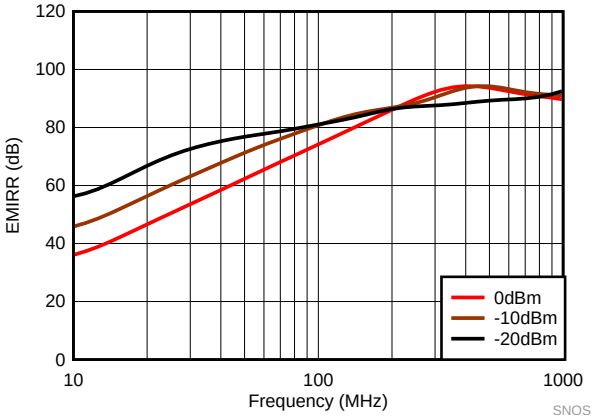
V_S = 3.3 V T_A = 25°C

Figure 24. Open Loop Output Impedance

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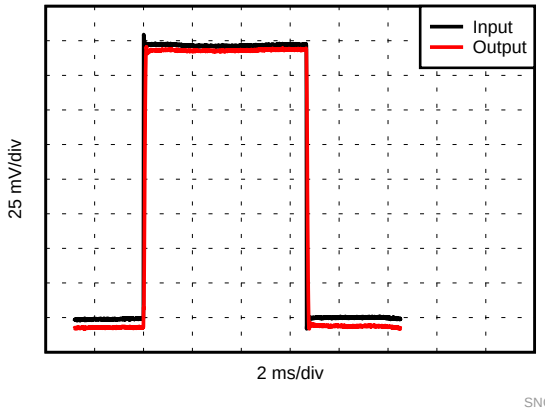
Typical Characteristics (continued)

TA = 25°C, R_L = 10 MΩ to V_S/2 ,C_L = 20 pF, V_{CM} = V_S / 2 V unless otherwise specified.



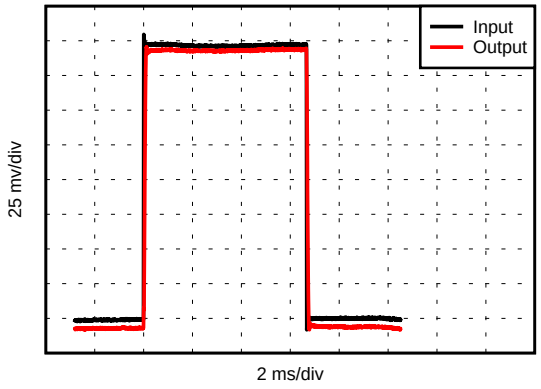
V_S = 3.3 V T_A = 25°C
A_V = 1

Figure 25. EMIRR Performance



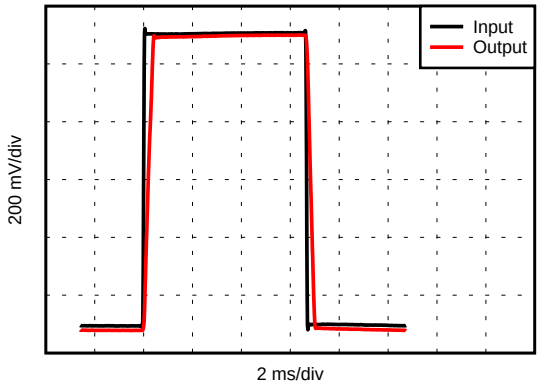
V_S = 1.8 V T_A = 25°C C_L = 50 pF
V_{IN} = 0.9 ± 0.1 V A_V = 1

Figure 26. Small Signal Pulse Response, 1.8 V



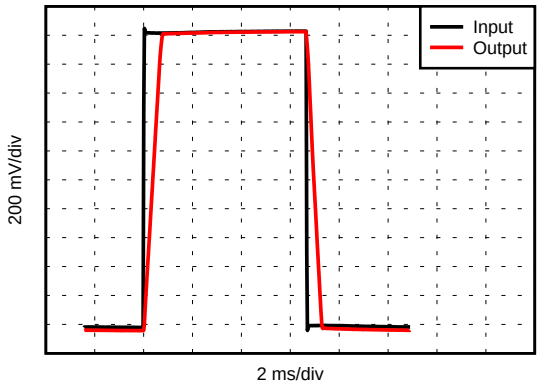
V_S = 3.3 V T_A = 25 °C C_L = 50 pF
V_{IN} = 1.65 ± 0.1 V A_V = 1

Figure 27. Small Signal Pulse Response, 3.3 V



V_S = 1.8 V T_A = 25°C C_L = 50 pF
V_{IN} = 0.9 ± 0.5 V A_V = 1

Figure 28. Large Signal Pulse Response, 1.8 V



V_S = 3.3 V T_A = 25°C C_L = 50 pF
V_{IN} = 1.65 ± 1 V A_V = 1

Figure 29. Large Signal Pulse Response, 3.3 V

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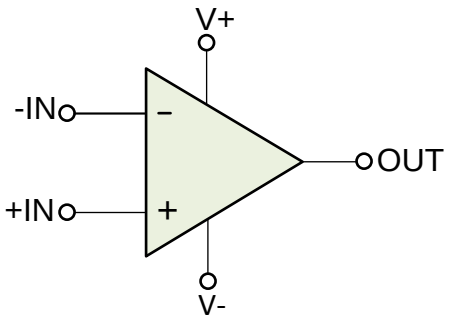
8 Detailed Description

8.1 Overview

The TLV854x amplifiers are unity-gain stable and can operate on a single supply, making them highly versatile and easy to use.

Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* curves.

8.2 Functional Block Diagram



8.3 Feature Description

The differential inputs of the TLV854x device consist of a non-inverting input (+IN) and an inverting input (–IN). The device amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amps V_{OUT} are given by Equation 1:

$$V_{OUT} = A_{OL} [(+IN) – (–IN)] \quad (1)$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 100 dB.

8.4 Device Functional Modes

8.4.1 Rail-To-Rail Input

The input common-mode voltage range of the TLV854x extends to the supply rails. This is achieved with a complementary input stage — an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 800 mV to 200 mV above the positive supply, while the P-channel pair is on for inputs from 300 mV below the negative supply to approximately (V+) – 800 mV. There is a small transition region, typically (V+) – 1.2 V to (V+) – 0.8 V, in which both pairs are on. This 400-mV transition region can vary 200 mV with process variation. Within the 400-mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

8.4.2 Supply Current Changes Over Common Mode

Because of the ultra-low supply current, changes in common mode voltages cause a noticeable change in the supply current as the input stages transition through the transition region, as shown in Figure 30.

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Device Functional Modes (continued)

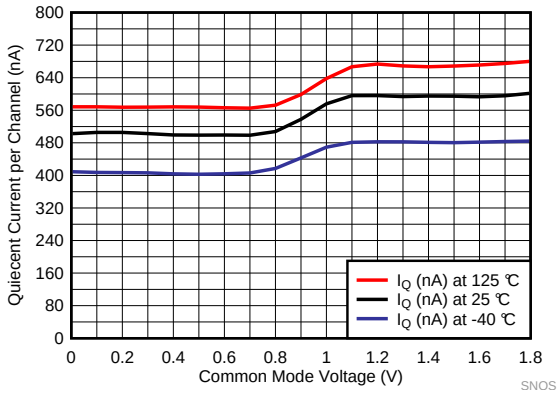


Figure 30. Supply Current Change Over Common Mode at 1.8 V

For the lowest supply current operation, keep the input common mode range between V– and 1 V below V+.

8.4.3 Design Optimization With Rail-To-Rail Input

In most applications, operation is within the range of only one differential pair. However, some applications can subject the amplifier to a common-mode signal in the transition region. Under this condition, the inherent mismatch between the two differential pairs may lead to degradation of the CMRR and THD. The unity-gain buffer configuration is the most problematic as it traverses through the transition region if a sufficiently wide input swing is required.

8.4.4 Design Optimization for Nanopower Operation

When designing for ultra-low power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors react with stray capacitance in the circuit and the input capacitance of the operational amplifier (op amp). These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

When possible, use AC coupling and AC feedback to reduce static current draw through the feedback elements. Use film or ceramic capacitors because large electolytics may have static leakage currents in the tens to hundreds of nanoamps.

8.4.5 Common-Mode Rejection

The CMRR for the TLV854x is specified in two ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region (V_{CM} < (V+) – 1.2 V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at V_S = 3.3 V over the entire common-mode range is specified.

8.4.6 Output Stage

The TLV854x output voltage swings 20 mV from rails at a 3.3-V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The TLV854x maximum output voltage swing defines the maximum swing possible under a particular output load.

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Device Functional Modes (continued)

8.4.7 Driving Capacitive Load

The TLV854x is internally compensated for stable unity-gain operation, with a 8-kHz typical gain bandwidth. However, the unity-gain follower is the most sensitive configuration-to-capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response is under-damped, which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy (> 50 pF) capacitive loads, use an isolation resistor, R_{ISO}, as shown in Figure 31. By using this isolation resistor, the capacitive load is isolated from the output of the amplifier. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop is stable, independent of the value of C_L. However, larger values of R_{ISO} (e.g. 50 kΩ) result in reduced output swing and reduced output current drive.

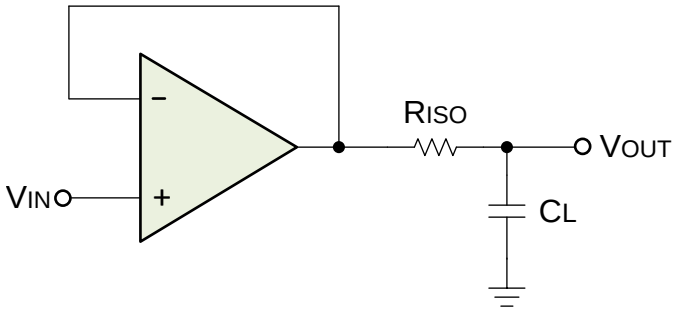


Figure 31. Resistive Isolation of Capacitive Load

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV854x is a nanopower op amps that provides 8-kHz bandwidth with only 500-nA typical quiescent current per channel and near precision drift specifications at a low cost. These rail-to-rail input and output amplifiers are specifically designed for battery-powered applications. The input common-mode voltage range extends to the power-supply rails and the output swings to within millivolts of the rails, maintaining a wide dynamic range.

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9.2 Typical Application: Battery-Powered Wireless PIR Motion Detectors

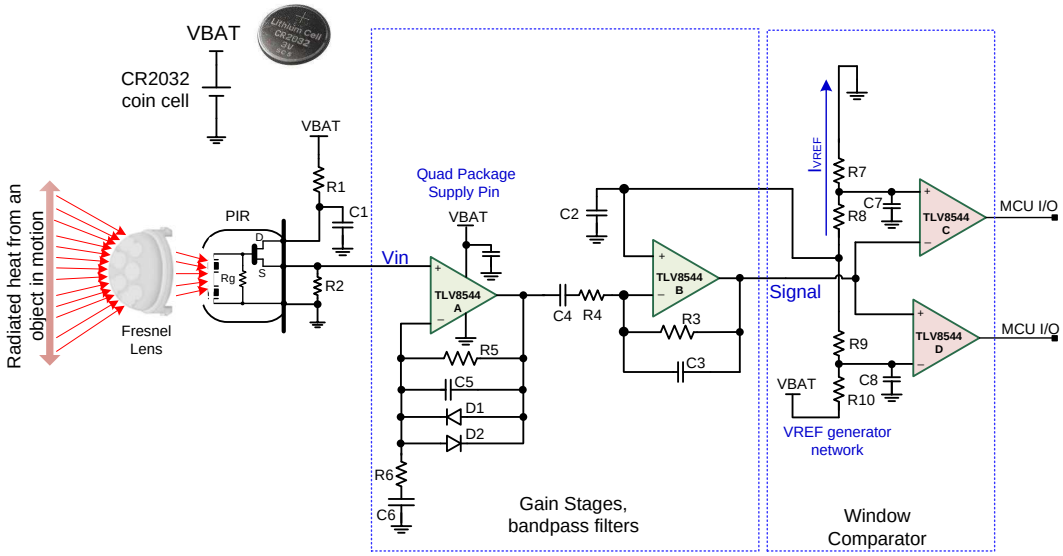


Figure 32. PIR Motion Detector Circuit

9.2.1 Design Requirements

Smart building automation systems employ a large number of various sensing nodes distributed throughout small, medium, and large infrastructures. The sensing nodes measure motion, temperature, vibration, and other parameters of interest. Wireless nodes are monitored in a central location. Because of the large number of distributed nodes , battery-operation and cost-optimized electronic components are required. Typically, the wireless nodes need to run on a single CR2032 coin battery for eight to ten years.

For more information see *Design of Ultra-Low Power Discrete Signal Conditioning Circuit for Battery-Power*, *Ultra-Low-Power Wireless PIR Motion Detector Reference Design* and *BOOSTXL-TLV8544PIR User's Guide*. The BOOSTXL-TLV8544PIR along with the companion CC2650 LaunchPad, LAUNCHXL-CC2650 can be obtained from the TI website for hands-on experiments.

9.2.2 Detailed Design Procedure

Referring to Figure 32, the TLV8544 4-channel op amp is powered directly by a 3.3-V CR2032 coin battery. The first two amplifier stages of the TLV8544 implement active filter functionality. The remaining two amplifiers of the TLV8544 are used for building a window comparator. The comparator flags the detection of a motion event to an ultra-low-power wireless microcontroller on the same board. Due to the higher gain in the filter stages and higher output noise from the sensor, it is necessary to optimize the placement of the high-frequency filter pole and the window comparator thresholds to avoid false detection.

The first two amplifiers (*A* and *B*) in the circuit are used in identical active bandpass filters with corner frequencies of 0.7 and 10.6 Hz. Each filter stage has a gain of about 220 V/V to account for the reduced sensitivity of the sensor due to the low current biasing of the PIR sensor. Considering the 8-kHz unity gain bandwidth (UGBW) product of the TLV8544, the bandwidth of each stage is limited to approximately 36 Hz. The above choice of cutoff frequencies give a relatively wide bandwidth to detect a person running in the field of view, yet narrow enough to limit the peak-to-peak noise at the output of the filters.

Amplifier *A* is a noninverting gain/filter stage providing the high input impedance needed to prevent loading of the sensor. The DC gain of the stage due to the presence of C6 is unity. Therefore, the sensor output provides the bias voltage needed at the *A* stage to avoid clipping of the lower cycle of the input signal. Diodes D1 and D2 limit the output signal, avoiding overdriving of the second stage and consequently placing a large charge on coupling capacitor C4, which helps with the recovery time.

9.2.2.1 Calculation of the Cutoff Frequencies and Gain of Stage A:

The low cutoff frequency of the bandpass filter in stage *A* is:

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Typical Application: Battery-Powered Wireless PIR Motion Detectors (continued)

$$f_{Clow} = \frac{1}{2\pi \times R_6 \times C_6} \quad (2)$$

Choosing R6 = 6.81 kΩ and C6 = 33 µF, the low cutoff frequency is f_{Clow}= 0.71 Hz. The high cutoff frequency of the filter is:

$$f_{Chigh} = \frac{1}{2\pi \times R_5 \times C_5} \quad (3)$$

For R5 = 1.5 MΩ and C5 = 0.01 µF, the high cutoff frequency is f_{Chigh}= 10.6 Hz. The gain of the stage is:

$$G = 1 + \frac{R5}{R6} \quad (4)$$

Choosing R5 = 1.5 MΩ and R6 = 6.81 kΩ, the gain of the stage *A* is G = 221.26 V/V (46.9 dB).

9.2.2.2 Calculation of the Cutoff Frequencies and Gain of Stage B

As shown in Figure 32, amplifier *B* is an inverting bandpass filter and gain stage. Capacitor C4 creates an AC coupled path between the *A* and the *B* stages. Thus the signal level must be shifted at the input of the amplifier *B*. This is done by connecting a midpoint voltage of the reference voltage dividers comprising R10, R9, R8 and R7 to the non-inverting input of amplifier *B*, biasing the input signal to the mid-rail (1.65 V). A very large feedback resistor R3 is chosen to minimize the dynamic current due to presence of peak-to-peak noise voltage at the output of this stage.

The low cutoff frequency of the filter of the stage *B* is:

$$f_{Clow} = \frac{1}{2\pi \times R_4 \times C_4} \quad (5)$$

Choosing R4 = 68.1 kΩ and C4 = 3.3 µF, the low cutoff frequency is f_{Clow} = 0.71 Hz. The high cutoff frequency of the filter is:

$$f_{Chigh} = \frac{1}{2\pi \times R_3 \times C_3} \quad (6)$$

For R3 = 15 MΩ and C3 = 1000 pF, the high cutoff frequency is f_{Chigh}= 10.6 Hz. The gain of the stage is:

$$G = -\frac{R3}{R4} \quad (7)$$

For R3 = 15 MΩ and R4 = 68.1 kΩ, the gain is calculated |G| = 220.26 V/V (46.9 dB).

9.2.2.3 Calculation of the Total Gain of Stages A and B

The overall gain of the two stages *A* and *B* is: $G_{Total} = G_A \times G_B$= 221.26 × 220.26 = 48810 V/V = 93.77 dB.

9.2.2.4 Window Comparator Stage

The signal from a moving object in front of the PIR sensor, after amplification and filtering, is connected to a window comparator. The comparator converts the analog signal to digital pulses for interrupting an on-board microcontroller unit (MCU), flagging detection of motion. A different approach is to digitize the analog signal continuously by an analog-to-digital converter (ADC) and implement the comparator functionality in the digital domain. This method has the advantage of enabling the post processing of the data to reduce the chance of false detection. However, continuous conversion and processing of data by the MCU increases the power consumption, lowering the lifetime of the battery substantially.

Rather than using a separate low-power comparator integrated circuits to implement the window comparator section of the circuit, the remaining op amps in the TLV8544 package are used to implement the comparator stage. Benefits of this approach include fewer components and thus reduced system cost.

Although an op amp can sometimes be used as a comparator, an amplifier cannot be used as a comparator interchangeably in all applications because of relatively long recovery time of the amplifier from output saturation and relatively long propagation delay due to internal compensation. Particularly, the nanopower op amps have very slow slew rate, limiting their usage as a comparator in only applications with very low frequency input signal. Fortunately, PIR sensor signals are relatively slow and this should not be an issue.

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Typical Application: Battery-Powered Wireless PIR Motion Detectors (continued)

The new TLV8544 device is particularly suitable for implementing a window comparator in a battery operated PIR motion detector application because of its rail-to-rail operation capability, relatively low offset voltage, low offset voltage drift, very low bias current, and nanopower consumption, all at an optimal cost. The input signal of the comparator stage in the presence of moving heat source across the sensor is shown in Figure 33. The signal is centered at mid-rail and can swing up or down from the center.

The window comparator is a combination of a non-inverting comparator implemented with amplifier *D* and an inverting comparator implemented with amplifier *C*, as shown in Figure 32.

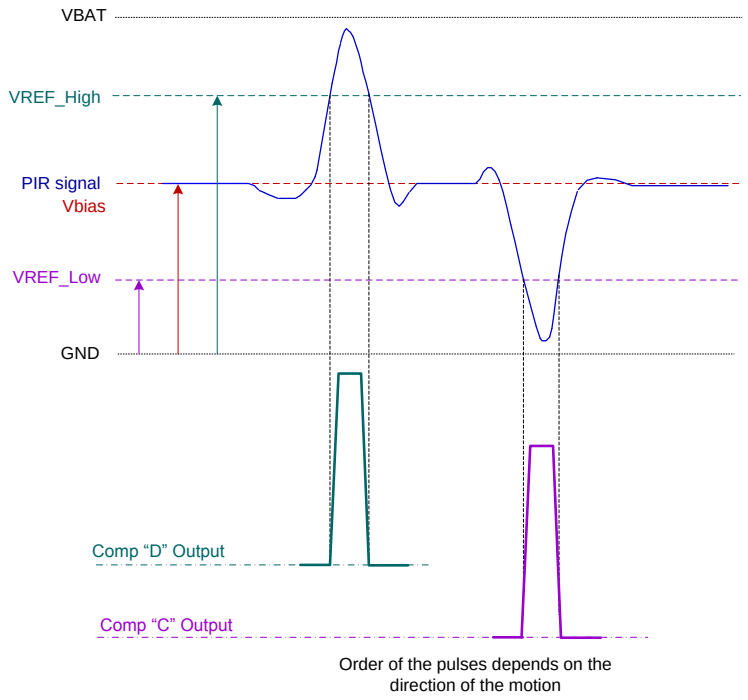


Figure 33. Ideal Amplified PIR Signal and the Output of the Window Comparator Circuit

9.2.2.5 Reference Voltages

Referring to Figure 32, the divider networks comprising R7, R8, R9, and R10, generate the reference voltages *VREF_High* and *VREF_Low* of the window comparator. The center point of the divider provides the bias voltage of the gain in the stage *B* through the connection to the noninverting input of the amplifier.

Due to the very low bias current of the TLV8544 device, it is possible to use very large values of resistors in the divider networks to minimize the current to ground through the resistors to a negligible amount. For R7 = R8 = R9 = R10 = 15 MΩ:

$$\text{VREF_High} = \left(\frac{\text{R7}+\text{R8}+\text{R9}}{\text{R7}+\text{R8}+\text{R9}+\text{R10}}\right)\text{V}_{\text{CC}} = \frac{4.5\times10^{6}}{6\times10^{6}}\times\text{V}_{\text{CC}} = 0.75\times\text{V}_{\text{CC}} \quad (8)$$

$$\text{VREF_Low} = \left(\frac{\text{R7}}{\text{R8}+\text{R9}+\text{R10}+\text{R7}}\right)\text{V}_{\text{CC}} = \frac{1.5\times10^{6}}{6\times10^{6}}\times\text{V}_{\text{CC}} = 0.25\times\text{V}_{\text{CC}} \quad (9)$$

Low leakage ceramic capacitors C7, and C8, maintain constant threshold voltages, preventing potential chatter at the output of the comparators. It should be noted that using cheap electrolytic capacitors must be avoided as they have high (many µA) leakage current. The comparator outputs stay low in the absence of motion across the sensor. In the presence of motion, comparators *C* and *D* generate *high* output pulses as shown in Figure 33. The order of the pulses depends on the direction of the motion in front of the sensor.

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Typical Application: Battery-Powered Wireless PIR Motion Detectors (continued)

9.2.3 Application Curve

Scope plots of the amplified PIR signal at the input of the noninverting comparator and the corresponding output signal are shown in Figure 34 and Figure 35. As the PIR signal (blue line) crosses the VREF_High threshold, the output of the comparator switches from the cutoff (slightly higher than ground) state to the saturation state (slightly lower than V_{BAT} = 3.3 V). Depending on the speed of the object, the PIR signal peaks to its maximum and roles off within several seconds. When the signal crosses the VREF_High threshold on the way down, the output of the noninverting amplifier toggles back to the cutoff region (low).

The data for plot of Figure 34 was captured using the BOOSTXL-TLV8544PIR board. Because the motion was created at very close proximity of the sensor on the booster board used to collect the data, the signal was limited by the diode in the first stage as shown in the plot.

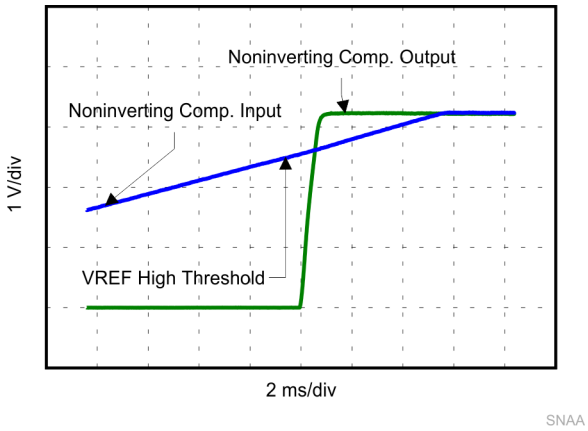


Figure 34. Noninverting Comparator Input and Output Signals

Referring to Figure 34, the output of the inverting comparator during the lower cycle of the PIR signal switches form the cutoff region to the saturation region as the input signal crosses the VREF_Low threshold.

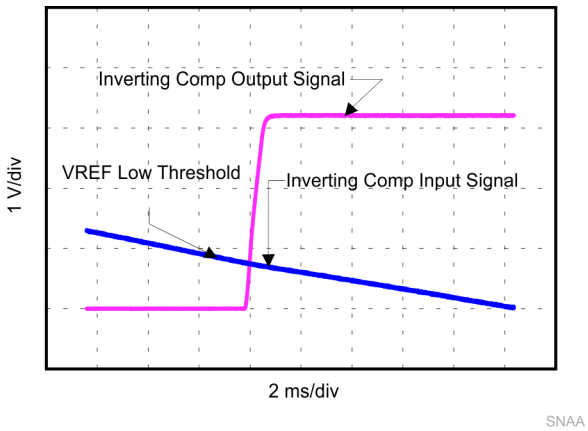


Figure 35. Noninverting Comparator Input and Output Signals

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9.3 Typical Application: 60-Hz Twin T Notch Filter

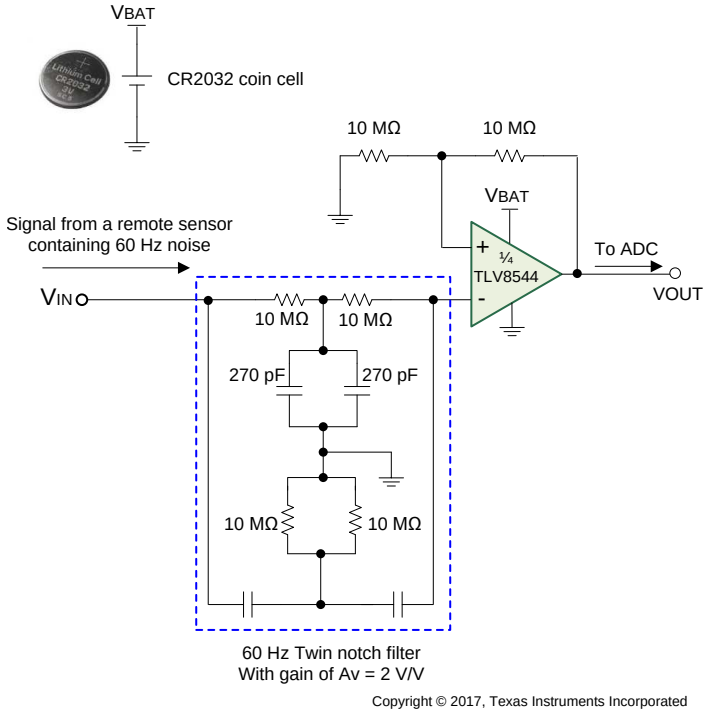


Figure 36. 60 Hz-Notch Filter

9.3.1 Design Requirements

Small signals from transducers in remote and distributed sensing applications commonly suffer strong 60-Hz interference from AC power lines. The circuit of Figure 36 filters out (notches out) the 60 Hz and provides a system gain of A_V = 2 V/V for the sensor signal represented by a 1-kHz sine wave. Similar stages may be cascaded to remove 2nd and 3rd harmonics of 60 Hz. Thanks to the nanopower consumption of the TLV8544, even five such circuits can run for 9.5 years from a small CR2032 lithium cell. These batteries have a nominal voltage of 3 V and an end of life voltage of 2 V. With an operating voltage from 1.7 V to 3.6 V the TLV8544 device can function over this voltage range.

9.3.2 Detailed Design Procedure

The notch frequency is set by:

$$F_0 = 1 / 2\pi RC. \quad (10)$$

To achieve a 60-Hz notch use R = 10 MΩ and C = 270 pF. If eliminating 50-Hz noise, use R = 11.8 MΩ and C = 270 pF.

The twin T notch filter works by having two separate paths from V_{IN} to the input of the amplifier. A low-frequency path through the series input resistors and another separate high-frequency path through the series input capacitors. However, at frequencies around the notch frequency, the two paths have opposing phase angles, and the two signals tend to cancel at the input of the amplifier.

To ensure that the target center frequency is achieved and to maximize the notch depth (Q factor) the filter must be as balanced as possible. To obtain circuit balance, while overcoming limitations of available standard resistor and capacitor values, use passives in parallel to achieve the 2C and R/2 circuit requirements for the filter components that connect to ground.

To make sure passive component values stay as expected, clean the board with alcohol, rinse with deionized water, and air dry. Make sure board remains in a relatively low humidity environment to minimize moisture which may increase the conductivity of board components. Also large resistors come with considerable parasitic stray capacitance which effects can be reduced by cutting out the ground plane below components of concern.

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Typical Application: 60-Hz Twin T Notch Filter (continued)

Large resistors are used in the feedback network to minimize battery drain. When designing with large resistors, resistor thermal noise, op amp current noise, as well as op-amp voltage noise, must be considered in the noise analysis of the circuit. The noise analysis for the circuit in Figure 36 can be done over a bandwidth of 2 kHz, which takes the conservative approach of overestimating the bandwidth (TLV8544 typical GBW/A_V is lower, where A_V is the gain of the system). The total noise at the output is approximately 800 µVpp, which is excellent considering the total consumption of the circuit is only 500 nA per channel. The dominant noise terms are op-amp voltage noise, current noise through the feedback network (430 µVp-p), and current noise through the notch filter network (280 µVp-p). Thus the total noise of the circuit is below 1/2 LSB of a 10-bit system with a 2-V reference, which is 1 mV.

9.3.3 Application Curve

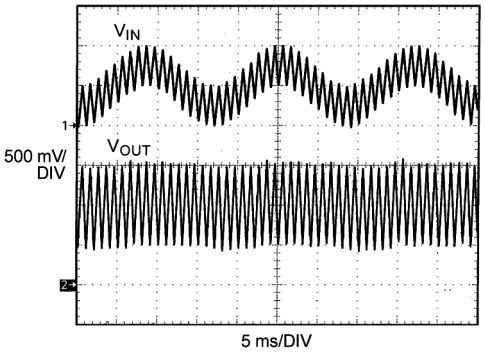


Figure 37. 60-Hz Notch Filter Waveform

9.4 Dos and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, particularly cables, multiplexers, and ADC inputs.

Do add series current limiting resistors and external Schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 KΩ per volt).

10 Power Supply Recommendations

The TLV854x is specified for operation from 1.7 V to 3.6 V (±0.85 V to ±1.8 V) over a –40°C to +125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 3.6 V can permanently damage the device.

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 100-nF capacitors be placed as close as possible to the op-amp power supply pins. For single supply, place a capacitor between V+ and V– supply leads. For dual supplies, place one capacitor between V+ and ground and one capacitor between V– and ground.

Low bandwidth nanopower devices do not have good high frequency (> 1 kHz) AC PSRR rejection against high-frequency switching supplies and other 1-kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

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11 Layout

11.1 Layout Guidelines

- The V+ pin must be bypassed to ground with a low ESR capacitor.
- The optimum placement is closest to the V+ and ground pins.
- Take care to minimize the loop area formed by the bypass capacitor connection between V+ and ground.
- Connect the ground pin to the PCB ground plane at the pin of the device.
- Place the feedback components as close as possible to the device to minimize stray impedance.

11.2 Layout Example

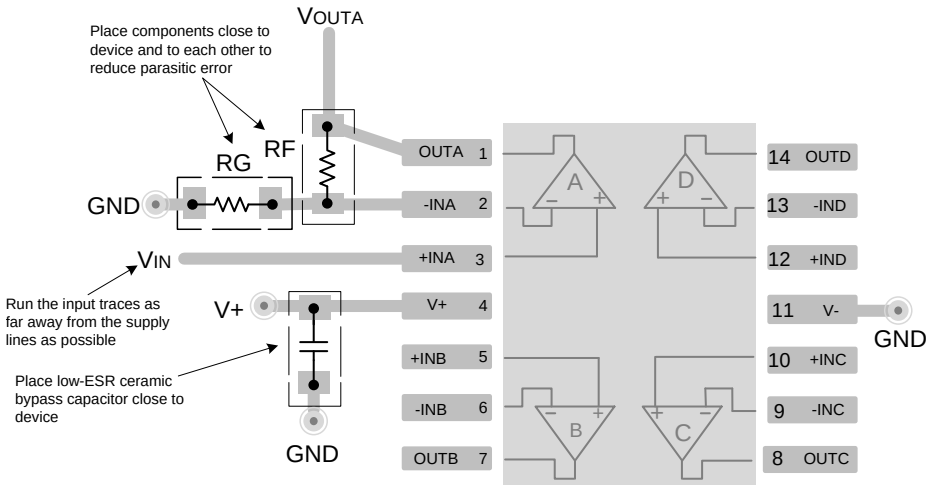


Figure 38. Layout Example of a Typical Dual Channel Package (Top View)

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

基于 SPICE 的 TINA-TI 模拟仿真程序

DIP 适配器评估模块

TI 通用运算放大器评估模块

TI FilterPro 滤波器设计软件

12.2 文档支持

12.2.1 相关文档

相关文档如下：

- *AN-1798《设计电化学传感器》*
- *《AN-1803 跨阻放大器设计注意事项》*
- *《AN-1852 使用 pH 电极进行设计》*
- *《用直观方式补偿互阻抗放大器》*
- *《高速运算放大器跨阻注意事项》*
- *《FET 跨阻放大器噪声分析》*
- *《电路板布局布线技巧》*
- *《运算放大器应用 手册》*

12.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及立即订购快速访问。

表 **1.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TLV8544	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV8542	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV8541	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 接收文档更新通知

要接收文档更新通知，请转至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

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12.6 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV8541DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1D5L
TLV8541DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1D5L
TLV8542DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL8542
TLV8542DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL8542
TLV8542DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL8542
TLV8542DRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL8542
TLV8542RUGR	Active	Production	X2QFN (RUG) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AR
TLV8542RUGR.B	Active	Production	X2QFN (RUG) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AR
TLV8544DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV8544
TLV8544DR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV8544
TLV8544DT	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV8544
TLV8544DT.B	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV8544
TLV8544PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TL8544
TLV8544PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL8544

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

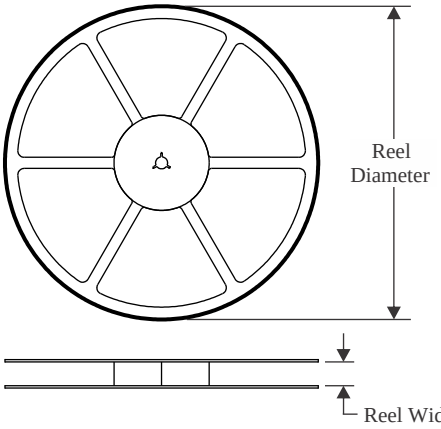
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

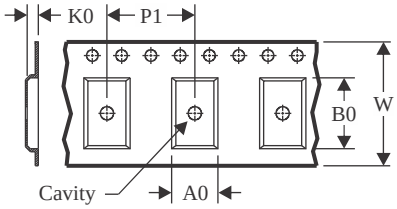
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

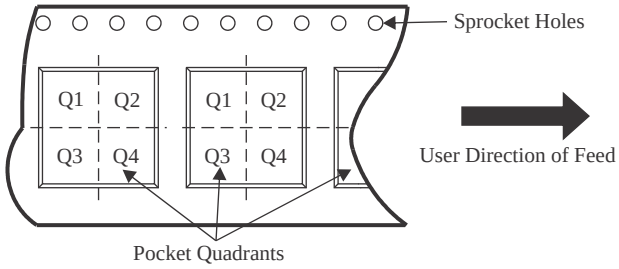


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

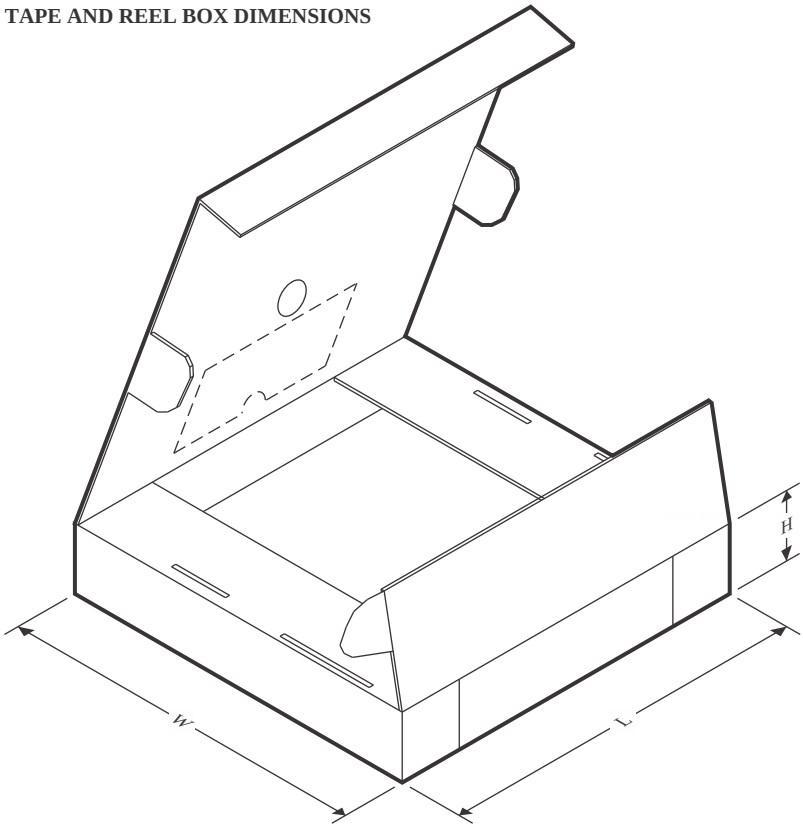
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV8541DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV8542DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV8542DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV8542RUGR	X2QFN	RUG	8	3000	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2
TLV8544DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV8544PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV8544PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

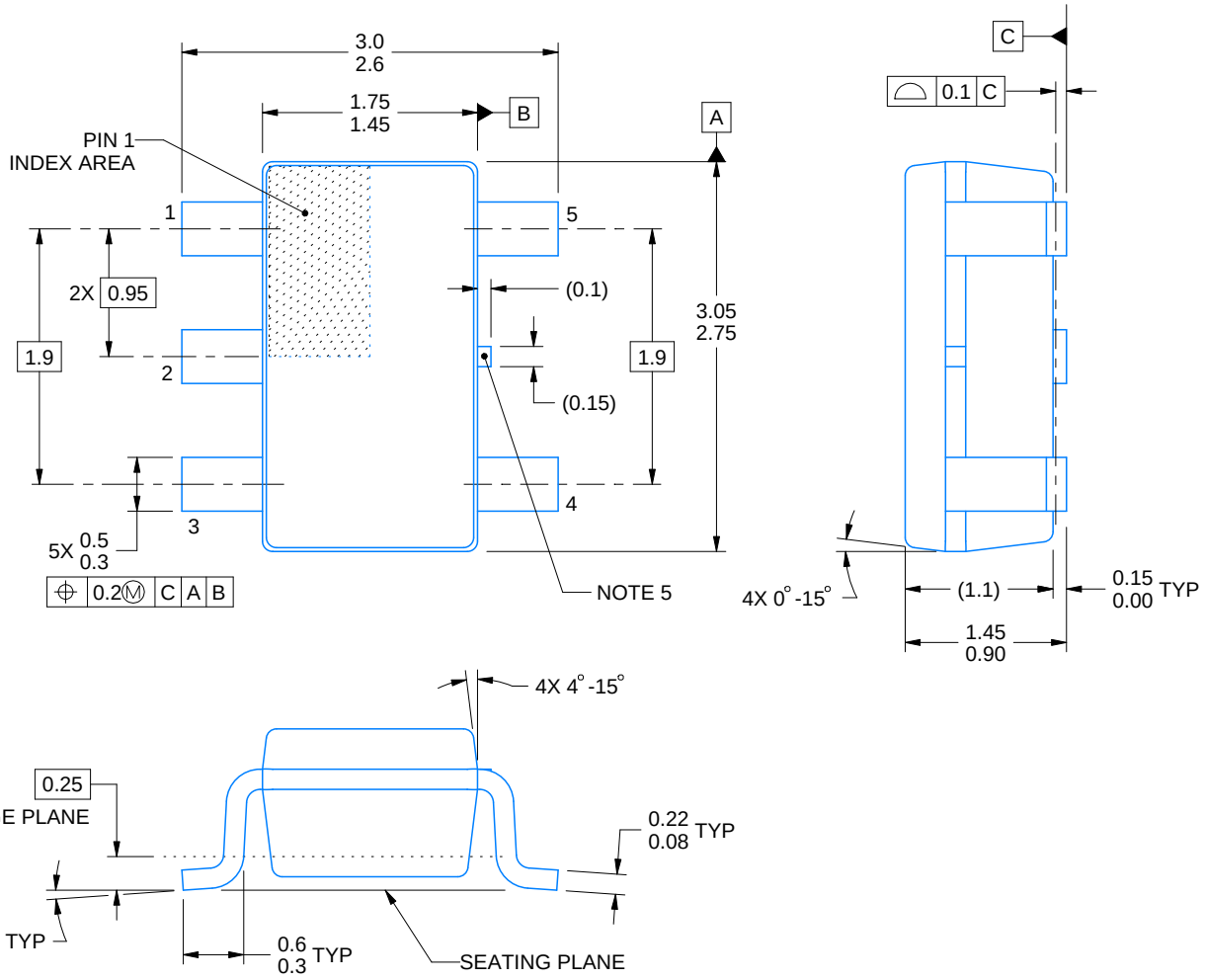
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV8541DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV8542DR	SOIC	D	8	2500	340.5	338.1	20.6
TLV8542DRG4	SOIC	D	8	2500	340.5	338.1	20.6
TLV8542RUGR	X2QFN	RUG	8	3000	183.0	183.0	20.0
TLV8544DR	SOIC	D	14	2500	340.5	336.1	32.0
TLV8544PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV8544PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

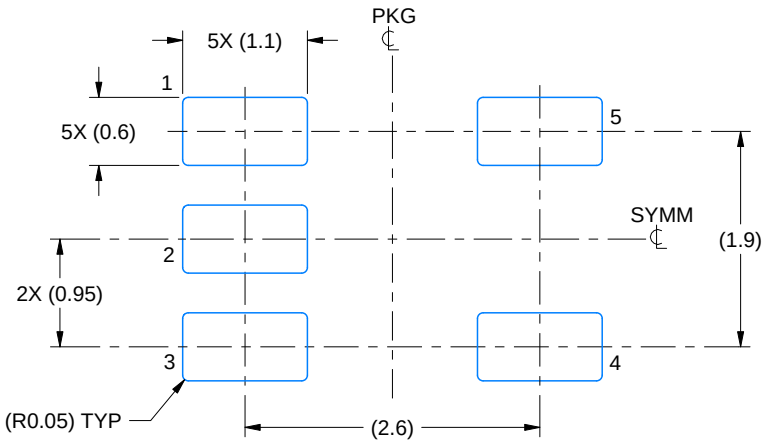
SMALL OUTLINE TRANSISTOR



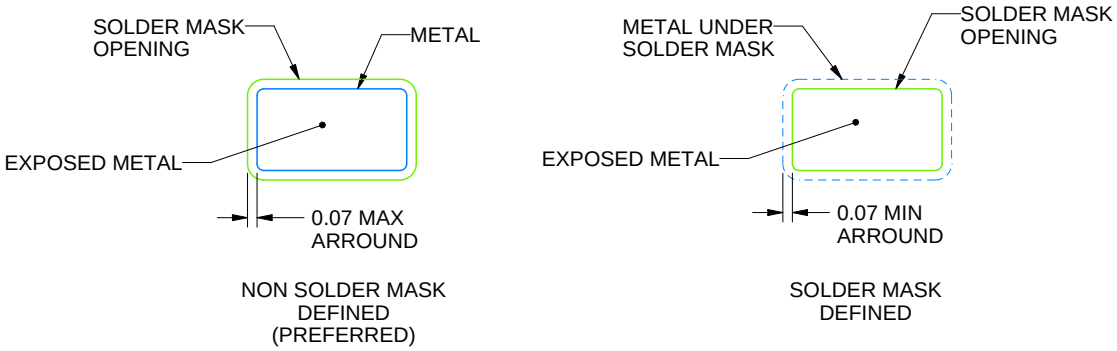
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

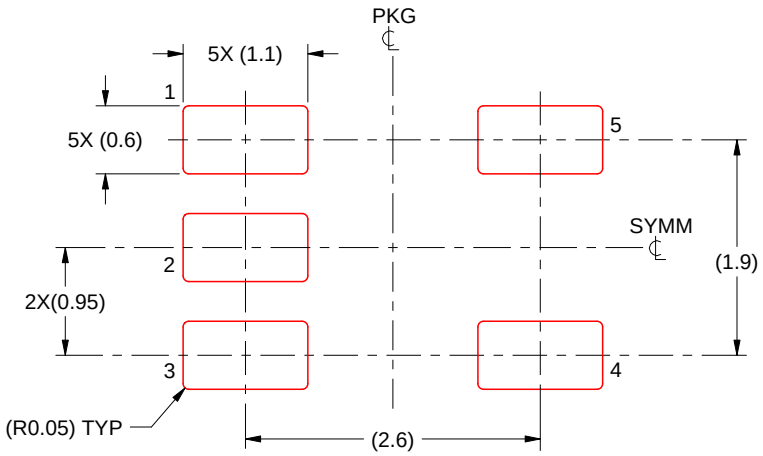


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

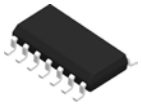


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

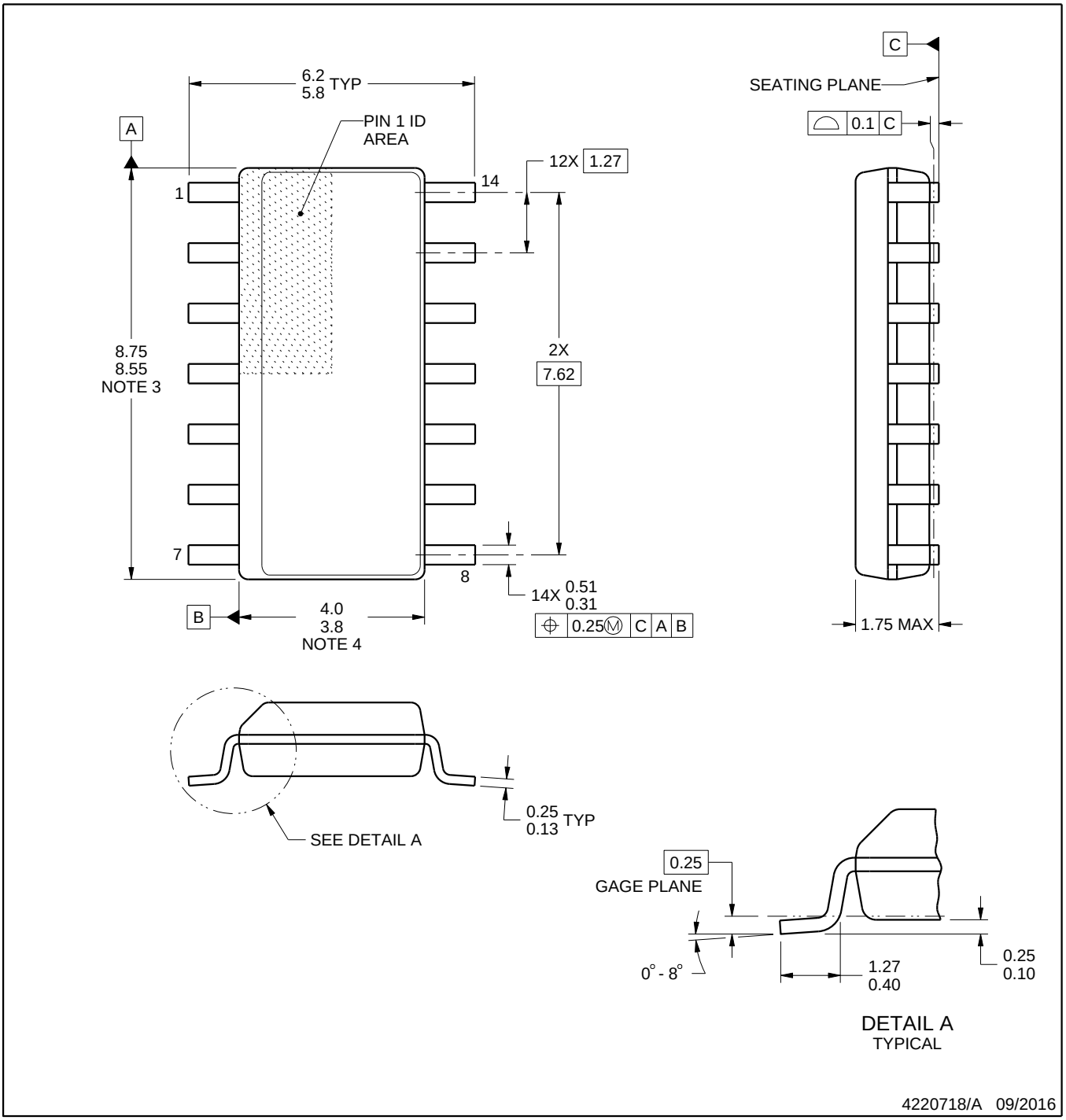


PACKAGE OUTLINE

D0014A

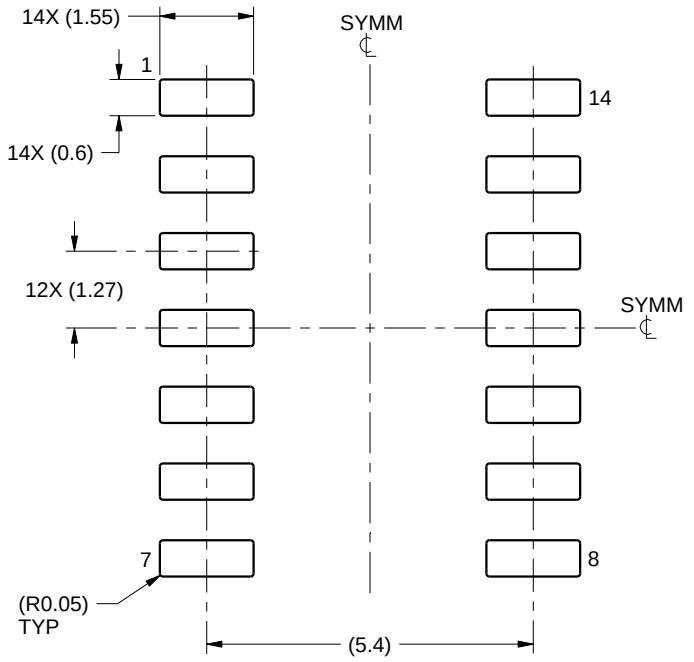
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

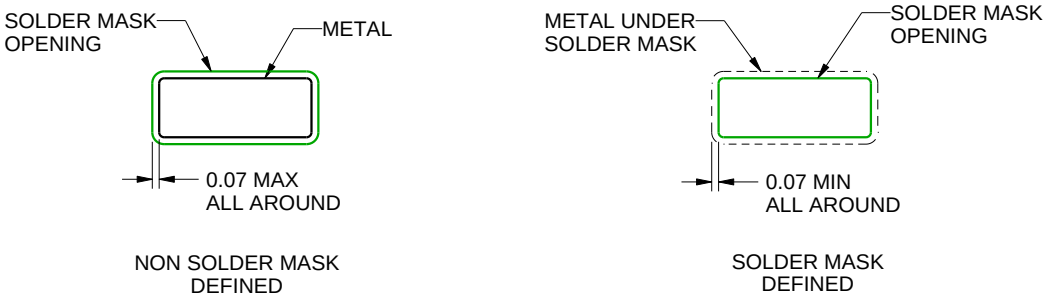


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

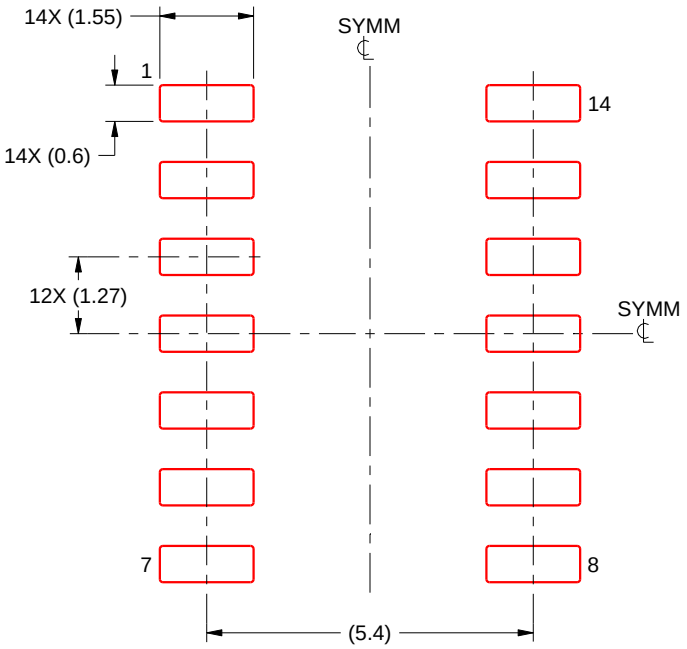
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



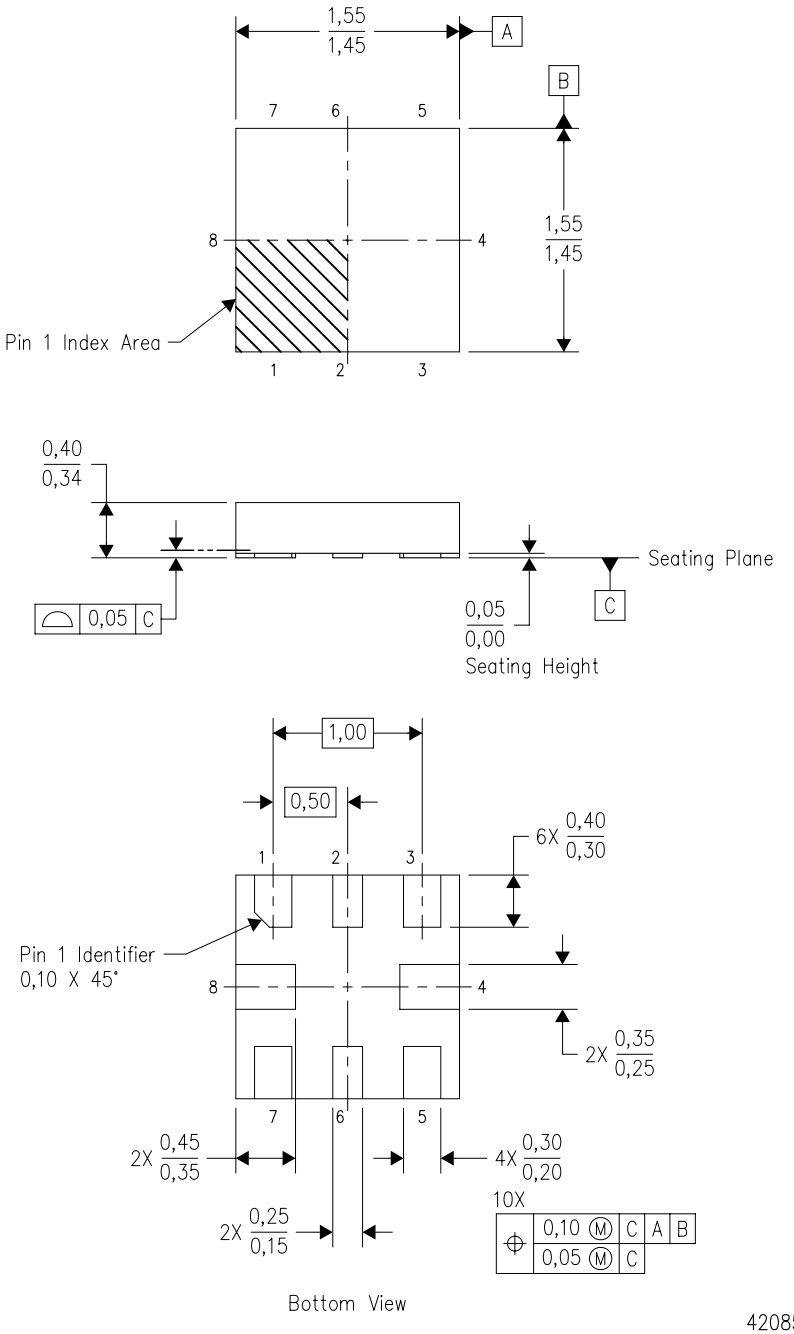
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

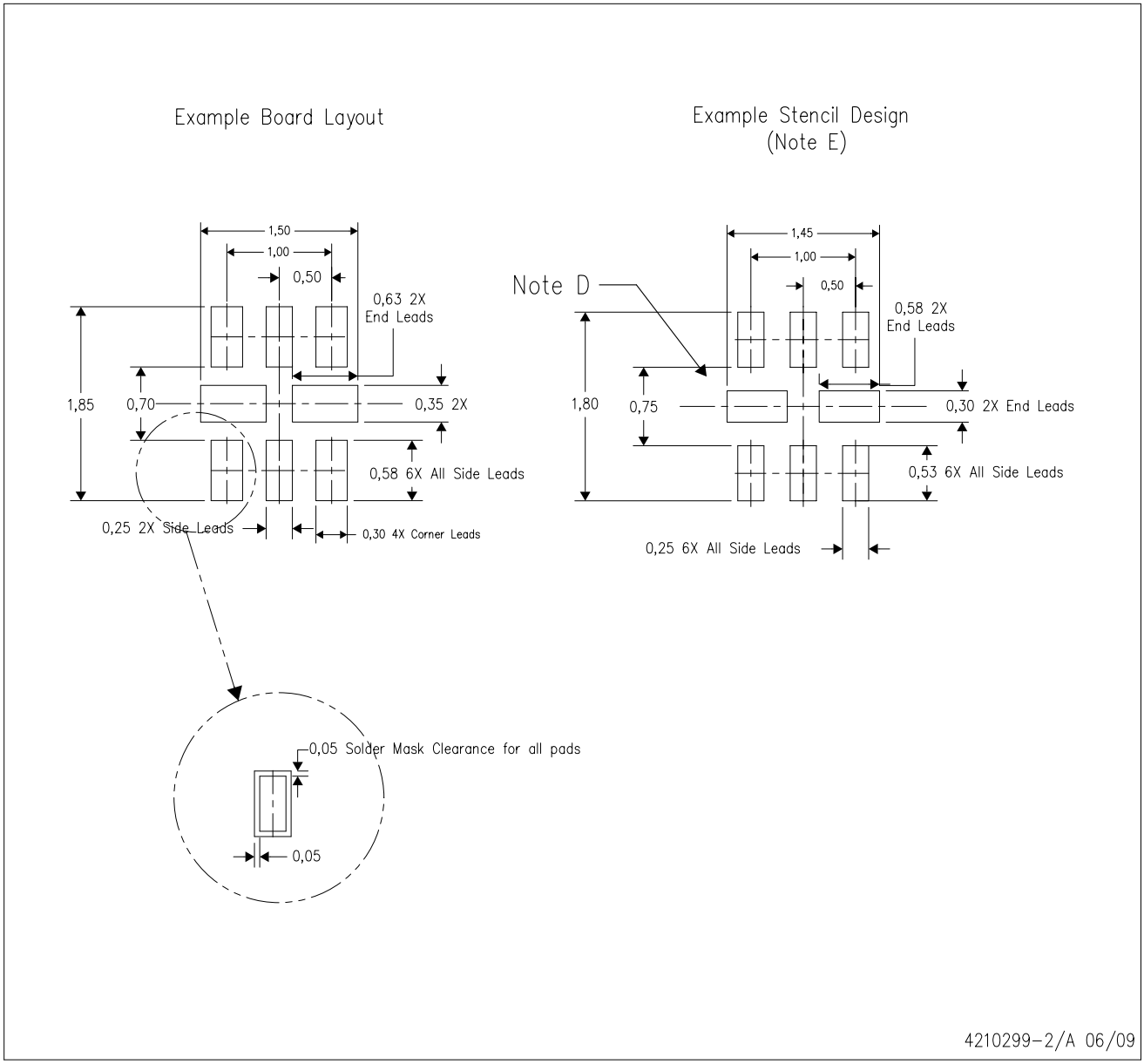
RUG (S–PQFP–N8) PLASTIC QUAD FLATPACK



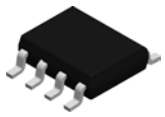
4208528–2/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2ECD.

RUG (R–PQFP–N8)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

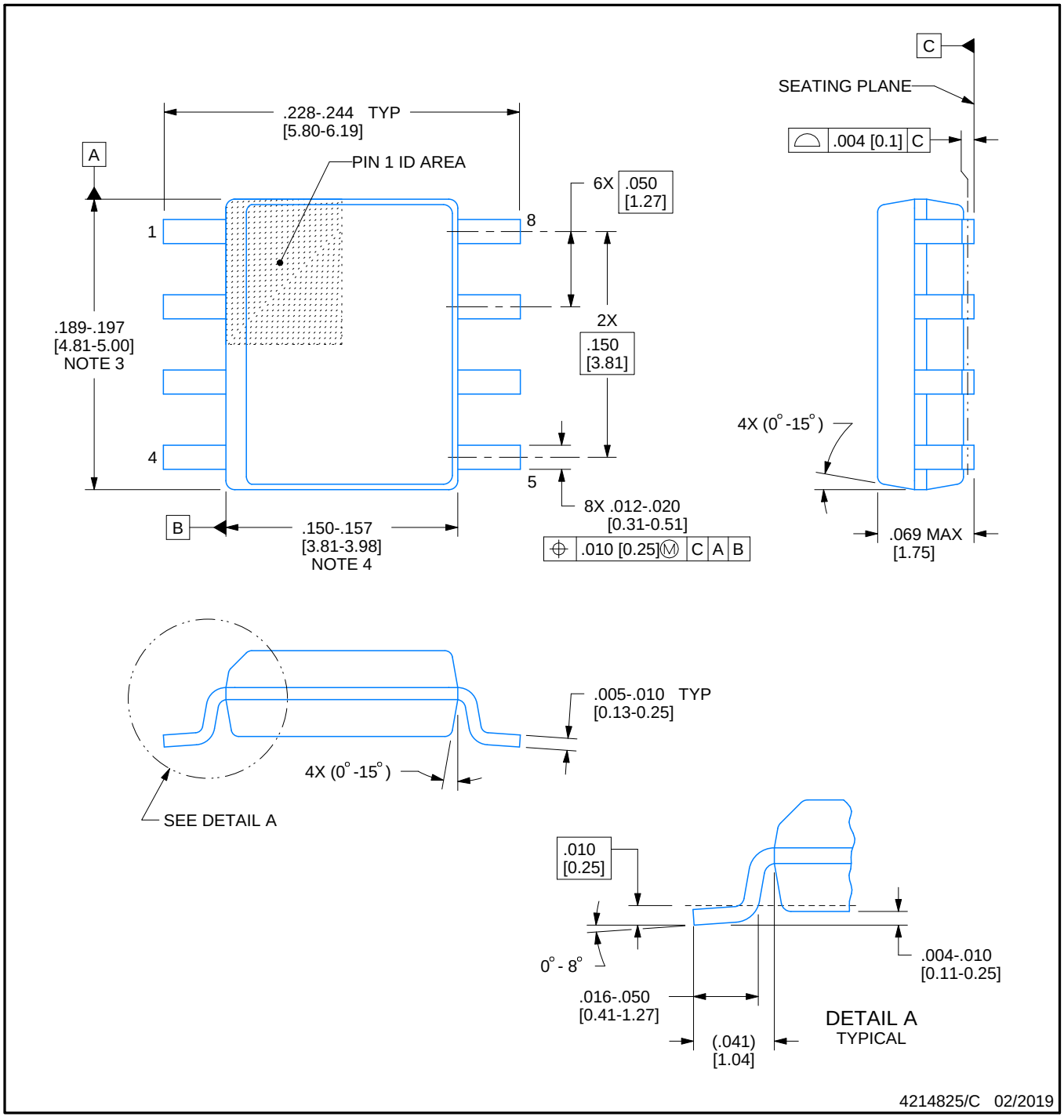


PACKAGE OUTLINE

D0008A

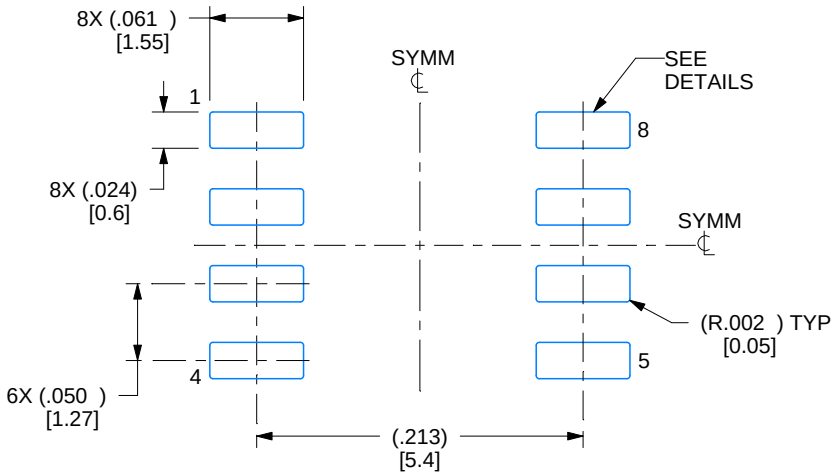
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

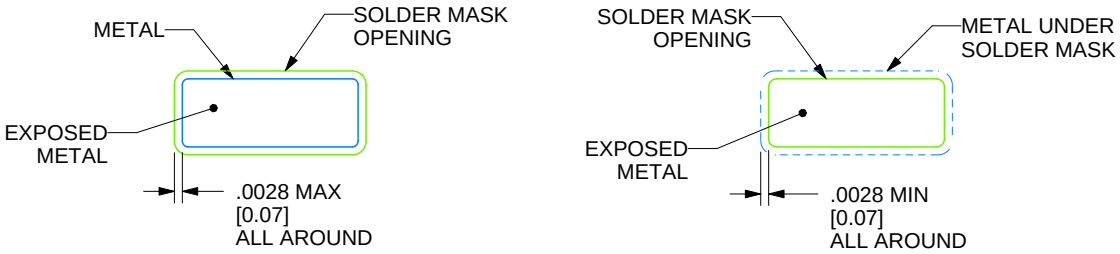


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

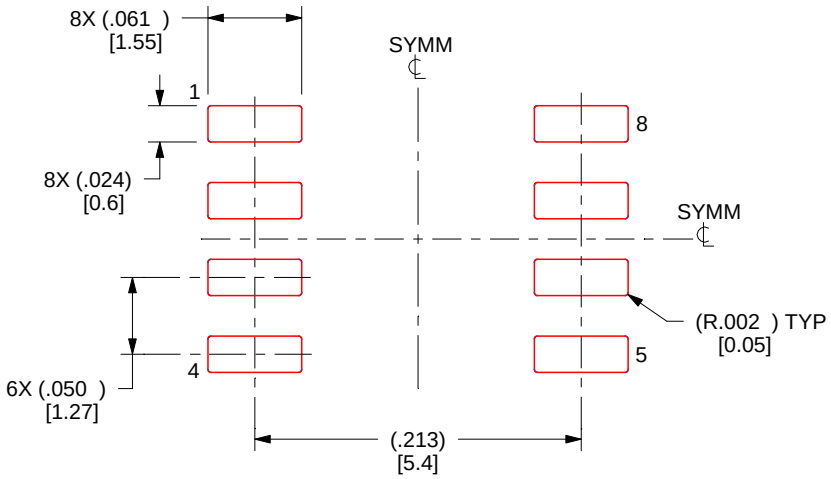
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

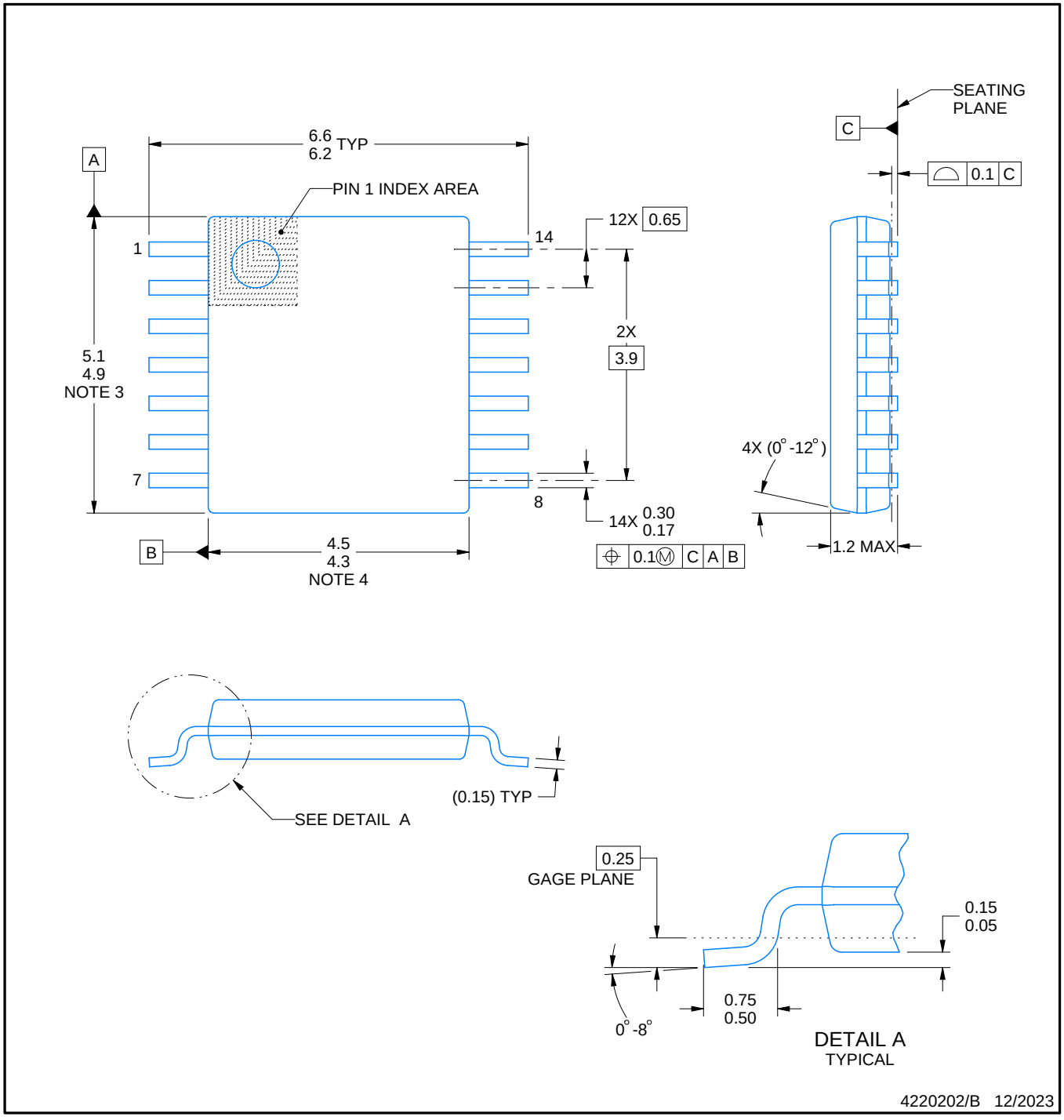
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

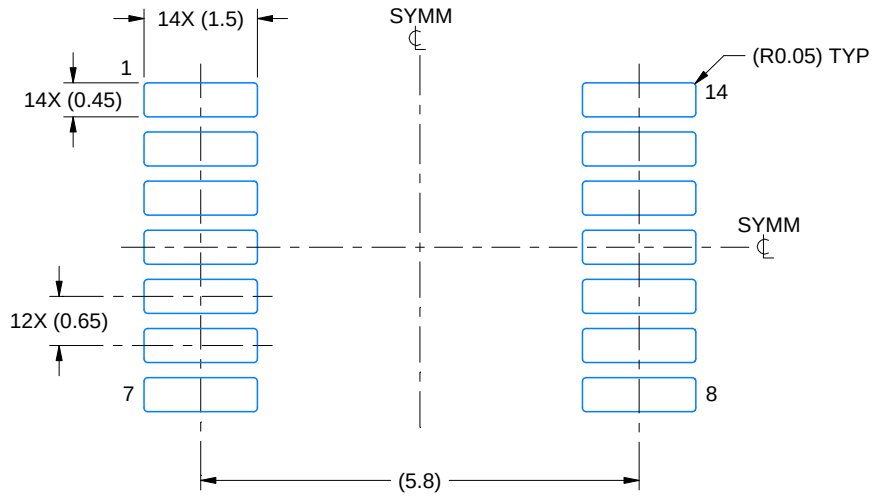
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

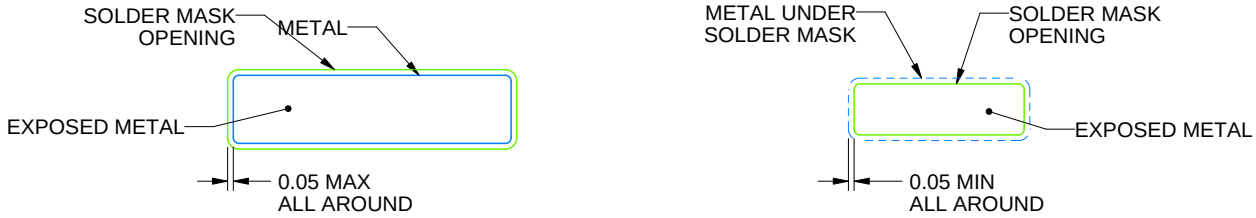


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

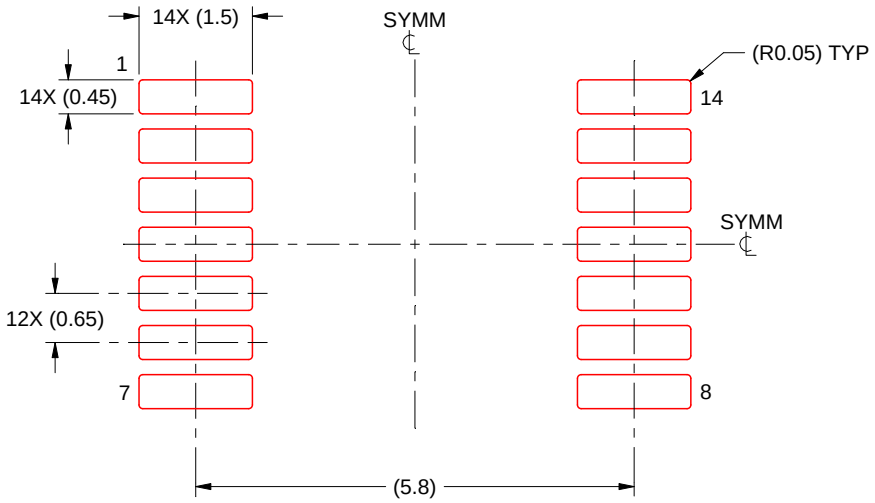


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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