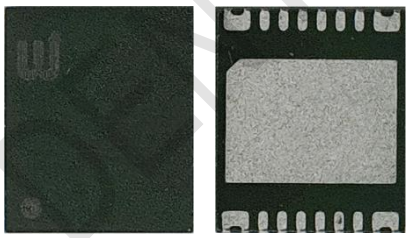
# WSD7025AD

**Smart High-Side Power Switch Dual Channel，23mΩ，DFN5×6-16L ，*AEC-Q100 qualified***

## Application

- Suitable for resistive, inductive and capacitive loads
- Specially intended for automotive signal lamps
- Replaces electromechanical relays, fuses and discrete circuits

| Package Information | |
|---|---|
| **Package** | DFN5×6-16L |
| **Marking** | WSD7025AD |



## Basic Features

- Dual channel device
- Standby current <2.0μA
- 3.3 V and 5 V compatible logic inputs
- RoHS compliant and lead free
- AEC-Q100 qualified

## Product Summary

| Parameter | Symbol | Value |
|---|---|---|
| Max. DC supply voltage | $V_{CC}$ | 35V |
| Operating voltage range | $V_{NOM}$ | 4.5-28V |
| On-state resistance (per channel, Typ.) | $R_{ON}$ | 23mohm |
| Nominal load current (one channel active) | $I_{L(NOM)1}$ | 7.5A |
| Nominal load current (All channels active) | $I_{L(NOM)2}$ | 5A |
| Typical current sense ratio ($I_{OUT}$=3A) | K | 3160 |
| Current limitation (typ.) | $I_{LIMH}$ | 24A |
| Supply current in standby mode | $I_{STBY}$ | <2.0μA |

## Diagnostic Functions

- Multiplexed analog feedback of load current with high precision proportional current mirror
- Off-state open load detection
- Output short to $V_S$ detection

## Protection Functions

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Output short-circuit protection
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of $V_S$
- Thermal shutdown indication
- Electrostatic discharge protection

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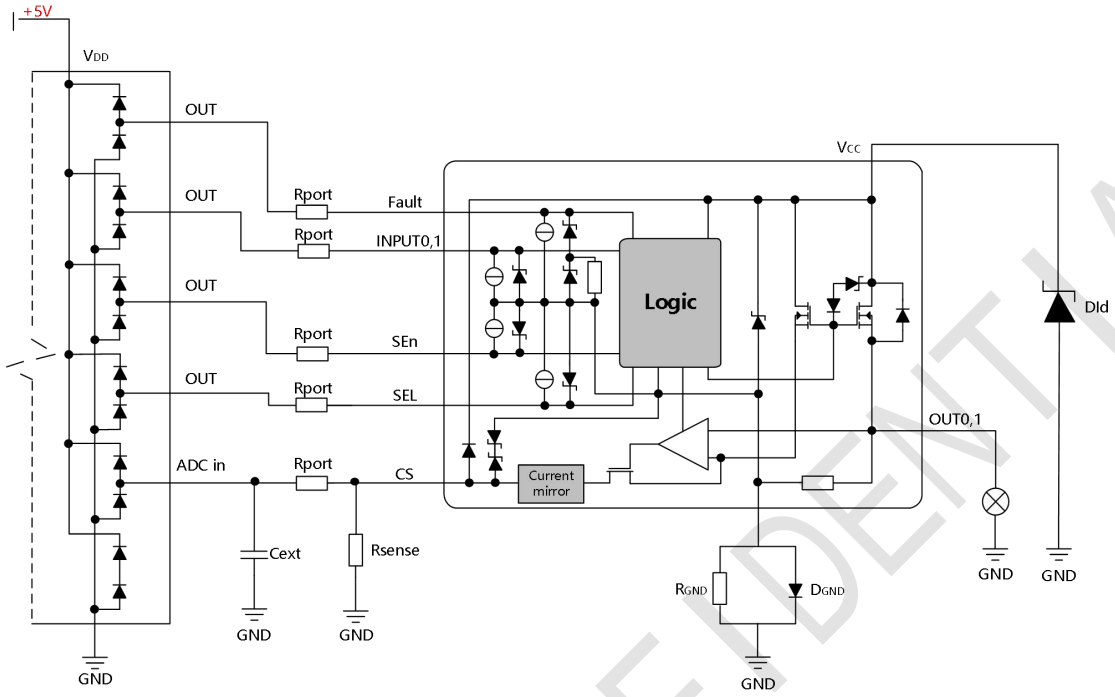
## Typical Application Circuit

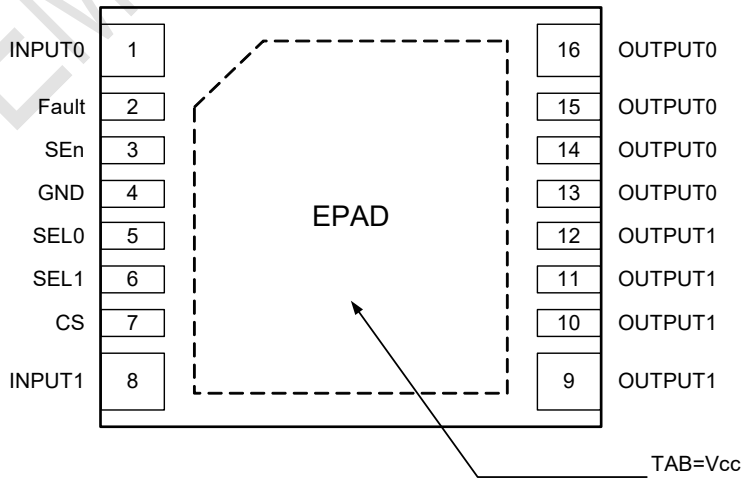



## Ordering Information

| Package | Top Mark | Part No. |
|---|---|---|
| 16-Pin DFN5×6-16L, Pb-free | WSD7025AD<br>XXYMXX | WSD7025AD |

## Pin Configuration

**Top view**




**DFN5×6-16L**

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## Pin Description

| Pin Name | Pin NO. | Pin Description |
|---|---|---|
| INPUT0/1 | 1/8 | Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state. |
| Fault | 2 | Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode. |
| SEn | 3 | Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the CS diagnostic pin. |
| GND | 4 | Ground connection. Must be reverse battery protected by an external diode / resistor network. |
| SEL0 | 5 | Active high compatible with 3 V and 5 V CMOS outputs pin; they address the CS multiplexer. |
| SEL1 | 6 | |
| CS | 7 | Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature. |
| OUTPUT1 | 9/10/11/12 | Power outputs. |
| OUTPUT0 | 13/14/15/16 | |
| $V_{CC}$ | EPAD | Battery connection. |

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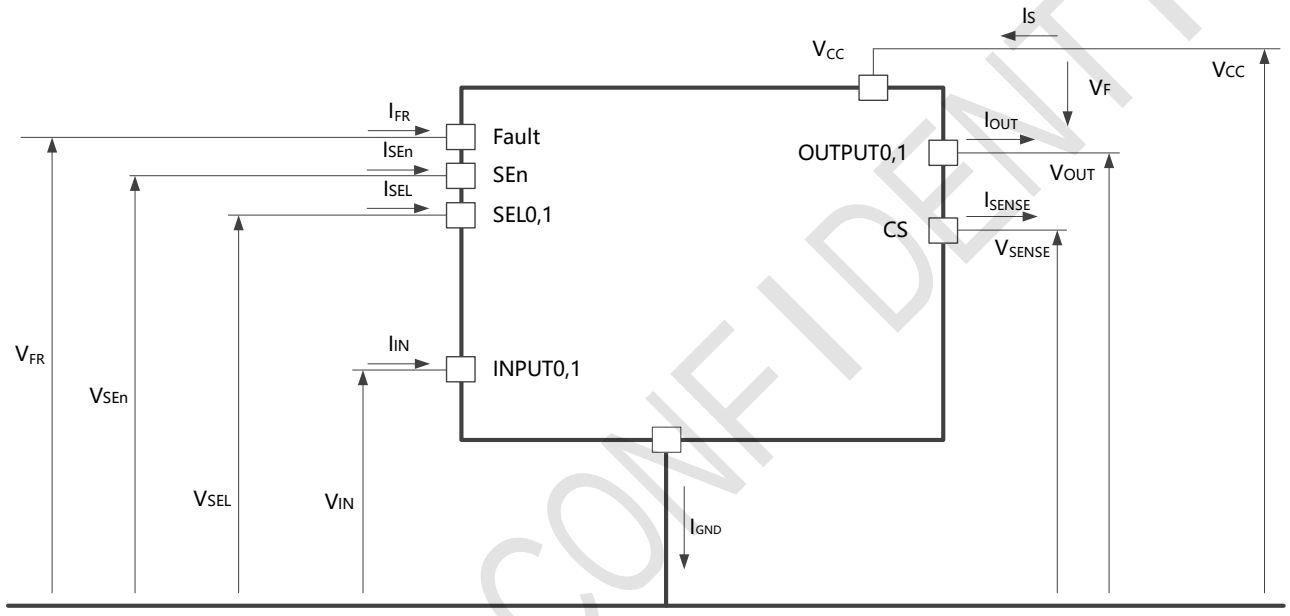
Table 1. Suggested connections for unused and not connected pins

| Connection / pin | CS | OUTPUT | INPUT | SEn, SEL0/1, Fault |
|---|---|---|---|---|
| Floating | Not allowed | X(1) | X | X |
| To ground | Through 1K resistor | Not allowed | Through 15K resistor | Through 15K resistor |

Note1：X do not care.

## Current and Voltage Conventions




Note2: $V_F = V_{OUT} - V_{CC}$ during reverse battery condition.

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## Absolute Maximum Ratings (Note3)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC supply voltage | 35 | V |
| $-V_{CC}$ | Reverse DC supply voltage | 0.3 | V |
| $-I_{GND}$ | DC reverse ground pin current | 200 | mA |
| $I_{OUT}$ | OUTPUT0,1 DC output current | Internally limited | A |
| $V_{IN}$, $V_{SEn}$, $V_{SEL}$, $V_{Fault}$ | INPUT0,1, SEn, SEL0,1, Fault DC input voltage | -0.3 to 6.0 | V |
| $I_{SENSE}$ | CS pin DC output current | 20 | mA |
| | CS pin DC output current in reverse | -20 | |
| $T_j$ | Junction operating temperature | -40 to 150 | ℃ |
| $T_{stg}$ | Storage temperature | -55 to 150 | |

Note3：Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

## Thermal Resistance (Note4)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{JC}$ | Thermal Resistance Junction-to-Case | 1.3 | ℃/W |
| $T_{JA}$ | Junction-to-Ambient Thermal Resistance | 35 | ℃/W |

Note4：According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

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## ESD Susceptibility (Note5)

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| $V_{ESD(HBM)}$ 3) | ESD Susceptibility all Pins (HBM) | ±2 | kV |
| $V_{ESD(HBM)_OUT}$ | ESD Susceptibility OUT vs GND and $V_{CC}$ connected (HBM) | ±4 | kV |
| $V_{ESD(CDM)}$ 4) | ESD Susceptibility all Pins (CDM) | ±500 | V |
| $V_{ESD(CDM)_CRN}$ | ESD Susceptibility Corner Pins (CDM) (pins 1, 8, 9, 16) | ±750 | V |

Note5：

1) Not subject to production test - specified by design.

2) Maximum digital input voltage to be considered for Latch-Up tests: 5.5 V.

3) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002.

4) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011.

## EAS/EAR Susceptibility (Note6)

| Symbol | Parameter | Values | | | Unit | Note or Test Conditon |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $E_{AS}$ | Maximum Energy Dissipation Single Pulse | | | 78 | mJ | $I_L = 2*I_{L(NOM)_85}$<br>$T_{J(0)}$ = 150 °C<br>$V_{CC}$ = 28 V |
| $E_{AR}$ | Maximum Energy Dissipation Repetitive Pulse | | | 25 | mJ | $I_L = I_{L(NOM)_85}$<br>$T_{J(0)}$ = 85°C<br>$V_{CC}$ = 13.5 V<br>1M Cycles |
| $\|I_L\|$ | Load Current | | | $I_{LIMH}$ | A | |

Note6:：Not subject to production test - specified by design.

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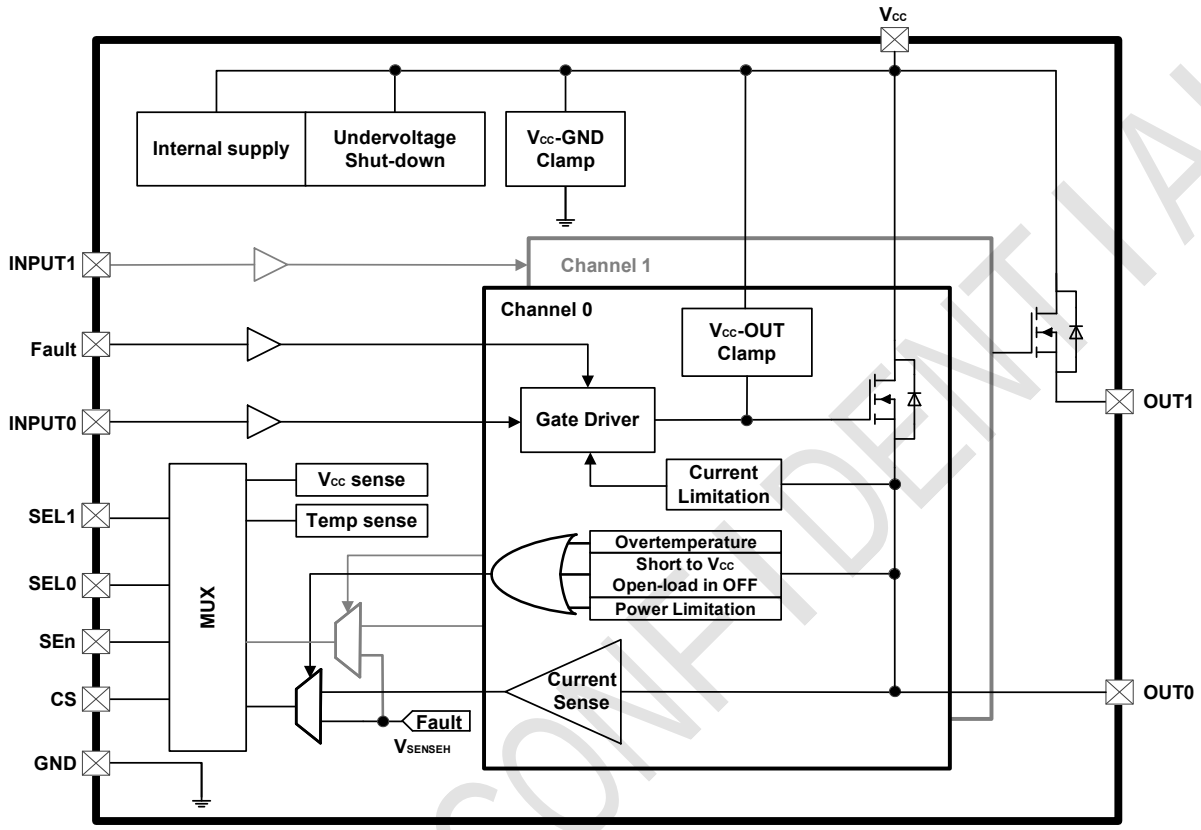
## Functional Block

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## Electrical Characteristics (Note7)

### Power section

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating supply voltage | $V_{CC}$ | | 4.5 | 13 | 28 | V |
| Under voltage shutdown | $V_{USD}$ | | | | 4.5 | V |
| Under voltage shutdown reset | $V_{USDReset}$ | | | | 5 | V |
| Under voltage shutdown hysteresis | $V_{USDhyst}$ | | | 0.3 | | V |
| On-state resistance | $R_{ON}$ | $I_{OUT}$=3A,$V_{SEn}$=5V, $T_j$ = 25℃ | | 23 | | mΩ |
| | | $I_{OUT}$=3A, $V_{SEn}$=5V,$T_j$ =150℃ | | | 60 | |
| | | $I_{OUT}$=3A, $V_{SEn}$=5V,$V_{CC}$ =4.5V, $T_j$ = 25℃ | | | 50 | |
| Nominal load current (One Channel Active) | $I_{L(NOM)1}$ | $T_A$=25℃ | | 7.5 | | A |
| Nominal load current at $T_A$=85℃ (One Channel Active) | $I_{L(NOM)1_85}$ | $T_A$=85℃, $T_j$ < 150℃ | | 6 | | A |
| Nominal load current (All Channels Active) | $I_{L(NOM)2}$ | $T_A$=25℃ | | 5 | | A |
| Nominal load current at $T_A$=85℃ (All Channels Active) | $I_{L(NOM)2_85}$ | $T_A$=85℃, $T_j$ < 150℃ | | 4 | | A |
| Inverse Current Capability | $I_{L(INV)}$ | $V_{CC}$<$V_{OUT}$, $V_{IN}$=5V, $T_A$=25℃ | | 7.5 | | A |
| $V_{CC}$ clamp voltage | $V_{clamp}$ | $I_S$=20 mA, 25℃ < $T_j$ < 150℃ | 35 | 42 | 48 | V |
| | | $I_S$ = 20 mA, $T_j$ =-40℃ | 33 | | | |
| Supply current in standby at $V_{CC}$ = 13 V | $I_{STBY}$ | $V_{CC}$ = 13V, $V_{IN}$=$V_{OUT}$=$V_{FR}$=$V_{SEn}$=0V $V_{SEL0,1}$ = 0 V, $T_j$ =25℃ | | | 2.0 | μA |
| | | $V_{CC}$ =13V, $V_{IN}$=$V_{OUT}$=$V_{FR}$=$V_{SEn}$ =0V, $V_{SEL0,1}$ = 0 V, $T_j$= 125℃ | | | 6.0 | μA |
| Standby mode blanking time | $t_{D_STBY}$ | $V_{CC}$=13V, $V_{IN}$=$V_{OUT}$=$V_{FR}$ =$V_{SEL0,1}$=0V $V_{SEn}$=5 V to 0 V | 100 | 400 | 800 | us |
| Supply current | $I_{S(ON)}$ | $V_{CC}$=13V, $V_{SEn}$=$V_{FR}$ =$V_{SEL0,1}$=0V, $V_{IN0,1}$=5V, $I_{OUT0,1}$=0A | | 6 | 12 | mA |
| Control stage current consumption in ON state | $I_{GND(ON)}$ | $V_{CC}$=13V, $V_{SEn}$=5V, $V_{FR}$=$V_{SEL0,1}$=0V $V_{IN0,1}$=5V, $I_{OUT0,1}$=1A | | | 12 | mA |
| Off-state output current at $V_{CC}$ =13V | $I_{L(off)}$ | $V_{IN}$ =$V_{OUT}$=0V, $V_{CC}$ =13V, $T_j$ =25℃ | 0 | 0.05 | 0.5 | μA |
| | | $V_{IN}$ =$V_{OUT}$=0V, $V_{CC}$ =13V, $T_j$ =125℃ | 0 | | 3.0 | μA |
| Output - $V_{CC}$ diode voltage at $T_j$=150℃ | $V_F$ | $I_{OUT}$ =-0.2A, $T_j$ =150℃ | | | 0.9 | V |

### Switching/$V_{CC}$ = 13 V, -40℃ < $T_j$< 150℃, unless otherwise specified

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Turn-on delay time at $T_j$ = 25℃ | $T_{d\ (on)}$ | $V_{CC}$=13V,$V_{SEn}$=5V,$R_L$=4.3Ω | 10 | 40 | 120 | us |
| Turn-off delay time at $T_j$ = 25℃ | $T_{d\ (off)}$ | | 10 | 75 | 120 | us |
| Turn-on voltage slope at $T_j$ = 25℃ | $(dV_{OUT}/dt)_{on}$ | $V_{CC}$=13V,$V_{SEn}$=5V,$R_L$=4.3Ω | 0.05 | 0.2 | 0.7 | V/us |
| Turn-off voltage slope at $T_j$ = 25℃ | $(dV_{OUT}/dt)_{off}$ | | 0.05 | 0.5 | 0.7 | |
| Differential pulse skew($t_{PHL}$ - $t_{PLH}$) | $t_{SKEW}$ | $V_{CC}$=13V,$V_{SEn}$=5V,$R_L$=4.3Ω | -50 | | 60 | us |

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| Logic input (IN0,1, Fault, SEL0,1, SEn) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Logic input low level voltage | $V_{LOW}$ | | | | 0.9 | V |
| Low level logic input current | $I_{LOW}$ | $V_{INL}$=0.9V | 0.5 | | | uA |
| Logic input high level voltage | $V_{HIGH}$ | | 2.1 | | 6.0 | V |
| High level logic input current | $I_{HIGH}$ | $V_{INH}$=2.1V | | | 24 | uA |
| Logic input hysteresis voltage | $V_{(hyst)}$ | | 0.1 | 0.3 | 0.7 | V |
| **Protections (7 V < $V_{CC}$< 18 V, -40℃ < $T_j$ < 150℃)** | | | | | | |
| **Parameter** | **Symbol** | **Test Condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| DC short circuit current | $I_{LIMH}$ | $V_{CC}$=13V,$V_{SEn}$=5V | 12 | 24 | 36 | A |
| | | 4.5V < $V_{CC}$< 18V ,$V_{SEn}$=5V | | | 36 | |
| Short circuit current during thermal cycling | $I_{LIML}$ | $V_{CC}$=13V, $V_{SEn}$=5V, $T_R$< $T_j$< $T_{TSD}$ | | 9 | | |
| Shutdown temperature | $T_{TSD}$ | | 150 | 175 | 200 | ℃ |
| Thermal hysteresis | $T_{HYST}$ | | | 20 | | ℃ |
| Dynamic temperature | $\Delta T_{J_SD}$ | $T_j$ = -40℃, $V_{CC}$=13V | | 60 | | ℃ |
| Current limit thermal hysteresis | $T_R$ | | | 40 | | ℃ |
| Fault reset time for output unlatch | $t_{LATCH_RST}$ | $V_{Fault}$ =5V to 0V, $V_{SEn}$=5V<br>E.g. Ch0<br>$V_{IN0}$=5V, $V_{SEL0}$=$V_{SEL1}$=0V | 3 | 20 | 60 | us |
| Turn-off output voltage clamp | $V_{DEMAG}$ | $I_{OUT}$=3A, $V_{SEn}$=5V, L= 6mH, $T_j$ = -40℃ | $V_{CC}$-33 | | | V |
| | | $I_{OUT}$=3A, $V_{SEn}$=5V, L= 6mH, $T_j$ =25℃ to 150℃ | $V_{CC}$-35 | $V_{CC}$-38 | $V_{CC}$-43 | |
| **Current sense / 7 V < $V_{CC}$< 18 V, -40℃ < $T_j$ < 150℃** | | | | | | |
| **Parameter** | **Symbol** | **Test Condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Current sense clamp voltage | $V_{SENSE_CL}$ | $V_{SEn}$=0V, $I_{SENSE}$ =1mA | | -15 | | V |
| | | $V_{SEn}$=0V, $I_{SENSE}$ = -1mA | | 7 | | |
| **Chip temperature analog feedback** | | | | | | |
| **Parameter** | **Symbol** | **Test Condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| CS output voltage proportional to chip temperature | $V_{SENSE_TC}$ | $V_{SEn}$ =5V, $V_{SEL0}$ =0V, $V_{SEL1}$=5V, $V_{IN0,1}$=0V, $R_{SENSE}$=1K, $T_j$ = -40℃ | 2.325 | 2.42 | 2.495 | V |
| | | $V_{SEn}$=5V, $V_{SEL0}$ =0V, $V_{SEL1}$=5V, $V_{IN0,1}$=0V, $R_{SENSE}$=1K, $T_j$= 25℃ | 1.985 | 2.07 | 2.155 | V |
| | | $V_{SEn}$=5V, $V_{SEL0}$ =0V, $V_{SEL1}$=5V, $V_{IN0,1}$=0V, $R_{SENSE}$=1K, $T_j$ = 150℃ | 1.285 | 1.35 | 1.425 | V |
| Temperature coefficient | $dV_{SENSE_TC}/dT$ | Tj = -40°C to 150°C | | -5.50 | | mV/K |
| **$V_{CC}$ supply voltage analog feedback** | | | | | | |
| **Parameter** | **Symbol** | **Test Condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| CS output voltage proportional to $V_{CC}$ supply voltage | $V_{SENSE_VCC}$ | $V_{CC}$ =13V, $V_{SEn}$=5V, $V_{SEL0}$= $V_{SEL1}$=5V, $V_{IN0,1}$=0V, $R_{SENSE}$ =1K | 2.52 | 2.6 | 2.68 | V |
| Transfer function | | $V_{SENSE_VCC}$ = $V_{CC}$ / 5 | | | | |

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## Current sense characteristics

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{OUT}/I_{SENSE}$ | $K_1$ | $I_{OUT}$=0.5A, $V_{SEn}$=5V | -50% | 2100 | +50% | |
| $I_{OUT}/I_{SENSE}$ | $K_2$ | $I_{OUT}$=1A, $V_{SEn}$=5V | -30% | 2680 | +30% | |
| $I_{OUT}/I_{SENSE}$ | $K_3$ | $I_{OUT}$=3A, $V_{SEn}$=5V | -15% | 3160 | +15% | |
| $I_{OUT}/I_{SENSE}$ | $K_4$ | $I_{OUT}$=8A, $V_{SEn}$=5V | -10% | 3360 | +10% | |
| Current sense leakage current | $I_{SENSE0}$ | CS disabled: $V_{SEn}$ =0V | 0 | | 0.5 | uA |
| | | CS disabled: -1V<$V_{SENSE}$<5V | -0.5 | | 3 | |
| | | CS enabled: $V_{SEn}$ = 5 V; All channels ON; $I_{OUTX}$ = 0 A; ChX diagnostic selected; • E.g. Ch0: $V_{IN0}$ = 5V; $V_{IN1}$ = 5V; $V_{SEL0}$ = 0V; $V_{SEL1}$ = 0V; $I_{OUT0}$ = 0A; $I_{OUT1}$ = 1A | 0 | | 150 | |
| | | CS enabled: $V_{SEn}$ = 5 V; All channels ON; $I_{OUTX}$ = 0 A; ChX diagnostic selected; • E.g. Ch0: $V_{IN0}$ = 0V; $V_{IN1}$ = 5V; $V_{SEL0}$ = 0V; $V_{SEL1}$ = 0V; $I_{OUT0}$ = 0A; $I_{OUT1}$ = 1A | 0 | | 2 | |
| Output voltage for CS shutdown | $V_{OUT_MSD}$ | $V_{SEn}$ = 5 V, $R_{SENSE}$ = 2.7K, $V_{IN0}$= 5 V; $V_{SEL0}$ = $V_{SEL1}$= 0 V, $I_{OUT0}$= 1A | | 5 | | V |
| CS saturation voltage | $V_{SENSE_SAT}$ | $V_{CC}$=7V,$R_{SENSE}$=2.7K,$V_{SEn}$=5V,$V_{IN0}$=5 V, $V_{SEL0}$=$V_{SEL1}$= 0 V, $I_{OUT0}$ =2 A, $T_j$ =150 ℃ | 5 | | | V |
| CS saturation current | $I_{SENSE_SAT}$ | $V_{CC}$=7V, $V_{SENSE}$=4V, $V_{IN0}$=5V, $V_{SEn}$=5V, $V_{SEL0}$= $V_{SEL1}$=0V, $T_j$ = 150 ℃ | 4 | | | mA |
| Output saturation current | $I_{OUT_SAT}$ | $V_{CC}$=7V, $V_{SENSE}$=4V, $V_{IN0}$=5V, $V_{SEn}$=5V, $V_{SEL0}$= $V_{SEL1}$=0V, $T_j$ = 150 ℃ | 10 | | | A |

## OFF-state diagnostic

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| OFF-state open load voltage detection threshold | $V_{OL}$ | $V_{SEn}$=5V, $V_{IN}$=0V, $V_{SEL0}$= $V_{SEL1}$= 0 V | 2 | 3 | 4 | V |
| OFF-state output sink current | $I_{L(off2)}$ | $V_{IN}$ = 0 V, $V_{OUT}$ = $V_{OL}$,$T_j$ = -40℃ to 150℃ | -300 | -150 | -50 | uA |
| OFF-state diagnostic delay time from falling edge of INPUT | $t_{DSTKON}$ | $V_{SEn}$=5V, $V_{IN0}$= 5V to 0 V, $V_{SEL0}$= $V_{SEL1}$= 0V, $V_{OUT0}$ = 4 V, $I_{OUT0}$ = 0A | 100 | 350 | 700 | us |
| Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn | $t_{D_OL_V}$ | $V_{IN0}$=0V,$V_{Fault}$=0V,$V_{SEL0}$=$V_{SEL1}$=0V, $V_{OUT0}$=4V, $V_{SEn}$ = 0 V to 5 V | | | 150 | us |
| OFF-state diagnostic delay time from rising edge of $V_{OUT}$ | $t_{D_VOL}$ | $V_{SEn}$=5V,$V_{IN0}$=0V,$V_{SEL0}$=$V_{SEL1}$=0V, $V_{OUT0}$= 0 V to 4 V | | 5 | 30 | us |

## Fault diagnostic feedback

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|

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| | | | | | | |
|---|---|---|---|---|---|---|
| Current sense output voltage in fault condition | $V_{SENSEH}$ | $V_{CC}$=13V, $R_{SENSE}$ =1K, $V_{IN0}$=0V, $V_{SEn}$ = 5V,$V_{SEL0}$= $V_{SEL1}$=0V, $I_{OUT0}$=0A,$V_{OUT0}$=4V | 5.0 | 6.0 | 6.6 | V |
| Current sense output current in fault condition | $I_{SENSEH}$ | $V_{CC}$=13V, $V_{SENSE}$ =5V | 10 | 20 | 30 | mA |
| **Current sense timings** | | | | | | |
| **Parameter** | **Symbol** | **Test Condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Current sense settling time from rising edge of SEn | $t_{DSENSE1H}$ | $V_{IN}$=5V, $V_{SEn}$=0V to 5V, $R_{SENSE}$=1K, $R_L$=13Ω | | | 100 | us |
| Current sense disable delay time from falling edge of SEn | $t_{DSENSE1L}$ | $V_{IN}$=5V, $V_{SEn}$=5V to 0V, $R_{SENSE}$=1K, $R_L$=13Ω | | 5 | 20 | us |
| Current sense settling time from rising edge of INPUT | $t_{DSENSE2H}$ | $V_{IN}$=0V to 5V, $V_{SEn}$=5 V, $R_{SENSE}$ =1K, $R_L$ =13Ω | | 80 | 250 | us |
| Current sense settling time from rising edge of $I_{OUT}$(dynamic response to a step change of $I_{OUT}$) | $\Delta t_{DSENSE2H}$ | $V_{IN}$=5V, $V_{SEn}$=5V, $R_{SENSE}$=1K, $I_{SENSE}$=90% of $I_{SENSEMAX}$, $R_L$=13Ω | | | 150 | us |
| Current sense turn-off delay time from falling edge of INPUT | $t_{DSENSE2L}$ | $V_{IN}$=5V to 0V, $V_{SEn}$=5V, $R_{SENSE}$=1K, $R_L$=13Ω | | 80 | 250 | us |
| $V_{SENSE_TC}$ settling time from rising edge of SEn | $t_{DSENSE3H}$ | $V_{SEn}$=0V to 5V, $V_{SEL0}$=0V, $V_{SEL1}$ = 5V, $R_{SENSE}$=1K | | | 60 | us |
| $V_{SENSE_TC}$ disable delay time from falling edge of SEn | $t_{DSENSE3L}$ | $V_{SEn}$=5V to 0V, $V_{SEL0}$=0V, $V_{SEL1}$ = 5V, $R_{SENSE}$=1K | | | 20 | us |
| $V_{SENSE_VCC}$ settling time from rising edge of SEn | $t_{DSENSE4H}$ | $V_{SEn}$=0V to 5V, $V_{SEL0}$=5V, $V_{SEL1}$ = 5V, $R_{SENSE}$=1K | | | 60 | us |
| $V_{SENSE_VCC}$ disable delay time from falling edge of SEn | $t_{DSENSE4L}$ | $V_{SEn}$=5V to 0V, $V_{SEL0}$=5V, $V_{SEL1}$ = 5V, $R_{SENSE}$=1K | | | 20 | us |
| Current sense transition delay from $Ch_X$ to $Ch_Y$ | $t_{D_XtoY}$ | $V_{IN0}$=$V_{IN1}$=$V_{SEn}$=5V, $V_{SEL1}$=0V, $V_{SEL0}$=0V to 5V, $I_{OUT0}$ =0A, $I_{OUT1}$=1.5A, $R_{SENSE}$ =1K | | | 60 | us |
| Current sense transition delay from current sense to $T_C$ sense | $t_{D_CStoTC}$ | $V_{IN0}$=5V, $V_{SEn}$=5V, $V_{SEL0}$=0V, $V_{SEL1}$=0V to 5V, $I_{OUT0}$=1.5A, $R_{SENSE}$=1K | | | 20 | us |
| Current sense transition delay from $T_C$ sense to current sense | $t_{D_TCtoCS}$ | $V_{IN0}$=5V, $V_{SEn}$=5V, $V_{SEL0}$=0V, $V_{SEL1}$=5V to 0V, $I_{OUT0}$=1.5A, $R_{SENSE}$=1K | | | 100 | us |
| Current sense transition delay from current sense to $V_{CC}$ sense | $t_{D_CStoVCC}$ | $V_{IN1}$=5V, $V_{SEn}$=5V, $V_{SEL0}$=5V, $V_{SEL1}$=0V to 5V, $I_{OUT1}$=1.5A, $R_{SENSE}$=1K | | | 20 | us |
| Current sense transition delay from $V_{CC}$ sense to current sense | $t_{D_VCCtoCS}$ | $V_{IN1}$=5V, $V_{SEn}$=5V, $V_{SEL0}$=5V, $V_{SEL1}$=5V to 0V, $I_{OUT1}$=1.5A, $R_{SENSE}$=1K | | | 100 | us |
| Current sense transition delay from $T_C$ sense to $V_{CC}$ sense | $t_{D_TCtoVCC}$ | $V_{CC}$=13 V, $V_{SEn}$=5V, $V_{SEL0}$=0V to 5V, $V_{SEL1}$=5V, $R_{SENSE}$=1K | | | 20 | us |
| Current sense transition delay from $V_{CC}$ sense to $T_C$ sense | $t_{D_VCCtoTC}$ | $V_{CC}$=13V, $V_{SEn}$=5V, $V_{SEL0}$=5V to 0V, $V_{SEL1}$=5V, $R_{SENSE}$=1K | | | 20 | us |
| Current sense transition delay from stable current sense on ChX to $V_{SENSEH}$ on ChY | $t_{D_CSotVSENSEH}$ | $V_{IN0}$ = 5 V, $V_{IN1}$ = 0 V, $V_{SEn}$ = 5 V, $V_{SEL1}$ = 0 V, $V_{SEL0}$ = 0 V to 5 V, $I_{OUT0}$ = 1.5A, $V_{OUT1}$ = 4V, $R_{SENSE}$=1K | | | 20 | us |

Note7: Except for the special test instructions, all electrical parameters are tested under $T_A$= +25℃. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis.

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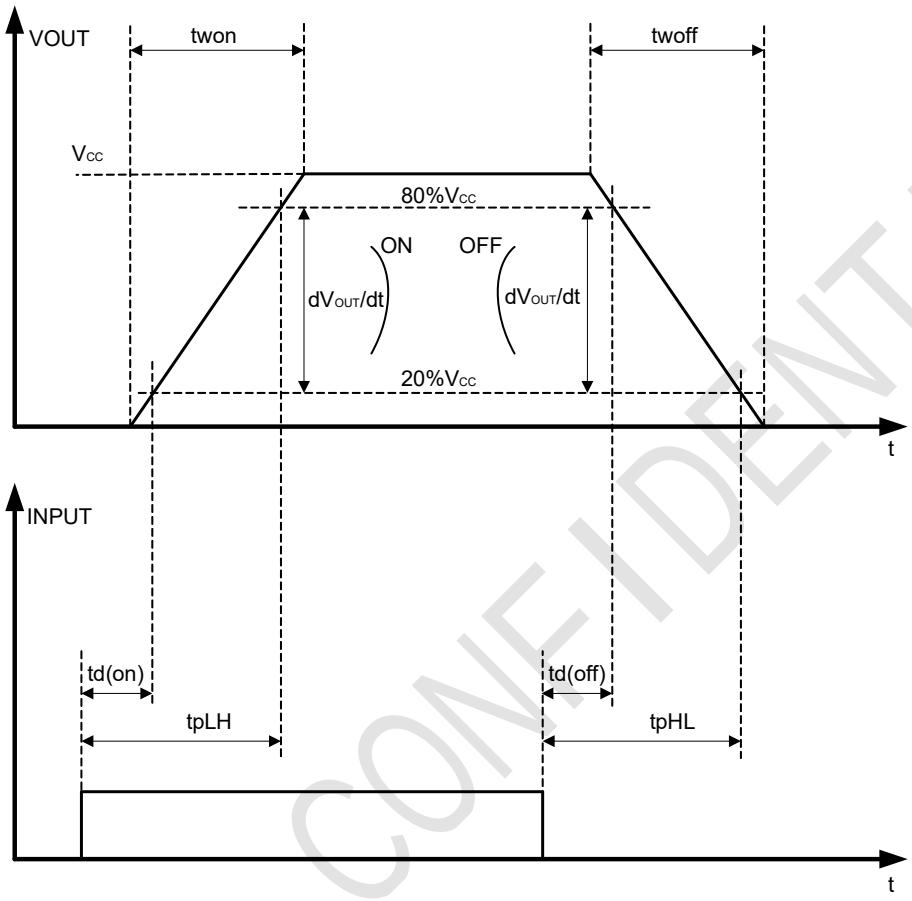
## Switching Status and Timing Relationship

### Switching time and pulse skew

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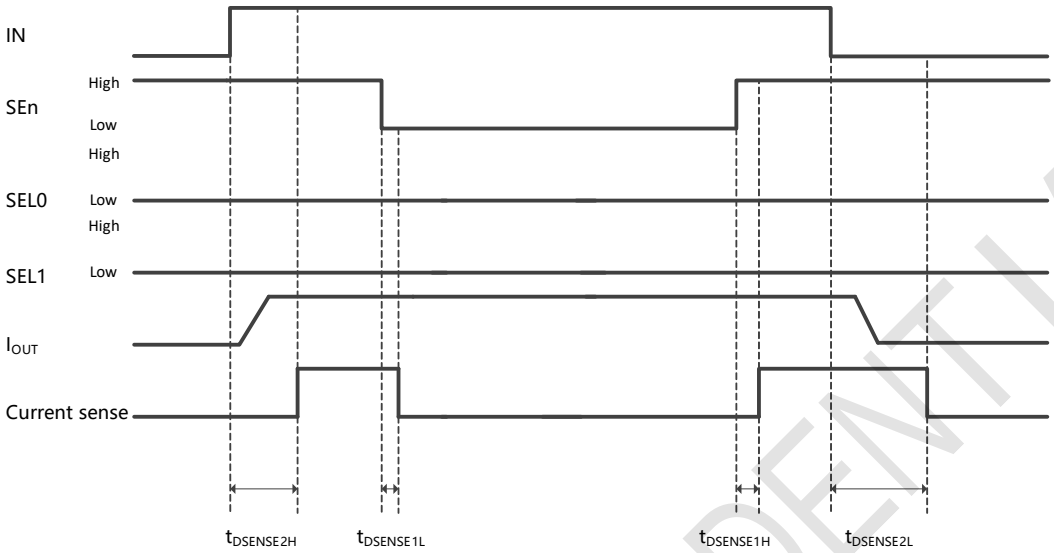
## Current sense timings (current sense mode)




## TDSTKON

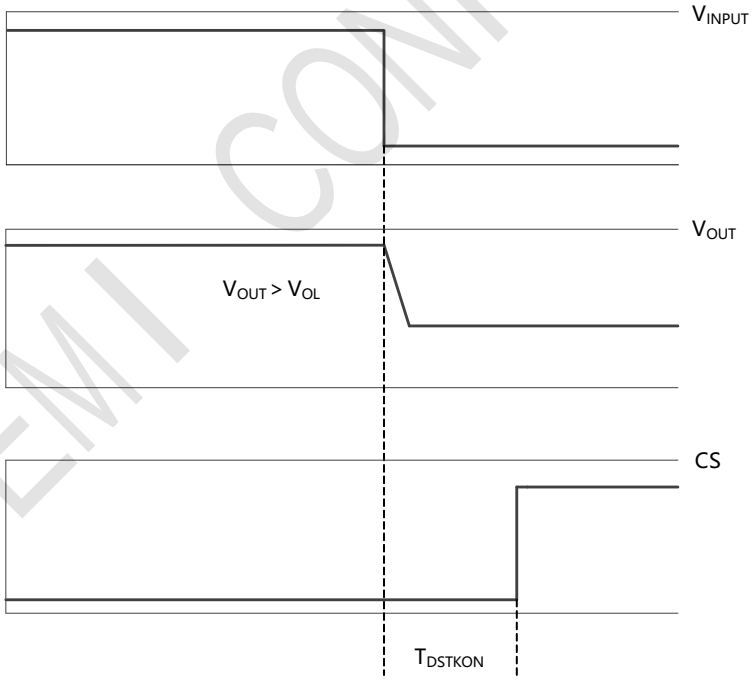



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Table 2. Truth table

| Mode | Conditions | $IN_X$ | FR | SEn | $SEL_X$ | $OUT_X$ | Current sense | Comments |
|---|---|---|---|---|---|---|---|---|
| Standby | All logic INs low | L | L | L | L | L | Hi-Z | Low quiescent current consumption |
| Normal | Nominal load connected; $T_j$ < 150℃ | L | X | See Table 3 | | L | See Table 3 | |
| | | H | L | | | H | See Table 3 | Outputs configured for auto-restart |
| | | H | H | | | H | See Table 3 | Outputs configured for latch-off |
| Overload | Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j_SD}$ | L | X | See Table 3 | | L | See Table 3 | |
| | | H | L | | | H | See Table 3 | Output cycles with temperature hysteresis |
| | | H | H | | | L | See Table 3 | Output latches-off |
| Undervoltage | $V_{CC} < V_{USD}$ | X | X | X | | L | Hi-Z | Re-start when $V_{CC} > V_{USD}$ + $V_{USDhyst}$ (rising ) |
| OFF-state diagnostics | Short to $V_{CC}$ | L | X | See Table 3 | | H | See Table 3 | |
| | Open-Load | L | X | | | H | See Table 3 | External pull-up |
| Negative output voltage | Inductive loads turn-off | L | X | See Table 3 | | <0 | See Table 3 | |

Table 3. Current sense output

| SEn | SEL1 | SEL0 | MUX Channel | Current sense output | | | |
|---|---|---|---|---|---|---|---|
| | | | | Normal | Overload | OFF-state | Negative output |
| L | X | X | | Hi-Z | | | |
| H | L | L | Channel 0 diagnostic | $I_{SENSE} = I_{OUT0}/K$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$ | Hi-Z |
| H | L | H | Channel 1 diagnostic | $I_{SENSE} = I_{OUT1}/K$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$ | Hi-Z |
| H | H | L | $T_{CHIP}$ Sense | $V_{SENSE} = V_{SENSE_TC}$ | | | |
| H | H | H | $V_{CC}$ Sense | $V_{SENSE} = V_{SENSE_VCC}$ | | | |

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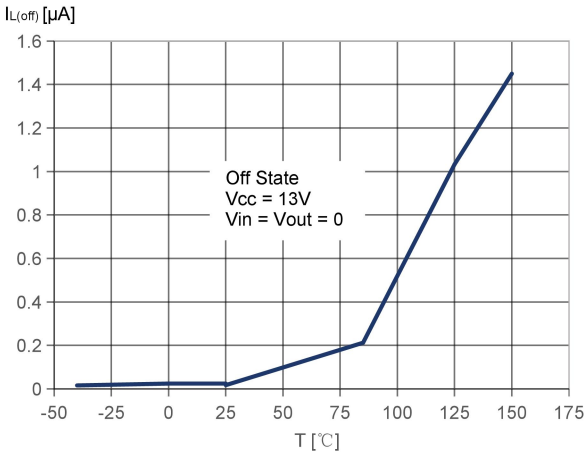
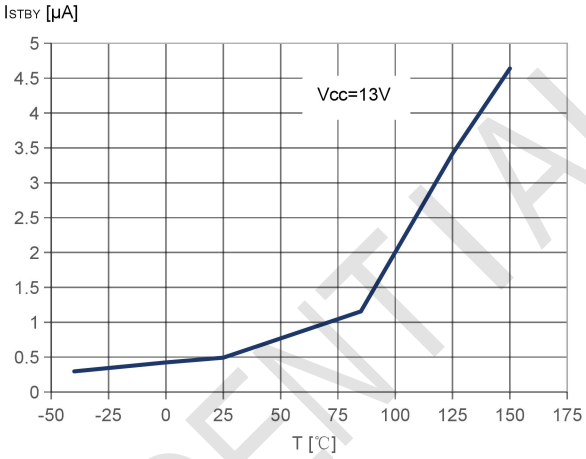
## Electrical Characteristics Curves

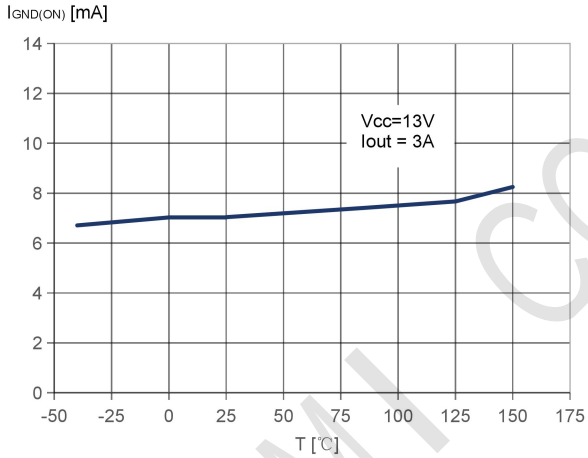
### OFF-state output current



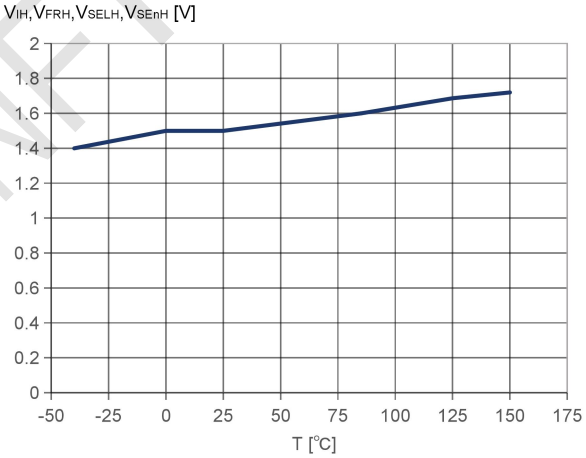

### Standby current



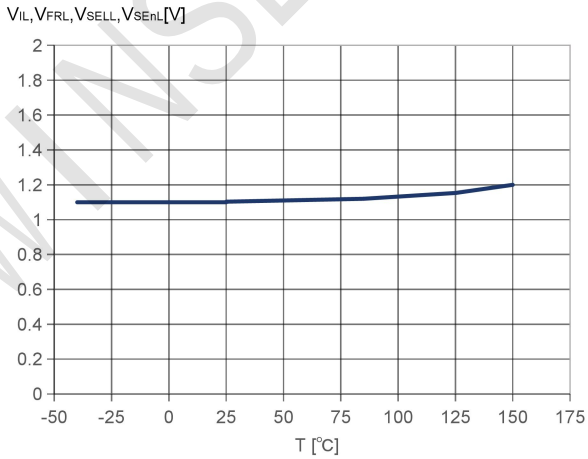

### IGND(ON) vs. TA



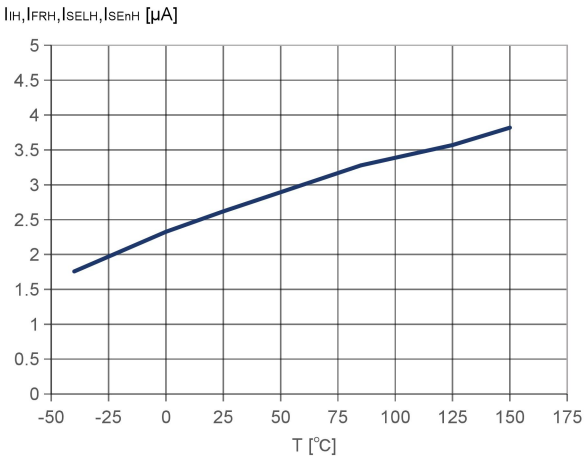

### Logic Input high level voltage




### Logic Input Low level voltage




### High level logic input current

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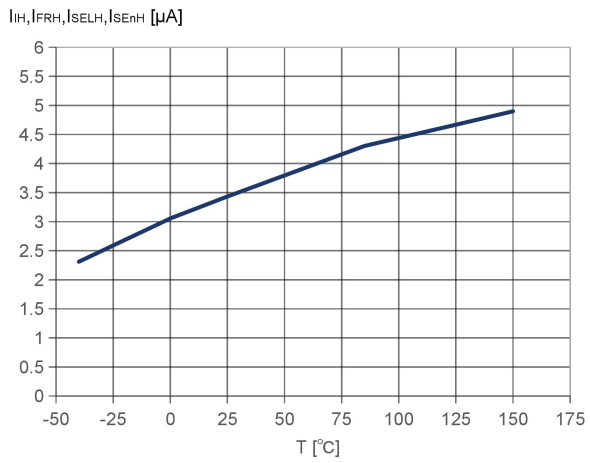
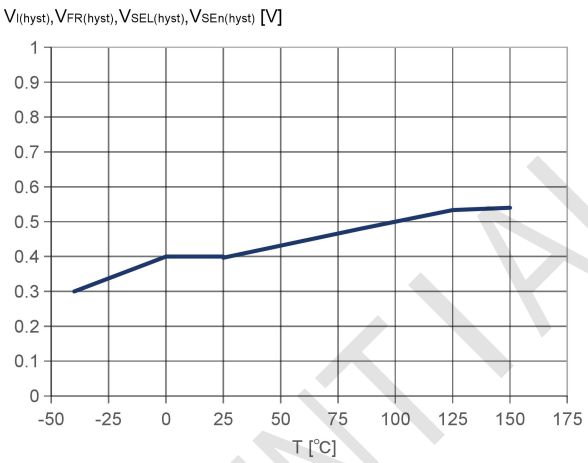
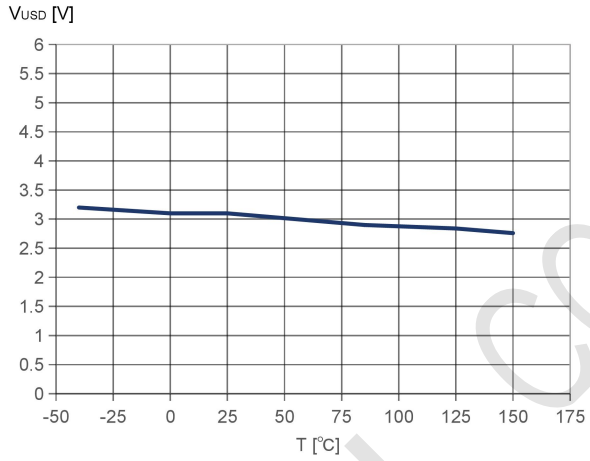
## Low level logic input current



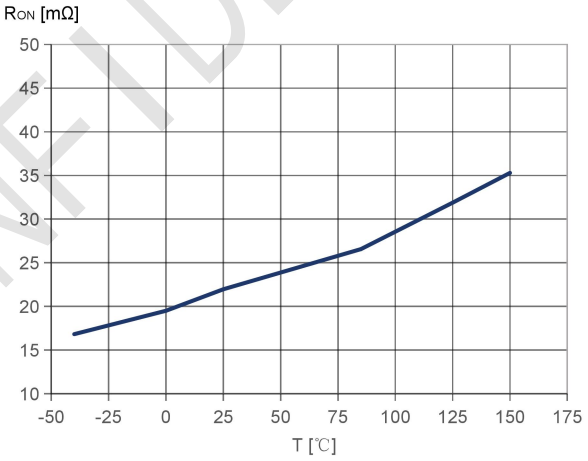

## Logic Input hysteresis voltage



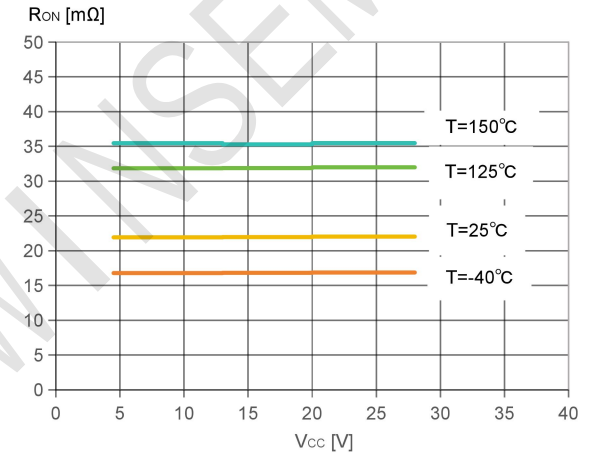

## Undervoltage shutdown



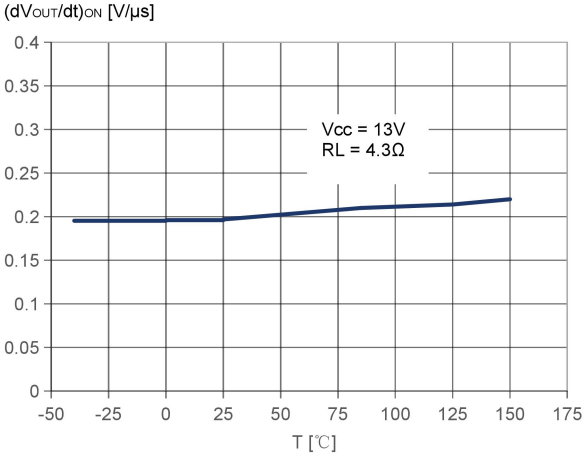

## On-state resistance vs. TA




## On-state resistance vs. TA




## Turn-on voltage slope

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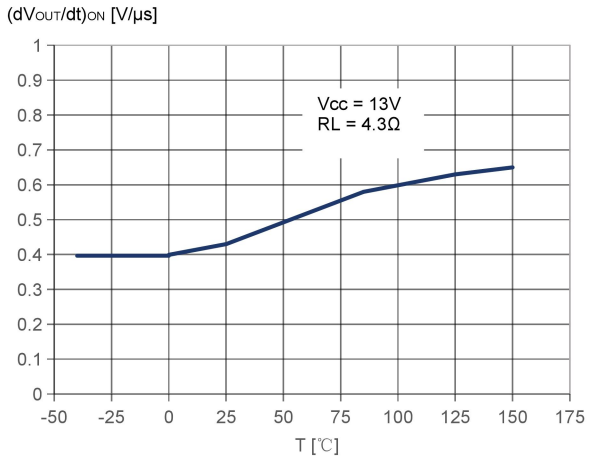
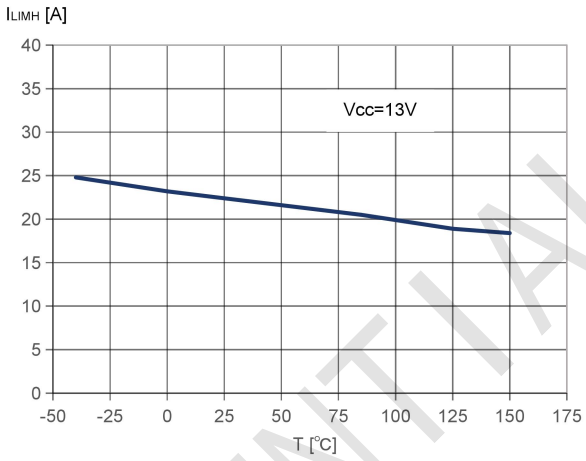
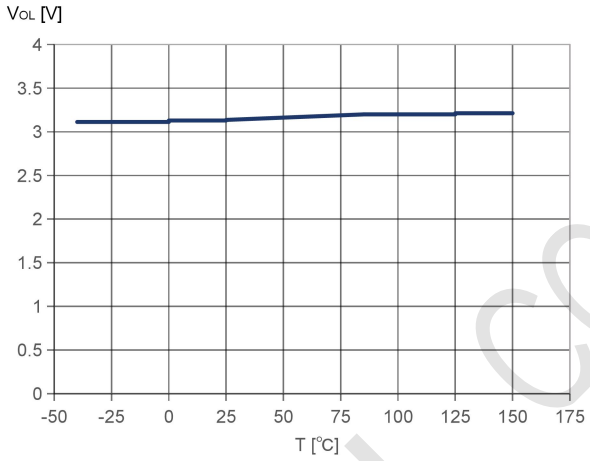
### Turn-off voltage slope



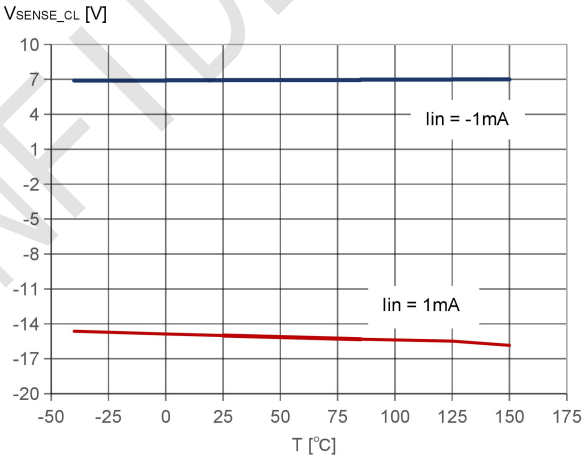

### ILIMH vs. TA



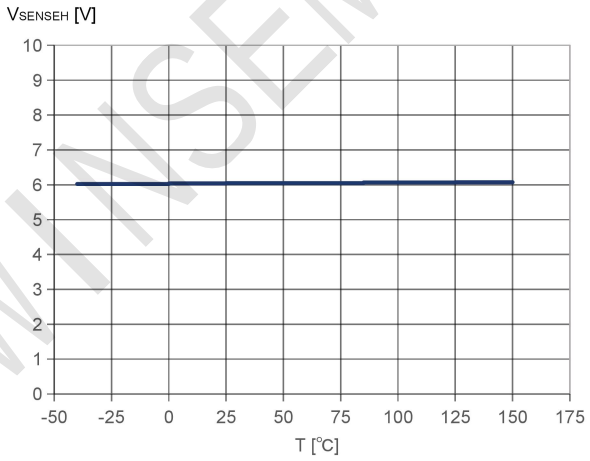

### OFF-state open-load voltage detection threshold



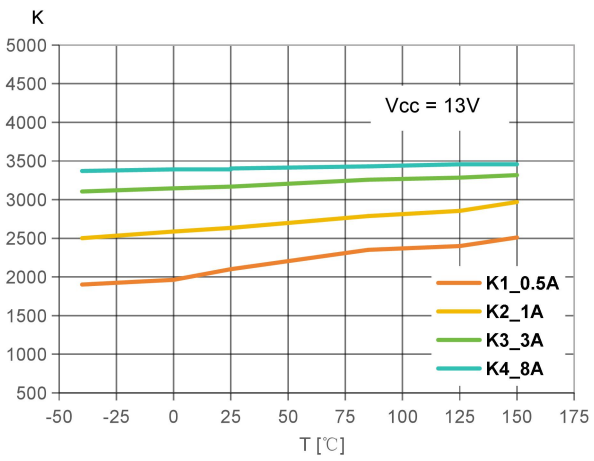

### VSENSE Clamp vs. TA




### VSENSEH vs. TA




### IOUT/ISENSE vs. TA

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# Functional Description

## Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing $\Delta T_j$ through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as $\Delta T_j$ exceeds the safety level of $\Delta T_{j_SD}$. According to the voltage level on the Fault pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (Fault = Low) or remains off (Fault = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

## Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175℃), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the Fault pin, the device switches on again as soon as its junction temperature drops to $T_R$ (Fault = Low) or remains off (Fault = High).

## Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, $I_{LIMH}$, by operating the output power MOSFET in the active region.

## Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, $V_{DEMAG}$, allowing the inductor energy to be dissipated without damaging the device.

## Diode ($D_{GND}$) in the ground line

A resistor (typ.$R_{GND}$=4.7K) should be inserted in parallel to $D_{GND}$ if the device drives an inductive load. This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

## MCU I/Os protection

If a ground protection network is used and negative transients are present on the $V_{CC}$ line, the control pins will be pulled negative. WS suggests to insert a resistor ($R_{prot}$=15K) in line both to prevent the micro-controller I/O pins from latching-up and to protect the HSD inputs. The value of these resistors is a compromise between the leakage current of micro-controller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of micro-controller I/Os.

## CS - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (CS) delivering the following signals:

- Current monitor: current mirror of channel output current
- $V_{CC}$ monitor: voltage proportional to $V_{CC}$
- $T_{CASE}$: voltage proportional to chip temperature

Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in CS multiplexer addressing Table.

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## Current monitor

When current mode is selected in the CS, this output is capable to provide:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to known ratio named K
- Diagnostics flag in fault conditions delivering fixed voltage $V_{SENSEH}$

The current delivered by the current sense circuit, $I_{SENSE}$ can be easily converted to a voltage $V_{SENSE}$ by using an external sense resistor, $R_{SENSE}$, allowing continuous load monitoring and abnormal condition detection.

While device is operating in normal conditions (no fault intervention), $V_{SENSE}$ calculation can be done using simple equations.

Current provided by CS output: $I_{SENSE} = I_{OUT}/K$

Voltage on $R_{SENSE}$: $V_{SENSE} = R_{SENSE}*I_{SENSE} = R_{SENSE}* I_{OUT}/K$

Where:

- $V_{SENSE}$ is voltage measurable on $R_{SENSE}$ resistor
- $I_{SENSE}$ is current provided from CS pin in current output mode

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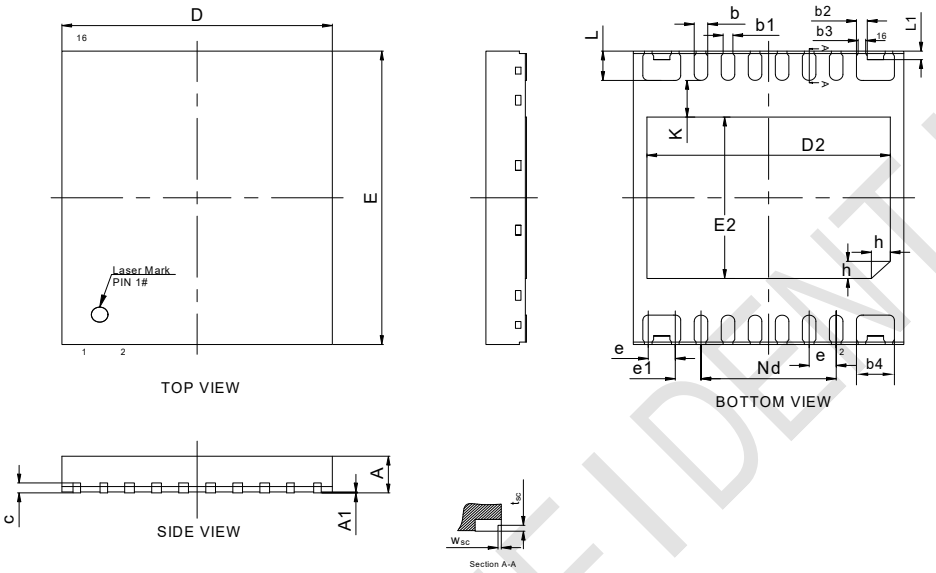
## Package Outline

### DFN5×6-16L




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| b1 | | 0.18REF | |
| b2 | 0.15 | 0.20 | 0.25 |
| b3 | | 0.14REF | |
| b4 | 0.65 | 0.70 | 0.75 |
| c | | 0.203REF | |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 4.40 | 4.50 | 4.60 |
| e | | 0.50BSC | |
| e1 | | 0.475BSC | |
| Nd | | 2.50BSC | |
| E | 5.90 | 6.00 | 6.10 |
| E2 | 3.20 | 3.30 | 3.40 |
| L | 0.55 | 0.60 | 0.65 |
| L1 | 0.16 | 0.21 | 0.26 |
| h | 0.30 | 0.35 | 0.40 |
| K | | 0.75REF | |
| $W_{SC}$ | 0.01 | - | 0.09 |
| $t_{SC}$ | 0.08 | - | 0.18 |

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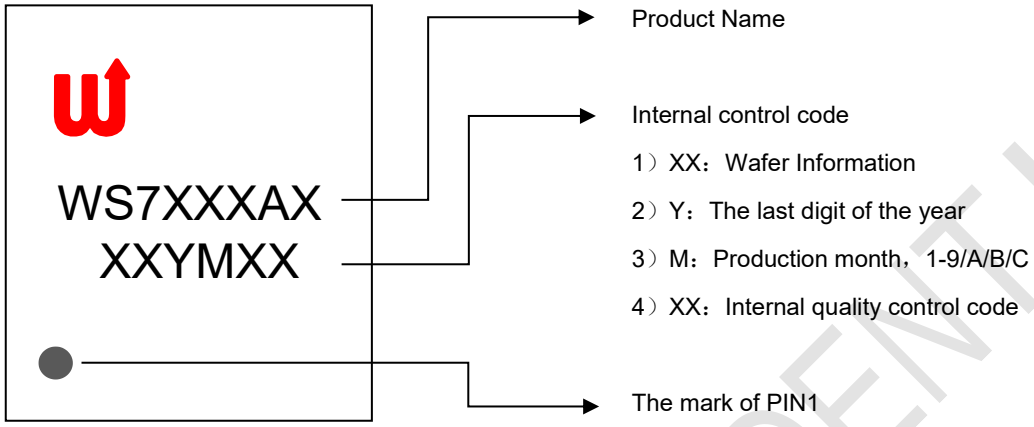
## Marking Information

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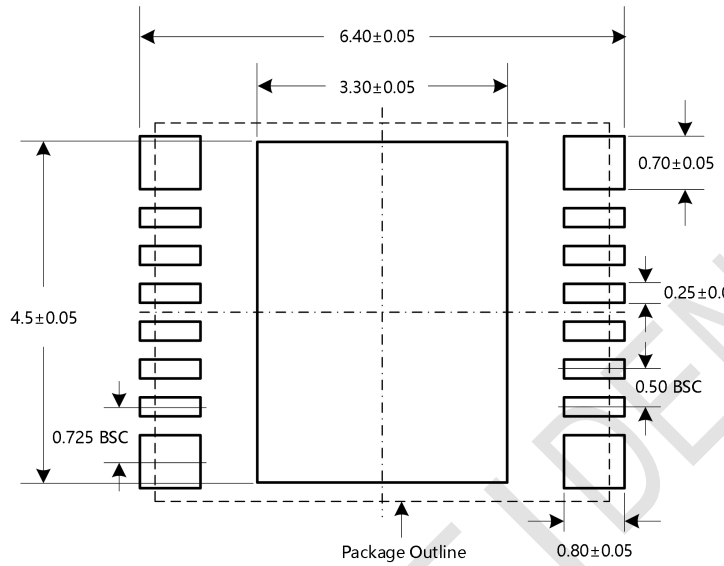
## Soldering Footprint

**DFN5×6-16L**

**Unit：mm**




**Recommended Solder PAD Pitch AND Dimensions**

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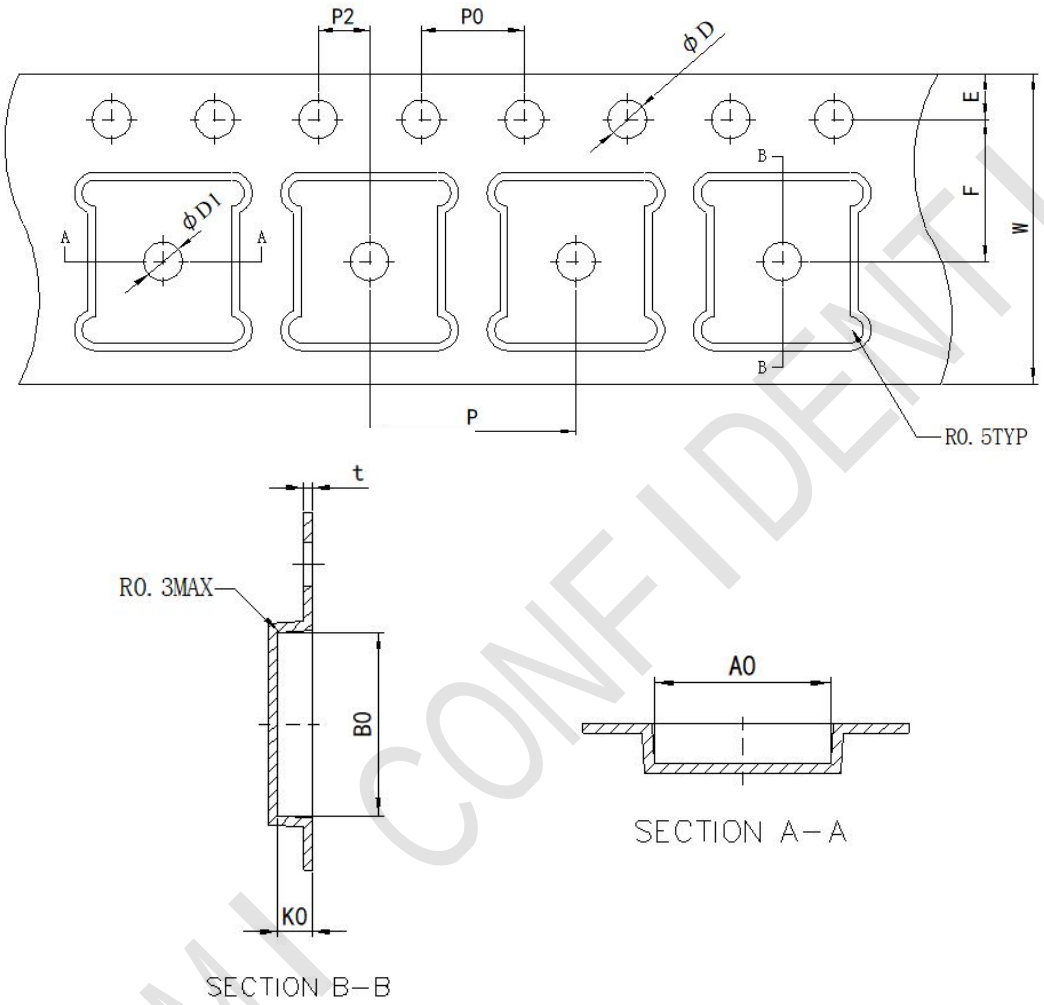
## Tape and Reel Information

**DFN5×6-16L Carrier tape**




DFN5×6-16L Carrier Tape Dimensions

| Description | Value（Unit：mm） |
|---|---|
| E | 1.75±0.10 |
| F | 5.50±0.05 |
| P2 | 2.00±0.05 |
| D | 1.50±0.1 |
| D1 | 1.50 MIN |
| P0 | 4.00±0.10 |
| W | 12.00±0.1 |
| P | 8.00±0.10 |
| A0 | 5.30±0.10 |
| B0 | 6.30±0.10 |
| K0 | 1.20±0.10 |

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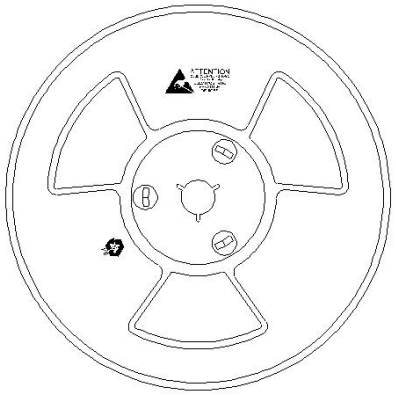
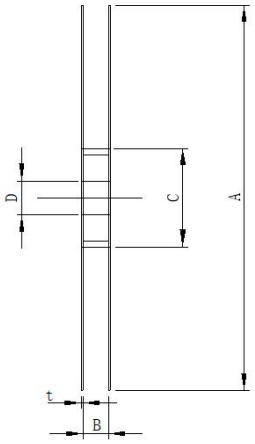
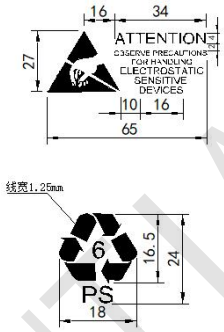
**DFN5×6-16L Reel（13 " ）**






DFN5×6-16L Reel Dimensions

| Description | Value（Unit：mm） |
|---|---|
| Carrier width | 12 |
| A | 329±1 |
| B | 12.4+2 |
| C | 100±1 |
| D | 13.3±0.3 |
| t | 2.0±0.3 |

Tape and Reel Information

| Package | Reel | QTY/Reel | Reel/Inner Box | Inner Box/Carton | QTY/Carton | Inner Box Size (mm) | Carton Size （mm） |
|---|---|---|---|---|---|---|---|
| DFN5×6-16L | 13 " | 3000 | 1 | 8 | 24000 | 336×336×48 | 420×355×365 |

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**CONTACT**

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