MP6543C

22V, 1.2A Three-Phase BLDC Motor Driver with Three Integrated Half-Bridges

DESCRIPTION

The MP6543C is a three-phase brushless DC (BLDC) motor driver with three integrated half-bridges, consisting of six N-channel power MOSFETs, as well as six pre-drivers, two gate driver power supplies, and three current-sense amplifiers. Each half-bridge includes an enable (EN) input and pulse-width modulation (PWM) input. The MP6543C can achieve up to 1.2A of continuous output current (I_{OUT}) across a 3V to 22V input voltage (V_{IN}) range.

The internal current-sense circuit does not require a low-ohmic shunt resistor. Each half-bridge has an independent ground pin (LSSA, LSSB, and LSSC) that allows current to be measured via an external shunt resistor. This allows the MP6543C to be used for different application requirements.

An internal charge pump generates the gate driver supply voltage for the high-side MOSFETs (HS-FETs). A trickle-charge circuit maintains a sufficient gate driver voltage for 100% duty cycle operation.

Full protection features include configurable over-current protection (OCP), under-voltage lockout protection (UVLO), and thermal shutdown.

The MP6543C is available in a QFN-24 (3mmx4mm) package with an exposed thermal pad.

FEATURES

- 3V to 22V Operating Input Voltage (V_{IN}) Range
- Three Integrated Half-Bridge Drivers
- 1.2A Continuous Output Current (I_{OUT})
- 110mΩ $R_{DS(ON)}$ per MOSFET
- Enable (EN) Input and Pulse-Width Modulation (PWM) Input
- 3.3V, 100mA Built-In Low-Dropout (LDO) Regulator
- Internal Charge Pump for 100% Duty Cycle
- Automatic Synchronous Rectification
- Integrated Bidirectional Current-Sense Amplifiers
- Configurable Over-Current Protection (OCP)
- Under-Voltage Lockout (UVLO) Protection
- Thermal Shutdown
- Available in a QFN-24 (3mmx4mm) Package

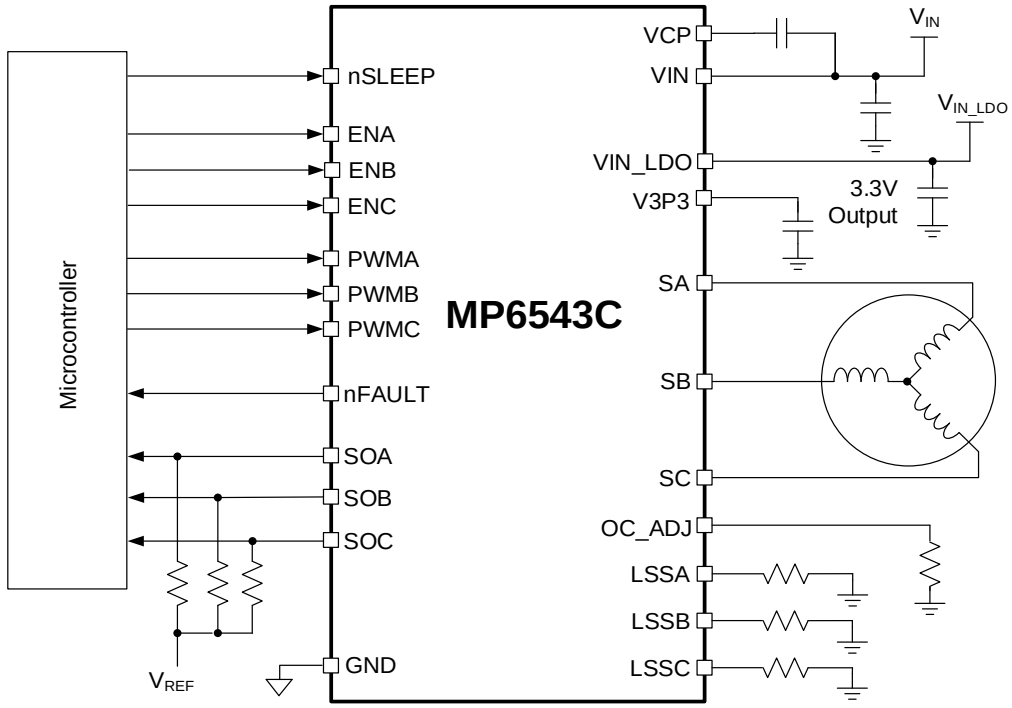
APPLICATIONS

- Three-Phase Brushless DC (BLDC) Motor Drivers

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6543CGL*	QFN-24 (3mmx4mm)	*See Below*	1

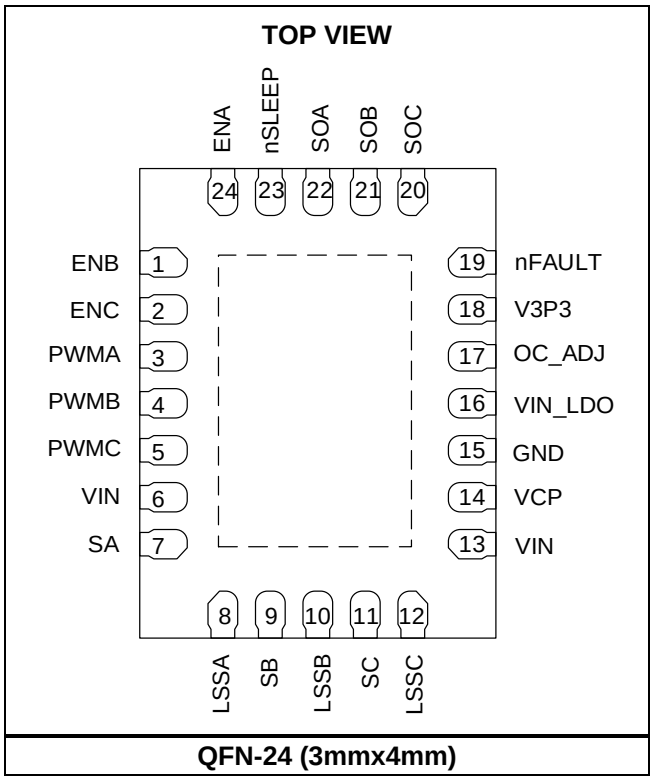
* For Tape & Reel, add suffix -Z (e.g. MP6543CGL-Z).

TOP MARKING

MPYW
6543
CLLL

MP: MPS prefix
Y: Year code
W: Week code
6543C: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-24 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	ENB	**Phase B enable input.**
2	ENC	**Phase C enable input.**
3	PWMA	**Phase A pulse-width modulation (PWM) input.**
4	PWMB	**Phase B PWM input.**
5	PWMC	**Phase C PWM input.**
6, 13	VIN	**Input supply voltage.**
7	SA	**Phase A output.**
8	LSSA	**Phase A low-side MOSFET (LS-FET) source connection.**
9	SB	**Phase B output.**
10	LSSB	**Phase B LS-FET source connection.**
11	SC	**Phase C output.**
12	LSSC	**Phase C LS-FET source connection.**
14	VCP	**Charge pump output.** Connect the VCP and VIN pins using a 1µF, 16V ceramic capacitor with X7R dielectrics.
15	GND	**Ground.**
16	VIN_LDO	**LDO input.**
17	OC_ADJ	**Over-current protection (OCP) configurable current limit pin.**
18	V3P3	**3.3V regulator output and LS-FET gate driver supply voltage.** Use a 4.7µF capacitor to bypass the V3P3 pin to GND.
19	nFAULT	**Fault indicator.** This pin is an open-drain output, and is logic low if a fault occurs.
20	SOC	**Phase C current-sense output.**
21	SOB	**Phase B current-sense output.**
22	SOA	**Phase A current-sense output.**
23	nSLEEP	**Sleep mode input.** Pull the nSLEEP pin low to enter low-power sleep mode; pull nSLEEP high to exit sleep mode. nSLEEP has an internal pull-down resistor.
24	ENA	**Phase A enable input.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}, V_{IN_LDO}).....-0.3V to +25V
V_{Sx}.....-0.3V to V_{IN} + 0.3V
V_{CP} .....-0.3V to V_{IN} + 5V
LSSx to GND .....-0.3V to +0.3V
All other pins .....-0.3 to +5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (3mmx4mm)…….... 2.6W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM)..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....3V to 22V
Output current (I_{OUT}) (4)..... 1.2A
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-24 (3mmx4mm)…….....48 .....10.....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Continuous current depends on the PCB layout and ambient temperature.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 18V, T_A = 25°C, LSSA = LSSB = LSSC = GND = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input voltage	V_{IN}		3		22	V
LDO input voltage	V_{IN_LDO}		3		22	V
Quiescent current	I_Q	nSLEEP = 1, ENx = 0		2.5	3.2	mA
	I_{SLEEP}	nSLEEP = 0		45	60	µA
Control Logic						
Input logic low threshold	V_{IN_LOW}				0.4	V
Input logic high threshold	V_{IN_HIGH}		1.5			V
Logic input current	I_{IN_HIGH}	V = 3.3V	-20		+20	µA
	I_{IN_LOW}	V = 0V	-20		+20	µA
Start-up delay	t_{DELAY_SU}	V_{IN} is rising or V_{nSLEEP} is rising		1.5		ms
Internal pull-down resistance	R_{PD}	All logic inputs		500		kΩ
nFAULT pull-down resistance	$R_{DS(ON)_nFAULT}$			15		Ω
V3P3 Regulator						
LDO output		I_{OUT} = 0mA to 80mA	3.2	3.32	3.45	V
Protection Circuits						
Under-voltage lockout (UVLO) threshold	V_{UVLO}	V_{IN} rising	2.5	2.7	2.9	V
UVLO hysteresis	ΔV_{UVLO}			150		mV
Over-current protection (OCP) threshold	I_{OCP}	ROCP = 0	4	5	6.5	A
		ROCP is floating	4.8	7	8.8	A
OCP deglitch time	t_{OCP}			1		µs
Thermal shutdown (6)	T_{TSD}	T_J rising		160		°C
Thermal shutdown hysteresis (6)	ΔT_{TSD}			25		°C
Current Sense (CS)						
CS ratio			1/3600	1/4000	1/4400	A/A
CS output current		I_{LS-FET} = 1A	225	250	275	µA
		I_{LS-FET} = -1A	-275	-250	-225	µA
		I_{LS-FET} = 100mA	22.5	25	27.5	µA
		I_{LS-FET} = -100mA	-27.5	-25	-22.5	µA
Positive-to-negative ratio (positive to negative matching)		I_{LS-FET} = ±1A, ±100mA	95%	1	105%	
Phase-to-phase ratio (phase matching)		I_{LS-FET} = ±1A, ±100mA	95%	1	105%	
CS output voltage swing		I_{LS-FET} = ±0.25A	0		3.6	V
Output						
HS-FET on resistance	$R_{DS(ON)_HS}$	I_{OUT} = 1A	90	115	135	mΩ
LS-FET on resistance	$R_{DS(ON)_LS}$	I_{OUT} = 1A	85	110	125	
Output rise time (6)		R_{LOAD} = 50Ω		25		ns
Output fall time (6)		R_{LOAD} = 50Ω		25		ns
Dead time (6)		R_{LOAD} = 50Ω		40		ns

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 18V, T_A = 25°C, LSSA = LSSB = LSSC = GND = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWMx to Sx delay time rising (6)				70		ns
PWMx to Sx delay time falling (6)				70		ns
Charge Pump						
Charge pump voltage	V_{CP}			V_{IN} + 3.3		V

Note:

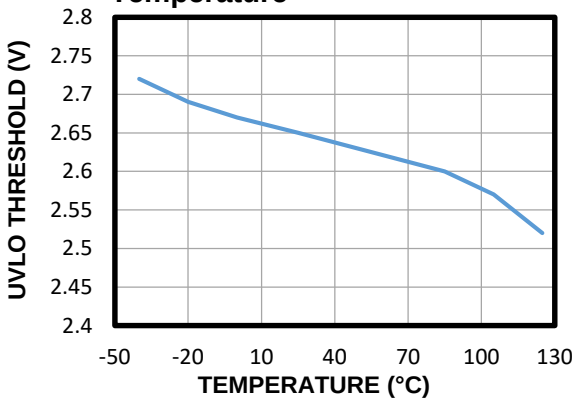
6) Not tested in production.

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TYPICAL CHARACTERISTICS

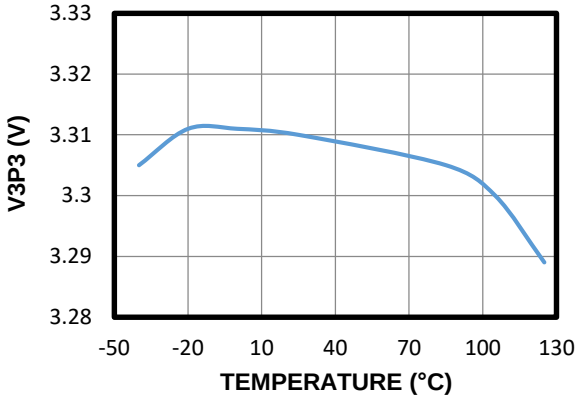
V_{IN} = 18V, unless otherwise noted.

UVLO Threshold vs. Temperature



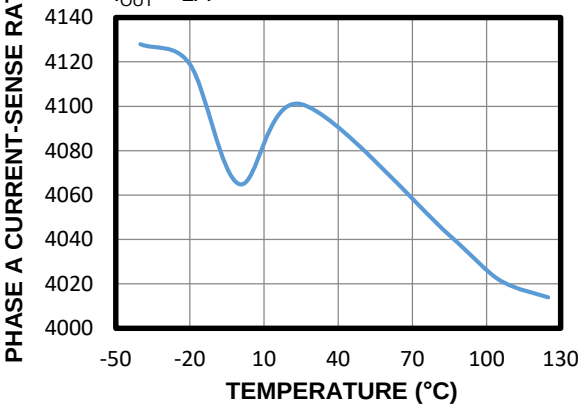
V3P3 vs. Temperature

LDO_LOAD = 100mA



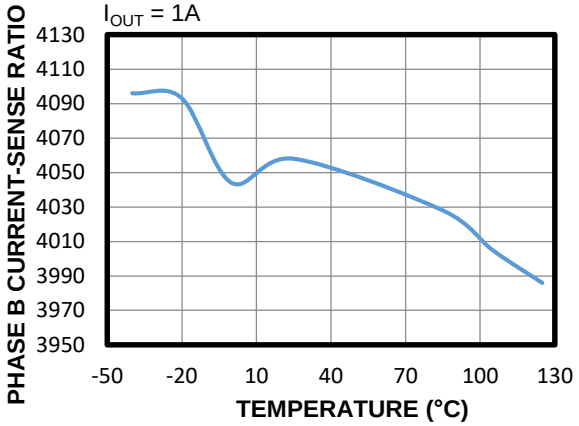
Phase A Current-Sense Ratio vs. Temperature

I_{OUT} = 1A



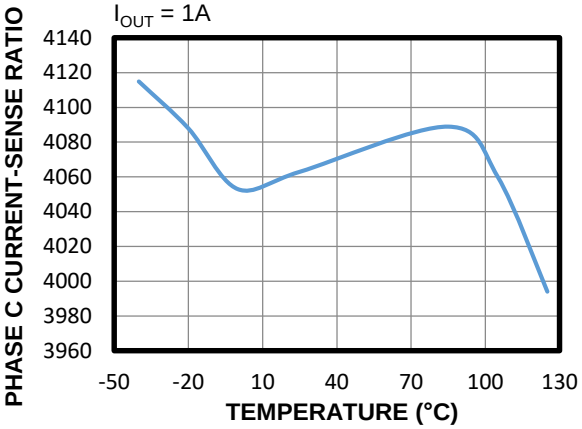
Phase B Current-Sense Ratio vs. Temperature

I_{OUT} = 1A



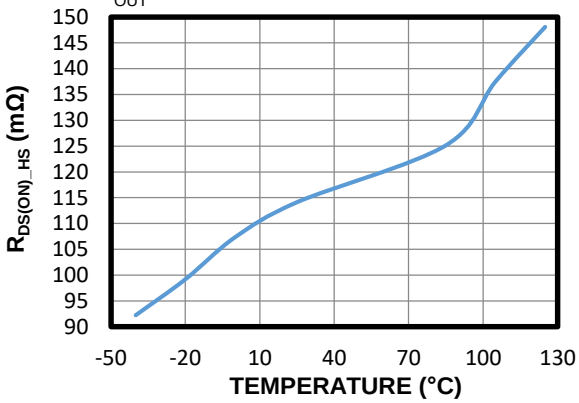
Phase C Current-Sense Ratio vs. Temperature

I_{OUT} = 1A



HS-FET On Resistance vs. Temperature

I_{OUT} = 1A



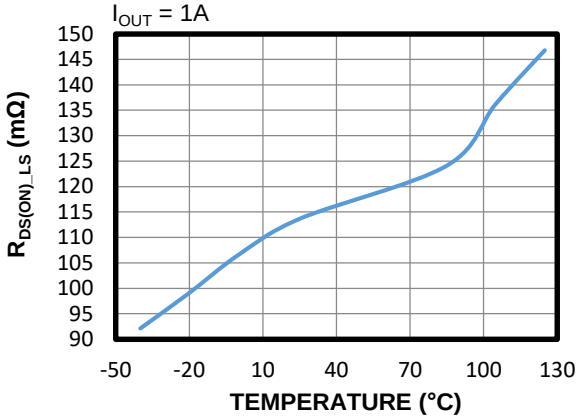
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TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 18V, unless otherwise noted.

LS-FET On Resistance vs. Temperature

I_{OUT} = 1A

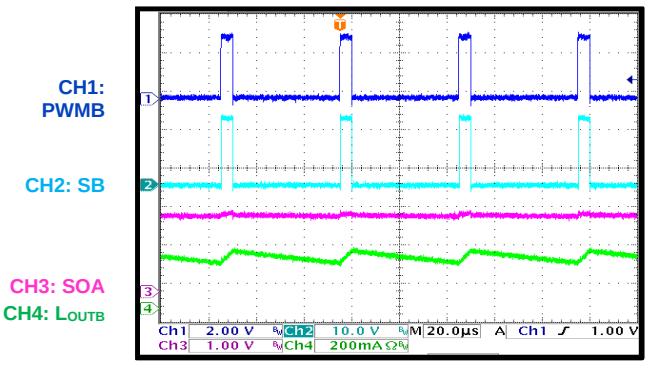


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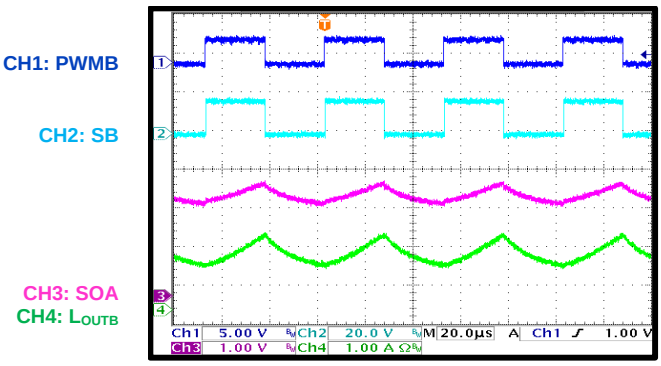
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{IN_LDO} = 18V, LSSA = LSSB = LSSC = GND, phase B f_{SW} = 20kHz, phase C is disabled, phase A LS-FET is turned on, V_{REF} = 3.3V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load = 5Ω + 1mH, unless otherwise noted.

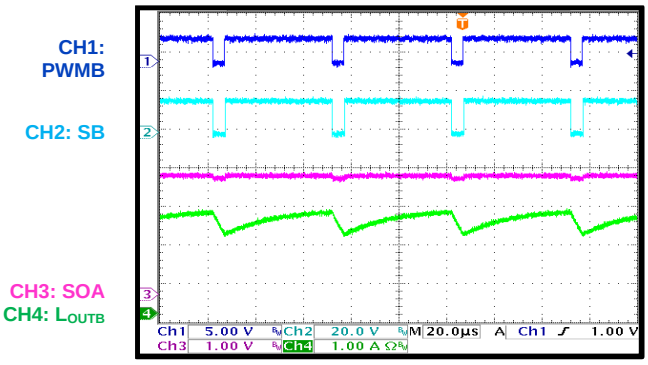
Steady State
Duty = 10%



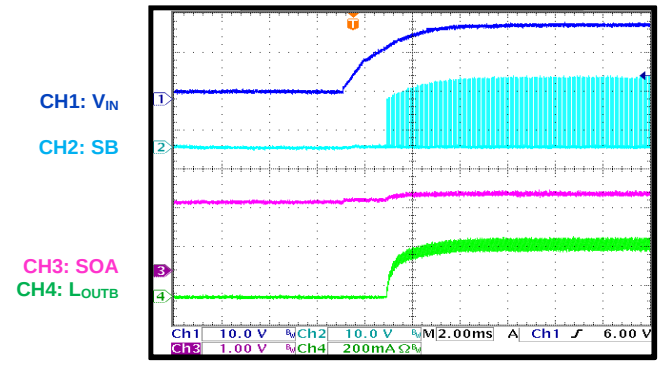
Steady State
Duty = 50%



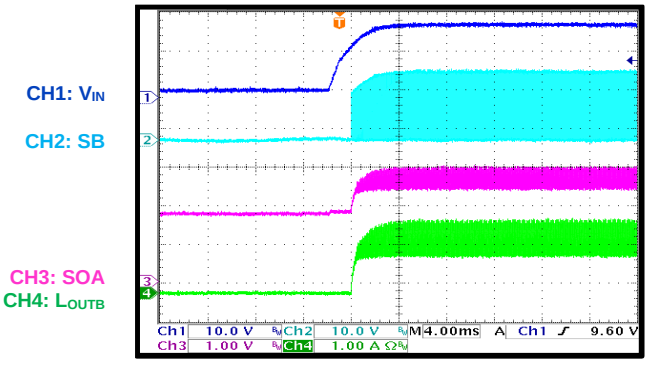
Steady State
Duty = 90%



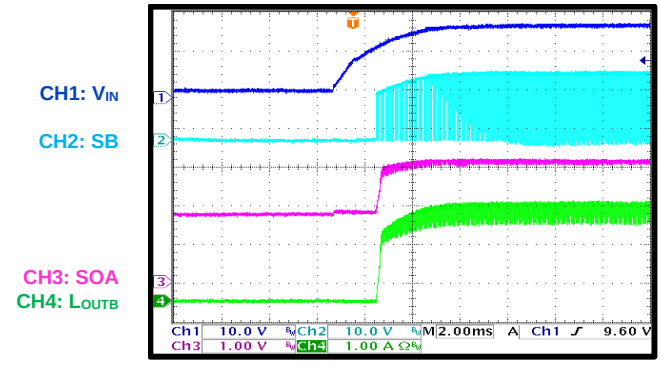
Power Ramping Up
Duty = 10%



Power Ramping Up
Duty = 50%



Power Ramping Up
Duty = 90%

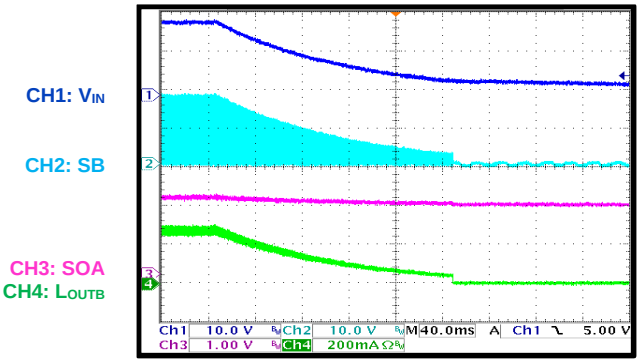


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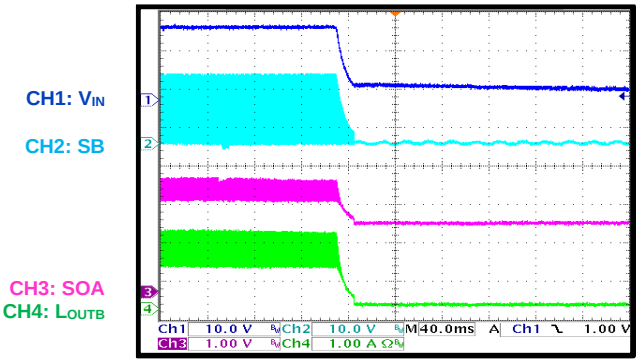
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = V_{IN_LDO} = 18V, LSSA = LSSB = LSSC = GND, phase B f_{SW} = 20kHz, phase C is disabled, phase A LS-FET is turned on, V_{REF} = 3.3V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load = 5Ω + 1mH, unless otherwise noted.

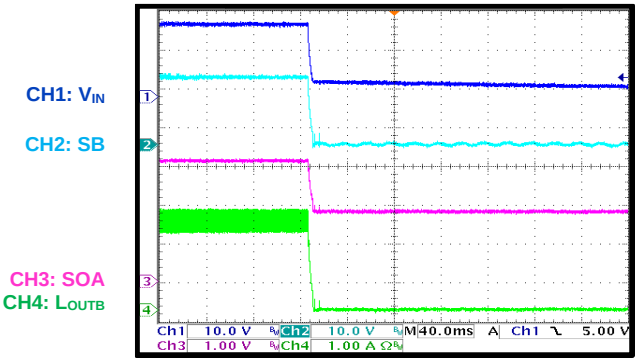
Power Ramping Down
Duty = 10%



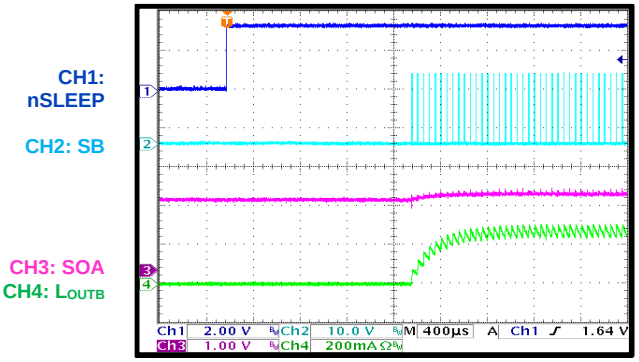
Power Ramping Down
Duty = 50%



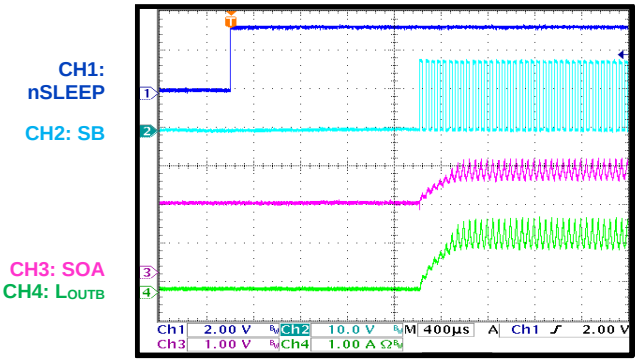
Power Ramping Down
Duty = 90%



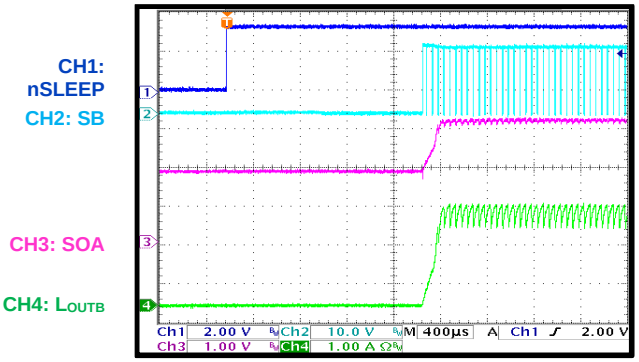
Sleep Mode Recovery
Duty = 10%



Sleep Mode Recovery
Duty = 50%



Sleep Mode Recovery
Duty = 90%



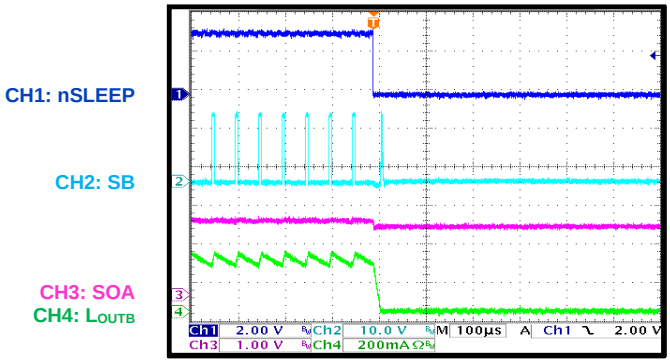
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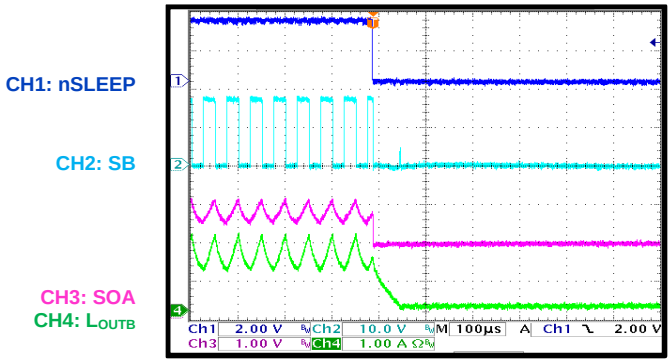
Sleep Mode Entry

Duty = 10%



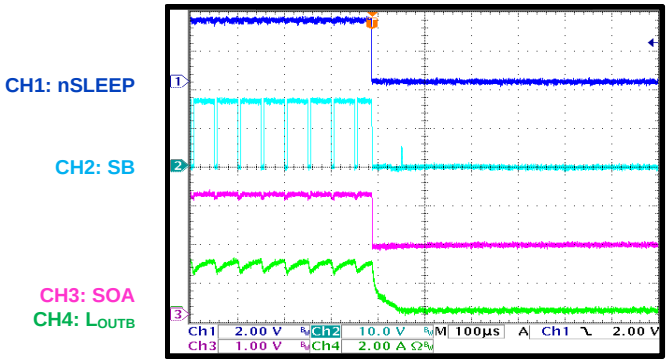
Sleep Mode Entry

Duty = 50%



Sleep Mode Entry

Duty = 90%



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FUNCTIONAL BLOCK DIAGRAM

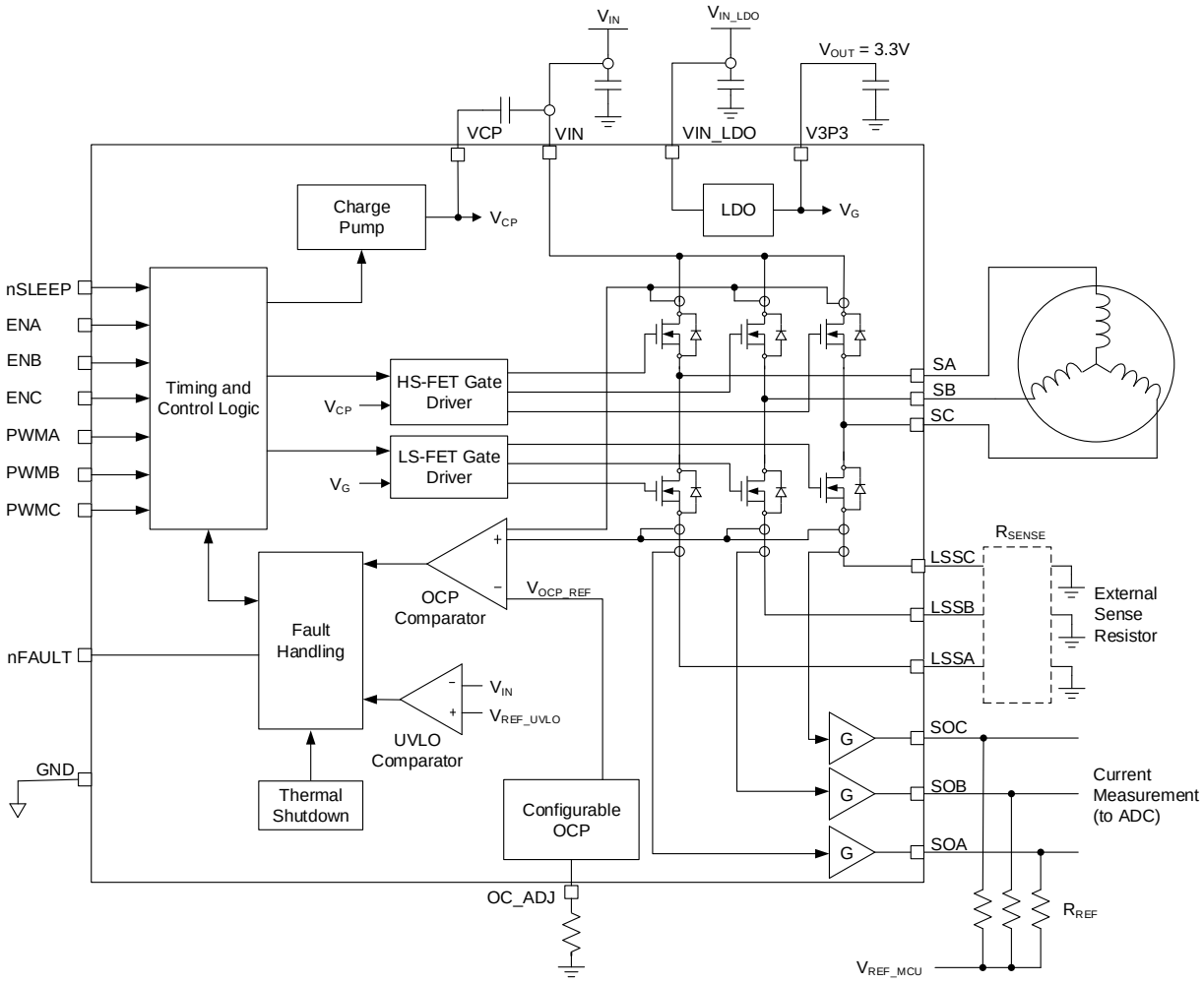


Figure 1: Functional Block Diagram

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OPERATION

The MP6543C is a three-phase half-bridge driver designed to drive brushless DC (BLDC) motor drivers.

Input Logic

The ENx input pins (ENA, ENB, and ENC) control the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) driver outputs of each phase. If ENx is low, then the corresponding driver outputs are disabled and the phase's PWMx input is ignored. If ENx is high, the driver outputs are enabled and the PWMx input is recognized (see Table 1).

Table 1: Input Logic Truth Table

ENx (7)	PWMx	Sx
High	High	V_{IN}
High	Low	GND
Low	x	Hi-Z

Note:

7) The ENx pins have internal weak pull-down resistors.

Sleep Mode

Pulling the nSLEEP pin low makes the device enter low-power sleep mode. In sleep mode, all internal circuits are disabled and all inputs are ignored. Pull nSLEEP high to force the device to exit sleep mode. While exiting sleep mode, the MP6543C takes about 1ms before responding to the inputs. nSLEEP has a weak pull-down resistor.

Current-Sense Amplifiers

The current flowing through each of the three Sx outputs (SA, SB, and SC) is sensed by an internal current-sensing circuit. The SOx pin (SOA, SOB, and SOC) sources or sinks a current proportional to the phase's current. Note that only the current flowing through the LS-FET is sensed, and that it is sensed in both the forward and reverse directions.

To convert this current into a voltage (e.g. to input to an analog-to-digital converter [ADC]), a termination resistor (R_{REF}) generates the reference voltage (V_{REF}). If no current is flowing, the voltage should equal V_{REF}. If current is flowing, the voltage should be above or below V_{REF}.

The voltage (V_{SOX}) can be calculated with Equation (1):

$$V_{SOx} = V_{REF} + (R_{REF} \times I_{LOAD}) / 4000 \quad (1)$$

Where I_{LOAD} is the load current.

To terminate the device's outputs while using an ADC with inputs that are ratiometric to its supply voltage, connect two equal-value resistors between the ADC supply and ground. The resulting ADC code should be half-scale at 0A of current. Figure 2 shows a simplified current measurement circuit.

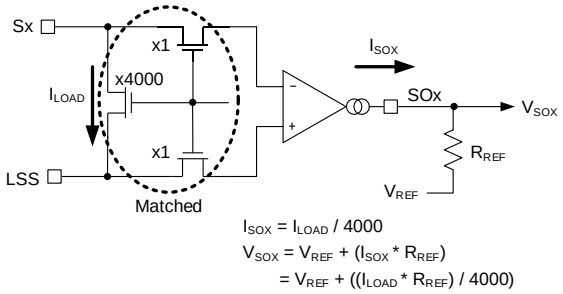


Figure 2: Simplified Measurement Current

Automatic Synchronous Rectification (SR)

The MP6543C employs automatic synchronous rectification (SR) to prevent excess power dissipation in the body diodes while driving a current through an inductive load with all of the MOSFET outputs turned off. In this scenario, a recirculation current must continue to flow through the MOSFET body diodes.

If both the HS-FET and LS-FET are turned off and the Sx voltage (V_{Sx}) is pulled to ground, then the LS-FET turns on until the current flowing through it reaches 0A, or until the HS-FET turns on. If V_{Sx} exceeds V_{IN}, then the HS-FET turns on until the current flowing through it reaches 0A, or until the LS-FET turns on.

Fault Indication

The MP6543C has a fault indication pin (nFAULT) that indicates whether a fault has occurred (e.g. an over-current (OC) or over-temperature (OT) event). nFAULT is an open-drain output. If a fault occurs, nFAULT is pulled low. Once the fault condition is removed, nFAULT is pulled high via an external pull-up resistor.

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Under-Voltage Lockout (UVLO) Protection

If V_{IN} drops below the UVLO threshold (typically 2.7V), UVLO protection is triggered. The device's circuitry is disabled, and the internal logic is reset. Once V_{IN} exceeds 2.7V, the MP6543C starts up again and resumes normal operation.

Over-Current Protection (OCP)

Over-current protection (OCP) limits the current flowing through each MOSFET. If I_{OUT} exceeds the OCP threshold (I_{OCP}) for longer than the OCP deglitch time (t_{OCP}, typically 1µs), then OCP is triggered. All six output MOSFETs enter a high-impedance (Hi-Z) state. The current is recirculated through the body diodes and the outputs are disabled. After about 4ms, the outputs are enabled again.

OC faults (e.g. short to ground, short to supply, and short across the motor) on both HS-FETs and LS-FETs can trigger OCP.

Figure 3 shows a simplified OCP circuit for an output.

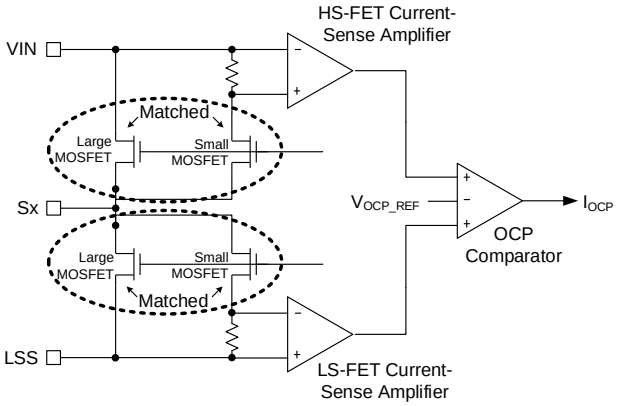


Figure 3: Simplified OCP Circuit

Table 2 shows the OCP threshold for OC_ADJ values outside of the specified range.

Table 2: OCP Threshold for Different OC_ADJ Values

OC_ADJ Resistor Value	Minimum OCP Threshold
0A	4A
Floating	4.8A

Thermal Shutdown

If the die temperature exceeds its safe threshold (160°C), the MP6543C shuts down. Once the die temperature drops below 135°C, the part starts up again and resumes normal operation. There is a hysteresis of 25°C.

3.3V LDO Output

An internal low-dropout (LDO) regulator generates a 3.3V voltage with a 100mA capacity, which is capable of powering a small, low-power microcontroller. The LDO requires a 4.7µF to 10µF bypass capacitor connected between V3P3 and GND.

Charge Pump

A charge pump generates the driver voltage for the HS-FETs. The charge pump requires an external, 10V, 1µF ceramic capacitor connected between the VIN and VCP pins.

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APPLICATION INFORMATION

External Component Selection

Bypass the VIN pin to GND using a 100nF ceramic X7R capacitor located as close to the IC as possible. Place an additional 1µF to 10µF ceramic capacitor nearby the 100nF capacitor. Depending on the supply impedance and distance to other large capacitors, an electrolytic bulk capacitor may also be required to stabilize VIN. The SOA, SOB and SOC pins are current measurement outputs. SOA, SOB and SOC are typically converted to a voltage via a termination resistor (R_{REF}) that creates a reference voltage (V_{REF}). A resistor divider connected between the ADC supply and GND can provide a ratiometric voltage for an AC/DC converter.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place supply bypass capacitors as close as possible to the IC (ideally, place them adjacent to the IC pins on the same PCB layer). Each VIN pin needs to have a bypass capacitor.
2. Supply bypass capacitors can also be placed on the opposite side of the PCB directly under the IC, using vias to make connections.
3. Place as much copper as possible on the power pads.
4. The thermal pad should be soldered directly to copper on the PCB. Thermal vias are often used to transfer heat to other layers of the PCB.

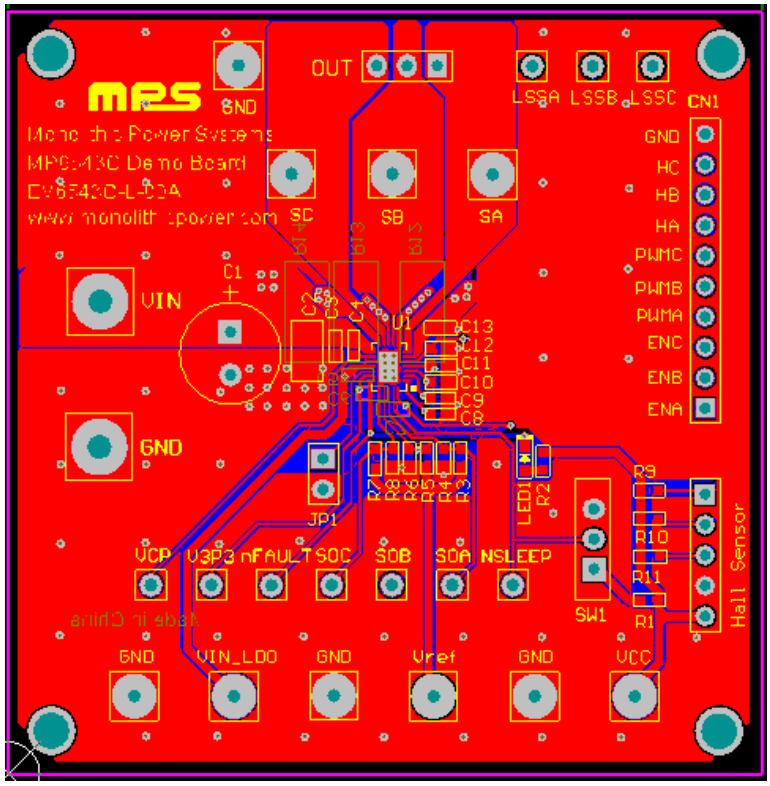


Figure 4: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

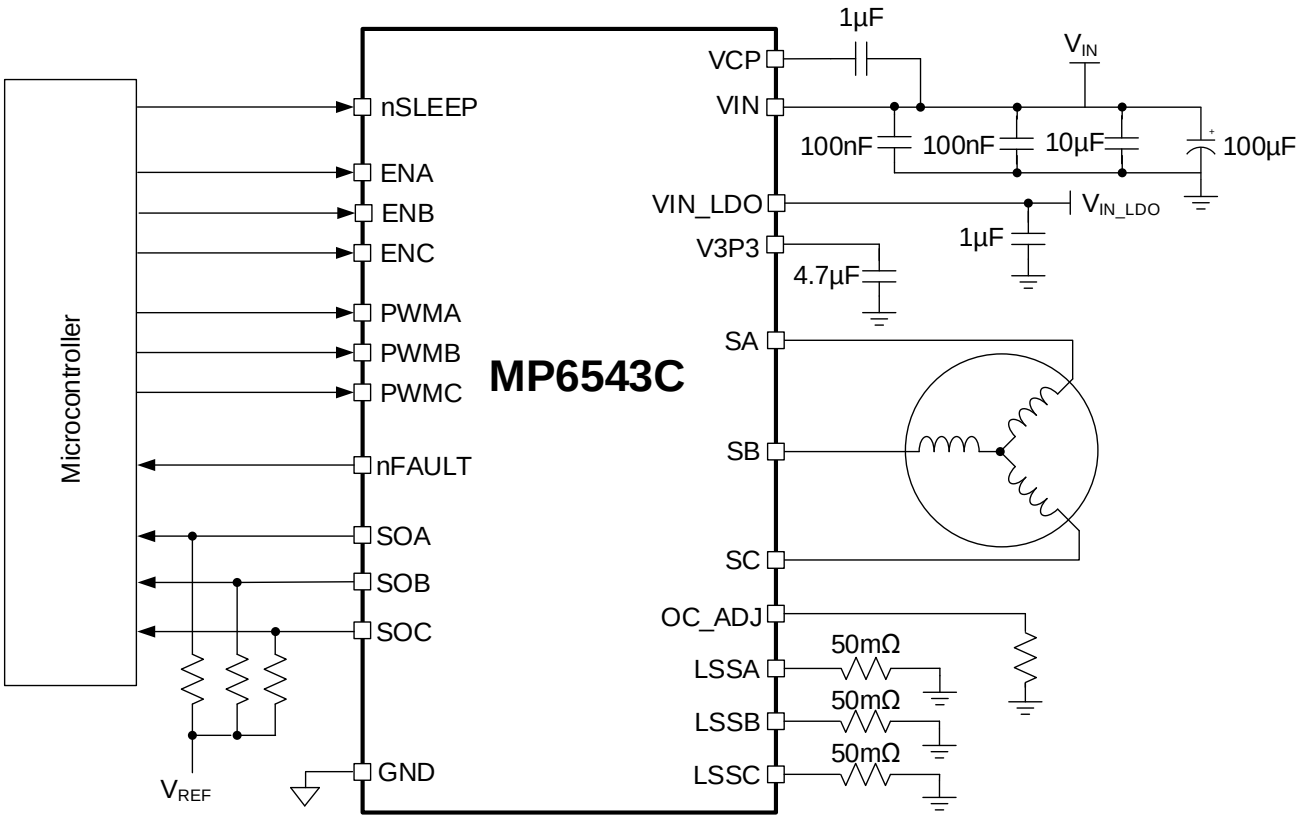
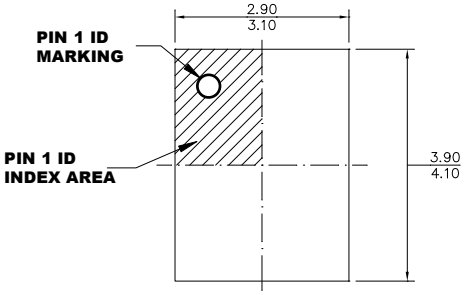


Figure 5: Typical Application Circuit

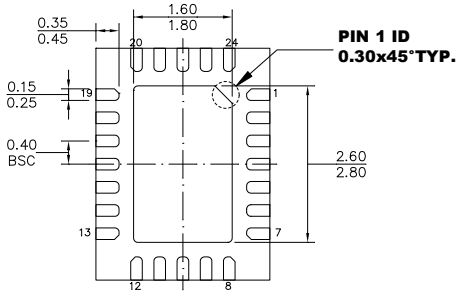
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PACKAGE INFORMATION

QFN-24 (3mmx4mm)



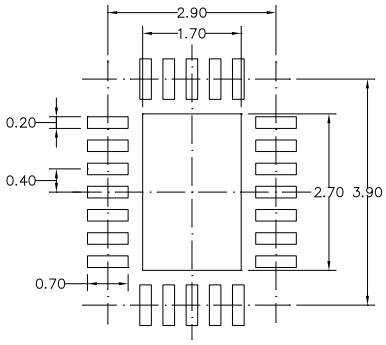
TOP VIEW



BOTTOM VIEW



SIDE VIEW



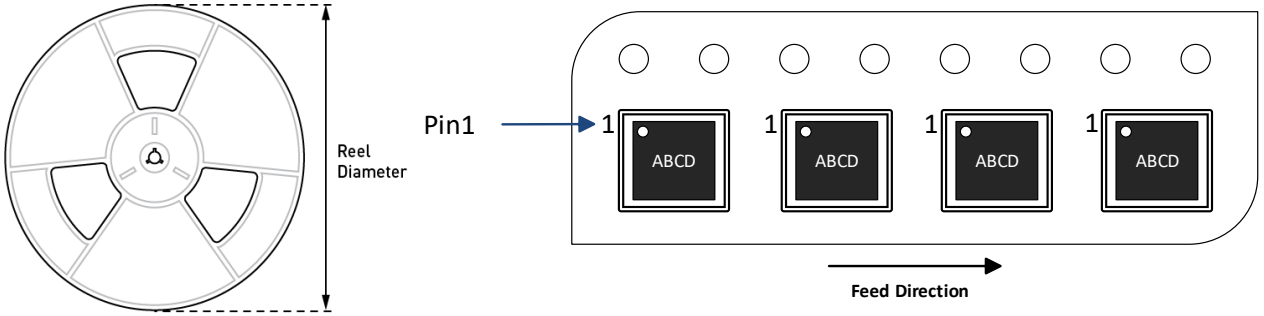
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITIES SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity /Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6543CGL-Z	QFN-24 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	08/18/2021	Initial Release	-

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