EPSON

S1D13705F00A

Embedded Memory LCD Controller

■ DESCRIPTION

The S1D13705 is a color / monochrome LCD graphics controller with an embedded 80K byte SRAM display buffer. The high integration of the S1D13705 provides a low cost, low power, single chip solution to meet the requirements of embedded markets such as Office Automation equipment, Mobile Communications devices, and Hand-Held PCs where board size and battery life are major concerns.

Products requiring a “Portrait” display can take advantage of the Hardware Portrait Mode feature of the S1D13705. Virtual and Split Screen are just some of the display modes supported. The above features, combined with the Operating System independence of the S1D13705, make it the ideal solution for a wide variety of applications.

■ FEATURES

◆ Integrated Frame Buffer

- Embedded 80K byte SRAM display buffer.

◆ CPU Interface

- Direct support of the following interfaces:
  Hitachi SH-3.
  Hitachi SH-4.
  Motorola M68K.
  MPU bus interface using WAIT# signal.
- Direct memory mapping of internal registers.
- Single level CPU write buffer.
- Registers are mapped into upper 32 bytes of 128K byte address space.
- The complete 80K byte display buffer is directly and contiguously available through the 17-bit address bus.

◆ Display Support

- 4/8-bit monochrome LCD interface.
- 4/8-bit color LCD interface.
- Single-panel, single-drive passive displays.
- Dual-panel, dual-drive passive displays.
- Active Matrix TFT / D-TFD interface
- Register level support for EL panels.
- Example resolutions:
  640x480 at a color depth of 2 bpp
  640x240 at a color depth of 4 bpp
  320x240 at a color depth of 8 bpp

◆ Display Modes

- SwivelView™: direct 90° hardware rotation of display image for portrait mode display
- 1/2/4 bit-per-pixel (bpp), 2/4/16-level grayscale display.
- 1/2/4/8 bit-per-pixel, 2/4/16/256-level color display.
- Up to 16 shades of gray by FRM on monochrome passive LCD panels; a 256x4 Look-Up Table is used to map 1/2/4 bpp modes into these shades.
- 256 simultaneous of 4096 colors on color passive and active matrix LCD panels; three 256x4 Look-Up Tables are used to map 1/2/4/8 bpp modes into these colors.
- Split screen display for all landscape panel modes allows two different images to be simultaneously displayed.
- Virtual display support (displays images larger than the panel size through the use of panning).

◆ Clock Source

- Maximum operating clock (CLK) frequency of 25MHz.
- Operating clock (CLK) is derived from CLKI input.
  CLK = CLKI
  or
  CLK = CLKI/2
- Pixel Clock (PCLK) and Memory Clock (MCLK) are derived from CLK.

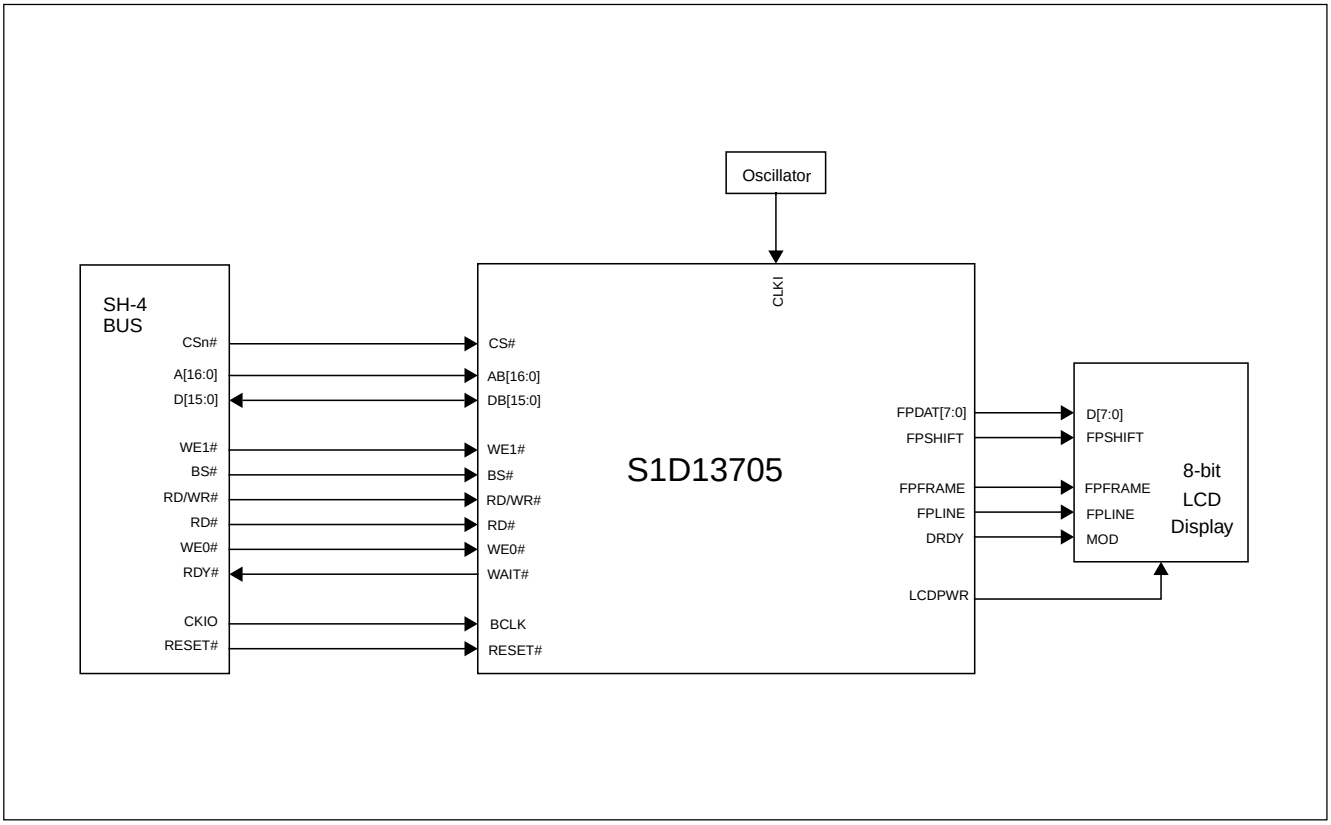
◆ Miscellaneous

- Hardware/Software Video Invert.
- Software Power Save mode.
- Hardware Power Save mode.
- LCD power-down sequencing.
- 5 General Purpose Input/Output pins are available.
  - GPIO0 is available if Hardware Power Save is not required.
  - GPIO[4:1] are available if upper LCD data pins (FPDAT[11:8]) are not required for TFT/D-TFD support or hardware inverse video.
- Core operates from 2.7 volts to 3.6 volts.
- IO Operates from the core voltage up to 5.5 volts.

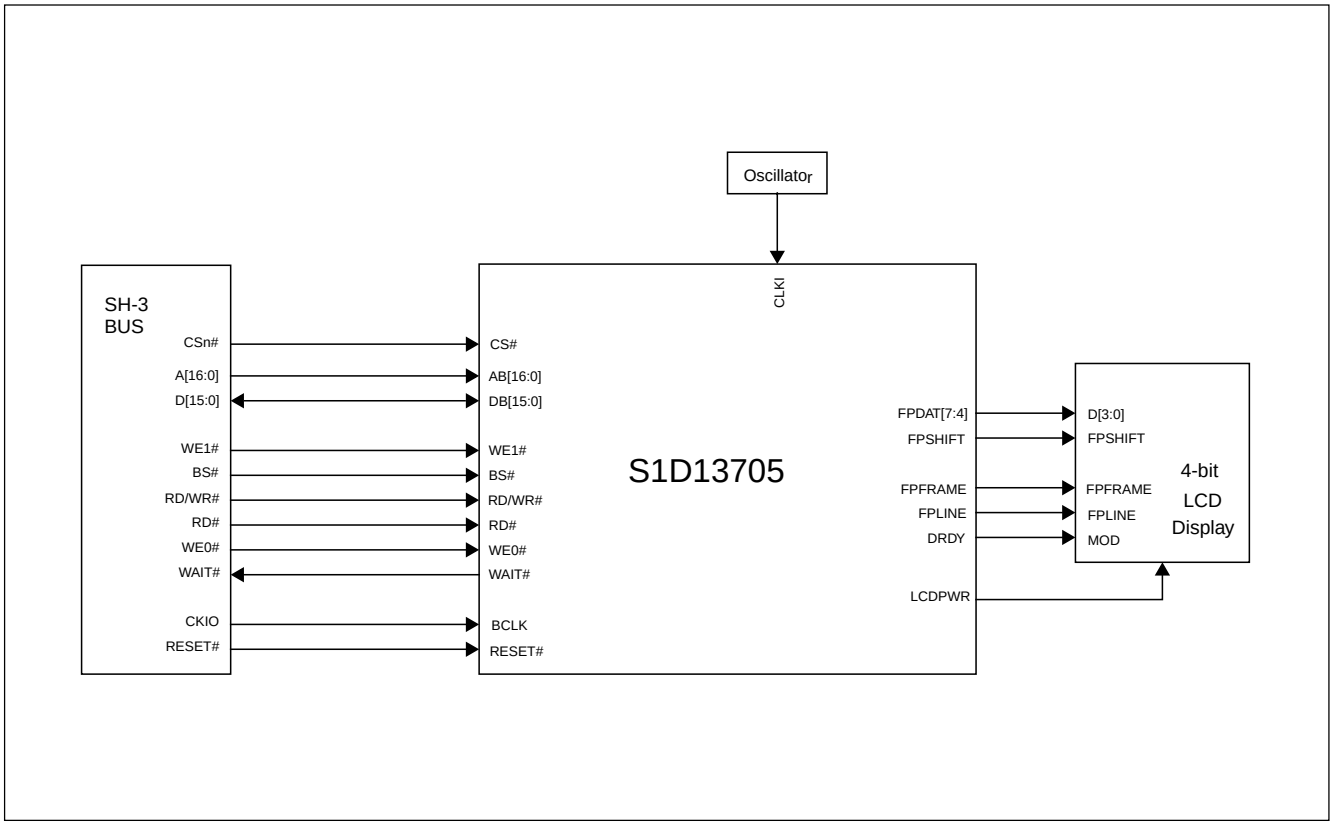
◆ Package

- 80 pin QFP14 package.

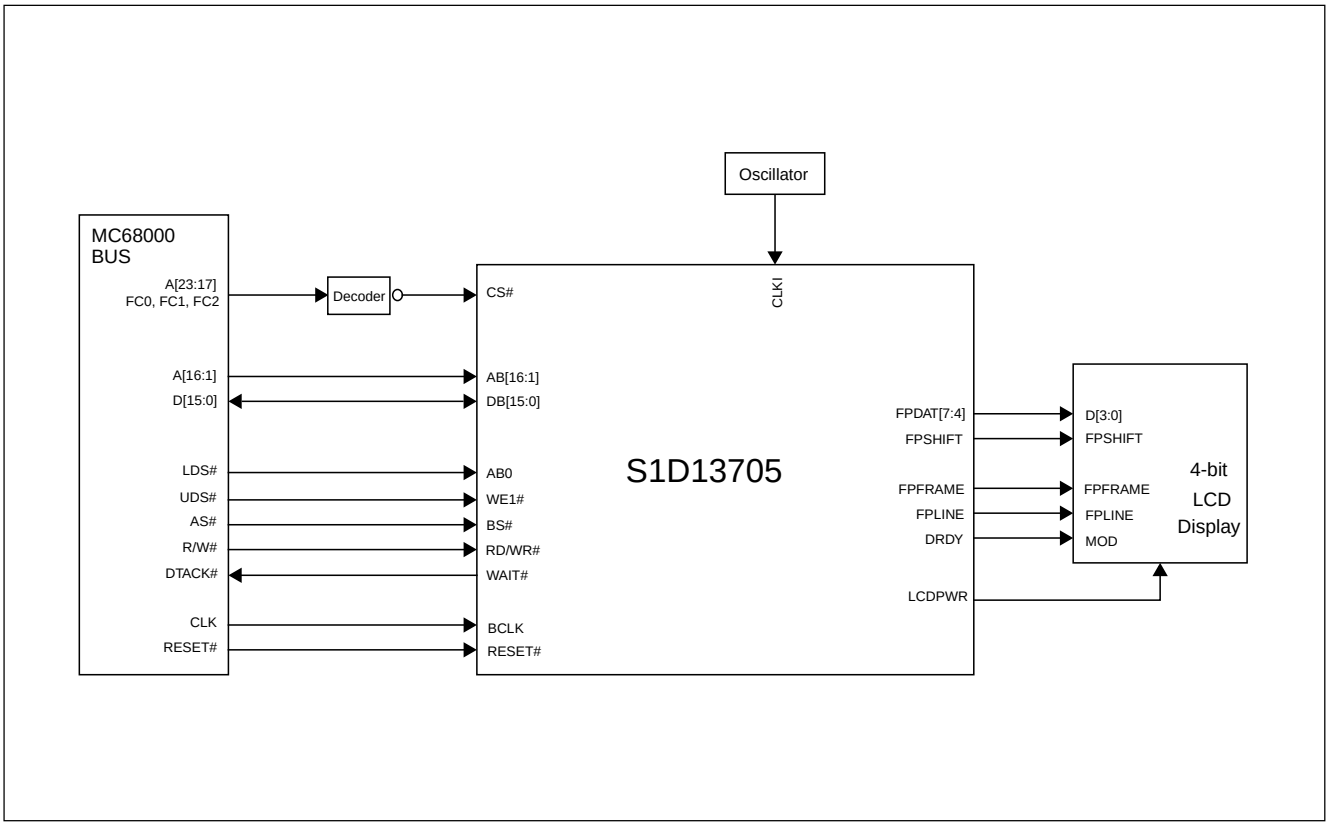
■ TYPICAL SYSTEM IMPLEMENTATION DIAGRAMS



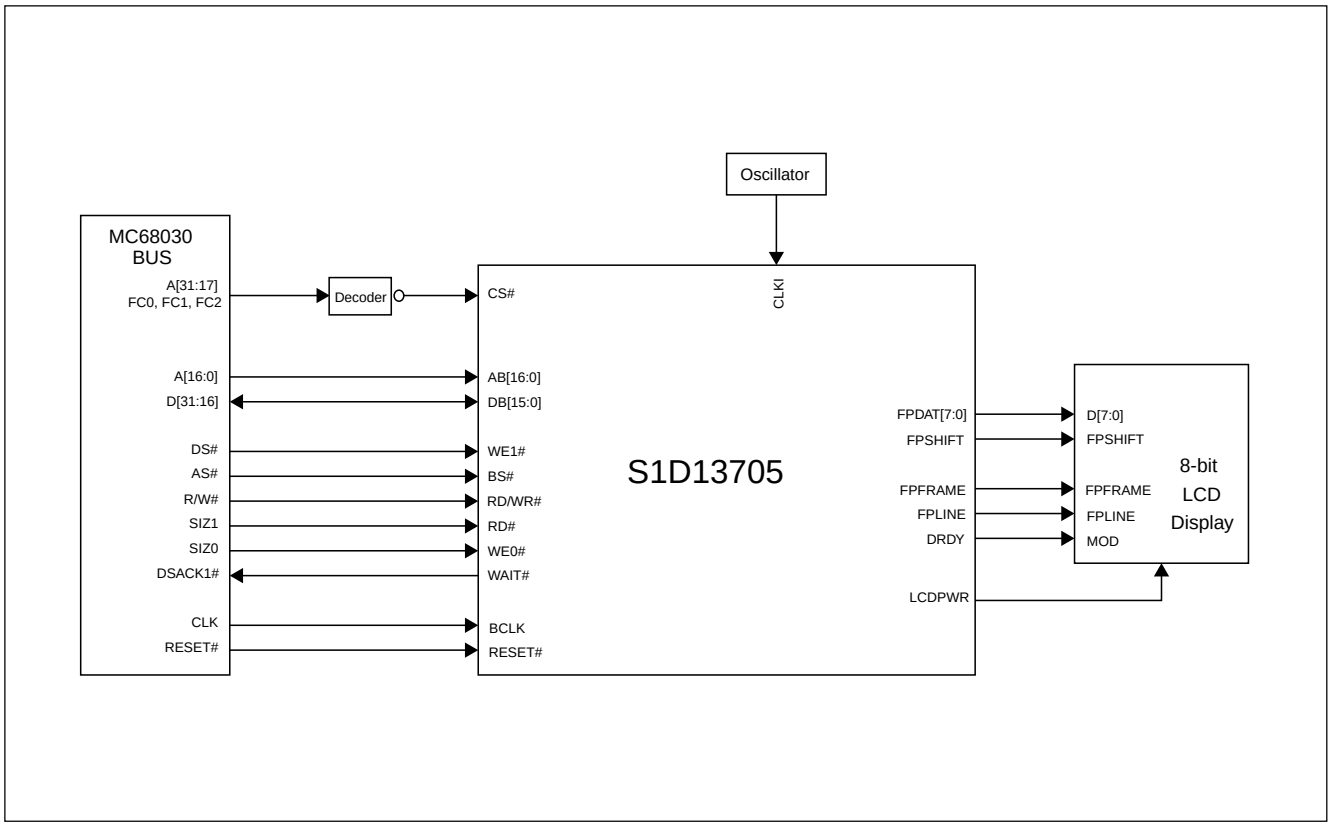
Typical System Diagram (SH-4 Bus)



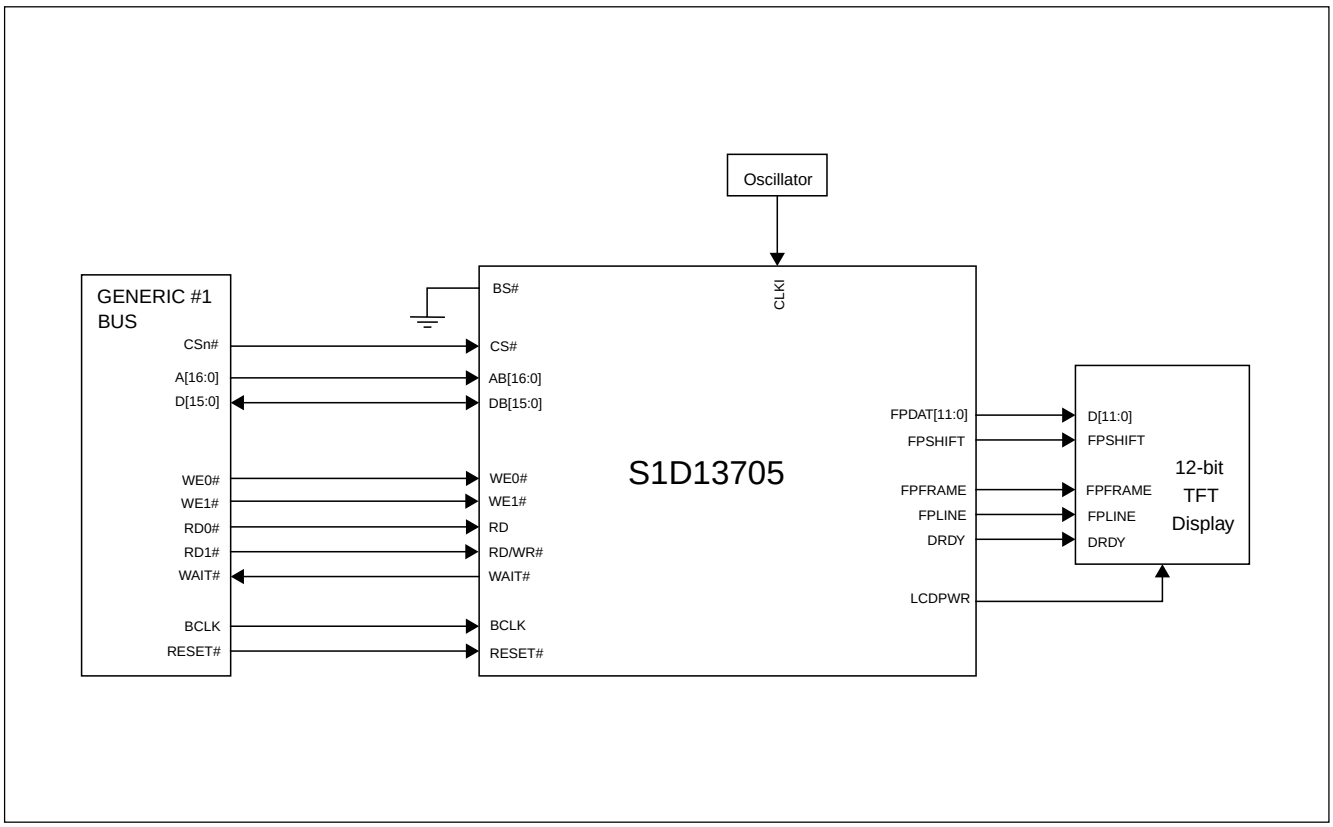
Typical System Diagram (SH-3 Bus)



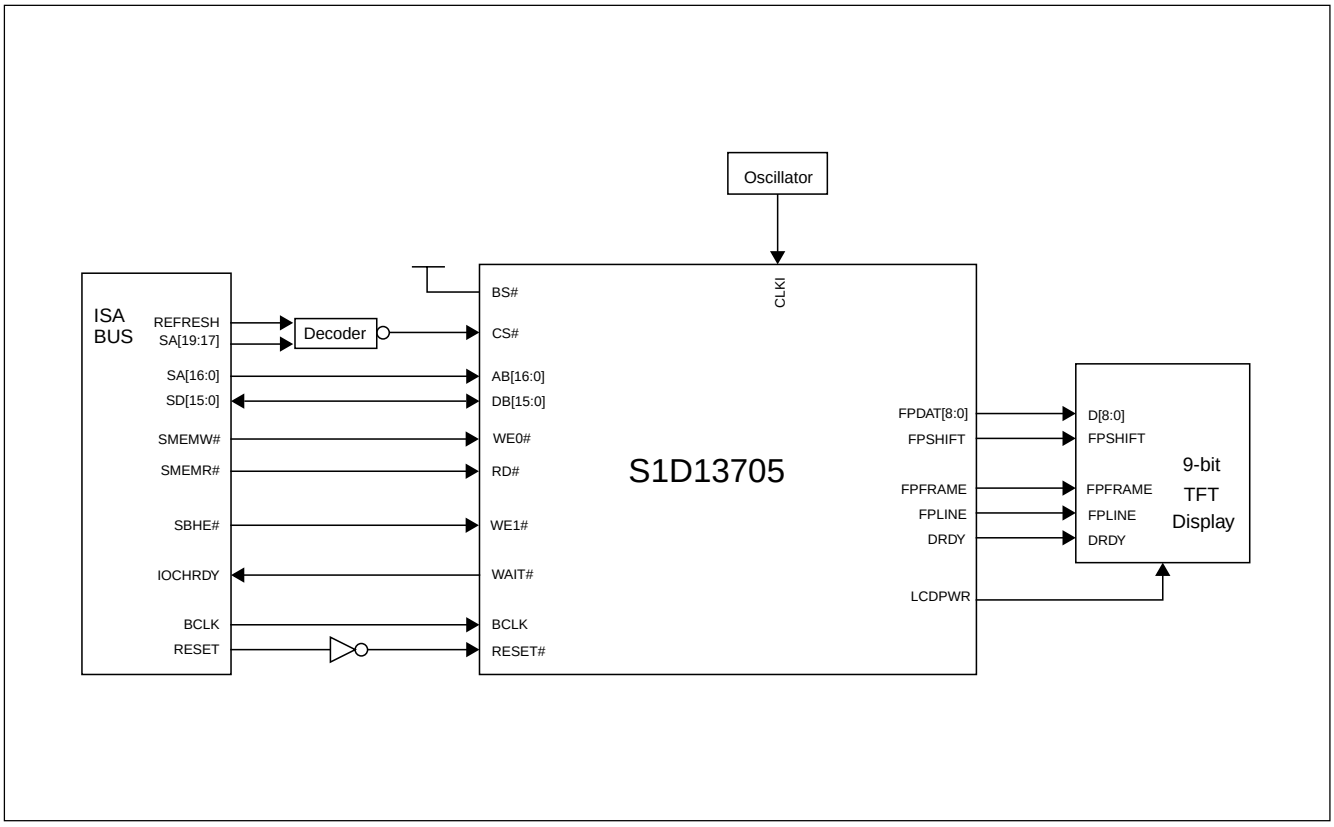
Typical System Diagram (M68K #1 Bus)



Typical System Diagram (M68K #2 Bus)

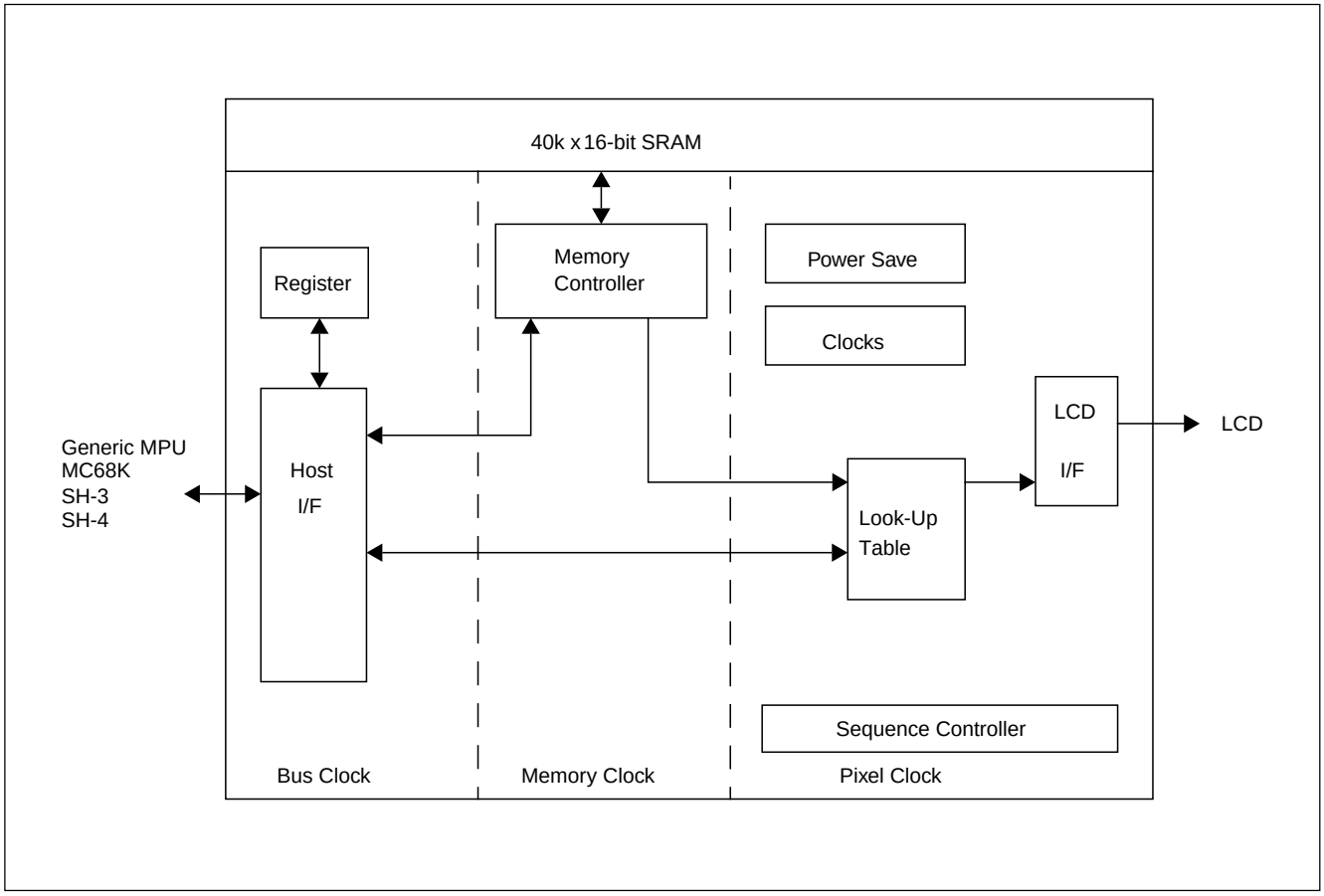


Typical System Diagram (Generic #1 Bus)



Typical System Diagram (Generic #2 Bus - e.g. ISA Bus)

■ FUNCTIONAL BLOCK DIAGRAM



System Block Diagram Showing Datapaths

◆ Functional Block Descriptions

Host Interface

The Host Interface provides the means for the CPU/MPU to communicate with the display buffer and internal registers.

Memory Controller

The Memory Controller arbitrates between CPU accesses and display refresh accesses. It also generates the necessary signals to control the SRAM frame buffer.

Sequence Controller

The Sequence Controller controls data flow from the Memory Controller through the Look-Up Table and to the LCD Interface. It also generates memory addresses for display refresh accesses.

Look-Up Table

The Look-Up Table contains three 256x4 Look-Up Tables or palettes, one for each primary color. In monochrome mode only the green Look-Up Table is used.

LCD Interface

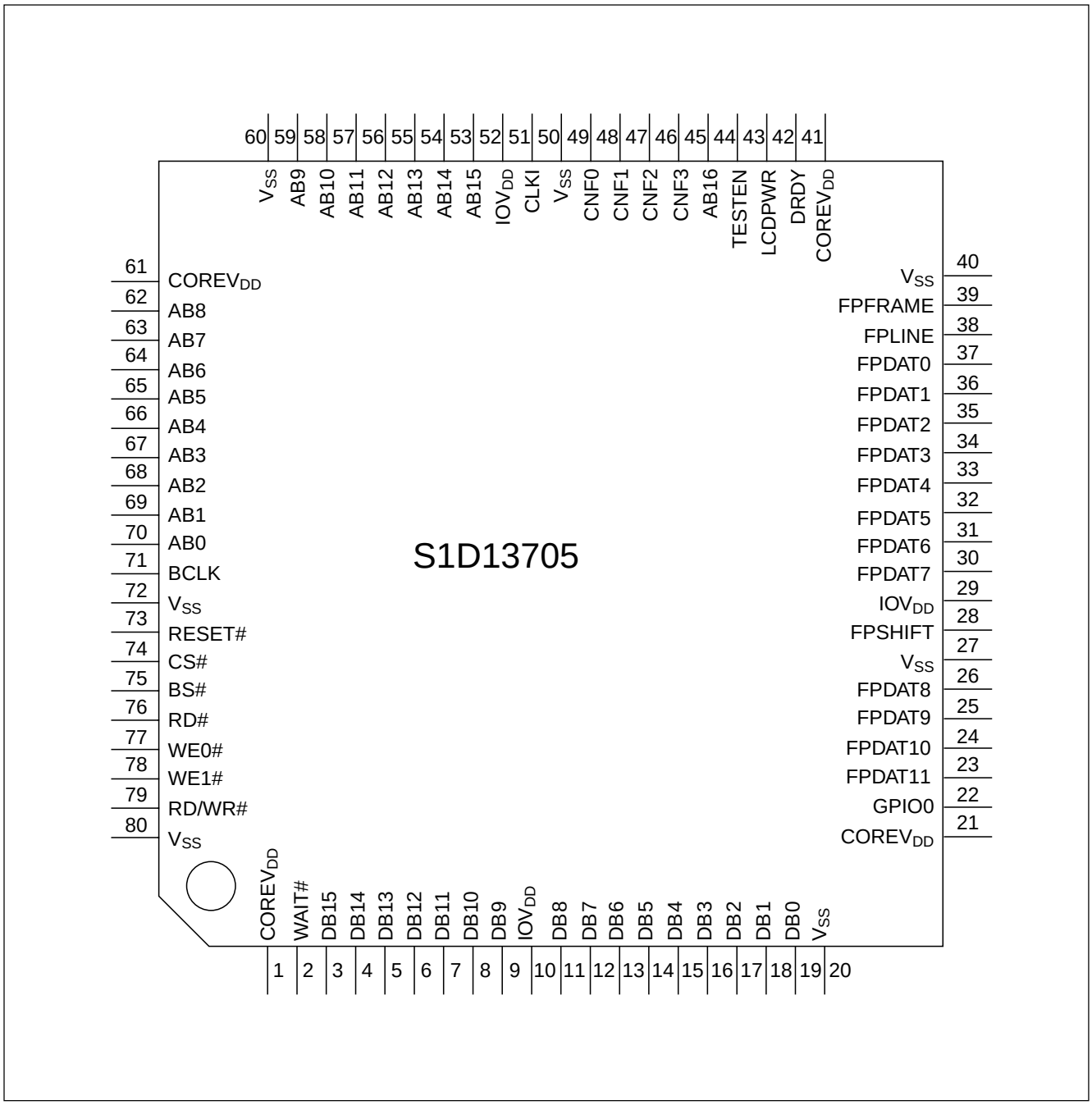
The LCD Interface performs frame rate modulation for passive LCD panels. It also generates the correct data format and timing control signals for various LCD and TFT/D-TFD panels.

Power Save

Power Save contains the power save mode circuitry.

■ PINS

◆ Pinout Diagram



Pinout Diagram

Note: Package type: 80 pin surface mount QFP14

◆ Pin Description

Key:

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
C	=	CMOS level input
CS	=	CMOS level Schmitt input
COx	=	CMOS output driver, x denotes driver type (see I_{OL}/I_{OH} in Table “Output Specifications”)
TSx	=	Tri-state CMOS output driver, x denotes driver type (see I_{OL}/I_{OH} in Table “Output Specifications”)
CNx	=	CMOS low-noise output driver, x denotes driver type (see I_{OL}/I_{OH} in Table “Output Specifications”)
TEST	=	CMOS level test input with pull down resistor

Host Interface

Host Interface Pin Descriptions

Pin Names	Type	Pin #	Cell	RESET# State	Description
AB0	I	70	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs system address bit 0 (A0). • For MC68K #1, this pin inputs the lower data strobe (LDS#). • For MC68K #2, this pin inputs system address bit 0 (A0). • For Generic #1, this pin inputs system address bit 0 (A0). • For Generic #2, this pin inputs system address bit 0 (A0). See Table “Host Bus Interface Pin Mapping” for summary.
AB[16:1]	I	45, 53, 54, 55, 56, 57, 58, 59, 62, 63, 64, 65, 66, 67, 68, 69	C	Input	These pins input the system address bits 16 through 1 (A[16:1]).
DB[15:0]	IO	3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 18, 19	C/TS2	Hi-Z	These pins have multiple functions. • For SH-3/SH-4 mode, these pins are connected to [D15:0]. • For MC68K #1, these pins are connected to D[15:0]. • For MC68K #2, these pins are connected to D[31:16] for a 32-bit device (e.g. MC68030) or D[15:0] for a 16-bit device (e.g.MC68340). • For Generic #1, these pins are connected to D[15:0]. • For Generic #2, these pins are connected to D[15:0]. See Table “Host Bus Interface Pin Mapping” for summary.
WE0#	I	77	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the write enable signal for the lower data byte (WE0#). • For MC68K #1, this pin must be tied to IOV_{DD} • For MC68K #2, this pin inputs the bus size bit 0 (SIZ0). • For Generic #1, this pin inputs the write enable signal for the lower data byte (WE0#). • For Generic #2, this pin inputs the write enable signal (WE#) See Table “Host Bus Interface Pin Mapping” for summary.

Host Interface Pin Descriptions(cont.)

Pin Names	Type	Pin #	Cell	RESET# State	Description
WE1#	I	78	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the write enable signal for the upper data byte (WE1#). • For MC68K #1, this pin inputs the upper data strobe (UDS#). • For MC68K #2, this pin inputs the data strobe (DS#). • For Generic #1, this pin inputs the write enable signal for the upper data byte (WE1#). • For Generic #2, this pin inputs the byte enable signal for the high data byte (BHE#). See Table “Host Bus Interface Pin Mapping” for summary.
CS#	I	74	C	Input	This pin inputs the chip select signal.
BCLK	I	71	C	Input	This pin inputs the system bus clock.
BS#	I	75	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the bus start signal (BS#). • For MC68K #1, this pin inputs the address strobe (AS#). • For MC68K #2, this pin inputs the address strobe (AS#). • For Generic #1, this pin must be tied to V_{SS}. • For Generic #2, this pin must be tied to IOV_{DD}. See Table “Host Bus Interface Pin Mapping” for summary.
RD/WR#	I	79	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the RD/WR# signal. The S1D13705 needs this signal for early decode of the bus cycle. • For MC68K #1, this pin inputs the R/W# signal. • For MC68K #2, this pin inputs the R/W# signal. • For Generic #1, this pin inputs the read command for the upper data byte (RD1#). • For Generic #2, this pin must be tied to IOV_{DD}. See Table “Host Bus Interface Pin Mapping” for summary.
RD#	I	76	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the read signal (RD#). • For MC68K #1, this pin must be tied to IOV_{DD}. • For MC68K #2, this pin inputs the bus size bit 1 (SIZ1). • For Generic #1, this pin inputs the read command for the lower data byte (RD0#). • For Generic #2, this pin inputs the read command (RD#). See Table “Host Bus Interface Pin Mapping” for summary.
WAIT#	O	2	TS2	Hi-Z	This pin has multiple functions. • For SH-3 mode, this pin outputs the wait request signal (WAIT#). • For SH-4 mode, this pin outputs the device ready signal (RDY#). • For MC68K #1, this pin outputs the data transfer acknowledge signal (DTACK#). • For MC68K #2, this pin outputs the data transfer and size acknowledge bit 1 (DSACK1#). • For Generic #1, this pin outputs the wait signal (WAIT#). • For Generic #2, this pin outputs the wait signal (WAIT#). See Table “Host Bus Interface Pin Mapping” for summary.
RESET#	I	73	CS	0	Active low input to set all internal registers to the default state and to force all signals to their inactive states.

LCD Interface

LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
FPDAT[7:0]	O	30, 31, 32, 33, 34, 35, 36, 37	CN3	0	Panel Data
FPDAT[10:8]	O, IO	24, 25, 26	CN3	Input	These pins have multiple functions. • Panel Data bits [10:8] for TFT/D-TFD panels. • General Purpose Input/Output pins GPIO[3:1]. These pins should be connected to IOV_{DD} when unused. See Table “LCD Interface Pin Mapping” for summary.
FPDAT11	O, IO	23	CN3	Input	This pin has multiple functions. • Panel Data bit 11 for TFT/D-TFD panels. • General Purpose Input/Output pin GPIO4. • Inverse Video select pin. This pin should be connected to IOV_{DD} when unused. See Table “LCD Interface Pin Mapping” for summary.
FPFRAME	O	39	CN3	0	Frame Pulse
FPLINE	O	38	CN3	0	Line Pulse
FPSHIFT	O	28	CN3	0	Shift Clock
LCDPWR	O	43	CO1	0	Active high LCD Power Control
DRDY	O	42	CN3	0	This pin has multiple functions. • TFT/D-TFD Display Enable (DRDY). • LCD Backplane Bias (MOD). • Second Shift Clock (FPSHIFT2). See Table “LCD Interface Pin Mapping” for summary.

Clock Input

Clock Input Pin Description

Pin Name	Type	Pin #	Driver	Description
CLKI	I	51	C	Input Clock

Miscellaneous

Miscellaneous Pin Descriptions

Pin Name	Type	Pin #	Cell	RESET# State	Description
CNF[3:0]	I	46, 47, 48, 49	C	As set by hardware	These inputs are used to configure the S1D13705 - see Table “Summary of Power On/Reset Options.” Must be connected directly to IOV_{DD} or V_{SS}.
GPIO0	IO, I	22	CS/ TS1	Input	This pin has multiple functions - see REG[03h] bit 2. General Purpose Input/Output pin. Hardware Power Save.
TESTEN	I	44	TEST	Pulled low	Test Enable input. This input must be connected to V_{SS}.

Power Supply

Power Supply Pin Descriptions

Pin Name	Type	Pin #	Driver	Description
$COREV_{DD}$	P	1, 21, 41, 61	P	$CoreV_{DD}$
IOV_{DD}	P	10, 29, 52	P	IOV_{DD}
V_{SS}	P	20,27,40, 50,60,72, 80	P	Common V_{SS}

◆ Summary of Configuration Options

Summary of Power On/Reset Options

Configuration Pin	Power On/Reset State				
	1				0
CNF3	Big Endian				Little Endian
CNF[2:0]	Select host bus interface as follows:				
	CNF2	**CNF1**	**CNF0**	**BS#**	**Host Bus**
	0	0	0	X	SH-4 interface
	0	0	1	X	SH-3 interface
	0	1	0	X	reserved
	0	1	1	X	MC68K #1, 16-bit
	1	0	0	X	reserved
	1	0	1	X	MC68K #2, 16-bit
	1	1	0	0	reserved
	1	1	0	1	reserved
	1	1	1	0	Generic #1, 16-bit
	1	1	1	1	Generic #2, 16-bit

◆ Host Bus Interface Pin Mapping

Host Bus Interface Pin Mapping

S1D13705 Pin Names	SH-3	SH-4	MC68K #1	MC68K #2	Generic #1	Generic #2
AB[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]
AB0	A0	A0	LDS#	A0	A0	A0
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[31:16]	D[15:0]	D[15:0]
WE1#	WE1#	WE1#	UDS#	DS#	WE1#	BHE#
CS#	CSn#	CSn#	External Decode	External Decode	External Decode	External Decode
BCLK	CKIO	CKIO	CLK	CLK	BCLK	BCLK
BS#	BS#	BS#	AS#	AS#	connect to V_{SS}	connect to IOV_{DD}
RD/WR#	RD/WR#	RD/WR#	R/W#	R/W#	RD1#	connect to IOV_{DD}
RD#	RD#	RD#	connect to IOV_{DD}	SIZ1	RD0#	RD#
WE0#	WE0#	WE0#	connect to IOV_{DD}	SIZ0	WE0#	WE#
WAIT#	WAIT#	RDY#	DTACK#	DSACK1#	WAIT#	WAIT#
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#

◆ LCD Interface Pin Mapping

LCD Interface Pin Mapping

S1D13705 Pin Name	Monochrome Passive Panel			Color Passive Panel				Color TFT/D-TFD	
	4-bit Single	8-bit Single	8-bit Dual	4-bit Single	8-bit Single Format 1	8-bit Single Format 2	8-bit Dual	9-bit	12-bit
FPFRAME	FPFRAME								
FPLINE	FPLINE								
FPSHIFT	FPSHIFT								
DRDY	MOD	MOD	MOD	MOD	FPSHIFT2	MOD	MOD	DRDY	
FPDAT0	driven0	D0	LD0	driven0	D0	D0	LD0	R2	R3
FPDAT1	driven0	D1	LD1	driven0	D1	D1	LD1	R1	R2
FPDAT2	driven0	D2	LD2	driven0	D2	D2	LD2	R0	R1
FPDAT3	driven0	D3	LD3	driven0	D3	D3	LD3	G2	G3
FPDAT4	D0	D4	UD0	D0	D4	D4	UD0	G1	G2
FPDAT5	D1	D5	UD1	D1	D5	D5	UD1	G0	G1
FPDAT6	D2	D6	UD2	D2	D6	D6	UD2	B2	B3
FPDAT7	D3	D7	UD3	D3	D7	D7	UD3	B1	B2
FPDAT8	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	B0	B1
FPDAT9	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	R0
FPDAT10	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	G0
FPDAT11	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4	B0

Note: 1. Unused GPIO pins must be connected to IOV_{DD}.
2. Hardware Video Invert is enabled on FPDAT11 by REG[02h] bit 1.

■ D.C. CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$CoreV_{DD}$	Supply Voltage	V_{SS} - 0.3 to 4.0	V
IOV_{DD}	Supply Voltage	$CoreV_{DD}$ to 7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to IOV_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to IOV_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. Max. at lead	°C

Recommended Operating Conditions for $CoreV_{DD}$ = 3.3V ± 10%

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$CoreV_{DD}$	Supply Voltage	V_{SS} = 0V	2.7	3.0/3.3	3.6	V
IOV_{DD}	Supply Voltage	V_{SS} = 0V, $IOV_{DD} \geq CoreV_{DD}$	2.7	3.0/3.3/5.0	5.5	V
V_{IN}	Input Voltage		V_{SS}		IOV_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	°C

Input Specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Low Level Input Voltage CMOS inputs	IOV_{DD} = 3.0 3.3 5.0			0.8 0.8 1.0	V V
V_{IH}	High Level Input Voltage CMOS inputs	IOV_{DD} = 3.0 3.3 5.0	1.9 2.0 3.5			V V
V_{T+}	Positive-going Threshold CMOS Schmitt inputs	IOV_{DD} = 3.0 3.3 5.0	1.0 1.1 2.0		2.3 2.4 4.0	V V
V_{T-}	Negative-going Threshold CMOS Schmitt inputs	IOV_{DD} = 3.0 3.3 5.0	0.5 0.6 0.8		1.7 1.8 3.1	V V
I_{IZ}	Input Leakage Current	V_{DD} = Max. V_{IH} = V_{DD} V_{IL} = V_{SS}	-1		1	µA
C_{IN}	Input Pin Capacitance				10	pF

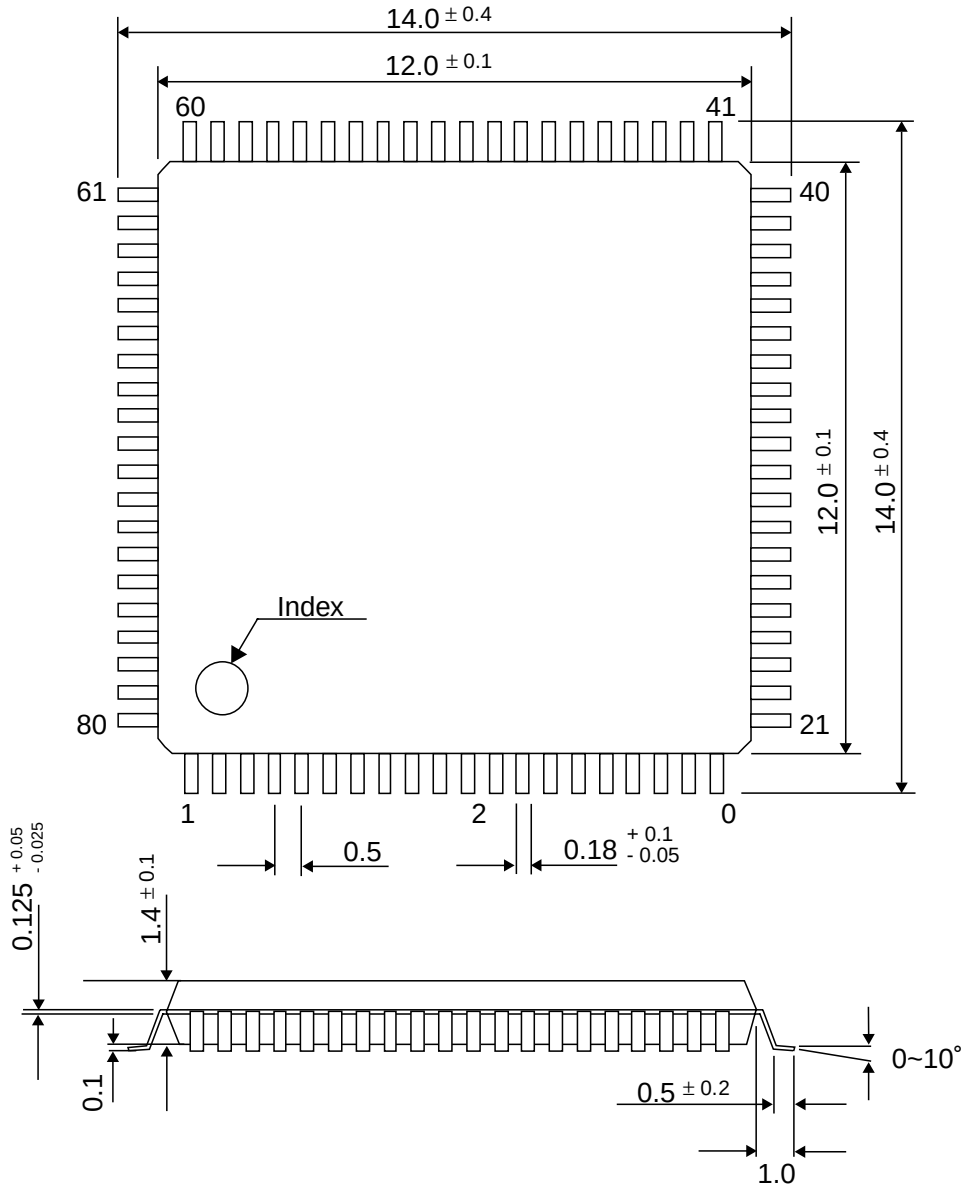
Output Specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{OL} (3.0V)	Low Level Output Current	IOV_{DD} = 3.0V V_O = 0.4V, Type = 1 2 3		1.8 5 10		mA
I_{OL} (3.3V)	Low Level Output Current	IOV_{DD} = 3.3V V_O = 0.4V, Type= 1 2 3		2 6 12		mA
I_{OL} (5.0V)	Low Level Output Current	IOV_{DD} = 5.0V V_O = 0.4V, Type= 1 2 3		3 8 12		mA
I_{OH} (3.0V)	High Level Output Current	IOV_{DD} = 3.0V V_O = IOV_{DD} - 0.4V,Type = 1 2 3		-1.8 -5 -10		mA
I_{OH} (3.3V)	High Level Output Current	IOV_{DD} = 3.3V V_O = IOV_{DD} - 0.4V,Type = 1 2 3		-2 -6 -12		mA
I_{OH} (5.0V)	High Level Output Current	IOV_{DD} = 5.0V V_O = IOV_{DD} - 0.4V,Type = 1 2 3		-3 -8 -12		mA
V_{OL}	Low Level Output Voltage	I = I_{OL}			0.4	V
V_{OH}	High Level Output Voltage	I = I_{OH}	IOV_{DD} - 0.4			V
I_{OZ}	Output Leakage Current	V_{DD} = Max. V_{OH} = V_{DD} V_{OL} = V_{SS}	-1		1	µA
C_{OUT}	Output Pin Capacitance				10	pF
C_{BID}	Bidirectional Pin Capacitance				10	pF

■ MECHANICAL DATA

QFP14 - 80 pin

Unit: mm



Mechanical Drawing QFP14

S1D13705F00A

NOTICE:
No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

© Seiko Epson Corporation 2001, All right reserved.

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION
IC Marketing & Engineering Group

ED International Marketing Department Europe & U.S.A.
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5812 FAX : 042-587-5564

ED International Marketing Department Asia
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814 FAX : 042-587-5110

■ EPSON Electronic Devices Website
http://www.epsondevice.com



Issue October, 2001
Printed in Japan ©