NCP500, NCV500

Voltage Regulator - CMOS, Low Noise, Low-Dropout

150 mA

The NCP500 series of fixed output low dropout linear regulators are designed for portable battery powered applications which require low noise operation, fast enable response time, and low dropout. The device achieves its low noise performance without the need of an external noise bypass capacitor. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, and resistors for setting output voltage, and current limit and temperature limit protection circuits.

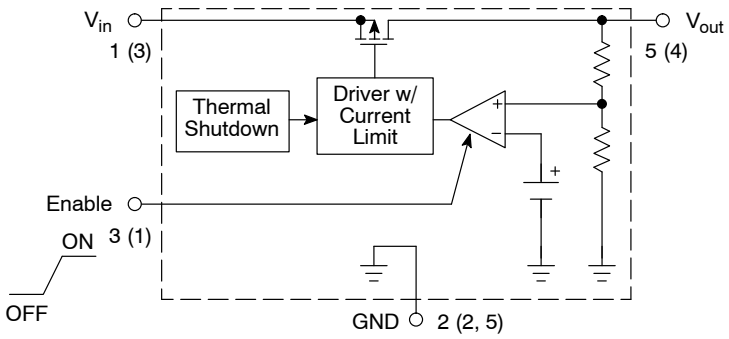
The NCP500 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of 1.0 μF.

Features

- Ultra−Low Dropout Voltage of 170 mV at 150 mA
- Fast Enable Turn−On Time of 20 μsec
- Wide Operating Voltage Range of 1.8 V to 6.0 V
- Excellent Line and Load Regulation
- High Accuracy Output Voltage of 2.5%
- Enable Can Be Driven Directly by 1.0 V Logic
- Typical RMS Noise Voltage 50 μV with No Bypass Capacitor (BW = 10 Hz to 100 kHz)
- Very Small DFN 2x2.2 Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Noise Sensitive Circuits − VCO's, RF Stages, etc.
- SMPS Post−Regulation
- Hand−Held Instrumentation
- Camcorders and Cameras

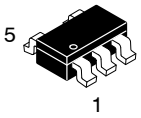


NOTE: Pin numbers in parenthesis indicate DFN package.

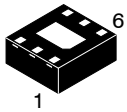
Figure 1. Simplified Block Diagram

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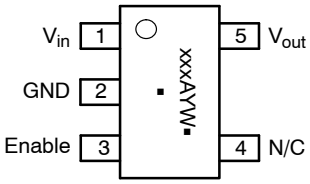
TSOP−5
SN SUFFIX
CASE 483



DFN 2x2.2 MM
SQL SUFFIX
CASE 506BA

PIN CONNECTIONS AND MARKING DIAGRAMS

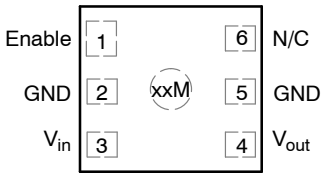
TSOP−5



(Top View)

xxx = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

DFN 2x2.2 mm



(Top View)

xx = Specific Device Code
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

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PIN FUNCTION DESCRIPTION

TSOP−5 Pin No.	DFN 2x2 Pin No.	Pin Name	Description
1	3	V_{in}	Positive power supply input voltage.
2	2, 5	GND	Power supply ground.
3	1	Enable	This input is used to place the device into low−power standby. When this input is pulled to a logic low, the device is disabled. If this function is not used, Enable should be connected to V_{in}.
4	6	N/C	No internal connection.
5	4	V_{out}	Regulated output voltage.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	0 to 6.0	V
Enable Voltage	$V_{on/off}$	−0.3 to V_{in} +0.3	V
Output Voltage	V_{out}	−0.3 to V_{in} +0.3	V
Output Short Circuit Duration	−	Infinite	−
Thermal Resistance, Junction−to−Ambient TSOP−5 DFN (Note 3)	$R_{\theta JA}$	 250 225	°C/W
Operating Junction Temperature	T_J	+125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL−STD−883, Method 3015
   Machine Model Method 200 V Latch up capability (85°C) ±100 mA.
2. Device is internally limited to 160°C by thermal shutdown.
3. For more information, refer to application note, AND8080/D.

ELECTRICAL CHARACTERISTICS (V_{in} = 2.35 V, C_{in} = 1.0 μF, C_{out} = 1.0 μF, for typical value T_A = 25°C, for min and max values T_A = −40°C to 85°C, T_{jmax} = 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
−1.8 V					
Output Voltage (T_A = −40°C to 85°C, I_{out} = 1.0 mA to 150 mA)	V_{out}	1.755	1.8	1.845	V
Line Regulation (V_{in} = 2.3 V to 6.0 V, I_{out} = 1.0 mA)	Reg_{line}	−	1.0	10	mV
Load Regulation (I_{out} = 1.0 mA to 150 mA)	Reg_{load}	−	15	45	mV
Dropout Voltage (Measured at V_{out} −2.0%, T_A = −40°C to 85°C) (Iout = 1.0 mA) (Iout = 75 mA) (Iout = 150 mA)	V_{in}−V_{out}	 − − −	 2.0 140 270	 10 200 350	mV
Output Short Circuit Current	$I_{out(max)}$	200	540	700	mA
Ripple Rejection (V_{in} = $V_{out\ (nom.)}$ + 1.0 V + 0.5 V_{pp}, f = 1.0 kHz, I_o = 60 mA)	RR	−	62	−	dB
Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I_{out} = 1.0 mA) (Enable Input = 0.9 V, I_{out} = 150 mA)	I_Q	 − − −	 0.01 175 175	 1.0 300 300	μA
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(EN)}$	 0.9 −	 − −	 − 0.15	V
Enable Input Bias Current	$I_{IB(EN)}$	−	3.0	100	nA
Output Turn On Time (Enable Input = 0 V to V_{in})	−	−	20	100	μs

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 2.35 V, C_{in} = 1.0 μF, C_{out} = 1.0 μF, for typical value T_A = 25°C, for min and max values T_A = −40°C to 85°C, T_{jmax} = 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
−1.85 V					
Output Voltage (T_A = −40°C to 85°C, I_{out} = 1.0 mA to 150 mA)	V_{out}	1.804	1.85	1.896	V
Line Regulation (V_{in} = 2.3 V to 6.0 V, I_{out} = 1.0 mA)	Reg_{line}	–	1.0	10	mV
Load Regulation (I_{out} = 1.0 mA to 150 mA)	Reg_{load}	–	15	45	mV
Dropout Voltage (Measured at V_{out} −2.0%, T_A = −40°C to 85°C) (Iout = 1.0 mA) (Iout = 75 mA) (Iout = 150 mA)	V_{in}–V_{out}	 – – –	 2.0 – –	 10 – –	mV
Output Short Circuit Current	$I_{out(max)}$	200	540	700	mA
Ripple Rejection (V_{in} = $V_{out\ (nom.)}$ + 1.0 V + 0.5 V_{pp}, f = 1.0 kHz, I_o = 60 mA)	RR	–	62	–	dB
Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I_{out} = 1.0 mA) (Enable Input = 0.9 V, I_{out} = 150 mA)	I_Q	 – – –	 0.01 175 175	 1.0 300 300	μA
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(EN)}$	 0.9 –	 – –	 – 0.15	V
Enable Input Bias Current	$I_{IB(EN)}$	–	3.0	100	nA
Output Turn On Time (Enable Input = 0 V to V_{in})	–	–	20	100	μs

ELECTRICAL CHARACTERISTICS (V_{in} = 3.0 V, C_{in} = 1.0 μF, C_{out} = 1.0 μF, for typical value T_A = 25°C, for min and max values T_A = −40°C to 85°C, T_{jmax} = 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
−2.5 V					
Output Voltage (T_A =−40°C to 85°C, I_{out} = 1.0 mA to 150 mA)	V_{out}	 2.438	 2.5	 2.563	V
Line Regulation (V_{in} = 3.0 V to 6.0 V, I_{out} = 1.0 mA)	Reg_{line}	–	1.0	10	mV
Load Regulation (I_{out} = 1.0 mA to 150 mA)	Reg_{load}	–	15	45	mV
Dropout Voltage (Measured at V_{out} −2.0%, T_A = −40°C to 85°C) (Iout = 1.0 mA) (Iout = 75 mA) (Iout = 150 mA)	V_{in}–V_{out}	 – – –	 2.0 100 190	 10 170 270	mV
Output Short Circuit Current	$I_{out(max)}$	200	540	700	mA
Ripple Rejection (V_{in} = $V_{out\ (nom.)}$ + 1.0 V + 0.5 V_{pp}, f = 1.0 kHz, I_o = 60 mA)	RR	–	62	–	dB
Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I_{out} = 1.0 mA) (Enable Input = 0.9 V, I_{out} = 150 mA)	I_Q	 – – –	 0.01 180 180	 1.0 300 300	μA
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(EN)}$	 0.9 –	 – –	 – 0.15	V
Enable Input Bias Current	$I_{IB(EN)}$	–	3.0	100	nA
Output Turn On Time (Enable Input = 0 V to V_{in})	–	–	20	100	μs

ELECTRICAL CHARACTERISTICS (V_{in} = 3.1 V, C_{in} = 1.0 μF, C_{out} = 1.0 μF, for typical value T_A = 25°C, for min and max values T_A = −40°C to 85°C, T_{jmax} = 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
−2.6 V					
Output Voltage (T_A =−40°C to 85°C, I_{out} = 1.0 mA to 150 mA)	V_{out}	 2.535	 2.6	 2.665	V
Line Regulation (V_{in} = 3.0 V to 6.0 V, I_{out} = 1.0 mA)	Reg_{line}	–	1.0	10	mV
Load Regulation (I_{out} = 1.0 mA to 150 mA)	Reg_{load}	–	15	45	mV
Dropout Voltage (Measured at V_{out} −2.0%, T_A = −40°C to 85°C) (Iout = 1.0 mA) (Iout = 75 mA) (Iout = 150 mA)	V_{in}–V_{out}	 – – –	 2.0 – –	 10 – –	mV
Output Short Circuit Current	$I_{out(max)}$	200	540	700	mA
Ripple Rejection (V_{in} = $V_{out\ (nom.)}$ + 1.0 V + 0.5 V_{pp}, f = 1.0 kHz, I_o = 60 mA)	RR	–	62	–	dB
Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I_{out} = 1.0 mA) (Enable Input = 0.9 V, I_{out} = 150 mA)	I_Q	 – – –	 0.01 180 180	 1.0 300 300	μA
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(EN)}$	 0.9 –	 – –	 – 0.15	V
Enable Input Bias Current	$I_{IB(EN)}$	–	3.0	100	nA
Output Turn On Time (Enable Input = 0 V to V_{in})	–	–	20	100	μs

ELECTRICAL CHARACTERISTICS (V_{in} = 3.2 V, C_{in} = 1.0 μF, C_{out} = 1.0 μF, for typical value T_A = 25°C, for min and max values T_A = −40°C to 85°C, T_{jmax} = 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
−2.7 V					
Output Voltage (T_A =−40°C to 85°C, I_{out} = 1.0 mA to 150 mA)	V_{out}	 2.633	 2.7	 2.768	V
Line Regulation (V_{in} = 3.2 V to 6.0 V, I_{out} = 1.0 mA)	Reg_{line}	–	1.0	10	mV
Load Regulation (I_{out} = 1.0 mA to 150 mA)	Reg_{load}	–	15	45	mV
Dropout Voltage (Measured at V_{out} −2.0%, T_A = −40°C to 85°C) (Iout = 1.0 mA) (Iout = 75 mA) (Iout = 150 mA)	V_{in}–V_{out}	 – – –	 2.0 90 180	 10 160 260	mV
Output Short Circuit Current	$I_{out(max)}$	200	540	700	mA
Ripple Rejection (V_{in} = $V_{out\ (nom.)}$ + 1.0 V + 0.5 V_{pp}, f = 1.0 kHz, I_o = 60 mA)	RR	–	62	–	dB
Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I_{out} = 1.0 mA) (Enable Input = 0.9 V, I_{out} = 150 mA)	I_Q	 – – –	 0.01 185 185	 1.0 300 300	μA
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(EN)}$	 0.9 –	 – –	 – 0.15	V
Enable Input Bias Current	$I_{IB(EN)}$	–	3.0	100	nA
Output Turn On Time (Enable Input = 0 V to V_{in})	–	–	20	100	μs

ELECTRICAL CHARACTERISTICS (V_{in} = 3.3 V, C_{in} = 1.0 μF, C_{out} = 1.0 μF, for typical value T_A = 25°C, for min and max values T_A = −40°C to 85°C, T_{jmax} = 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
−2.8 V					
Output Voltage (T_A =−40°C to 85°C, I_{out} = 1.0 mA to 150 mA)	V_{out}	 2.730	 2.8	 2.870	V
Line Regulation (V_{in} = 3.3 V to 6.0 V, I_{out} = 1.0 mA)	Reg_{line}	–	1.0	10	mV
Load Regulation (I_{out} = 1.0 mA to 150 mA)	Reg_{load}	–	15	45	mV
Dropout Voltage (Measured at V_{out} −2.0%, T_A = −40°C to 85°C) (Iout = 1.0 mA) (Iout = 75 mA) (Iout = 150 mA)	V_{in}–V_{out}	 – – –	 2.0 90 170	 10 150 250	mV
Output Short Circuit Current	$I_{out(max)}$	200	540	700	mA
Ripple Rejection (V_{in} = $V_{out\ (nom.)}$ + 1.0 V + 0.5 V_{pp}, f = 1.0 kHz, I_o = 60 mA)	RR	–	62	–	dB
Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I_{out} = 1.0 mA) (Enable Input = 0.9 V, I_{out} = 150 mA)	I_Q	 – – –	 0.01 185 185	 1.0 300 300	μA
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(EN)}$	 0.9 –	 – –	 – 0.15	V
Enable Input Bias Current	$I_{IB(EN)}$	–	3.0	100	nA
Output Turn On Time (Enable Input = 0 V to V_{in})	–	–	20	100	μs

ELECTRICAL CHARACTERISTICS (V_{in} = 3.5 V, C_{in} = 1.0 μF, C_{out} = 1.0 μF, for typical value T_A = 25°C, for min and max values T_A = −40°C to 85°C, T_{jmax} = 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
−3.0 V					
Output Voltage (T_A =−40°C to 85°C, I_{out} = 1.0 mA to 150 mA)	V_{out}	 2.925	 3.0	 3.075	V
Line Regulation (V_{in} = 3.5 V to 6.0 V, I_{out} = 1.0 mA)	Reg_{line}	–	1.0	10	mV
Load Regulation (I_{out} = 1.0 mA to 150 mA)	Reg_{load}	–	15	45	mV
Dropout Voltage (Measured at V_{out} −2.0%, T_A = −40°C to 85°C) (Iout = 1.0 mA) (Iout = 75 mA) (Iout = 150 mA)	V_{in}–V_{out}	 – – –	 2.0 85 165	 10 130 240	mV
Output Short Circuit Current	$I_{out(max)}$	200	540	700	mA
Ripple Rejection (V_{in} = $V_{out\ (nom.)}$ + 1.0 V + 0.5 V_{pp}, f = 1.0 kHz, I_o = 60 mA)	RR	–	62	–	dB
Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I_{out} = 1.0 mA) (Enable Input = 0.9 V, I_{out} = 150 mA)	I_Q	 – – –	 0.01 190 190	 1.0 300 300	μA
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(EN)}$	 0.9 –	 – –	 – 0.15	V
Enable Input Bias Current	$I_{IB(EN)}$	–	3.0	100	nA
Output Turn On Time (Enable Input = 0 V to V_{in})	–	–	20	100	μs

ELECTRICAL CHARACTERISTICS (V_{in} = 3.8 V, C_{in} = 1.0 μF, C_{out} = 1.0 μF, for typical value T_A = 25°C, for min and max values T_A = −40°C to 85°C, T_{jmax} = 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
−3.3 V					
Output Voltage (T_A =−40°C to 85°C, I_{out} = 1.0 mA to 150 mA)	V_{out}	 3.218	 3.3	 3.383	V
Line Regulation (V_{in} = 3.8 V to 6.0 V, I_{out} = 1.0 mA)	Reg_{line}	–	1.0	10	mV
Load Regulation (I_{out} = 1.0 mA to 150 mA)	Reg_{load}	–	15	45	mV
Dropout Voltage (Measured at V_{out} −2.0%, T_A = −40°C to 85°C) (Iout = 1.0 mA) (Iout = 75 mA) (Iout = 150 mA)	V_{in}–V_{out}	 – – –	 2.0 80 150	 10 110 230	mV
Output Short Circuit Current	$I_{out(max)}$	200	540	700	mA
Ripple Rejection (V_{in} = $V_{out\ (nom.)}$ + 1.0 V + 0.5 V_{pp}, f = 1.0 kHz, I_o = 60 mA)	RR	–	62	–	dB
Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I_{out} = 1.0 mA) (Enable Input = 0.9 V, I_{out} = 150 mA)	I_Q	 – – –	 0.01 195 195	 1.0 300 300	μA
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(EN)}$	 0.9 –	 – –	 – 0.15	V
Enable Input Bias Current	$I_{IB(EN)}$	–	3.0	100	nA
Output Turn On Time (Enable Input = 0 V to V_{in})	–	–	20	100	μs

ELECTRICAL CHARACTERISTICS (V_{in} = 5.5 V, C_{in} = 1.0 μF, C_{out} = 1.0 μF, for typical value T_A = 25°C, for min and max values T_A = −40°C to 85°C, T_{jmax} = 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
−5.0 V					
Output Voltage (T_A =−40°C to 85°C, I_{out} = 1.0 mA to 150 mA)	V_{out}	 4.875	 5.0	 5.125	V
Line Regulation (V_{in} = 5.5 V to 6.0 V, I_{out} = 1.0 mA)	Reg_{line}	–	1.0	10	mV
Load Regulation (I_{out} = 1.0 mA to 150 mA)	Reg_{load}	–	15	45	mV
Dropout Voltage (Measured at V_{out} −2.0%, T_A = −40°C to 85°C) (Iout = 1.0 mA) (Iout = 75 mA) (Iout = 150 mA)	V_{in}–V_{out}	 – – –	 2.0 60 120	 10 100 180	mV
Output Short Circuit Current	$I_{out(max)}$	200	540	700	mA
Ripple Rejection (V_{in} = $V_{out\ (nom.)}$ + 1.0 V + 0.5 V_{pp}, f = 1.0 kHz, I_o = 60 mA)	RR	–	62	–	dB
Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I_{out} = 1.0 mA) (Enable Input = 0.9 V, I_{out} = 150 mA)	I_Q	 – – –	 0.01 210 210	 1.0 300 300	μA
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(EN)}$	 0.9 –	 – –	 – 0.15	V
Enable Input Bias Current	$I_{IB(EN)}$	–	3.0	100	nA
Output Turn On Time (Enable Input = 0 V to V_{in})	–	–	20	100	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Maximum package power dissipation limits must be observed.

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

5. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

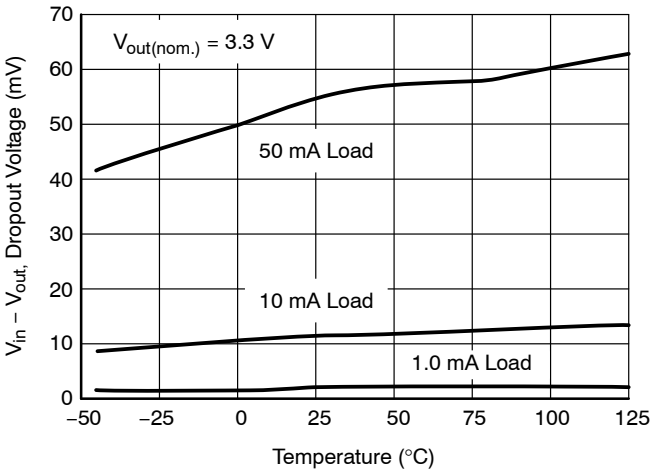


Figure 2. Dropout Voltage vs. Temperature

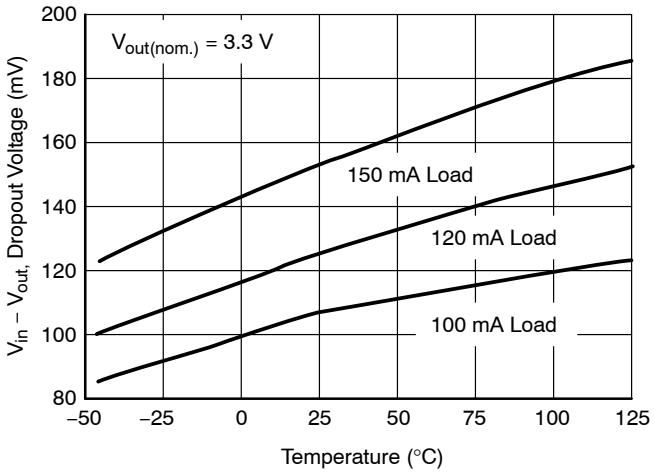


Figure 3. Dropout Voltage vs. Temperature

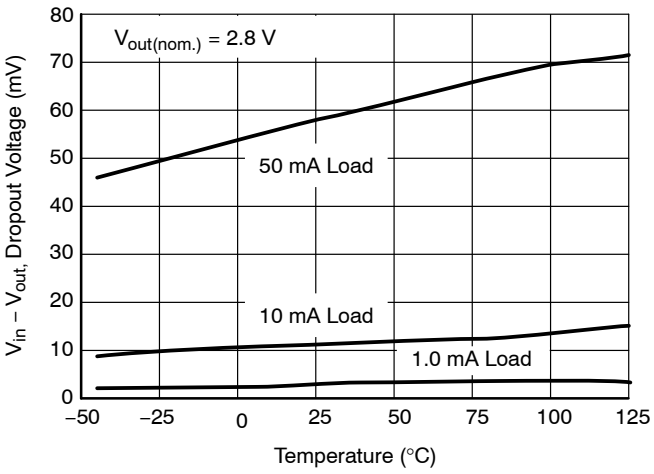


Figure 4. Dropout Voltage vs. Temperature

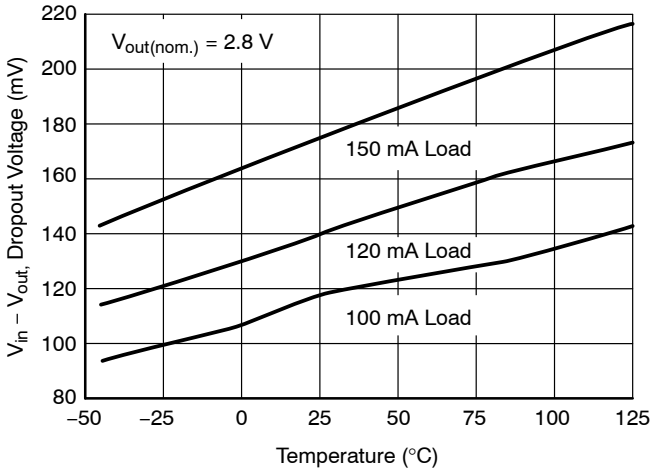


Figure 5. Dropout Voltage vs. Temperature

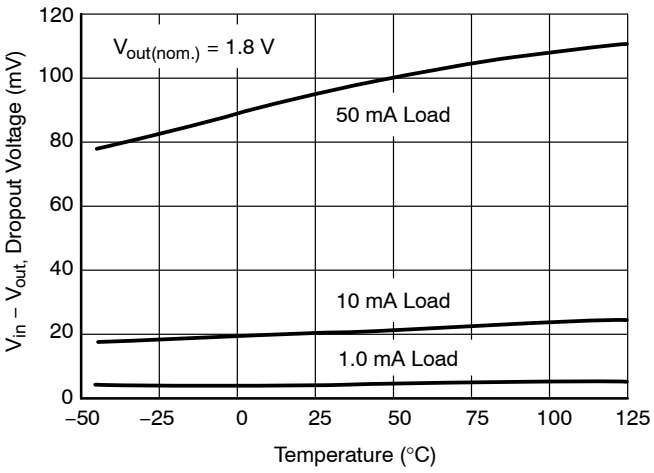


Figure 6. Dropout Voltage vs. Temperature

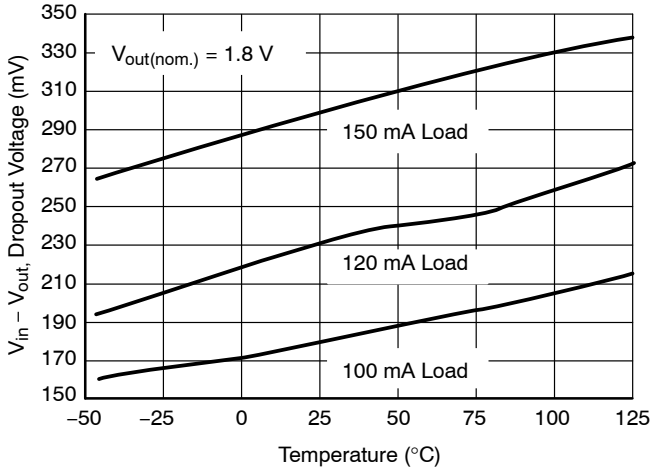


Figure 7. Dropout Voltage vs. Temperature

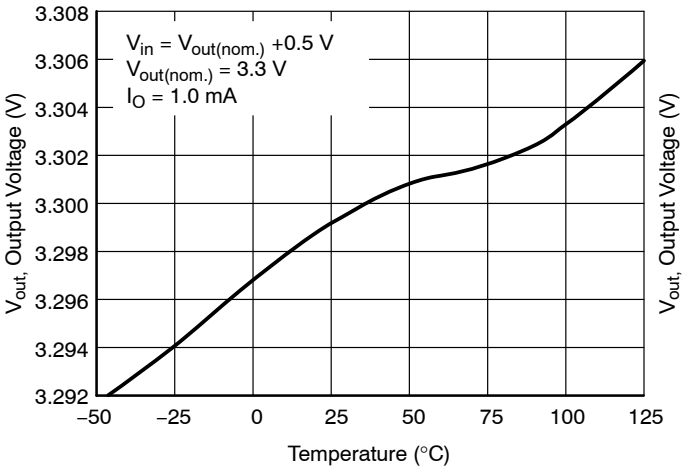


Figure 8. Output Voltage vs. Temperature

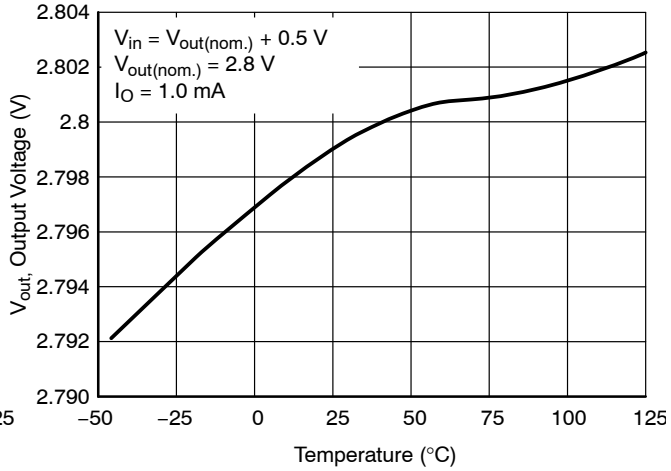


Figure 9. Output Voltage vs. Temperature

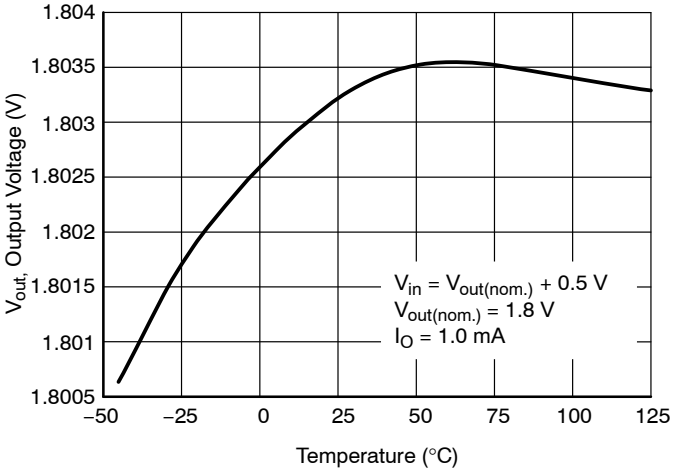


Figure 10. Output Voltage vs. Temperature

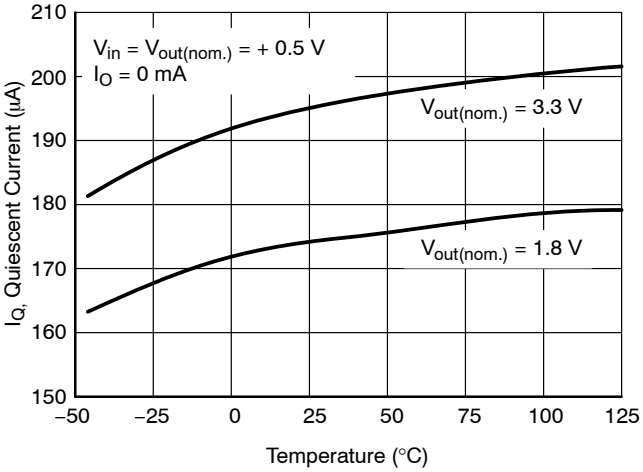


Figure 11. Quiescent Current vs. Temperature

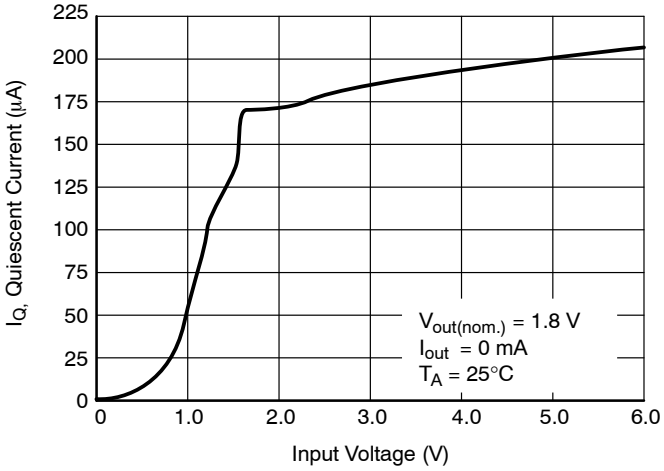


Figure 12. Quiescent Current vs. Input Voltage

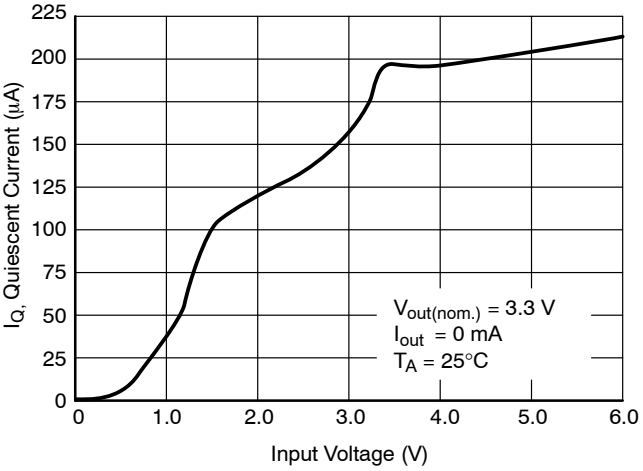


Figure 13. Quiescent Current vs. Input Voltage

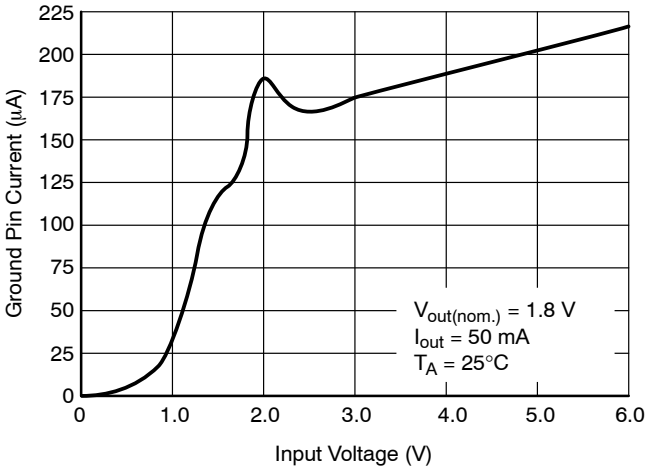


Figure 14. Ground Pin Current vs. Input Voltage

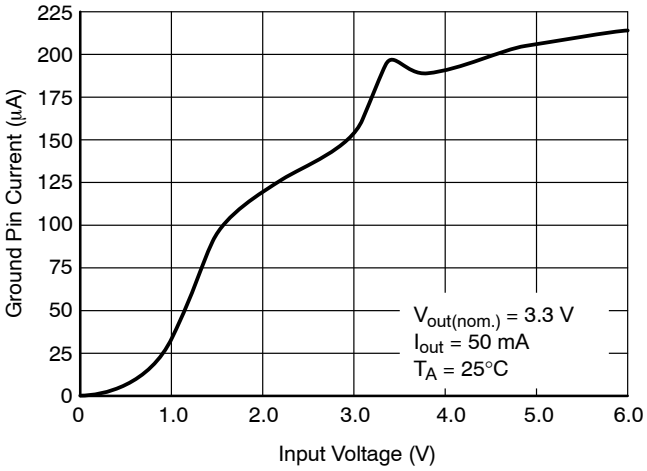


Figure 15. Ground Pin Current vs. Input Voltage

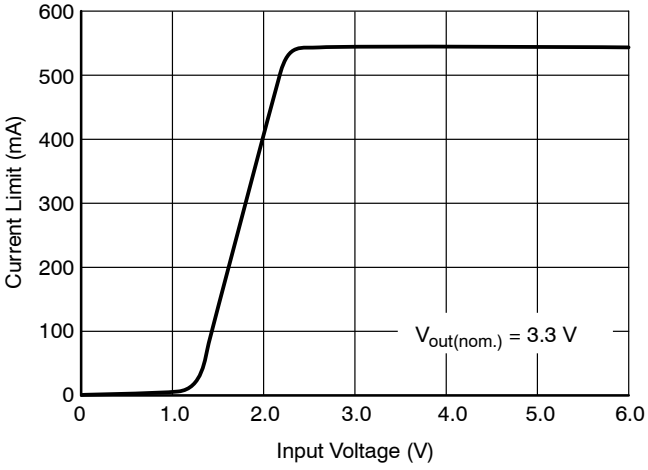


Figure 16. Current Limit vs. Input Voltage

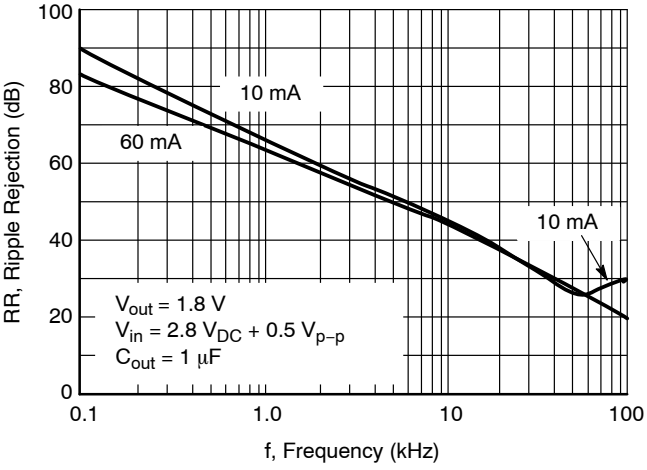


Figure 17. Ripple Rejection vs. Frequency

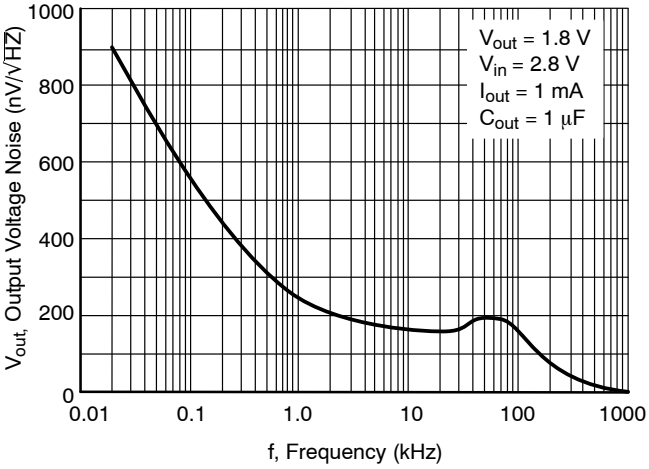


Figure 18. Output Noise Density

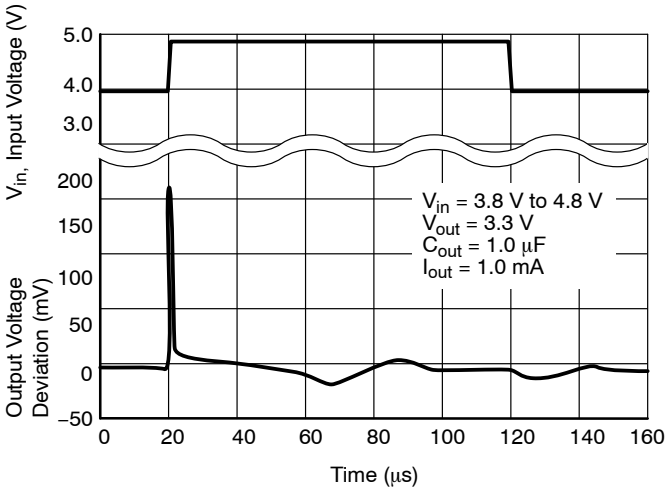


Figure 19. Line Transient Response

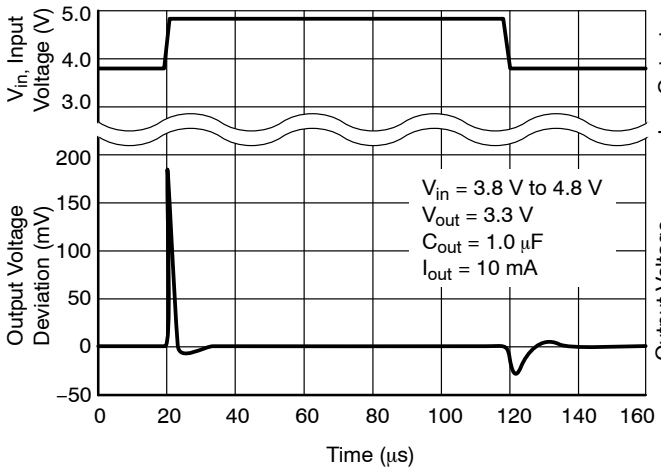


Figure 20. Line Transient Response

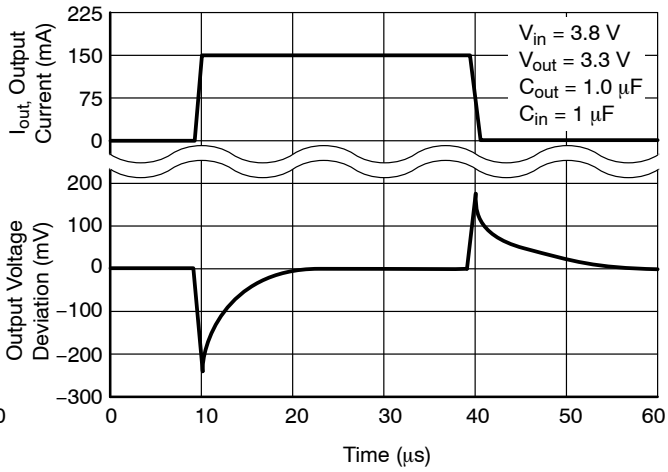


Figure 21. Load Transient Response

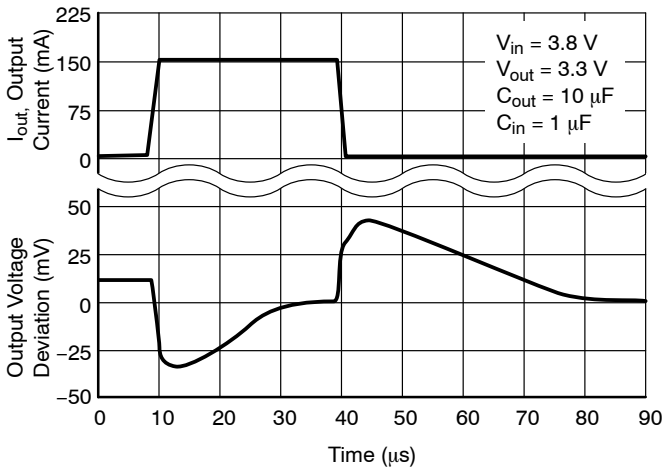


Figure 22. Load Transient Response

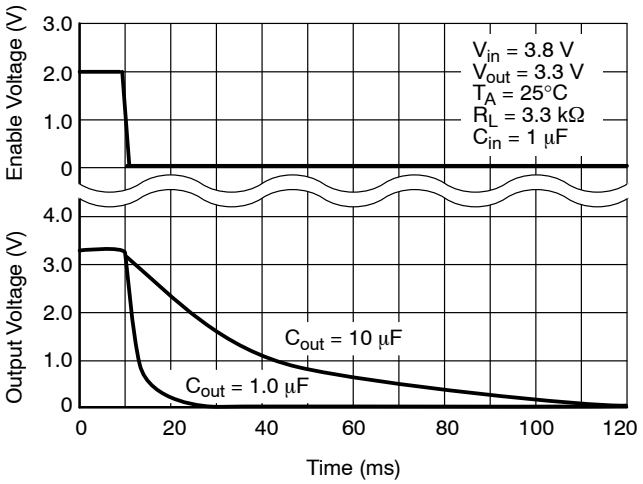


Figure 23. Turn−off Response

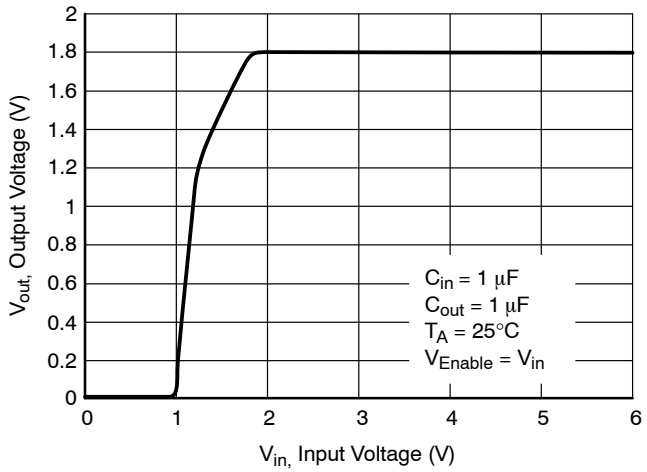


Figure 24. Output Voltage vs. Input Voltage

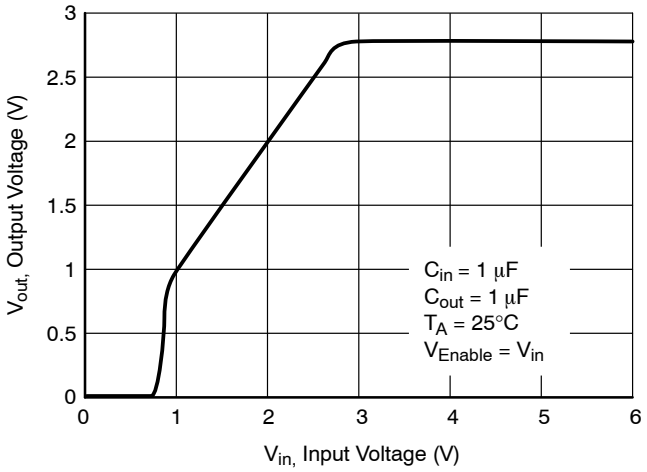


Figure 25. Output Voltage vs. Input Voltage

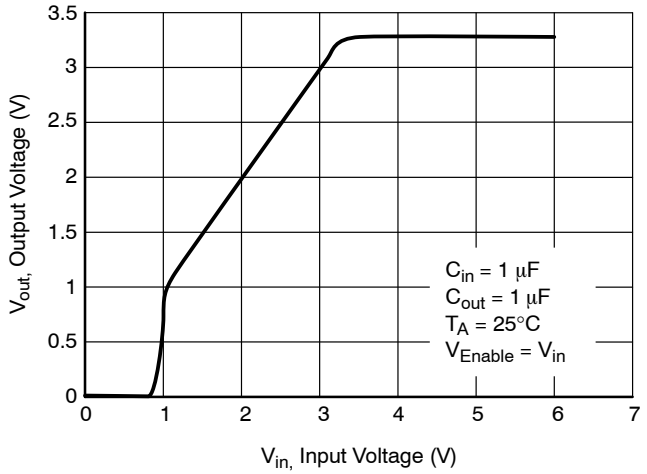


Figure 26. Output Voltage vs. Input Voltage

DEFINITIONS

Load Regulation

The change in output voltage for a change in output load current at a constant temperature.

Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 2% below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Output Noise Voltage

This is the integrated value of the output noise over a specified frequency range. Input voltage and output load current are kept constant during the measurement. Results are expressed in $\mu VRMS$ or $nV\sqrt{Hz}$.

Quiescent Current

The current which flows through the ground pin when the regulator operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 160°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C.

APPLICATIONS INFORMATION

The NCP500 series regulators are protected with internal thermal shutdown and internal current limit. A typical application circuit is shown in Figure 27.

Input Decoupling (C1)

A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP500 package. Higher values and lower ESR will improve the overall line transient response.

Output Decoupling (C2)

The NCP500 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) or a minimum output current. The minimum decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response. Figure 29 shows the stability region for a range of operating conditions and ESR values.

Noise Decoupling

The NCP500 is a low noise regulator without the need of an external bypass capacitor. It typically reaches a noise level of 50 μVRMS overall noise between 10 Hz and 100 kHz. The classical bypass capacitor impacts the start up phase of standard LDOs. However, thanks to its low noise architecture, the NCP500 operates without a bypass element and thus offers a typical 20 μs start up phase.

Enable Operation

The enable pin will turn on or off the regulator. These limits of threshold are covered in the electrical specification section of this data sheet. The turn−on/turn−off transient voltage being supplied to the enable pin should exceed a slew rate of 10 mV/μs to ensure correct operation. If the enable is not to be used then the pin should be connected to V_{in}.

Thermal

As power across the NCP500 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature effect the rate of junction temperature rise for the part. This is stating that when the NCP500 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

If T_J is not recommended to exceed 125°C, then the NCP500 can dissipate up to 400 mW @ 25°C.

The power dissipated by the NCP500 can be calculated from the following equation:

$$P_{tot} = [V_{in} * I_{gnd}\ (I_{out})] + [V_{in} - V_{out}] * I_{out}$$

or

$$V_{inMAX} = \frac{P_{tot} + V_{out} * I_{out}}{I_{gnd} + I_{out}}$$

If a 150 mA output current is needed the ground current is extracted from the data sheet curves: 200 μA @ 150 mA. For a NCP500SN18T1 (1.8 V), the maximum input voltage will then be 4.4 V, good for a 1 Cell Li−ion battery.

Hints

Please be sure the V_{in} and GND lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

Package Placement

DFN packages can be placed using standard pick and place equipment with an accuracy of ±0.05 mm. Component pick and place systems are composed of a vision system that recognizes and positions the component and a mechanical system which physically performs the pick and place operation. Two commonly used types of vision systems are: (1) a vision system that locates a package silhouette and (2) a vision system that locates individual bumps on the interconnect pattern. The latter type renders more accurate place but tends to be more expensive and time consuming. Both methods are acceptable since the parts align due to a self−centering feature of the DFN solder joint during solder re−flow.

Solder Paste

Type 3 or Type 4 solder paste is acceptable.

Re−flow and Cleaning

The DFN may be assembled using standard IR/IR convection SMT re−flow processes without any special considerations. As with other packages, the thermal profile for specific board locations must be determined. Nitrogen purge is recommended during solder for no−clean fluxes. The DFN is qualified for up to three re−flow cycles at 235°C peak (J−STD−020). The actual temperature of the DFN is a function of:

- Component density
- Component location on the board
- Size of surrounding components

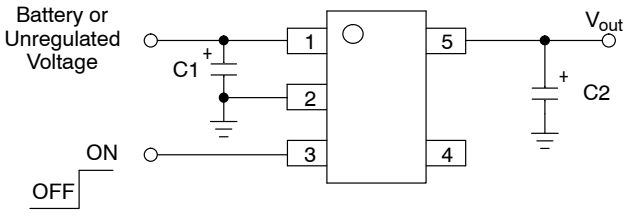


Figure 27. Typical Application Circuit

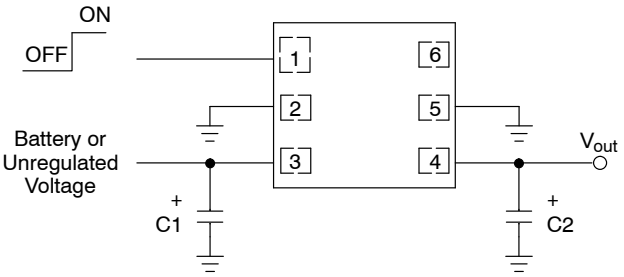


Figure 28. Typical Application Circuit

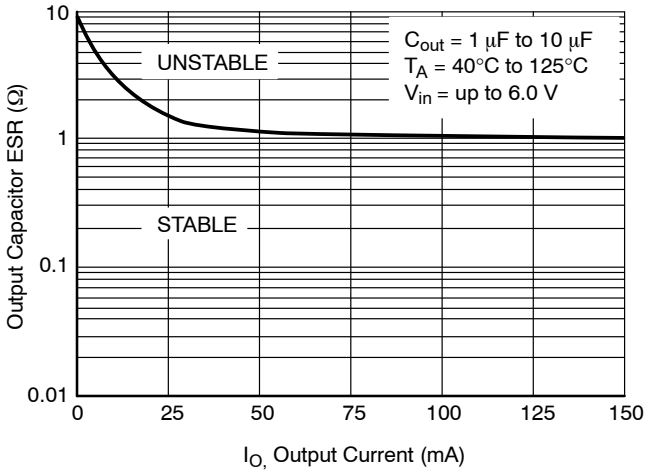


Figure 29. Stability

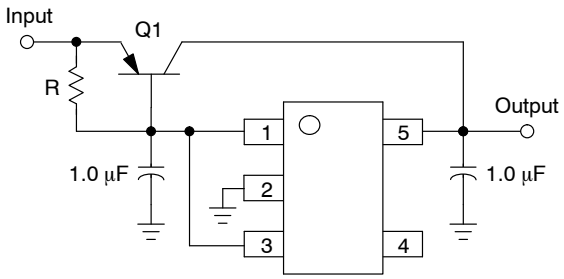


Figure 30. Current Boost Regulator

The NCP500 series can be current boosted with a PNP transistor. Resistor R in conjunction with V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input/Output differential voltage minimum is increased by V_{BE} of the pass resistor.

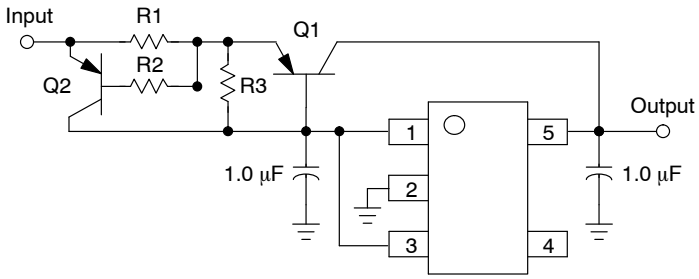


Figure 31. Current Boost Regulator with Short Circuit Limit

Short circuit current limit is essentially set by the V_{BE} of Q2 and R1. $I_{SC} = ((V_{BEQ2} - ib * R2) / R1) + I_{O(max)\ Regulator}$

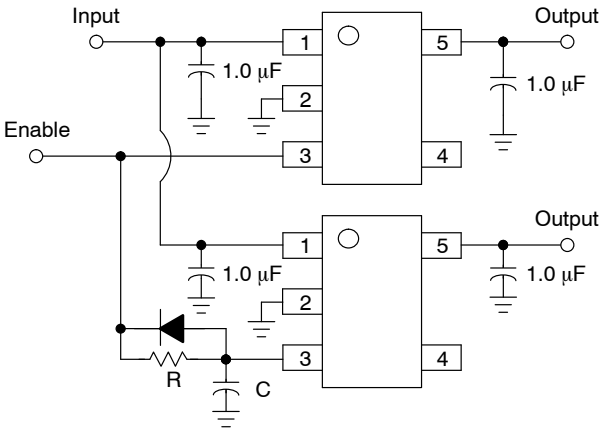


Figure 32. Delayed Turn−on

If a delayed turn−on is needed during power up of several voltages then the above schematic can be used. Resistor R, and capacitor C, will delay the turn−on of the bottom regulator. A few values were chosen and the resulting delay can be seen in Figure 33.

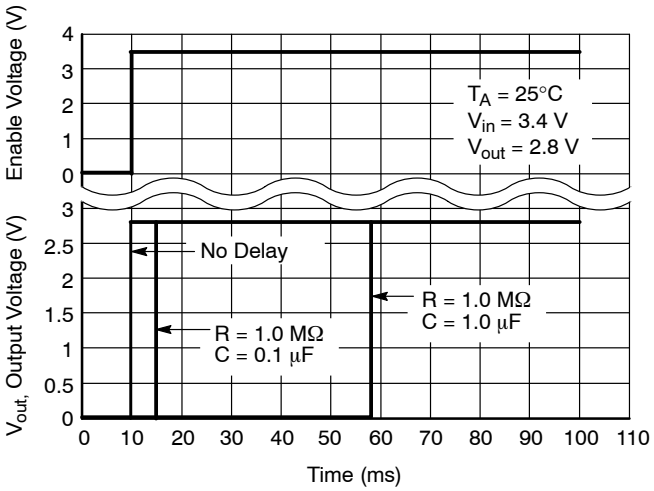


Figure 33. Delayed Turn−on

The graph shows the delay between the enable signal and output turn−on for various resistor and capacitor values.

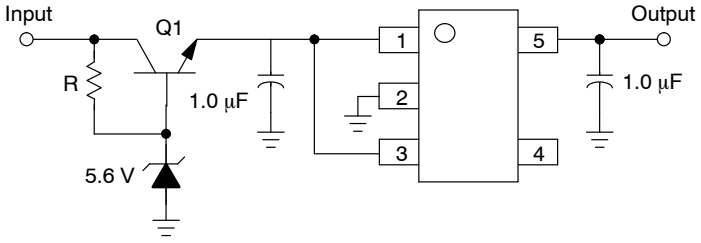


Figure 34. Input Voltages Greater than 6.0 V

A regulated output can be achieved with input voltages that exceed the 6.0 V maximum rating of the NCP500 series with the addition of a simple pre−regulator circuit. Care must be taken to prevent Q1 from overheating when the regulated output (V_{out}) is shorted to G_{nd}.

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Package	Shipping†
NCP500SN18T1G	1.8	LCS	TSOP−5 (Pb−Free)	3000 Units/ 7″ Tape & Reel
NCP500SN185T1G	1.85	LFL		
NCP500SN25T1G	2.5	LCT		
NCP500SN26T1G	2.6	LFM		
NCP500SN27T1G	2.7	LCU		
NCP500SN28T1G	2.8	LCV		
NCP500SN30T1G	3.0	LCW		
NCP500SN30T2G	3.0	LCW		
NCP500SN33T1G	3.3	LCX		
NCP500SN50T1G	5.0	LCY		
NCV500SN185T1G*	1.85	LFL		
NCV500SN18T1G*	1.8	LCS		
NCV500SN28T1G*	2.8	LCV		
NCV500SN33T1G*	3.3	LCX		
NCP500SQL18T1G	1.8	LD	DFN6 2x2.2 (Pb−Free)	3000 Units/ 7″ Tape & Reel
NCP500SQL25T1G	2.5	LE		
NCP500SQL27T1G	2.7	LF		
NCP500SQL28T1G	2.8	LG		
NCP500SQL30T1G	3.0	LH		
NCP500SQL33T1G	3.3	LJ		
NCP500SQL50T1G	5.0	LK		

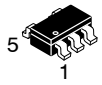
For availability of other output voltages, please contact your local ON Semiconductor Sales Representative.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

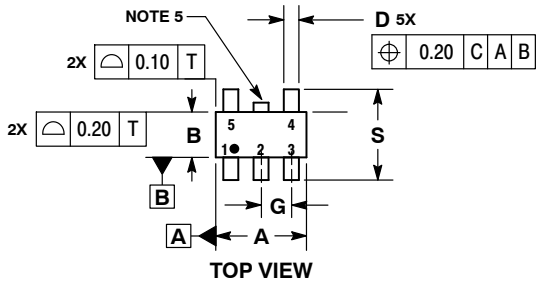
ON Semiconductor®



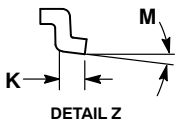
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TSOP−5
CASE 483
ISSUE N

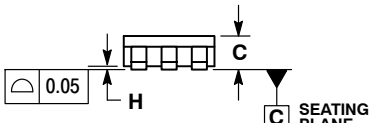
DATE 12 AUG 2020



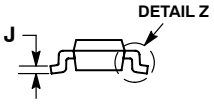
TOP VIEW



DETAIL Z



SIDE VIEW

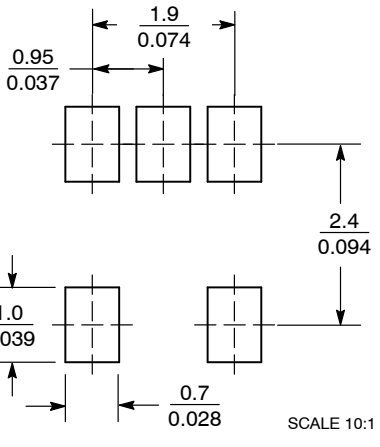


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

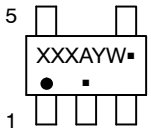
SOLDERING FOOTPRINT*



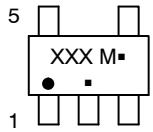
SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

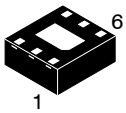
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

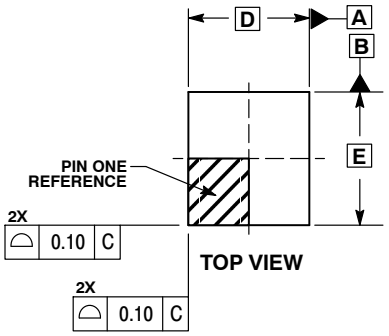
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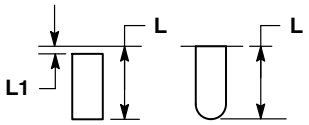


SCALE 4:1

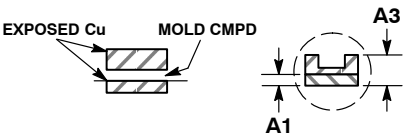
DFN6, 2x2.2, 0.65P
CASE 506BA−01
ISSUE A

DATE 07 JUL 2008

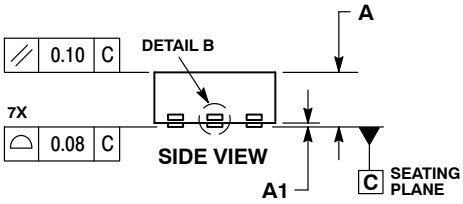


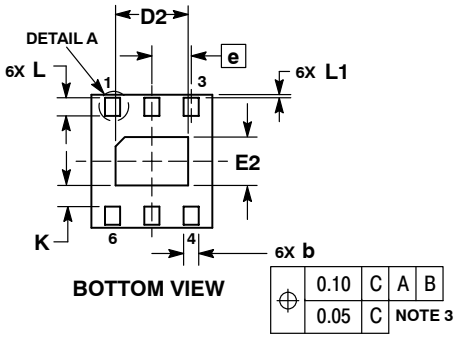


DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS

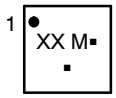




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.20 BSC	
E2	0.70	0.90
e	0.65 BSC	
K	0.20	−−−
L	0.25	0.35
L1	0.00	0.10

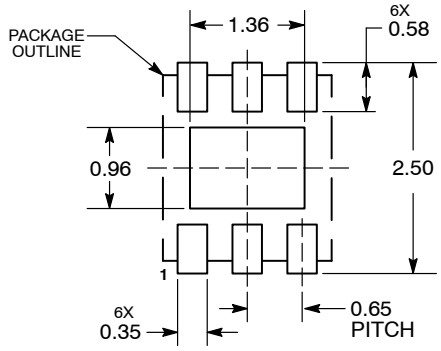
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**6 PIN DFN, 2.0X2.2, 0.65P**	**PAGE 1 OF 1**

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