# SN74HCS74 具有清零和预设功能的施密特触发输入双路正边沿触发式 D 型触发器

## 1 特性

- 宽工作电压范围：2V 至 6V
- 施密特触发输入可实现慢速或高噪声输入信号
- 低功耗
  - $I_{CC}$ 典型值为 100nA
  - 输入泄漏电流典型值为 ±100nA
- 电压为 6V 时，输出驱动为 ±7.8mA
- 工作环境温度范围：–40°C 至 +125°C，$T_A$

## 2 应用

- 将瞬时开关转换为拨动开关
- 在控制器复位期间保持信号
- 输入慢速边沿速率信号
- 可在高噪声环境中运行
- 将时钟信号一分为二

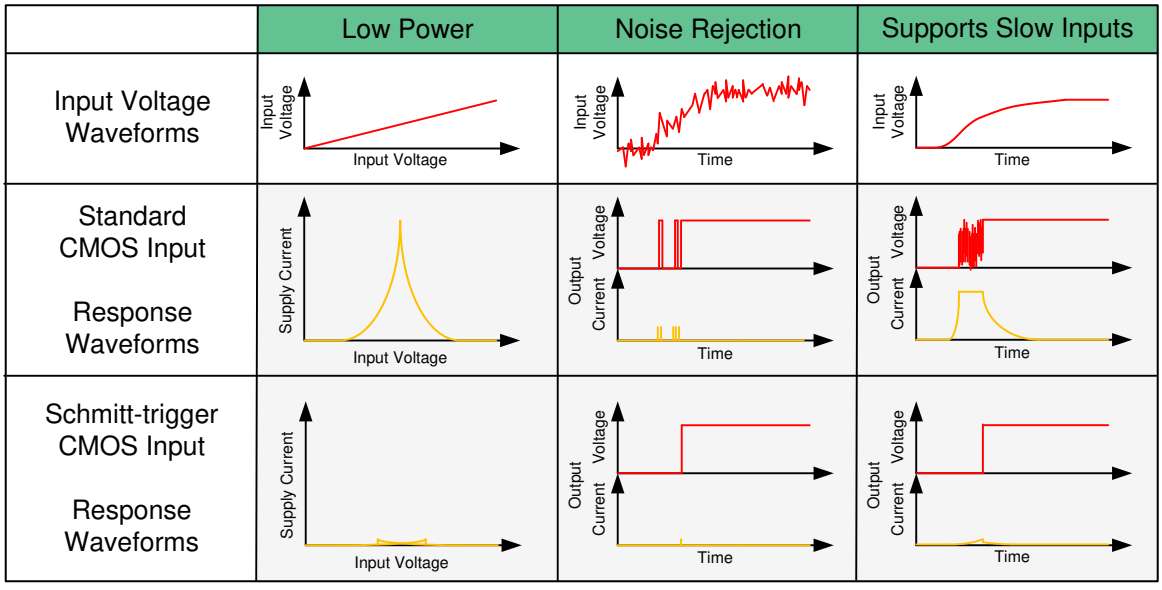
## 3 说明

该器件包含两个独立的 D 型正缘触发触发器。所有输入均包括施密特触发，可实现慢速或高噪声输入信号。将预设 (PRE) 输入设为低电平，会输出高电平。将清零 (CLR) 输入设为低电平，会重新输出低电平。预设和清零功能是异步的，并且不依赖于其他输入的电平。当 PRE 和 CLR 处于非活动状态（高电平）时，数据 (D) 输入处满足设置时间要求的数据将传输到时钟 (CLK) 脉冲正向缘上的输出（Q，$\overline{Q}$）处。时钟触发在一定电压电平下发生，并且不与输入 (CLK) 信号的上升时间直接相关。经过保持时间间隔后，可以更改数据 (D) 输入处的数据而不影响输出（Q，$\overline{Q}$）处的电平。

**器件信息**

| 器件型号 | 封装(1) | 封装尺寸（标称值） |
|---|---|---|
| SN74HCS74PW | TSSOP (14) | 5.00mm × 4.40mm |
| SN74HCS74D | SOIC (14) | 8.70mm × 3.90mm |
| SN74HCS74BQA | WQFN (14) | 3.00mm × 2.50mm |
| SN74HCS74DYY | SOT-23-THIN (14) | 2.00 mm x 4.20 mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




**施密特触发输入的优势**

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

# Table of Contents

**1 特性** ..... 1
**2 应用** ..... 1
**3 说明** ..... 1
**4 Revision History** ..... 2
**5 Pin Configuration and Functions** ..... 3
Pin Functions ..... 3
**6 Specifications** ..... 4
6.1 Absolute Maximum Ratings ..... 4
6.2 ESD Ratings ..... 4
6.3 Recommended Operating Conditions ..... 4
6.4 Thermal Information ..... 4
6.5 Electrical Characteristics ..... 5
6.6 Switching Characteristics ..... 5
6.7 Timing Characteristics ..... 6
6.8 Typical Characteristics ..... 7
**7 Parameter Measurement Information** ..... 8
**8 Detailed Description** ..... 9
8.1 Overview ..... 9
8.2 Functional Block Diagram ..... 9
8.3 Feature Description ..... 9
8.4 Device Functional Modes ..... 10
**9 Application and Implementation** ..... 11
9.1 Application Information ..... 11
9.2 Typical Application ..... 11
**10 Power Supply Recommendations** ..... 14
**11 Layout** ..... 14
11.1 Layout Guidelines ..... 14
11.2 Layout Example ..... 14
**12 Device and Documentation Support** ..... 15
12.1 Documentation Support ..... 15
12.2 接收文档更新通知 ..... 15
12.3 支持资源 ..... 15
12.4 Trademarks ..... 15
12.5 静电放电警告 ..... 15
12.6 术语表 ..... 15
**13 Mechanical, Packaging, and Orderable Information** ..... 16

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

**Changes from Revision C (January 2021) to Revision D (December 2021)** — **Page**

- 向“器件信息”添加了 DYY 封装信息 ..... 1
- Added DYY package information to *Pin Configuration and Functions* ..... 3
- Added DYY package to Thermal Information table ..... 4

**Changes from Revision B (November 2020) to Revision C (January 2021)** — **Page**

- 将 BQA 封装状态从“预发布”更改为“正在供货” ..... 1
- 将数据表状态从“混合状态”更改为“量产数据” ..... 1

**Changes from Revision A (May 2020) to Revision B (November 2020)** — **Page**

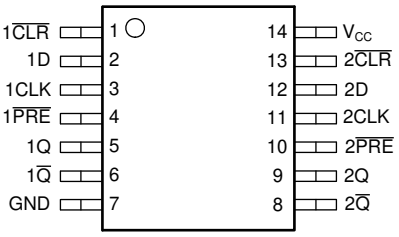
- 更新了整个文档中的表格、图和交叉参考的编号格式。 ..... 1
- 向“器件信息”添加了 BQA 封装信息 ..... 1
- Added BQA pinout diagram and package information to *Pin Configuration and Functions* ..... 3
- Added BQA package to *Thermal Information* table ..... 4

**Changes from Revision * (November 2019) to Revision A (May 2020)** — **Page**

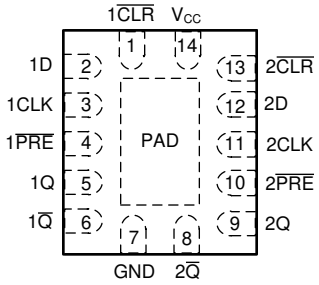
- 向“器件信息”添加了 D 封装信息 ..... 1
- Added D package information to *Pin Configuration and Functions* ..... 3
- Added D package column to *Thermal Information* table ..... 4


Copyright © 2022 Texas Instruments Incorporated

# 5 Pin Configuration and Functions




**D, PW or DYY Package**
**14-Pin SOIC, TSSOP or SOT**
**Top View**




**BQA Package**
**14-Pin WQFN**
**Top View**

## Pin Functions

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1 $\overline{CLR}$ | 1 | Input | Clear for channel 1, active low |
| 1D | 2 | Input | Data for channel 1 |
| 1CLK | 3 | Input | Clock for channel 1, rising edge triggered |
| 1 $\overline{PRE}$ | 4 | Input | Preset for channel 1, active low |
| 1Q | 5 | Output | Output for channel 1 |
| 1 $\overline{Q}$ | 6 | Output | Inverted output for channel 1 |
| GND | 7 | — | Ground |
| 2 $\overline{Q}$ | 8 | Output | Inverted output for channel 2 |
| 2Q | 9 | Output | Output for channel 2 |
| 2 $\overline{PRE}$ | 10 | Input | Preset for channel 2, active low |
| 2CLK | 11 | Input | Clock for channel 2, rising edge triggered |
| 2D | 12 | Input | Data for channel 2 |
| 2 $\overline{CLR}$ | 13 | Input | Clear for channel 2, active low |
| $V_{CC}$ | 14 | — | Positive supply |
| Thermal Pad(1) | | — | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply |

(1) BQA package only.

Copyright © 2022 Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I$ < –0.5 V or $V_I$ > $V_{CC}$ + 0.5 V | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_I$ < –0.5 V or $V_I$ > $V_{CC}$ + 0.5 V | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±35 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_J$ | Junction temperature(3) | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Assured by design.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2 | 5 | 6 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | V |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74HCS74 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | PW (TSSOP) | D (SOIC) | BQA (WQFN) | DYY (SOT) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 151.7 | 133.6 | 109.7 | 236.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 79.4 | 89.0 | 111.0 | 143.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 94.7 | 89.5 | 77.9 | 146.0 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 25.2 | 45.5 | 20.2 | 29.5 | °C/W |


Copyright © 2022 Texas Instruments Incorporated

| THERMAL METRIC(1) | | SN74HCS74 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | PW (TSSOP) | D (SOIC) | BQA (WQFN) | DYY (SOT) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 94.1 | 89.1 | 77.8 | 145.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | 56.6 | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive switching threshold | | | 2 V | 0.7 | | 1.5 | V |
| | | | | 4.5 V | 1.7 | | 3.15 | |
| | | | | 6 V | 2.1 | | 4.2 | |
| $V_{T-}$ | Negative switching threshold | | | 2 V | 0.3 | | 1.0 | V |
| | | | | 4.5 V | 0.9 | | 2.2 | |
| | | | | 6 V | 1.2 | | 3.0 | |
| $\Delta V_T$ | Hysteresis ($V_{T+}$ - $V_{T-}$)(1) | | | 2 V | 0.2 | | 1.0 | V |
| | | | | 4.5 V | 0.4 | | 1.4 | |
| | | | | 6 V | 0.6 | | 1.6 | |
| $V_{OH}$ | High-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20 µA | 2 V to 6 V | $V_{CC}$ – 0.1 | $V_{CC}$ – 0.002 | | V |
| | | | $I_{OH}$ = -6 mA | 4.5 V | 4.0 | 4.3 | | |
| | | | $I_{OH}$ = -7.8 mA | 6 V | 5.4 | 5.75 | | |
| $V_{OL}$ | Low-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V to 6 V | | 0.002 | 0.1 | V |
| | | | $I_{OL}$ = 6 mA | 4.5 V | | 0.18 | 0.30 | |
| | | | $I_{OL}$ = 7.8 mA | 6 V | | 0.22 | 0.33 | |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or 0 | | 6 V | | ±100 | ±1000 | nA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or 0, $I_O$ = 0 | | 6 V | | 0.1 | 2 | µA |
| $C_i$ | Input capacitance | | | 2 V to 6 V | | | 5 | pF |
| $C_{pd}$ | Power dissipation capacitance per gate | No load | | 2 V to 6 V | | 10 | | pF |

(1) Guaranteed by design.

## 6.6 Switching Characteristics

$C_L$ = 50 pF; over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Max switching frequency | | | 2 V | 18 | 31 | | MHz |
| | | | | 4.5 V | 45 | 95 | | |
| | | | | 6 V | 65 | 105 | | |
| $t_{pd}$ | Propagation delay | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 2 V | | 19 | 42 | ns |
| | | | | 4.5 V | | 8 | 19 | |
| | | | | 6 V | | 7 | 15 | |
| | | CLK | Q or $\overline{Q}$ | 2 V | | 19 | 42 | ns |
| | | | | 4.5 V | | 8 | 19 | |
| | | | | 6 V | | 7 | 15 | |

Copyright © 2022 Texas Instruments Incorporated

$C_L$ = 50 pF; over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_t$ | Transition-time | | Q or $\overline{Q}$ | 2 V | | 9 | 16 | ns |
| | | | | 4.5 V | | 5 | 9 | |
| | | | | 6 V | | 4 | 8 | |

## 6.7 Timing Characteristics

$C_L$ = 50 pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*.

| PARAMETER | | | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{clock}$ | Clock frequency | | 2 V | | 18 | MHz |
| | | | 4.5 V | | 45 | |
| | | | 6 V | | 65 | |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 2 V | 11 | | ns |
| | | | 4.5 V | 11 | | |
| | | | 6 V | 11 | | |
| | | CLK high or low | 2 V | 14 | | ns |
| | | | 4.5 V | 12 | | |
| | | | 6 V | 11 | | |
| $t_{su}$ | Setup time before CLK high | Data | 2 V | 24 | | ns |
| | | | 4.5 V | 9 | | |
| | | | 6 V | 6 | | |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 2 V | 7 | | ns |
| | | | 4.5 V | 5 | | |
| | | | 6 V | 5 | | |
| $t_h$ | Hold time | Data after CLK ↑ | 2 V | 0 | | ns |
| | | | 4.5 V | 0 | | |
| | | | 6 V | 0 | | |


Copyright © 2022 Texas Instruments Incorporated

## 6.8 Typical Characteristics

$T_A$ = 25°C

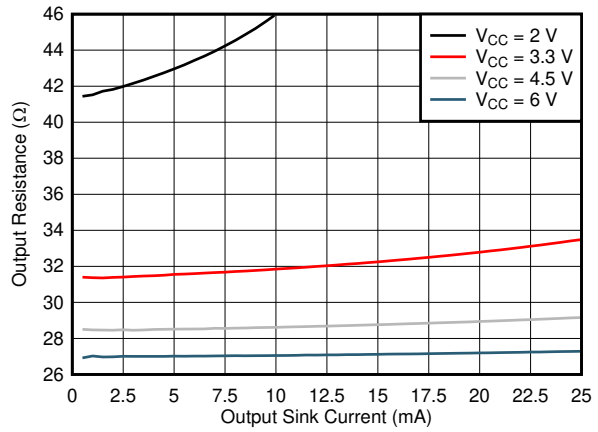



图 6-1. Output Driver Resistance in LOW State

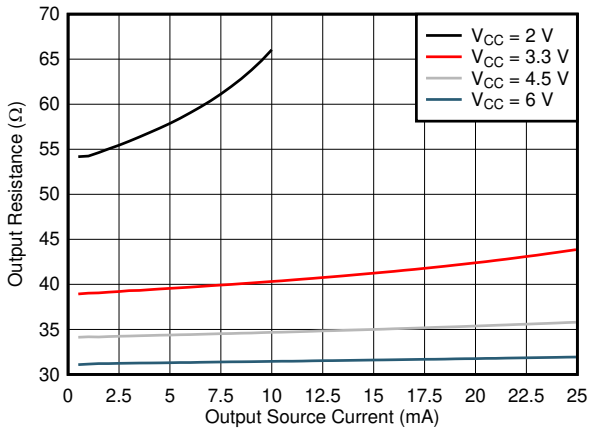



图 6-2. Output Driver Resistance in HIGH State

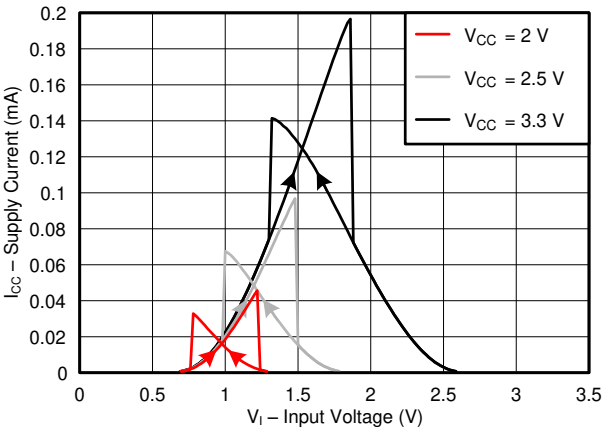



图 6-3. Supply Current Across Input Voltage, 2-, 2.5-, and 3.3-V Supply

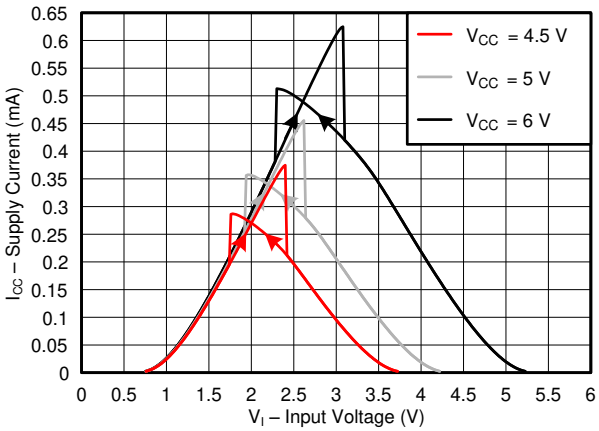



图 6-4. Supply Current Across Input Voltage, 4.5-, 5-, and 6-V Supply

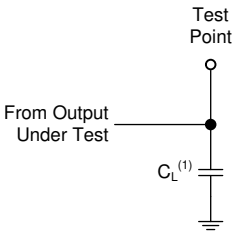
Copyright © 2022 Texas Instruments Incorporated

## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 2.5 ns.

For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.




(1) $C_L$ includes probe and test-fixture capacitance.

**图 7-1. Load Circuit for Push-Pull Outputs**

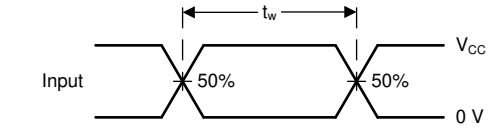



**图 7-2. Voltage Waveforms, Pulse Duration**

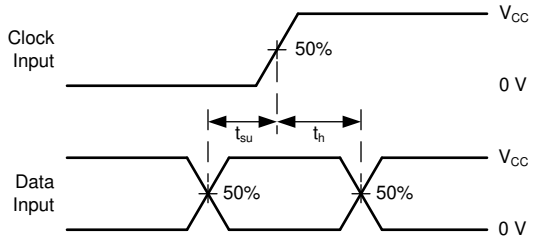
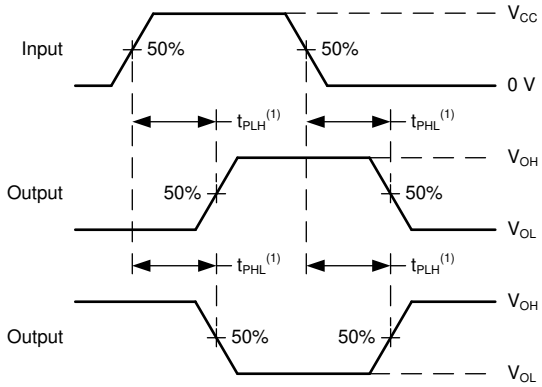
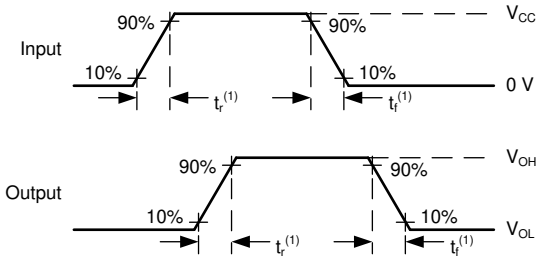



**图 7-3. Voltage Waveforms, Setup and Hold Times**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**图 7-4. Voltage Waveforms Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

**图 7-5. Voltage Waveforms, Input and Output Transition Times**


Copyright © 2022 Texas Instruments Incorporated

# 8 Detailed Description

## 8.1 Overview

Logic Diagram (Positive Logic) for one channel of SN74HCS74 describes the SN74HCS74. As the SN74HCS74 is a dual D-Type positive-edge-triggered flip-flop with clear and preset, the diagram below describes one of the two device flip-flops.

## 8.2 Functional Block Diagram

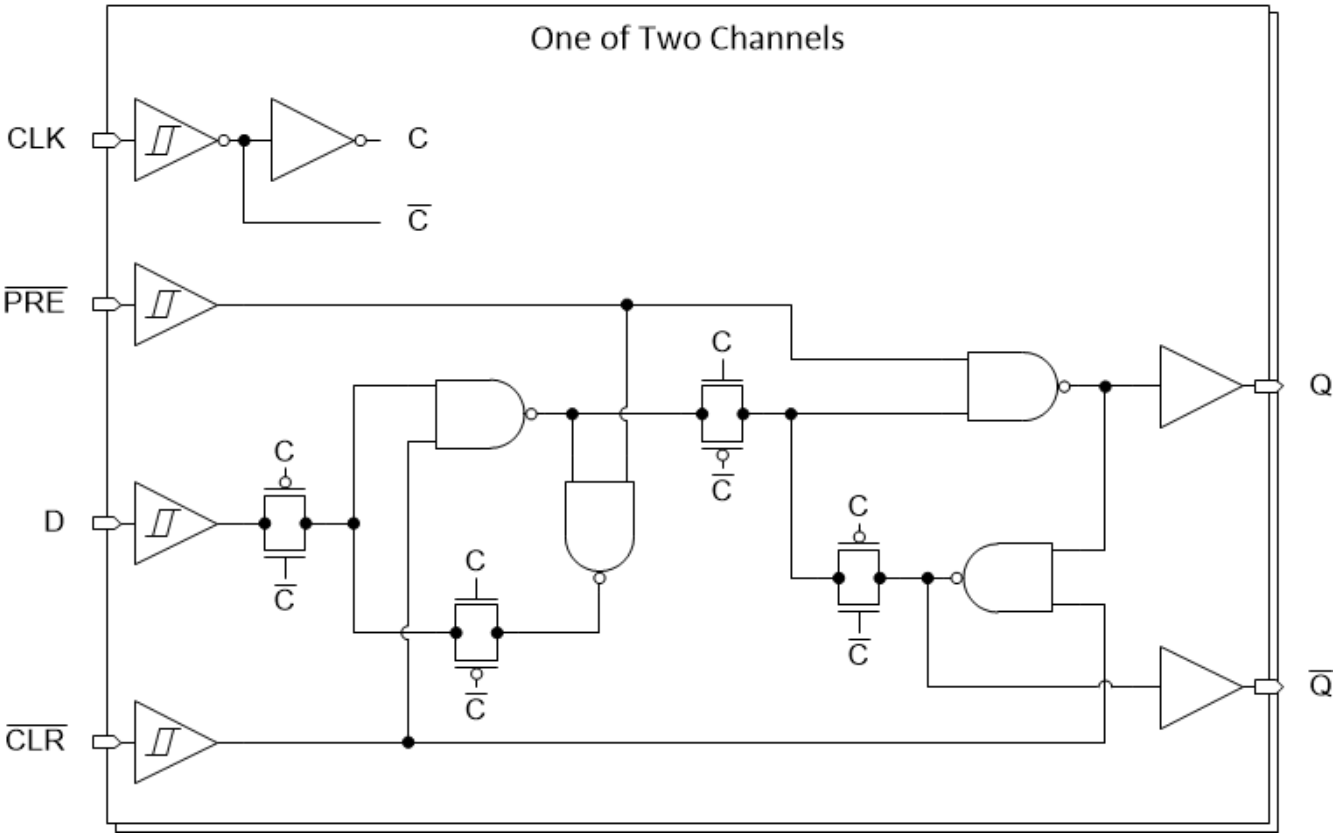



**图 8-1. Logic Diagram (Positive Logic) for one channel of SN74HCS74**

## 8.3 Feature Description

### 8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

### 8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

Copyright © 2022 Texas Instruments Incorporated

The Schmitt-trigger input architecture provides hysteresis as defined by $\Delta V_T$ in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Electrical Placement of Clamping Diodes for Each Input and Output.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

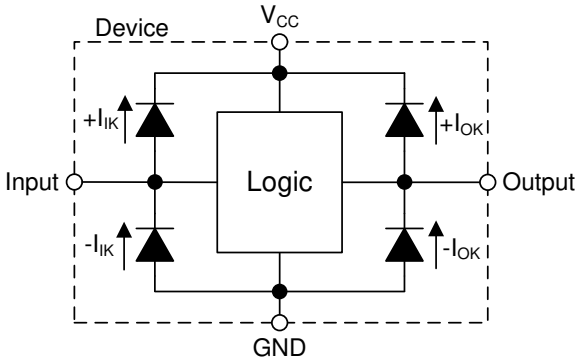



**图 8-2. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

Function Table lists the functional modes of the SN74HCS74.

**表 8-1. Function Table**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H(1) | H(1) |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.


Copyright © 2022 Texas Instruments Incorporated

# 9 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 9.1 Application Information

Toggle switches are typically large, mechanically complex and relatively expensive. It is desirable to use a momentary switch instead because they are small, mechanically simple and low cost. Some systems require a toggle switch's functionality but are space or cost constrained and must use a momentary switch instead. The SN74HCS74 has integrated Schmitt-trigger inputs that eliminate the need for a second IC for signal conditioning, reducing the required board space. This makes the SN74HCS74 an ideal device for converting a momentary switch into a toggle switch.

If the data input (D) of the SN74HCS74 is tied to the inverted output ( $\overline{Q}$), then each clock pulse will cause the value at the output (Q) to toggle. The momentary switch can be debounced and directly connected to the clock input (CLK) to toggle the output.

## 9.2 Typical Application

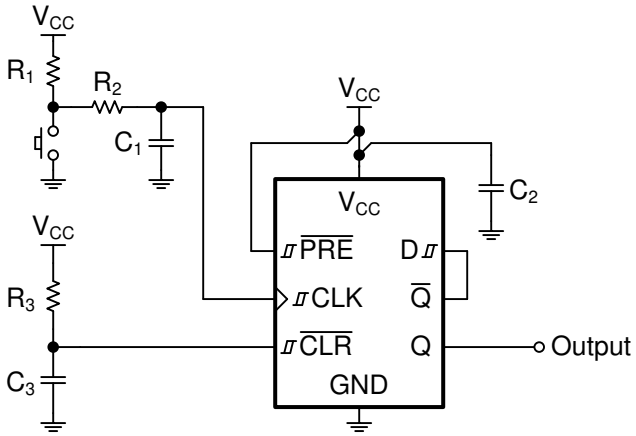



**图 9-1. Device Power Button Circuit**

### 9.2.1 Design Requirements

#### *9.2.1.1 Power Considerations*

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS74 plus the maximum static supply current, $I_{CC}$, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS74 plus the maximum supply current, $I_{CC}$, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS74 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

Copyright © 2022 Texas Instruments Incorporated

The SN74HCS74 can drive a load with total resistance described by $R_L \geqslant V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### *9.2.1.2 Input Considerations*

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS74, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HCS74 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than $V_{CC}$ or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### *9.2.1.3 Output Considerations*

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.


Copyright © 2022 Texas Instruments Incorporated

2. Ensure the capacitive load at the output is ⩽ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS74 to the receiving device(s).
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.

### 9.2.3 Application Curve

Circuit response without RC debounce
$V_{in}$ := CLK input, $V_{out}$ := Q output illustrates an example of a single button press bouncing and causing the output to toggle multiple times. This will cause issues in the desired application. Circuit response with RC debounce
$V_{in}$ := CLK input, $V_{out}$ := Q output illustrates 4 button presses with an added debounce circuit, fixing the unwanted toggling and allowing for proper toggle switch operation.

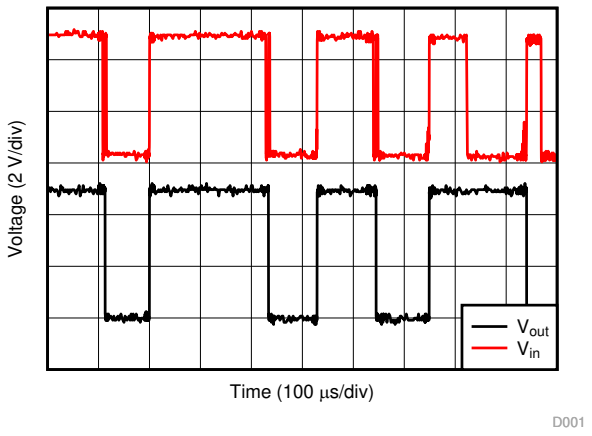



**图 9-2. Circuit response without RC debounce**
**$V_{in}$ := CLK input, $V_{out}$ := Q output**

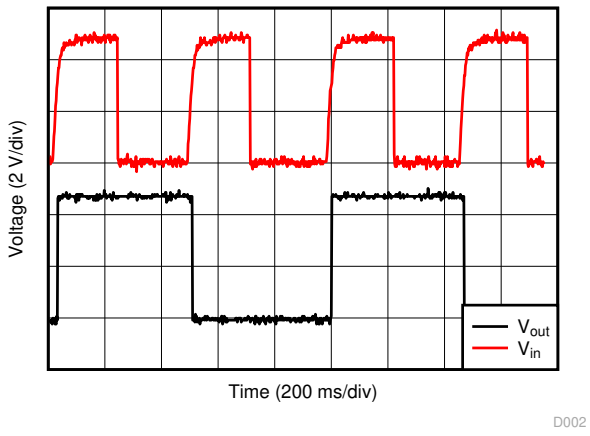



**图 9-3. Circuit response with RC debounce**
**$V_{in}$ := CLK input, $V_{out}$ := Q output**

Copyright © 2022 Texas Instruments Incorporated

# 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

# 11 Layout

## 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

## 11.2 Layout Example

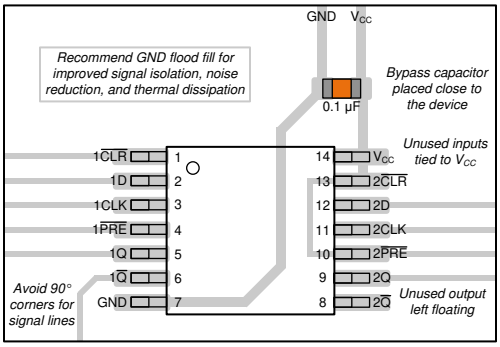



**图 11-1. Layout Example of the SN74HCS74**


Copyright © 2022 Texas Instruments Incorporated

# 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *HCMOS Design Considerations* application report (SCLA007)
- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application report (SDYA009)
- Texas Instruments, *Designing With Logic* application report

## 12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 12.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

Copyright © 2022 Texas Instruments Incorporated

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


Copyright © 2022 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74HCS74BQAR | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | HCS74 |
| SN74HCS74BQAR.A | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS74 |
| SN74HCS74DR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | HCS74 |
| SN74HCS74DR.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS74 |
| SN74HCS74DYYR | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS74 |
| SN74HCS74DYYR.A | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS74 |
| SN74HCS74PWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | HCS74 |
| SN74HCS74PWR.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS74 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74HCS74 :**

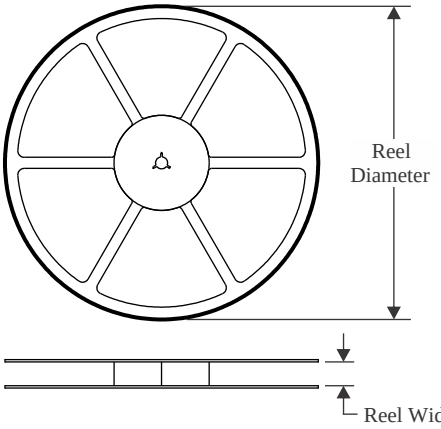
- Automotive : SN74HCS74-Q1

NOTE: Qualified Version Definitions:

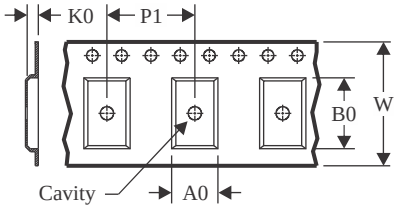
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

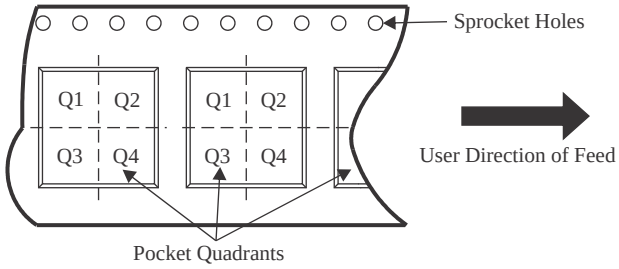



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

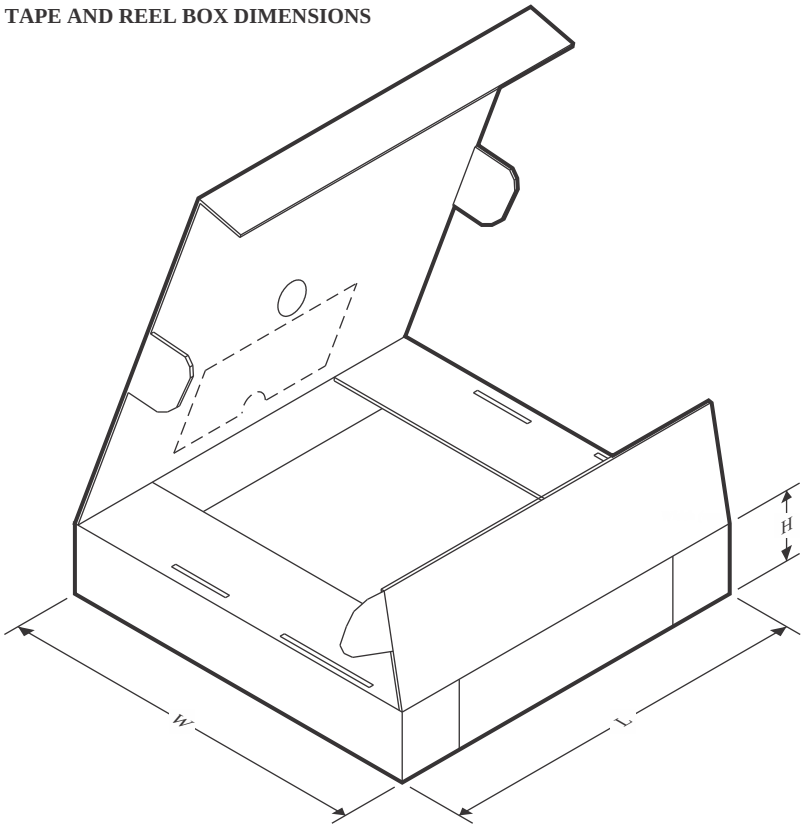
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HCS74BQAR | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |
| SN74HCS74BQAR | WQFN | BQA | 14 | 3000 | 177.8 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |
| SN74HCS74DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.6 | 9.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCS74DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCS74DYYR | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| SN74HCS74PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCS74PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

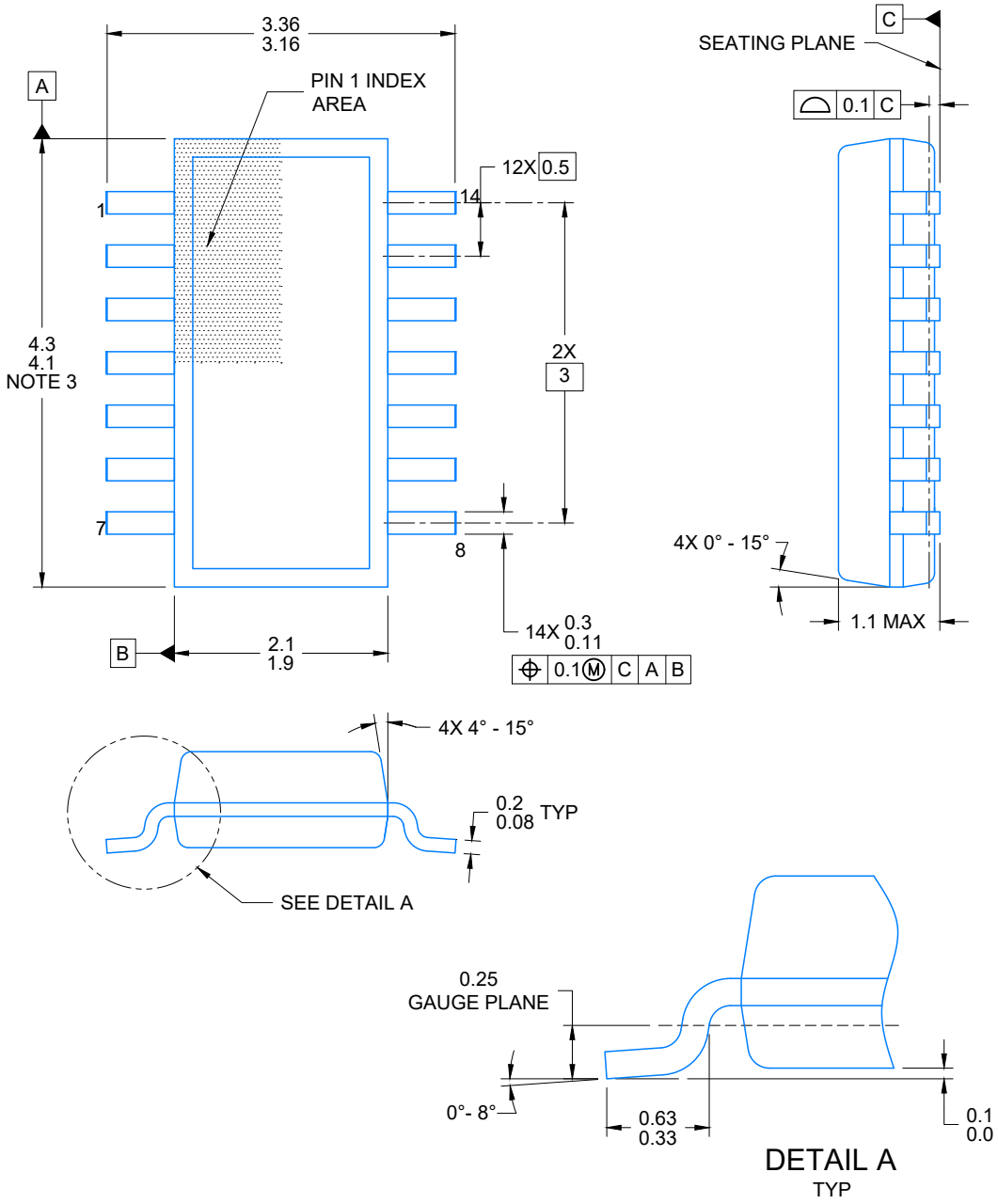
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HCS74BQAR | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74HCS74BQAR | WQFN | BQA | 14 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74HCS74DR | SOIC | D | 14 | 2500 | 366.0 | 364.0 | 50.0 |
| SN74HCS74DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HCS74DYYR | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |
| SN74HCS74PWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HCS74PWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

# PACKAGE OUTLINE

## DYY0014A

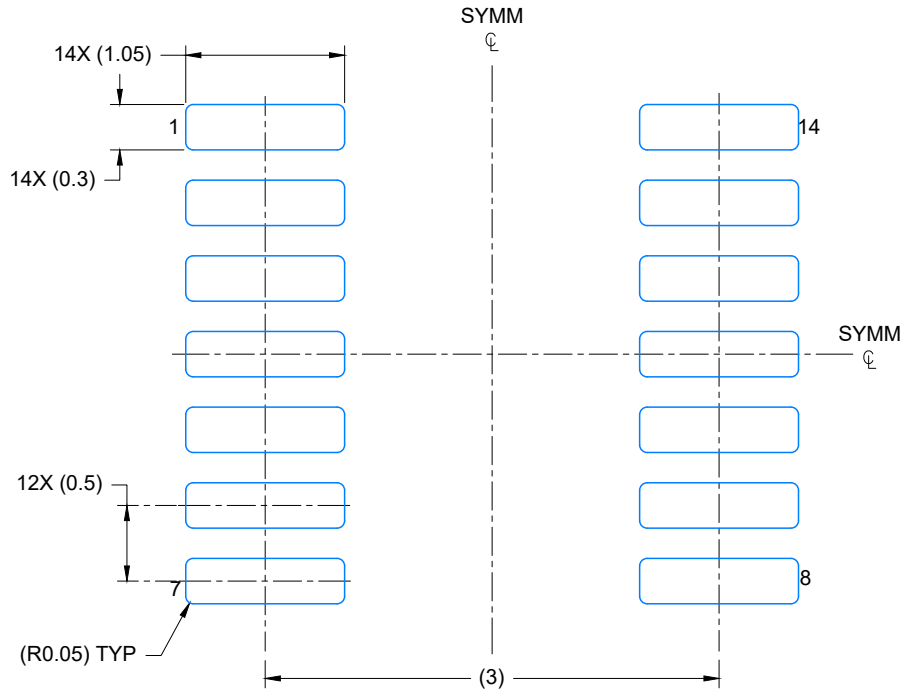
## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

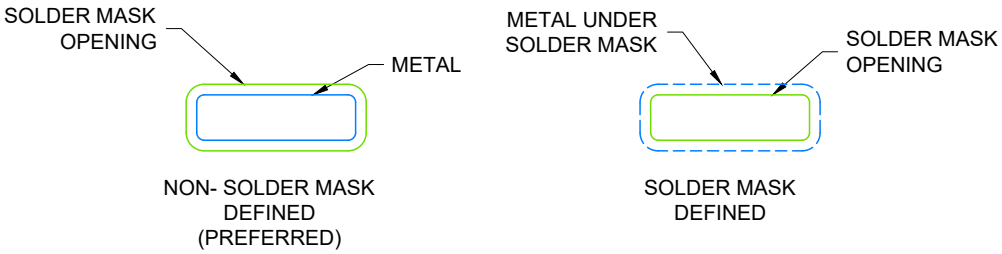



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

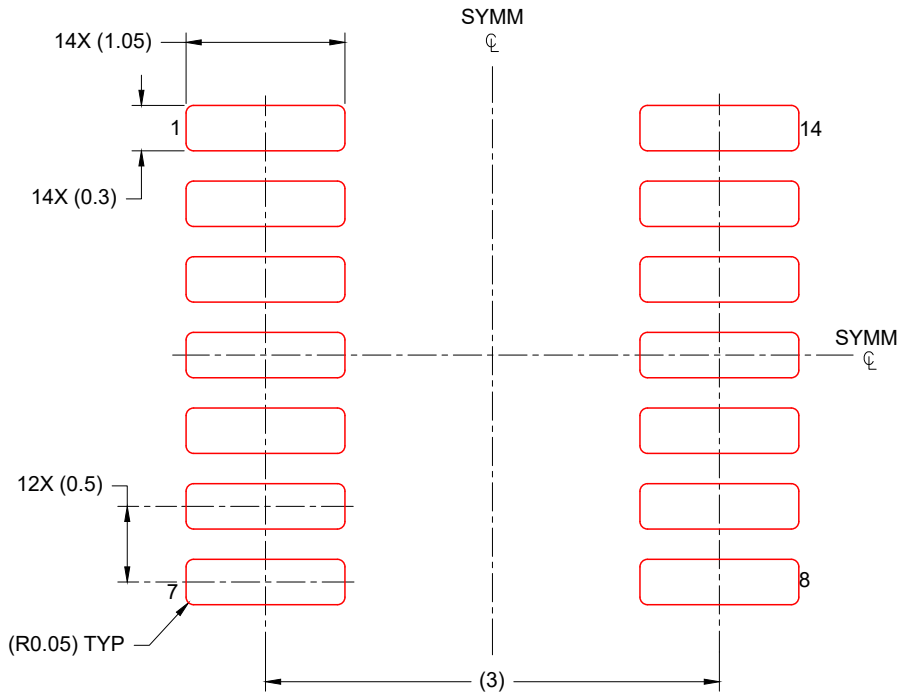



SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

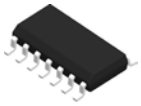



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

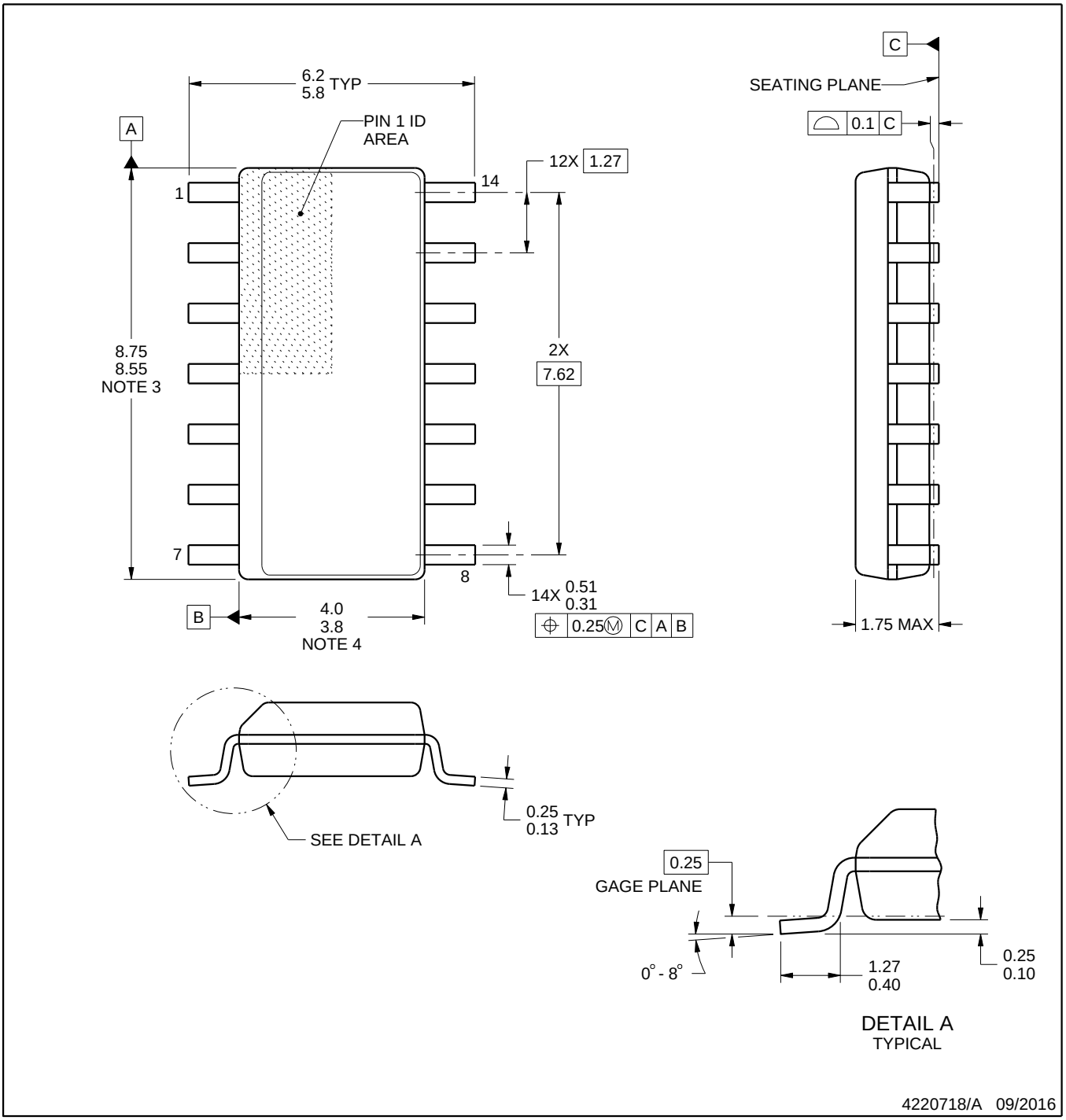


# PACKAGE OUTLINE

## D0014A

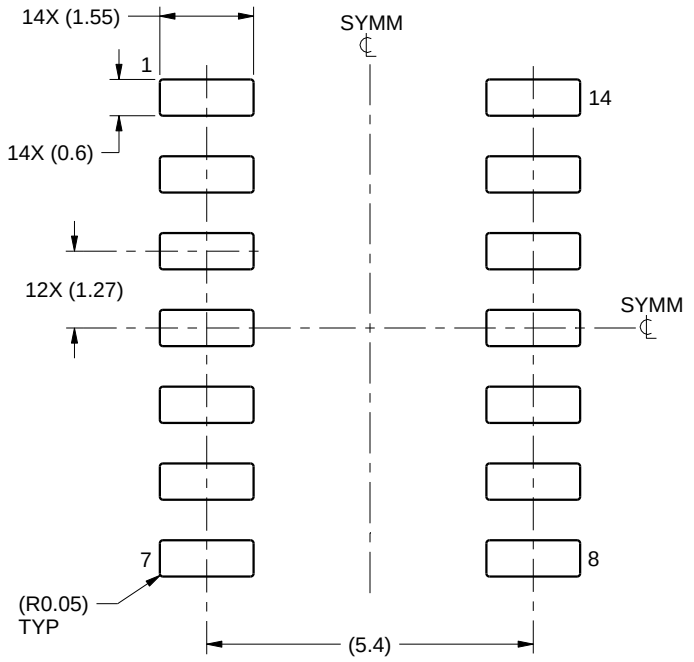
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

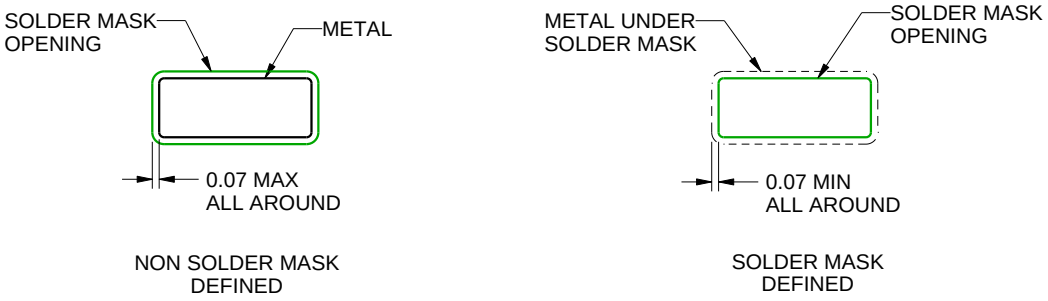



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

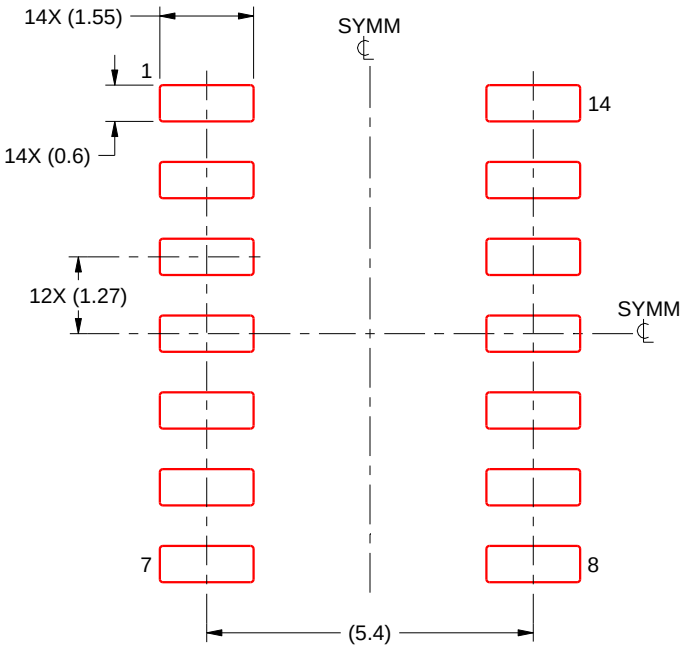
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

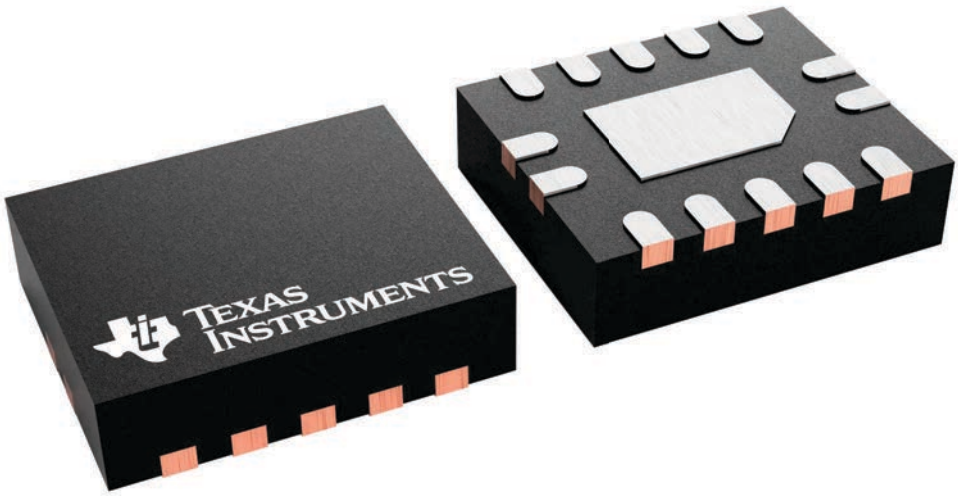
## BQA 14

## WQFN - 0.8 mm max height

**2.5 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

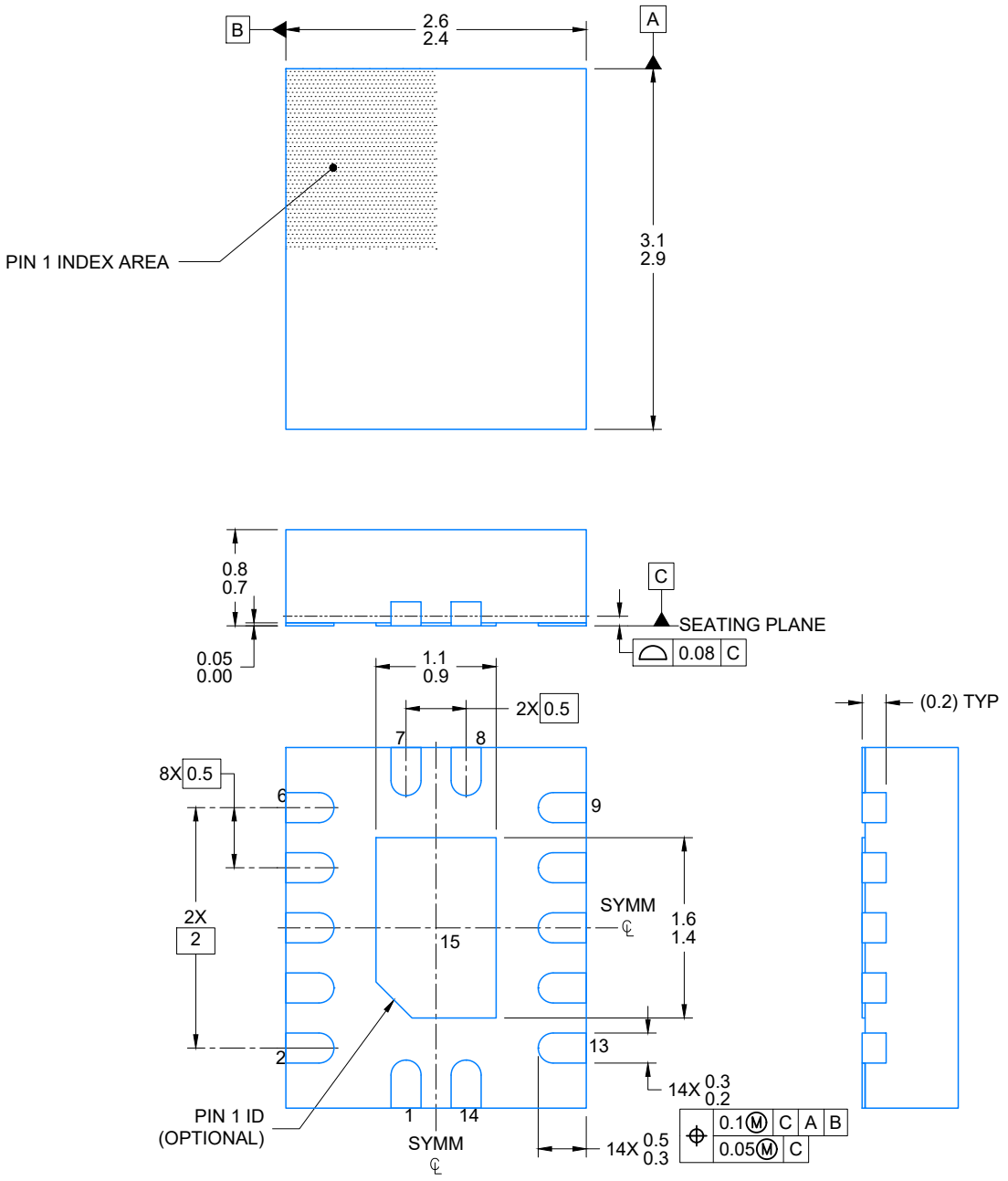


# PACKAGE OUTLINE

## BQA0014A

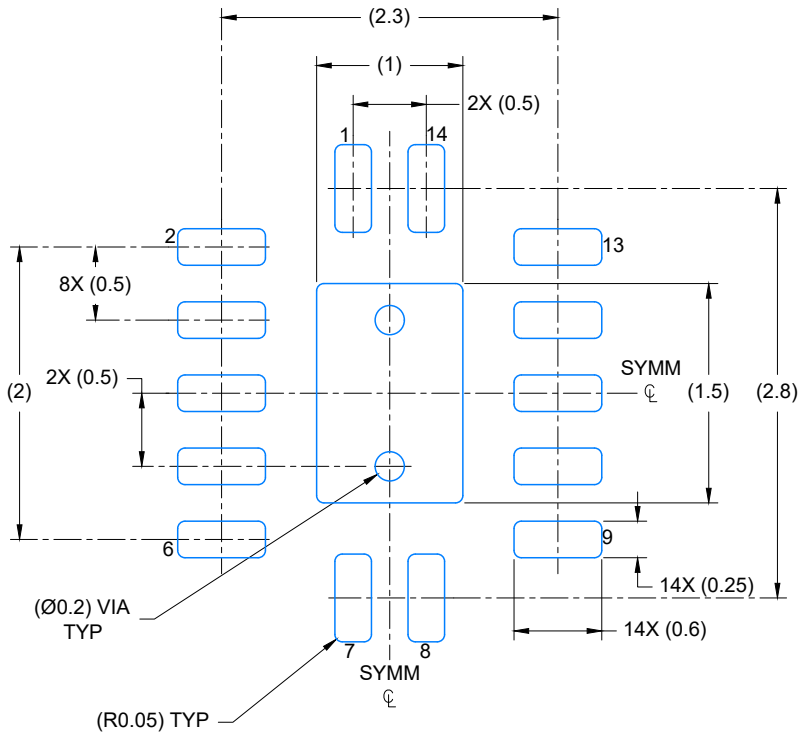
### WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

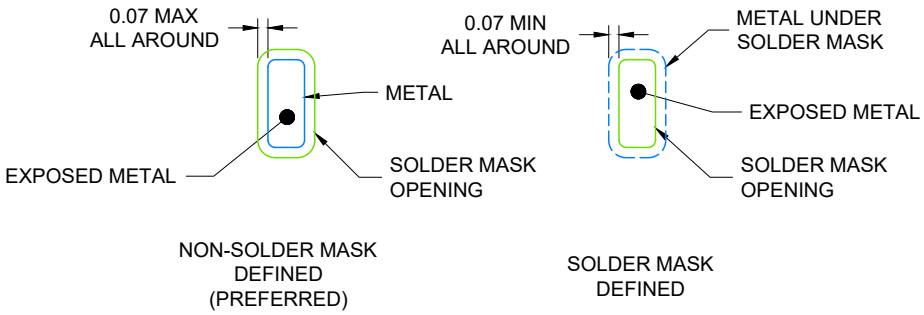



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



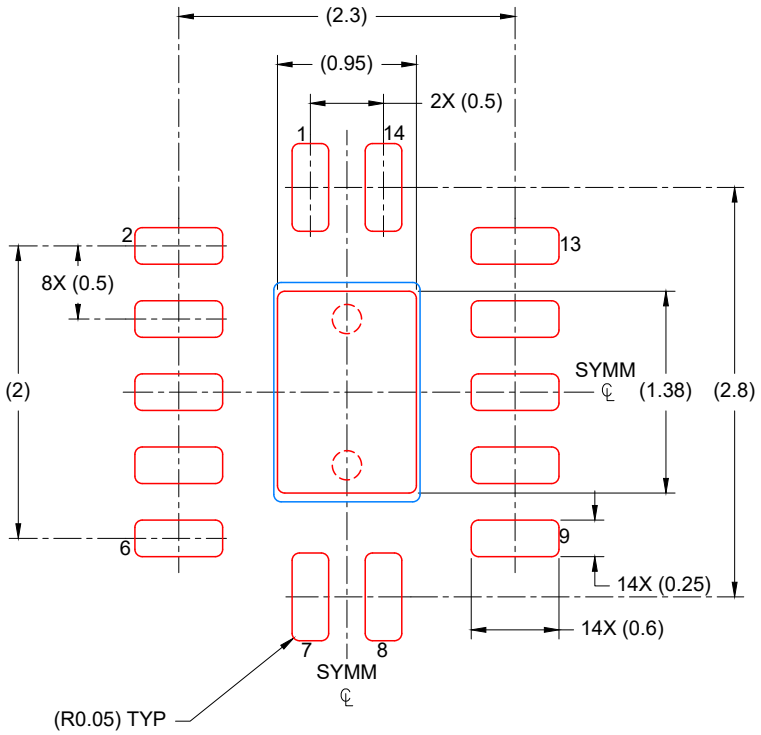

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

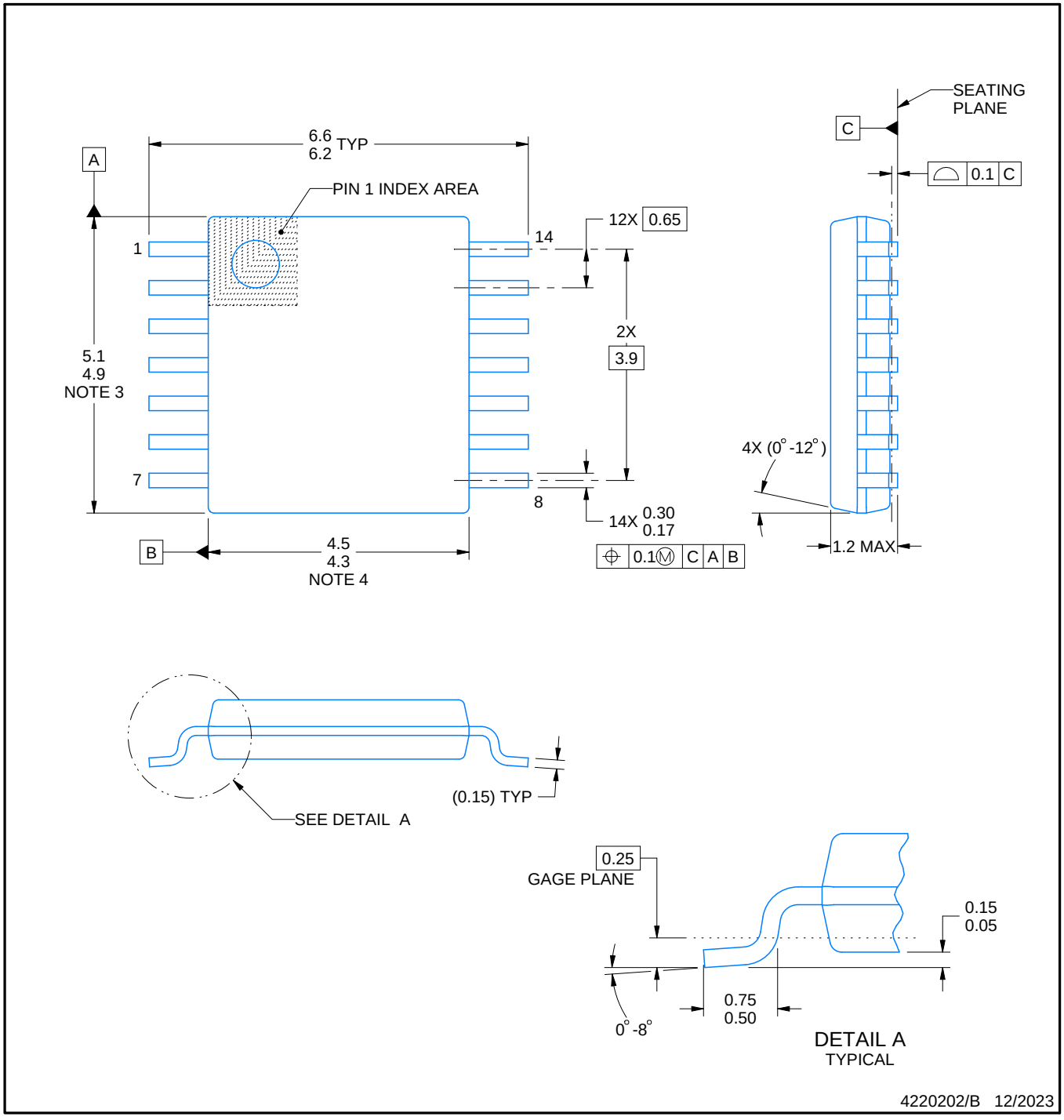
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## PW0014A

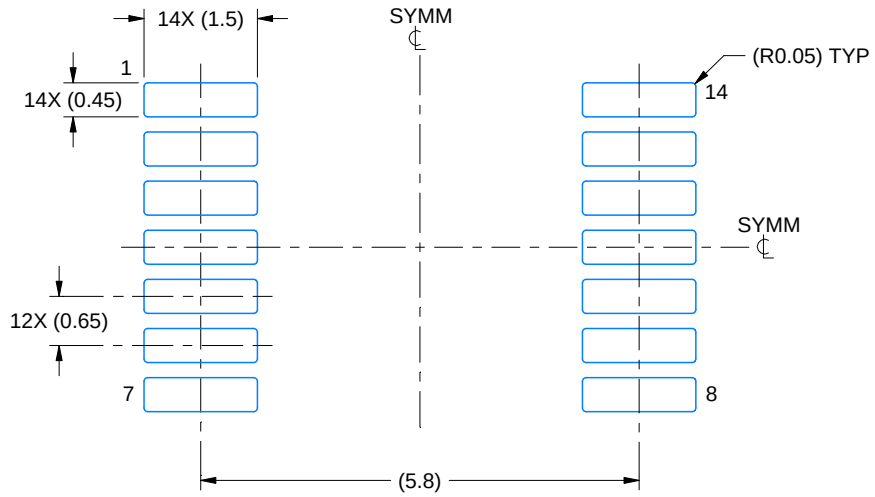
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

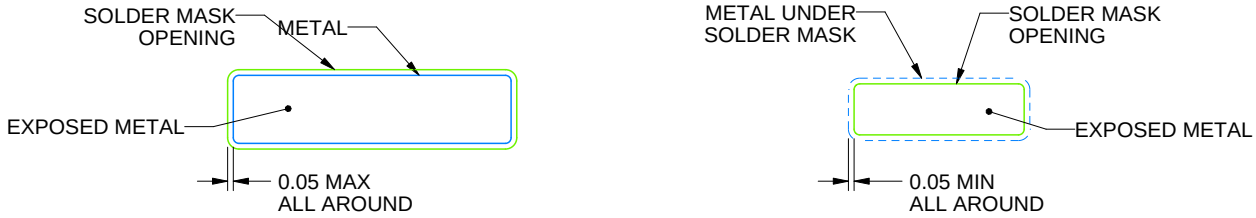



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

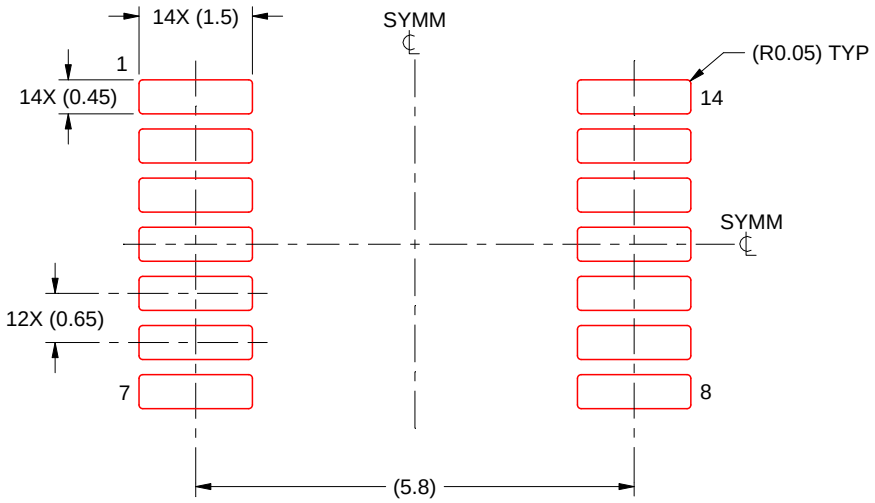



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月