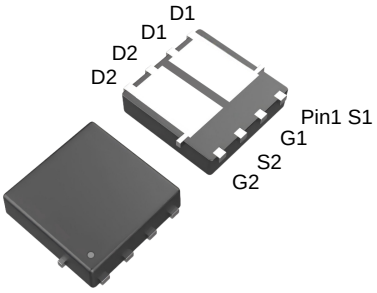
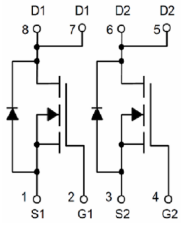
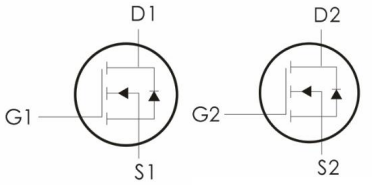
Description：

This Dual N-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.







Features：

1) V_{DS}=40V,I_D=22A,$R_{DS(ON)}$<17mΩ @V_{GS}=10V（Typ：13.5mΩ）
2) Low gate charge.
3) Green device available.
4) Advanced high cell denity trench technology for ultra low $R_{DS(ON)}$.
5) Excellent package for good heat dissipation.
6) MSL3

Package Marking and Ordering Information：

Part NO.	Marking	Package	Packing
DOZ22DN04	22DN04	DFN3*3-8D	5000 pcs/Reel

Absolute Maximum Ratings：（T_c=25℃ unless otherwise noted）

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current [1]	22	A
	Continuous Drain Current-T_c=100℃ [1]	15	
I_{DM}	Pulsed Drain Current[2]	88	
P_D	Power Dissipation	20	W
E_{AS}	Single pulse avalanche energy [3]	26	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55-+150	℃

Thermal Characteristics：

Symbol	Parameter	Max	Units
$R_{\theta JC}$	Thermal Resistance,Junction to Case	4.8	℃/W

Electrical Characteristics: (T_c=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=0V,I_D=250μA	40	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=40V	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0A	---	---	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=250μA	1	1.6	2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance[4]	V_{GS}=10V,I_D=4A	---	13.5	17	mΩ
		V_{GS}=4.5V,I_D=3A	---	18	28	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=20V, V_{GS}=0V, f=1MHz	---	1000	---	pF
C_{oss}	Output Capacitance		---	96	--	
C_{rss}	Reverse Transfer Capacitance		---	67.5	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=20V, R_L=1Ω, R_G=6Ω,V_{GS}=10V	---	10	---	ns
t_r	Rise Time		---	12	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	35	---	ns
t_f	Fall Time		---	8	---	ns
Q_g	Total Gate Charge	V_{GS}=8V, V_{DS}=20V, I_D=5A	---	20	---	nC
Q_{gs}	Gate-Source Charge		---	1.8	---	nC
Q_{gd}	Gate-Drain “Miller” Charge		---	2.2	---	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_{SD}=8A	---	---	1.2	V
I_S	Continuous Drain Curren	V_D=V_G=0V	---	---	22	A
I_{SM}	Pulsed Drain Current		---	---	76	A

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : TJ=25℃,VDD=20V,V_G=10V,L=0.5mH
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Characteristics: (T_c=25℃ unless otherwise noted)

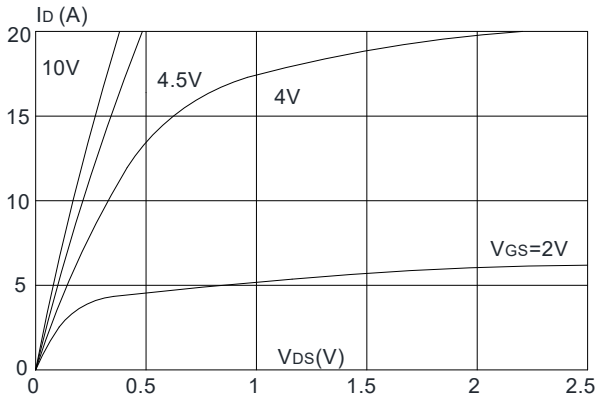


Figure1: Output Characteristics

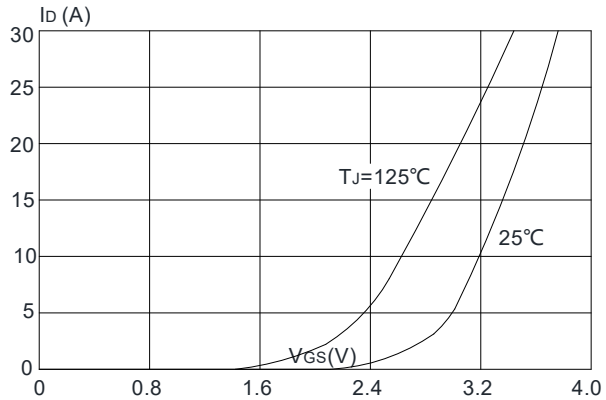


Figure 2: Typical Transfer Characteristics

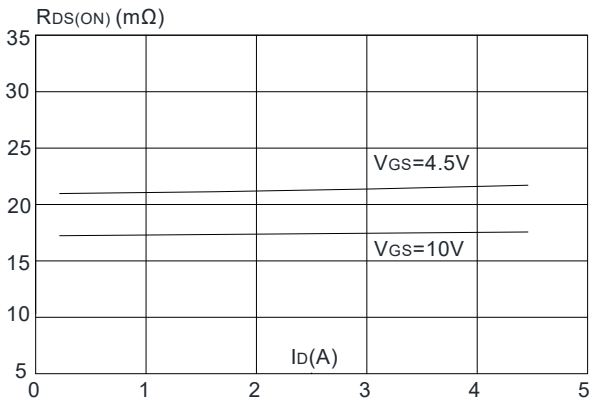


Figure 3: On-resistance vs. Drain Current

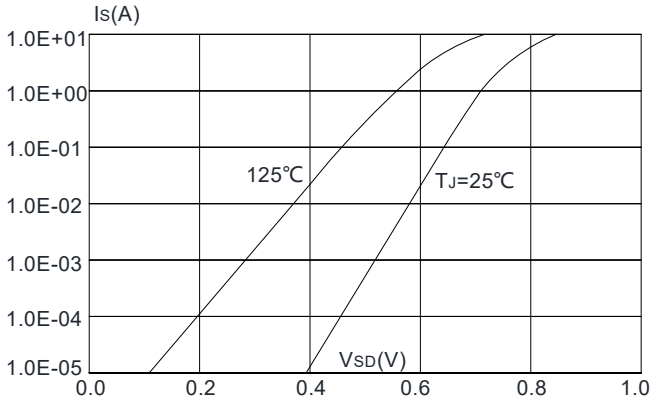


Figure 4: Body Diode Characteristics

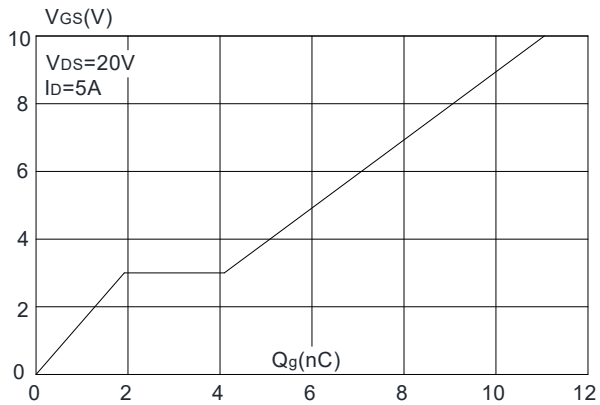


Figure 5: Gate Charge Characteristics

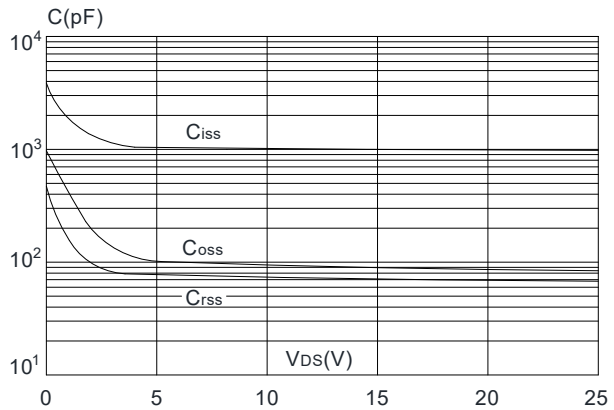


Figure 6: Capacitance Characteristics

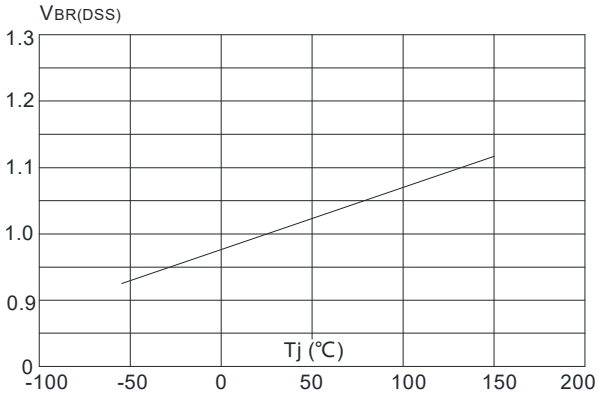


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

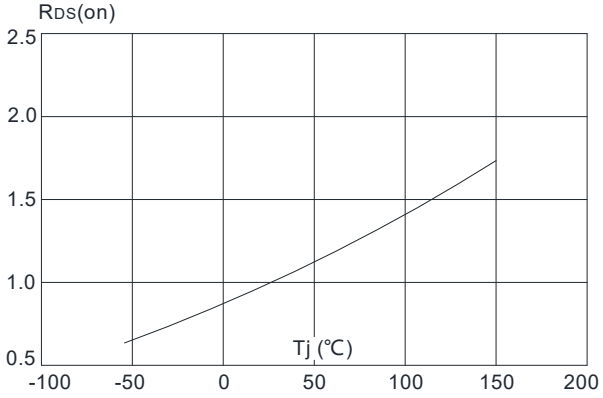


Figure 8: Normalized on Resistance vs. Junction Temperature

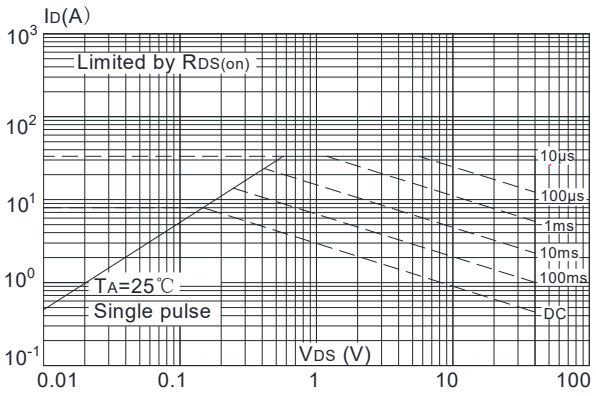


Figure 9: Maximum Safe Operating Area

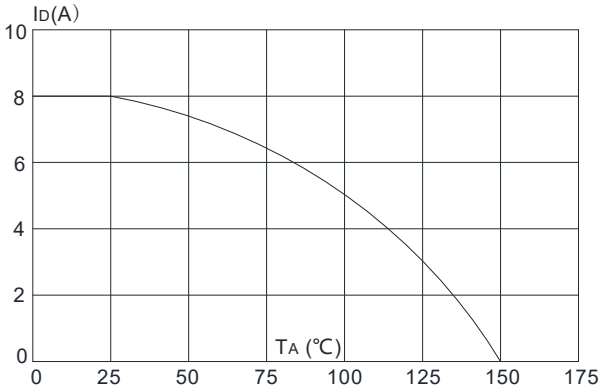


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

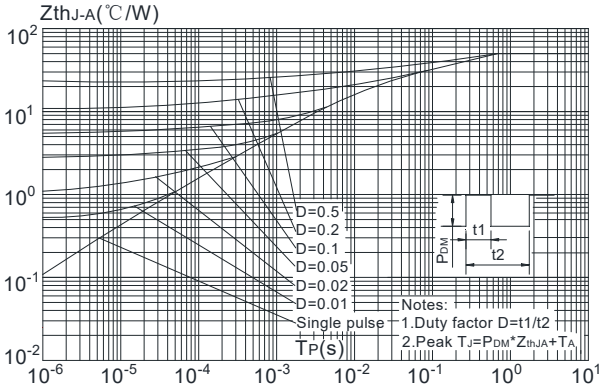
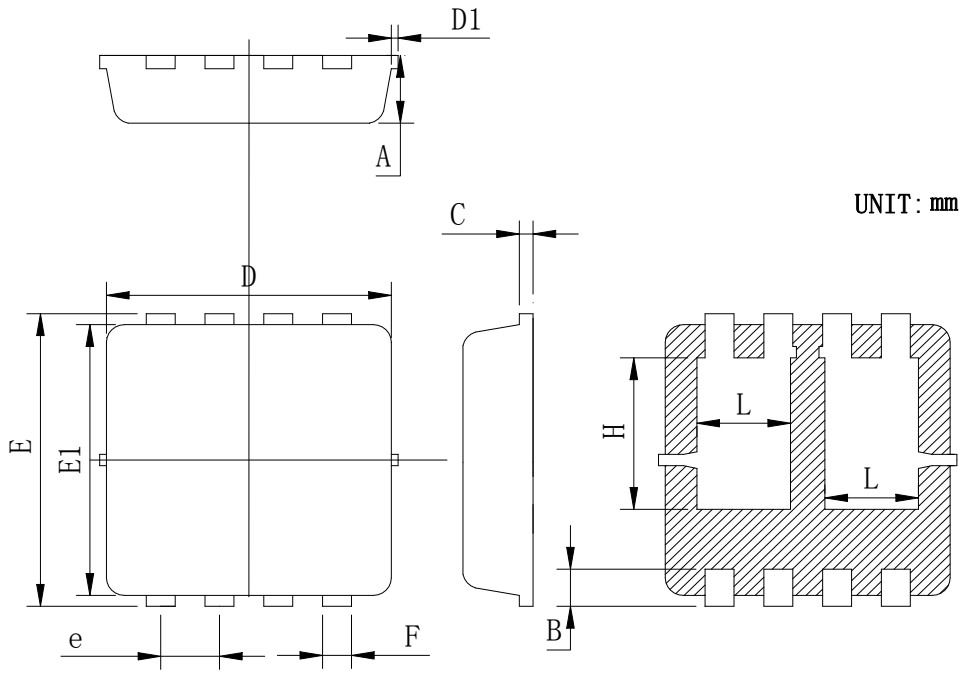


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

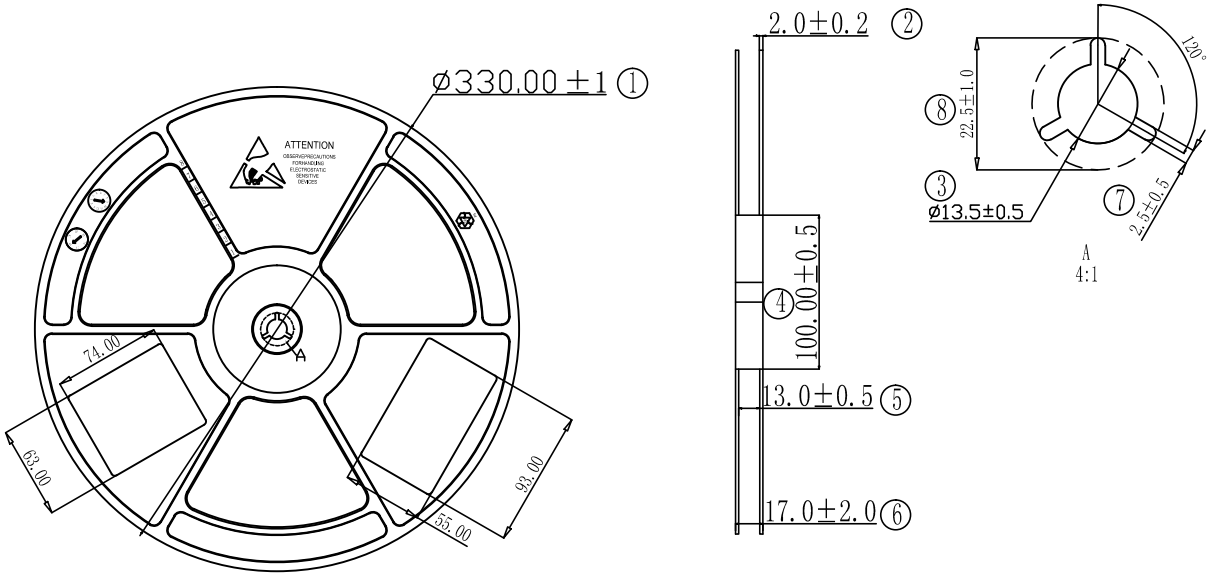
DFN3X3-8D Package Outline Data



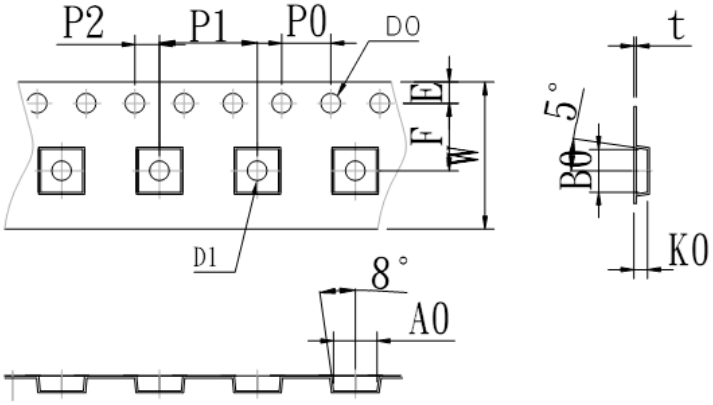
Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	0.93	1.03	1.13

Tape & Reel Information

Dimensions in mm



Symbol	A0	B0	K0	D0	D1	P0	P1	10*P0
Spec	3.55±0.10	3.45±0.10	1.13±0.10	1.55±0.10	1.55±0.10	4.00±0.10	8.00±0.10	40.0±0.10
Symbol	W	E	F	P2	t			
Spec	12.00±0.10	1.75±0.10	5.50±0.10	2.00±0.10	0.20±0.05			



Pulling direction →

Marking Information：

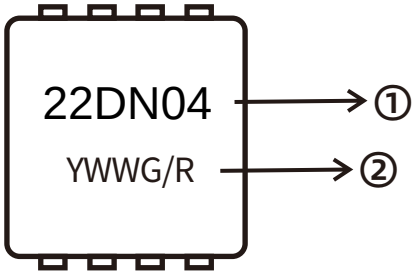
①: Part NO.

②: Date Code (YWWG / R)

Y: Year Code , last digit of the year

WW : Week Code (01-53)

G/R: G(Green) /R(Lead Free)



Previous Version

Version	Date	Subjects (major changes since last revision)
1.0	2025-05-18	Release of final version

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