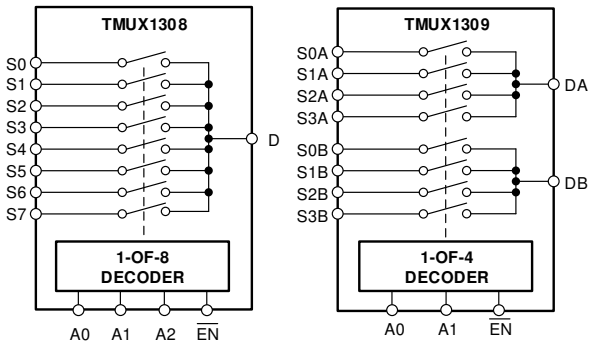
具有注入电流控制功能的 TMUX13xx 5V 双向 8:1 单通道和 4:1 双通道多路复用器

1 特性

- 注入电流控制
- 反向供电保护
  - 无到 V_{DD} 的 ESD 二极管路径
- 宽电源电压范围：1.62V 至 5.5V
- 低电容
- 双向信号路径
- 轨到轨运行
- 兼容 1.8V 逻辑电平
- 失效防护逻辑
- 先断后合开关
- 提供功能安全型
  - 可提供用于功能安全系统设计的文档
- TMUX1308 - 与以下器件引脚兼容：
  - 业界通用的 4051 和 4851 多路复用器
- TMUX1309 - 与以下器件引脚兼容：
  - 业界通用的 4052 和 4852 多路复用器

2 应用

- 模拟和数字多路复用和多路信号分离
- 诊断和监控
- 数据中心交换机
- 远程无线电单元 (RRU)
- 机架式服务器
- 电表
- 电器
- 空调机
- 多功能打印机
- 串式逆变器
- IP 网络摄像头
- 点钞机
- 非公路用车控制系统



TMUX1308 和 TMUX1309 方框图

3 说明

TMUX1308 和 TMUX1309 为通用互补金属氧化物半导体 (CMOS) 多路复用器 (MUX)。TMUX1308 是 8:1 单通道（单端）多路复用器，而 TMUX1309 是 4:1 双通道（差分）多路复用器。这些器件可在源极 (Sx) 和漏极 (Dx) 引脚上支持从 GND 到 V_{DD} 范围的双向模拟和数字信号。

TMUX13xx 器件具有内部注入电流控制功能，从而无需外部二极管和电阻器网络（通常用于保护开关并使输入信号保持在电源电压范围之内）。内部注入电流控制电路允许禁用信号路径上的信号超过电源电压，而不会影响启用信号路径的信号。此外，TMUX13xx 器件没有到电源引脚的内部二极管路径，从而消除了损坏连接到电源引脚的元件或为电源轨提供意外电源的风险。

所有逻辑输入均具有兼容 1.8 V 逻辑的阈值，在有效电源电压下运行时，这些阈值可确保 TTL 和 CMOS 逻辑兼容性。失效防护逻辑电路允许先在控制引脚上施加电压，然后在电源引脚上施加电压，从而保护器件免受潜在的损害。

封装信息(1)(2)

器件型号	封装	封装尺寸（标称值）
TMUX1308 TMUX1309	PW（TSSOP，16）	5.00mm × 4.40mm
	DYY（SOT-23-THIN，16）	4.20mm × 2.00mm
	BQB（WQFN，16）	3.50mm × 2.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。
(2) 请参阅*器件比较表*。

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Revision History 2
5 Device Comparison Table 3
6 Pin Configuration and Functions 3
7 Specifications 7
7.1 Absolute Maximum Ratings 7
7.2 ESD Ratings 7
7.3 Recommended Operating Conditions 7
7.4 Thermal Information: TMUX1308 8
7.5 Thermal Information: TMUX1309 8
7.6 Electrical Characteristics 9
7.7 Logic and Dynamic Characteristics 10
7.8 Timing Characteristics 11
7.9 Injection Current Coupling 12
7.10 Typical Characteristics 13
8 Parameter Measurement Information 16
8.1 On-Resistance 16
8.2 Off-Leakage Current 16
8.3 On-Leakage Current 17
8.4 Transition Time 17
8.5 Break-Before-Make 18
8.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$ 18
8.7 Charge Injection 19
8.8 Off Isolation 19
8.9 Crosstalk 20
8.10 Bandwidth 20
8.11 Injection Current Control 21
9 Detailed Description 22
9.1 Overview 22
9.2 Functional Block Diagram 22
9.3 Feature Description 22
9.4 Device Functional Modes 26
9.5 Truth Tables 26
10 Application and Implementation 28
10.1 Application Information 28
10.2 Typical Application 28
10.3 Design Requirements 29
10.4 Detailed Design Procedure 29
11 Power Supply Recommendations 29
12 Layout 29
12.1 Layout Guidelines 29
12.2 Layout Example 30
13 Device and Documentation Support 31
13.1 Documentation Support 31
13.2 Receiving Notification of Documentation Updates 31
13.3 支持资源 31
13.4 Trademarks 31
13.5 Electrostatic Discharge Caution 31
13.6 术语表 31
14 Mechanical, Packaging, and Orderable Information 31

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (November 2020) to Revision E (October 2022)	Page
• Updated the *Injection Current Control* section	23

Changes from Revision C (August 2020) to Revision D (November 2020)	Page
• 将 TMUX1309 器件的状态从预发布更改为量产	1
• Changed ΔR_{ON} test condition to V_{DD} / 2	9
• Changed max ΔR_{ON} spec limit for 1.8 V and 2.5 V supply	9

Changes from Revision B (August 2020) to Revision C (August 2020)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Added the Typical Characteristics	13

Changes from Revision A (June 2020) to Revision B (August 2020)	Page
• Added thermal information for TMUX1309	8

Changes from Revision * (March 2020) to Revision A (June 2020)	Page

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5 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX1308	8:1, 1-channel, single-ended multiplexer
TMUX1309	4:1, 2-channel, differential multiplexer

6 Pin Configuration and Functions

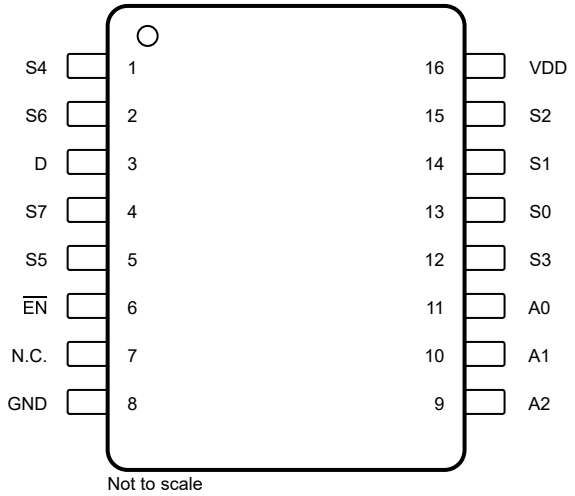

图 6-1. TMUX1308: PW Package, 16-Pin TSSOP (Top View)

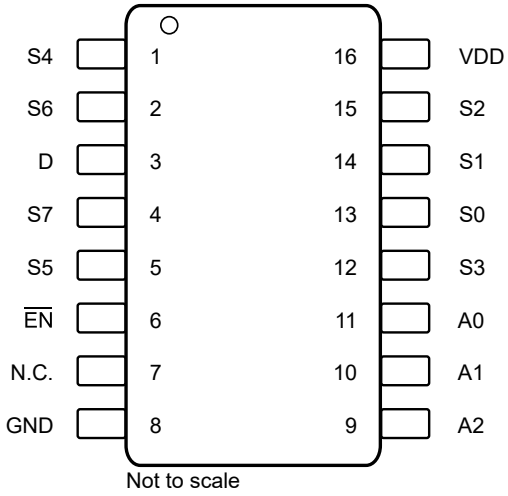

图 6-2. TMUX1308: DYY Package, 16-Pin SOT-23-THIN (Top View)

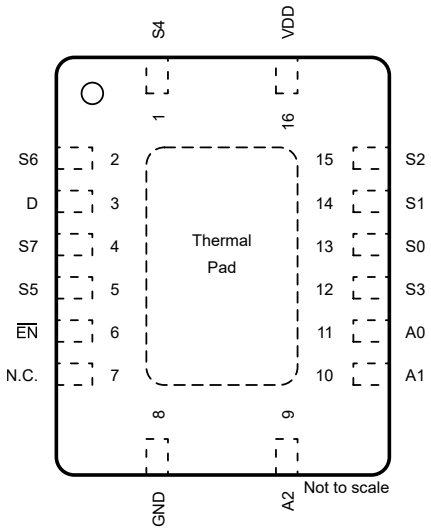

图 6-3. TMUX1308: BQB Package, 16-Pin WQFN (Top View)

表 6-1. Pin Functions TMUX1308

PIN		TYPE[1]	DESCRIPTION[2]
NAME	NO.		
S4	1	I/O	Source pin 4. Signal path can be an input or output.
S6	2	I/O	Source pin 6. Signal path can be an input or output.
D	3	I/O	Drain pin (common). Signal path can be an input or output.
S7	4	I/O	Source pin 7. Signal path can be an input or output.
S5	5	I/O	Source pin 5. Signal path can be an input or output.
$\overline{EN}$	6	I	Active low logic input. When this pin is high, all switches are turned off. When this pin is low, the A[2:0] address inputs determine which switch is turned on as listed in 表 9-1.
N.C.	7	Not Connected	Not internally connected.
GND	8	P	Ground (0 V) reference
A2	9	I	Address line 2. Controls the switch configuration as listed in 表 9-1.
A1	10	I	Address line 1. Controls the switch configuration as listed in 表 9-1.
A0	11	I	Address line 0. Controls the switch configuration as listed in 表 9-1.
S3	12	I/O	Source pin 3. Signal path can be an input or output.
S0	13	I/O	Source pin 0. Signal path can be an input or output.
S1	14	I/O	Source pin 1. Signal path can be an input or output.
S2	15	I/O	Source pin 2. Signal path can be an input or output.
VDD	16	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
Thermal pad		—	Exposed thermal pad with conductive die attached. No requirement to solder this pad. If connected, then it should be left floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power.
(2) For what to do with unused pins, refer to 节 9.4.

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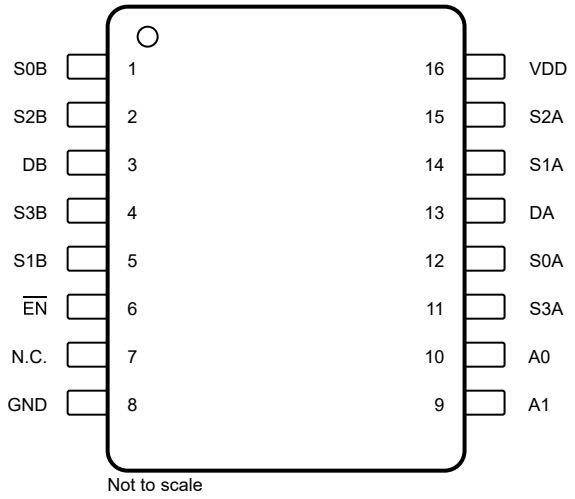

图 6-4. TMUX1309: PW Package, 16-Pin TSSOP (Top View)

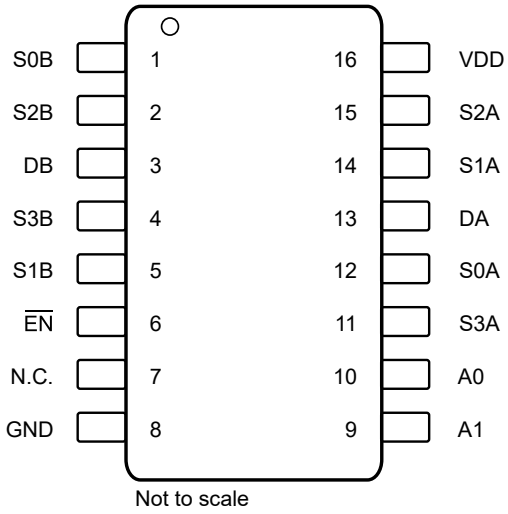

图 6-5. TMUX1309: DYY Package, 16-Pin SOT-23-THIN (Top View)

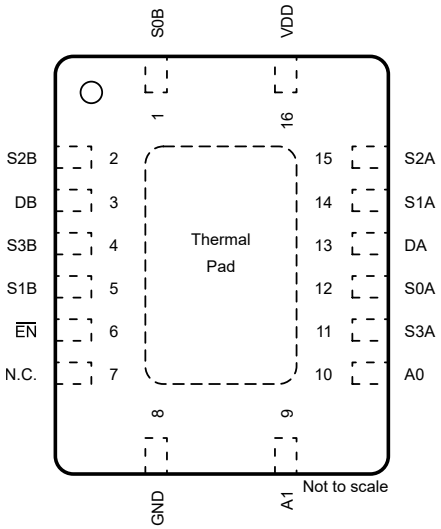

图 6-6. TMUX1309: BQB Package, 16-Pin WQFN (Top View)

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表 6-2. Pin Functions TMUX1309

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
S0B	1	I/O	Source pin 0 of mux B. Can be an input or output.
S2B	2	I/O	Source pin 2 of mux B. Can be an input or output.
DB	3	I/O	Drain pin (Common) of mux B. Can be an input or output.
S3B	4	I/O	Source pin 3 of mux B. Can be an input or output.
S1B	5	I/O	Source pin 1 of mux B. Can be an input or output.
$\overline{EN}$	6	I	Active low logic input. When this pin is high, all switches are turned off. When this pin is low, the A[1:0] address inputs determine which switch is turned on.
N.C.	7	Not Connected	Not internally connected.
GND	8	P	Ground (0 V) reference
A1	9	I	Address line 1. Controls the switch configuration as listed in 表 9-2.
A0	10	I	Address line 0. Controls the switch configuration as listed in 表 9-2.
S3A	11	I/O	Source pin 3 of mux A. Can be an input or output.
S0A	12	I/O	Source pin 0 of mux A. Can be an input or output.
DA	13	I/O	Drain pin (Common) of mux A. Can be an input or output.
S1A	14	I/O	Source pin 1 of mux A. Can be an input or output.
S2A	15	I/O	Source pin 2 of mux A. Can be an input or output.
VDD	16	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
Thermal pad		—	Exposed thermal pad with conductive die attached. No requirement to solder this pad. If connected, then it should be left floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power.
(2) For what to do with unused pins, refer to 节 9.4.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	– 0.5	6	V
V_{SEL} or V_{EN}	Logic control input pin voltage ($\overline{EN}$, A0, A1, A2)	– 0.5	6	
V_S or V_D	Source or drain voltage (Sx, D)	– 0.5	V_{DD}+0.5	
I_{SEL} or I_{EN}	Logic control input pin current ($\overline{EN}$, A0, A1, A2)	– 30	30	mA
I_S or $I_{D\ (CONT)}$	Continuous current through switch (Sx, D pins) – 40°C to +85°C	– 50	50	
I_S or $I_{D\ (CONT)}$	Continuous current through switch (Sx, D pins) – 40°C to +125°C	– 25	25	
I_{GND}	Continuous current through GND	– 100	100	
P_{tot}	Total power dissipation(4)		500	mW
T_{stg}	Storage temperature	– 65	150	°C
T_J	Junction temperature		150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) For TSSOP package: P_{tot} derates linearly above T_A = 80°C by 7.2mW/°C.
For SOT-23-THIN package: P_{tot} derates linearly above T_A = 66°C by 6mW/°C.
For BQB package: P_{tot} derates linearly above T_A = 102°C by 10.6mW/°C.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.62		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	0		V_{DD}	V
V_{SEL} or V_{EN}	Logic control input pin voltage ($\overline{EN}$, A0, A1, A2)	0		5.5	V
I_S or $I_{D\ (CONT)}$	Continuous current through switch (Sx, D pins) – 40°C to +85°C	– 50		50	mA
I_S or $I_{D\ (CONT)}$	Continuous current through switch (Sx, D pins) – 40°C to +125°C	– 25		25	mA
I_{OK}	Current per input into source or drain pins when singal voltage exceeds recommended operating voltage (1)	– 50		50	mA
I_{INJ}	Injected current into single off switch input	– 50		50	mA
I_{INJ_ALL}	Total injected current into all off switch inputs combined	– 100		100	mA
T_A	Ambient temperature	– 40		125	°C

(1) If source or drain voltage exceeds VDD, or goes below GND, the pin will be shunted to GND through an internal FET, the current must be limited within the specified value. If $V_{signal} > V_{DD}$ or if $V_{signal} <$ GND.

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7.4 Thermal Information: TMUX1308

THERMAL METRIC[1]		TMUX1308			UNIT
		PW (TSSOP)	DYY (SOT)	BQB (WQFN)	
		PINS	PINS	PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	139.6	167.1	94.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.2	106.3	92.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.2	90.0	64.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	26.5	17.2	13.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	83.8	90.0	64.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	42.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Thermal Information: TMUX1309

THERMAL METRIC[1]		TMUX1309			UNIT
		PW (TSSOP)	DYY (SOT)	BQB (WQFN)	
		PINS	PINS	PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance thermal information for TMUX1309	139.6	172.4	94.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.2	107.0	92.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.2	96.1	64.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	26.5	19.7	13.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	83.8	95.9	64.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	42.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.6 Electrical Characteristics

At specified V_{DD} ±10%
Typical values measured at nominal V_{DD}

PARAMETER		TEST CONDITIONS	V_{DD}	Operating free-air temperature (T_A)									UNIT
				25°C			– 40°C to 85°C			– 40°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH													
R_{ON}	On-state switch resistance	V_S = 0 V to V_{DD} I_{SD} = 0.5 mA	1.8 V		650	1500			1700			1700	Ω
			2.5 V		230	600			670			670	
			3.3 V		120	330			350			370	
			5 V		75	195			220			270	
ΔR_{ON}	On-state switch resistance matching between inputs	V_S = V_{DD} / 2 I_{SD} = 0.5 mA	1.8 V		10	38			45			45	Ω
			2.5 V		3	20			22			22	
			3.3 V		2	8			11			15	
			5 V		1	7			10			14	
$I_{S(OFF)}$	Source off-state leakage current	Switch Off V_D = 0.8 x V_{DD}/ 0.2 x V_{DD} V_S = 0.2 x V_{DD}/ 0.8 x V_{DD}	1.8 V		±1		– 25		25	– 800		800	nA
			2.5 V		±1		– 25		25	– 800		800	
			3.3 V		±1		– 25		25	– 800		800	
			5 V		±1		– 25		25	– 800		800	
$I_{D(OFF)}$	Drain off-state leakage current (common drain pin)	Switch Off V_D = 0.8 x V_{DD}/ 0.2 x V_{DD} V_S = 0.2 x V_{DD}/ 0.8 x V_{DD}	1.8 V		±1		– 45		45	– 800		800	nA
			2.5 V		±1		– 45		45	– 800		800	
			3.3 V		±1		– 45		45	– 800		800	
			5 V		±1		– 45		45	– 800		800	
$I_{D(ON)}$ $I_{S(ON)}$	Channel on-state leakage current	Switch On V_D = V_S = 0.8 x V_{DD} or V_D = V_S = 0.2 x V_{DD}	1.8 V		±1		– 45		45	– 800		800	nA
			2.5 V		±1		– 45		45	– 800		800	
			3.3 V		±1		– 45		45	– 800		800	
			5 V		±1		– 45		45	– 800		800	
C_{SOFF}	Source off capacitance	V_S = V_{DD} / 2 f = 1 MHz	1.8 V		2	14			14			14	pF
			2.5 V		2	14			14			14	
			3.3 V		2	14			14			14	
			5 V		2	14			14			14	
C_{DOFF}	Drain off capacitance	V_S = V_{DD} / 2 f = 1 MHz	1.8 V		7	37			37			37	pF
			2.5 V		7	37			37			37	
			3.3 V		7	37			37			37	
			5 V		7	37			37			37	
C_{SON} C_{DON}	On capacitance	V_S = V_{DD} / 2 f = 1 MHz	1.8 V		11	40			40			40	pF
			2.5 V		11	40			40			40	
			3.3 V		11	40			40			40	
			5 V		11	40			40			40	
POWER SUPPLY													
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or V_{DD}	1.8 V			1			1			1.2	µA
			2.5 V			1			1			1.5	
			3.3 V			1			1			2	
			5 V			1			1.5			3	

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7.7 Logic and Dynamic Characteristics

At specified V_{DD} ±10%
Typical values measured at nominal V_{DD} and T_A = 25°C.

PARAMETER		TEST CONDITIONS	V_{DD}	Operating free-air temperature (T_A) – 40°C to 125°C			UNIT
				MIN	TYP	MAX	
LOGIC INPUTS ($\overline{EN}$, A0, A1, A2)							
V_{IH}	Input logic high		1.8 V	0.95		5.5	V
			2.5 V	1.1		5.5	
			3.3 V	1.15		5.5	
			5 V	1.25		5.5	
V_{IL}	Input logic low		1.8 V	0		0.6	V
			2.5 V	0		0.7	
			3.3 V	0		0.8	
			5 V	0		0.95	
I_{IH}	Logic high input leakage current	V_{LOGIC} = 1.8 V or V_{DD}	All			1	uA
I_{IL}	Logic low input leakage current	V_{LOGIC} = 0 V	All	–1			uA
C_{IN}	Logic input capacitance	V_{LOGIC} = 0 V, 1.8 V, V_{DD} f = 1 MHz	All		1	2	pF
DYNAMIC CHARACTERISTICS							
Q_{INJ}	Charge Injection	V_S = V_{DD} / 2 R_S = 0 Ω, C_L = 100 pF	1.8 V		–0.5		pC
			2.5 V		–0.5		
			3.3 V		–1		
			5 V		–6.5		
O_{ISO}	Off Isolation	V_{BIAS} = V_{DD} / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 100 kHz	1.8 V		–110		dB
			2.5 V		–110		
			3.3 V		–110		
			5 V		–110		
O_{ISO}	Off Isolation	V_{BIAS} = V_{DD} / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 1 MHz	1.8 V		–90		dB
			2.5 V		–90		
			3.3 V		–90		
			5 V		–90		
X_{TALK}	Crosstalk	V_{BIAS} = V_{DD} / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 100 kHz	1.8 V		–110		dB
			2.5 V		–110		
			3.3 V		–110		
			5 V		–110		
X_{TALK}	Crosstalk	V_{BIAS} = V_{DD} / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 1 MHz	1.8 V		–90		dB
			2.5 V		–90		
			3.3 V		–90		
			5 V		–90		
BW	Bandwidth	V_{BIAS} = V_{DD} / 2 V_S = 200 mVpp RL = 50 Ω, CL = 5 pF	1.8 V		350		MHz
			2.5 V		450		
			3.3 V		500		
			5 V		500		

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7.8 Timing Characteristics

At specified V_{DD} ±10%
Typical values measured at nominal V_{DD}.

PARAMETER		TEST CONDITIONS	V_{DD}	Operating free-air temperature (T_A)									UNIT
				25°C			–40°C to 85°C			–40°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS													
t_{PD}	Propagation delay	C_L = 50 pF Sx to D, D to Sx	1.8 V		15	30			30			30	ns
			2.5 V		8	15			20			20	
			3.3 V		5	11			15			15	
			5 V		4	9			10			10	
		CL = 15 pF	5 V		1.5	4			5			5	
t_{TRAN}	Transition-time between inputs	R_L = 10 kΩ, C_L = 50 pF Ax to D, Ax to Sx	1.8 V		44	94			103			103	ns
			2.5 V		30	63			67			67	
			3.3 V		23	51			54			54	
			5 V		18	43			46			46	
		R_L = 10 kΩ, C_L = 15 pF	5 V		15	39			43			43	
$t_{ON(EN)}$	Turnon-time from enable	R_L = 10 kΩ, C_L = 50 pF EN to D, EN to Sx	1.8 V		39	64			75			75	ns
			2.5 V		30	45			50			50	
			3.3 V		26	38			42			42	
			5 V		24	32			37			37	
		R_L = 10 kΩ, C_L = 15 pF	5 V		22	31			35			35	
$t_{OFF(EN)}$	Turnoff time from enable	R_L = 10 kΩ, C_L = 50 pF EN to D, EN to Sx	1.8 V		58	80			85			85	ns
			2.5 V		21	70			72			72	
			3.3 V		15	65			70			70	
			5 V		11	40			45			45	
		R_L = 10 kΩ, C_L = 15 pF	5 V		8	15			20			20	
t_{BBM}	Break before make time	R_L = 10 kΩ, C_L = 15 pF Sx to D, D to Sx	1.8 V	1	16		1			1			ns
			2.5 V	1	22		1			1			
			3.3 V	1	24		1			1			
			5 V	1	33		1			1			

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7.9 Injection Current Coupling

At specified V_{DD} ±10%
Typical values measured at nominal V_{DD} and T_A = 25°C.

PARAMETER		V_{DD}	TEST CONDITIONS		-40°C to 125°C			UNIT
					MIN	TYP	MAX	
INJECTION CURRENT COUPLING								
ΔV_{OUT}	Maximum shift of output voltage of enabled analog input	1.8 V	$R_S \leq$ 3.9 kΩ	$I_{INJ} \leq$ 1 mA		0.01	1	mV
		3.3 V				0.05	1	
		5 V				0.1	1	
		1.8 V	$R_S \leq$ 3.9 kΩ	$I_{INJ} \leq$ 10 mA		0.01	2	
		3.3 V				0.3	3	
		5 V				0.06	4	
		1.8 V	$R_S \leq$ 20 kΩ	$I_{INJ} \leq$ 1 mA		0.05	2	
		3.3 V				0.05	2	
		5 V				0.1	2	
		1.8 V	$R_S \leq$ 20 kΩ	$I_{INJ} \leq$ 10 mA		0.05	15	
		3.3 V				0.05	15	
		5 V				0.02	15	

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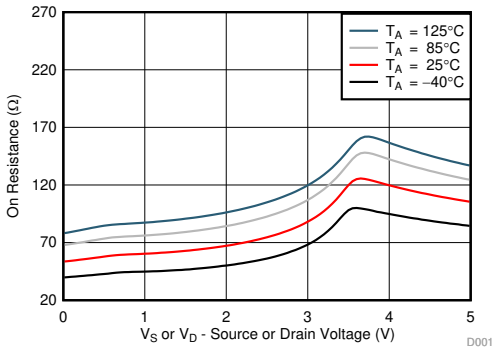
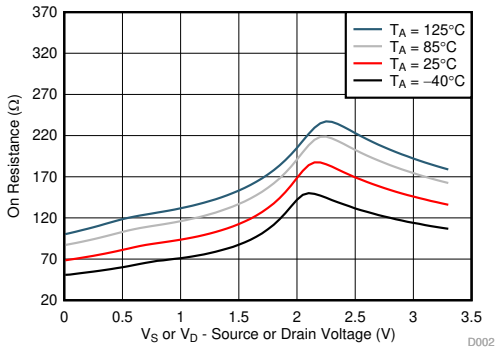
7.10 Typical Characteristics

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)



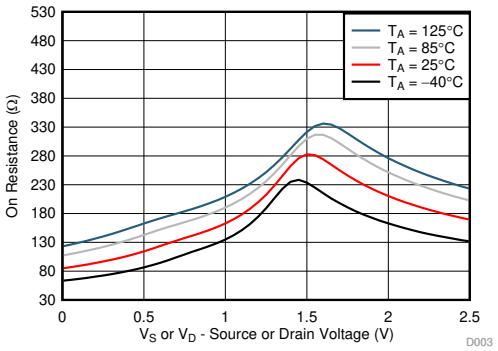
V_{DD} = 5 V

图 7-1. On-Resistance vs Temperature



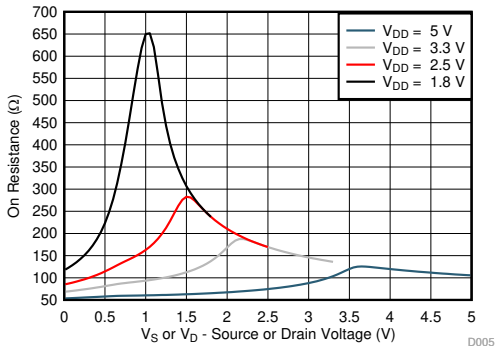
V_{DD} = 3.3 V

图 7-2. On-Resistance vs Temperature



V_{DD} = 2.5 V

图 7-3. On-Resistance vs Temperature



T_A = 25°C

图 7-4. On-Resistance vs Source or Drain Voltage

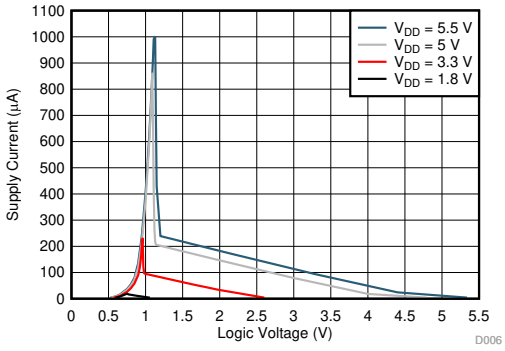
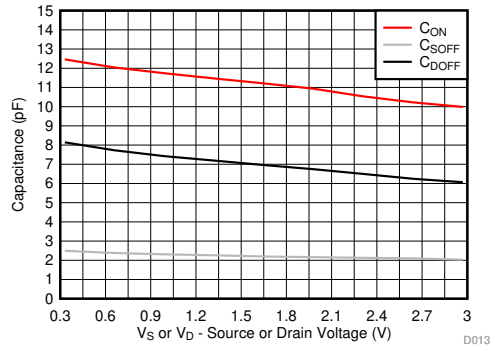


图 7-5. Supply Current vs Logic Voltage

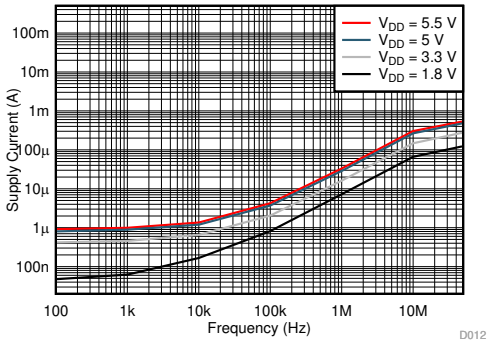


V_{DD} = 3.3 V

图 7-6. Capacitance vs Source Voltage

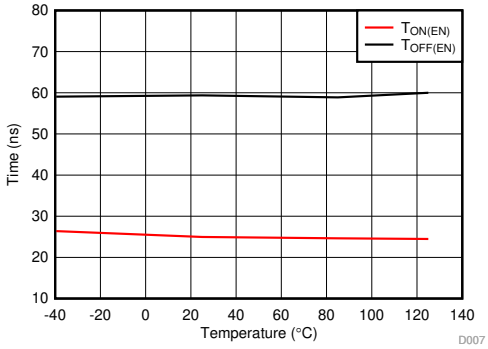
7.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)



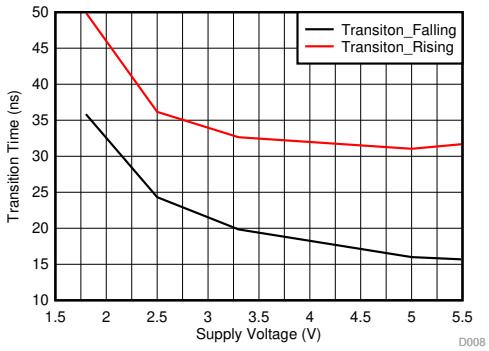
T_A = 25°C

图 7-7. Supply Current vs Input Switching Frequency



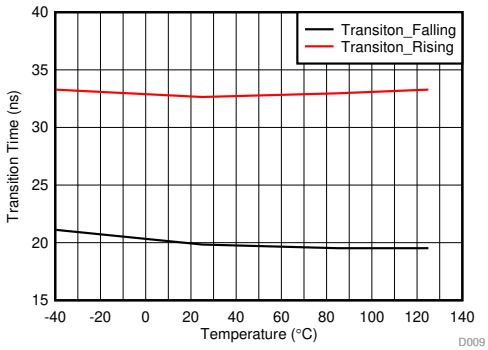
V_{DD} = 3.3 V

图 7-8. $T_{ON(EN)}$ and $T_{OFF(EN)}$ vs Temperature



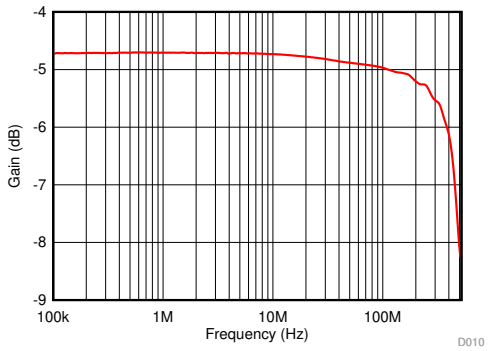
T_A = 25°C

图 7-9. $T_{TRANSITION}$ vs Supply Voltage



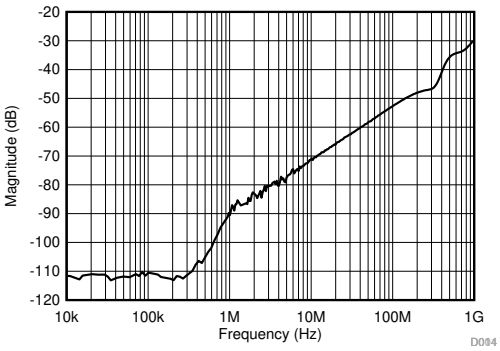
T_A = 25°C

图 7-10. $T_{TRANSITION}$ vs Temperature



T_A = 25°C

图 7-11. On Response vs Frequency



T_A = 25°C , V_{DD} = 3.3 V

图 7-12. Xtalk and Off-Isolation vs Frequency

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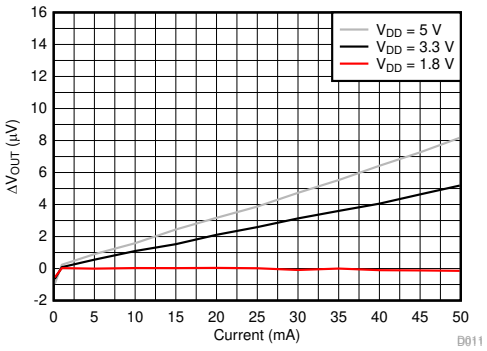
7.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)



V_S = (V_{DD}/2), T_A = 25°C

图 7-13. Injection Current vs Maximum Output Voltage Shift

8 Parameter Measurement Information

8.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown below. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed as shown in 图 8-1 with $R_{ON} = V / I_{SD}$:

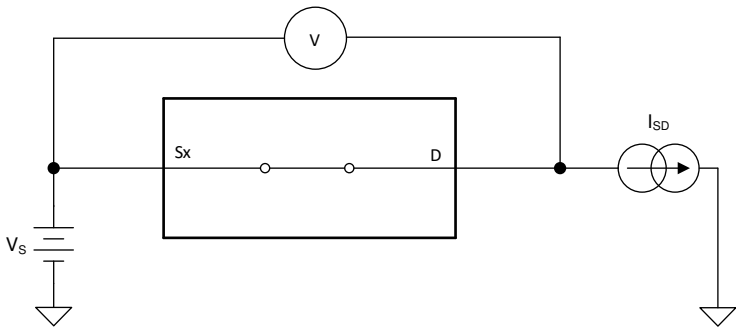


图 8-1. On-Resistance Measurement Setup

8.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

图 8-2 shows the setup used to measure both off-leakage currents.

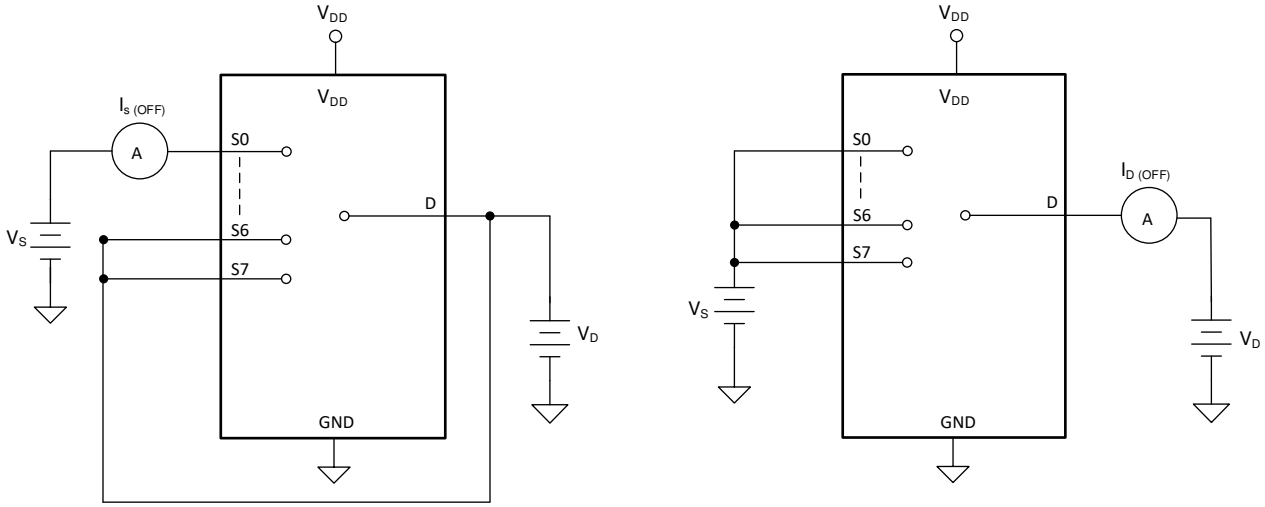


图 8-2. Off-Leakage Measurement Setup

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8.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 8-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

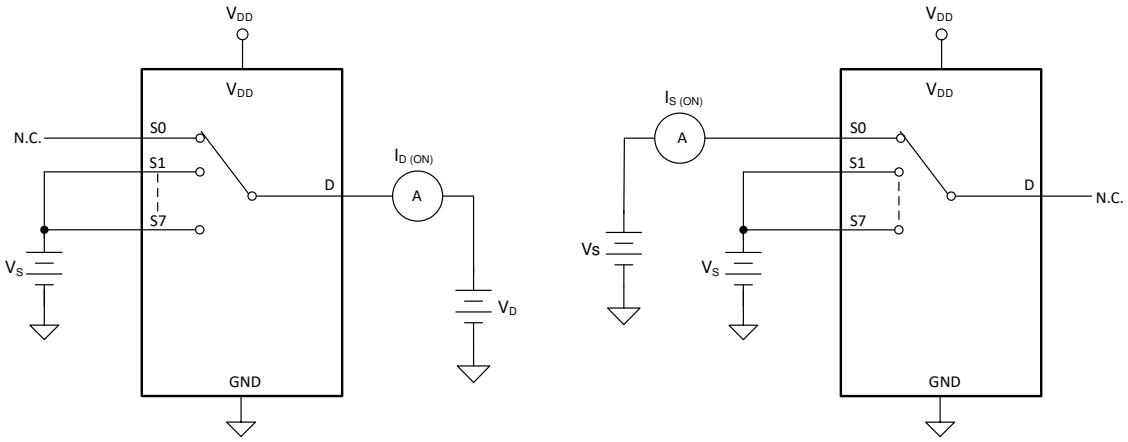

图 8-3. On-Leakage Measurement Setup

8.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 50% after the address signal has risen or fallen past the 50% threshold. 图 8-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

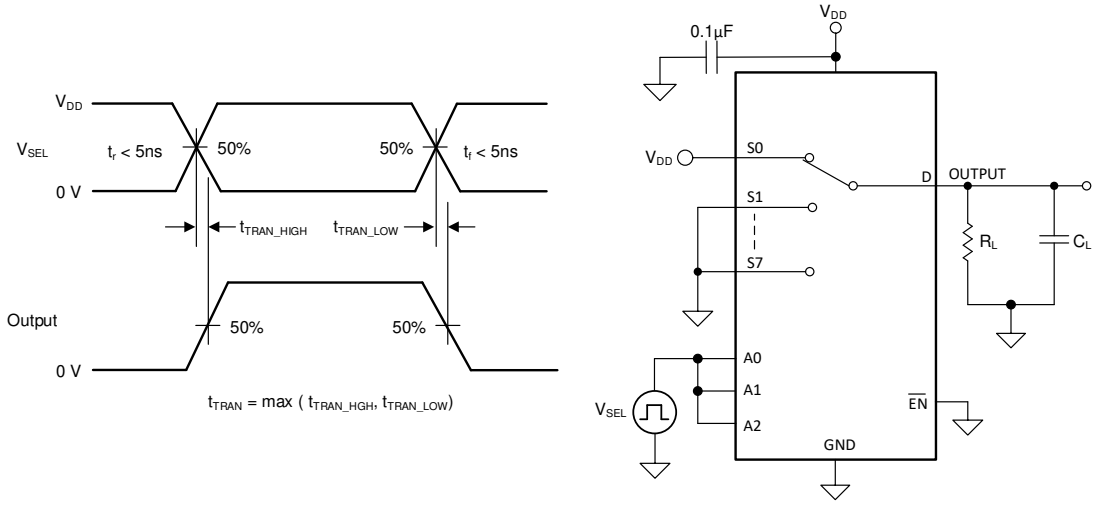

图 8-4. Transition-Time Measurement Setup

8.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 8-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

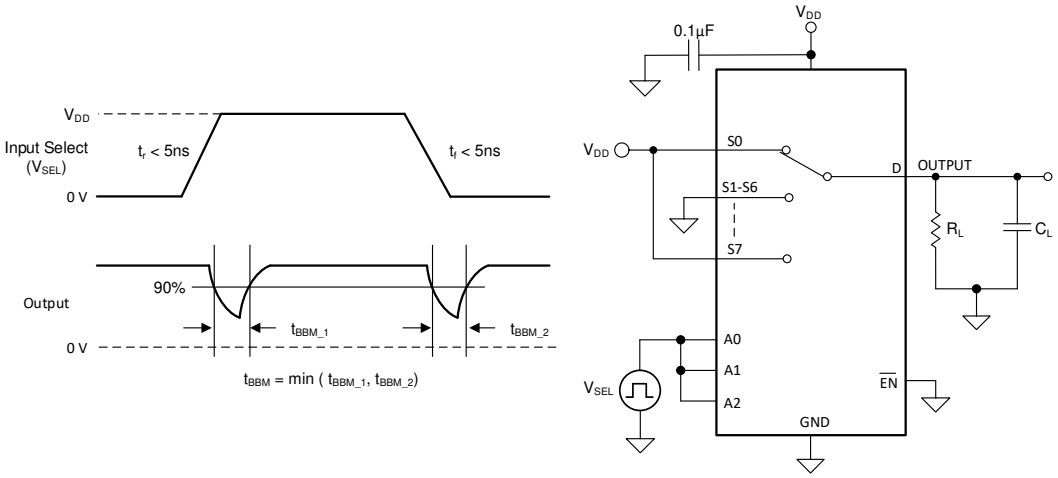

图 8-5. Break-Before-Make Delay Measurement Setup

8.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 10% after the enable has risen past the 50% threshold. The 10% measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. 图 8-6 shows the setup used to measure transition time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the 50% threshold. The 90% measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. 图 8-6 shows the setup used to measure transition time, denoted by the symbol $t_{OFF(EN)}$.

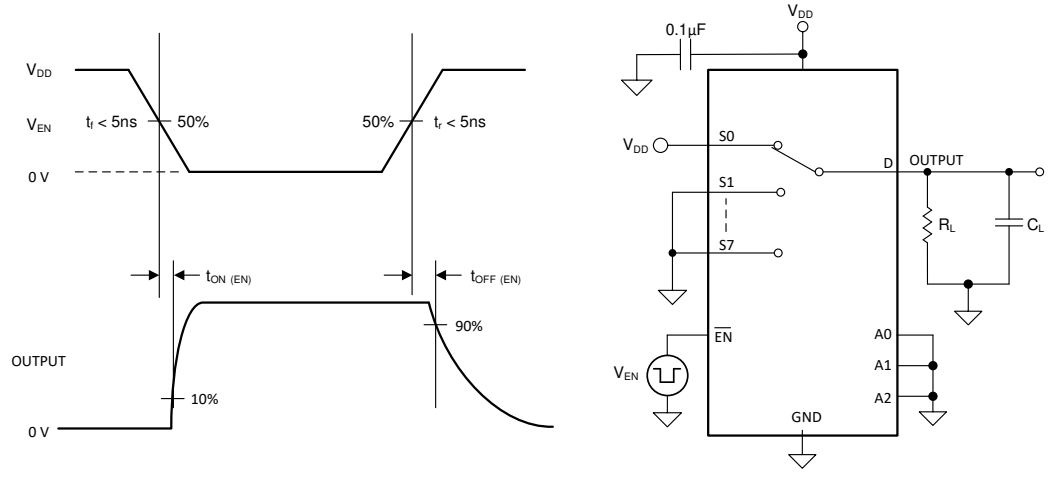

图 8-6. Turn-On and Turn-Off Time Measurement Setup

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8.7 Charge Injection

The TMUX1308 and TMUX1309 device have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. 图 8-7 shows the setup used to measure charge injection from source (Sx) to drain (D).

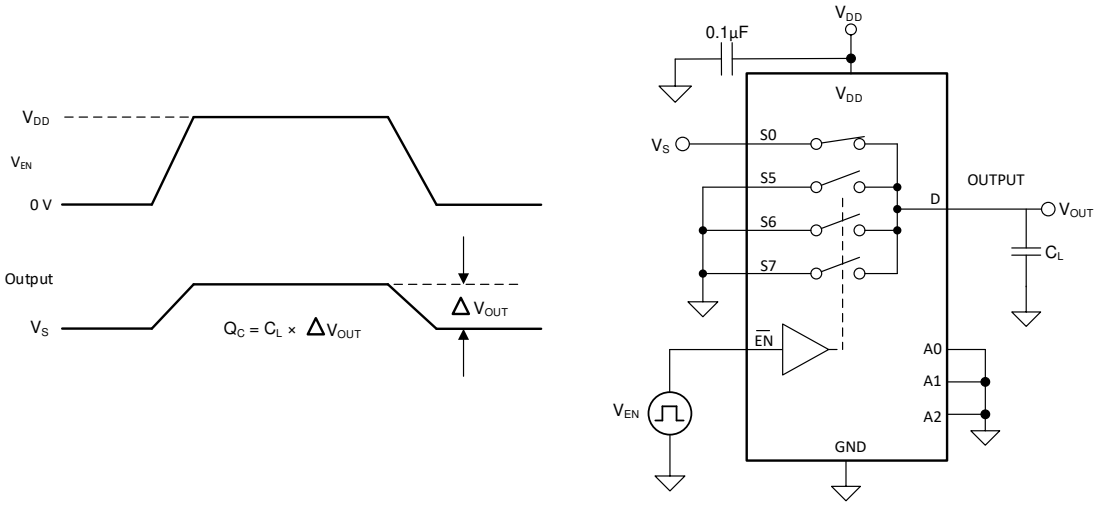

图 8-7. Charge-Injection Measurement Setup

8.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 图 8-8 shows the setup used to measure, and the equation to compute off isolation.

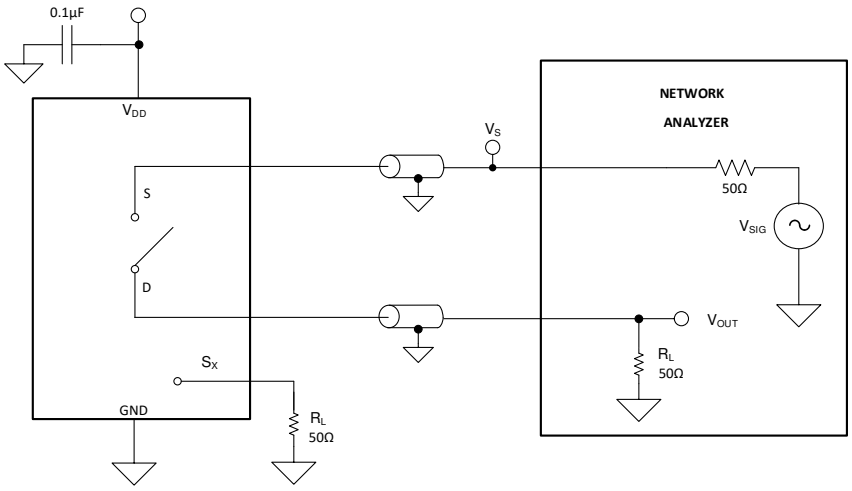

图 8-8. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

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8.9 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 图 8-9 shows the setup used to measure, and the equation used to compute crosstalk.

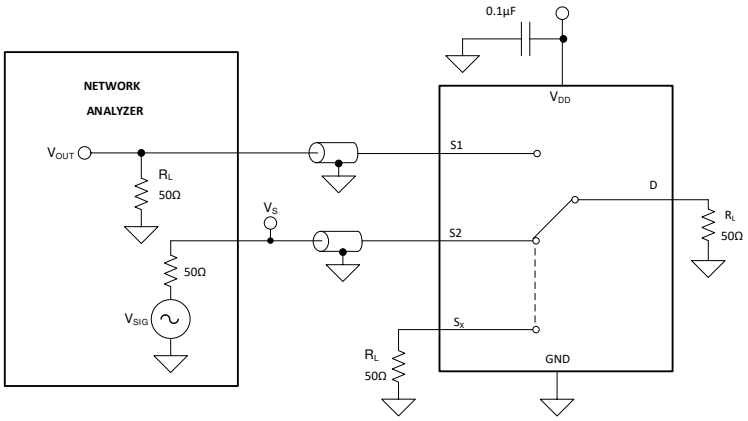

图 8-9. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

8.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 图 8-10 shows the setup used to measure bandwidth.

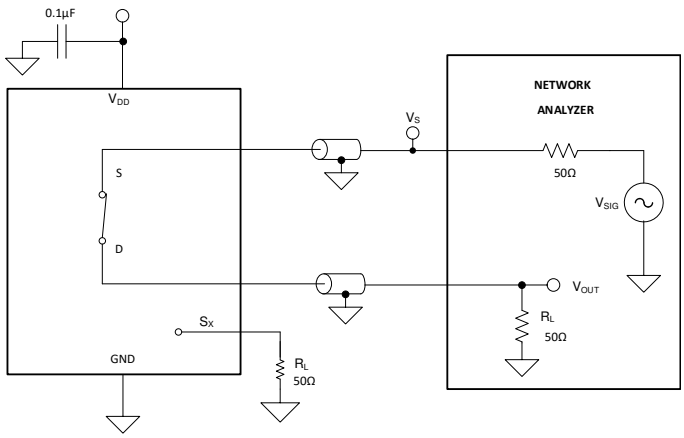

图 8-10. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right) \quad (3)$$

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8.11 Injection Current Control

Injection current is measured at the change in output of the enabled signal path when a current is injected into a disabled signal path. 图 8-11 shows the setup used to measure injection current control.

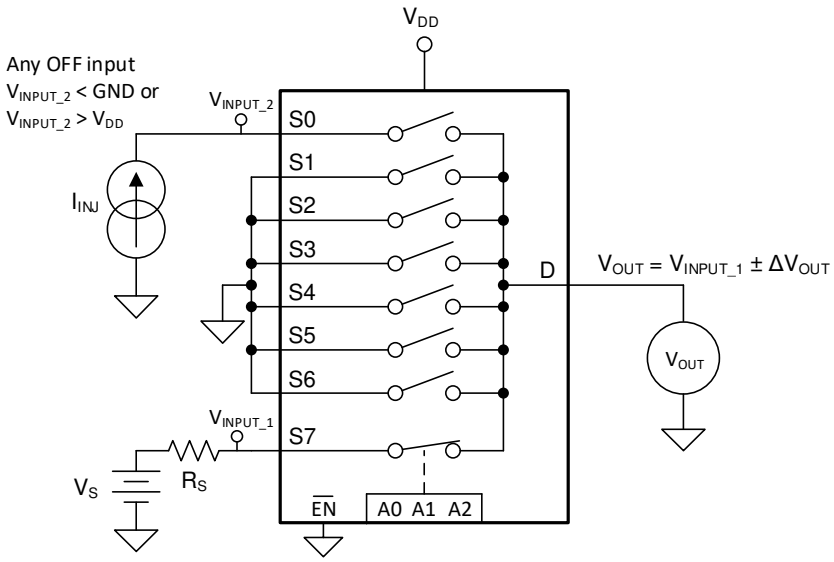


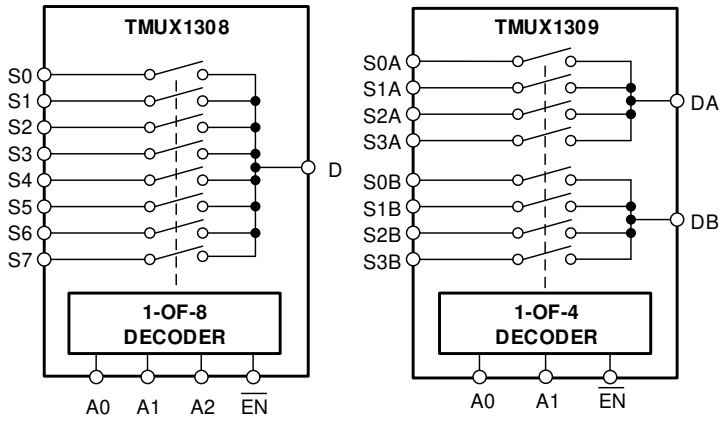
图 8-11. Injection Current Measurement Setup

9 Detailed Description

9.1 Overview

The TMUX1308 is an 8:1, single-ended (1-channel), mux. The TMUX1309 is a 4:1, differential (2-channel) mux. Each channel is turned on or turned off based on the state of the address lines and enable pin.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Bidirectional Operation

The TMUX1308 and TMUX1309 devices conduct equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each signal path has very similar characteristics in both directions so they can be used as both multiplexers and demultiplexer to support both analog and digital signals.

9.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for the TMUX1308 and TMUX1309 ranges from GND to V_{DD}.

9.3.3 1.8 V Logic Compatible Inputs

The TMUX1308 and TMUX1309 support 1.8-V logic compatible control for all logic control inputs. The logic input thresholds scale with supply but still provide 1.8-V logic control when operating at 5.5-V supply voltage. 1.8-V logic level inputs allows the multiplexers to interface with processors that have lower logic I/O rails and eliminates the need for an external voltage translator, which saves both space and BOM cost. The current consumption of the TMUX1308 and TMUX1309 devices increase when using 1.8-V logic with higher supply voltage. For more information on 1.8-V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

9.3.4 Fail-Safe Logic

The TMUX1308 and TMUX1309 device have Fail-Safe Logic on the control input pins (EN, A0, A1, and A2) allowing for operation up to 5.5-V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX1308 and TMUX1309 to be ramped to 5.5-V while V_{DD} = 0-V. Additionally, the feature enables operation of the multiplexers with V_{DD} = 1.8-V while allowing the select pins to interface with a logic level of another device up to 5.5-V, eliminating the potential need for an external voltage translator.

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9.3.5 Injection Current Control

Injection current is the current that is being forced into a pin by an input voltage (V_{IN}) higher than the positive supply (V_{DD} + ΔV) or lower than ground (V_{SS}). The current flows through the input protection diodes into whichever supply of the device is potentially compromising the accuracy and reliability of the system. Injected currents can come from various sources depending on the application.

- Harsh environments and applications with long cabling, such as in factory automation and automotive systems, may be susceptible to injected currents from switching or transient events.
- Other self-contained systems can also be subject to injected current if the input signal is coming from various sensors or current sources.

Injected Current Impact: typical CMOS switches have ESD protection diodes on the inputs and outputs. These diodes not only serve as ESD protection but also provide a voltage clamp to prevent the inputs or outputs going above V_{DD} or below GND and V_{SS}. When current is injected into the pin of a disabled signal path, a small amount of current goes through the ESD diode but most of the current goes through conduction to the drain. If forward diode voltage of the ESD diode (VF) is greater than the PMOS threshold voltage (VT), then the PMOS of all OFF switches turns ON and there would be undesirable subthreshold leakage between the source and the drain that can lift the OFF source pins up also. 图 9-1 shows a simplified diagram of a typical CMOS switch and associated injected current path.

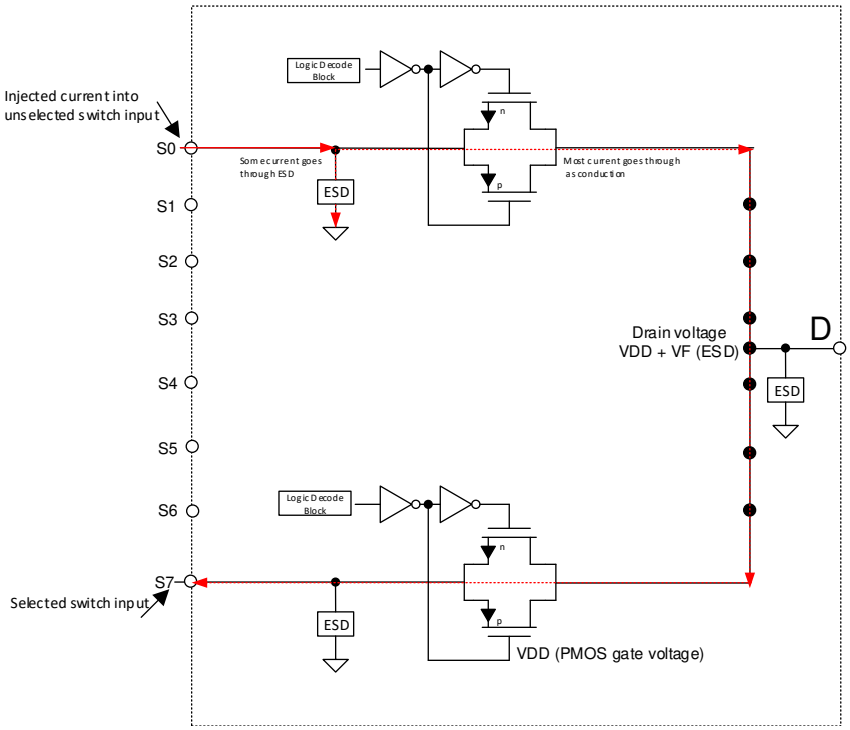

图 9-1. Simplified Diagram of Typical CMOS Switch and Associated Injected Current Path

It is quite difficult to cut off these current paths. The drain pin can never be allowed to exceed the voltage above V_{DD} by more than a VT. Analog pins can be protected against current injection by adding external components like a Schottky diode from the drain pin to ground to clamp the drain voltage at < V_{DD} + VT and cut off the current path.

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Change in R_{ON} due to Current Injection: because the ON resistance of the enabled FET switch is impacted by the change in the supply rail, when the drain pin voltage exceeds the supply voltage by more than a VT, an error in the output signal voltage can be expected. This undesired change in the output can cause issues related to false trigger events and incorrect measurement readings, potentially compromising the accuracy and reliability of the system. As shown in 图 9-2, S2 is the enabled signal path that is conducting a signal from S2 pin to D pin. Because there is an injected current at the disabled S1 pin, the voltage at that pin increases above the supply voltage and the ESD protection diode is forward biased, shifting the power supply rail. This shift in supply voltage alters the R_{ON} of the internal FET switches, causing a ΔV error on the output at the D pin.

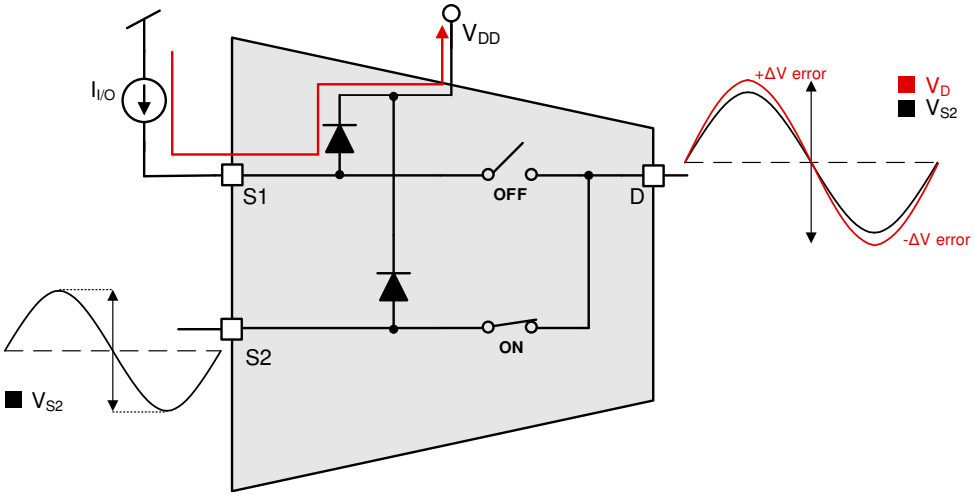

图 9-2. Injected Current Impact on R_{ON}

To avoid the complications of added external protection to your system, the TMUX1308 and TMUX1309 devices have an internal injection current control feature which eliminates the need for external diode and resistor networks typically used to protect the switch and keep the input signals within the supply voltage. The internal injection current control circuitry allows the signals on the disabled signal paths to exceed the supply voltage without affecting the signal of the enabled signal path. The injection current control circuitry also protects the TMUX13xx from currents injected into disabled signal paths without impacting the enabled signal path, which typical CMOS switches do not support. Additionally, the TMUX1308 and TMUX1309 do not have any internal diode paths to the supply pin, which eliminates the risk of damaging components connected to the supply pin or providing unintended power to the system supply rail. For a simplified diagram that shows one signal path for the TMUX13xx devices and the associated injection current circuit, refer to 节 9.2.

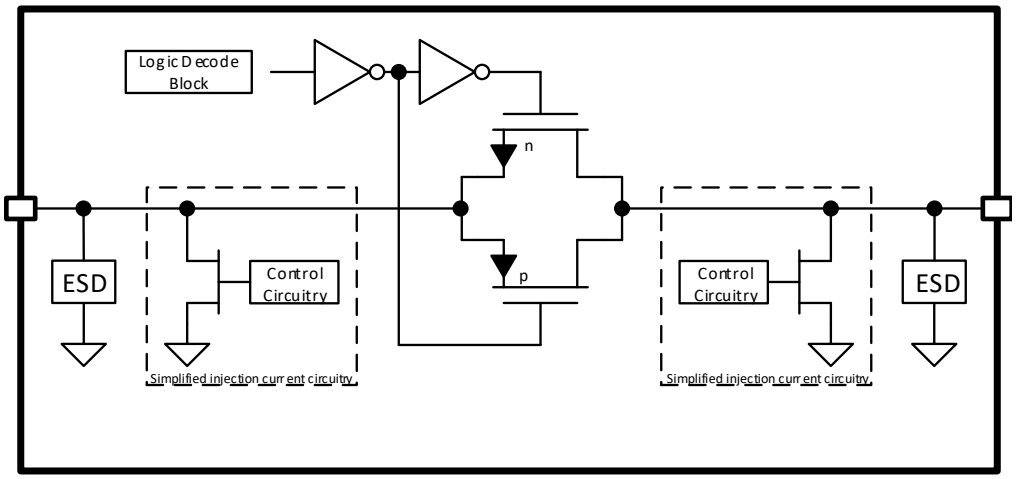

图 9-3. Simplified Diagram of Injection Current Control

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The injection current control circuitry is independently controlled for each source or drain pin (Sx or D). The control circuitry for a particular pin is enabled when that input is disabled by the logic pins and the injected current causes the voltage at the pin to be above V_{DD} or below GND. The injection current circuit includes an FET to shunt the undesired current to GND in the case of overvoltage or injected current events. Each injection current circuit is rated to handle up to 50 mA; the device, however, can support a maximum current of 100 mA at any given time. Depending on the system application, a series limiting resistor may be needed and must be sized appropriately. 图 9-3 shows the TMUX13xx protection circuitry with an injected current at an input pin.

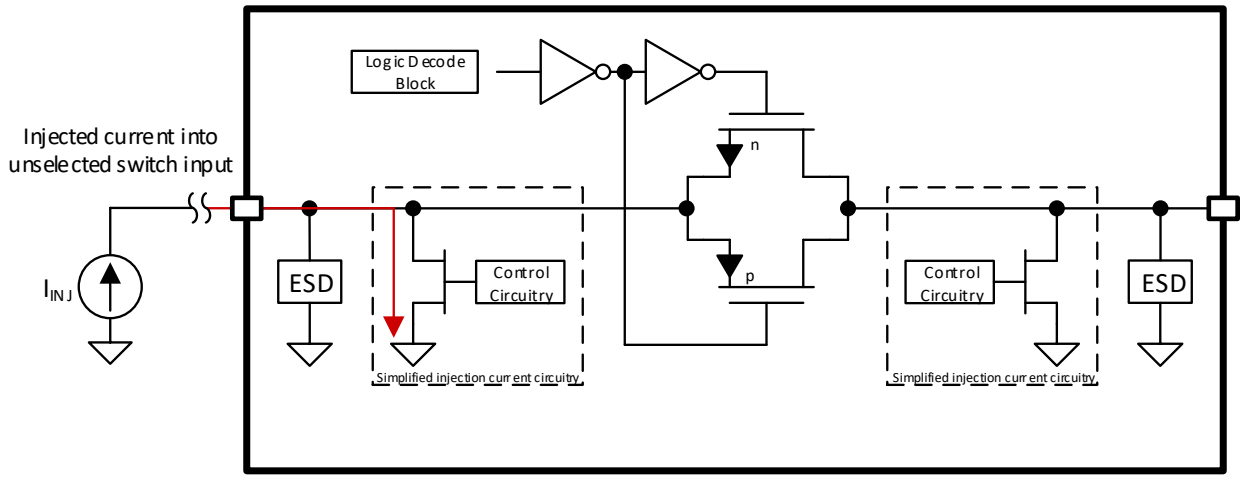

图 9-4. Injected Current at Input Pin

图 9-5 shows an example of using a series limiting resistor in the case of an overvoltage event.

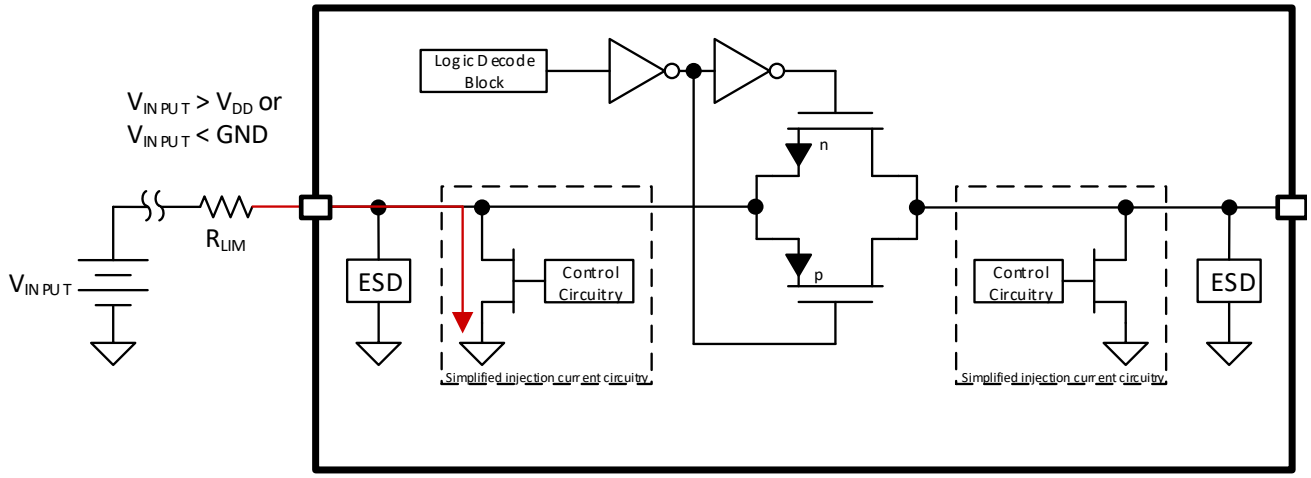

图 9-5. Over-Voltage Event with Series Resistor

For the injection current control circuitry to be active, two conditions must be present. First, the voltage at the source or drain pins is greater than V_{DD}, or less than GND. Next, the channel must be unselected. With those two requirements met, the protection FET will be turned on for any disabled signal path and shunt the pin to GND. In this event, a series resistor is needed to limit the total current injected into the device to be less than 100 mA. Three example scenarios are outlined in the following sections.

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9.3.5.1 TMUX13xx is Powered, Channel is Unselected, and the Input Signal is Greater Than V_{DD} (V_{DD} = 5 V, V_{INPUT} = 5.5 V)

A typical CMOS switch would have an internal ESD diode to the supply pin rated for ≅30 mA that would be turned on and a series limited resistor would be needed. However, any conducted current would be injected into the supply rail potentially damaging the system, unexpectedly turning on other devices on the same supply rail, or requiring additional components for protection. The TMUX13xx implementation also handles this scenario with a series limiting resistor; the current path, however, is now to GND which does not have the same issues as the current injected into the supply rail.

9.3.5.2 TMUX13xx is Powered, Channel is Selected, and the Input Signal is Greater Than V_{DD} (V_{DD} = 5 V, V_{INPUT} = 5.5 V)

The injection current control circuitry is fully active when the channel is unselected and an overvoltage event is present (overvoltage being defined as 0.5 V above the supply rail). However, in situations where the channel is selected and an overvoltage event occurs, this protection circuitry will still be partially active. In this instance, a portion of the injected current will be redirected through the protection circuitry to GND, but will not be a full shunt. So, some current will also flow through the source to drain path. This allows the device to tolerate overvoltage conditions in the event of the channel being selected, but precautions are still necessary to protect the device from overcurrent events such as implementing a current limiting resistor to keep the device below the maximum continuous source and drain current specification.

9.3.5.3 TMUX13xx is Unpowered and the Input Signal has a Voltage Present (V_{DD} = 0 V, V_{INPUT} = 3 V)

Many CMOS switches are unable to support a voltage at the input without a valid supply voltage present, otherwise the voltage will be coupled from input to output and could damage downstream devices or impact power-sequencing. The TMUX13xx circuitry can handle an input signal present without a supply voltage while minimizing power transfer from the input to output of the switch. By limiting the output voltage coupling to 400 mV the TMUX1308 and TMUX1309 help reduce the chance of conduction through any downstream ESD diodes.

9.4 Device Functional Modes

When the $\overline{EN}$ pin of the TMUX1308 is pulled low, one of the switches is closed based on the state of the address lines. Similarly, when the $\overline{EN}$ pin of the TMUX1309 is pulled low, two of the switches are closed based on the state of the address lines. When the $\overline{EN}$ pin is pulled high, all the switches are in an open state regardless of the state of the address lines.

Unused logic control pins must be tied to GND or V_{DD} to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx and Dx) should be connected to GND.

9.5 Truth Tables

表 9-1 and 表 9-2 provides the truth tables for the TMUX1308 and TMUX1309 respectively.

表 9-1. TMUX1308 Truth Table

$\overline{EN}$	A2	A1	A0	Selected Signal Path Connected To Drain (D) Pin
0	0	0	0	S0
0	0	0	1	S1
0	0	1	0	S2
0	0	1	1	S3
0	1	0	0	S4
0	1	0	1	S5
0	1	1	0	S6
0	1	1	1	S7
1	X(1)	X(1)	X(1)	All channels are off

(1) X denotes *do not care*.

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表 9-2. TMUX1309 Truth Table

$\overline{EN}$	A1	A0	Selected Signal Path Connected To Drain (DA and DB) Pins
0	0	0	S0A to DA S0B to DB
0	0	1	S1A to DA S1B to DB
0	1	0	S2A to DA S2B to DB
0	1	1	S3A to DA S3B to DB
1	X(1)	X(1)	All channels are off

(1) X denotes *do not care*.

10 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TMUX13xx family offers protection against injection current invents across a wide operating supply range (1.62 V to 5.5 V). These devices include 1.8 V logic compatible control input pins that enable operation in systems with 1.8 V I/O rails. Additionally, the control input pins support Fail-Safe Logic which allows for operation up to 5.5 V, regardless of the state of the supply pin. This feature stops the logic pins from back-powering the supply rail while the injection current circuitry prevents the signal path from back-powering the supply. These features make the TMUX13xx a family of general purpose multiplexers and switches that can reduce system complexity, board size, and overall system cost.

10.2 Typical Application

One useful application that takes advantage of the TMUX13xx features is multiplexing various signals into an ADC that is integrated into an MCU. Utilizing an integrated ADC in an MCU allows a system to minimize cost with a potential tradeoff of system performance when compared to an external ADC. The multiplexer allows for multiple inputs or sensors to be monitored with a single ADC pin of the device, which is critical in systems with limited I/O. The TMUX1309 is suitable for a similar design example using differential signals, or as two 4:1 multiplexers.

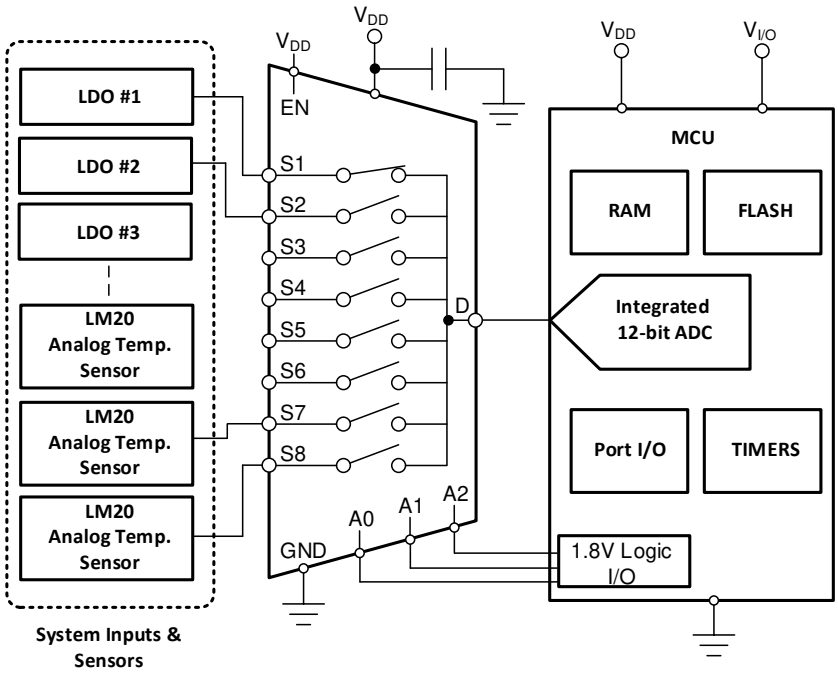

图 10-1. Multiplexing Signals to Integrated ADC

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10.3 Design Requirements

For this design example, use the parameters listed in 表 10-1.

表 10-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	5.0 V
I/O signal range	0 V to V_{DD} (Rail to Rail)
Control logic thresholds	1.8 V compatible

10.4 Detailed Design Procedure

The TMUX1308 and TMUX1309 can operate without any external components except for the supply decoupling capacitors. If the parts desired power-up state is disabled, then the enable pin should have a weak pull-up resistor and be controlled by the MCU through the GPIO. All inputs being muxed to the ADC of the MCU must fall within the recommended operating conditions of the TMUX1308 and TMUX1309, including signal range and continuous current. For this design with a supply of 5 V, the signal range can be 0 V to 5 V; the maximum continuous current can be 100 mA at an ambient temperature of 85°C or 25 mA at 125°C.

11 Power Supply Recommendations

The TMUX1308 and TMUX1309 devices operate across a wide supply range of 1.62 V to 5.5 V. Note: do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

12 Layout

12.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight; therefore, some traces must turn corners. 图 12-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

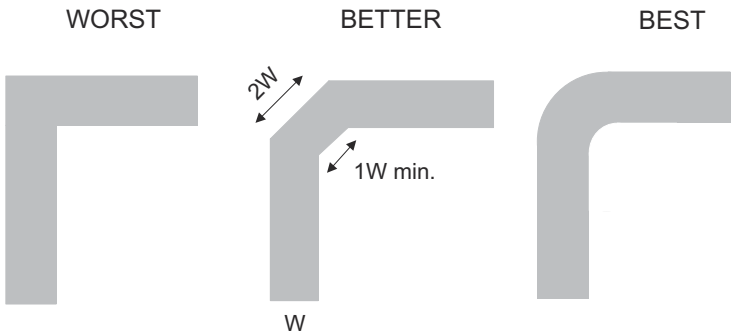

图 12-1. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

图 12-2 shows an example of a PCB layout with the TMUX1308 and TMUX1309. Some key considerations are as follows:

- Decouple the V_{DD} pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

12.2 Layout Example

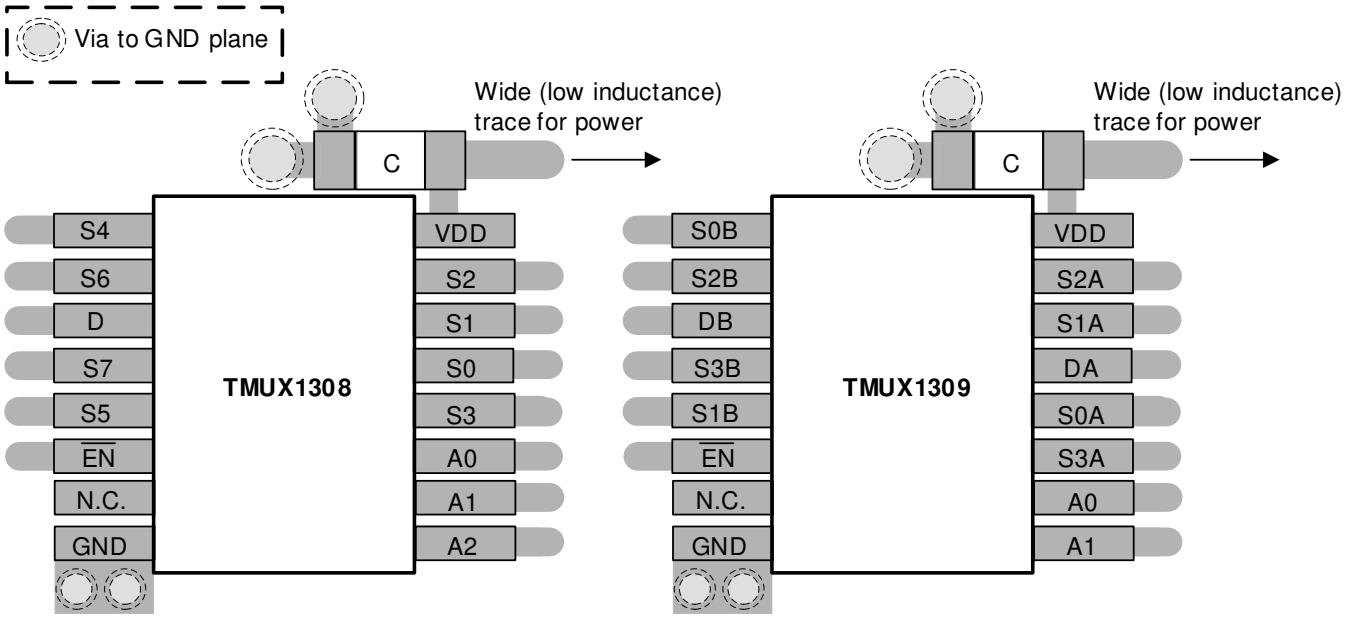

图 12-2. TMUX1308 and TMUX1309 Layout Example

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*
- Texas Instruments, *QFN/SON PCB Attachment*
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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13.4 Trademarks

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13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX1308BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1308
TMUX1308BQBR.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1308
TMUX1308BQBRG4	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1308
TMUX1308BQBRG4.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1308
TMUX1308DYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX1308
TMUX1308DYYR.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX1308
TMUX1308DYYRG4	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX1308
TMUX1308DYYRG4.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX1308
TMUX1308PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TM1308
TMUX1308PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1308
TMUX1309BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1309
TMUX1309BQBR.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1309
TMUX1309BQBRG4	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1309
TMUX1309BQBRG4.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1309
TMUX1309DYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX1309
TMUX1309DYYR.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX1309
TMUX1309DYYRG4	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX1309
TMUX1309DYYRG4.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX1309
TMUX1309PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TM1309
TMUX1309PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1309

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMUX1308, TMUX1309 :

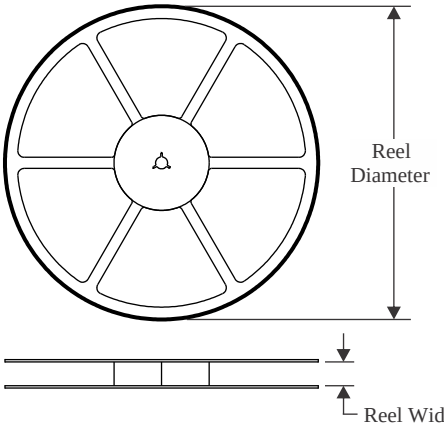
- Automotive : TMUX1308-Q1, TMUX1309-Q1

NOTE: Qualified Version Definitions:

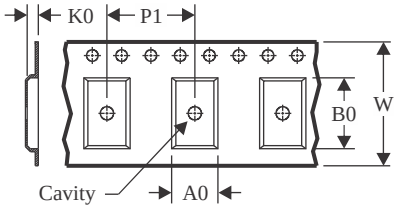
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

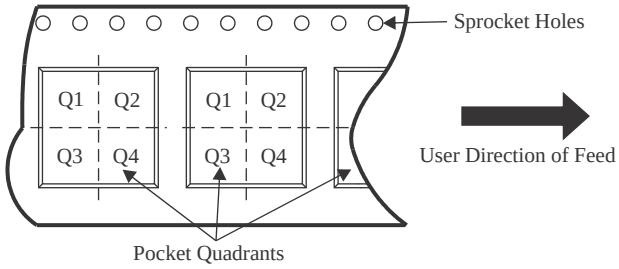


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

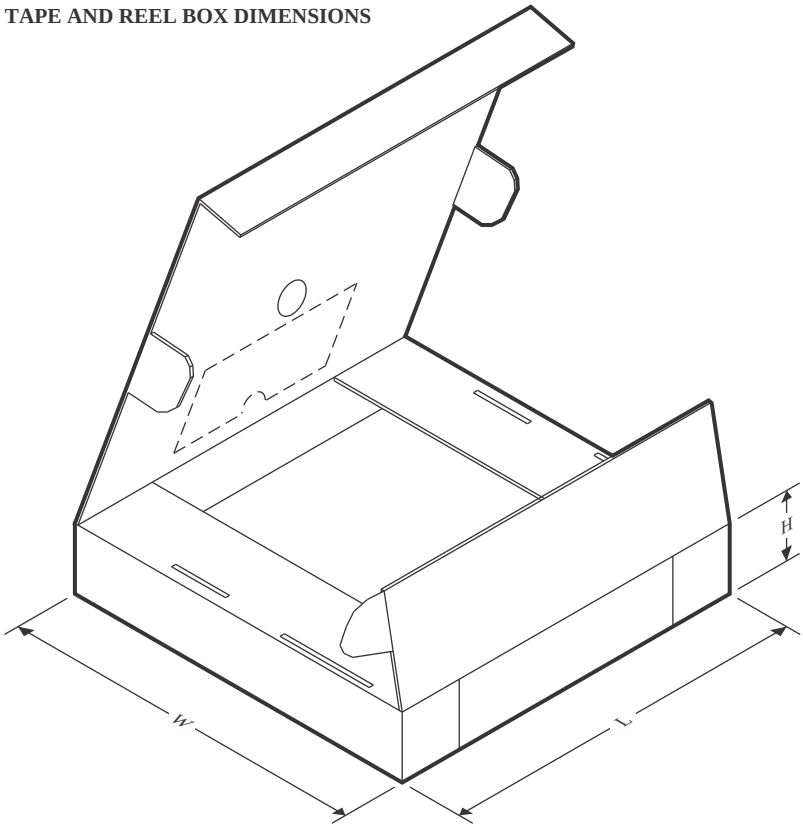
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1308BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TMUX1308BQBRG4	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TMUX1308DYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TMUX1308DYYRG4	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TMUX1308PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX1308PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX1309BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TMUX1309BQBRG4	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TMUX1309DYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TMUX1309DYYRG4	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TMUX1309PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX1309PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1308BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
TMUX1308BQBRG4	WQFN	BQB	16	3000	210.0	185.0	35.0
TMUX1308DYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TMUX1308DYYRG4	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TMUX1308PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX1308PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TMUX1309BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
TMUX1309BQBRG4	WQFN	BQB	16	3000	210.0	185.0	35.0
TMUX1309DYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TMUX1309DYYRG4	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TMUX1309PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX1309PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

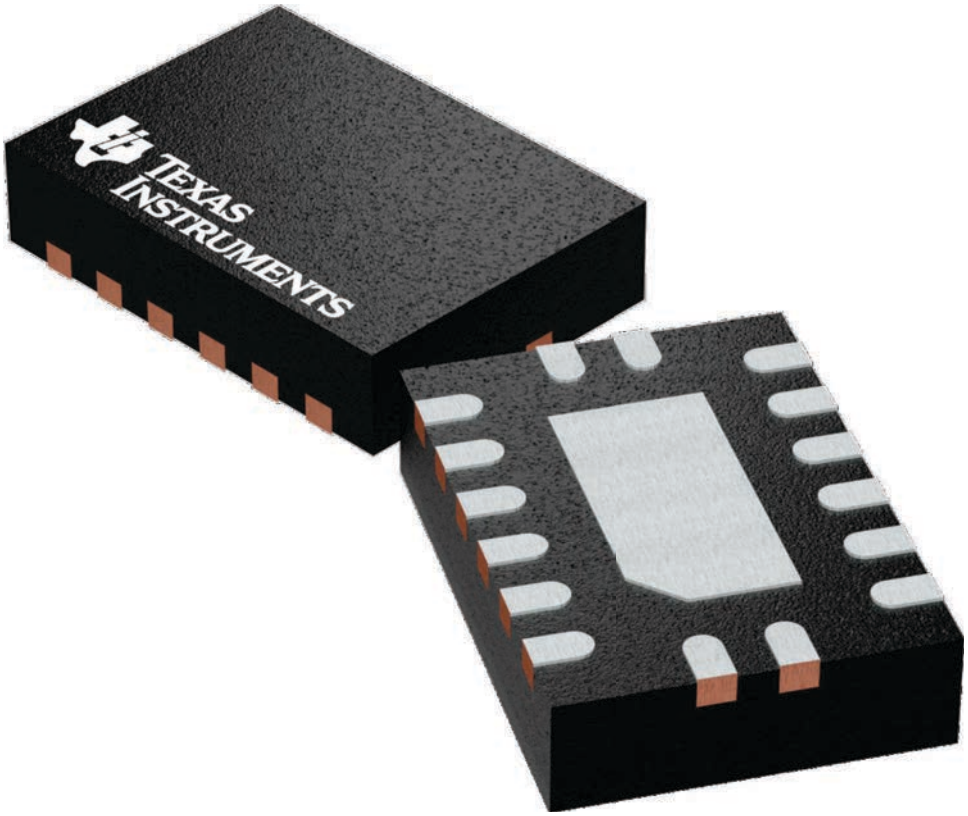
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



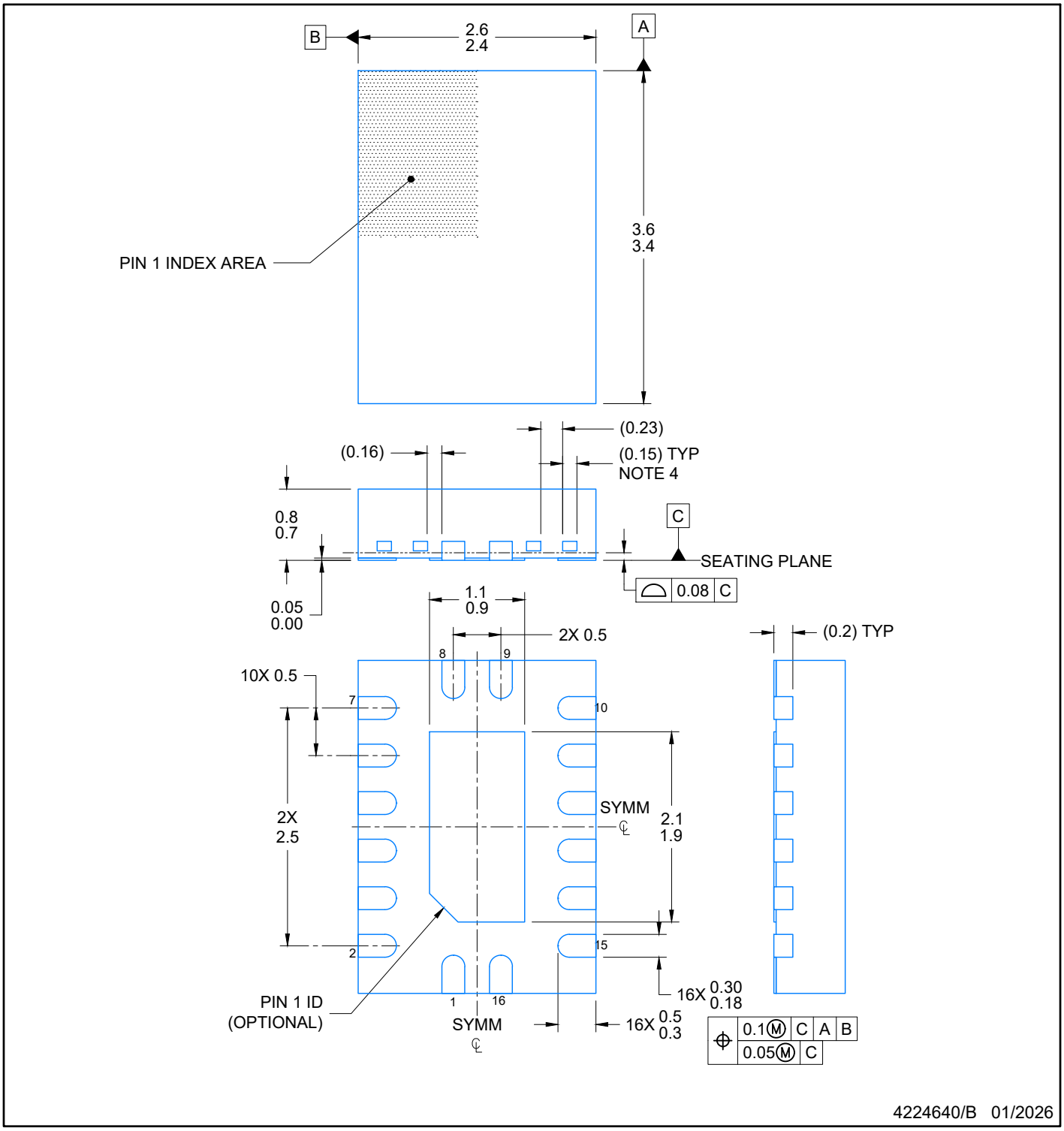
4226161/A

PACKAGE OUTLINE

BQB0016A

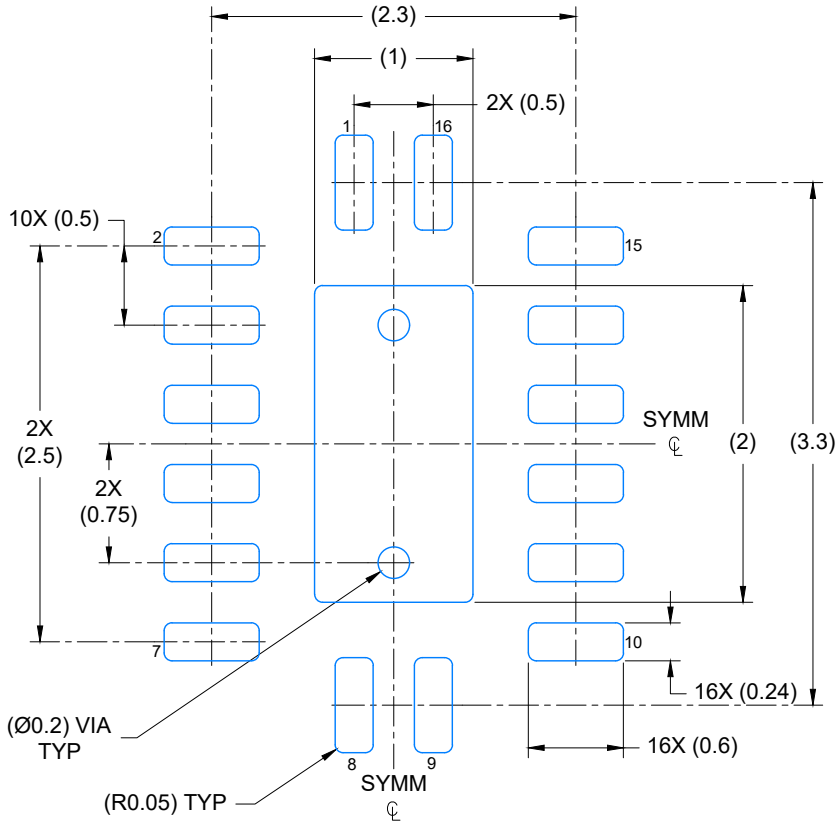
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

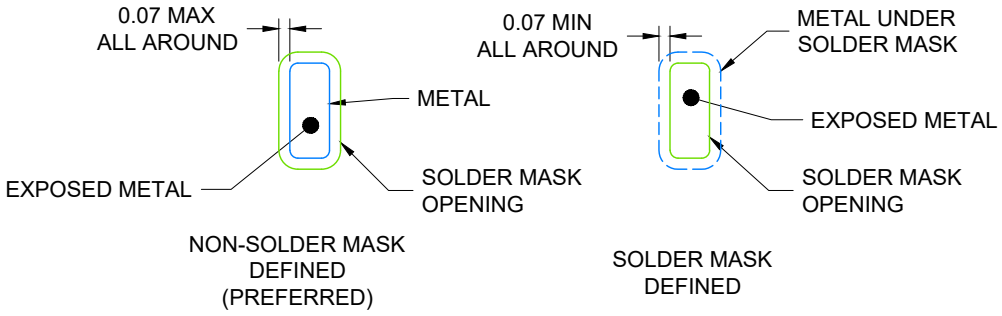


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

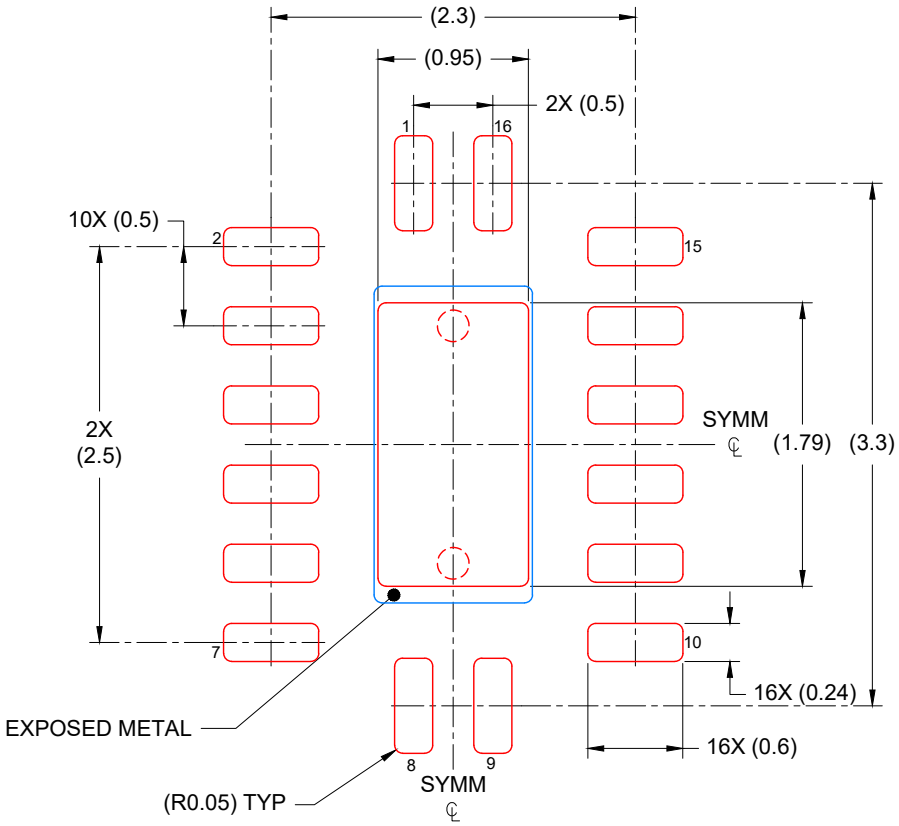


4224640/B 01/2026

1. NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/B 01/2026

NOTES: (continued)

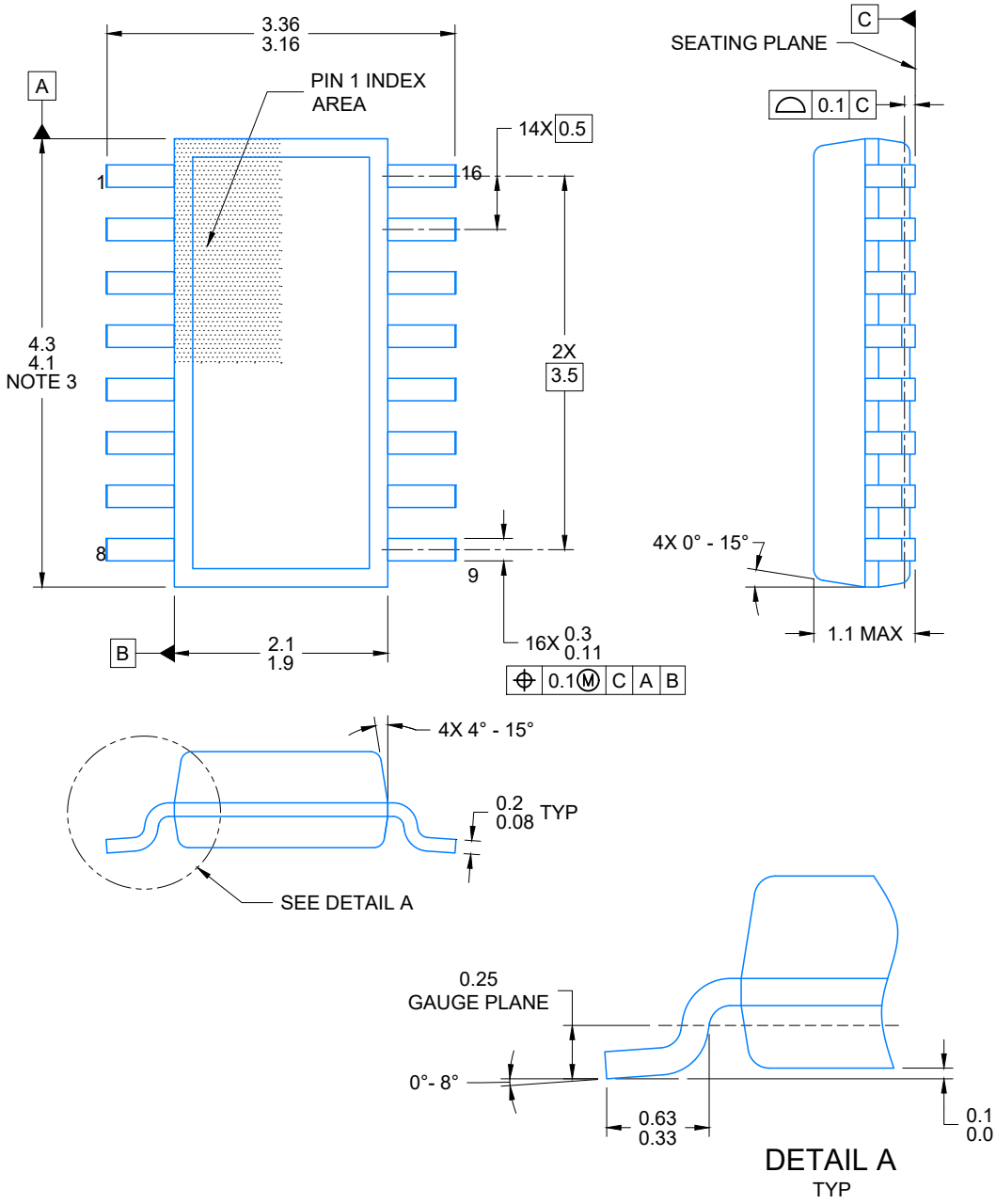
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0016A

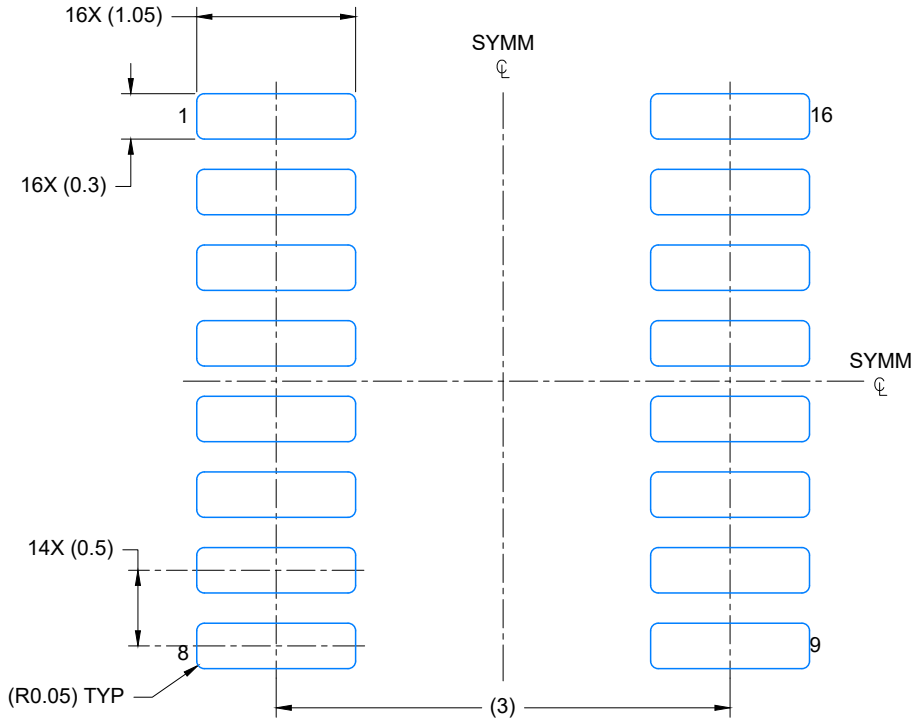
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

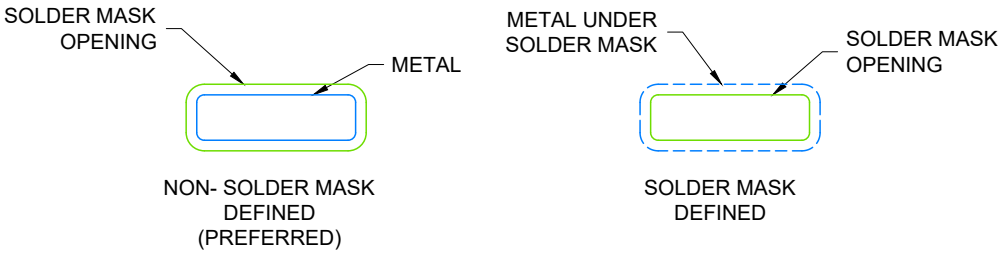


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

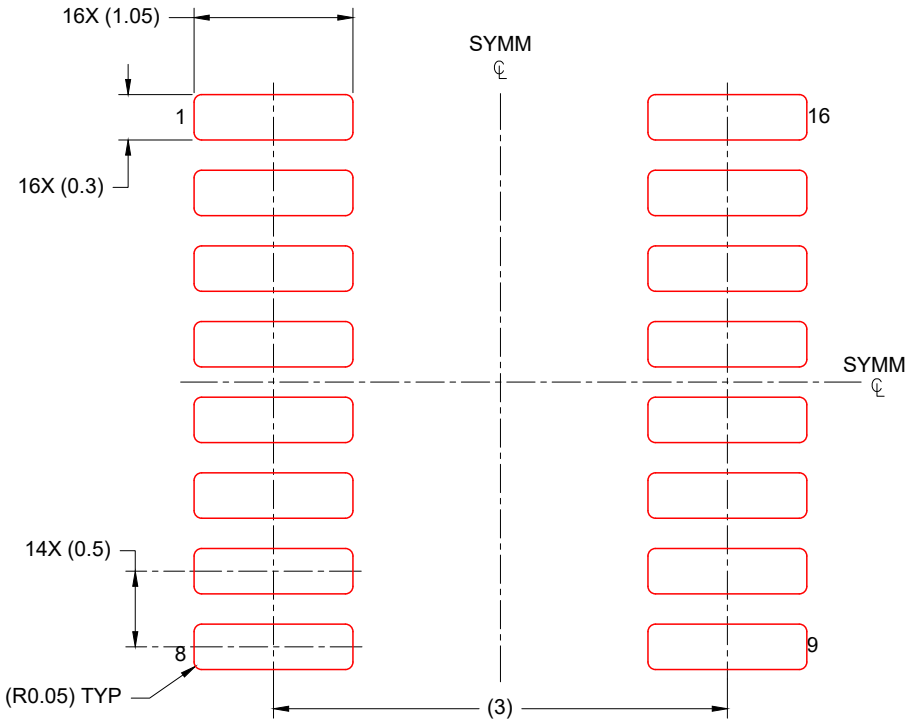
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

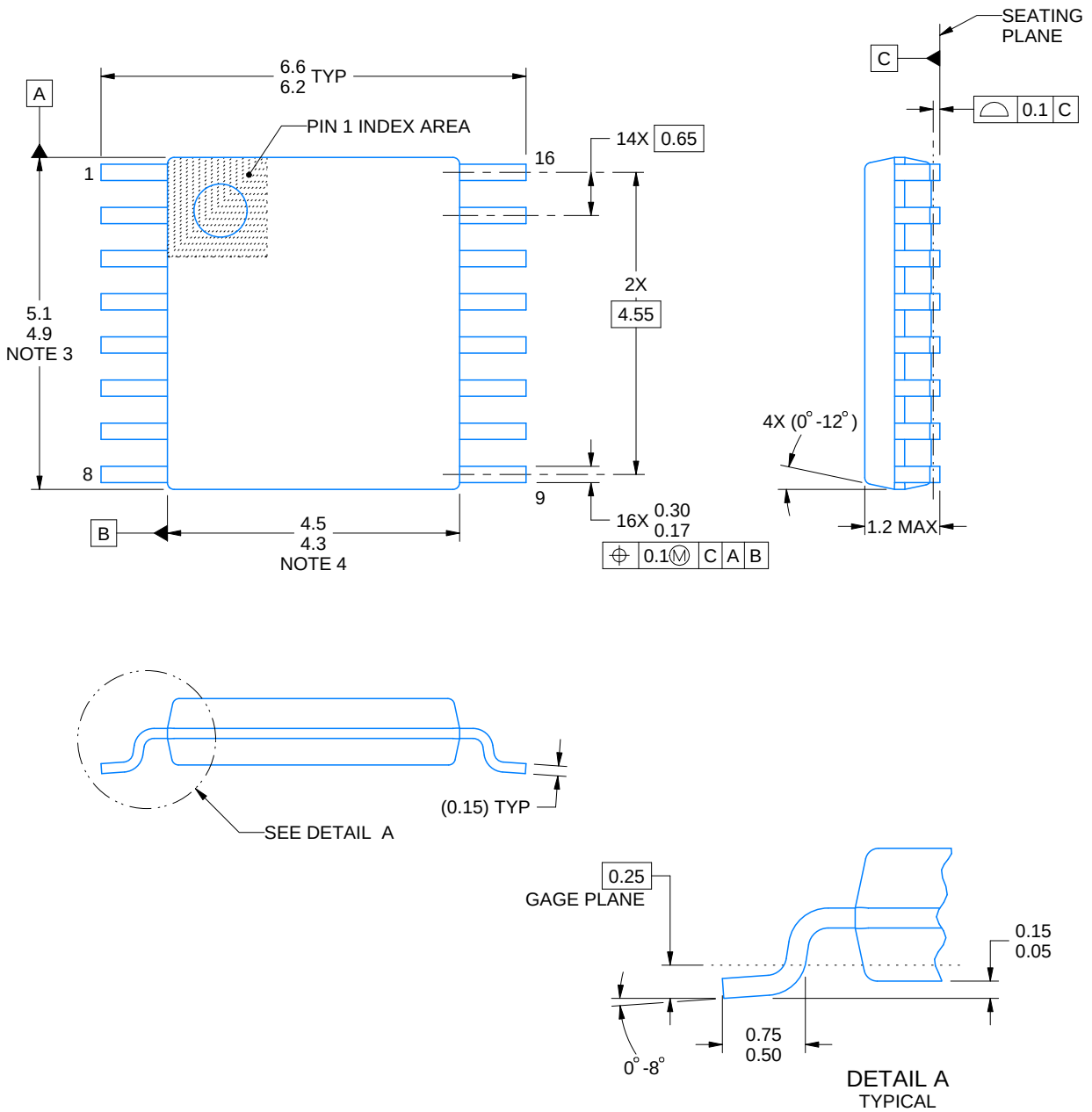
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

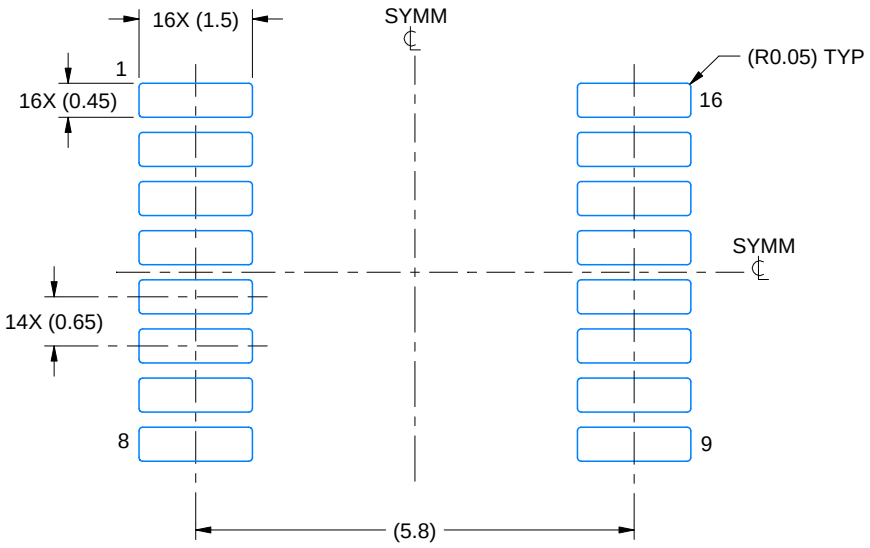
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

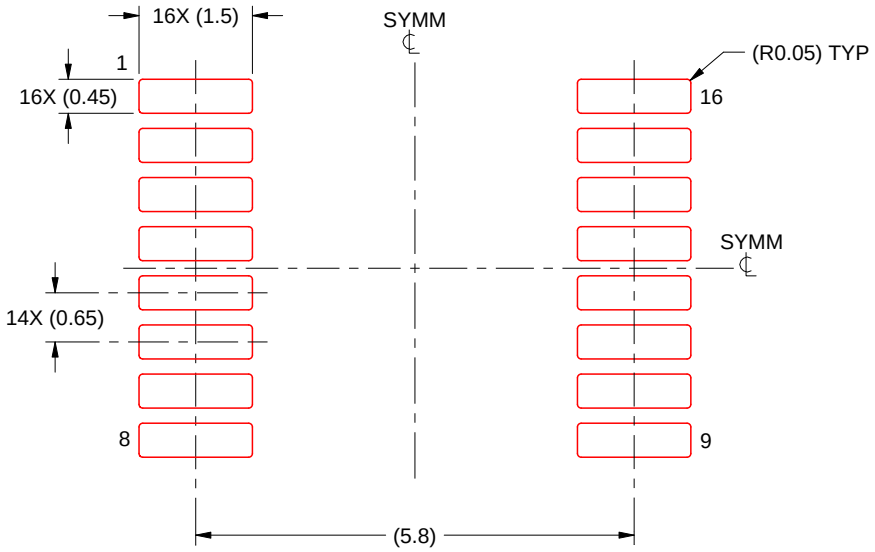


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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