MAX3222E 具有 ±15kV ESD 保护的 3V 至 5.5V 多通道 RS-232 线路驱动器和接收器

1 特性

- 为 RS-232 总线引脚提供 ESD 保护
  - ±15kV 人体放电模型 (HBM)
  - ±8kV IEC61000-4-2，接触放电
  - ±15kV IEC61000-4-2，气隙放电
- 符合或超出 TIA/EIA-232-F 和 ITU v.28 标准的要求
- 由 3V 至 5.5V V_{CC} 电源供电
- 速率高达 500kbit/s
- 两个驱动器和两个接收器
- 低待机电流：1 μA（典型值）
- 外部电容器：4 × 0.1 μF
- 支持 5V 逻辑输入（3.3V 电源时）
- 适合 SNx5C3222E 的备选高速引脚兼容器件 (1Mbit/s)

2 应用

- 工业 PC
- 有线网络
- 数据中心和网络设备
- 笔记本电脑
- 手持设备

3 说明

MAX3222E 由两个线路驱动器、两个线路接收器和一个双电荷泵电路组成，具有引脚对引脚（串行端口连接引脚，包括 GND）±15kV ESD 保护。

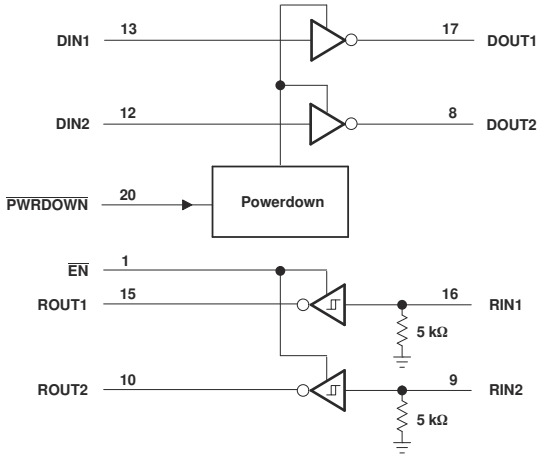
该器件符合 TIA/EIA-232-F 的要求并在异步通信控制器与串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由单个 3V 至 5.5V 电源供电。该器件以高达 500kbit/s 的数据信号传输速率和最高 30V/μs 的驱动器输出压摆率运行。

通过设置关断 ($\overline{PWRDOWN}$) 输入低电平（仅从电源消耗 1 μA 电流），可以将 MAX3222E 置于关断模式。当器件关断时，接收器保持活动状态，而驱动器置于高阻抗状态。此外，在关断期间，将会禁用板载电荷泵；V+ 降低至 V_{CC}，V– 升高至 GND。通过将启用 ($\overline{EN}$) 设置为高电平，接收器输出也可以置于高阻抗状态。

封装信息

器件型号	封装(1)	封装尺寸(2)
MAX3222E	DB（SSOP，20）	7.2mm x 7.8mm
	DW（SOIC，20）	12.8mm x 10.3mm
	PW（TSSOP，20）	6.5mm x 6.4mm
	DGS（VSSOP，20）	5.1mm x 4.9mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



引脚编号用于 DB、DW 和 PW 封装。

逻辑图（正逻辑）

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

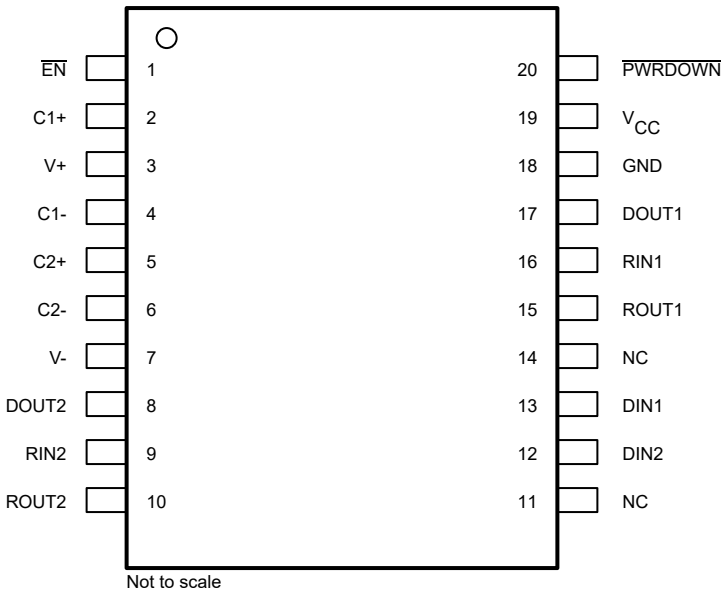


图 4-1. DB, DW, PW DGS Package (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	2	—	Charge pump capacitor pin
C1-	4	—	Charge pump capacitor pin
C2+	5	—	Charge pump capacitor pin
C2-	6	—	Charge pump capacitor pin
DIN1	13	I	Driver logic input
DIN2	12	I	Driver logic input
DOUT1	17	O	RS-232 driver output
DOUT2	8	O	RS-232 driver output
$\overline{EN}$	1	I	Receiver enable, active low
GND	18	—	Ground
NC	11,14	—	No internal connection
$\overline{PWRDOWN}$	20	I	Driver disable, active low
RIN1	16	I	RS-232 receiver input
RIN2	9	I	RS-232 receiver input
ROUT1	15	O	Receiver logic output
ROUT2	10	O	Receiver logic output
V_{CC}	19	—	Power Supply
V+	3	—	Charge pump capacitor pin
V-	7	—	Charge pump capacitor pin

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive-output supply voltage range(2)		–0.3	7	V
V–	Negative-output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Driver ($\overline{EN}$, $\overline{PWRDOWN}$)	–0.3	6	V
		Receiver	–25	25	
V_O	Output voltage range	Driver	–13.2	13.2	V
		Receiver	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

ESD Ratings

				TYP	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except RIN1, RIN2, DOUT1 and DOUT2 pins	±3000	V
			RIN1, RIN2, DOUT1 and DOUT2 pins to GND	±15,000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	All pins	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ESD Ratings - IEC Specifications

				TYP	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2, Contact Discharge(1)	RIN1, RIN2, DOUT1, DOUT2 pins(2)	±8,000	V
		IEC 61000-4-2, Air-Gap Discharge(1)		±15,000	

(1) For PW and DB packages only, a minimum of 1µF capacitor is required between V_{CC} and GND to meet the specified IEC 61000-4-2 rating.
(2) For optimized IEC ESD performance for DGS package, the recommendation is to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

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5.2 Recommended Operating Conditions

See 图 8-1 and (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{EN}$, $\overline{PWRDOWN}$	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{EN}$, $\overline{PWRDOWN}$				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{EN}$, $\overline{PWRDOWN}$		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature		MAX3222EC	0		70	°C
			MAX3222EI	–40		85	

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

5.3 Thermal Information

THERMAL METRIC(1)		MAX3222E				UNIT
		DB (SSOP)	DW (SOIC)	PW (TSSOP)	DGS (VSSOP)	
		20 Pins	20 Pins	20 Pins	20 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.0	58.0	94.1	92.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.2	30.0	35.2	35.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.1	29.6	45.5	48.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.3	7.7	3.1	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.6	29.3	45.1	47.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 8-1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP(1)	MAX	UNIT
I_I	Input leakage current ($\overline{EN}$, $\overline{PWRDOWN}$)			±0.01	±1	μA
I_{CC}	Supply current	No load, $\overline{PWRDOWN}$ at V_{CC}		0.3	1	mA
	Supply current (powered off)	No load, $\overline{PWRDOWN}$ at GND		1	10	μA

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

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5.5 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 8-1)

PARAMETER		TEST CONDITIONS(3)		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	μA
I_{OS}	Short-circuit output current(2)	V_{CC} = 3.6 V	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V					
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V	300	10M		Ω
I_{OZ}	Output leakage current	$\overline{PWRDOWN}$ = GND	V_{CC} = 3 V to 3.6 V, V_O = ±12 V			±25	μA
			V_{CC} = 4.5 V to 5.5 V, V_O = ±10 V			±25	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
(3) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

5.6 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 8-1)

PARAMETER		TEST CONDITIONS(3)		MIN	TYP(1)	MAX	UNIT
	Maximum data rate	C_L = 1000 pF, One DOUT switching,	R_L = 3 kΩ, See 图 6-1	250	500		kbit/s
$t_{sk(p)}$	Pulse skew(2)	C_L = 150 pF to 2500 pF, See 图 6-2	R_L = 3 kΩ to 7 kΩ,		300		ns
SR(tr)	Slew rate, transition region (see 图 6-1)	R_L = 3 kΩ to 7 kΩ, V_{CC} = 3.3 V	C_L = 150 pF to 1000 pF	6		30	V/μs
			C_L = 150 pF to 2500 pF	4		30	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

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5.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 8-1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})			0.3		V
I_{OZ}	Output leakage current	$\overline{EN}$ = 1		±0.05	±10	μA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

5.8 Switching Characteristics: Receiver

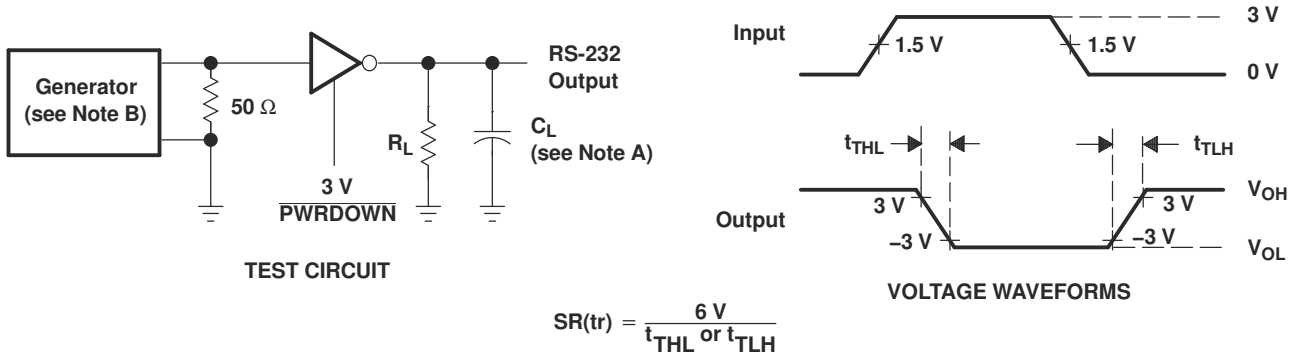
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(3)	TYP(1)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 图 6-3	300	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, See 图 6-3	300	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 图 6-4	200	ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, See 图 6-4	200	ns
$t_{sk(p)}$	Pulse skew(2)	See 图 6-3	300	ns

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

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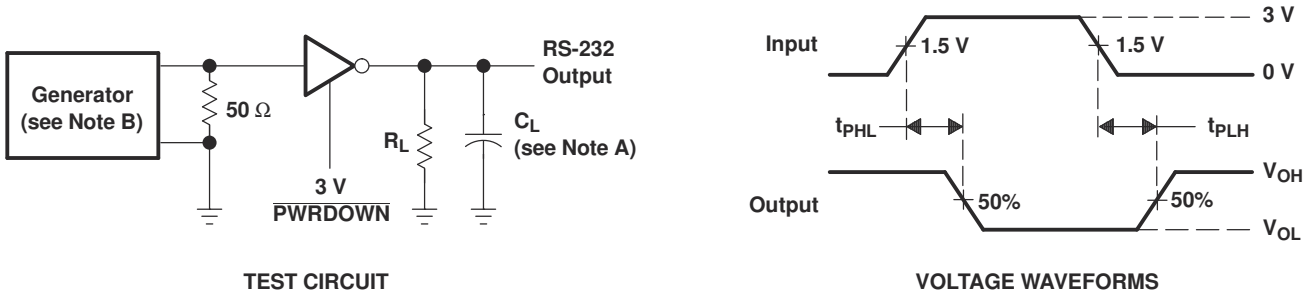
6 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250kbit/s, Z_O = 50Ω, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

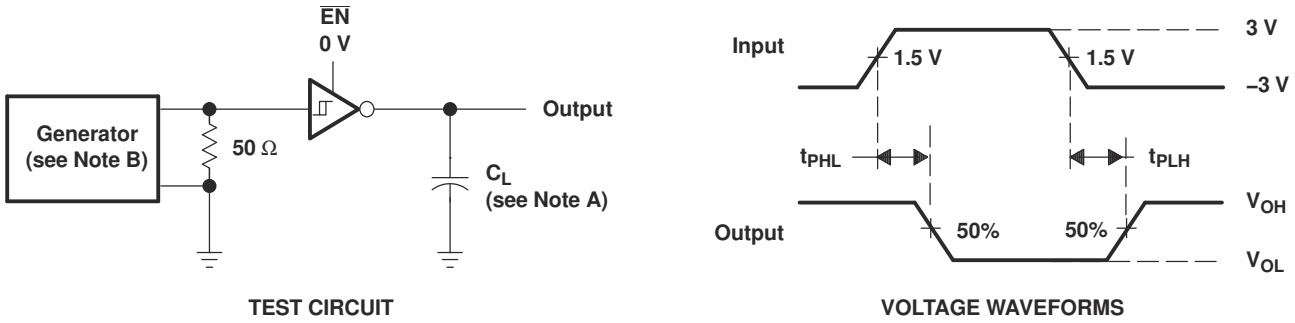
图 6-1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250kbit/s, Z_O = 50Ω, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

图 6-2. Driver Pulse Skew

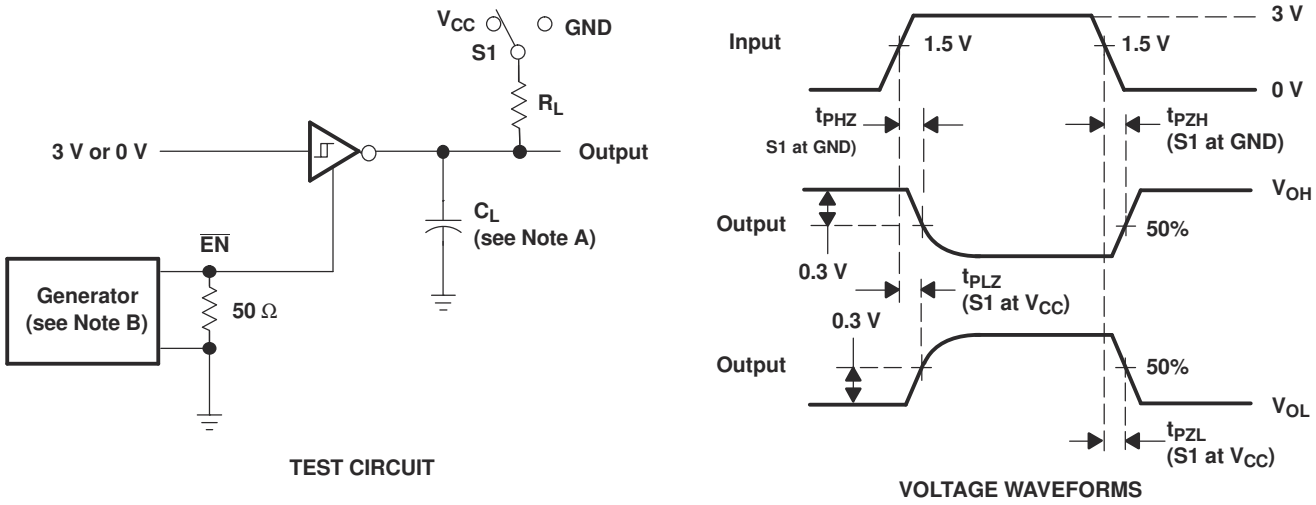


A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50Ω, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

图 6-3. Receiver Propagation Delay Times

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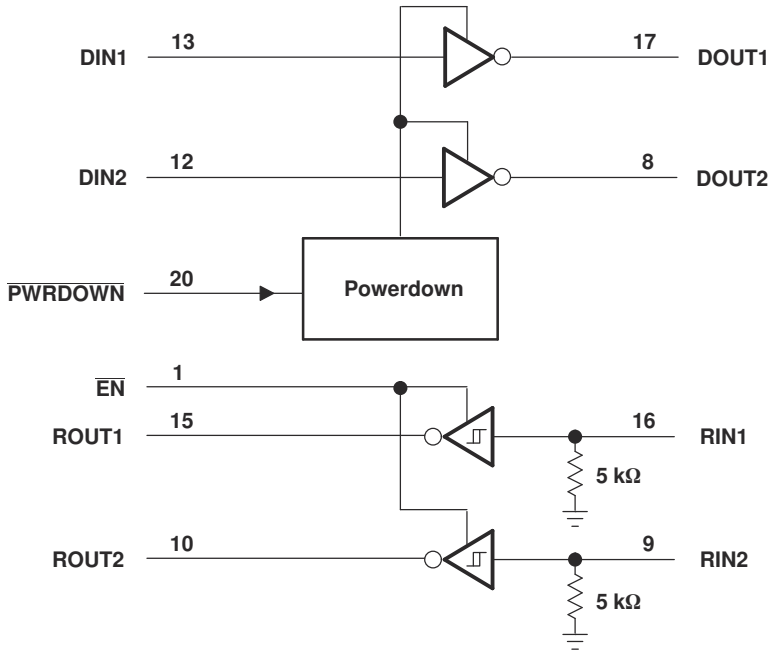
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50Ω, 50% duty cycle, t_r ⩽ 10ns, t_f ⩽ 10ns.

图 6-4. Receiver Enable and Disable Times

7 Detailed Description

7.1 Functional Block Diagram



Pin numbers are for the DB, DW, and PW packages.

图 7-1. Logic Diagram (Positive Logic)

7.2 Device Functional Modes

表 7-1. Function Table: Each Driver

INPUTS(1)		OUTPUT DOUT
DIN	$\overline{\text{PWRDOWN}}$	
X	L	Z
L	H	H
H	H	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 7-2. Function Table: Each Receiver

INPUTS(1)		OUTPUT ROUT
RIN	$\overline{\text{EN}}$	
L	L	H
H	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off),
Open = input disconnected or connected driver off

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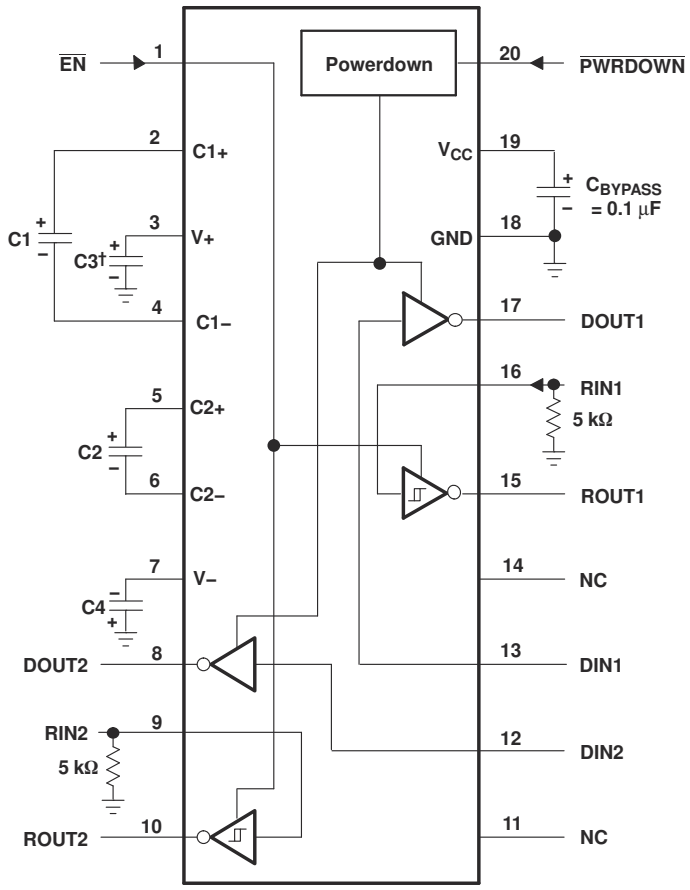
8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.2 Typical Application



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.
B. NC – No internal connection
C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

图 8-1. Typical Operating Circuit and Capacitor Values

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (December 2024) to Revision E (December 2024)	Page
• 将整个数据表中的 VSSOP (DSG) 封装更改为 VSSOP (DGS) 封装	1

Changes from Revision C (January 2023) to Revision D (December 2024)	Page
• 将*器件信息* 表更改为*封装信息* 表	1
• 向数据表中添加了 VSSOP (DSG) 封装	1
• Added Note 2 to the *ESD Ratings, IEC Specifications*	4

Changes from Revision B (August 2021) to Revision C (January 2023)	Page
• Changed the *ESD Ratings - IEC Specifications* table note to include the DB package	4
• Changed the values of $R_{\theta JA}$ in the *Thermal Information* table for the DB package	5

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Changes from Revision A (September 2009) to Revision B (August 2021) **Page**

- 更新了*应用*部分的列表。 1
- 删除了*订购信息*表 1
- 添加了*器件信息*表、*引脚配置和功能*、*详细说明*部分、*应用和实施*部分 1
- Deleted the Package thermal impedance from the *Absolute Maximum Ratings* 4
- Changed the *ESD Ratings* table 4
- Added the *ESD Ratings - IEC Specifications* table 4
- Added the *Thermal Information* table 5
- Changed the value of $R_{\theta JA}$ for PW package (previously in the *Absolute Maximum Ratings* table), and added additional thermal parameters for all packages in the *Thermal Information* table 5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX3222ECDB	Obsolete	Production	SSOP (DB) | 20	-	-	Call TI	Call TI	0 to 70	MP222EC
MAX3222ECDBR	Obsolete	Production	SSOP (DB) | 20	-	-	Call TI	Call TI	0 to 70	MP222EC
MAX3222ECDW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	0 to 70	MAX3222EC
MAX3222ECDWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3222EC
MAX3222ECDWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3222EC
MAX3222ECDWRG4	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3222EC
MAX3222ECDWRG4.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3222EC
MAX3222ECPWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP222EC
MAX3222ECPWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP222EC
MAX3222EIDB	Obsolete	Production	SSOP (DB) | 20	-	-	Call TI	Call TI	-40 to 85	MP222EI
MAX3222EIDBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP222EI
MAX3222EIDBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP222EI
MAX3222EIDBRG4	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP222EI
MAX3222EIDBRG4.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP222EI
MAX3222EIDGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	222EI
MAX3222EIDGSR.A	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	222EI
MAX3222EIDW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 85	MAX3222EI
MAX3222EIDWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3222EI
MAX3222EIDWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3222EI
MAX3222EIPWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP222EI
MAX3222EIPWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP222EI
MAX3222EIPWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP222EI
MAX3222EIPWRG4.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP222EI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

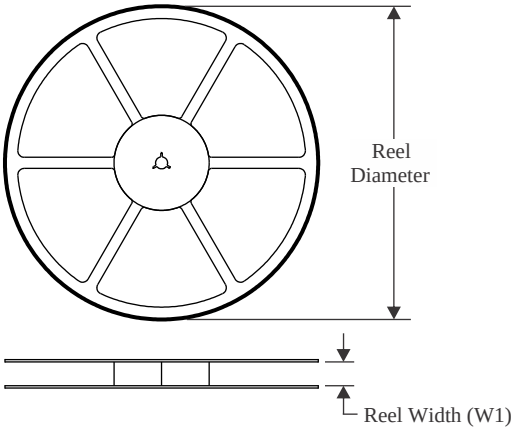
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

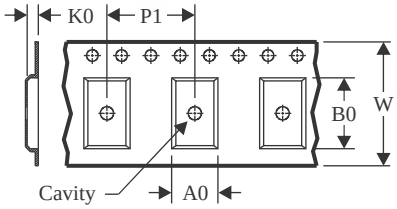
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

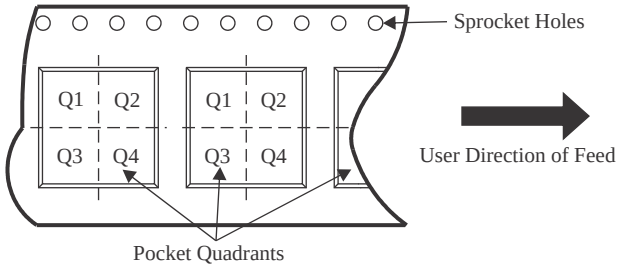


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

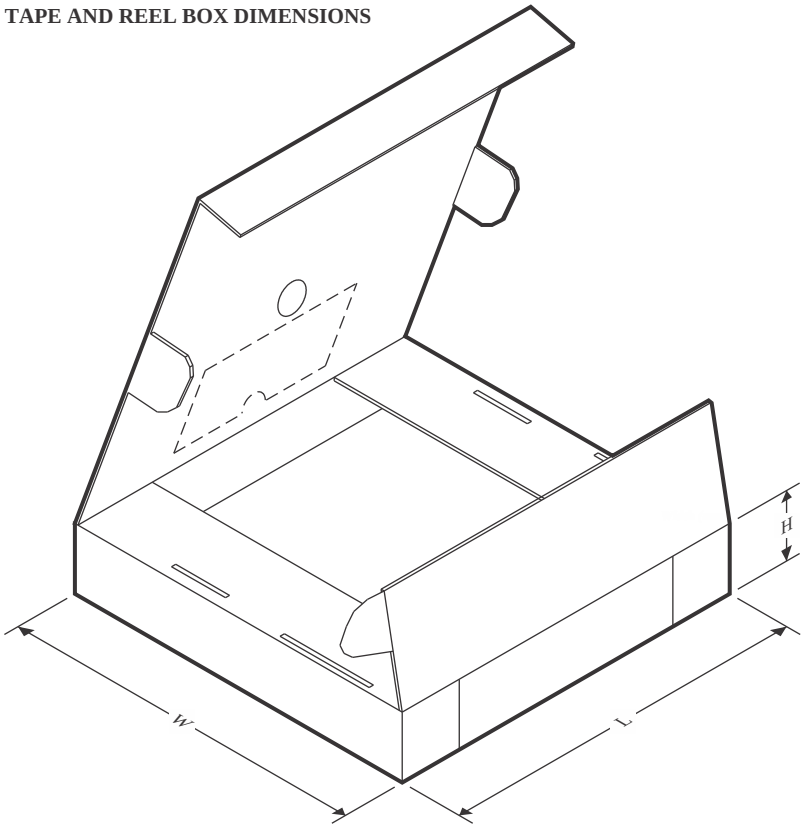
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

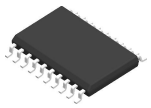
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3222ECDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3222ECDWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3222ECPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
MAX3222EIDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
MAX3222EIDBRG4	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
MAX3222EIDGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MAX3222EIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3222EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
MAX3222EIPWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3222ECDWR	SOIC	DW	20	2000	356.0	356.0	45.0
MAX3222ECDWRG4	SOIC	DW	20	2000	356.0	356.0	45.0
MAX3222ECPWR	TSSOP	PW	20	2000	353.0	353.0	32.0
MAX3222EIDBR	SSOP	DB	20	2000	353.0	353.0	32.0
MAX3222EIDBRG4	SSOP	DB	20	2000	353.0	353.0	32.0
MAX3222EIDGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
MAX3222EIDWR	SOIC	DW	20	2000	356.0	356.0	45.0
MAX3222EIPWR	TSSOP	PW	20	2000	353.0	353.0	32.0
MAX3222EIPWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0

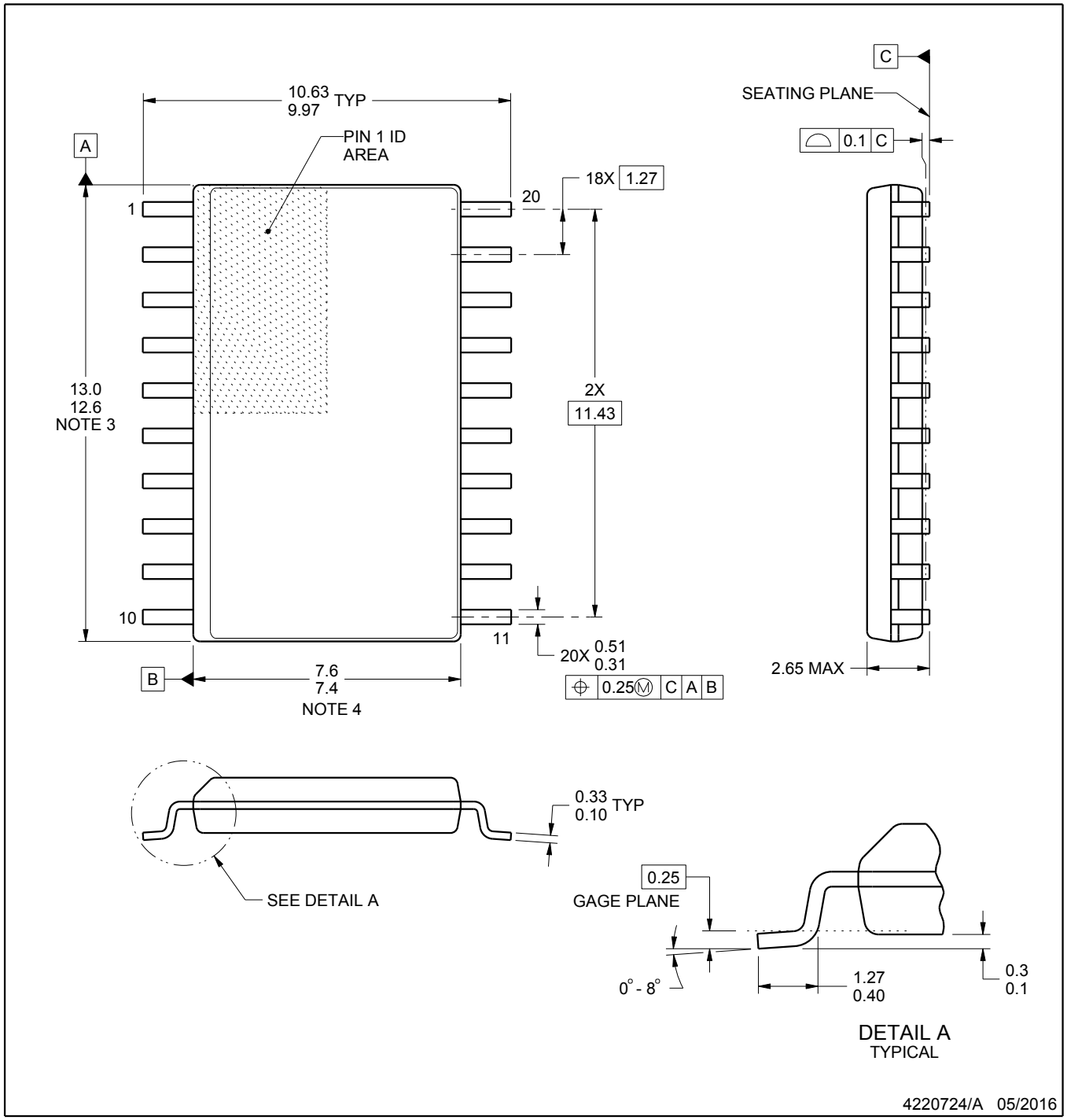


PACKAGE OUTLINE

DW0020A

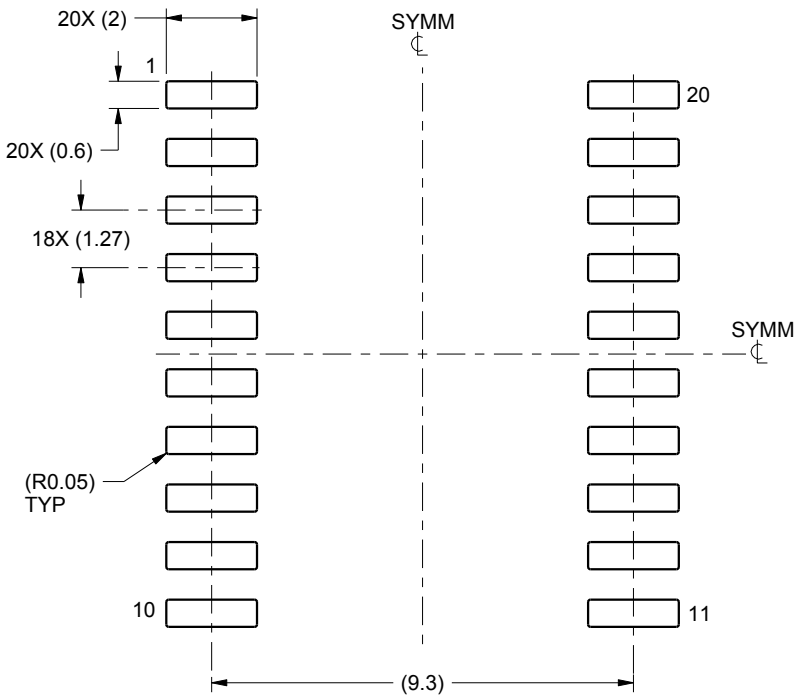
SOIC - 2.65 mm max height

SOIC

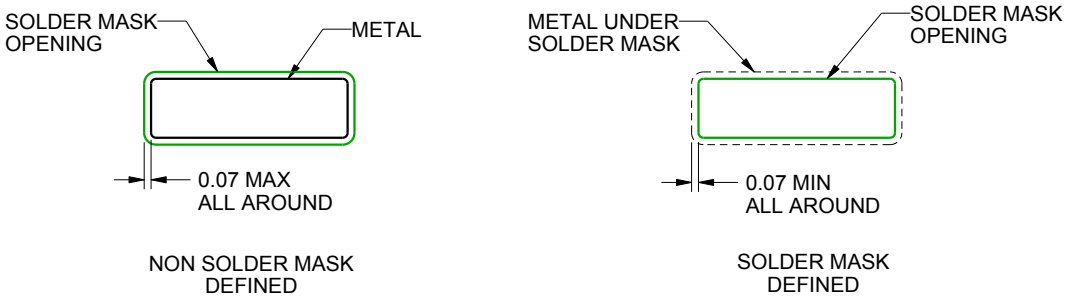


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

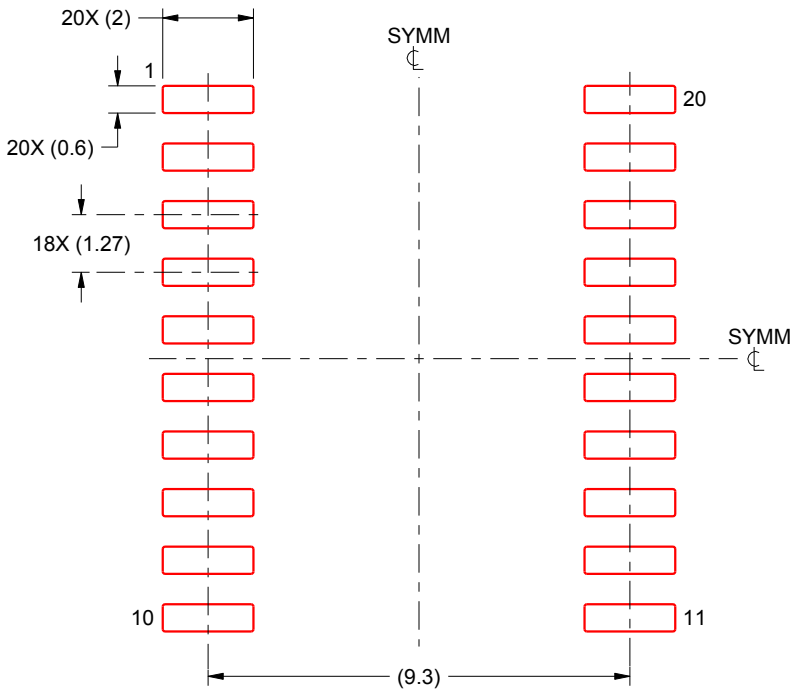


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

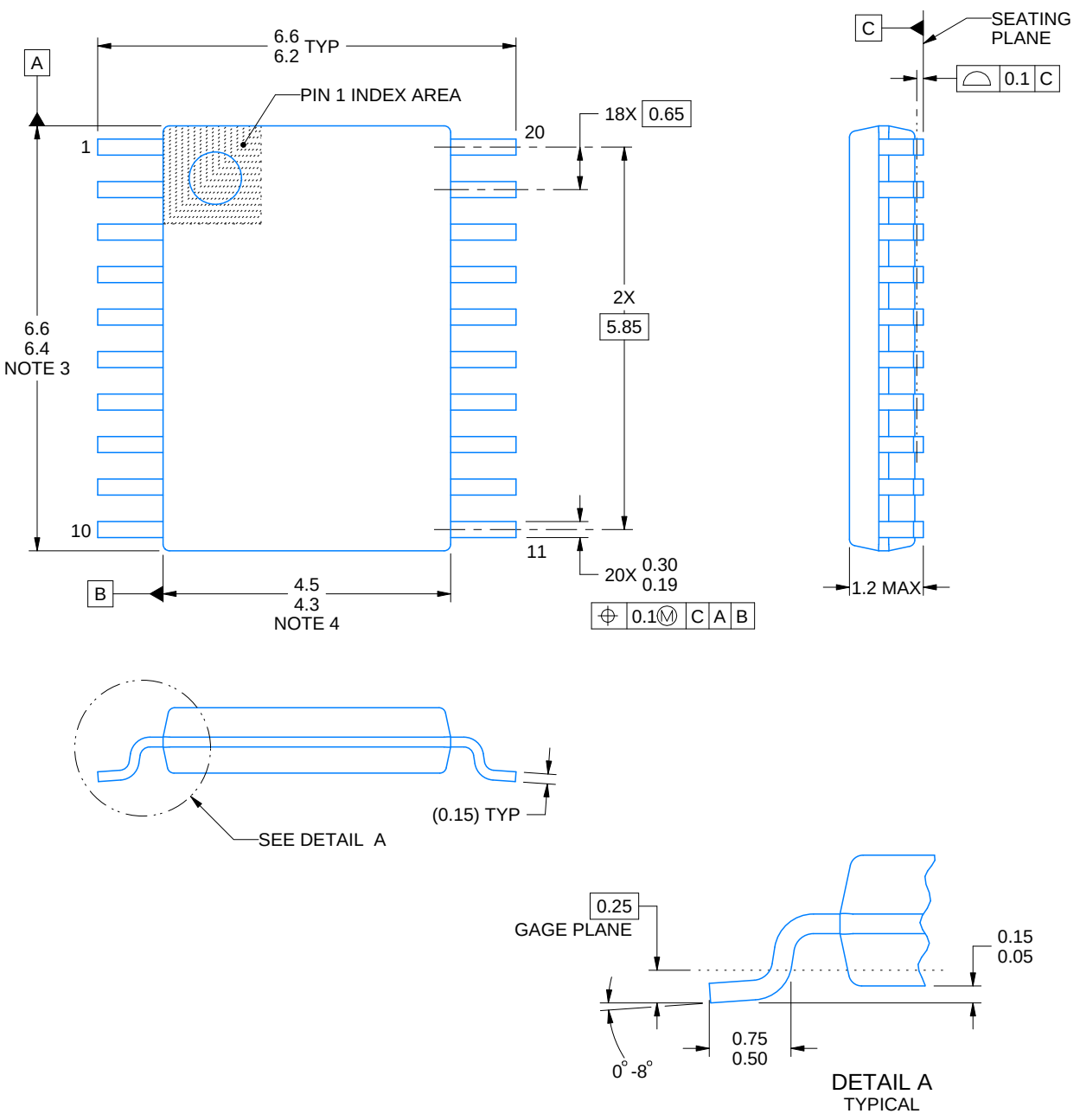
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

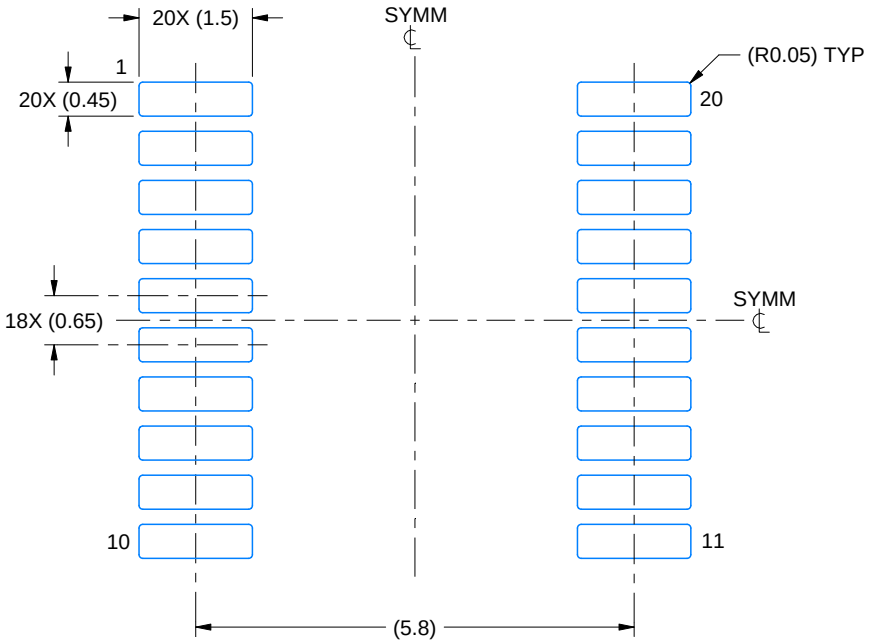
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

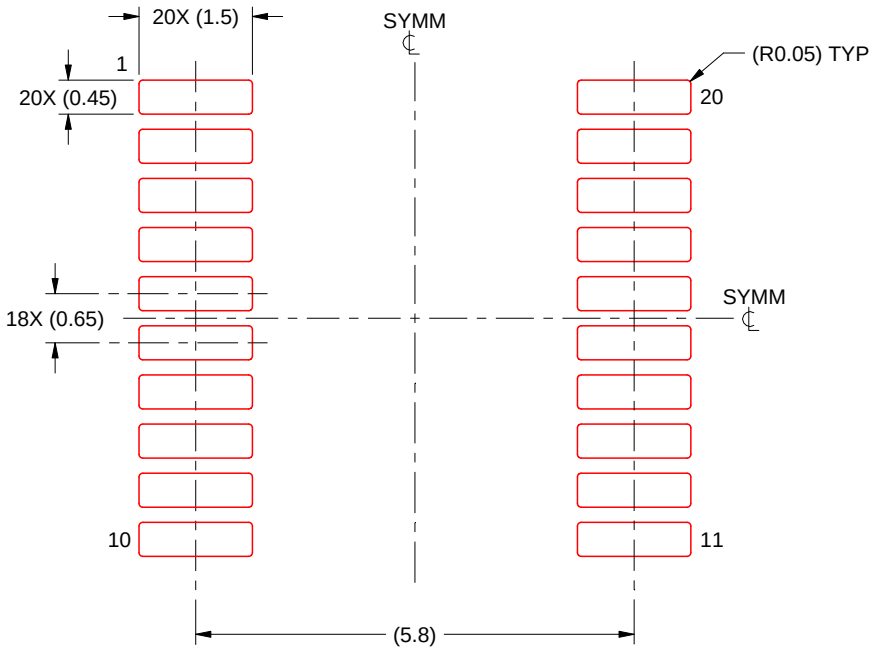


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

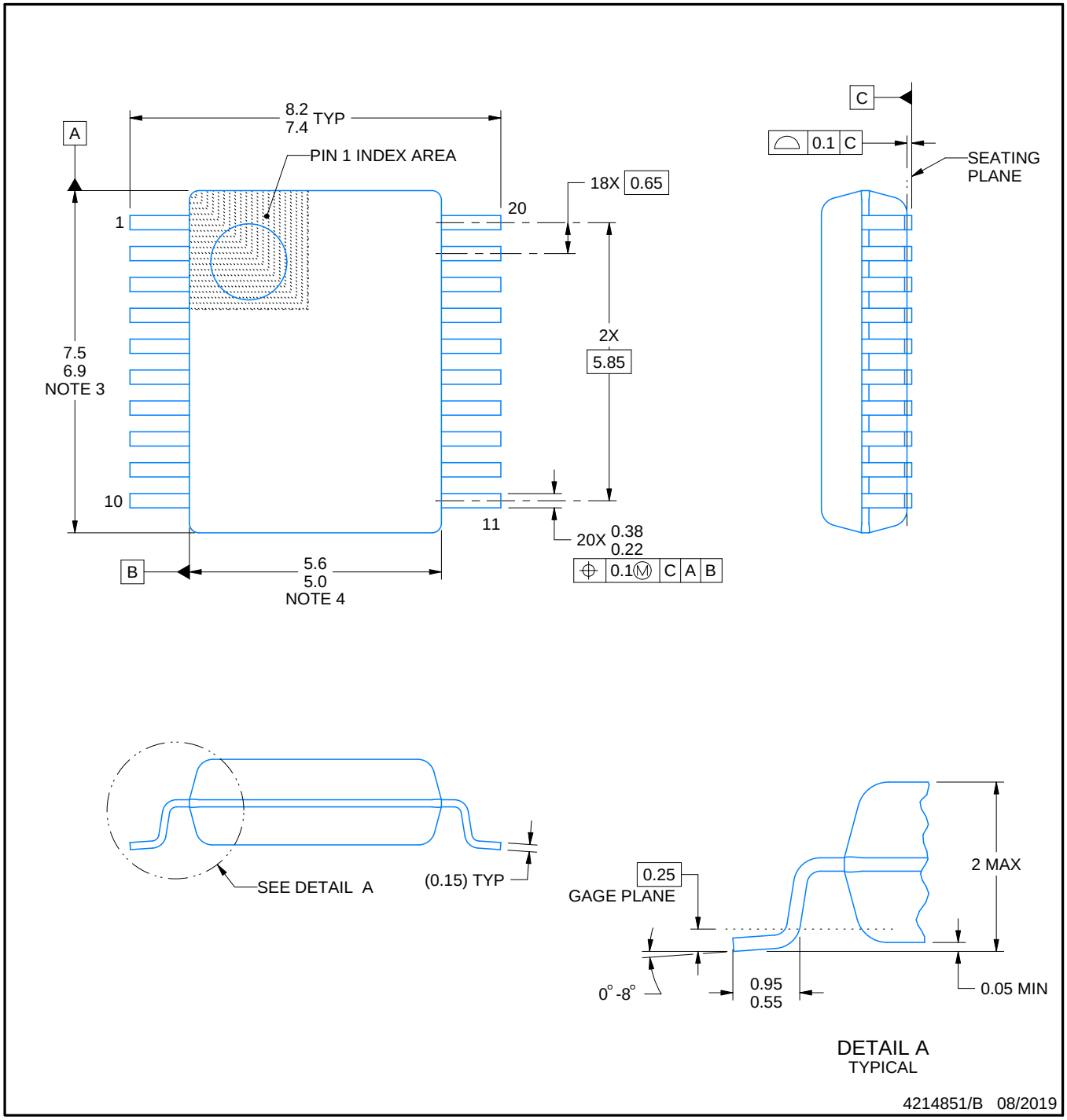
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0020A

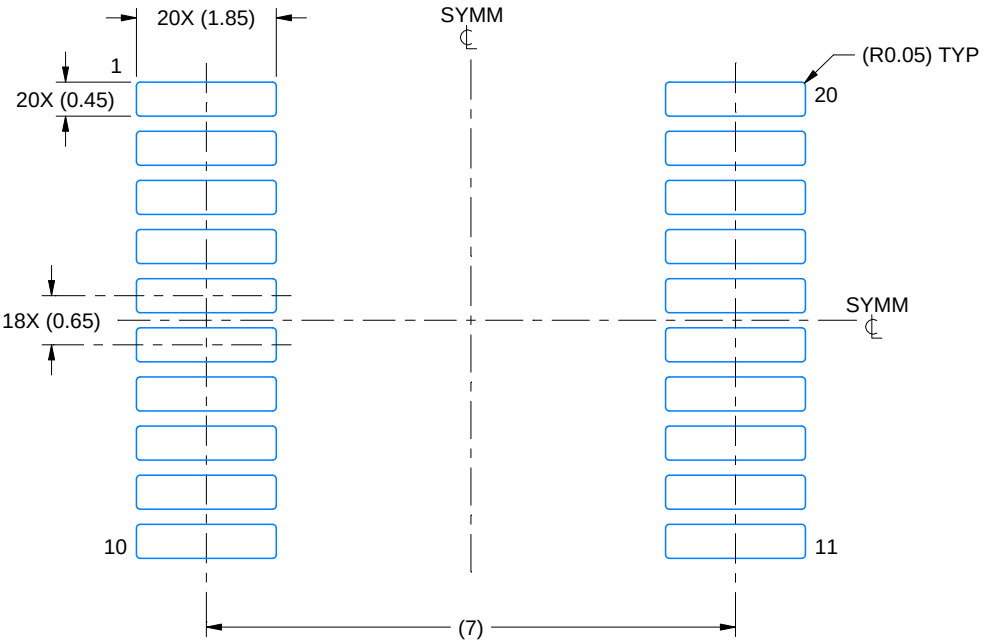
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

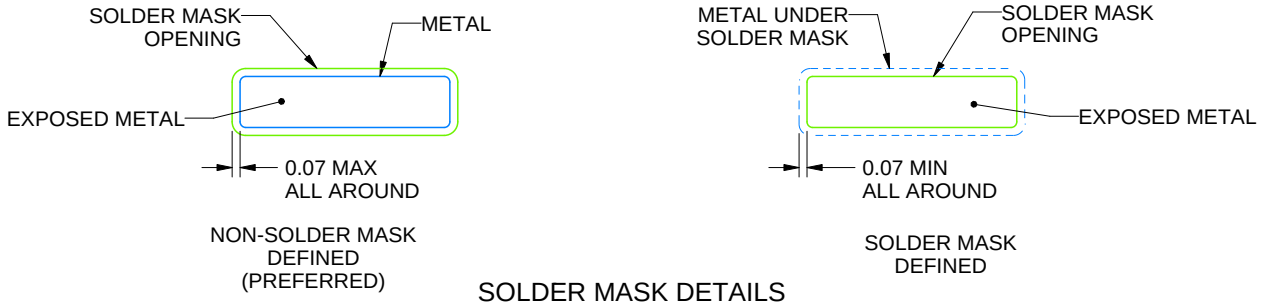


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

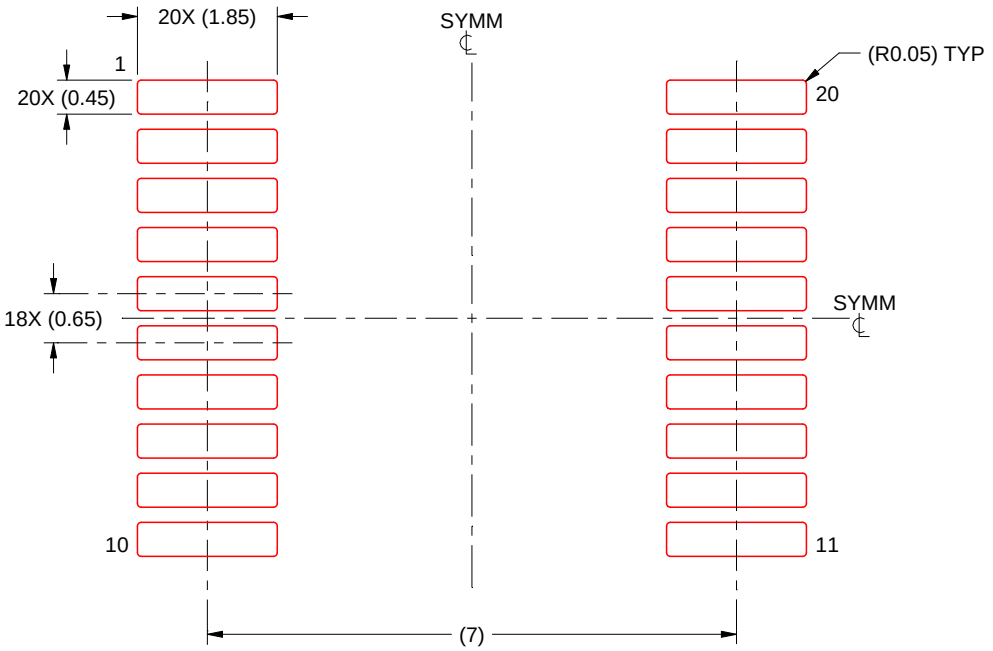
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

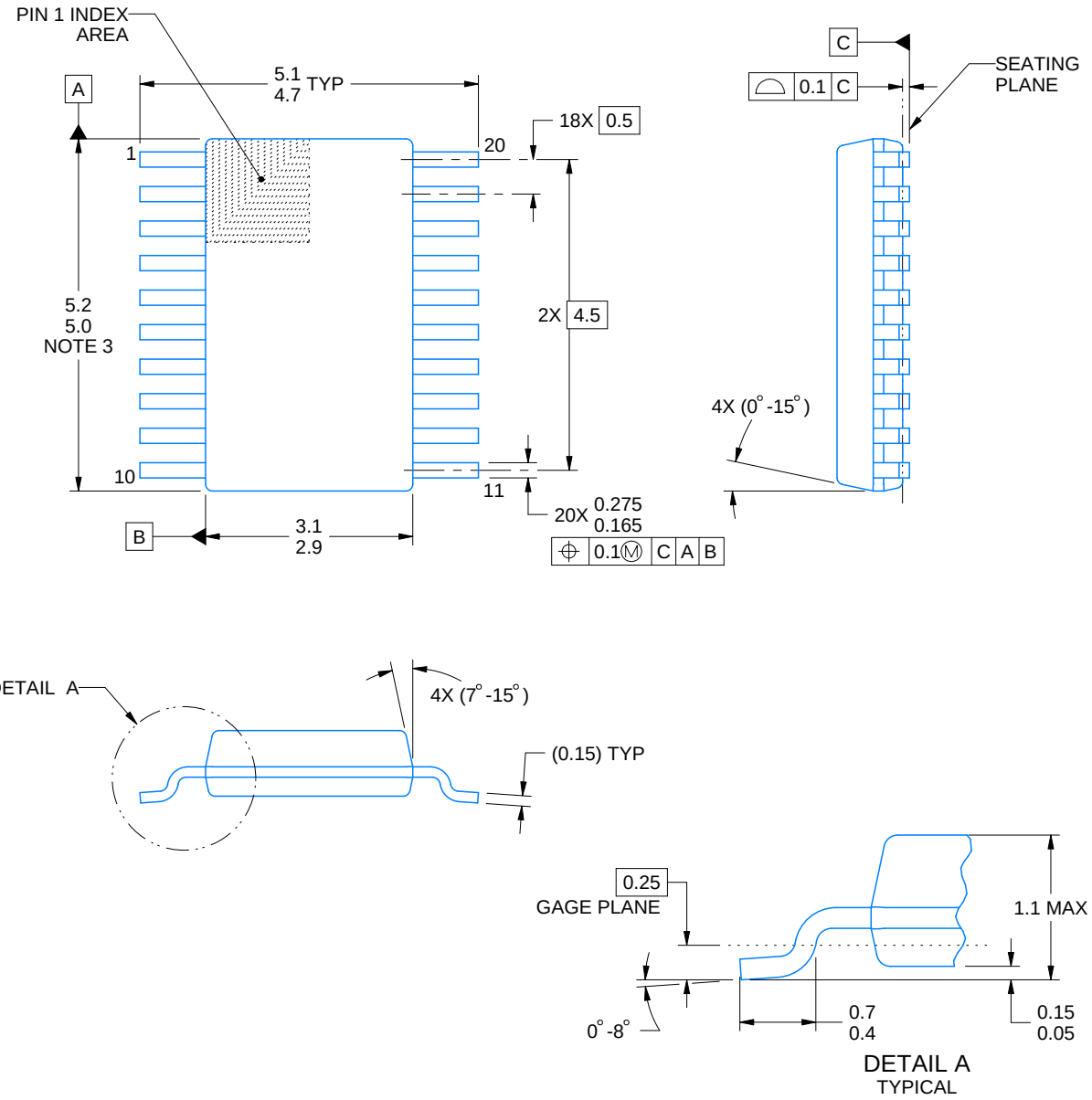
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

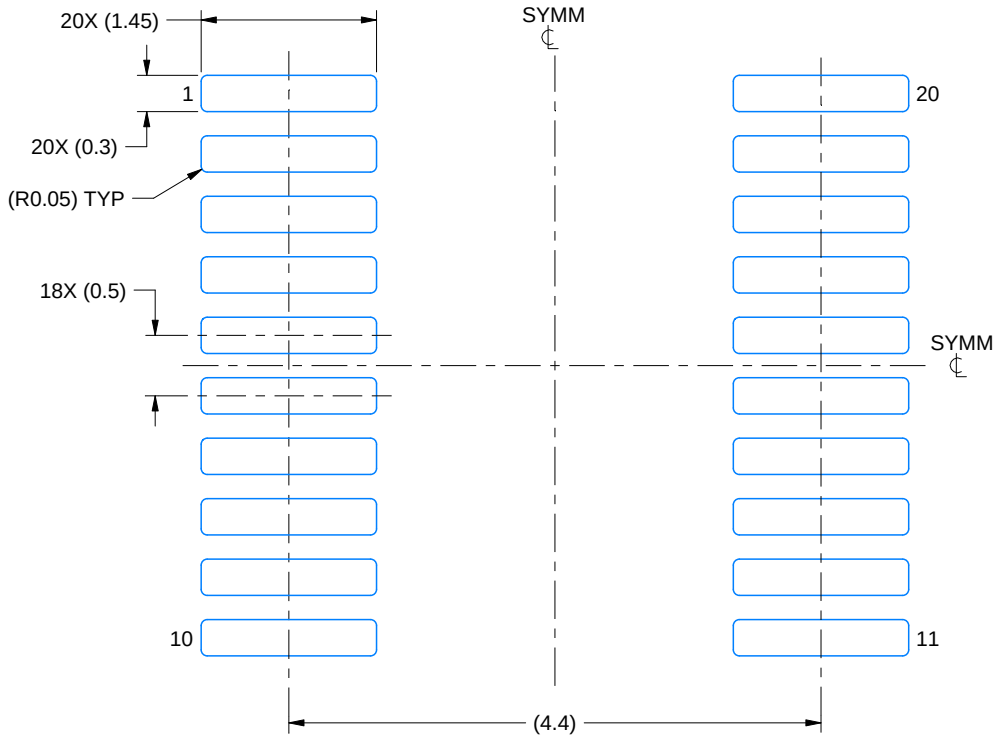
SMALL OUTLINE PACKAGE



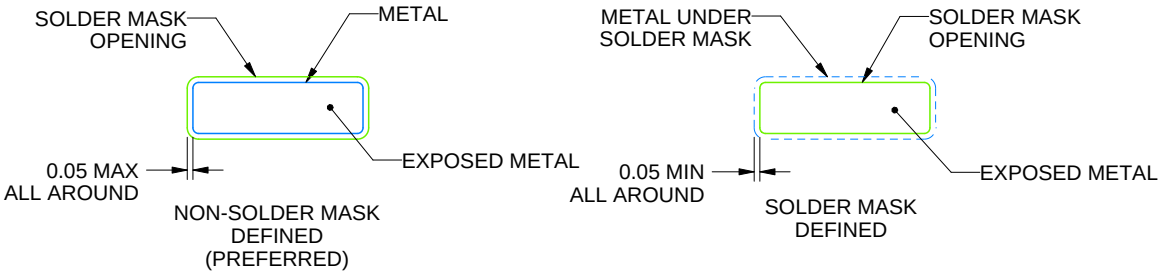
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

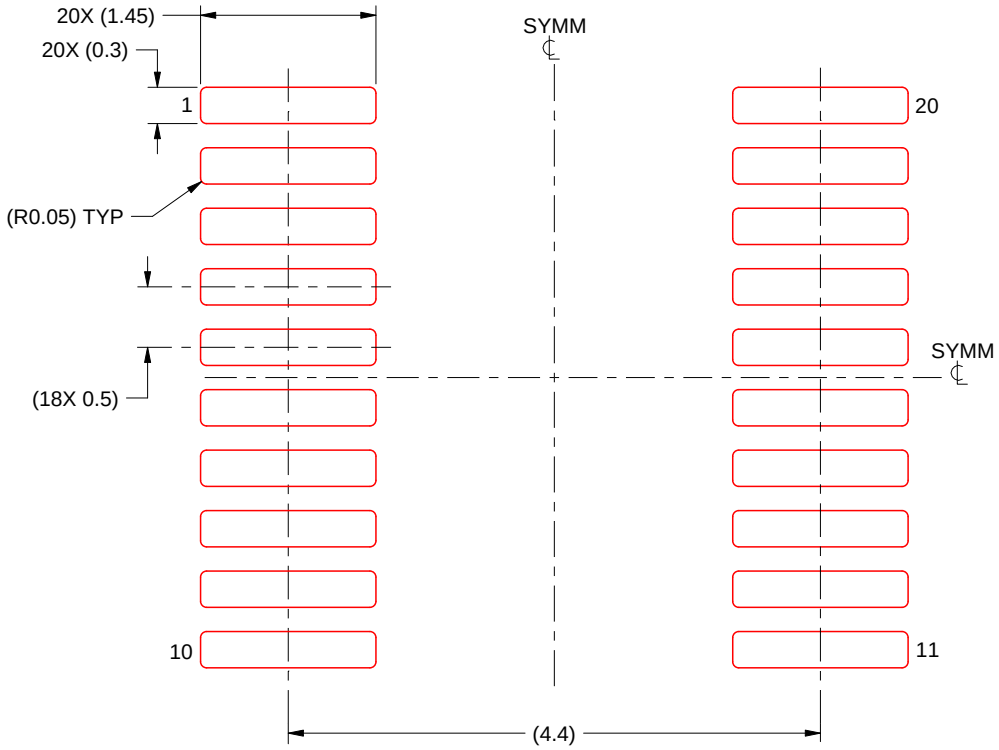


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月