TMUX111x 5V 低漏电流、1:1 (SPST)、4 通道精密开关

1 特性

- 宽电源电压范围：1.08V 至 5.5V
- 低漏电流：3pA
- 低电荷注入：-1.5pC
- 低导通电阻：2Ω
- 工作温度范围：-40°C 至 +125°C
- 兼容 1.8V 逻辑电平
- 失效防护逻辑
- 轨到轨运行
- 双向信号路径
- 先断后合开关
- ESD 保护 HBM：2000V

2 应用

- 采样保持电路
- 反馈增益开关
- 信号隔离
- 现场变送器
- 可编程逻辑控制器 (PLC)
- 工厂自动化和控制
- 超声波扫描仪
- 患者监护和诊断
- 心电图 (ECG)
- 数据采集系统 (DAQ)
- ATE 测试设备
- 电池测试设备
- 仪表：实验室、分析、便携
- 智能仪表：水表和燃气表
- 光纤网络
- 光学测试设备

3 说明

TMUX1111、TMUX1112 和 TMUX1113 是精密互补金属氧化物半导体 (CMOS) 器件，具有四个独立的可选 1:1、单极单投 (SPST) 开关。1.08V 至 5.5V 的宽工作电源电压范围使其适用于从医疗设备到工业系统的各种应用。该器件可在源极 (Sx) 和漏极 (Dx) 引脚上支持从 GND 到 V_{DD} 范围的双向模拟和数字信号。

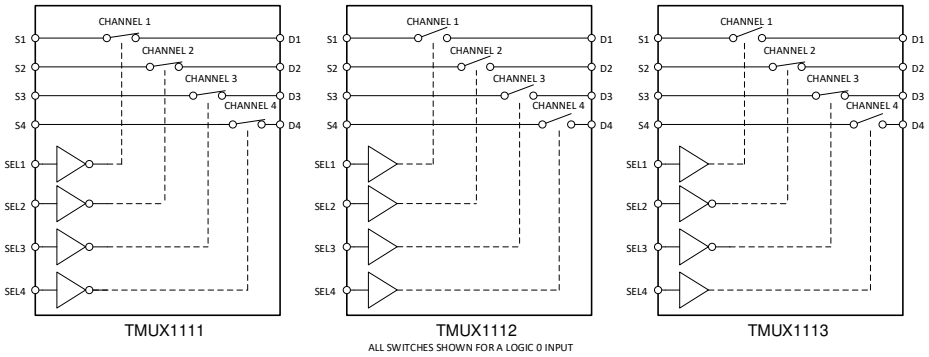
TMUX1111 的开关可通过逻辑 0 在恰当的逻辑控制输入下打开，而要打开 TMUX1112 中的开关，则需逻辑 1。TMUX1113 的四个通道通过两个支持逻辑 0 的开关分开，而另外两个开关则支持逻辑 1。TMUX1113 具有先断后合开关，因此该器件可用于交叉点开关应用。

TMUX111x 器件是精密开关和多路复用器器件系列中的一部分。此类器件具有非常低的导通和关断漏电流以及较低的电荷注入，因此可用于高精度测量应用。8nA 的低电源电流和小型封装选项使其可用于便携式应用。

器件信息

器件型号(1)	控制逻辑(1)	封装(2)
TMUX1111	低电平有效	PW（TSSOP，16） RSV（UQFN，16）
TMUX1112	高电平有效	
TMUX1113	混合	

(1) 请参阅器件比较。
(2) 有关更多信息，请参阅节 12。



TMUX111x 方框图

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

Table of Contents

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 Device Comparison Table ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics (V_{DD} = 5V ±10 %) ... 6
6.6 Electrical Characteristics (V_{DD} = 3.3V ±10 %) ... 8
6.7 Electrical Characteristics (V_{DD} = 1.8V ±10 %) ... 10
6.8 Electrical Characteristics (V_{DD} = 1.2V ±10 %) ... 12
6.9 Typical Characteristics ... 14
7 Parameter Measurement Information ... 17
7.1 On-resistance ... 17
7.2 Off-leakage current ... 17
7.3 On-leakage current ... 18
7.4 Transition time ... 18
7.5 Break-before-make ... 19
7.6 Charge injection ... 19
7.7 Off isolation ... 20
7.8 Channel-to-Channel Crosstalk ... 20
7.9 Bandwidth ... 21
8 Detailed Description ... 22
8.1 Overview ... 22
8.2 Functional Block Diagram ... 22
8.3 Feature Description ... 22
8.4 Device Functional Modes ... 24
8.5 Truth Tables ... 24
9 Application and Implementation ... 25
9.1 Application Information ... 25
9.2 Typical Application - Sample-and-Hold Circuit ... 25
9.3 Typical Application - Switched Gain Amplifier ... 27
9.4 Power Supply Recommendations ... 29
9.5 Layout ... 29
10 Device and Documentation Support ... 31
10.1 Documentation Support ... 31
10.2 接收文档更新通知 ... 31
10.3 支持资源 ... 31
10.4 Trademarks ... 31
10.5 静电放电警告 ... 31
10.6 术语表 ... 31
11 Revision History ... 31
12 Mechanical, Packaging, and Orderable Information ... 32

4 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX1111	Low-Leakage-Current, Precision, 4-Channel, 1:1 (SPST) Switches (Normally Closed)
TMUX1112	Low-Leakage-Current, Precision, 4-Channel, 1:1 (SPST) Switches (Normally Open)
TMUX1113	Low-Leakage-Current, Precision, 4-Channel, 1:1 (SPST) Switches (Dual Open + Dual Closed)

Copyright © 2024 Texas Instruments Incorporated

5 Pin Configuration and Functions

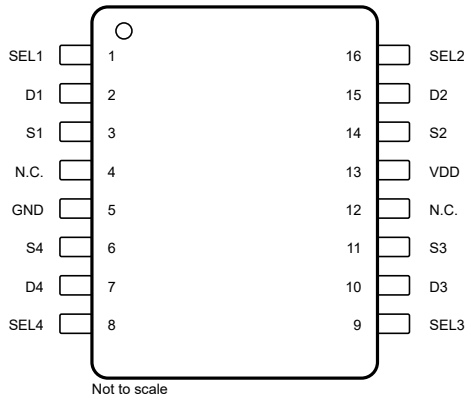


图 5-1. PW Package, 16-Pin TSSOP (Top View)

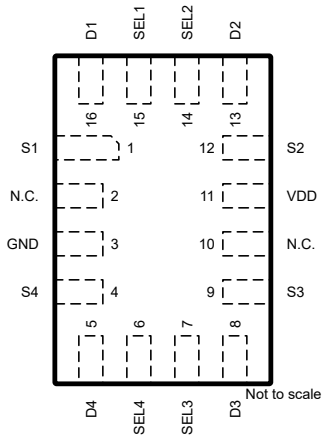


图 5-2. RSV Package, 16-Pin UQFN (Top View)

表 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	TSSOP	UQFN		
SEL1	1	15	I	Logic control input 1. Controls channel 1 state as shown in 节 8.5.
D1	2	16	I/O	Drain pin 1. Can be an input or output.
S1	3	1	I/O	Source pin 1. Can be an input or output.
N.C.	4	2	—	No internal connection.
GND	5	3	P	Ground (0 V) reference
S4	6	4	I/O	Source pin 4. Can be an input or output.
D4	7	5	I/O	Drain pin 4. Can be an input or output.
SEL4	8	6	I	Logic control input 4. Controls channel 4 state as shown in 节 8.5.
SEL3	9	7	I	Logic control input 3. Controls channel 3 state as shown in 节 8.5.
D3	10	8	I/O	Drain pin 3. Can be an input or output.
S3	11	9	I/O	Source pin 3. Can be an input or output.
N.C.	12	10	—	No internal connection.
VDD	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μF to 10 μF between V_{DD} and GND.
S2	14	12	I/O	Source pin 2. Can be an input or output.
D2	15	13	I/O	Drain pin 2. Can be an input or output.
SEL2	16	14	I	Logic control input 2. Controls channel 2 state as shown in 节 8.5.

(1) I = input, O = output, I/O = input and output, P = power

Copyright © 2024 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	– 0.5	6	V
V_{SEL}	Logic control input pin voltage (SELx)	– 0.5	6	V
I_{SEL}	Logic control input pin current (SELx)	– 30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	– 0.5	V_{DD}+0.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)	I_{DC} ± 10 %(4)	I_{DC} ± 10 %(4)	mA
I_S or $I_{D\ (PEAK)}$	Source and drain peak current: (1 ms period max, 10% duty cycle maximum) (Sx, D)	I_{peak} ± 10 %(4)	I_{peak} ± 10 %(4)	mA
T_{stg}	Storage temperature	– 65	150	°C
P_{tot}	Total power dissipation(5) (6)		500	mW
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Refer to Recommended Operating Conditions for I_{DC} and I_{Peak} ratings.
(5) For PW package: P_{tot} derates linearly above TA=88°C by 8.08mW/°C
(6) For QFN package: P_{tot} derates linearly above TA=76°C by 6.81mW/°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Positive power supply voltage		1.08		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, Dx)		0		V_{DD}	V
V_{SEL}	Logic control input pin voltage (SELx)		0		5.5	V
T_A	Ambient temperature		– 40		125	°C
I_{DC}	Continuous current through switch	T_j = 25°C		150		mA
		T_j = 85°C		120		mA
		T_j = 125°C		60		mA
		T_j = 130°C		50		mA
I_{peak}	Peak current through switch(1 ms period max, 10% duty cycle maximum)	T_j = 25°C		300		mA
		T_j = 85°C		300		mA
		T_j = 125°C		180		mA
		T_j = 130°C		160		mA

Copyright © 2024 Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC[1]		TMUX1111 / TMUX1112 / TMUX1113		UNIT
		PW (TSSOP)	RSV (QFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.7	146.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.8	83.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.9	75.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.8	9.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.3	73.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Copyright © 2024 Texas Instruments Incorporated

6.5 Electrical Characteristics (V_{DD} = 5V ±10 %)

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to On-resistance	25°C		2	4	Ω
			–40°C to +85°C			4.5	Ω
			–40°C to +125°C			4.9	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to On-resistance	25°C		0.13		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to On-resistance	25°C		0.85		Ω
			–40°C to +85°C			1.6	Ω
			–40°C to +125°C			1.6	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 5V Switch Off V_D = 4.5V / 1.5V V_S = 1.5V / 4.5V Refer to Off-leakage current	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 5V Switch Off V_D = 4.5V / 1.5V V_S = 1.5V / 4.5V Refer to Off-leakage current	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5V Switch On V_D = V_S = 2.5V Refer to On-leakage current	25°C	–0.025	±0.003	0.025	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.95		0.95	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5V Switch On V_D = V_S = 4.5V / 1.5V Refer to On-leakage current	25°C	–0.1	±0.01	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SELx)							
V_{IH}	Input logic high		–40°C to +125°C	1.49		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.87	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.06	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.008		µA
			–40°C to +125°C			1	µA

Copyright © 2024 Texas Instruments Incorporated

6.5 Electrical Characteristics (V_{DD} = 5V ±10 %)（续）

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 3V R_L = 200 Ω, C_L = 15pF Refer to Transition time	25°C		12		ns
			–40°C to +85°C			18	ns
			–40°C to +125°C			19	ns
t_{OPEN} (BBM)	Break before make time (TMUX1113 Only)	V_S = 3V R_L = 200 Ω, C_L = 15pF Refer to Break-before-make	25°C		8		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = 1V R_S = 0 Ω, C_L = 1nF Refer to Charge injection	25°C		–1.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5pF f = 1MHz Refer to Off isolation	25°C		–62		dB
		R_L = 50 Ω, C_L = 5pF f = 10MHz Refer to Off isolation	25°C		–40		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5pF f = 1MHz Refer to Channel-to Channel Crosstalk	25°C		–100		dB
		R_L = 50 Ω, C_L = 5pF f = 10MHz Refer to Channel-to Channel Crosstalk	25°C		–90		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5pF Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		7		pF
C_{DOFF}	Drain off capacitance	f = 1MHz	25°C		10		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		17		pF

(1) When V_S is 4.5V, V_D is 1.5V or when V_S is 1.5V, V_D is 4.5V.

Copyright © 2024 Texas Instruments Incorporated

6.6 Electrical Characteristics (V_{DD} = 3.3V ±10 %)

at T_A = 25°C, V_{DD} = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to On-resistance	25°C		3.7	8.8	Ω
			–40°C to +85°C			9.5	Ω
			–40°C to +125°C			9.8	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to On-resistance	25°C		0.13		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to On-resistance	25°C		1.9		Ω
			–40°C to +85°C		2		Ω
			–40°C to +125°C		2.2		Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 3.3V Switch Off V_D = 3V / 1V V_S = 1V / 3V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 3.3V Switch Off V_D = 3V / 1V V_S = 1V / 3V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 3.3V Switch On V_D = V_S = 3V / 1V Refer to On-leakage current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SELx)							
V_{IH}	Input logic high		–40°C to +125°C	1.35		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.8	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.005		µA
			–40°C to +125°C			1	µA

Copyright © 2024 Texas Instruments Incorporated

6.6 Electrical Characteristics (V_{DD} = 3.3V ±10 %) （续）

at T_A = 25°C, V_{DD} = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 2V R_L = 200 Ω, C_L = 15pF Refer to Transition time	25°C		14		ns
			–40°C to +85°C			20	ns
			–40°C to +125°C			22	ns
t_{OPEN} (BBM)	Break before make time (TMUX1113 Only)	V_S = 2V R_L = 200 Ω, C_L = 15pF Refer to Break-before-make	25°C		9		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = 1V R_S = 0 Ω, C_L = 1nF Refer to Charge injection	25°C		–1.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5pF f = 1MHz Refer to Off isolation	25°C		–62		dB
		R_L = 50 Ω, C_L = 5pF f = 10MHz Refer to Off Isolation	25°C		–40		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5pF f = 1MHz Refer to Channel-to-Channel Crosstalk	25°C		–100		dB
		R_L = 50 Ω, C_L = 5pF f = 10MHz Refer to Channel-to-Channel Crosstalk	25°C		–90		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5pF Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		7		pF
C_{DOFF}	Drain off capacitance	f = 1MHz	25°C		10		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		17		pF

(1) When V_S is 3V, V_D is 1V or when V_S is 1V, V_D is 3V.

Copyright © 2024 Texas Instruments Incorporated

6.7 Electrical Characteristics (V_{DD} = 1.8V ±10 %)

at T_A = 25°C, V_{DD} = 1.8V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to On-resistance	25°C		40		Ω
			–40°C to +85°C			80	Ω
			–40°C to +125°C			80	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to On-resistance	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.98V Switch Off V_D = 1.62V / 1V V_S = 1V / 1.62V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 1.98V Switch Off V_D = 1.62V / 1V V_S = 1V / 1.62V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.98V Switch On V_D = V_S = 1.62V / 1V Refer to On-leakage current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SELx)							
V_{IH}	Input logic high		–40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.001		µA
			–40°C to +125°C			0.85	µA

Copyright © 2024 Texas Instruments Incorporated

6.7 Electrical Characteristics (V_{DD} = 1.8V ±10 %) （续）

at T_A = 25°C, V_{DD} = 1.8V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1V R_L = 200 Ω, C_L = 15pF Refer to Transition time	25°C		25		ns
			–40°C to +85°C			44	ns
			–40°C to +125°C			44	ns
t_{OPEN} (BBM)	Break before make time (TMUX1113 Only)	V_S = 1V R_L = 200 Ω, C_L = 15pF Refer to Break-before-make	25°C		17		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = 1V R_S = 0 Ω, C_L = 1nF Refer to Charge injection	25°C		–0.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5pF f = 1MHz Refer to Off isolation	25°C		–62		dB
		R_L = 50 Ω, C_L = 5pF f = 10MHz Refer to Off isolation	25°C		–40		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5pF f = 1MHz Refer to Channel-to-Channel Crosstalk	25°C		–100		dB
		R_L = 50 Ω, C_L = 5pF f = 10MHz Refer to Channel-to-Channel Crosstalk	25°C		–90		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5pF Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		7		pF
C_{DOFF}	Drain off capacitance	f = 1MHz	25°C		10		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		17		pF

(1) When V_S is 1.62V, V_D is 1V or when V_S is 1V, V_D is 1.62V.

Copyright © 2024 Texas Instruments Incorporated

6.8 Electrical Characteristics (V_{DD} = 1.2V ±10 %)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to On-resistance	25°C		70		Ω
			–40°C to +85°C			105	Ω
			–40°C to +125°C			105	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to On-resistance	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.32V Switch Off V_D = 1V / 0.8V V_S = 0.8V / 1V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 1.32V Switch Off V_D = 1V / 0.8V V_S = 0.8V / 1V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.32V Switch On V_D = V_S = 1V / 0.8V Refer to On-leakage current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SELx)							
V_{IH}	Input logic high		–40°C to +125°C	0.96		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.36	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.001		µA
			–40°C to +125°C			0.7	µA

Copyright © 2024 Texas Instruments Incorporated

6.8 Electrical Characteristics (V_{DD} = 1.2V ±10 %) （续）

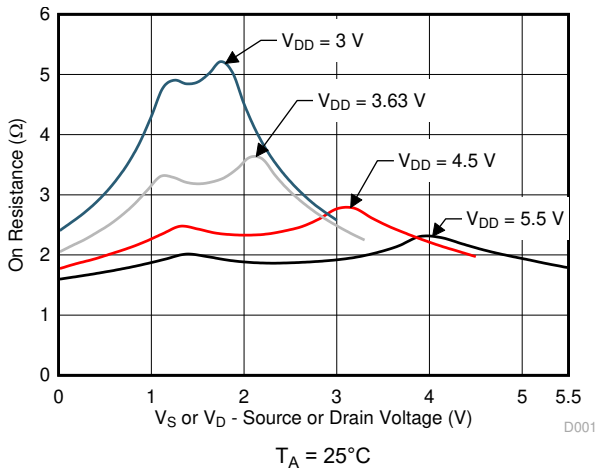
PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1V R_L = 200 Ω, C_L = 15pF Refer to Transition time	25°C		55		ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			190	ns
t_{OPEN} (BBM)	Break before make time (TMUX1113 Only)	V_S = 1V R_L = 200 Ω, C_L = 15pF Refer to Break-before-make	25°C		28		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = 1V R_S = 0 Ω, C_L = 1nF Refer to Charge injection	25°C		–0.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5pF f = 1MHz Refer to Off isolation	25°C		–62		dB
		R_L = 50 Ω, C_L = 5pF f = 10MHz Refer to Off isolation	25°C		–40		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5pF f = 1MHz Refer to Channel-to-Channel Crosstalk	25°C		–100		dB
		R_L = 50 Ω, C_L = 5pF f = 10MHz Refer to Channel-to-Channel Crosstalk	25°C		–90		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5pF Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		8		pF
C_{DOFF}	Drain off capacitance	f = 1MHz	25°C		11		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		18		pF

(1) When V_S is 1V, V_D is 0.8V or when V_S is 0.8V, V_D is 1V.

Copyright © 2024 Texas Instruments Incorporated

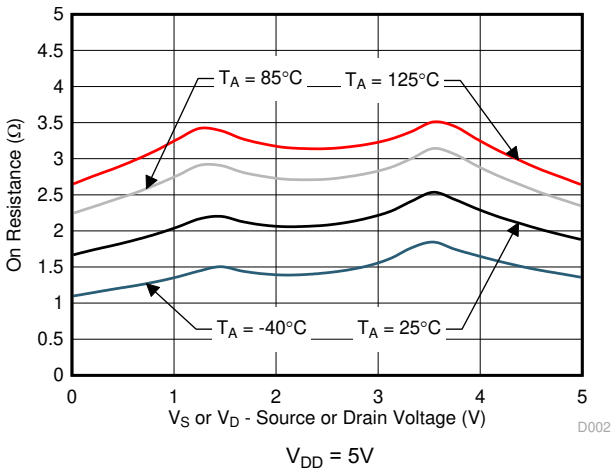
6.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



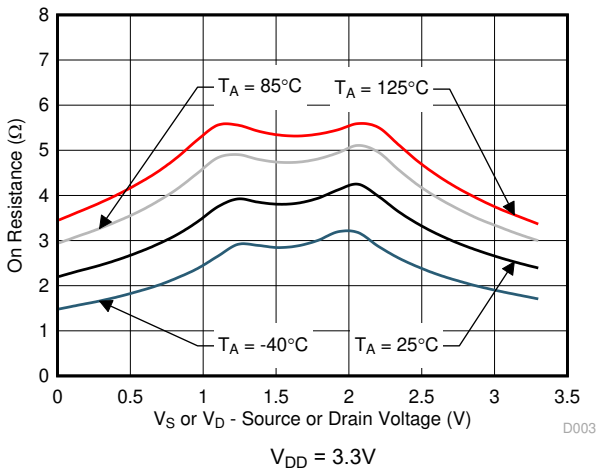
T_A = 25°C

图 6-1. On-Resistance vs Source or Drain Voltage



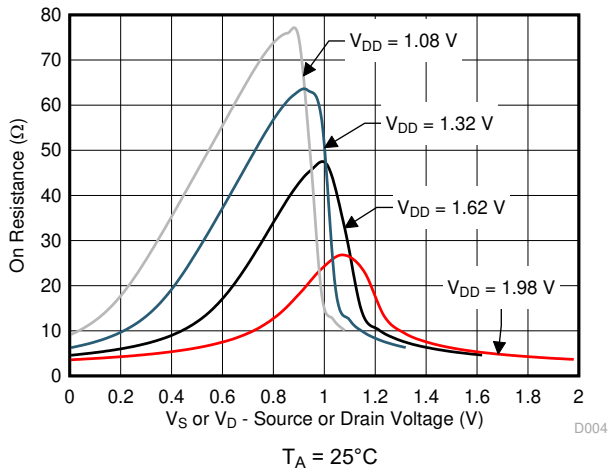
V_{DD} = 5V

图 6-2. On-Resistance vs Temperature



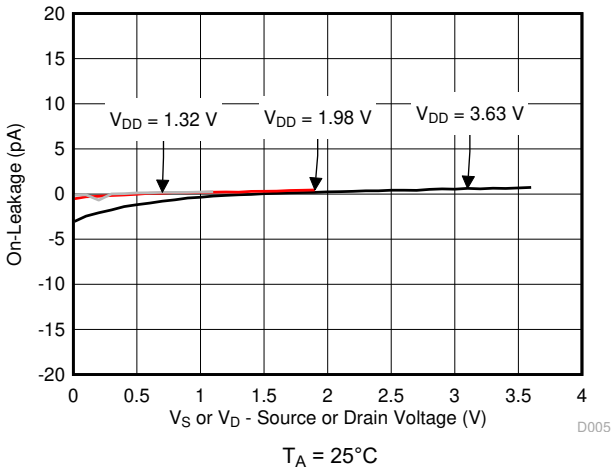
V_{DD} = 3.3V

图 6-3. On-Resistance vs Temperature



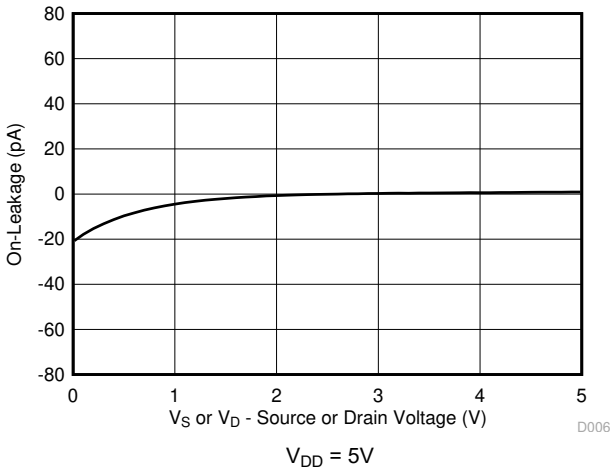
T_A = 25°C

图 6-4. On-Resistance vs Source or Drain Voltage



T_A = 25°C

图 6-5. On-Leakage vs Source or Drain Voltage



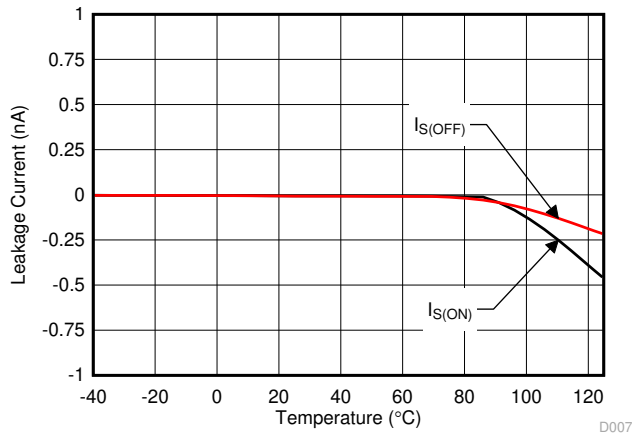
V_{DD} = 5V

图 6-6. On-Leakage vs Source or Drain Voltage

Copyright © 2024 Texas Instruments Incorporated

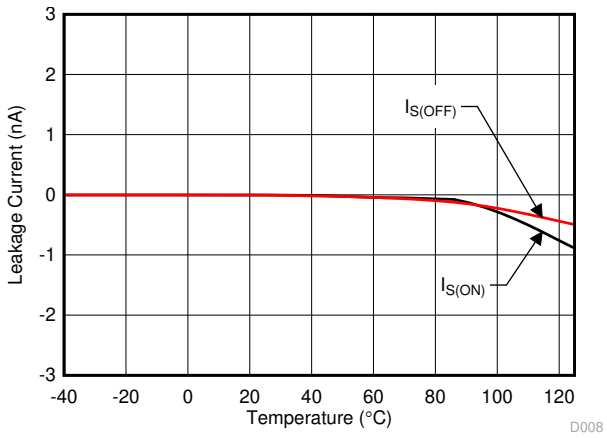
6.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



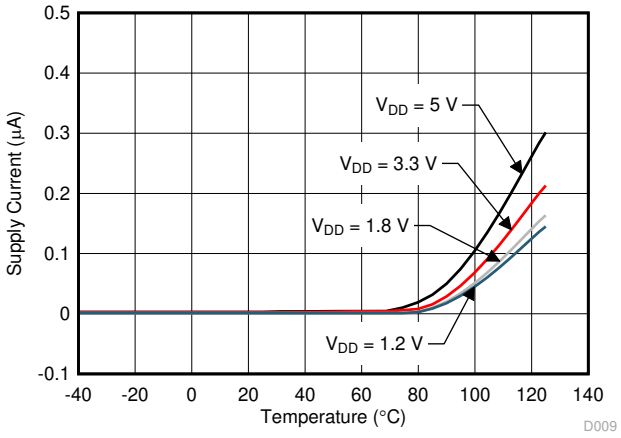
V_{DD} = 3.3V

图 6-7. Leakage Current vs Temperature



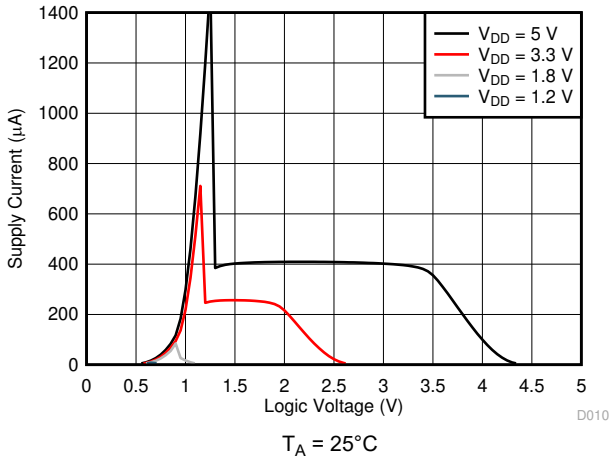
V_{DD} = 5V

图 6-8. Leakage Current vs Temperature



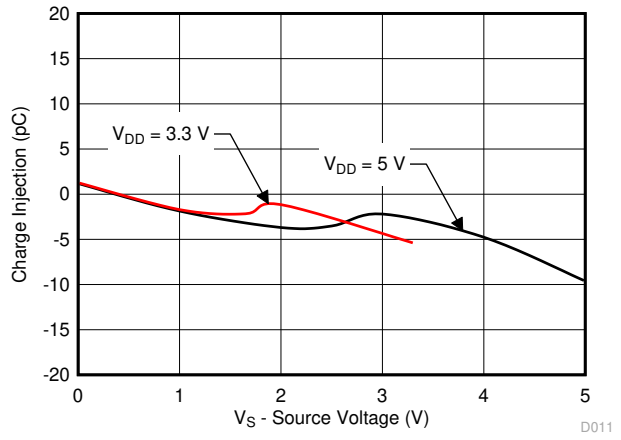
V_{SEL} = 5.5V

图 6-9. Supply Current vs Temperature



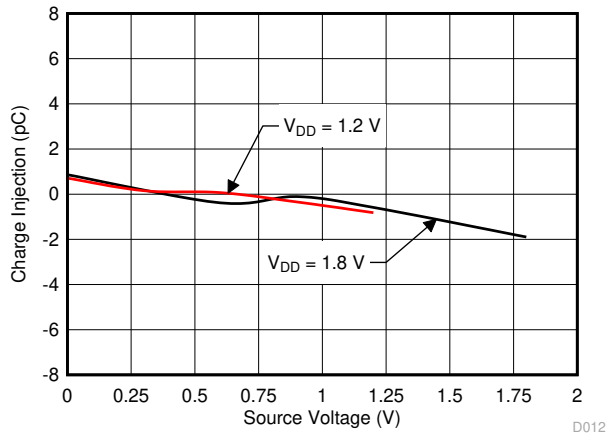
T_A = 25°C

图 6-10. Supply Current vs Logic Voltage



T_A = -40°C to 125°C

图 6-11. Charge Injection vs Source Voltage



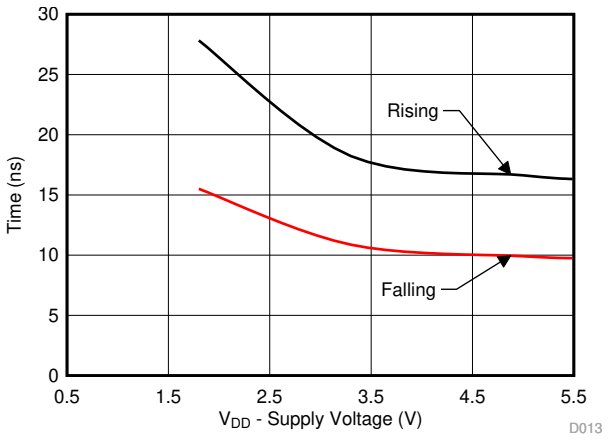
T_A = -40°C to 125°C

图 6-12. Charge Injection vs Source Voltage

Copyright © 2024 Texas Instruments Incorporated

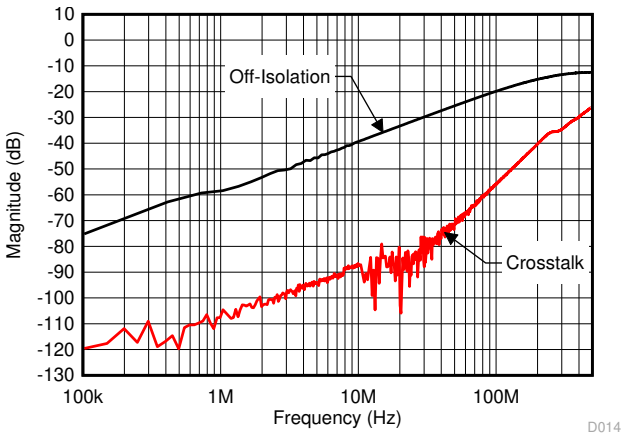
6.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



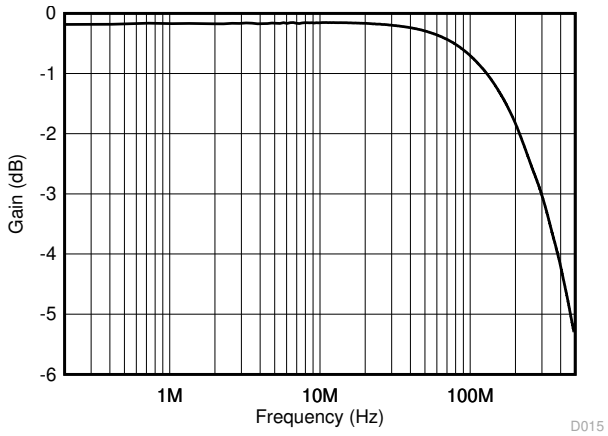
T_A = -40°C to +125°C

图 6-13. Output $T_{TRANSITION}$ vs Supply Voltage



T_A = -40°C to +125°C

图 6-14. Xtalk and Off-Isolation vs Frequency



T_A = -40°C to +125°C

图 6-15. On Response vs Frequency

Copyright © 2024 Texas Instruments Incorporated

7 Parameter Measurement Information

7.1 On-resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 图 7-1. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

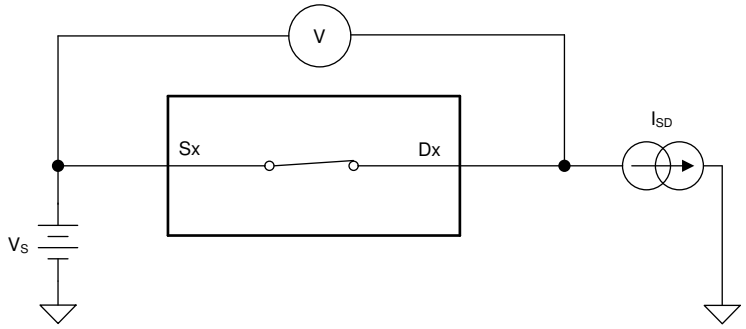


图 7-1. On-Resistance Measurement Setup

7.2 Off-leakage current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in 图 7-2.

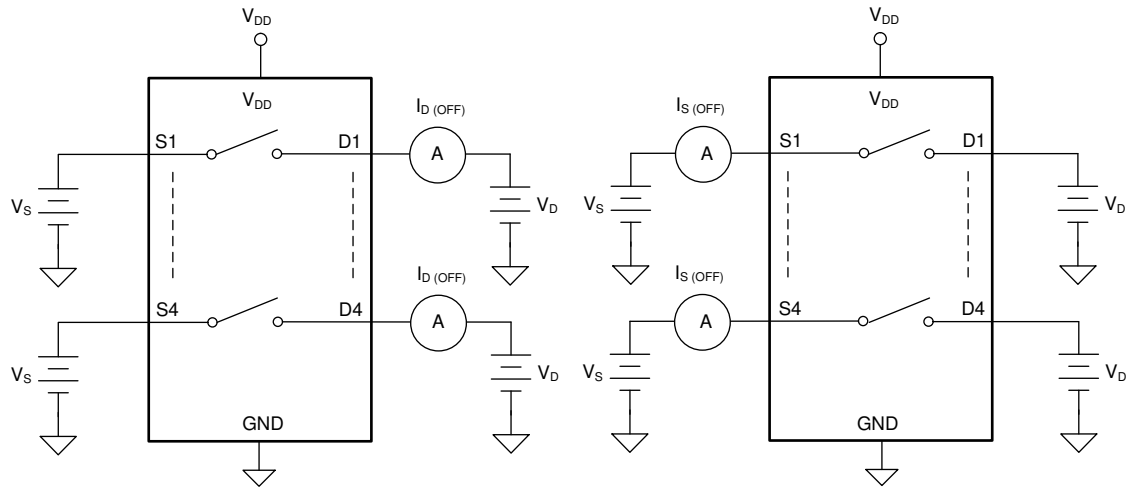


图 7-2. Off-Leakage Measurement Setup

7.3 On-leakage current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

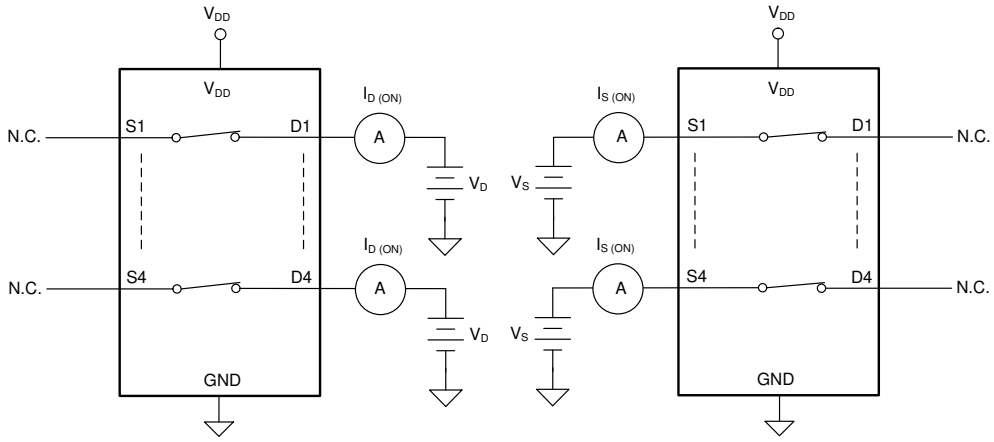


图 7-3. On-Leakage Measurement Setup

7.4 Transition time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

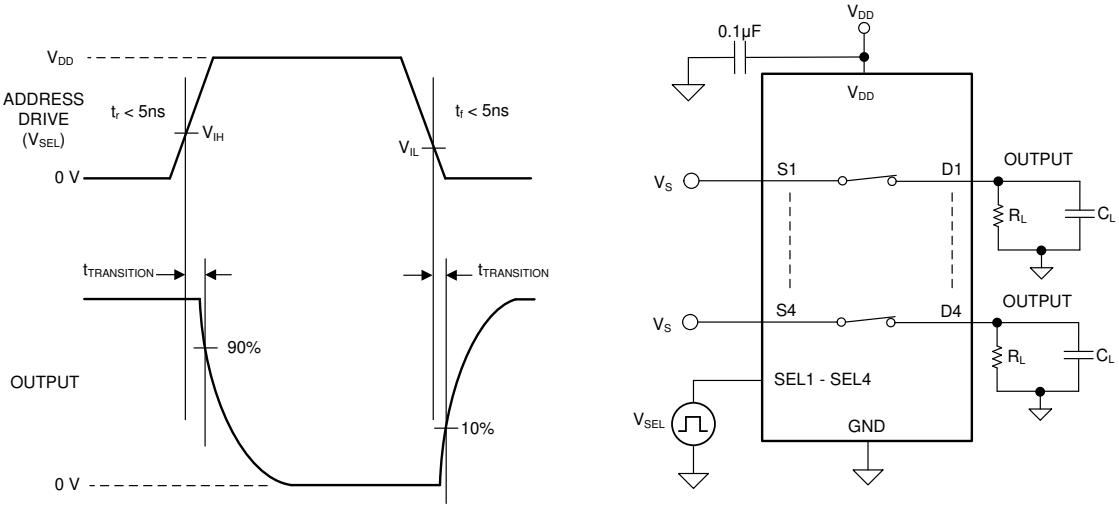


图 7-4. Transition-Time Measurement Setup

Copyright © 2024 Texas Instruments Incorporated

7.5 Break-before-make

The TMUX1113 has break-before-make delay which allows the device to be used in cross-point switching application. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 7-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

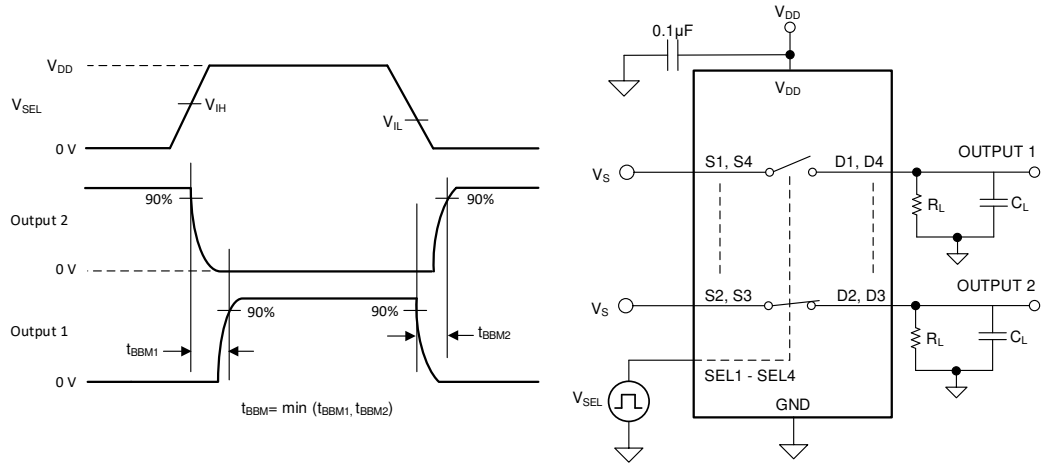


图 7-5. Break-Before-Make Delay Measurement Setup

7.6 Charge injection

The TMUX111x devices have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. 图 7-6 shows the setup used to measure charge injection from source (Sx) to drain (Dx).

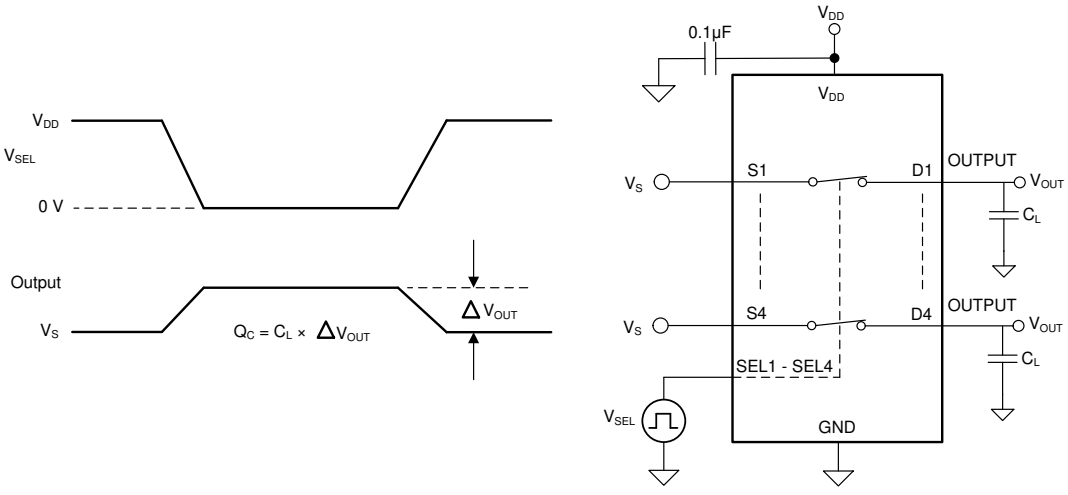


图 7-6. Charge-Injection Measurement Setup

7.7 Off isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. 图 7-7 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

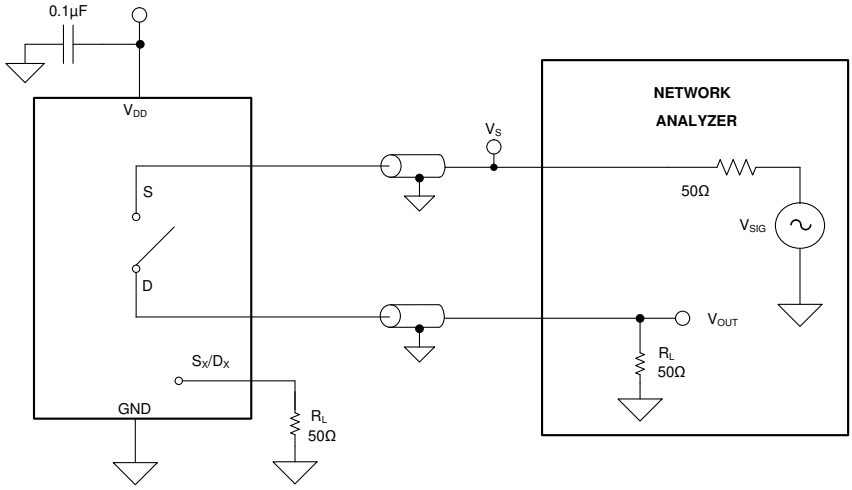


图 7-7. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

7.8 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. 图 7-8 shows the setup used to measure, and the equation used to compute crosstalk.

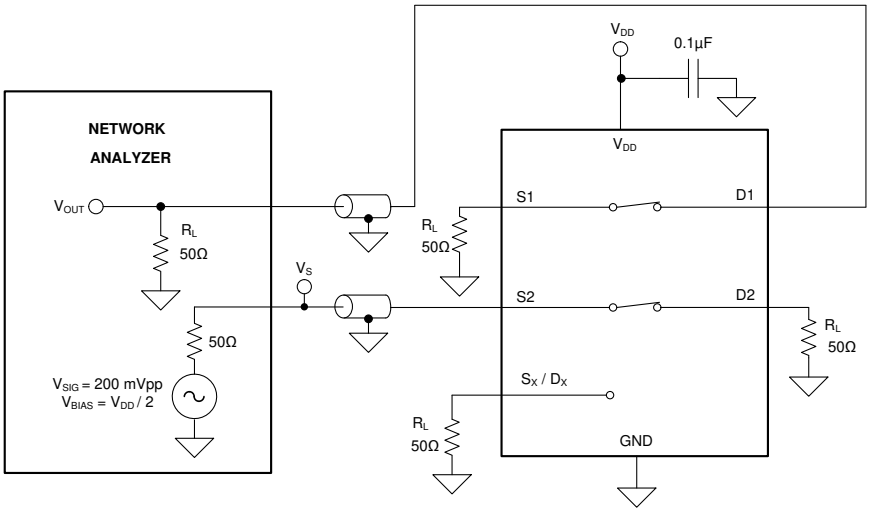


图 7-8. Channel-to-Channel Crosstalk Measurement Setup

Copyright © 2024 Texas Instruments Incorporated

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50 Ω. 图 7-9 shows the setup used to measure bandwidth.

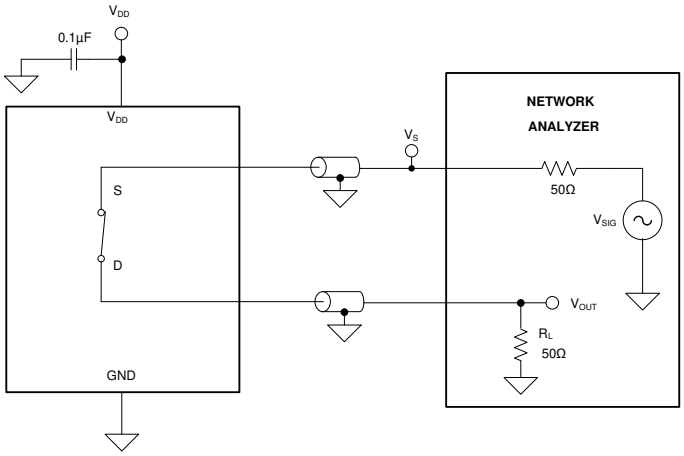


图 7-9. Bandwidth measurement setup

8 Detailed Description

8.1 Overview

The TMUX1111, TMUX1112, and TMUX1113 are 1:1 (SPST), 4-Channel switches. The devices have four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin.

8.2 Functional Block Diagram

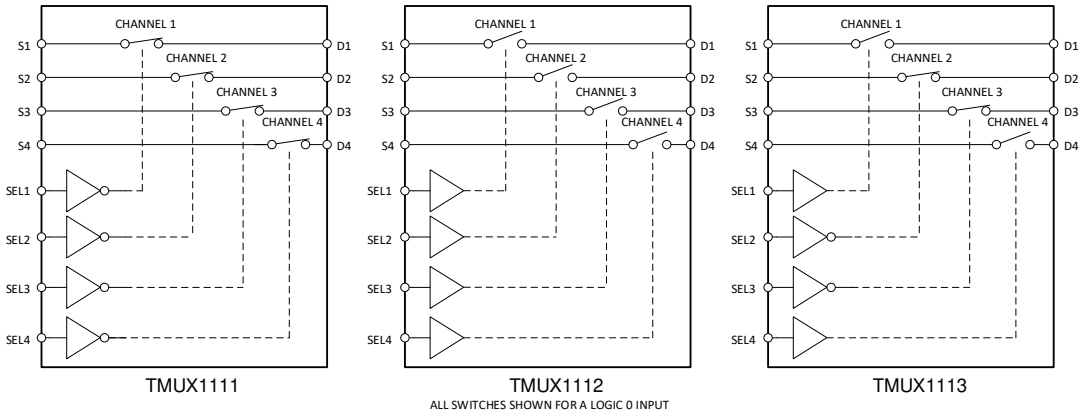


图 8-1. TMUX111x Functional Block Diagram

8.3 Feature Description

8.3.1 Bidirectional operation

The TMUX111x conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail to rail operation

The valid signal path input/output voltage for TMUX111x ranges from GND to V_{DD}.

8.3.3 1.8V Logic compatible inputs

The TMUX111x devices have 1.8V logic compatible control for all logic control inputs. The logic input thresholds scale with supply but still provide 1.8V logic control when operating at 5.5V supply voltage. 1.8V logic level inputs allows the TMUX111x devices to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. The current consumption of the TMUX111x devices increase when using 1.8V logic with higher supply voltage as shown in 图 6-10. For more information on 1.8V logic implementations refer to *Simplifying Design with 1.8V logic Muxes and Switches*

8.3.4 Fail-safe logic

The TMUX111x supports Fail-Safe Logic on the control input pins (EN, A0, A1) allowing for operation up to 5.5V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX111x to be ramped to 5.5V while V_{DD} = 0V. Additionally, the feature enables operation of the TMUX111x with V_{DD} = 1.2V while allowing the select pins to interface with a logic level of another device up to 5.5V.

8.3.5 Ultra-Low Leakage Current

The TMUX111x devices provide extremely low on-leakage and off-leakage currents. The TMUX111x devices are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with

Copyright © 2024 Texas Instruments Incorporated

minimal offset error because of the ultra-low leakage currents. 图 8-2 shows typical leakage currents of the TMUX111x devices versus temperature at V_{DD} = 5V.

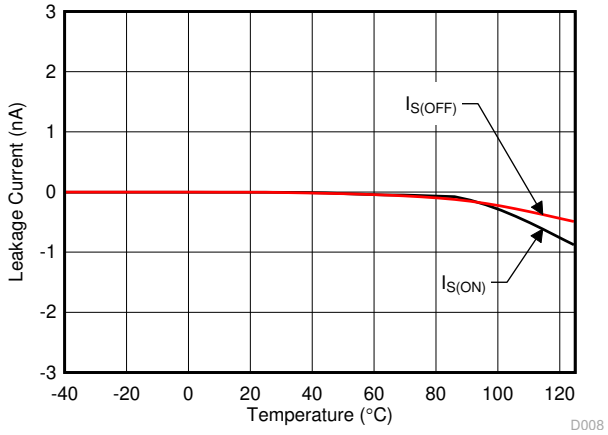


图 8-2. Leakage Current vs Temperature

8.3.6 Ultra-Low Charge Injection

The TMUX111x devices have a transmission gate topology, as shown in 图 8-3. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

The TMUX111x devices have special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to -1.5pC at V_S = 1V as shown in 图 8-4.

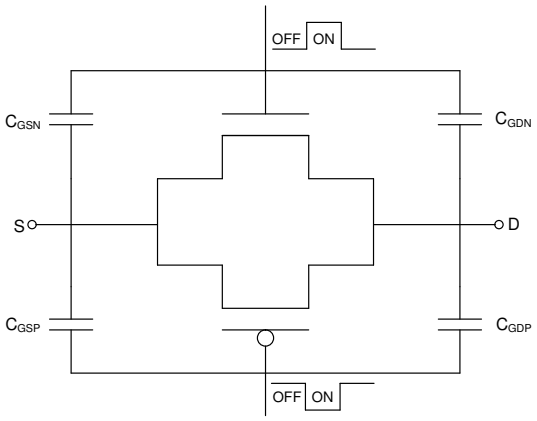


图 8-3. Transmission Gate Topology

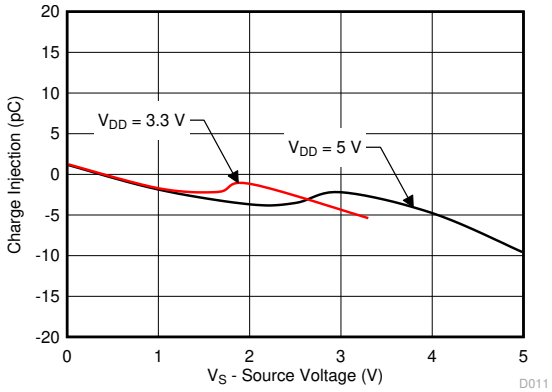


图 8-4. Charge Injection vs Source Voltage

8.4 Device Functional Modes

The TMUX111x devices have four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins can be as high as 5.5V.

The TMUX111x devices can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins should be tied to GND or V_{DD} so that the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or Dx) should be connection to GND.

8.5 Truth Tables

表 8-1, 表 8-2, and 表 8-3 provides the truth tables for the TMUX1111, TMUX1112, and TMUX1113, respectively.

表 8-1. TMUX1111 Truth Table(1)

SEL x	CHANNEL x
0	Channel x ON
1	Channel x OFF

表 8-2. TMUX1112 Truth Table

SEL x	CHANNEL x
0	Channel x OFF
1	Channel x ON

(1) x denotes 1, 2, 3 , or 4 for the corresponding channel.

表 8-3. TMUX1113 Truth Table(1)

SEL1	SEL2	SEL3	SEL4	ON / OFF CHANNELS
0	X	X	X	CHANNEL 1 OFF
1	X	X	X	CHANNEL 1 ON
X	0	X	X	CHANNEL 2 ON
X	1	X	X	CHANNEL 2 OFF
X	X	0	X	CHANNEL 3 ON
X	X	1	X	CHANNEL 3 OFF
X	X	X	0	CHANNEL 4 OFF
X	X	X	1	CHANNEL 4 ON

(1) X denotes *do not care*.

Copyright © 2024 Texas Instruments Incorporated

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TMUX11xx family offers ultra-low input/output leakage currents and low charge injection. These devices operate up to 5.5V, and offer true rail-to-rail input and output of both analog and digital signals. The TMUX111x have a low on-capacitance which allows faster settling time when multiplexing inputs in the time domain. These features make the TMUX11xx devices a family of precision, high-performance switches and multiplexers for low-voltage applications.

9.2 Typical Application - Sample-and-Hold Circuit

One useful application to take advantage of the TMUX1111, TMUX1112, and TMUX1113 performance is the sample-and-hold circuit. A sample-and-hold circuit can be useful for an analog to digital converter (ADC) to sample a varying input voltage with improved reliability and stability. It can also be used to store the output samples from a single digital-to-analog converter (DAC) in a multi-output application. A simple sample-and-hold circuit can be realized using an analog switch such as the TMUX1111, TMUX1112, and TMUX1113 analog switches. 图 9-1 shows a single channel sample-and hold circuit using only 1 of 4 channels in the TMUX111x devices.

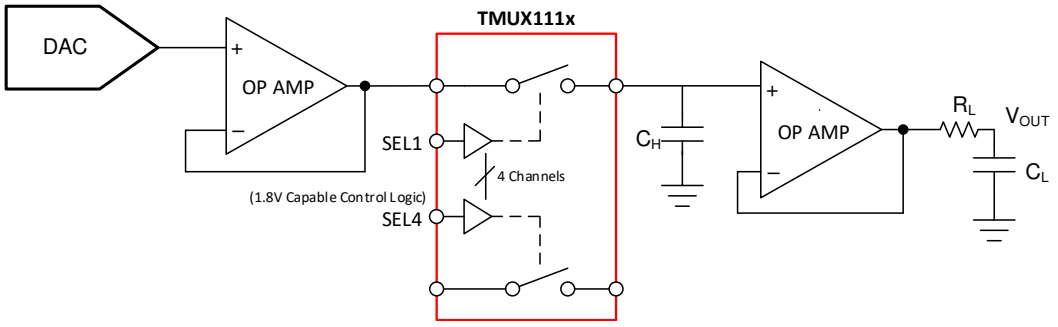


图 9-1. Single Channel Sample-and-Hold Circuit Example

An optional op amp is used before the switch since buffered DACs typically have limitations in driving capacitive loads. The additional buffer stage is included following the DAC to prevent potential stability problems from driving a large capacitive load.

Ideally, the switch delivers only the input signals to the holding capacitors. However, when the switch gets toggled, some amount of charge also gets transferred to the switch output in the form of charge injection, resulting in a pedestal sampling error. The TMUX1111, TMUX1112, and TMUX1113 switches have excellent charge injection performance of only -1.5pC, making them excellent choices for this implementation to minimize sampling error. The pedestal error voltage is indirectly related to the size of the capacitance on the output, for better precision a larger capacitor is required due to charge injection. Larger capacitance limits the system settling time which may not be acceptable in some applications. 图 9-2 shows a TMUX111x device configured for a 2-channel sample-and-hold circuit with pedestal error compensation.

Copyright © 2024 Texas Instruments Incorporated

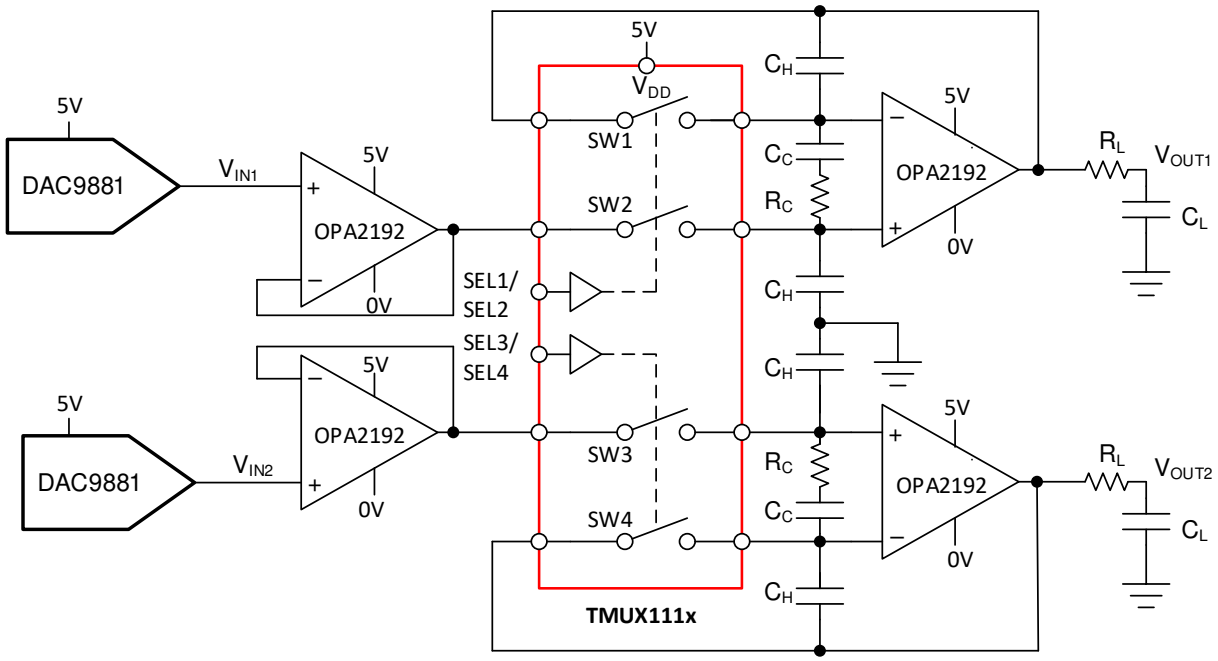


图 9-2. 2-Channel Sample-and-Hold Circuit with Pedestal Error Compensation

9.2.1 Design Requirements

The purpose of this precision design is to implement an optimized 2-output sample-and-hold circuit using a 4-channel SPST switch. The sample and hold circuit needs to be capable of supporting high accuracy with minimized pedestal error and fast settling time..

9.2.2 Detailed Design Procedure

9.2.2.1 Detailed Design Procedure

The TMUX1111, TMUX1112, or TMUX1113 switch is used in conjunction with the voltage holding capacitors (C_H) to implement the sample-and-hold circuit. The basic operation is:

1. When the switch (SW2 or SW3) is closed, it samples the input voltage and charges the holding capacitors (C_H) to the input voltages values.
2. When the switch (SW2 or SW3) is open, the holding capacitors (C_H) holds its previous value, maintaining stable voltage at the amplifier output (V_{OUT}).

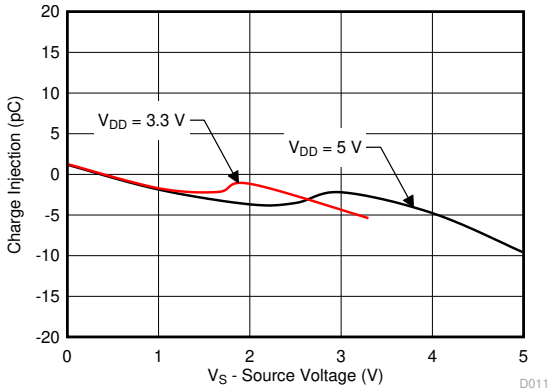
Due to switch and capacitor leakage current, as well as amplifier bias current, the voltage on the hold capacitors droops with time. The TMUX1111, TMUX1112, or TMUX1113 minimize the droops due to its ultra-low leakage performance. At 25°C, the TMUX1111, TMUX1112, andTMUX1113 have extremely low leakage current at 3pA typical.

A second switch SW1 (or SW4) is also included to operate in parallel with SW2 (or SW3) to reduce pedestal error during switch toggling. Because both switches are driven at the same potential, they act as common-mode signal to the op-amp, thereby minimizing the charge injection effects caused by the switch toggling action. Compensation network consisting of R_C and C_C is also added to further reduce the pedestal error, whiling reducing the hold-time glitch and improving the settling time of the circuit. Refer to *Sample and Hold Glitch Reduction for Precision Outputs Reference Design* for more information on sample-and-hold circuits.

Copyright © 2024 Texas Instruments Incorporated

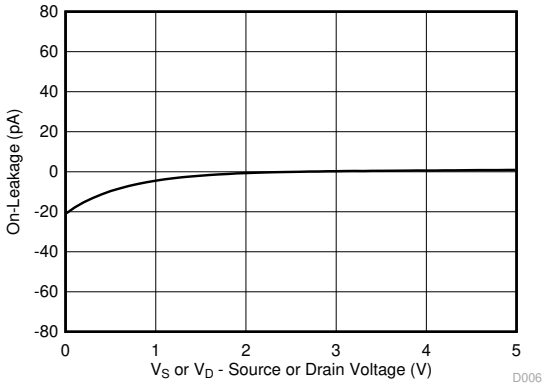
9.2.3 Application Curve

TMUX1111, TMUX1112, andTMUX1113 have excellent charge injection performance and ultra-low leakage current, making them excellent choices to minimize sampling error for the sample and hold application.



T_A = -40°C to +125°C

图 9-3. Charge Injection vs Source Voltage



V_{DD}= 5V

图 9-4. On-Leakage vs Source or Drain Voltage

9.3 Typical Application - Switched Gain Amplifier

Switches and multiplexers are commonly used in the feedback path of amplifier circuits to provide configurable gain control. By using various resistor values on each switch path the TMUX111x allows the system to have multiple gain settings. An external resistor, or utilizing 1 channel always being closed, causes the amplifier to not operate in an open loop configuration. A transimpedance amplifier (TIA) for photodiode inputs is a common circuit that requires gain control using a multi-channel switch to convert the output current of the photodiode into a voltage for the MCU or processor. The leakage current, capacitance, and charge injection performance of the TMUX111x are key specifications to evaluate when selecting a device for gain control.

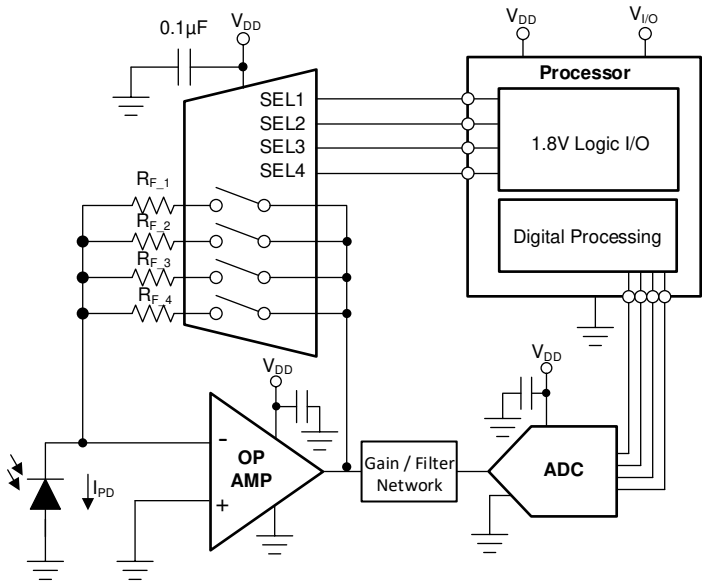


图 9-5. Switching Gain Settings of a TIA circuit

Copyright © 2024 Texas Instruments Incorporated

9.3.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design parameters

PARAMETERS	VALUES
Supply (V_{DD})	3.3V
Input / Output signal range	0μA to 10μA
Control logic thresholds	1.8V compatible

9.3.2 Detailed Design Procedure

The TMUX111x devices can be operated without any external components except for the supply decoupling capacitors. All inputs signals passing through the switch must fall within the recommend operating conditions of the TMUX111x including signal range and continuous current. For this design example, with a supply of 3.3V, the signals can range from 0V to 3.3V when the device is powered. The max continuous current can be 30mA.

Photodiodes commonly have a current output that ranges from a few hundred picoamps to tens of microamps based on the amount of light being absorbed. The TMUX111x have a typical On-leakage current of less than 10pA which would lead to an accuracy well within 1% of a full scale 10μA signal. The low ON and OFF capacitance of the TMUX111x improves system stability by minimizing the total capacitance on the output of the amplifier. Lower capacitance leads to less overshoot and ringing in the system which can cause the amplifier circuit to go unstable if the phase margin is not at least 45°. Refer to *Improve Stability Issues with Low C_{ON} Multiplexers* for more information on calculating the phase margin vs. percent overshoot.

9.3.3 Application Curve

The TMUX1111 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents.

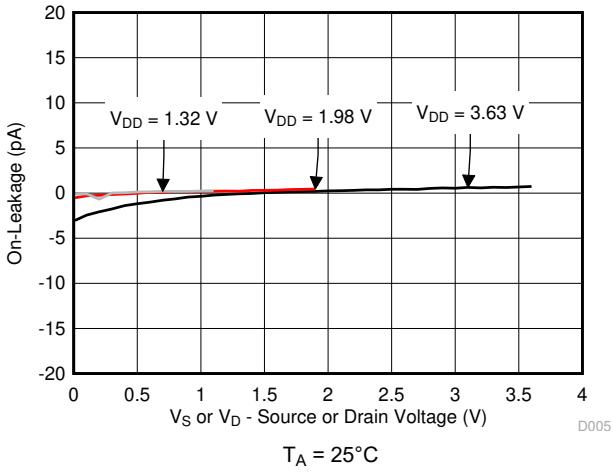


图 9-6. On-Leakage vs Source or Drain Voltage

Copyright © 2024 Texas Instruments Incorporated

9.4 Power Supply Recommendations

The TMUX111x operate across a wide supply range of 1.08V to 5.5V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

9.5 Layout

9.5.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self‐inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 9-7 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

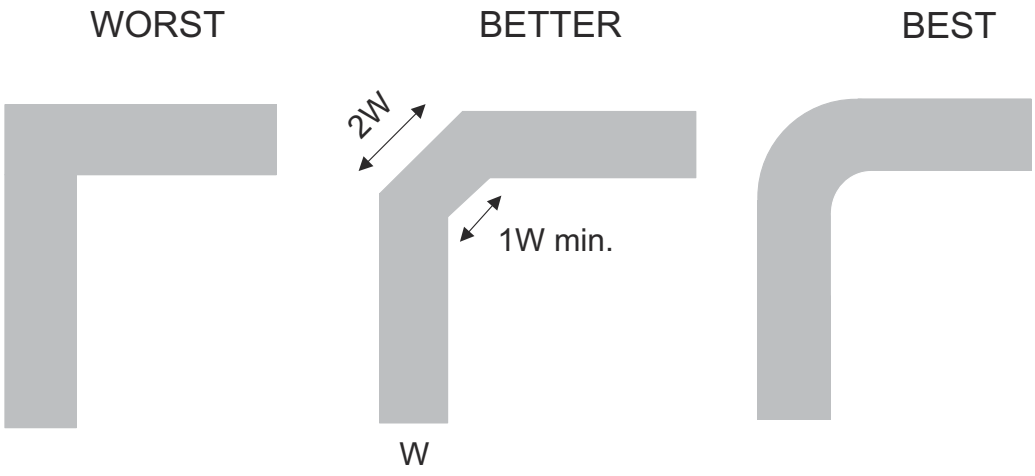


图 9-7. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Copyright © 2024 Texas Instruments Incorporated

9.5.2 Layout Example

图 9-8 shows an example of a PCB layout with the TMUX111x. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

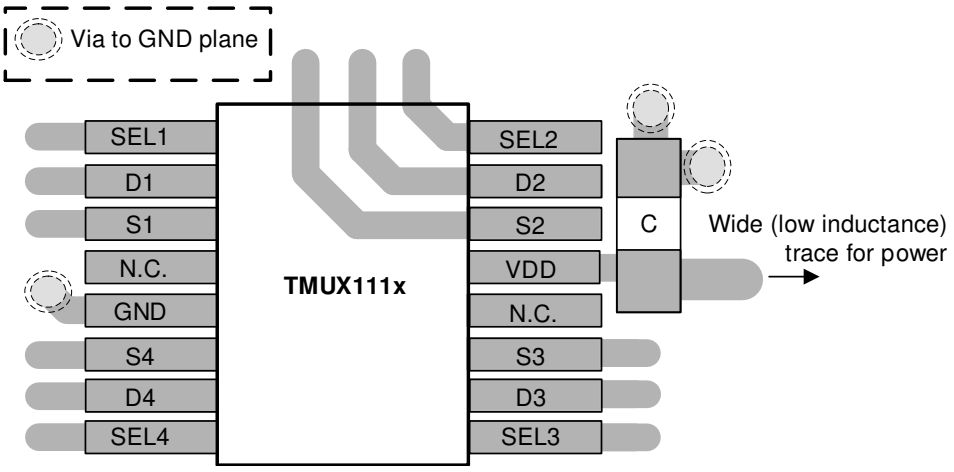


图 9-8. TMUX111x Layout Example

Copyright © 2024 Texas Instruments Incorporated

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Sample and Hold Glitch Reduction for Precision Outputs Reference Design*.
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit*.
- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches*.
- Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.
- Texas Instruments, *QFN/SON PCB Attachment*.
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages*.

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (August 2019) to Revision C (December 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated Is or Id (Continuous Current) values	4
• Added Ipeak values to recommended operating conditions table	4

Changes from Revision A (June 2019) to Revision B (August 2019)	Page
• 从*器件信息* 表中的 TMUX1113、TMUX1112 和 RSV 封装中删除了*产品预发布* 注释	1
• Deleted the *Product Preview* note from: TMUX1113, TMUX1112 in the *Device Comparison Table* table	2
• Deleted the *Product Preview* note from:the RSV package in the *Pin Configuration and Functions* section	3

Copyright © 2024 Texas Instruments Incorporated

- Added RSV (UQFN) thermal values to *Thermal Information* 5

Changes from Revision * (February 2019) to Revision A (June 2019)	Page
• 将文档从*预告信息*更改为*混合状态*	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2024 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX1111PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TM1111
TMUX1111PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1111
TMUX1111RSVR	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FC
TMUX1111RSVR.A	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FC
TMUX1112PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TM1112
TMUX1112PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1112
TMUX1112PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1112
TMUX1112PWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1112
TMUX1112RSVR	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FD
TMUX1112RSVR.A	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FD
TMUX1112RSVRG4.A	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FD
TMUX1113PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TM1113
TMUX1113PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1113
TMUX1113PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1113
TMUX1113PWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1113
TMUX1113RSVR	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FE
TMUX1113RSVR.A	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

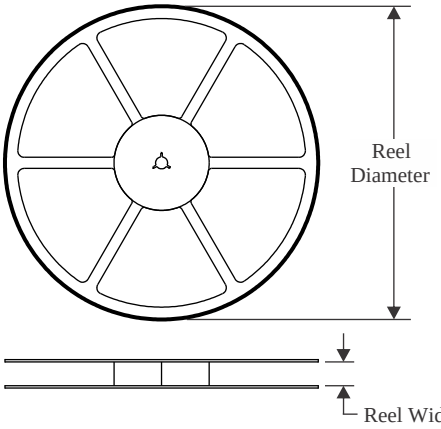
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

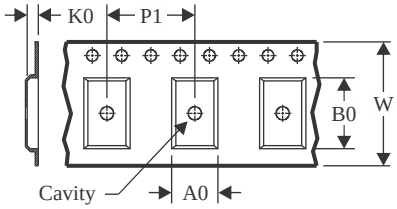
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

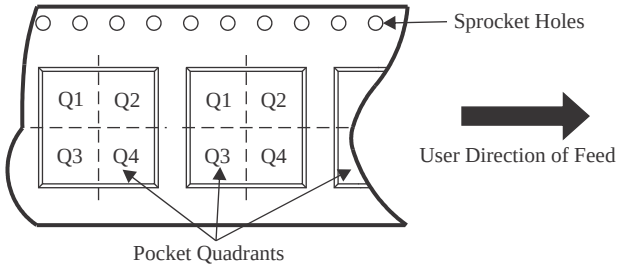


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

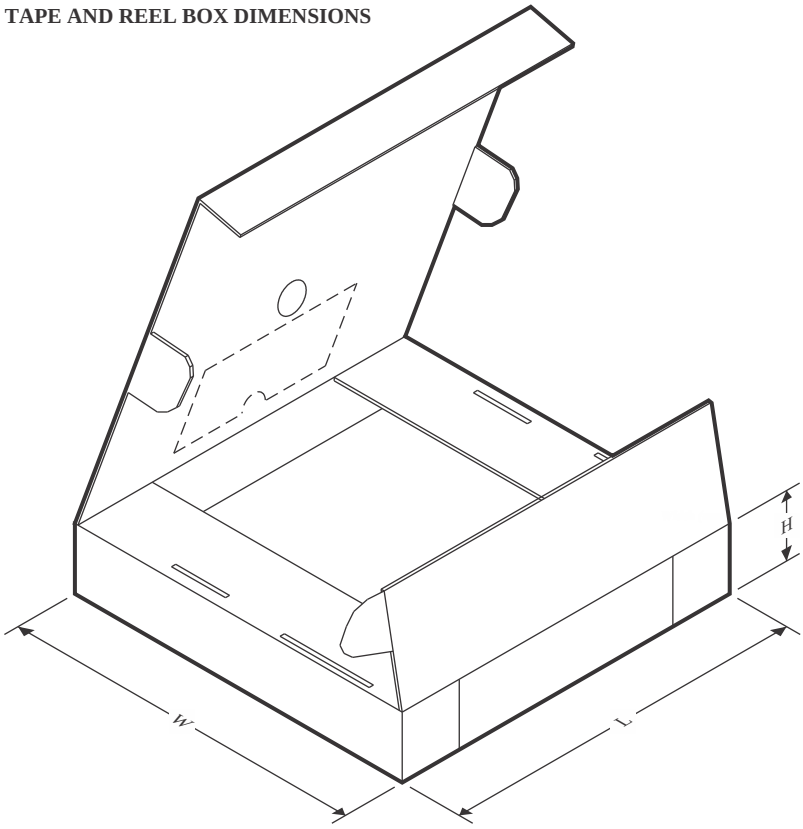
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1111PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX1111RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TMUX1112PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX1112PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX1112PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX1112RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TMUX1113PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX1113PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX1113RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1111PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TMUX1111RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
TMUX1112PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TMUX1112PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX1112PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX1112RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
TMUX1113PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TMUX1113PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX1113RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0

GENERIC PACKAGE VIEW

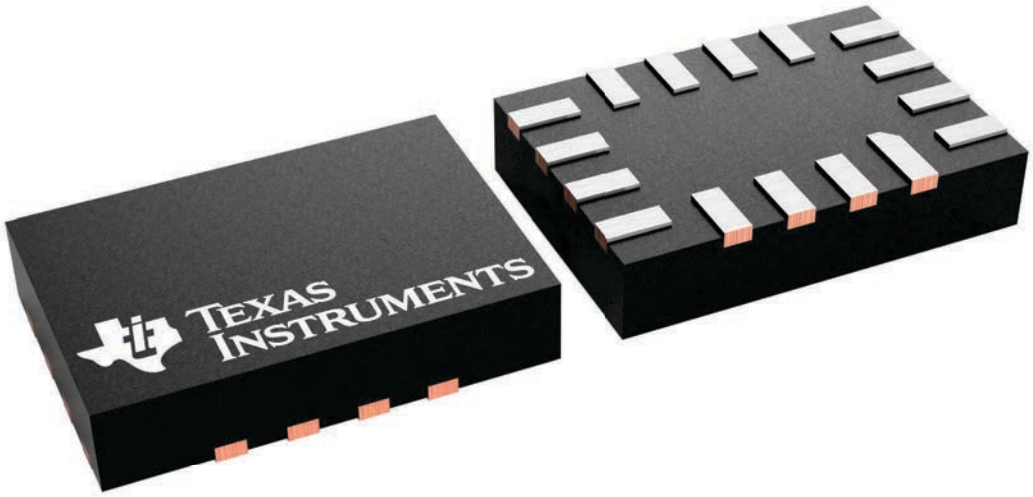
RSV 16

UQFN - 0.55 mm max height

1.8 x 2.6, 0.4 mm pitch

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



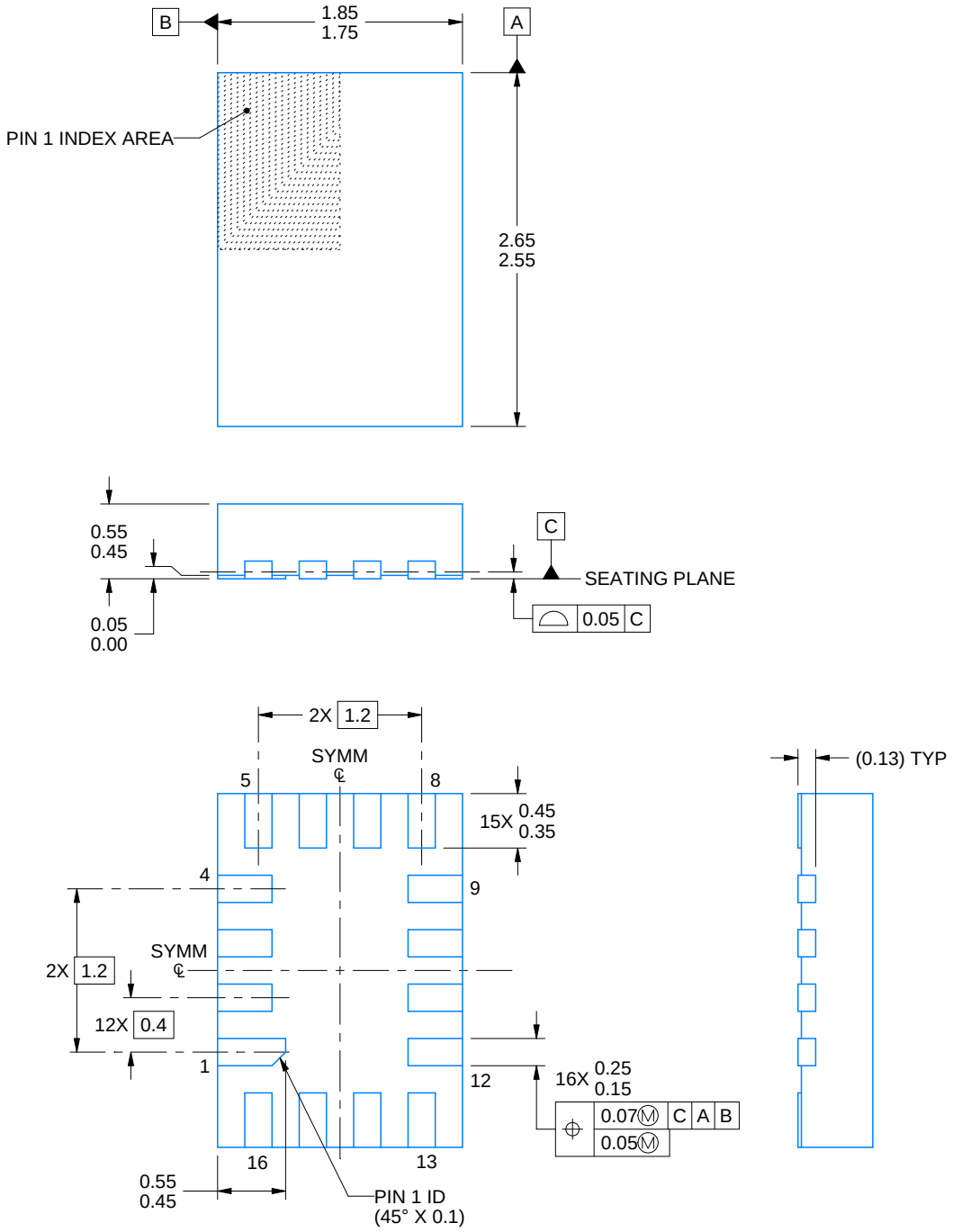
4231225/A

RSV0016A

PACKAGE OUTLINE

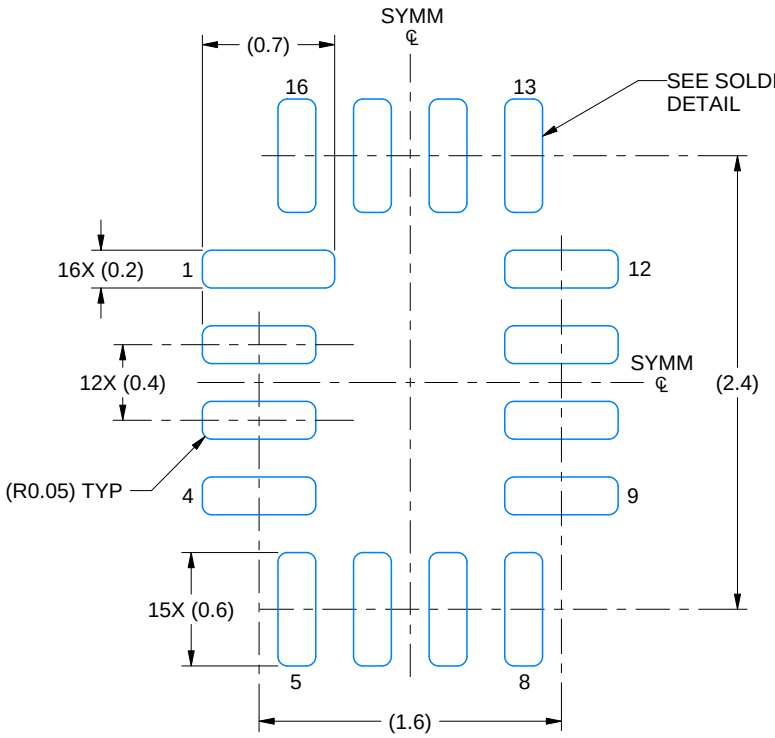
UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

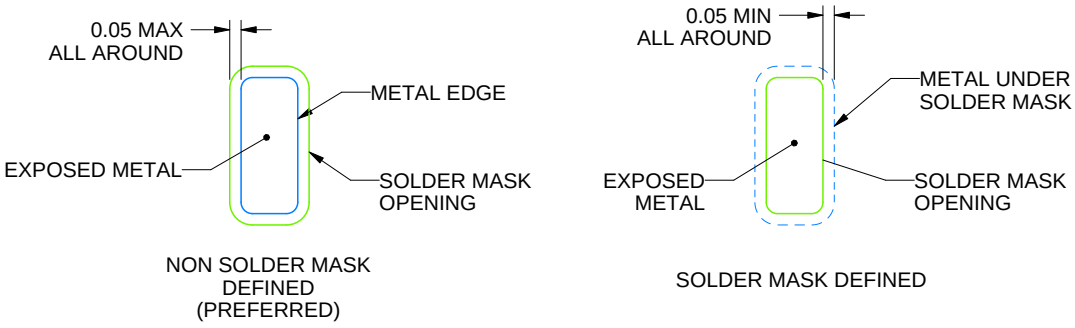


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

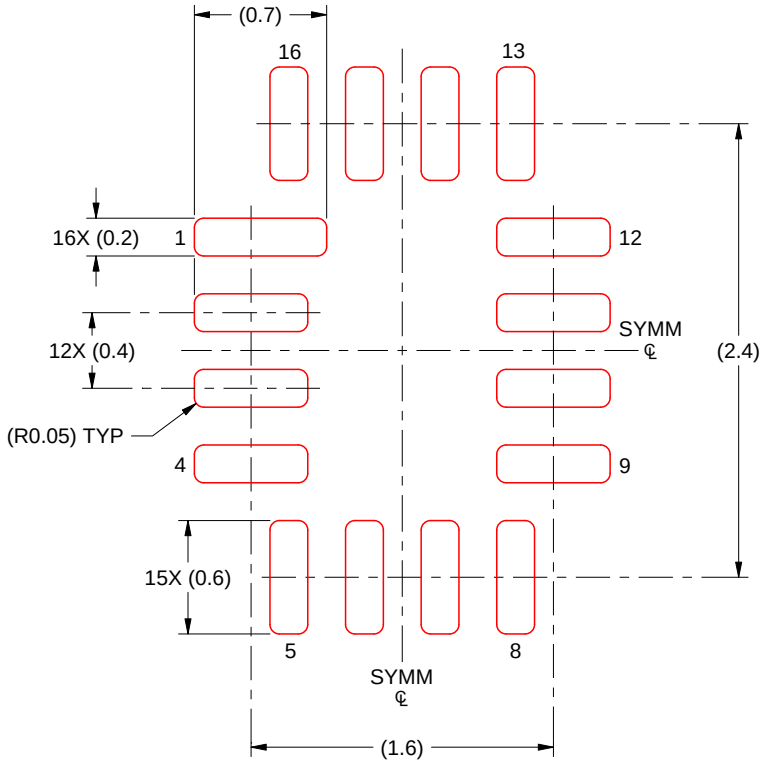


SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

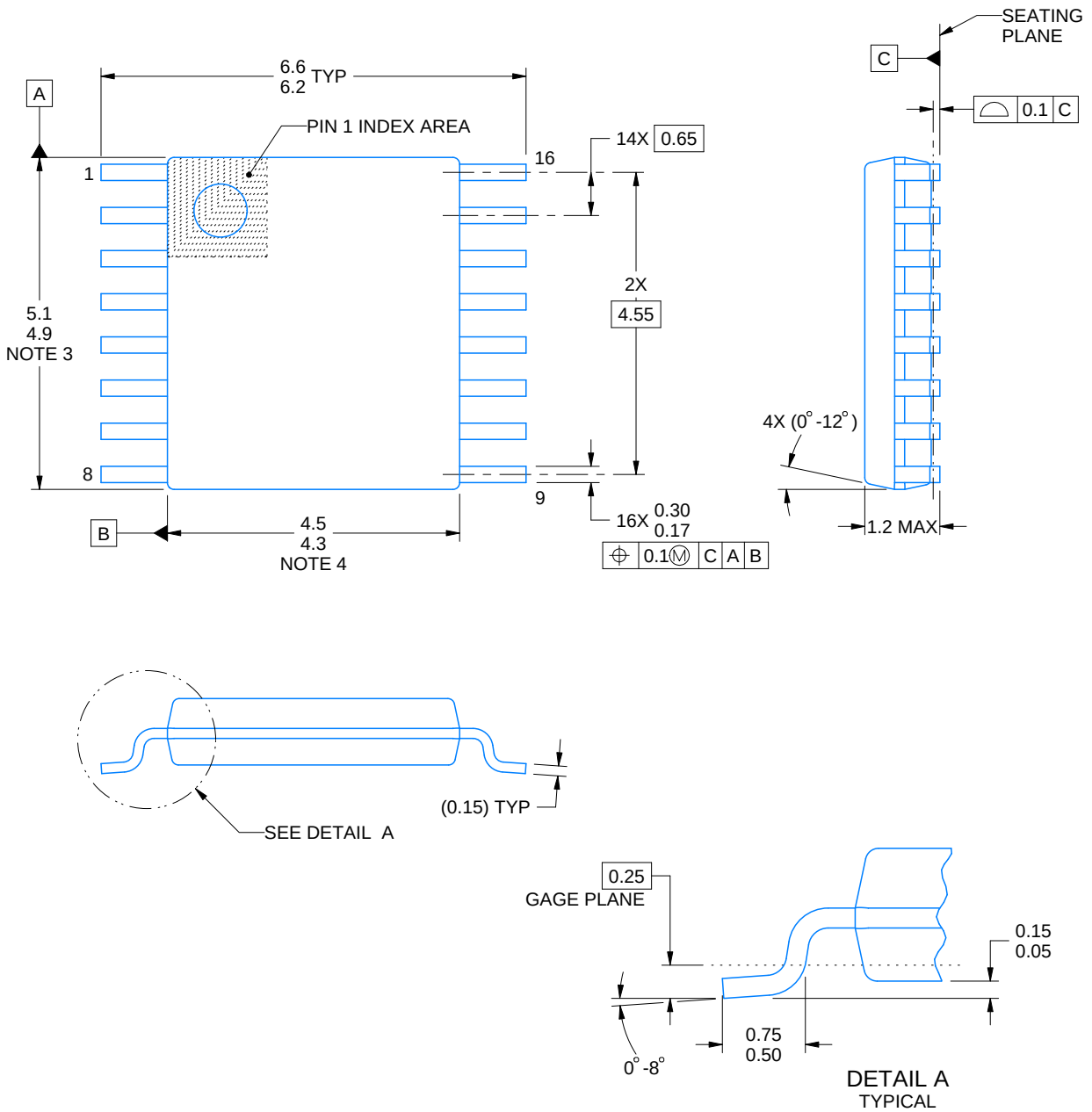
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

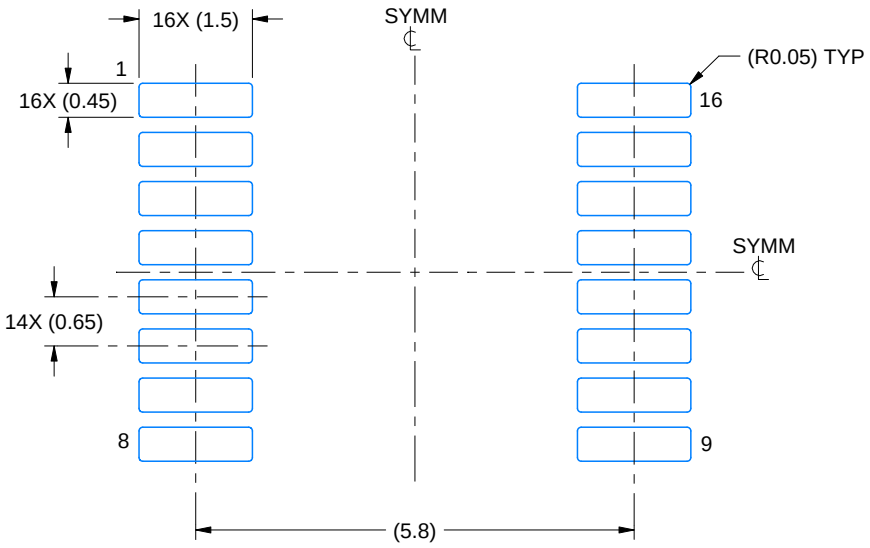
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

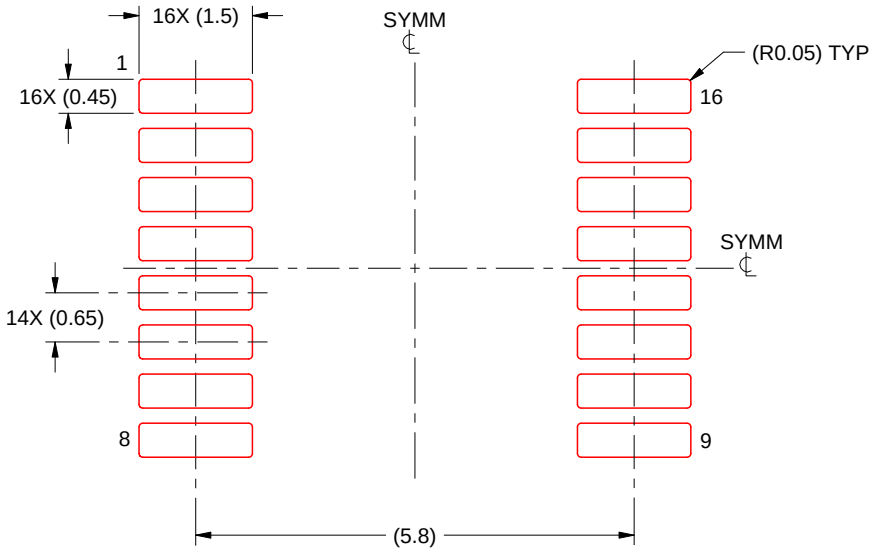


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月