HIGH SPEED POWER DRIVER

Check for Samples: UC1705, UC2705, UC3705

FEATURES

- **1.5 A Source/Sink Drive**
- **100 nsec Delay**
- **40 nsec Rise Fall into 1000 pF**
- **Inverting and Non-Inverting Inputs**
- **Low Cross-Conduction Current Spike**
- **Low Quiescent Current**
- **5 V to 40 V Operation**
- **Thermal Shutdown Protection**
- **Minidip and Power Packages**

DESCRIPTION

The UC1705 family of power drivers is made with a high sppeed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices are also an optimum choise for capacitive line drivers where up to 1.5 A may be switched in either direction. With both inverting and non-inverting inputs available, logic signals of either polarity may be accepted, or one input can be used to gate or strobe the other.

Supply voltages for both V_S and V_C can independently range from 5 V to 40 V. For additional application details, see the UC1707/3707 data sheet (SLUS177).

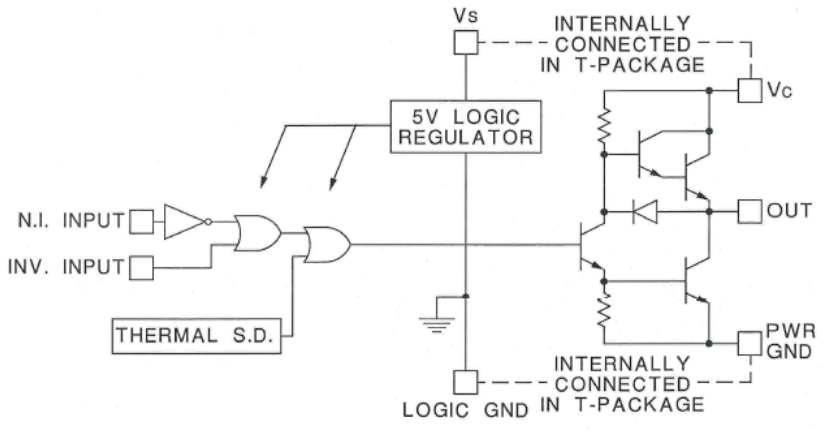
The UC1705 is packaged in an 8-pin hermetically sealed CERDIP for -55°C to 125°C operation. The UC3705 is specified for a temperature range of 0°C to 70°C and is available in either a plastic minidip or a 5-pin, power TO-220 package.

TRUTH TABLE (1) (2)

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

(1) $\overline{OUT}$ = $\overline{INV}$ and N.I.
(2) $\overline{OUT}$ = INV and N.i.

BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

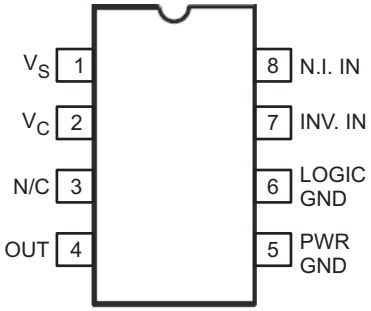
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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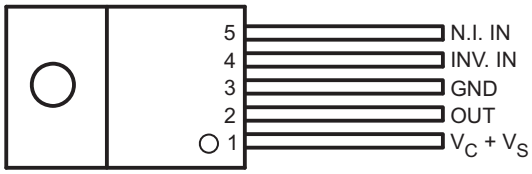
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAMS

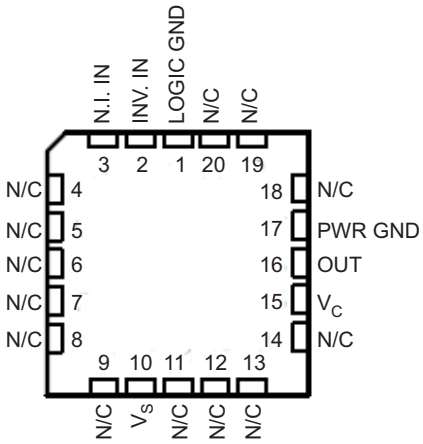
DIL-8 MINIDIP, SOIC-8
(TOP VIEW)
N, JG OR D PACKAGE



5-PIN TO-220
(TOP VIEW)
T PACKAGE



LCCC-20
(TOP VIEW)
FK PACKAGE



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ABSOLUTE MAXIMUM RATINGS(1)

	VALUE			UNIT
	N-Pkg	JG-Pkg	T-Pkg	
Supply Voltage (V_{IN})	40	40	40	V
Collector Supply Voltage, V_C	40	40	40	
Output current (source or sink)				
Steady-State	±500	±500	±1	A
Peak Transient	±1.5	±1	±2	A
Capacitive Discharge Energy	20	15	50	µJ
Digital Inputs (2)	5.5	5.5	5.5	V
Power Dissipation at T_A = 25°C (1)	1	1	3	W
Power Dissipation at T_A (Lead/Case) = 25°C (1)	3	2	25	W
Operating Temperature Range	0 to 70	–55 to 125	0 to 70	°C
Storage temperaturee	–65 to 150	–65 to 150	–65 to 150	°C

(1) All currents are positive into, negative out of the specified terminal.
(2) Digital Drive can exceed 5.5 V if the input current is limited to 10 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1705, –25°C to +85°C for the UC2707, and 0°C to +70°C for the UC3705; $V_{IN} = V_C$ = 20 V. $T_A = T_J$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_S	Supply current	V_S = 40 V, outputs high, T package		6	8	mA
		V_C = 40 V, outputs low, T package		6	12	mA
V_C	Supply current (N, JG Only)	V_C = 40 V, outputs low		2	4	mA
V_C	Leakage current (N, JG Only)	V_S = 0, V_C = 30 V		0.05	0.1	mA
	Digital input low level				0.8	V
	Digital input high level		2.2			V
	Input current	V_I = 0		–0.6	–1	mA
	Input leakage	V_I = 5 V		0.05	0.1	mA
$V_C – V_O$	Output high saturation	I_O = –50 mA			2	V
		I_O = –500 mA			2.5	
V_O	Output low saturation	I_O = –50 mA			0.4	V
		I_O = –500 mA			2.5	
	Thermal shutdown			155		°C

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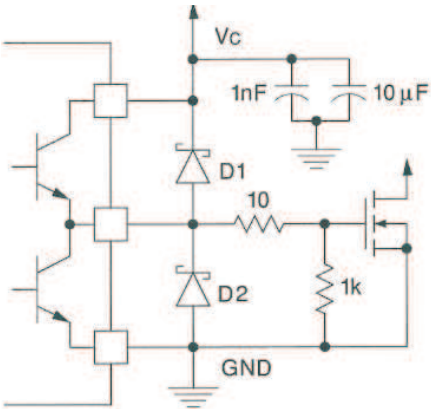
TYPICAL SWITCHING CHARACTERISTICS

V_{IN} = V_C = 20 V, T_A = 25°C. Delays measured to 10% output change.

PARAMETER	TEST CONDITIONS	OUTPUT CL =			UNIT
From Inv. Input to Output		open	1	2.2	nF
Rise time delay		60	60	60	ns
10% to 90% rise		20	40	60	ns
Fall time delay		60	60	60	ns
90% to 10% fall		25	40	50	ns
From N.I. Input to Output					
Rise time delay		90	90	90	ns
10% to 90% rise		20	40	60	ns
Fall time delay		60	60	60	ns
90% to 10% fall		25	40	50	ns
V_C cross-conduction current spike duration	Output rise	25			ns
	Output fall	0			ns

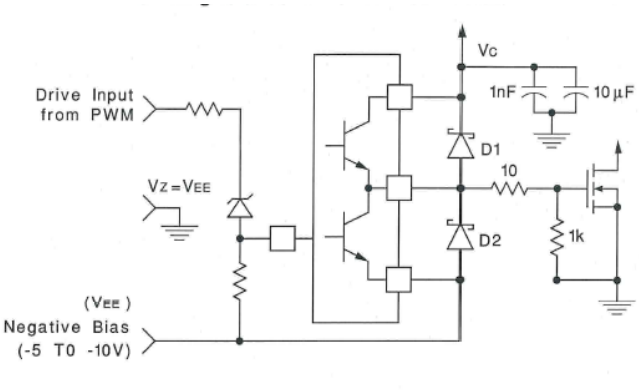
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APPLICATION INFORMATION



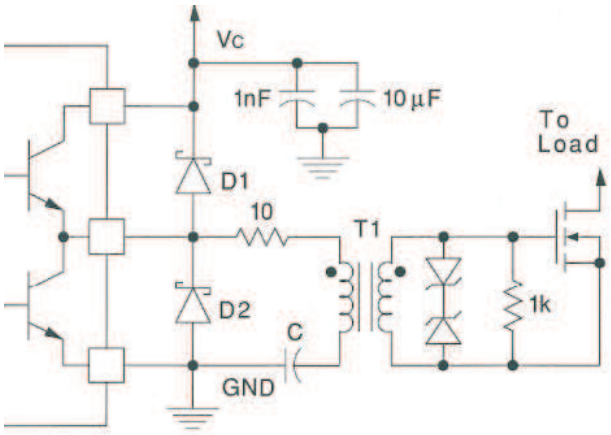
D1, D2: UC3611 Schottky Diodes

Figure 1. Power MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

Figure 2. Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs



D1, D2: UC3611 Schottky Diodes

Figure 3. Transformer Coupled MOSFET DRIVE Circuit

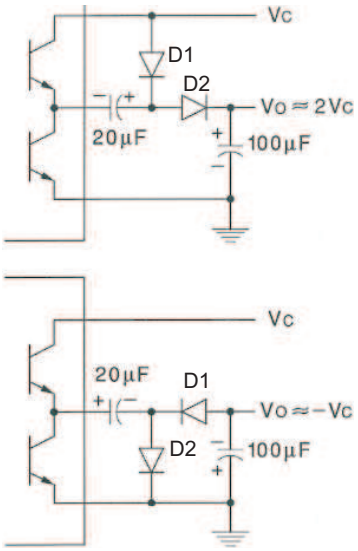


Figure 4. Charge Pump Circuit

REVISION HISTORY

Changes from Revision C (December, 2011) to Revision D	Page
• Deleted SN54BCT373 from title for FK package image	2

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9579801M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9579801M2A UC1705L/ 883B
5962-9579801MPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9579801MPA UC1705
5962-9579801VPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9579801VPA UC1705
5962-9579801VPA.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9579801VPA UC1705
UC1705J	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1705J
UC1705J.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1705J
UC1705J883B	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9579801MPA UC1705
UC1705J883B.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9579801MPA UC1705
UC1705L883B	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9579801M2A UC1705L/ 883B
UC1705L883B.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9579801M2A UC1705L/ 883B
UC2705D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2705D
UC2705D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2705D
UC2705DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2705D
UC2705N	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2705N
UC2705N.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2705N
UC3705D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3705D
UC3705D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3705D
UC3705DTR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3705D
UC3705DTR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3705D

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC3705J	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	0 to 70	UC3705J
UC3705J.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	0 to 70	UC3705J
UC3705N	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3705N
UC3705N.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3705N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC1705, UC1705-SP, UC3705, UC3705M :

- Catalog : UC3705, UC1705, UC3705M, UC3705

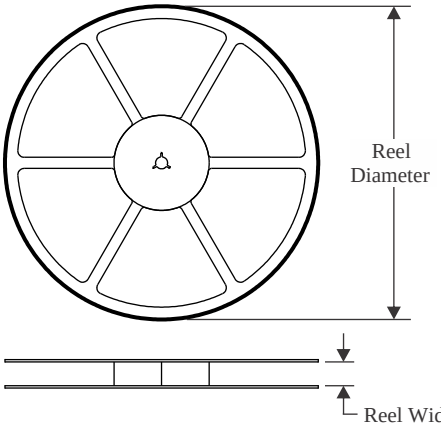
- Military : UC1705, UC1705
- Space : UC1705-SP

NOTE: Qualified Version Definitions:

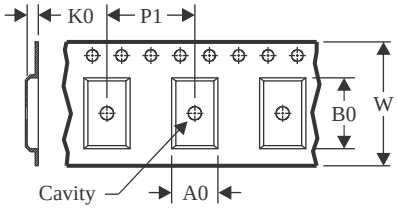
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

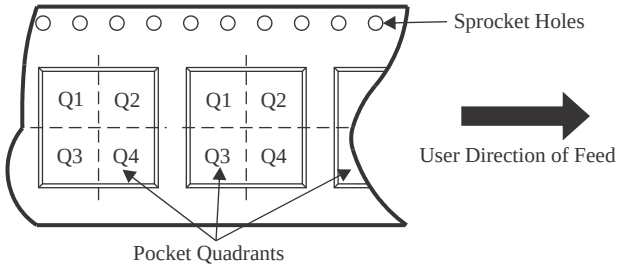


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

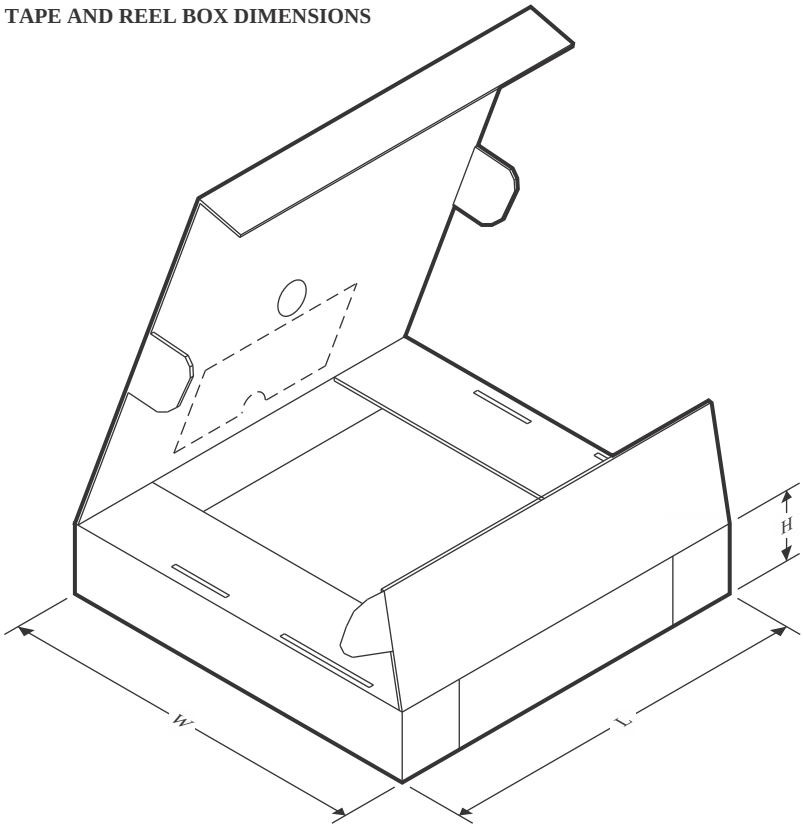
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3705DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

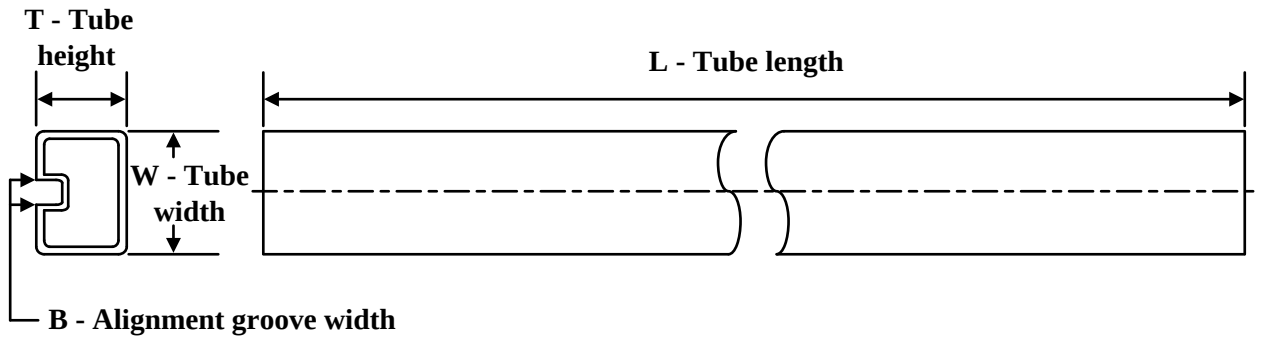
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3705DTR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9579801M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1705L883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1705L883B.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC2705D	D	SOIC	8	75	506.6	8	3940	4.32
UC2705D.A	D	SOIC	8	75	506.6	8	3940	4.32
UC2705DG4	D	SOIC	8	75	506.6	8	3940	4.32
UC2705N	P	PDIP	8	50	506	13.97	11230	4.32
UC2705N.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3705D	D	SOIC	8	75	506.6	8	3940	4.32
UC3705D.A	D	SOIC	8	75	506.6	8	3940	4.32
UC3705N	P	PDIP	8	50	506	13.97	11230	4.32
UC3705N.A	P	PDIP	8	50	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

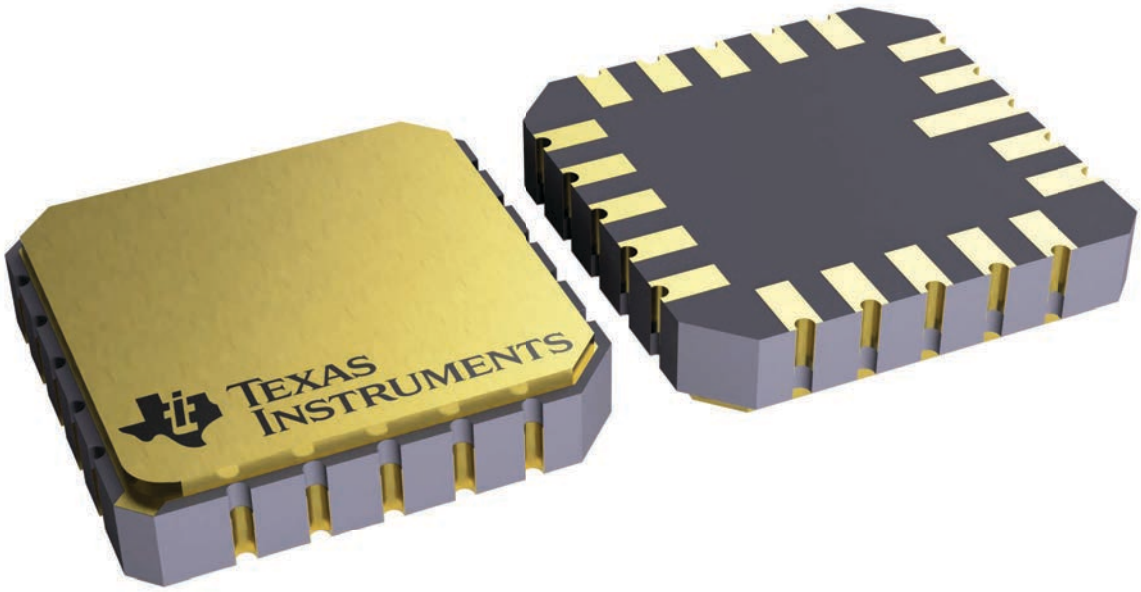
FK 20

LCCC - 2.03 mm max height

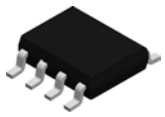
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

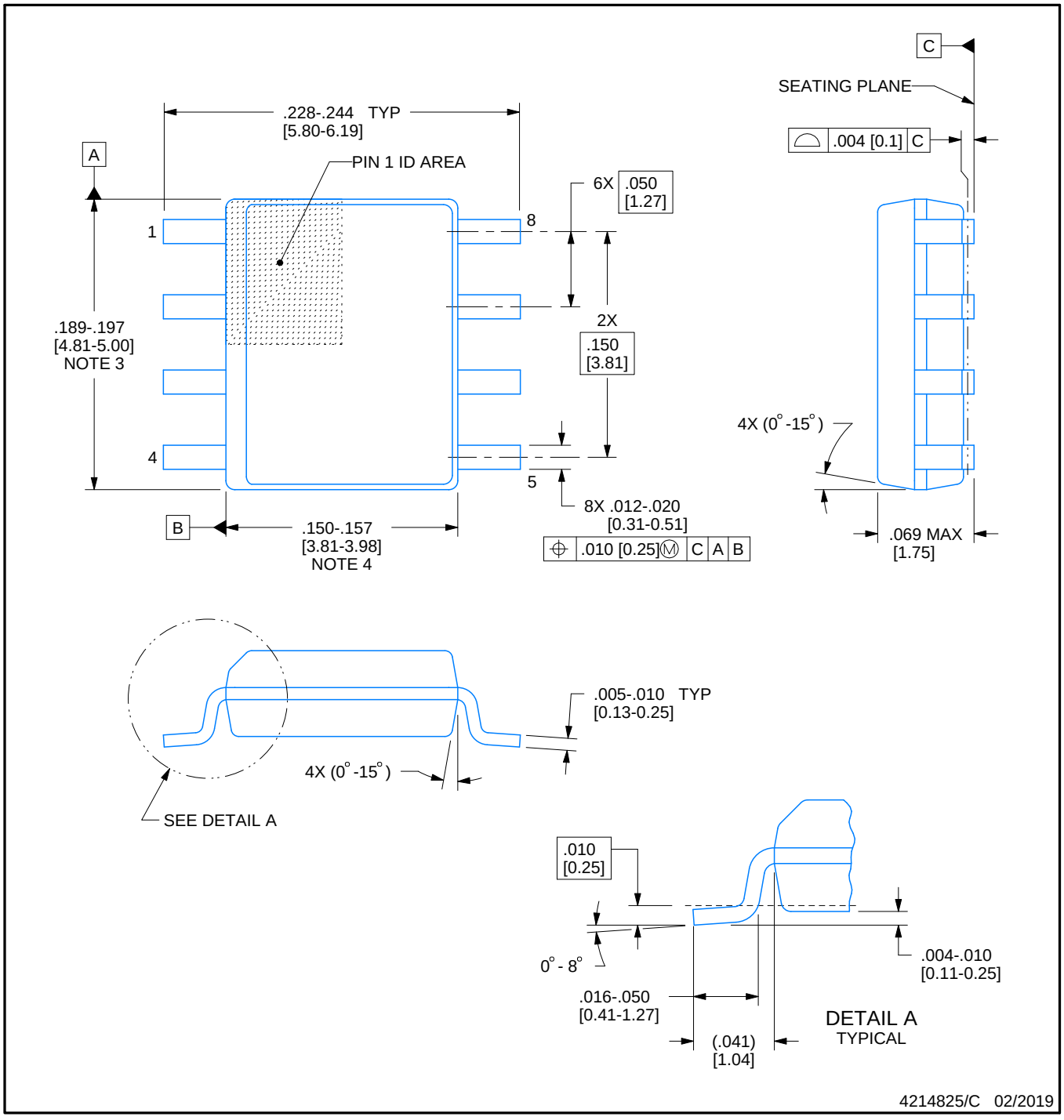


PACKAGE OUTLINE

D0008A

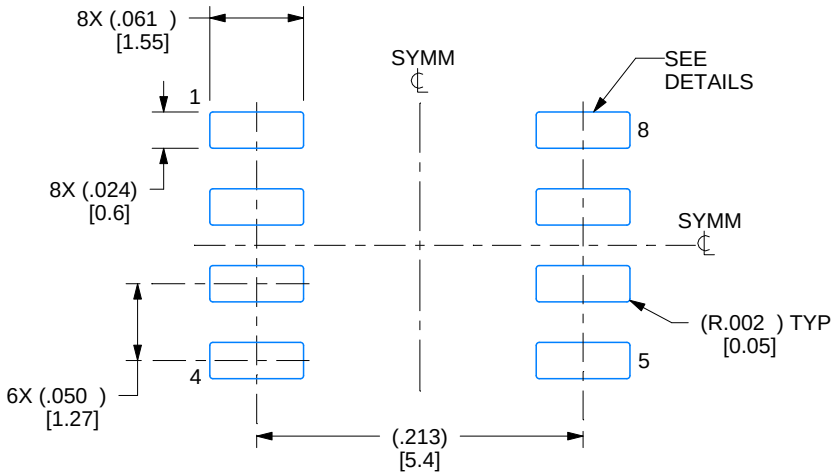
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

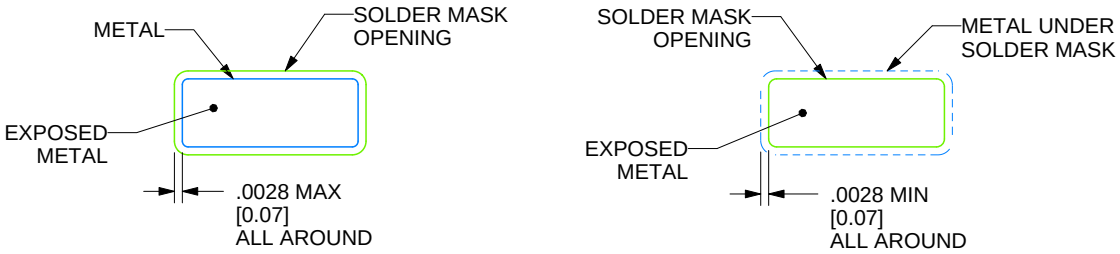


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

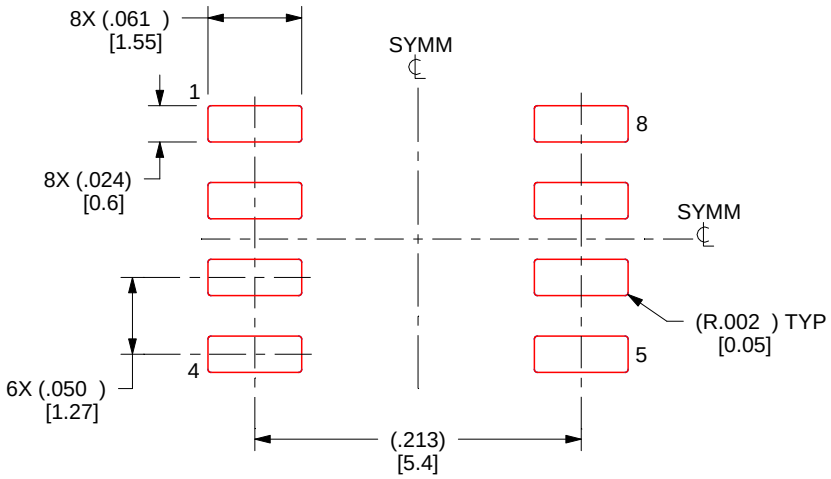
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



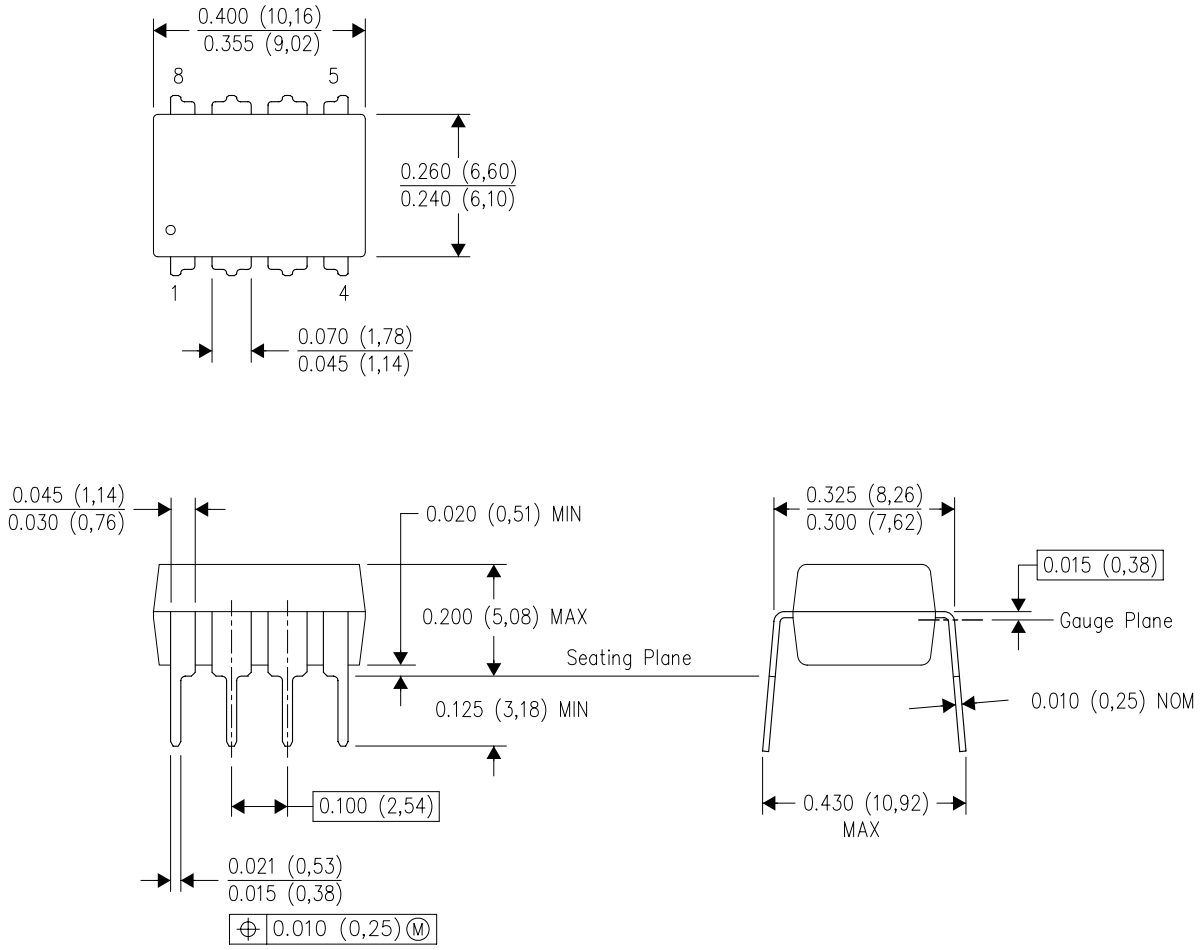
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



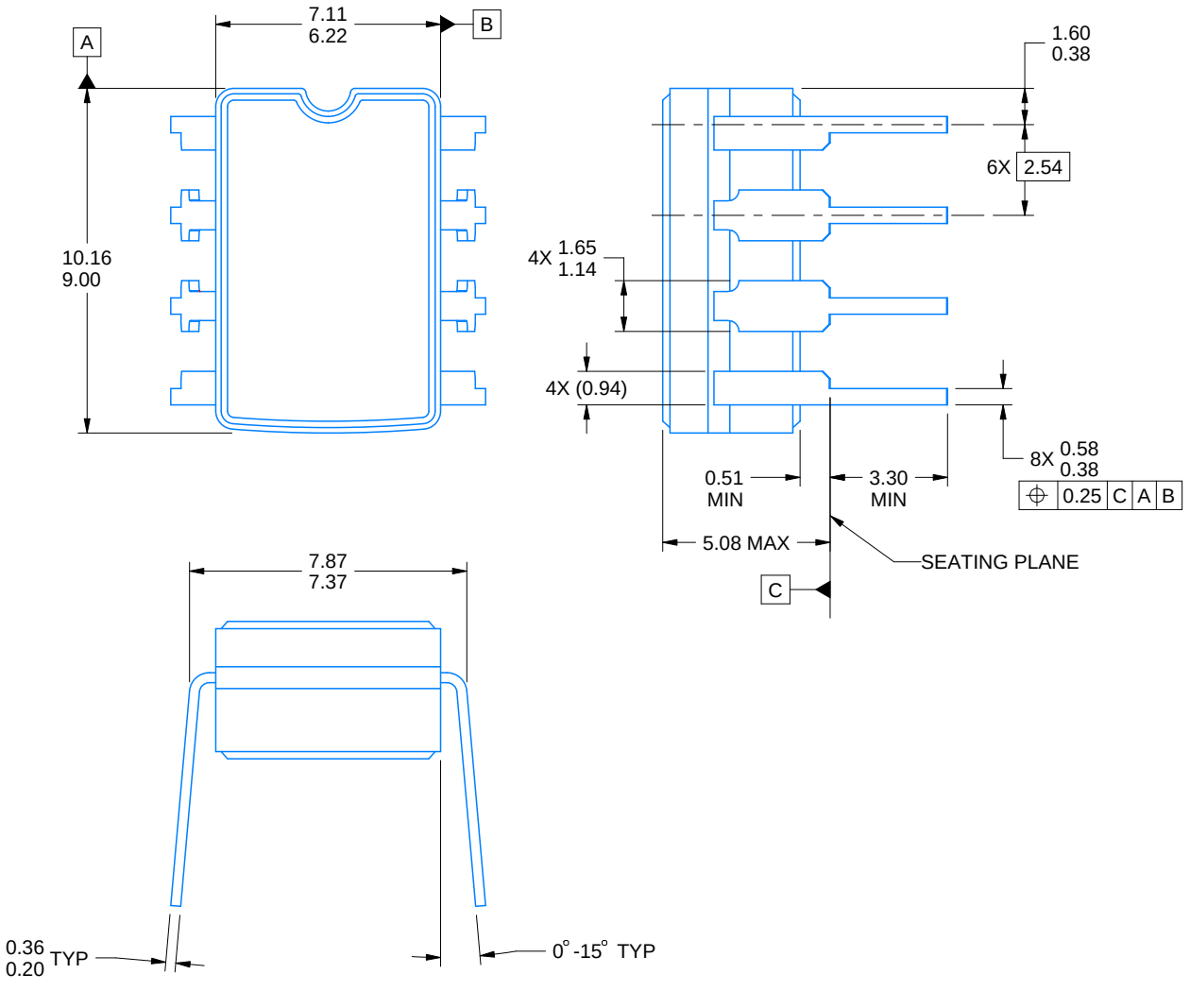
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

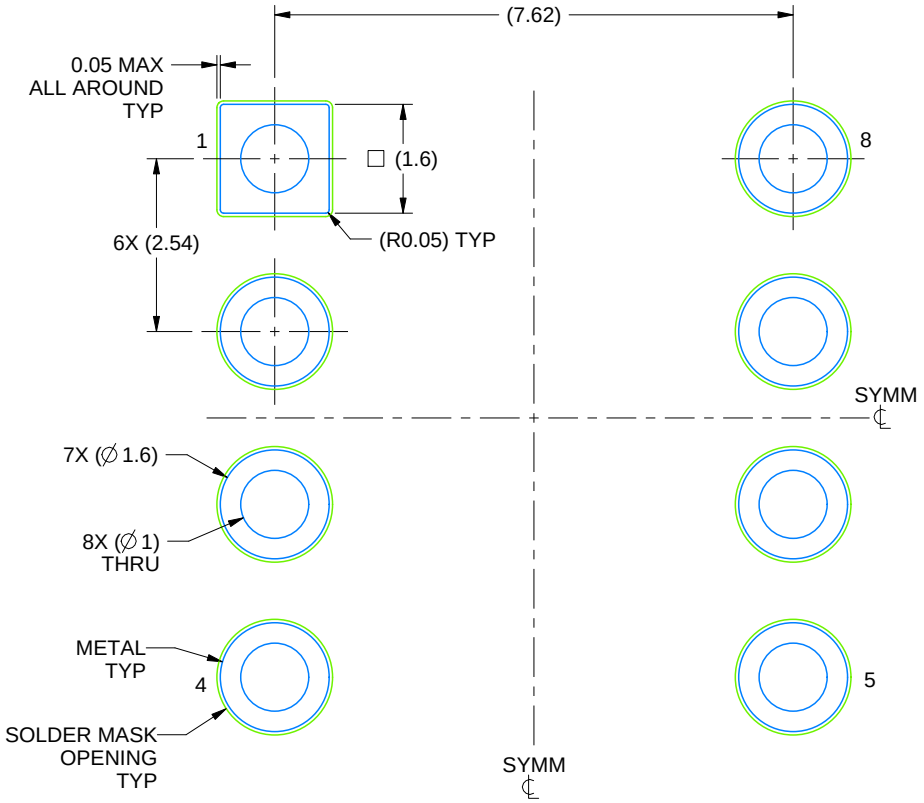
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

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