SC667
7 LED Light Management Unit
Automatic Dropout Prevention, Ambient Light Sense Input, PWM Dimming, and 4 LDOs

Features

- Seven LED backlight sinks with 32 current settings from 0mA to 25mA
- Up to four LED backlight banks
- Lighting effects — fade-in/fade-out, breathe, blink, auto-dim full, and auto-dim partial functions
- ADP (Automatic Dropout Prevention) for backlights
- ALS (Ambient Light Sense) option sets the backlight brightness according to ambient lighting conditions
- I²C Bus fast mode and standard mode
- IRQ (Interrupt request) — open-drain output indicates a change of state for the ALS
- Backlight current accuracy — ±1.5% typical
- Backlight current matching — ±0.5% typical
- Four programmable 200mA low-noise LDO regulators
- PWM interface (200Hz to 50kHz) with internal digital low-pass filter
- Automatic sleep mode with all LEDs off
- Shutdown current — 0.1µA typical
- Ultra-thin package — 3 x 3 x 0.6 (mm)
- Lead-free and halogen-free
- WEEE and RoHS compliant

Applications

- Cellular phones, smart phones, and PDAs
- LCD modules
- Portable media players and digital cameras
- Personal navigation devices
- Display/keypad backlighting and LED indicators

Description

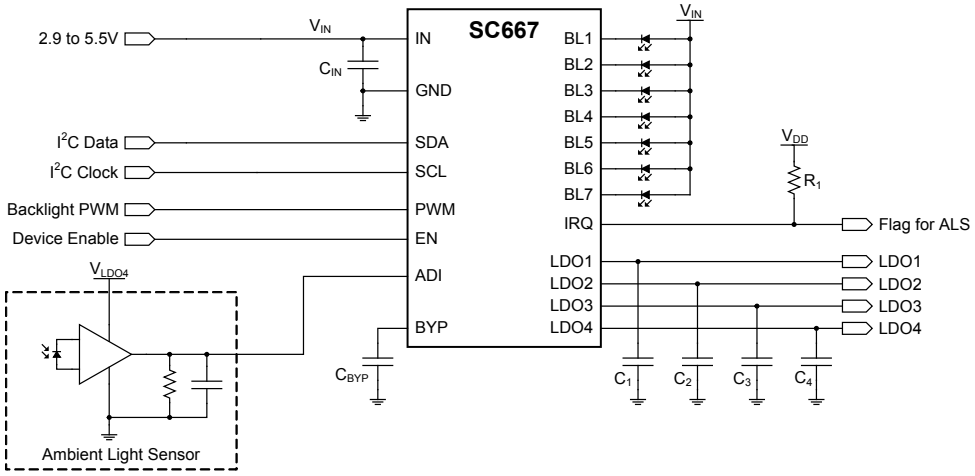
The SC667 is a highly integrated light management unit that provides programmable current for up to seven LED current sinks. Four LED banks are provided to allow settings for various LED zones or indicators. Four low-noise LDOs with programmable outputs ranging from 1.2V to 3.3V and 200mA maximum output current are also included.

ADP limits the maximum LED current to a level that ensures the LEDs maintain matched currents when the supply voltage approaches dropout. This feature produces acceptable light output at low supply voltage levels without requiring a boost converter or charge pump.

Two interfaces are provided for design flexibility. The I²C interface controls the LED on/off functions, assigns the LEDs to backlight banks, programs the LED currents, programs the lighting effects, enables the LDOs, and sets the LDO output voltages. The PWM interface reduces the current setting for LED bank #1 by a factor equal to the duty cycle of the applied PWM signal. A filter at the PWM input converts the pulsed signal to a DC current level, resulting in less switching noise compared to pulsed current methods.

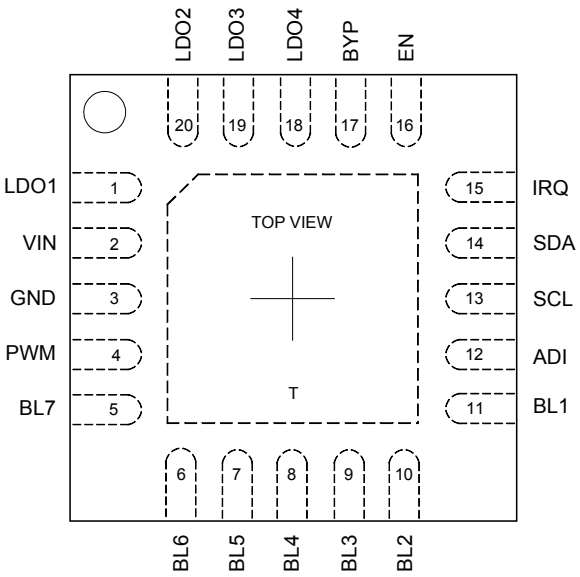
The ADI input translates the voltage from an external ALS (Ambient Light Sensor) into a digitized code using a sigma-delta ADC. This block includes level detection to adjust the current setting of bank #1 with two different programmable levels based on the ambient light level. An interrupt output transitions low to notify the host processor that a level adjustment has been made.

Typical Application Circuit



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Pin Configuration



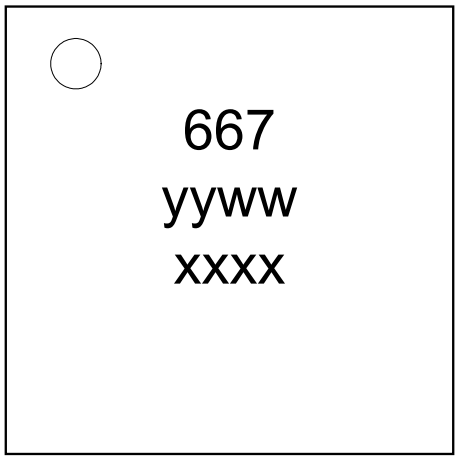
MLPQ-UT-20; 3x3, 20 LEAD
θ_{JA} = 35°C/W

Ordering Information

Device	Package
SC667ULTRT[1][2]	MLPQ-UT-20 3×3
SC667EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free package only. Device is WEEE and RoHS compliant and halogen-free.

Marking Information



yyww = Date Code
xxxx = Semtech Lot Number

SEMTECH

Absolute Maximum Ratings

Pin Voltage — IN (V) ..... -0.3 to +6.0
Pin Voltage — All Other Pins (V) ..... -0.3 to (V_{IN} + 0.3)
LDOn[1] Short Circuit Duration ..... Continuous
ESD Protection Level[2] (kV) 4.5

Recommended Operating Conditions

Ambient Temperature Range (°C) ..... $-40 \le T_A \le +85$
Input Voltage (V) ..... $2.9 \le V_{IN} \le 5.5$
Backlight Sink Voltage (V) ..... $0.05 \le V_{BLn} \le 4.2$

Thermal Information

Thermal Resistance, Junction to Ambient[3] (°C/W) 35
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Subscripting for all LDOs (LDOn), n = 1, 2, 3, 4.
(2) Tested according to JEDEC standard JESD22-A114-B.
(3) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted, T_A = +25°C for Typ, -40°C to +85°C for Min and Max, $T_{J(MAX)}$ = 125°C, V_{IN} = 3.7V, $C_{IN} = C_{LDO1} = C_{LDO2} = C_{LDO3} = C_{LDO4}$ = 1.0µF, C_{BYP} = 22nF, (ESR = 0.03Ω)[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Specifications						
Input Supply Voltage	V_{IN}		2.9		5.5	V
Shutdown Current	$I_{Q(OFF)}$	Shutdown, V_{IN} = 4.2V		0.1	2.0	µA
Total Quiescent Current	I_Q	Sleep (all LDOs off), EN = V_{IN}[2]		90	135	µA
		Sleep (all LDOs on), EN = V_{IN}[2]		300	450	
		7 LEDs on		1.4		mA
LED Sink Electrical Specifications						
Maximum Total Backlight Current	$I_{OUT(MAX)}$	Sum of all active LED currents, V_{IN} above dropout level		175		mA
Backlight Current Setting Range	I_{BL}	Nominal setting for BL1 – BL7	0		25	mA
Backlight Current Accuracy	I_{BL_ACC}	I_{BLn}[3] = 12mA		±1.5		%
Backlight Current Matching[4]	I_{BL-BL}	I_{BLn}[3] = 12mA	-3.5	±0.5	+3.5	%
Dropout Voltage[5]	V_{DO}	One bank of 6 backlights set equal to 20mA		59		mV
Current Sink Off-State Leakage Current	$I_{BL/FL(OFF)}$	$V_{IN} = V_{BLn}$[3] = 4.2V		0.1	1	µA

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LDO Electrical Specifications						
LDO1, LDO3, and LDO4 Voltage Setting Range	V_{LDOm} (6)	Range of nominal settings	1.5		3.3	V
LDO2 Voltage Setting Range	V_{LDO2}	Range of nominal settings	1.2		1.8	V
Output Voltage Accuracy	ΔV_{LDO}	I_{LDOn} (6) = 1mA, T_A = 25°C, 2.9V ≤ V_{IN} ≤ 4.2V	-3	±1.0	+3	%
		I_{LDOn} (6) = 1mA to 100mA, 2.9V ≤ V_{IN} ≤ 4.2V	-3.5		+3.5	%
Dropout Voltage	V_{Dm} (6)	I_{LDOm} (6) = 150mA, $V_{IN} = V_{LDOm} + V_{Dm}$		150	200	mV
	V_{D2}	I_{LDO2} = 100mA, $V_{IN} = V_{LDO2} + V_{D2}$		100	150	
Current Limit	I_{LIM}		200			mA
Line Regulation	ΔV_{LINE}	I_{LDOm} (6) = 1mA, V_{IN} = 2.9V to 4.2V, V_{LDOm} = 2.8V		2.1	7.2	mV
		I_{LDO2} = 1mA, V_{IN} = 2.9V to 4.2V, V_{LDO2} = 1.8V		1.3	4.8	
Load Regulation	ΔV_{LOAD}	V_{LDOm} (6) = 3.3V, I_{LDOm} = 1mA to 100mA		10	25	mV
		V_{LDO2} = 1.8V, I_{LDO2} = 1mA to 100mA		8	20	
Power Supply Rejection Ratio	$PSRR_m$ (6)	1.5V < V_{LDOm} < 3.0V, f < 10kHz, C_{BYP} = 22nF, I_{LDOm} = 50mA, with 0.5V_{P-P} supply ripple		53		dB
	$PSRR_2$	1.2V < V_{LDO2} < 1.8V, f < 10kHz, C_{BYP} = 22nF, I_{LDO2} = 50mA, with 0.5V_{P-P} supply ripple		61		
Output Voltage Noise	e_{n-LDOm} (6)	10Hz < f < 100kHz, C_{BYP} = 22nF, C_{LDOm} = 1µF, I_{LDOm} = 50 mA, 1.5V < V_{LDOm} < 3.0V		67		µV_{RMS}
	e_{n-LDO2}	10Hz < f < 100kHz, C_{BYP} = 22nF, C_{LDO2} = 1µF, I_{LDO2} = 50 mA, 1.2V < V_{LDO2} < 1.8V		47		
Minimum LDO Capacitor (1)	$C_{LDO(MIN)}$	Nominal value for C_{LDOn} (6)	1			µF
ADC Specifications						
Resolution	AD_{RES}			8		bits
Offset	AD_{OFFSET}	V_{LDO4} = 3.3V		1		LSB
Gain Error	AD_{GAIN_ERR}	V_{LDO4} = 3.3V		0.1		%
Integral Non-Linearity	INL	V_{LDO4} = 3.3V		1		LSB

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Digital Input Electrical Specifications (PWM, EN, SDA, SCL)						
Input High Threshold (7) (8)	V_{IH}	V_{IN} = 5.5V	1.6			V
Input Low Threshold (7) (8)	V_{IL}	V_{IN} = 2.9V			0.4	V
Input High Current	I_{IH}	V_{IN} = 5.5V	-1		+1	µA
Input Low Current	I_{IL}	V_{IN} = 5.5V	-1		+1	µA
Digital Output Electrical Specification (IRQ)						
IRQ Output Low Level	V_{OL}	I_{IRQ} ≤ 3mA			0.4	V
PWM Input Specification (PWM)						
PWM Input Frequency	f_{PWM}		0.2		50	kHz
I²C Interface Interface complies with slave mode I²C interface as described by Philips I²C specification version 2.1 dated January, 2000.						
Digital Input Voltage (7)	V_{B-IL}				0.4	V
	V_{B-IH}		1.6			V
SDA Output Low Level		I_{DIN} (SDA) ≤ 3mA			0.4	V
Digital Input Current	I_{B-IN}		-0.2		0.2	µA
Hysteresis of Schmitt Trigger Inputs	V_{HYS}			0.1		V
Maximum Glitch Pulse Rejection	t_{SP}			50		ns
I/O Pin Capacitance	C_{IN}			10		pF
I²C Timing						
Clock Frequency (7)	f_{SCL}			400	440	kHz
SCL Low Period (7) (8)	t_{LOW}		1.3			µs
SCL High Period (7) (8)	t_{HIGH}		0.6			µs
Data Hold Time (7) (8)	t_{HD_DAT}		0			µs
Data Setup Time (7) (8)	t_{SU_DAT}		100			ns
Setup Time for Repeated START Condition (7) (8)	t_{SU_STA}		0.6			µs
Hold Time for Repeated START Condition (7) (8)	t_{HD_STA}		0.6			µs
Setup Time for STOP Condition (7) (8)	t_{SU_STO}		0.6			µs
Bus-Free Time Between STOP and START (7) (8)	t_{BUF}		1.3			µs
Interface Start-up Time (7) (8)	t_{EN}	Bus start-up time after EN pin is pulled high			900	µs

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Fault Protection						
Over-Temperature	T_{OTP}	Rising threshold		165		°C
	T_{HYS}	Hysteresis		30		°C
Under Voltage Lockout	V_{UVLO}	Increasing V_{IN}		2.4		V
	$V_{UVLO-HYS}$			500		mV

Notes:

(1) Capacitors are MLCC of X5R type.

(2) EN is high for more than 10ms.

(3) Subscript for all backlights (BLn), n = 1, 2, 3, 4, 5, 6, and 7.

(4) Current matching is defined as $\pm [I_{BL(MAX)} - I_{BL(MIN)}] / [I_{BL(MAX)} + I_{BL(MIN)}]$.

(5) V_{DO} is defined as the voltage at the BLn pin when current has dropped from the target value by 10%.

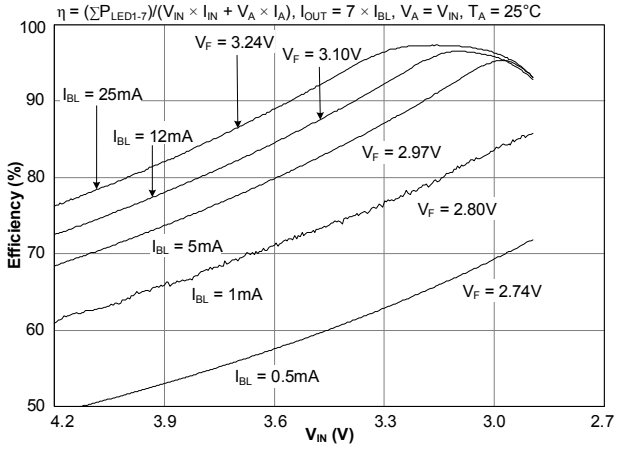
(6) Subscript m = 1, 3, and 4 and applies only to LDO1, LDO3, and LDO4. Subscripting for all LDOs (LDOn), n = 1, 2, 3, 4.

(7) The host processor must meet these limits.

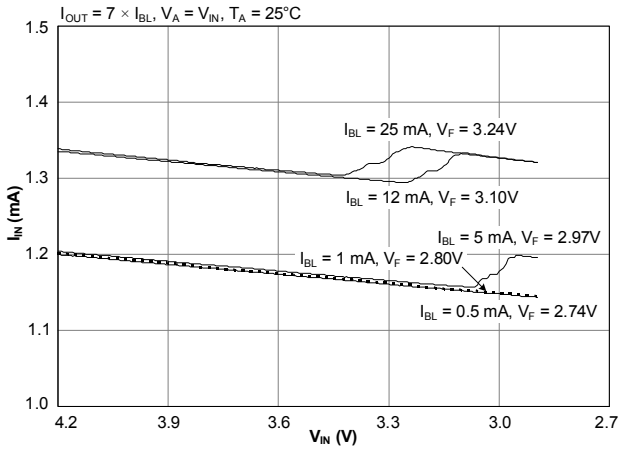
(8) Guaranteed by design.

Typical Characteristics — Backlights

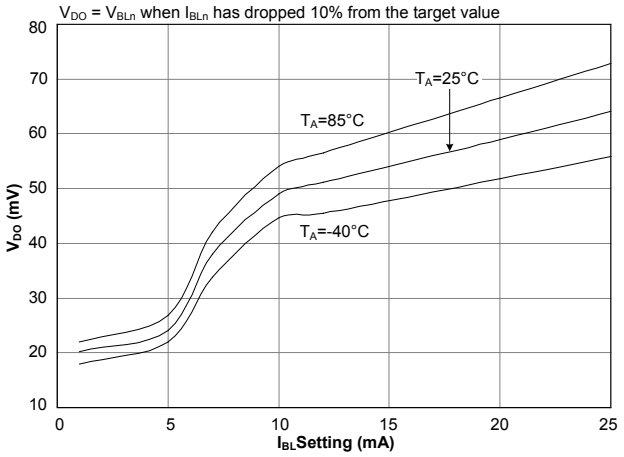
Backlight Efficiency (7 LEDs)



Supply Current (7 LEDs)



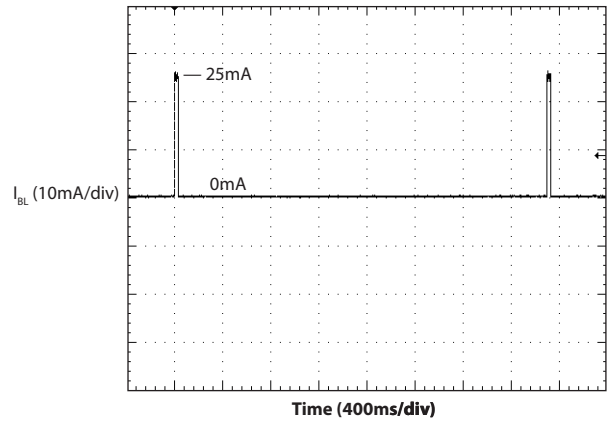
Dropout Voltage V_{DO} vs I_{BL} (6 LEDs)



Typical Characteristics — Backlights (continued)

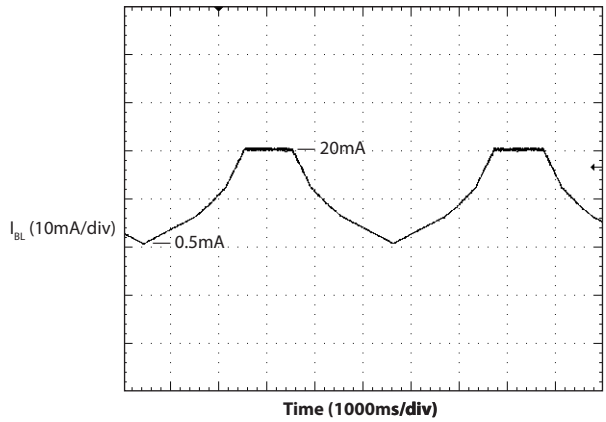
Group #1 Blink Function (25mA)

Start time = 32ms, target time = 3072ms



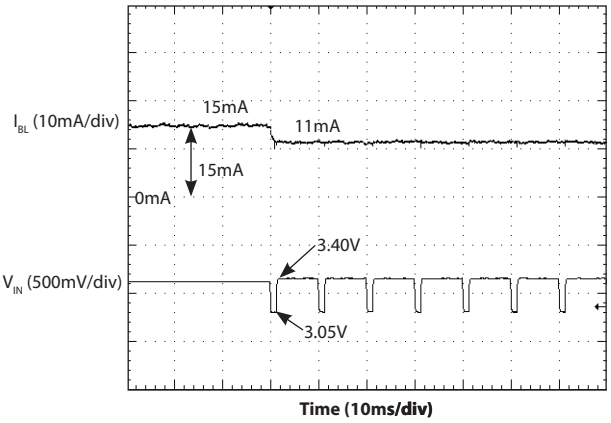
Group #1 Breathe Function (20mA to 0.5mA)

Breathe rate = 24ms, start time = 32ms, target time = 1024ms



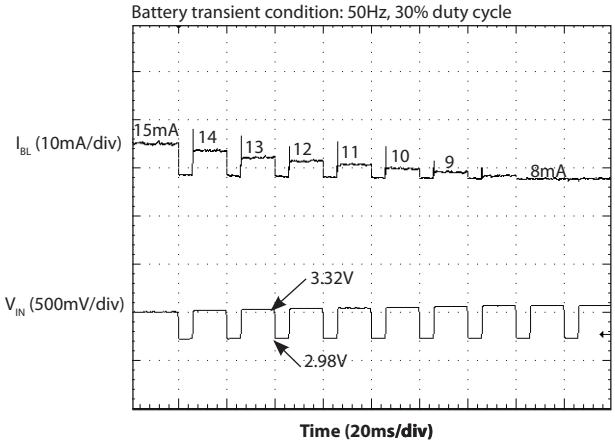
Bank #1 with ADP (rate = 256µs)

Battery transient condition: 100Hz, 12.5% duty cycle



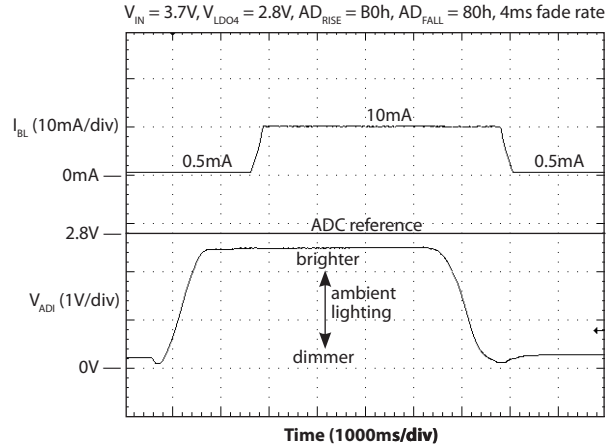
Backlight with ADP (rate = 4ms)

Battery transient condition: 50Hz, 30% duty cycle



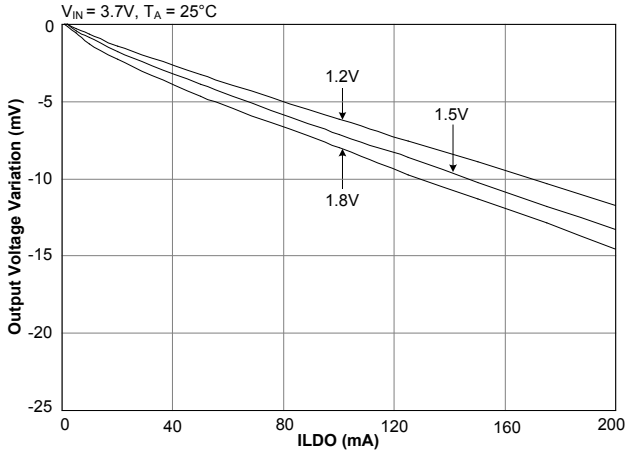
Backlight Dimming with ALS and Fade

V_{IN} = 3.7V, V_{LDO4} = 2.8V, AD_{RISE} = B0h, AD_{FALL} = 80h, 4ms fade rate

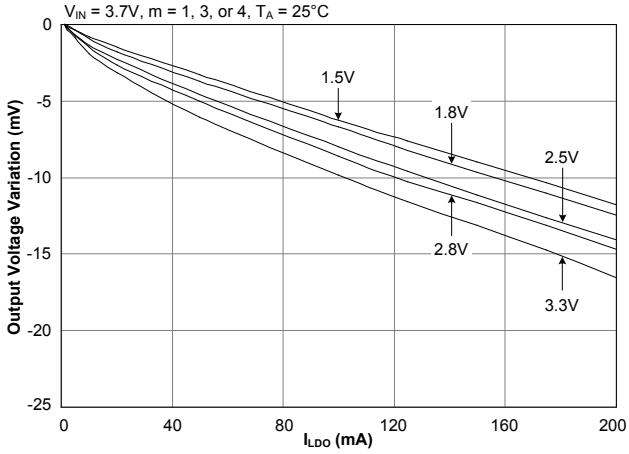


Typical Characteristics — LDOs

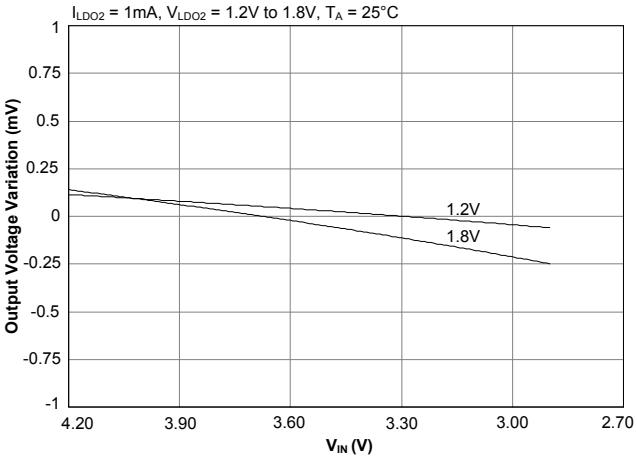
Load Regulation (LDO2)



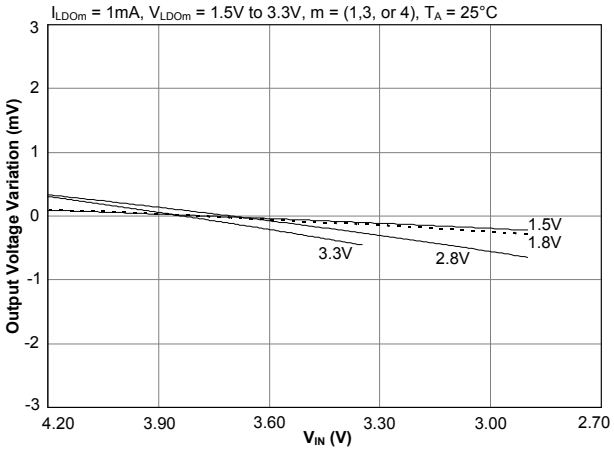
Load Regulation (LDOm)



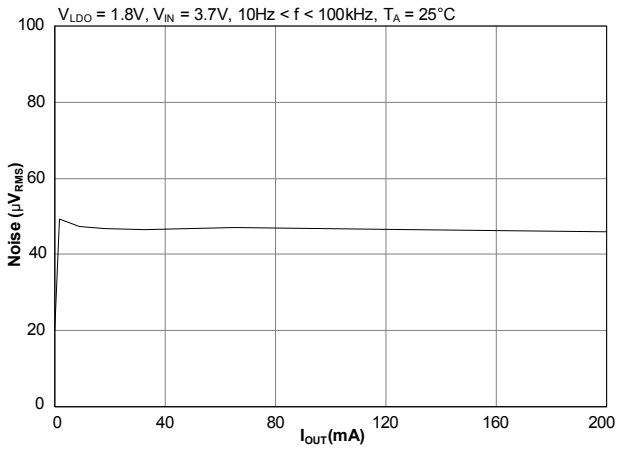
Line Regulation (LDO2)



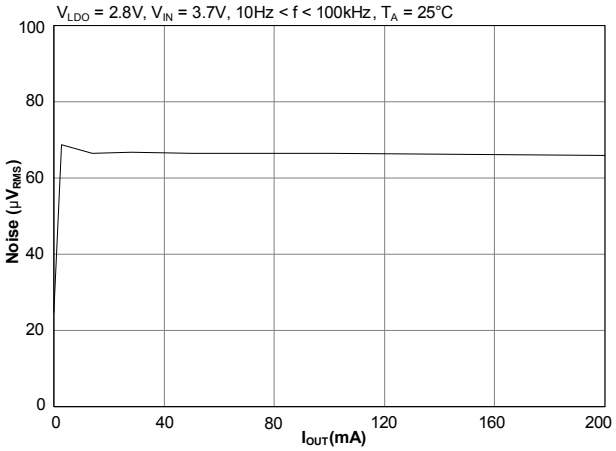
Line Regulation (LDOm)



LDO Noise vs. Load Current (1.8V)

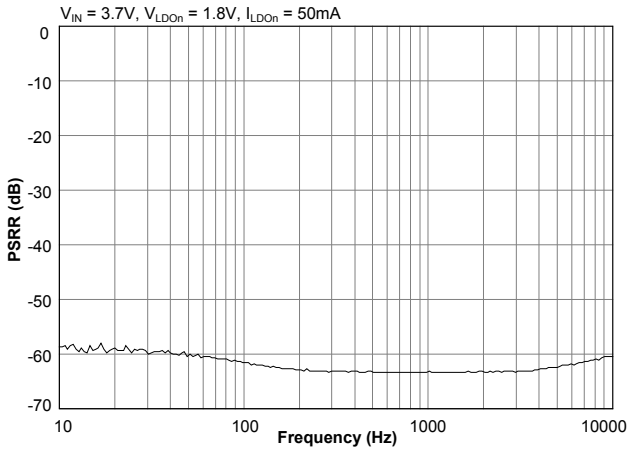


LDO Noise vs. Load Current (2.8V)

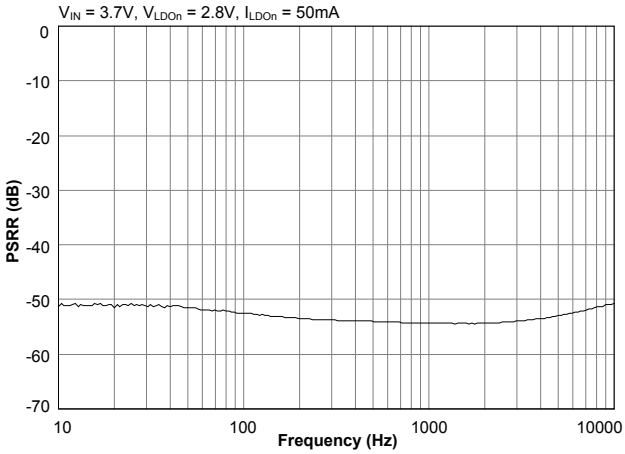


Typical Characteristics — LDOs (continued)

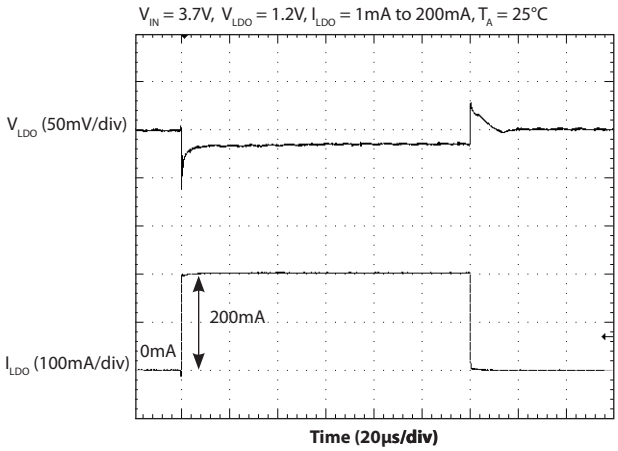
PSRR vs. Frequency (1.8V)



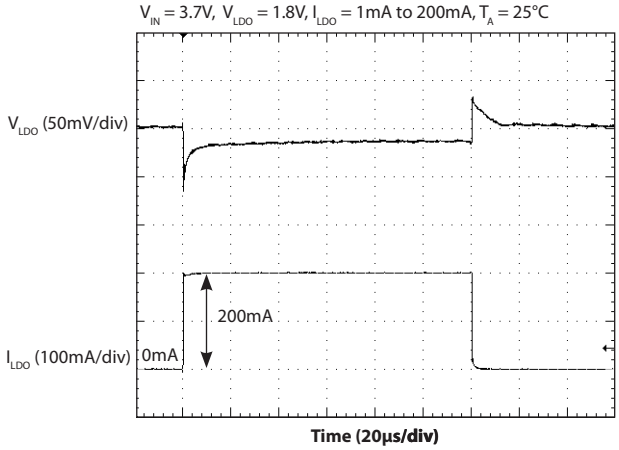
PSRR vs. Frequency (2.8V)



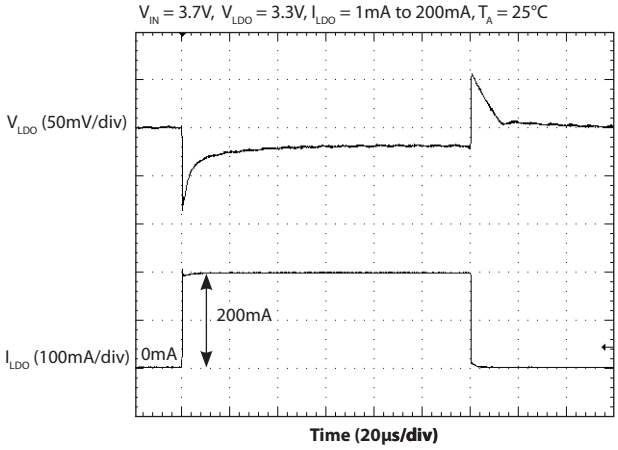
Load Transient Response (1.2V)



Load Transient Response (1.8V)



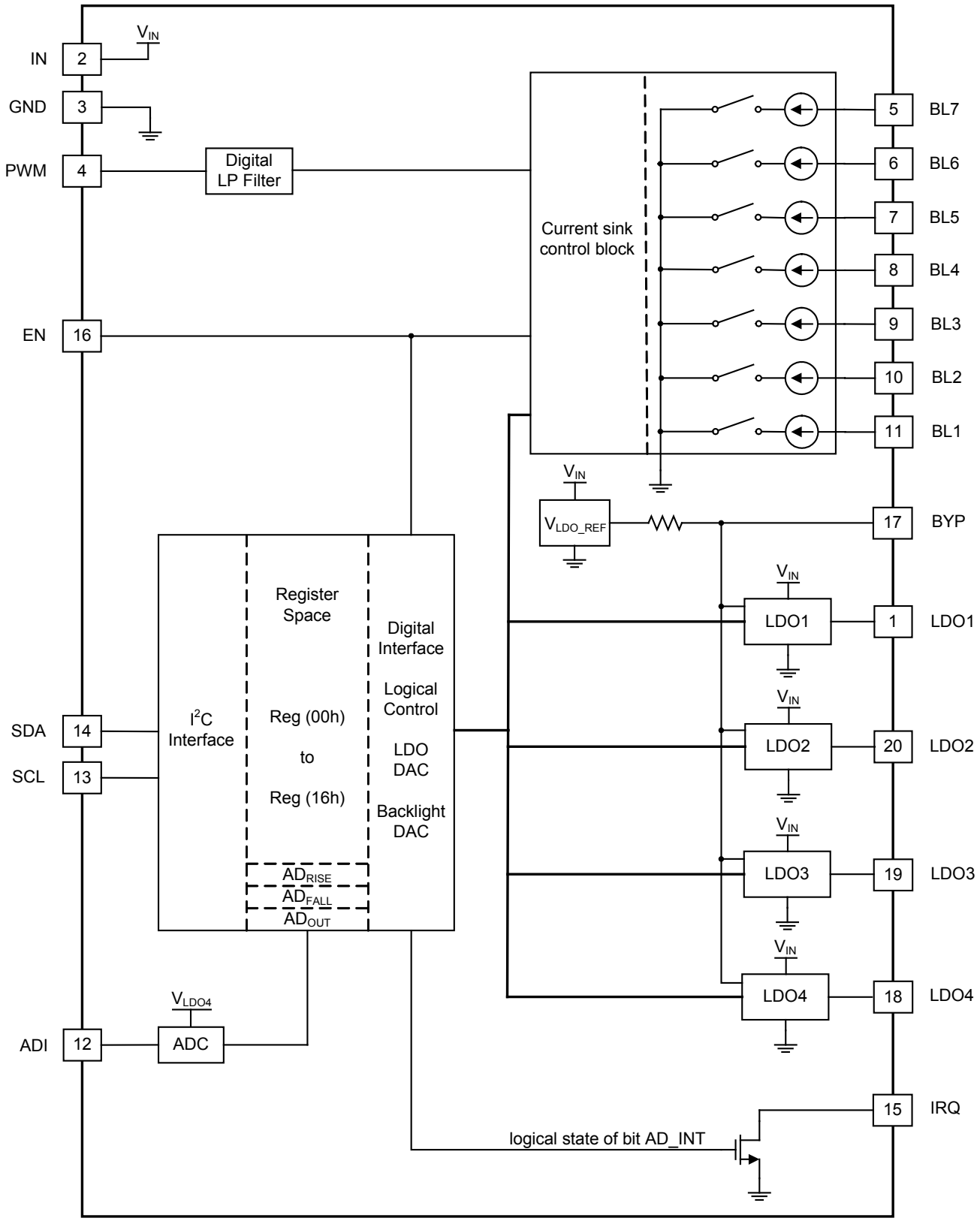
Load Transient Response (3.3V)



Pin Descriptions

Pin #	Pin Name	Pin Function
1	LDO1	LDO1 output
2	VIN	Battery voltage input
3	GND	Ground pin
4	PWM	Backlight PWM control signal input
5	BL7	Current sink output for backlight LED 7 — leave this pin open or grounded if unused
6	BL6	Current sink output for backlight LED 6 — leave this pin open or grounded if unused
7	BL5	Current sink output for backlight LED 5 — leave this pin open or grounded if unused
8	BL4	Current sink output for backlight LED 4 — leave this pin open or grounded if unused
9	BL3	Current sink output for backlight LED 3 — leave this pin open or grounded if unused
10	BL2	Current sink output for backlight LED 2 — leave this pin open or grounded if unused
11	BL1	Current sink output for backlight LED 1 — leave this pin open or grounded if unused
12	ADI	ADC input — connect this pin to ground if unused
13	SCL	I^2C clock input — I^2C buss pull-up resistor is required.
14	SDA	I^2C data — bi-directional line used for read and write operations for all internal registers (refer to Register Map and I^2C Interface sections) — I^2C buss pull-up resistor is required.
15	IRQ	Interrupt request — open-drain output, active-low
16	EN	Chip enable — active high
17	BYP	Bypass pin for LDO reference — connect a 22nF ceramic capacitor to GND
18	LDO4	LDO4 output
19	LDO3	LDO3 output
20	LDO2	LDO2 output
T	THERMAL PAD	Thermal pad for heatsinking purposes — connect to ground plane using multiple vias — not connected internally

Block Diagram



Applications Information

General Description

The SC667 is optimized for handheld applications supplied from a single cell Li-Ion and includes the following key functions:

- Seven matched current sinks — BL1, BL2, BL3, BL4, BL5, BL6, and BL7 regulate LED backlighting current, with 0mA to 25mA per LED.
- Four adjustable LDOs — LDO1, LDO3, and LDO4 are adjustable with 15 settings from 1.5V to 3.3V. LDO2 is adjustable with 7 settings from 1.2V to 1.8V.
- ALS with a sigma-delta ADC that can also be used for general purpose ADC functions.
- PWM with an internal digital low-pass filter
- I^2C Bus fast mode and standard mode

LED Backlight Current Settings

The backlight current is set via the I^2C interface. The current is regulated to one of 32 values between 0mA and 25mA. The step size varies depending upon the current setting. The first three steps are 50µA, 100µA, and 200µA. Between 0.5mA and 5mA, the step size is 0.5mA. The step size increases to 1mA for settings between 5mA and 21mA. Steps are 2mA between 21mA and 25mA. The variation in step size allows finer adjustment for dimming functions in the low current range and coarse adjustment at higher current settings where larger changes are not visible. The settings are psuedo-logarithmic. A zero setting also disables the current sink, providing an alternative to the enable bit.

LED Backlight Current Sinks

Backlight current is independent of forward voltage mismatch (ΔV_F) between LEDs. When two or more backlight sinks are set to the same target current, their currents will match, even if the LED voltages are different. The backlight current sinks are designed with a low dropout voltage (typically 59mV for a bank of 6 LEDs at 20mA) to optimize run-time when the LED anode voltage is provided by a battery.

LED Anode Supply

In the typical application circuit, the battery voltage supplies the LEDs. An alternative to this configuration is to connect the LED anodes to a second DC supply as shown in Figure 1. Such a connection is especially useful when an alternate voltage that is slightly higher than the forward voltage of the LEDs is available. The resulting efficiency in this scenario would be optimal. To achieve best accuracy, the current sink amplifier requires the LED sink pin (BLn) to be within the operational range of $V_{DO} \le V_{BLn} \le 4.2V$. When the sink is off, V_{BLn} may float as high as 5.5V.

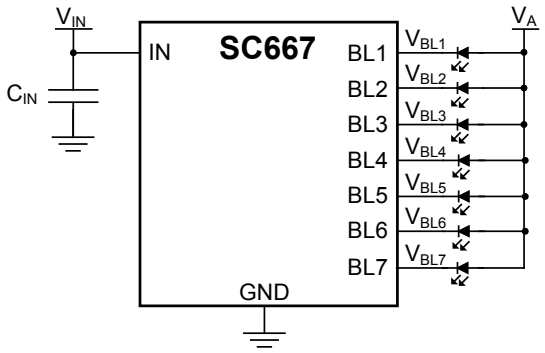


Figure 1 — Anode Supply

Unused Backlight Current Sinks

The backlight LEDs default to the off state upon power-up. For backlight applications using fewer than 7 LEDs, any unused output must be left open or grounded and the unused LED must remain disabled. When writing to the backlight enable register, a zero (0) must be written to the corresponding enable bit of any unused output.

Backlight Quiescent Current

The quiescent current required to operate the backlights is reduced when backlight current is less than 8.0mA. This feature results in higher efficiency under light-load conditions. Further quiescent current reduction will result from using fewer LEDs.

Backlight Configuration into Banks

The seven LED backlight drivers can be assigned to a single bank or divided among up to four independent banks — refer to the Register Map section for more details. The independent banks can each be configured with different settings for backlight current and fade operation.

Bank Configuration into Groups

The four backlight banks can be assigned to two groups (group #1 and group #2). Each group provides independent settings for the fade and breathe effect rate options. Each group also provides independent settings for target time and start time, which are used to customize the

Applications Information (continued)

blink and breathe lighting effects. Details of the fade, breathe, and blink effects are introduced later in this Applications Information section.

Target Backlight Settings for Lighting Effects

The target backlight setting is the current which will result at the end of a blink or breathe lighting effect cycle. The Register Map contains four control registers which set the target backlight currents for each bank. Registers 06h, 07h, 08h, and 09h contain the target current values for: bank #1, bank #2, bank #3, and bank #4, respectively.

Bank #1 also uses the target value of register 06h in association with the ALS function. Bank #1 can be set to automatically change to the target value of register 06h when the ADC exceeds a programmable rising threshold. ALS is defined in more detail under Ambient Light Sense, and in the Register Map section under ADC Function Register 12h.

Breathe Lighting Effect

The breathe lighting effect may be applied independently to each group. When this feature is enabled, the bank's backlight current will increase and decrease periodically at a rate that mimics calm and smooth breathing. Once initialized via the I^2C interface, this function will run continuously, independent of the host processor, saving instruction cycles and simplifying timing requirements.

Three timing parameters must be set to define the breathe effect timing: effect rate, start time, and target time. Group #1 and group #2 have independent timing parameters to support a variety of options. When a bank is assigned to a group, it adopts the timing parameters of the respective group.

When enabled, the breathe function causes the backlights to change brightness by stepping the current incrementally, using the effect rate parameter, until the final backlight current is reached. The current will remain at the target value for a time set by the target time parameter. When the target time has ended, the brightness will again change, this time in reverse order, stepping the current incrementally, using the effect rate parameter, until the current returns to the start value. The current will remain at the start value for the time set by the start time parameter. When the start time has ended, the breathe cycle begins again.

The breathe effect rate is programmable for group #1 and group #2 and can be independently set to 4, 8, 16, 24, 32, 48, or 64ms for each group. Also, the start time and target time parameters for group #1 and group #2 can be independently set to 32, 64, 256, 512, 1024, 2048, 3072, or 4096ms.

In addition to the group's timing parameters, start current and target current values and BxBEN (blink/breathe enable) and BxFEN (fade enable) bits are set for each bank to define that bank's min and max current during a breathe cycle and enable the breathe function.

The five parameters that define the breathe effect are:

1. Effect rate — write value to register 0Fh
2. Start current — write value to register 02h, 03h, 04h, or 05h (bank dependent)
3. Target current — write value to registers 06, 07h, 08h, or 09h (bank dependent)
4. Start time — write value to register 10h or 11h (group dependent)
5. Target time — write to register 10h or 11h (group dependent

Figure 3 illustrates the breathe effect with respect to time. For an example of the breathe effect, with bank #1 assigned to group #1, the terms used in the illustration are as follows:

- I_{BL_START} = contents of register 02h (B1FEN must equal 1)
- I_{BL_TARGET} = contents of register 06h (B1BEN must equal 1)
- t_{START} = contents of bits ST1_[2:0] in register 10h
- t_{TARGET} = contents of bits TT1_[2:0] in register 10h
- $t_{BREATHE}$ = breathe time. Equal to the breathe rate times the number of steps between I_{BL_START} and I_{BL_TARGET}. Breathe time is set with the bits ER1_[2:0] in register 0Fh.

Blink Lighting Effect

The blink lighting effect provides an automatic LED blinking function that can be applied to a single LED driver or

Applications Information (continued)

an LED driver bank without any host processor interaction. Blinking can be initialized via the I²C interface at power up and the settings maintained in the SC667 registers with no need for additional software interaction.

Two timing parameters must be set to define the blink effect timing: start time and target time. Start and target times can be independently set to 32, 64, 256, 512, 1024, 2048, 3072, 4096ms. The total blink cycle time is equal to the sum of the start and target times.

In addition to timing parameters, start current and target current values are used to set the bank's min and max current, and a combination of bits BxBEN (blink/breathe enable) and BxFEN (fade enable) are used to enable the blink function.

The four parameters are:

1. Start current — write value to register 02h, 03h, 04h, or 05h (bank dependent)
2. Target current — write value to register 06, 07h, 08h, or 09h (bank dependent)
3. Start time — write value to register 10h or 11h (group dependent)
4. Target time — write to register 10h or 11h (group dependent)

Figure 4 illustrates the blink effect with respect to time. For an example of the blink effect, with bank #2 assigned to group #2, the terms used in the illustration are as follows:

- I_{BL_START} = contents of register 03h (B2FEN must equal 0)
- I_{BL_TARGET} = contents of register 07h (B2BEN must equal 1)
- t_{START} = contents of bits ST2_[2:0] in register 11h
- t_{TARGET} = contents of bits TT2_[2:0] in register 11h

Backlight Fade-In and Fade-Out Lighting Effects

When enabled, the fade function causes the backlights to change brightness by stepping the current incrementally until the final backlight current is reached. The backlight fade-in and fade-out may be applied to selected banks. When enabled, the bank current will gradually increase during fade-in and gradually decrease during fade-out. The rate of increase or decrease is programmable for group #1 and group #2 and can be independently set to 1, 2, 4, 6, 8, 12, or 16ms for each group. The fade function causes the bank to begin stepping from its current state to the next programmed state as soon as the new state is stored in its register. For example, if the bank is set to 25mA, fade is enabled, and the bank is changed to 0mA, the bank will step from 25mA down to 0mA using all settings between 25mA and 0mA.

In addition to the 32 programmable backlight current values, there are also 75 non-programmable current steps. The non-programmable steps are active only during a fade or breathe operation to provide for a very smooth change in backlight brightness. Backlight current steps proceed at a programmable fade rate of 1, 2, 4, 6, 8, 12, or 16ms. The exact length of time used to fade between any two backlight values is determined by multiplying the fade rate by the number of steps between the old and new backlight values. The fade time can be calculated from the data provided in Table 1 on page 19.

Two parameters must be programmed to enable the fade effects: effect rate and start current. The fade function will begin when a new start current is set along with the FEN bit in the associated register.

The fade effect rate parameter must be set to define the fade timing. Group #1 and group #2 have independent sets of timing parameters to support a variety of fade timing options. When a bank is assigned to a group, it adopts the timing parameters of the respective group.

Registers associated with fade are described below:

1. Effect Rate — write a value to register 0Fh (group dependent)
2. Start Current — write value to register 02h, 03h, 04h, or 05h (bank dependent)

Figure 5 illustrates the fade-in and fade-out effects with respect to time. For an example of the fade effects assigned to bank 3 with effect rate 2, the terms in the illustration are as follows:

- $I_{BL_INITIAL}$ = contents of register 04h (B3FEN must equal 1)

Applications Information (continued)

- I_{BL_FINAL} = new value written to register 04h (register 07h bit B3BEN must equal 0), however, the "Target" value of register 07h has no effect on fade.
- t_{FADE_IN} = contents of bits ER2_[2:0] in register 0Fh
- $t_{FADE_OUT} = t_{FADE_IN}$

Auto-Dim Lighting Effect

Two auto-dim settings are provided — auto-dim full and auto-dim partial. These settings provide automatic dimming of bank #1. The auto-dim delay times are set using the group #1 target and start time register (10h). Delay times are 8 times the group #1 target and start times.

Auto-dim full provides a time-out and dimming function followed by a time-out and turn-off function. Auto-dim full begins when the bank is enabled (or re-enabled), the bank will first go to the target current and wait for a count of 8 times the group #1 target time. The bank will then dim to the "start" current and wait for a count of 8 times the group #1 start time. The bank will then turn off.

Auto dim partial provides the time-out and dimming function, but does not turn off backlights. Auto-dim partial begins when the bank is enabled (or re-enabled), the bank will first go to the target current and wait for a count of 8 times the group #1 target time. The bank will then dim to the "start" current. The bank will not turn off automatically.

Auto-dim is available only for group #1. After selecting an auto-dim option, the bank's blink effect must be enabled to enable auto-dim. The bank must then be enabled or re-enabled to begin the auto-dim. Auto-dim partial is illustrated in Figure 6, and auto-dim full is illustrated in Figure 7.

Brightness Change without Effects

There are two ways to change brightness while using no lighting effect. One way is to set the effect rate option to the zero value "snap to target" (a function of register 0Fh). This method will block all lighting effects on all banks within a group. Another way to change brightness, with no lighting effect, is to set the BxFEN and BxBEN both equal to zero. This second method will block all lighting effects on a single bank, and with no influence over other banks within the group.

Writing a new value to the backlight current register, while effects are disabled, will cause the change in brightness to occur immediately. When changing brightness without effects, registers 02h through 05h are used for this function. The target values of registers 06h through 09h are not involved.

Figure 8 illustrates the brightness change with respect to time. An example of brightness change to bank #4 with no lighting effect, is as follows:

- $I_{BL_INITIAL}$ = previous value written to register 05h
- I_{BL_FINAL} = new value written to register 05h

The register 05h bit B4FEN must equal 0, and register 09h bit B4BEN must equal 0, however, the "Target" value of register 09h has no effect on the final current.

Fade State Diagram

The state diagram in Figure 2 describes the fade operation. If the backlight enable bits are disabled during an

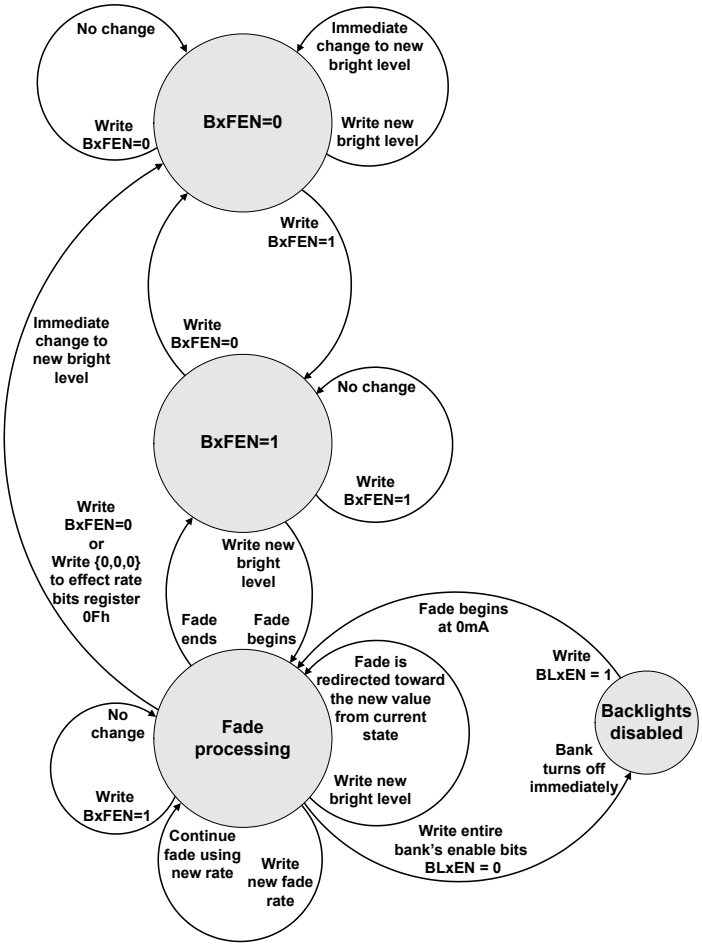


Figure 2 — State Diagram for Fade Function

Applications Information (continued)

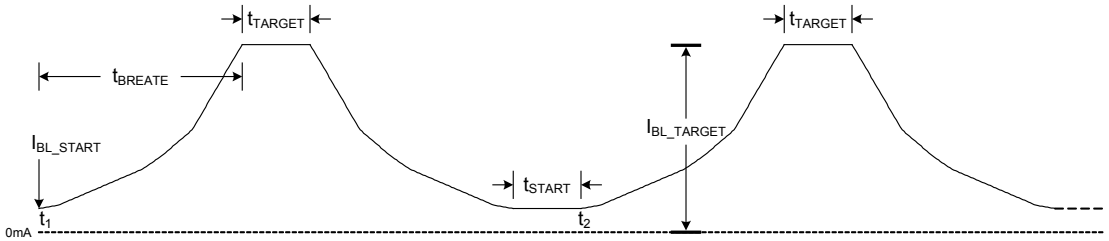


Figure 3 — Breathe Timing Diagram

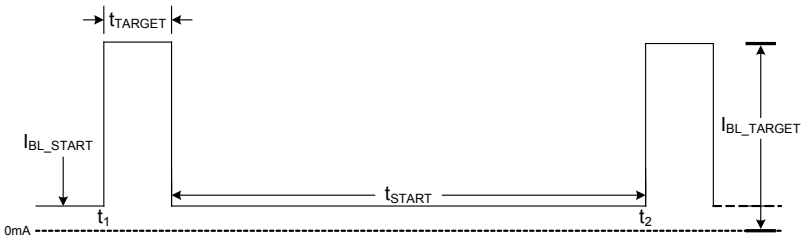


Figure 4 — Blink Timing Diagram

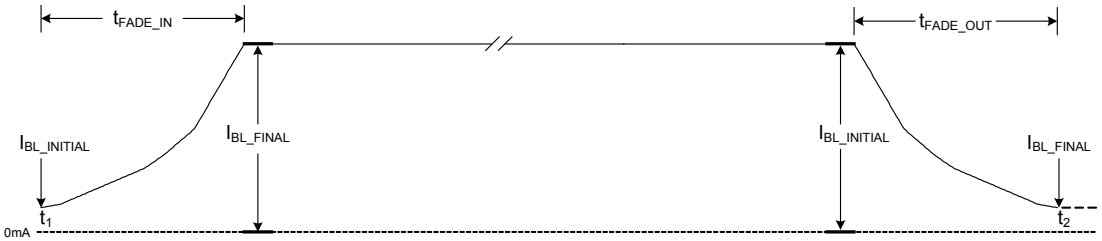


Figure 5 — Fade-in and Fade-out Timing Diagram

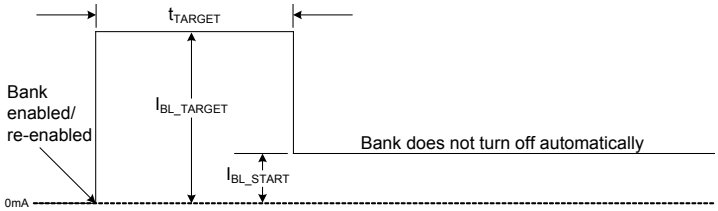


Figure 6 — Auto-Dim Partial Timing Diagram

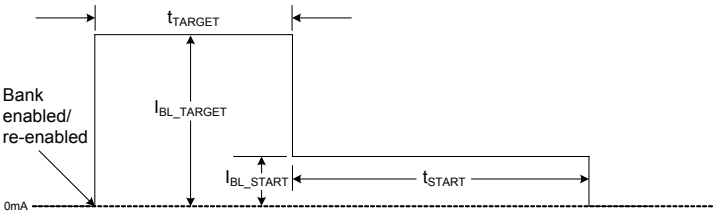


Figure 7 — Auto-Dim Full Timing Diagram

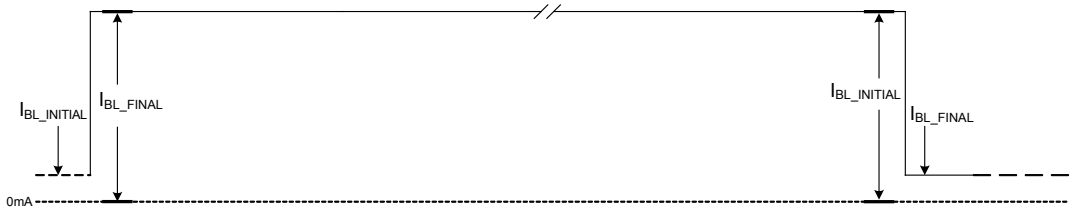


Figure 8 — Brightness Increase and Decrease Without Fade Timing Diagram

Note: See next page for figure notes.

Applications Information (continued)

Notes for figures on previous page

t_1 = start of cycle

t_2 = end of cycle

t_{START} = The time that the bank's current remains at the start value.

t_{TARGET} = The time that the bank's current remains at the target value.

$t_{BREATHE}$ = The time that the bank's current will continue to increase or decrease during a breathe cycle. Breathe time is determined by multiplying the breathe rate by the number of steps (from Table1). Breathe rate is a group dependent value of the effect rate register 0Fh.

t_{FADE_IN} = The fade time of increasing bank current, determined by multiplying the fade rate by the number of steps (from Table 1). Fade rate is a group dependent value of the effect rate register 0Fh.

t_{FADE_OUT} = The fade time of decreasing bank current, determined by multiplying the fade rate by the number of steps (from Table 1). Fade rate is a group dependent value of the effect rate register 0Fh. t_{FADE_IN} is always equal to t_{FADE_OUT}.

I_{BL_START} = The bank current at the start of the cycle. This is the bank dependent value of register 02h, 03h, 04h, or 05h.

I_{BL_TARGET} = The bank current at the end of the cycle. This is the bank dependent value of register 06h, 07h, 08h, or 09h.

$I_{BL_INITIAL}$ = The bank dependent value of register 02h, 03h, 04h, or 05h.

I_{BL_FINAL} = The bank dependent value of register 02h, 03h, 04h, or 05h.

NOTE: "START" and "TARGET" subscripts apply only to blink and breathe effects which require a target value to complete a cycle. "INITIAL" and "FINAL" subscripts apply when changing a bank's current without use of the target registers.

Applications Information (continued)

Table 1 — Number of Backlight Fade / Breathe Steps between Values (See Note)

Starting Value (mA) \ Ending Value (mA)	0.0	0.05	0.1	0.2	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	6.0	7.0	8.0	9.0	10.0	11.0	12.0	13.0	14.0	15.0	16.0	17.0	18.0	19.0	20.0	21.0	23.0	25.0
25	106	105	104	102	96	90	88	84	80	76	72	68	64	60	52	47	42	38	34	30	26	24	22	20	18	16	14	12	10	8	4	0
23	102	101	100	98	92	86	84	80	76	72	68	64	60	56	48	43	38	34	30	26	22	20	18	16	14	12	10	8	6	4	0	4
21	98	97	96	94	88	82	80	76	72	68	64	60	56	52	44	39	34	30	26	22	18	16	14	12	10	8	6	4	2	0	4	8
20	96	95	94	92	86	80	78	74	70	66	62	58	54	50	42	37	32	28	24	20	16	14	12	10	8	6	4	2	0	2	6	10
19	94	93	92	90	84	78	76	72	68	64	60	56	52	48	40	35	30	26	22	18	14	12	10	8	6	4	2	0	2	4	8	12
18	92	91	90	88	82	76	74	70	66	62	58	54	50	46	38	33	28	24	20	16	12	10	8	6	4	2	0	2	4	6	10	14
17	90	89	88	86	80	74	72	68	64	60	56	52	48	44	36	31	26	22	18	14	10	8	6	4	2	0	2	4	6	8	12	16
16	88	87	86	84	78	72	70	66	62	58	54	50	46	42	34	29	24	20	16	12	8	6	4	2	0	2	4	6	8	10	14	18
15	86	85	84	82	76	70	68	64	60	56	52	48	44	40	32	27	22	18	14	10	6	4	2	0	2	4	6	8	10	12	16	20
14	84	83	82	80	74	68	66	62	58	54	50	46	42	38	30	25	20	16	12	8	4	2	0	2	4	6	8	10	12	14	18	22
13	82	81	80	78	72	66	64	60	56	52	48	44	40	36	28	23	18	14	10	6	2	0	2	4	6	8	10	12	14	16	20	24
12	80	79	78	76	70	64	62	58	54	50	46	42	38	34	26	21	16	12	8	4	0	2	4	6	8	10	12	14	16	18	22	26
11	76	75	74	72	66	62	58	54	50	46	42	38	34	30	22	17	12	8	4	0	4	6	8	10	12	14	16	18	20	22	26	30
10	72	71	70	68	62	58	54	50	46	42	38	34	30	26	18	13	8	4	0	4	8	10	12	14	16	18	20	22	24	26	30	34
9	68	67	66	64	58	54	50	46	42	38	34	30	26	22	14	9	4	0	4	8	12	14	16	18	20	22	24	26	28	30	34	38
8	64	63	62	60	54	50	46	42	38	34	30	26	22	18	10	5	0	4	8	12	16	18	20	22	24	26	28	30	32	34	38	42
7	59	58	57	55	49	45	41	37	33	29	25	21	17	13	5	0	5	9	13	17	21	23	25	27	29	31	33	35	37	39	43	47
6	54	53	52	50	44	40	36	32	28	24	20	16	12	8	0	5	10	14	18	22	26	28	30	32	34	36	38	40	42	44	48	52
5	46	45	44	42	36	32	28	24	20	16	12	8	4	0	8	13	18	22	26	30	34	36	38	40	42	44	46	48	50	52	56	60
4.5	42	41	40	38	32	28	24	20	16	12	8	4	0	4	12	17	22	26	30	34	38	40	42	44	46	48	50	52	54	56	60	64
4	38	37	36	34	28	24	20	16	12	8	4	0	4	8	16	21	26	30	34	38	42	44	46	48	50	52	54	56	58	60	64	68
3.5	34	33	32	30	24	20	16	12	8	4	0	4	8	12	20	25	30	34	38	42	46	48	50	52	54	56	58	60	62	64	68	72
3.0	30	29	28	26	20	16	12	8	4	0	4	8	12	16	24	29	34	38	42	46	50	52	54	56	58	60	62	64	66	68	72	76
2.5	26	25	24	22	16	12	8	4	0	4	8	12	16	20	28	33	38	42	46	50	54	56	58	60	62	64	66	68	70	72	76	80
2.0	22	21	20	18	12	8	4	0	4	8	12	16	20	24	32	37	42	46	50	54	58	60	62	64	66	68	70	72	74	76	80	84
1.5	18	17	16	14	8	4	0	4	8	12	16	20	24	28	36	41	46	50	54	58	62	64	66	68	70	72	74	76	78	80	84	88
1.0	14	13	12	10	4	0	4	8	12	16	20	24	28	32	40	45	50	54	58	62	64	66	68	70	72	74	76	78	80	82	86	90
0.5	10	9	8	6	0	4	8	12	16	20	24	28	32	36	44	49	54	58	62	66	70	72	74	76	78	80	82	84	86	88	92	96
0.2	4	3	2	0	6	10	14	18	22	26	30	34	38	42	50	55	60	64	68	72	76	78	80	82	84	86	88	90	92	94	98	102
0.1	2	1	0	2	8	12	16	20	24	28	32	36	40	44	52	57	62	66	70	74	78	80	82	84	86	88	90	92	94	96	100	104
0.05	1	0	1	3	9	13	17	21	25	29	33	37	41	45	53	58	63	67	71	75	79	81	83	85	87	89	91	93	95	97	101	105
0.0	0	1	2	4	10	14	18	22	26	30	34	38	42	46	54	59	64	68	72	76	80	82	84	86	88	90	92	94	96	98	102	106

NOTE

The fade time is determined by multiplying the number of steps by the fade rate (fade steps × fade rate = fade time).

The breathe time is determined by multiplying the number of steps by the breathe rate (breathe steps × breathe rate = breathe time).

Applications Information (continued)

ongoing fade, the bank will turn off immediately. When the backlight bits are re-enabled and BxFEN = 1, the backlight currents will begin at 0mA and fade to the value determined by the backlight current register bits IBx[4:0]. If the backlight enable bits are re-enabled and BxFEN = 0, the main backlights will proceed immediately to the value of IBx[4:0]. Note that the words "target value" are not used to describe the final value after a fade operation. "Target value" is reserved for describing the backlight settings at the end of the blink or breathe effect cycles.

Non-Programmable Backlight Steps

In addition to the 32 programmable backlight steps, there are 75 non-programmable steps which are used only during a fade or breathe operation. Table 1 provides the total number of steps between the starting and ending value of any fade or breathe operation. The value from Table 1 is multiplied by the fade rate to determine the total fade time. The maximum possible fade-in duration, from 0mA to 25mA, or fade-out duration, from 25mA to 0mA, is equal to 106 x 16ms = 1696ms.

Figures 10 through 14 provide additional information about the non-programmable steps. Each figure represents one linear segment of the overall fade range shown in Figure 15. The overall fade range is a piece-wise linear approximation of a logarithmic function which provides for a very smooth visual fading or breathing effect.

The fade rate may be changed dynamically when a fade operation is active by writing new values to the fade register. When a new backlight level is written during an ongoing fade operation, the fade will be redirected to the new value from the present state. An ongoing fade operation may be cancelled by disabling fade, which will result in the backlight current changing immediately to the final value. If fade is disabled, the current level will change immediately to the final value without the fade delay.

PWM Operation on Bank #1

A PWM signal on the PWM pin can be used to adjust the DC current through the LEDs in bank #1. When the duty cycle is 100%, the backlight current through each LED (I_{BL}) equals the full scale current value set for bank #1. The PWM input samples voltage at the PWM pin and converts the duty cycle to a DC current level. A DC current is passed through the LEDs, providing lower noise compared to the more conventional pulsed current PWM method.

PWM Sampling

The sampling system that translates the PWM signal to a DC current requires the PWM pin to have a minimum high time t_{HIGH_MIN} to set the DC level. High time less than t_{HIGH_MIN} impacts the accuracy of the target I_{BL}. The minimum duty cycle needed to support the minimum high time specification varies with the applied PWM frequency (see Figure 9). Note that use of a lower PWM frequency, from 200Hz to 10kHz, will support a lower minimum duty cycle and an extended backlight dimming range.

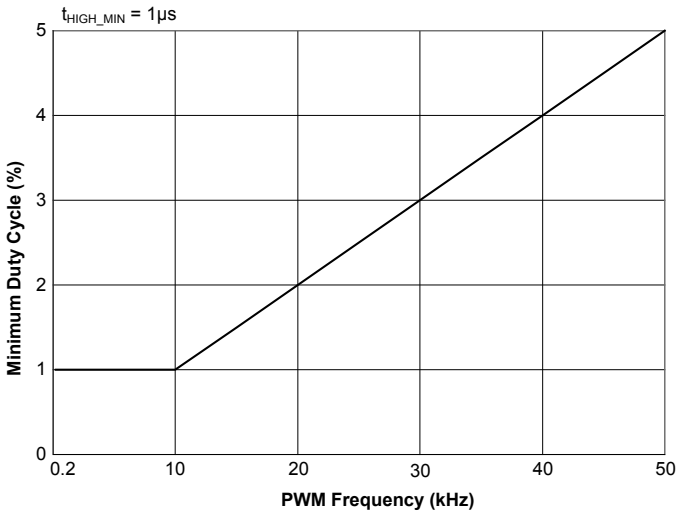


Figure 9 — Minimum Duty Cycle

Ambient Light Sense

The SC667 includes a general purpose sigma-delta ADC that is designed to interface with an ambient light sensor. The ADC input accepts the output of an external ambient light sensor circuit. When the ADC is enabled via the I^2C bus, the analog signal produced by the ambient light sensor is compared with two user programmable threshold levels. The result of the comparison is then used to automatically change the brightness of the LEDs in bank #1 to a user defined value. This function is used to compensate for ambient lighting conditions — increasing brightness where brighter ambient conditions exist and decreasing brightness in lower lighting conditions.

Applications Information (continued)

NOTES: ● = Programmable backlight steps, o = Non-programmable fade/breathe steps

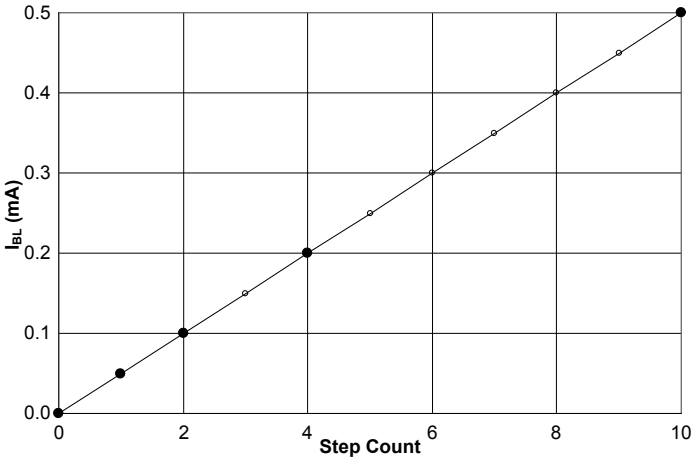


Figure 10 — Backlight Steps (0.0mA to 0.5mA)

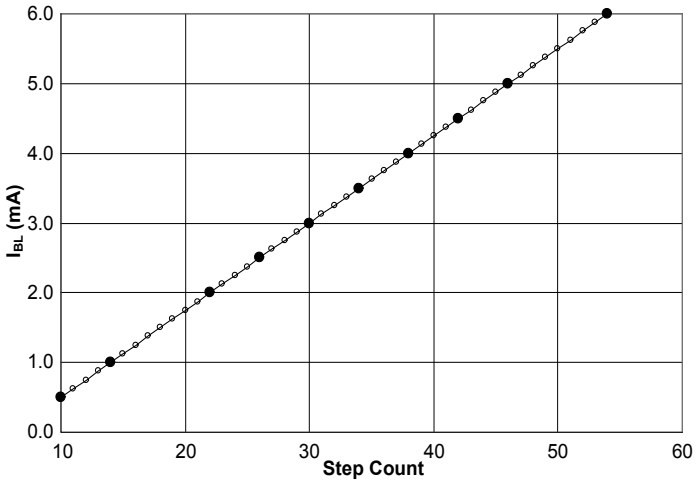


Figure 11 — Backlight Steps (0.5mA to 6.0mA)

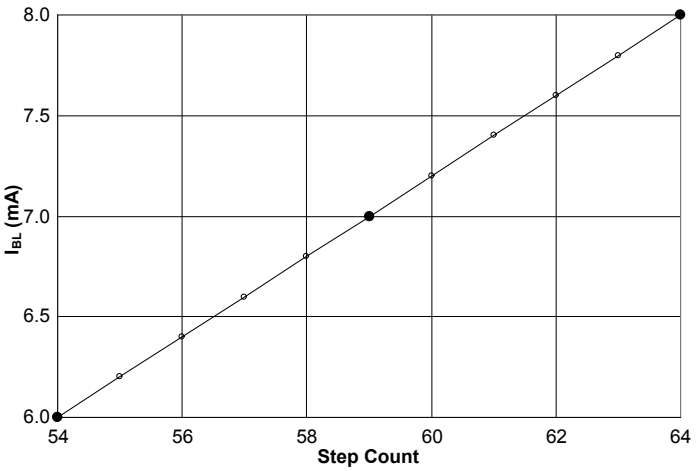


Figure 12 — Backlight Steps (6.0mA to 8.0mA)

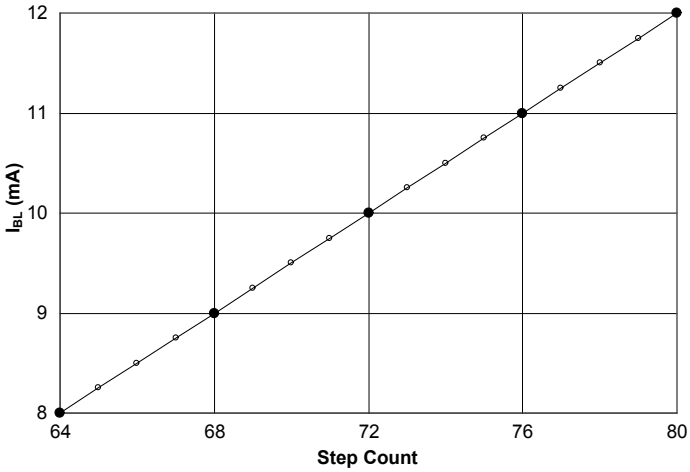


Figure 13 — Backlight Steps (8.0mA to 12.0mA)

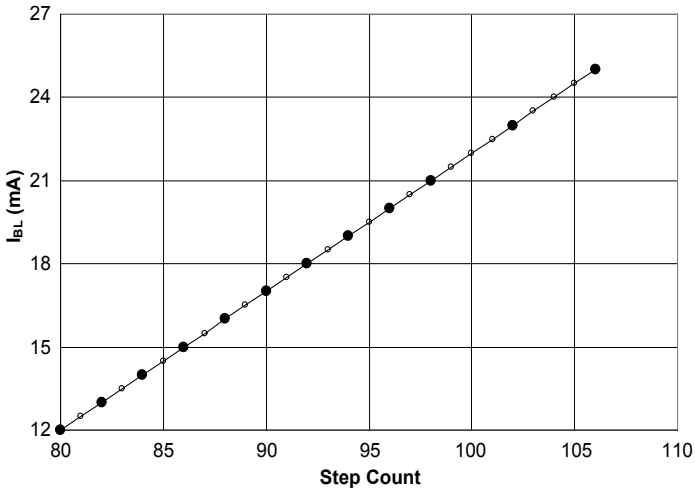


Figure 14 — Backlight Steps (12.0mA to 25.0mA)

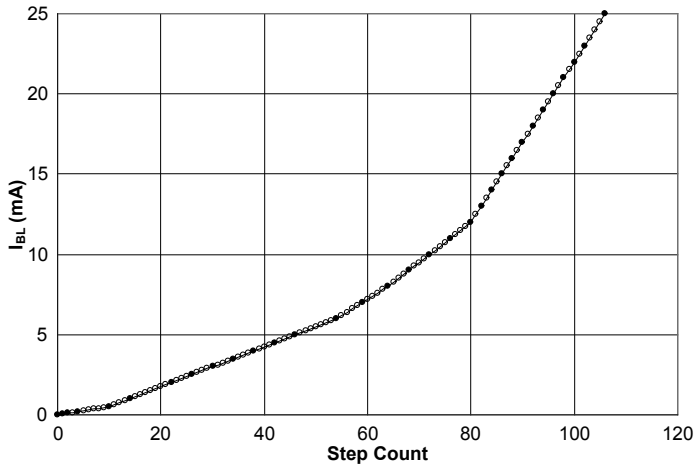


Figure 15 — Backlight Steps (0.0mA to 25.0mA)

Applications Information (continued)

General Purpose ADC

The ADI pin may also be used for general purpose ADC functions. For example, a linear temperature sensor may be added to the application circuit, and the SC667 may provide temperature data or an over-temperature warning flag. In this case, registers 13h, 14h, and 15h can be used to store the ADC reading and set thresholds that will trigger and interrupt output if the reading does not remain between them.

IRQ Output

A hardware interrupt request function is provided by the IRQ pin. This is an open-drain, active-low output that provides a flag indicating that the ALS input has exceeded a threshold level, or indicates that an overflow or underflow condition exists. Refer to Figure 16 for a description of this function.

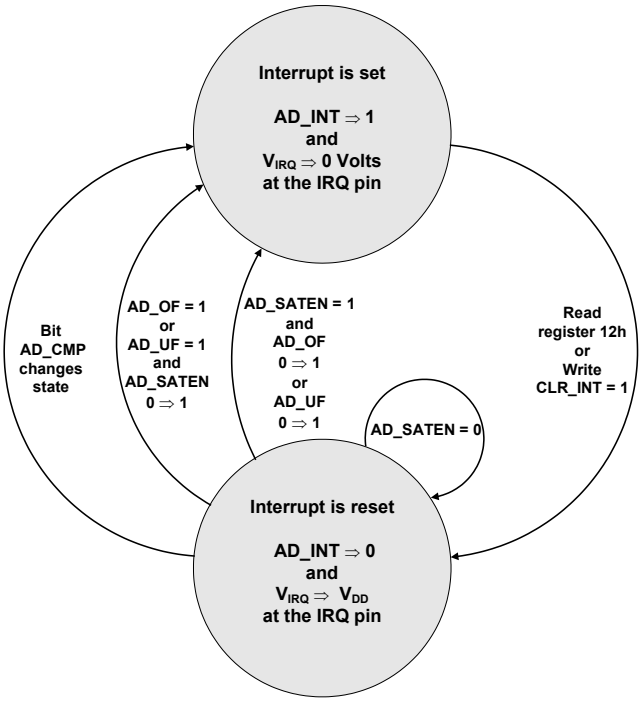


Figure 16 — IRQ Pin State Diagram

Programmable LDO Outputs

Four LDO (low dropout) regulators are included to supply power to peripheral circuits. Each LDO output voltage setting has ±3.5% accuracy over the line, load, and operating temperature ranges. Output current greater than specification is possible at somewhat reduced accuracy (refer to the typical characteristic section of this datasheet for load regulation examples). LDO1, LDO3, and LDO4 have identical specifications, with a programmable output ranging from 1.5V to 3.3V. LDO2 is specified to operate with programmable output ranging from 1.2V to 1.8V. All of the LDOs are low noise and can be used with noise sensitive circuits.

LDO4 is internally connected to the ADC (Analog to Digital Converter) to provide the reference voltage for the ADC. LDO4 must be enabled for the ADC to function. When the ALS function is used, LDO4 may also be used to provide power to the external ALS circuit.

Shutdown Mode

The device is disabled when the EN pin is held low for the shutdown time specified in the electrical characteristics section. All registers are reset to default conditions at shutdown. Typical current consumption in this mode is 0.1µA.

Sleep Mode

Sleep mode is activated when all backlights are off. This is a reduced current mode that helps minimize overall current consumption. In sleep mode, the I^2C interface continues to monitor its input for commands from the host processor. All registers retain their settings in sleep mode. Typical current consumption in this mode is 90µA.

Protection Features

The SC667 provides OT (Over-temperature) protection and LDO current limiting to safeguard the device from catastrophic failures.

Over-Temperature Protection

The OT protection circuit prevents the device from overheating and experiencing a catastrophic failure. When the junction temperature exceeds 165°C, the device goes into thermal shutdown with all outputs disabled until the junction temperature is reduced. All register information is retained during thermal shutdown. Hysteresis of 30°C is provided to ensure that the device cools sufficiently before re-enabling.

LDO Current Limit

The device limits current at each LDO output pin. The typical limit is 400mA, with a minimum limit rating of 200mA. The LDOs may be used for up to 200mA without tripping the current limit.

Applications Information (continued)

Thermal Management

A junction temperature calculation should be performed for each new application design to ensure the device will not exceed 125°C during normal operation. The first step is to determine how much power can be dissipated by the SC667 in the application. The following formula approximates the maximum dissipation. This formula can be used to sum the maximum internal power dissipation required of each LDO and each backlight sink.

$$P_D = \sum_{n=1}^{4} (V_{IN} - V_{LDOn}) \times I_{LDOn} + \sum_{m=1}^{7} V_{BLm} \times I_{BLm}$$

The resulting power dissipation can then be used in the calculation for maximum junction temperature.

$$T_J = T_A + \Theta_{JA} \times P_D$$

where,

T_A = Maximum ambient temperature rating in °C.
Θ_{JA}= Thermal resistance, from junction to ambient, equal to 35°C/W for a optimum circuit board layout.

Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 17 illustrates a two-layer PCB layout for the SC667 and supporting components. Following fundamental layout rules is critical for achieving the performance specified in the Electrical Characteristics table. The following guidelines are recommended when developing a PCB layout:

- Place all bypass and decoupling capacitors — C_{IN}, C_{LDO1}, C_{LDO2}, C_{LDO3}, C_{LDO4}, and C_{BYP} as close to the device as possible.
- Ensure that all connections to pins IN and OUT make use of wide traces so that the resistive drop on each connection is minimized.
- The thermal pad should be connected to the ground plane using multiple vias to ensure proper thermal connection for optimal heat transfer.
- C_{LDO1}, C_{LDO2}, C_{LDO3}, C_{LDO4}, and C_{BYP} should be grounded together. Connect these capacitors to the ground plane at one point near the SC667 as shown in Figure 17.
- Figure 18 shows the component copper layer. Make all ground connections to a solid ground plane as shown in Figure 19.
- All LDO output traces should be made as wide as possible to minimize resistive losses.

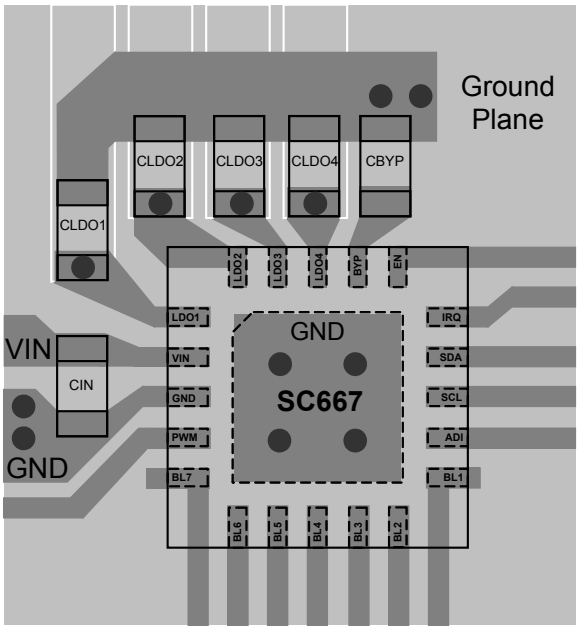


Figure 17 — Recommended PCB Layout

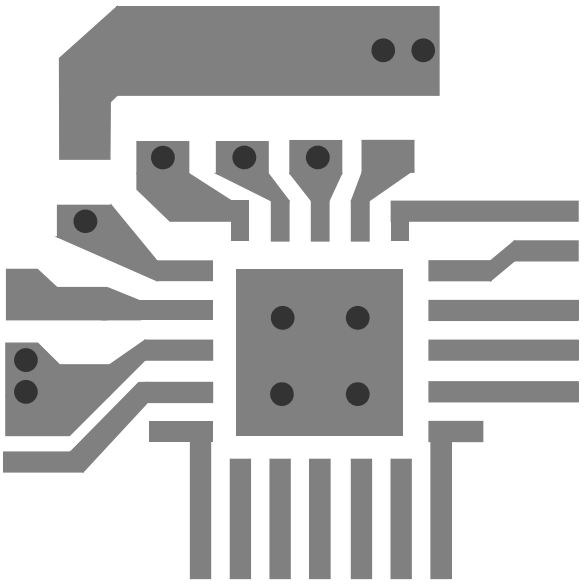


Figure 18 — Layer 1

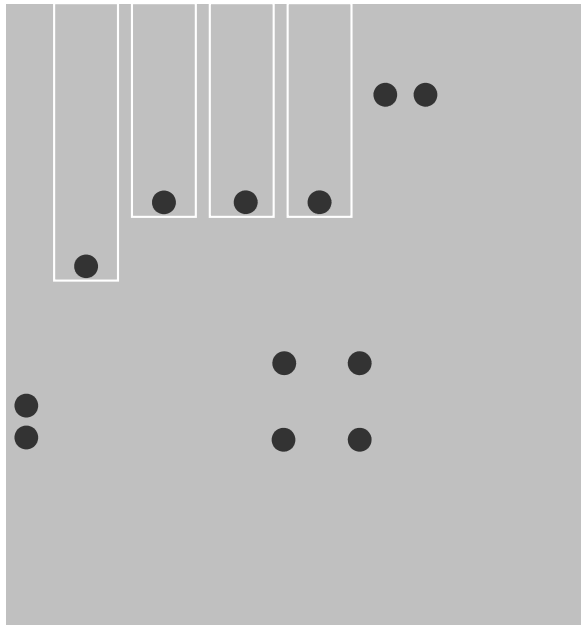


Figure 19 — Layer 2

Serial Interface

The I²C General Specification

The SC667 is a read-write slave-mode I²C device and complies with the Philips I²C standard Version 2.1, dated January 2000. The SC667 has twenty-three user-accessible internal 8-bit registers. The I²C interface has been designed for program flexibility, supporting direct format for write operation. Read operations are supported on both combined format and stop separated format. While there is no auto increment/decrement capability in the SC667 I²C logic, a tight software loop can be designed to randomly access the next register independent of which register you begin accessing. The start and stop commands frame the data-packet and the repeat start condition is allowed if necessary.

SC667 Limitations to the I²C Specifications

The SC667 only recognizes seven bit addressing. This means that ten bit addressing and CBUS communication are not compatible. The device can operate in either standard mode (100kbit/s) or fast mode (400kbit/s).

Slave Address Assignment

The seven bit slave address is 1110 000x. The eighth bit is the data direction bit. E0h is used for a write operation, and E1h is used for a read operation.

Supported Formats

The supported formats are described in the following subsections.

Direct Format — Write

The simplest format for an I²C write is direct format. After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The SC667 I²C then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the appropriate 8 bit data byte. Once again, the slave acknowledges and the master terminates the transfer with the stop condition [P].

Combined Format — Read

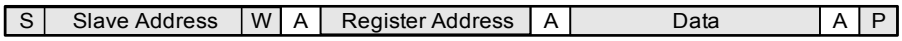
After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The SC667 I²C then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the repeated start condition [Sr]. Once again, the slave address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge and the 8 bit data from the previously addressed register; the master then sends a non-acknowledge (NACK). Finally, the master terminates the transfer with the stop condition [P].

Stop Separated Reads

Stop-separated reads can also be used. This format allows a master to set up the register address pointer for a read and return to that slave at a later time to read the data. In this format the slave address followed by a write command are sent after a start [S] condition. The SC667 then acknowledges it is being addressed, and the master responds with the 8-bit register address. The master sends a stop or restart condition and may then address another slave. After performing other tasks, the master can send a start or restart condition to the SC667 with a read command. The device acknowledges this request and returns the data from the register location that had previously been set up.

Serial Interface (continued)

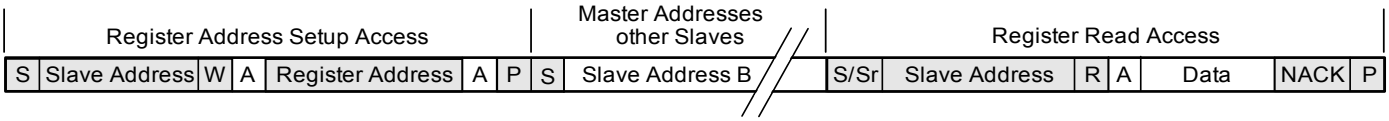
I²C Direct Format Write



S – Start Condition
W – Write = '0'
A – Acknowledge (sent by slave)
P – Stop condition

Slave Address – 7-bit
Register address – 8-bit
Data – 8-bit

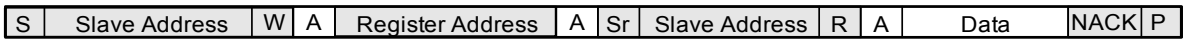
I²C Stop Separated Format Read



S – Start Condition
W – Write = '0'
R – Read = '1'
A – Acknowledge (sent by slave)
NAK – Non-Acknowledge (sent by master)
Sr – Repeated Start condition
P – Stop condition

Slave Address – 7-bit
Register address – 8-bit
Data – 8-bit

I²C Combined Format Read



S – Start Condition
W – Write = '0'
R – Read = '1'
A – Acknowledge (sent by slave)
NAK – Non-Acknowledge (sent by master)
Sr – Repeated Start condition
P – Stop condition

Slave Address – 7-bit
Register address – 8-bit
Data – 8-bit

Register Map(1)

Register Address	D7	D6	D5	D4	D3	D2	D1	D0	Description
00h	0(2)	0(2)	BL6EN	BL5EN	BL4EN	BL3EN	BL2EN	BL1EN	Backlight enable for BL1 — BL6
01h	0(2)	0(2)	DIS	EN	X(3) / BANK4EN	X(3) / BANK3EN	X(3) / BANK2EN	BL7EN / BANK1EN	Bank enable, plus backlight enable for BL7
02h	0(2)	0(2)	B1FEN	IB1_4	IB1_3	IB1_2	IB1_1	IB1_0	Fade enable and bank #1 backlight current (4)
03h	0(2)	0(2)	B2FEN	IB2_4	IB2_3	IB2_2	IB2_1	IB2_0	Fade enable and bank #2 backlight current (4)
04h	0(2)	0(2)	B3FEN	IB3_4	IB3_3	IB3_2	IB3_1	IB3_0	Fade enable and bank #3 backlight current (4)
05h	0(2)	0(2)	B4FEN	IB4_4	IB4_3	IB4_2	IB4_1	IB4_0	Fade enable and bank #4 backlight current (4)
06h	0(2)	0(2)	B1BEN	IBT1_4	IBT1_3	IBT1_2	IBT1_1	IBT1_0	Blink/breathe bank #1 target backlight settings
07h	0(2)	0(2)	B2BEN	IBT2_4	IBT2_3	IBT2_2	IBT2_1	IBT2_0	Blink/breathe bank #2 target backlight settings
08h	0(2)	0(2)	B3BEN	IBT3_4	IBT3_3	IBT3_2	IBT3_1	IBT3_0	Blink/breathe bank #3 target backlight settings
09h	0(2)	0(2)	B4BEN	IBT4_4	IBT4_3	IBT4_2	IBT4_1	IBT4_0	Blink/breathe bank #4 target backlight settings
0Ah	0(2)	0(2)	0(2)	0(2)	LDO1V3	LDO1V2	LDO1V1	LDO1V0	LDO 1 voltage settings
0Bh	0(2)	0(2)	0(2)	0(2)	0(2)	LDO2V2	LDO2V1	LDO2V0	LDO 2 voltage settings
0Ch	0(2)	0(2)	0(2)	0(2)	LDO3V3	LDO3V2	LDO3V1	LDO3V0	LDO 3 voltage settings
0Dh	0(2)	0(2)	0(2)	0(2)	LDO4V3	LDO4V2	LDO4V1	LDO4V0	LDO 4 voltage settings
0Eh	0(2)	0(2)	0(2)	GRP1	GRP0	BANK2	BANK1	BANK0	Lighting effects assignments, banks & groups
0Fh	0(2)	0(2)	ER2_2	ER2_1	ER2_0	ER1_2	ER1_1	ER1_0	Effect rates for group #1 and group #2
10h	0(2)	0(2)	TT1_2	TT1_1	TT1_0	ST1_2	ST1_1	ST1_0	Target time and start time for group #1
11h	0(2)	0(2)	TT2_2	TT2_1	TT2_0	ST2_2	ST2_1	ST2_0	Target time and start time for group #2
12h	AD_CMP	AD_INT	AD_SATEN	AD_OF	AD_UF	CLR_INT	AD_AUTO	AD_EN	ALS function
13h	AD_O7	AD_O6	AD_O5	AD_O4	AD_O3	AD_O2	AD_O1	AD_O0	ADC output AD_{OUT}
14h	AD_R7	AD_R6	AD_R5	AD_R4	AD_R3	AD_R2	AD_R1	AD_R0	ADC rising threshold AD_{RISE}
15h	AD_F7	AD_F6	AD_F5	AD_F4	AD_F3	AD_F2	AD_F1	AD_F0	ADC falling threshold AD_{FALL}
16h	0(2)	ADP_ACT	ADP_RATE	ADP_EN	OLE_EN2	OLE_EN1	OLE_EN0	PWM_BYP	Other lighting effects — auto-dim full or partial, auto-dim enable

Notes:

(1) Reset value for all registers = 00h

(2) 0 = always write a 0 to these bits

(3) X = no function — see register 01h description for more details.

(4) Registers 02h, 03h, 04h, and 05h serve as the "start" setting for blink/breathe lighting effects.

Register Map (continued)

Definition of Registers and Bits

Backlight Enable Register (00h)

The bits of register 00h are used to enable individual backlight current sinks BL1 through BL6.

BL6EN through BL1EN [D5:D0]

These bits are used to enable current sinks which control backlight current. When enabled, the current sinks will regulate the backlight current set by the corresponding backlight current register.

Bank Enable Register (01h)

The bits of register 01h are multi-function bits. The function of bits D3 through D0 depend upon the state of bits D5 and D4. Bits D3 through D0 may be used to turn individual banks on and off. An alternate function of bit D0 is used to enable and disable backlight BL7. Figure 20 shows how the function of bits D3 through D0 change according to the state of the DIS bit D5 and the EN bit D4.

DIS [Bit D5]

When writing to register 01h, if DIS bit D5 = 1 and EN bit D4 = 0, then bits D3 through D0 can each disable one of four banks. When disabling a bank, all associated BLxEN bits are automatically overwritten with a zero.

EN [Bit D4]

When writing to register 01h, if EN bit D4 = 1 and DIS bit D5 = 0, then bits D3 through D0 can each enable one of four banks. When enabling a bank, all associated BLxEN bits are automatically overwritten with a one.

BANK4EN through BANK1EN [Bits D3:D0]

The following bits — BANK4EN, BANK3EN, BANK2EN, and BANK1EN are used to enable or disable individual backlight banks dependent upon the state of the DIS and EN bits, D5 and D4. These bits provide no function when both DIS and EN are equal to one.

BL7EN [Alternate Function for Bit D0]

This bit is used to enable the current sink which controls backlight current for backlight BL7. When enabled, the current sink will regulate the backlight current set by the corresponding backlight current register.

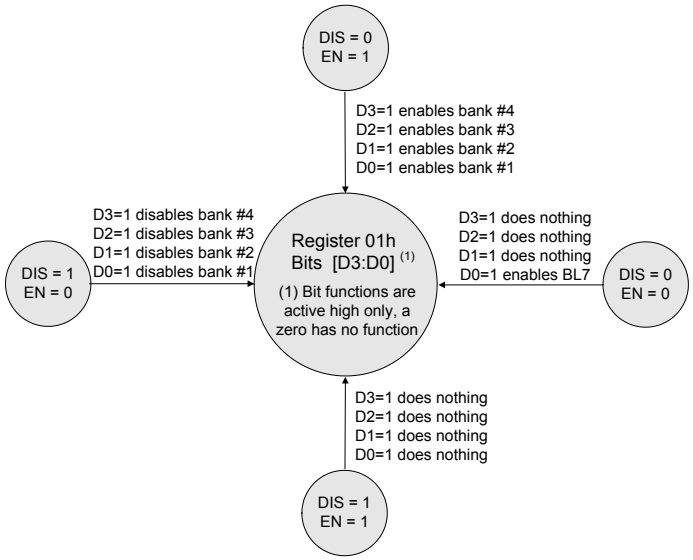


Figure 20 — Multi-function Bits of Register (01h)

Register Map (continued)

Bank #1 Backlight Register (02h)

This register is used to set the current for the backlight LEDs in bank #1 and to enable the lighting effect feature for bank #1. These backlights can be turned off using the backlight enable bits of registers 00h and 01h. Writing the 0mA value into this register will also turn off the backlights, but only if the blink and breathe effects are disabled.

B1FEN Bit D5

This bit works in conjunction with the B1BEN bit of register 06h to set a lighting effect for bank #1. Figure 21 shows the lighting effects which are enabled by the combination of B1FEN and B1BEN. When fade is enabled, fading will occur in bank #1 each time the bank #1 current is changed, enabled, or disabled. Blink and breathe functions run in a continuous loop when they are enabled.

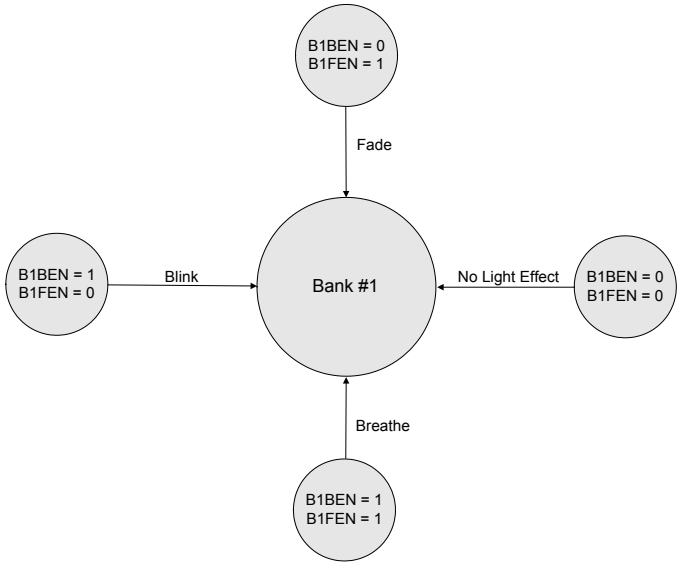


Figure 21 — Bank #1 Lighting Effect

IB1_4 through IB1_0 [Bits D4:D0]

These bits are used to set the current for the backlight LEDs in bank #1. All bank #1 enabled current sinks will sink the same current as shown in Table 2.

Table 2 — Bank #1 Backlight Current

IB1_4	IB1_3	IB1_2	IB1_1	IB1_0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	0.05
0	0	0	1	0	0.1
0	0	0	1	1	0.2
0	0	1	0	0	0.5
0	0	1	0	1	1
0	0	1	1	0	1.5
0	0	1	1	1	2
0	1	0	0	0	2.5
0	1	0	0	1	3
0	1	0	1	0	3.5
0	1	0	1	1	4
0	1	1	0	0	4.5
0	1	1	0	1	5
0	1	1	1	0	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	0	1	9
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

Register Map (continued)

Bank #2 Backlight Register (03h)

This register is used to set the current for the backlight LEDs in bank #2 and to enable the lighting effect feature for bank #2. These backlights can be turned off using the backlight enable bits of registers 00h and 01h. Writing the 0mA value into this register will also turn off the backlights, but only if the blink and breathe effects are disabled.

B2FEN Bit D5

This bit works in conjunction with the B1BEN bit of register 07h to set a lighting effect for bank #2. Figure 22 shows the lighting effects which are enabled by the combination of B2FEN and B2BEN. When fade is enabled, fading will occur in bank #2 each time the bank #2 current is changed, enabled, or disabled. Blink and breathe functions run in a continuous loop when they are enabled.

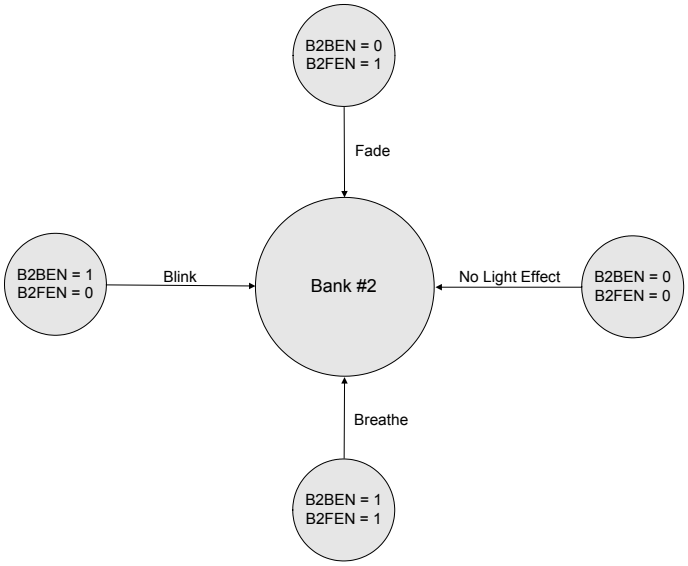


Figure 22 — Bank #2 Lighting Effect

IB2_4 through IB2_0 [Bits D4:D0]

These bits are used to set the current for the backlight LEDs in bank #2. All bank #2 enabled current sinks will sink the same current as shown in Table 3.

Table 3 — Bank #2 Backlight Current

IB2_4	IB2_3	IB2_2	IB2_1	IB2_0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	0.05
0	0	0	1	0	0.1
0	0	0	1	1	0.2
0	0	1	0	0	0.5
0	0	1	0	1	1
0	0	1	1	0	1.5
0	0	1	1	1	2
0	1	0	0	0	2.5
0	1	0	0	1	3
0	1	0	1	0	3.5
0	1	0	1	1	4
0	1	1	0	0	4.5
0	1	1	0	1	5
0	1	1	1	0	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	0	1	9
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

Register Map (continued)

Bank #3 Backlight Register (04h)

This register is used to set the current for the backlight LEDs in bank #3 and to enable the lighting effect feature for bank #3. These backlights can be turned off using the backlight enable bits of registers 00h and 01h. Writing the 0mA value into this register will also turn off the backlights, but only if the blink and breathe effects are disabled.

B3FEN Bit D5

This bit works in conjunction with the B1BEN bit of register 08h to set a lighting effect for bank #3. Figure 23 shows the lighting effects which are enabled by the combination of B3FEN and B3BEN. When fade is enabled, fading will occur in bank #3 each time the bank #3 current is changed, enabled, or disabled. Blink and breathe functions run in a continuous loop when they are enabled.

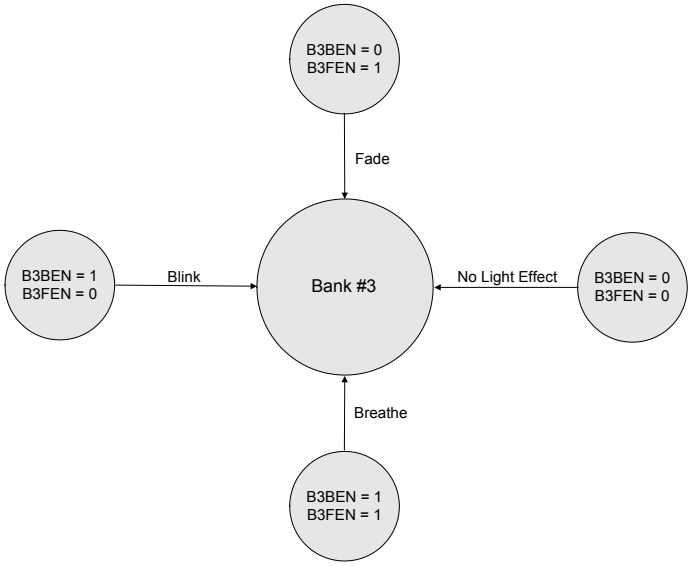


Figure 23 — Bank #3 Lighting Effect

IB3_4 through IB3_0 [Bits D4:D0]

These bits are used to set the current for the backlight LEDs in bank #3. All bank #3 enabled current sinks will sink the same current as shown in Table 4.

Table 4 — Bank #3 Backlight Current

IB3_4	IB3_3	IB3_2	IB3_1	IB3_0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	0.05
0	0	0	1	0	0.1
0	0	0	1	1	0.2
0	0	1	0	0	0.5
0	0	1	0	1	1
0	0	1	1	0	1.5
0	0	1	1	1	2
0	1	0	0	0	2.5
0	1	0	0	1	3
0	1	0	1	0	3.5
0	1	0	1	1	4
0	1	1	0	0	4.5
0	1	1	0	1	5
0	1	1	1	0	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	0	1	9
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

Register Map (continued)

Bank #4 Backlight Register (05h)

This register is used to set the current for the backlight LEDs in bank #4 and to enable the lighting effect feature for bank #4. These backlights can be turned off using the backlight enable bits of registers 00h and 01h. Writing the 0mA value into this register will also turn off the backlights, but only if the blink and breathe effects are disabled.

B4FEN Bit D5

This bit works in conjunction with the B4BEN bit of register 09h to set a lighting effect for bank #4. Figure 24 shows the lighting effects which are enabled by the combination of B4FEN and B4BEN. When fade is enabled, fading will occur in bank #4 each time the bank #4 current is changed, enabled, or disabled. Blink and breathe functions run in a continuous loop when they are enabled.

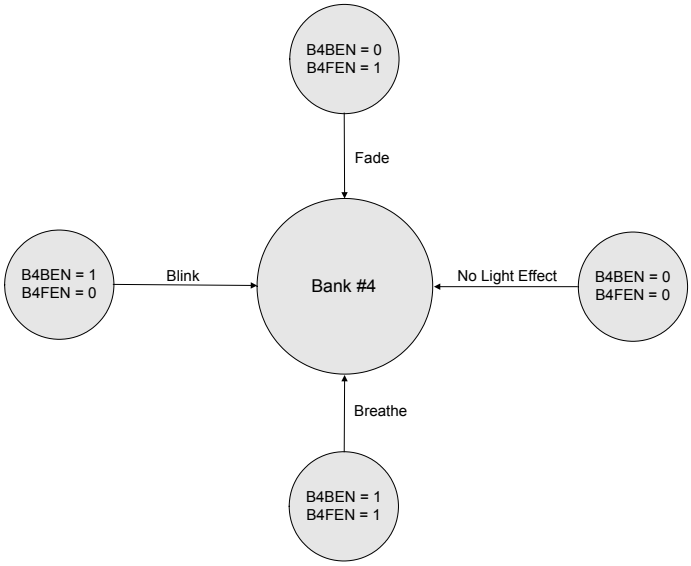


Figure 24 — Bank #4 Lighting Effect

IB4_4 through IB4_0 [Bits D4:D0]

These bits are used to set the current for the backlight LEDs in bank #4. All bank #4 enabled current sinks will sink the same current as shown in Table 5.

Table 5 — Bank #4 Backlight Current

IB4_4	IB4_3	IB4_2	IB4_1	IB4_0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	0.05
0	0	0	1	0	0.1
0	0	0	1	1	0.2
0	0	1	0	0	0.5
0	0	1	0	1	1
0	0	1	1	0	1.5
0	0	1	1	1	2
0	1	0	0	0	2.5
0	1	0	0	1	3
0	1	0	1	0	3.5
0	1	0	1	1	4
0	1	1	0	0	4.5
0	1	1	0	1	5
0	1	1	1	0	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	0	1	9
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

Register Map (continued)

Blink/Breathe Bank #1 Target Register (06h)

This register is used to enable the LED blink and breathe lighting effects for bank #1 and set the target backlight current.

B1BEN Bit [D5]

This bit works in conjunction with the B1FEN bit of register 02h to set a lighting effect for bank #1. Figure 25 shows the lighting effects which are enabled by the combination of B1FEN and B1BEN.

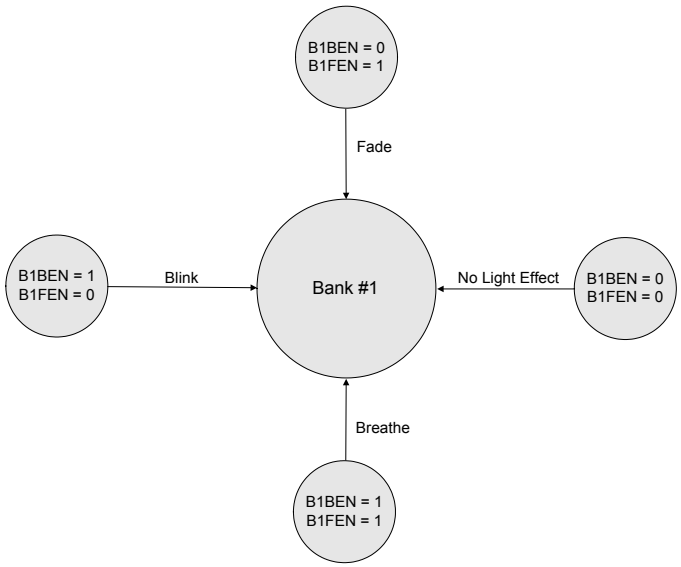


Figure 25 — Bank #1 Lighting Effect

IBT1_4 through IBT1_0 [D4:D0]

When lighting effects are enabled, these bits set the target backlight current for bank #1. Target values are shown in Table 6.

Table 6 — Bank #1 Target Backlight Current

IBT1_4	IBT1_3	IBT1_2	IBT1_1	IBT1_0	Bank #1 Target Current (mA)
0	0	0	0	0	0
0	0	0	0	1	0.05
0	0	0	1	0	0.1
0	0	0	1	1	0.2
0	0	1	0	0	0.5
0	0	1	0	1	1
0	0	1	1	0	1.5
0	0	1	1	1	2
0	1	0	0	0	2.5
0	1	0	0	1	3
0	1	0	1	0	3.5
0	1	0	1	1	4
0	1	1	0	0	4.5
0	1	1	0	1	5
0	1	1	1	0	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	0	1	9
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

Register Map (continued)

Blink/Breathe Bank #2 Target Register (07h)

This register is used to enable the LED blink and breathe lighting effects for bank #2 and set the target backlight current.

B2BEN Bit [D5]

This bit, in conjunction with the B2FEN bit, enables blink/breathe functions for bank #2 as shown in Figure 26.

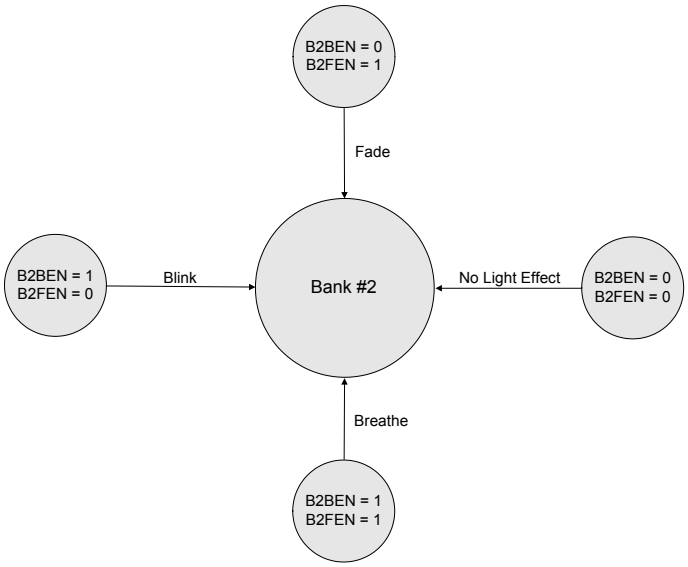


Figure 26 — Bank #2 Lighting Effect

IBT2_4 through IBT2_0 [D4:D0]

When lighting effects are enabled, these bits set the target backlight current for bank #2. Target values are shown in Table 7.

Table 7 — Bank #2 Target Backlight Current

IBT2_4	IBT2_3	IBT2_2	IBT2_1	IBT2_0	Bank #2 Target Current (mA)
0	0	0	0	0	0
0	0	0	0	1	0.05
0	0	0	1	0	0.1
0	0	0	1	1	0.2
0	0	1	0	0	0.5
0	0	1	0	1	1
0	0	1	1	0	1.5
0	0	1	1	1	2
0	1	0	0	0	2.5
0	1	0	0	1	3
0	1	0	1	0	3.5
0	1	0	1	1	4
0	1	1	0	0	4.5
0	1	1	0	1	5
0	1	1	1	0	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	0	1	9
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

Register Map (continued)

Blink/Breathe Bank #3 Target Register (08h)

This register is used to enable the LED blink and breathe lighting effects for bank #3 and set the target backlight current.

B3BEN Bit [D5]

This bit, in conjunction with the B3FEN bit, enables blink/breathe functions for bank #3 as shown in Figure 27.

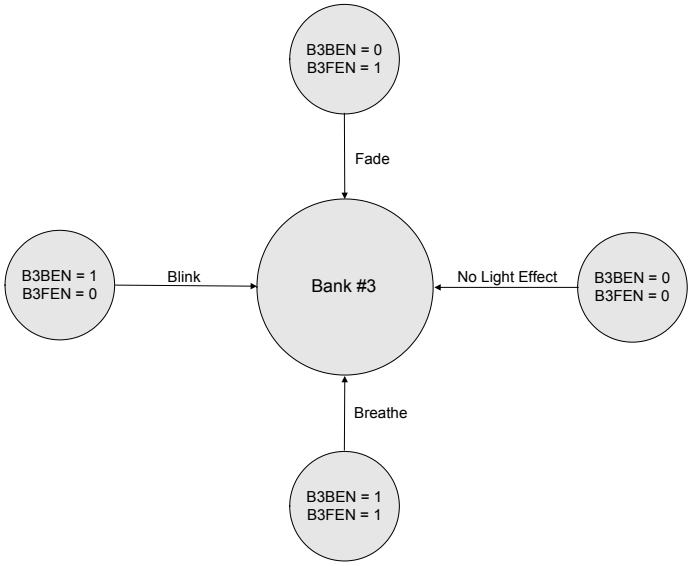


Figure 27 — Bank #3 Lighting Effect

IBT3_4 through IBT3_0 [D4:D0]

When lighting effects are enabled, these bits set the target backlight current for bank #3. Target values are shown in Table 8.

Table 8 — Bank #3 Target Backlight Current

IBT3_4	IBT3_3	IBT3_2	IBT3_1	IBT3_0	Bank #3 Target Current (mA)
0	0	0	0	0	0
0	0	0	0	1	0.05
0	0	0	1	0	0.1
0	0	0	1	1	0.2
0	0	1	0	0	0.5
0	0	1	0	1	1
0	0	1	1	0	1.5
0	0	1	1	1	2
0	1	0	0	0	2.5
0	1	0	0	1	3
0	1	0	1	0	3.5
0	1	0	1	1	4
0	1	1	0	0	4.5
0	1	1	0	1	5
0	1	1	1	0	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	0	1	9
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

Register Map (continued)

Blink/Breathe Bank #4 Target Register (09h)

This register is used to enable the LED blink and breathe lighting effects for bank #4 and set the target backlight current.

B4BEN Bit [D5]

This bit, in conjunction with the B4FEN bit, enables blink/breathe functions for bank #4 as shown in Figure 28.

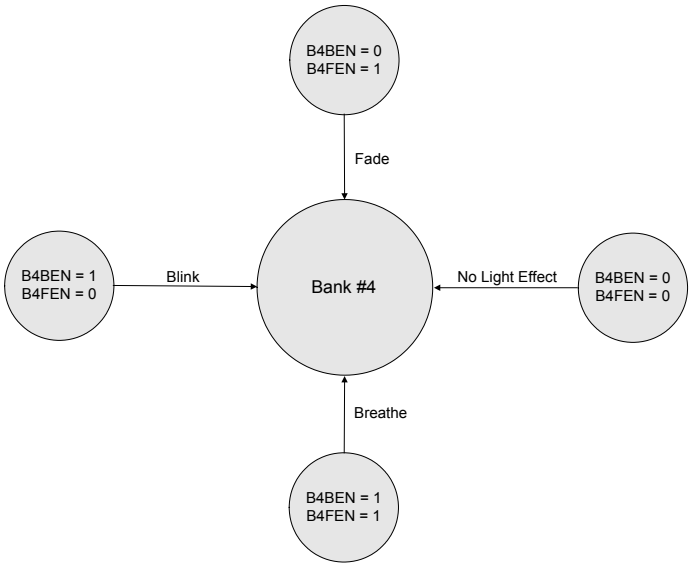


Figure 28 — Bank #4 Lighting Effect

IBT4_4 through IBT4_0 [D4:D0]

When lighting effects are enabled, these bits set the target backlight current for bank #4. Target values are shown in Table 9.

Table 9 — Bank #4 Target Backlight Current

IBT4_4	IBT4_3	IBT4_2	IBT4_1	IBT4_0	Bank #4 Target Current (mA)
0	0	0	0	0	0
0	0	0	0	1	0.05
0	0	0	1	0	0.1
0	0	0	1	1	0.2
0	0	1	0	0	0.5
0	0	1	0	1	1
0	0	1	1	0	1.5
0	0	1	1	1	2
0	1	0	0	0	2.5
0	1	0	0	1	3
0	1	0	1	0	3.5
0	1	0	1	1	4
0	1	1	0	0	4.5
0	1	1	0	1	5
0	1	1	1	0	6
0	1	1	1	1	7
1	0	0	0	0	8
1	0	0	0	1	9
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

Register Map (continued)

LDO1 Control Register (0Ah)

This register is used to enable LDO1 and set its output voltage level.

Bits [D5:D4]

These bits are unused and are always zeroes.

LDO1V3 through LDO1V0 [D3:D0]

These bits set the output voltage of LDO1 as shown in Table 10.

Table 10 — LDO1 Control Codes

LDO1V3	LDO1V2	LDO1V1	LDO1V0	V_{LDO1}
0	0	0	0	OFF
0	0	0	1	3.3V
0	0	1	0	3.2V
0	0	1	1	3.1V
0	1	0	0	3.0V
0	1	0	1	2.9V
0	1	1	0	2.8V
0	1	1	1	2.7V
1	0	0	0	2.6V
1	0	0	1	2.5V
1	0	1	0	2.4V
1	0	1	1	2.2V
1	1	0	0	1.8V
1	1	0	1	1.7V
1	1	1	0	1.6V
1	1	1	1	1.5V

LDO2 Control Register (0Bh)

This register is used to enable LDO2 and set its output voltage level.

Bits [D5:D3]

These bits are unused and are always zeroes.

LDO2V2 through LDO2V0 [D2:D0]

These bits are used to set the output voltage of LDO2 in accordance with Table 11.

Table 11 — LDO2 Control Codes

LDO2V2	LDO2V1	LDO2V0	V_{LDO2}
0	0	0	OFF
0	0	1	1.8V
0	1	0	1.7V
0	1	1	1.6V
1	0	0	1.5V
1	0	1	1.4V
1	1	0	1.3V
1	1	1	1.2V

Register Map (continued)

LDO3 Control Register (0Ch)

This register is used to enable LDO3 and set its output voltage level.

Bits [D5:D4]

These bits are unused and are always zeroes.

LDO3V3 through LDO3V0 [D3:D0]

These bits are used to set the output voltage of LDO3 as shown in Table 12.

Table 12 — LDO3 Control Codes

LDO3V3	LDO3V2	LDO3V1	LDO3V0	V_{LDO3}
0	0	0	0	OFF
0	0	0	1	3.3V
0	0	1	0	3.2V
0	0	1	1	3.1V
0	1	0	0	3.0V
0	1	0	1	2.9V
0	1	1	0	2.8V
0	1	1	1	2.7V
1	0	0	0	2.6V
1	0	0	1	2.5V
1	0	1	0	2.4V
1	0	1	1	2.2v
1	1	0	0	1.8V
1	1	0	1	1.7V
1	1	1	0	1.6V
1	1	1	1	1.5V

LDO4 Control Register (0Dh)

This register is used to enable LDO4, set its output voltage level, and provide power for the internal ADC. The ADC will not function without first turning on LDO4.

The output of LDO4 is used internally to provide the full-scale reference voltage for the ADC. When the ADC is active, LDO4 also provides a convenient source of power for devices such as ambient light sensors and temperature sensors.

Bits [D5:D4]

These bits are unused and are always zeroes.

LDO4V3 through LDO4V0 [D3:D0]

These bits are used to set the output voltage of LDO4 as shown in Table 13.

Table 13 — LDO4 Control Codes

LDO4V3	LDO4V2	LDO4V1	LDO4V0	V_{LDO4}
0	0	0	0	OFF
0	0	0	1	3.3V
0	0	1	0	3.2V
0	0	1	1	3.1V
0	1	0	0	3.0V
0	1	0	1	2.9V
0	1	1	0	2.8V
0	1	1	1	2.7V
1	0	0	0	2.6V
1	0	0	1	2.5V
1	0	1	0	2.4V
1	0	1	1	2.2V
1	1	0	0	1.8V
1	1	0	1	1.7V
1	1	1	0	1.6V
1	1	1	1	1.5V

Register Map (continued)

Lighting Effects Assignment Register (0Eh)

This register is used to assign the backlight LEDs to four banks, bank #1, bank #2, bank #3, and bank #4. This register is also used to assign the banks to two groups, group #1 and group #2. Group #1 and group #2 are assigned independently to a lighting effect and an effect rate, as described in the next section, Effect Rate Options.

GRP1 and GRP0 [D4:D3]

These bits are used to assign banks into two groups of independent lighting effects and effect rates. The group assignments are shown in Table 14.

Table 14 — Lighting Effect Assignments

GRP1	GRP0	Bank(s) Assigned Group #1	Bank(s) Assigned to Group #2
0	0	#1	#2, #3, and #4
0	1	#1 and #2	#3 and #4
1	0	#1, #2, and #3	#4
1	1	#1,# 2, #3, and #4	no banks assigned

BANK2, BANK1, and BANK0 [D2:D0]

These bits provide bank assignments for all backlight LEDs. Backlight bank assignments are shown in Table 15. The table shows the backlight pins assigned to each of the four banks, as assigned by the data bits BANK2, BANK1, and BANK0.

Table 15 — Backlight Bank Assignments

BANK2	BANK1	BANK0	Bank #4	Bank #3	Bank #2	Bank #1
0	0	0	-	-	-	BL1 - BL7
0	0	1	-	-	BL1	BL2 - BL7
0	1	0	-	-	BL1 - BL2	BL3 - BL7
0	1	1	-	BL1	BL2	BL3 - BL7
1	0	0	-	-	BL1 - BL3	BL4 - BL7
1	0	1	BL1	BL2	BL3	BL4 - BL7
1	1	0	BL1	BL2	BL3 - BL4	BL5 - BL7
1	1	1	BL1	BL2	BL3 - BL5	BL6 - BL7

Effect Rate Options (0Fh)

This register is used to set the effects rate for the fade and breathe effects. Different effect rates may be applied to group #1 and group #2.

ER2_2, ER2_1, and ER2_0 [D5:D3]

Banks assigned to group #2 will step through settings at the rate shown in Table 16.

Table 16 — Effect Rates for Group #2

ER2_2	ER2_1	ER2_0	Breathe Rate (ms/step)	Fade Rate (ms/step)
0	0	0	snap to target	snap to target
0	0	1	4	1
0	1	0	8	2
0	1	1	16	4
1	0	0	24	6
1	0	1	32	8
1	1	0	48	12
1	1	1	64	16

ER1_2, ER1_1, and ER1_0 [D2:D0]

Banks assigned to group #1 will step through settings at the rate shown in table 17.

Table 17 — Effect Rates for Group #1

ER1_2	ER1_1	ER1_0	Breathe Rate (ms/step)	Fade Rate (ms/step)
0	0	0	snap to target	snap to target
0	0	1	4	1
0	1	0	8	2
0	1	1	16	4
1	0	0	24	6
1	0	1	32	8
1	1	0	48	12
1	1	1	64	16

Register Map (continued)

Group #1 Target and Start Times Register (10h)

This register is used to set the duration that the backlights will stay at the start value and at the target value. This feature provides additional customization of the breathe and blink lighting effects. Register 10h will only effect banks that are assigned to group #1.

TT1_2, TT1_1, and TT1_0 [D5:D3]

These bits set the duration that backlights will stay at the target value. These bits effect only banks assigned to group #1. Target times are given in Table 18.

Table 18 — Target Time (Group #1)

TT1_2	TT1_1	TT1_0	Target Time (ms)
0	0	0	32
0	0	1	64
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	3072
1	1	1	4096

ST1_2, ST1_1, and ST1_0 [D2:D0]

These bits set the duration of time that backlights will stay at the starting value. These bits effect only banks assigned to group #1. Start times are given in Table 19.

Table 19 — Start Time (Group #1)

ST1_2	ST1_1	ST1_0	Start Time (ms)
0	0	0	32
0	0	1	64
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	3072
1	1	1	4096

Group #2 Target and Start Times Register (11h)

This register is used to set the duration that the backlights will stay at the start value and at the target value. This feature provides additional customization of the breathe and blink lighting effects. Register 11h will only effect banks that are assigned to group #2.

TT2_2, TT2_1, and TT2_0 [D5:D3]

These bits set the duration that backlights will stay at the target value. These bits effect only banks assigned to group #2. Target times are given in Table 20.

Table 20 — Target Time (Group #2)

TT2_2	TT2_1	TT2_0	Target Time (ms)
0	0	0	32
0	0	1	64
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	3072
1	1	1	4096

ST2_2, ST2_1, and ST2_0 [D2:D0]

These bits set the duration that backlights will stay at the starting value. These bits effect only banks assigned to group #2. Start times are given in Table 21.

Table 21 — Start Time (Group #2)

ST2_2	ST2_1	ST2_0	Start Time (ms)
0	0	0	32
0	0	1	64
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	3072
1	1	1	4096

Register Map (continued)

ADC Function Register (12h)

This register is used to enable the functions of the ADC and store related status bits. The ADC converts the analog output voltage signal of an ALS (Ambient Light Sense) circuit and stores the digital conversion in the ADC output AD_{OUT} (register 13h). The data may be used to automatically adjust the brightness of bank #1 backlights in response to changes in ambient lighting conditions.

AD_CMP [D7]

This bit indicates the comparison of AD_{OUT} (register 13h) to both AD_{RISE} (register 14h) and AD_{FALL} (register 15h). When AD_{OUT} exceeds AD_{RISE}, AD_CMP = 1. When AD_{OUT} falls below AD_{FALL}, AD_CMP = 0.

AD_INT [D6]

This bit is set when the AD_CMP bit [D7] changes state. If the AD_SATEN [D5] bit is set, AD_INT bit [D6] may also be used to indicate an overflow or underflow in AD_{OUT} (register 13h). This bit is cleared when ADC function register (12h) is read, or when writing INT_CLR bit [D2] equal to one.

AD_SATEN [D5]

This bit, when set, allows an underflow or overflow to generate an interrupt which sets the AD_INT bit [D6]. When AD_SATEN = 1, an overflow or underflow condition in register 13h will set the AD_INT bit.

AD_OF [D4]

This bit indicates an overflow condition in register 13h. This bit is set to one whenever AD_{OUT} > F8h.

AD_UF [D3]

This bit indicates an underflow condition in register 13h. This bit is set to one whenever AD_{OUT} < 08h.

INT_CLR [D2]

Writing a one to this bit automatically resets bit AD_INT to zero. INT_CLR resets itself and will always read as zero.

AD_AUTO [D1]

When the AD_AUTO bit is high, the contents of the AD_{OUT}, AD_{RISE}, and AD_{FALL} registers are compared and used to control the brightness of the bank #1 backlights. AD_{OUT} is compared with two threshold values contained in registers AD_{RISE} and AD_{FALL}. If AD_{OUT} becomes greater than AD_{RISE}, bank #1 will change to the bank #1 target backlight setting of register 06h. If AD_{OUT} becomes less than AD_{FALL}, bank #1 will change to the bank #1 backlight setting of register 02h.

When the AD_AUTO bit is low, the comparison of AD_{OUT} to AD_{RISE} and AD_{FALL} is disabled so that bank #1 does not react to changes in the value of AD_{OUT}, AD_{RISE}, or AD_{FALL}.

AD_EN [D0]

When the AD_EN bit is high, the ADC is activated and the results of each conversion are stored in AD_{OUT} (register 13h).

The functions of the AD_AUTO and AD_EN bits are shown in Table 22.

Table 22 — ALS Function Enable Bits

AD_AUTO	AD_EN	Comments
0	0	ADC is disabled. Bank #1 will not change brightness with ambient conditions.
0	1	ADC is enabled. ADC output is stored in the AD_{OUT} register. Bank #1 does not respond to the AD_{OUT} value.
1	0	ADC is disabled. Bank #1 current is set to the start or target current. AD_{OUT} is compared to AD_{RISE} and AD_{FALL} registers. A new value may be written to AD_{OUT} via the I^2C interface.
1	1	ADC is enabled. Bank #1 current is set to the start or target current. AD_{OUT} is compared to AD_{RISE} and AD_{FALL} registers.

Register Map (continued)

The ALS comparator functions are shown in Table 23.

Table 23 — ALS Comparator Function(1)

Conditions	AD_{OUT} Effect on Bank #1
$AD_{OUT} > AD_{RISE}$	Brightness changes to target value
$AD_{OUT} < AD_{FALL}$	Brightness changes to start value
$AD_{FALL} \le AD_{OUT} \le AD_{RISE}$	Brightness does not change
$AD_{FALL} \ge AD_{RISE}$	Hysteresis between the rising and falling thresholds is disabled and . . . AD_{FALL} → has no effect on brightness $AD_O > AD_{RISE}$ → brightness changes to target value $AD_O < AD_{RISE}$ → brightness changes to start value $AD_O = AD_{RISE}$ → brightness does not change

Note:
1) When AD_AUTO bit is high.

The state diagram of Figure 29 shows how the ADC is used to change the brightness of backlight bank #1. No automatic change in brightness occurs when AD_AUTO = 0.

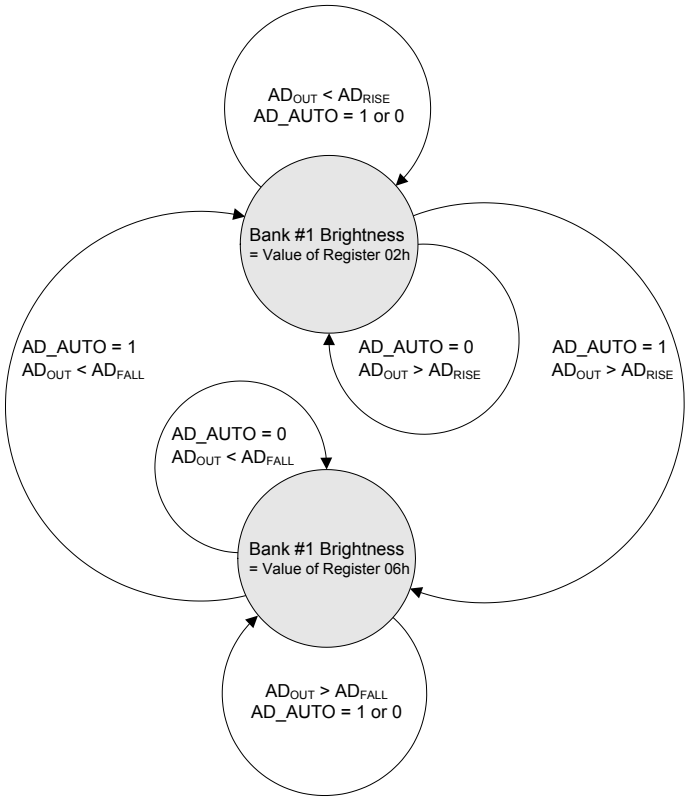


Figure 29 — ADC function at Bank #1 Brightness

ADC Output and Threshold Register (13h)

This register contains the value AD_{OUT} which is compared with AD_{RISE} and AD_{FALL}. The contents of AD_{OUT} may originate automatically from the ADC, when the AD_EN bit is a logic one. Alternatively, AD_{OUT} may be written to the register via the I^2C interface when the AD_EN bit is a logic zero.

When AD_EN = 1, the ADC receives its analog voltage input signal from the external photo-detector circuit connected to the ADI pin. V_{ADI} is then converted into digital and stored as the 8 bit word AD_{OUT}. The reference voltage for the ADC is provided internally by the output of LDO4 (V_{LDO4}). When the voltage V_{ADI} is equal to V_{LDO4} , the ADC is at full-scale value FFh, and AD_{OUT} will equal FFh.

When using an external photo-detection circuit, the ADC requires the LDO output voltage V_{LDO4} to remain constant. V_{LDO4} can drop-out if the supply voltage becomes too low. V_{LDO4} should be set to a value sufficiently low to guard against drop-out.

To prevent drop-out, the maximum LDO4 output setting should be limited to: $V_{LDO4(MAX)} = V_{IN(MIN)} - [1.33 \times I_{LDO4(MAX)}]$, where $V_{IN(MIN)}$ is the minimum battery voltage and $I_{LDO4(MAX)}$ is the maximum load current of LDO4. LDO4 load current includes current to the external photo-detection circuit.

AD_O7 through AD_O0 [D7:D0]

These are the 8 bits of AD_{OUT}. AD_O7 [D7] is the Most Significant Bit (MSB), and AD_O0 [D0] is the Least Significant Bit (LSB). Binary weights of these bits are shown in Table 24.

Table 24 — AD_{OUT} Bits [D7:D0]

Name	Bit	Binary Weight
AD_O7	D7	1/2
AD_O6	D6	1/4
AD_O5	D5	1/8
AD_O4	D4	1/16
AD_O3	D3	1/32
AD_O2	D2	1/64
AD_O1	D1	1/128
AD_O0	D0	1/256

Register Map (continued)

To calculate the voltage at the ADC input, the weights of only the bits set to one are summed together and multiplied by the voltage provided by LDO4. The result is equal to the analog voltage applied to the ADI pin. For example, if the value of register 13h reads AD_{OUT} = 01111111, and V_{LDO4} = 2.8V, the ADC input is at:

$2.8 \times (4^{-1} + 8^{-1} + 16^{-1} + 32^{-1} + 64^{-1} + 128^{-1} + 256^{-1}) = 1.38V$.

ADC Rising Threshold (14h)

This register contains the value AD_{RISE}. When AD_{OUT} rises above AD_{RISE} and AD_AUTO = 1, backlight bank #1 changes to the target value in the bank #1 target register (06h).

AD_R7 through AD_R0 [D7:D0]

These are the 8 bits of AD_{RISE}. AD_R7 is the MSB, and AD_R0 is the LSB.

ADC Falling Threshold (15h)

This register contains the value AD_{FALL}. When AD_{OUT} falls below AD_{FALL} and AD_AUTO = 1, backlight bank #1 changes to the starting value in the bank #1 register (02h).

AD_F7 through AD_F0 [D7:D0]

These are the 8 bits of AD_{FALL}. AD_F7 is the MSB, and AD_F0 is the LSB.

ADP and OLE Functions (16h)

ADP (Automatic Drop-out Protection) and OLE (Other Lighting Effects) are controlled with this register. ADP applies to bank #1 only.

ADP ensures current matching in the LEDs by responding to a low battery voltage. ADP limits the maximum backlight current to a level which ensures that backlight LEDs maintain matched currents. The ADP feature also prevents the ripple on a low battery from inducing flicker in the LEDs. As the battery voltage gradually proceeds lower, ADP gradually dims the backlights. The normal backlight brightness is restored after the battery is recharged by writing a logic zero to the ADP_EN bit.

Bank #1 will try to resume the original backlight current setting whenever ADP_EN = 0. Also, if any bank #1 current sink is floating, the ADP_EN bit is cleared automatically. Any write operations to change the following bit combinations in register 01h will also cause bank #1 to resume the original setting:

- DIS = 1, EN = 0, BANK1EN = 1
- DIS = 0, EN = 1, BANK1EN = 1
- DIS = 1, EN = 1, BANK1EN = 1

ADP_ACT Bit D6

This bit is a flag. A logic one indicates that ADP has been activated. Once activated, the ADP is limiting the backlight current. This flag bit is reset when ADP_EN = 0, or when any bank#1 current sink is floating, or by writing any of the following bit combinations in register 01h:

- DIS = 1, EN = 0, BANK1EN = 1
- DIS = 0, EN = 1, BANK1EN = 1
- DIS = 1, EN = 1, BANK1EN = 1

ADP_RATE Bit D5

This bit sets the time that elapses before backlight current reduces after ADP activates. A logic one delays reduction of current for 4ms. A logic zero delays reduction of current for 256µs.

When a reduction in bank #1 backlight current becomes necessary, the first step change is delayed for 4ms (logic one) or 256µs (logic zero). If bank #1 continues to need a current reduction after the delay time has elapsed, the brightness setting is lowered by one step. If further reductions in current are needed, the second and all subsequent reductions occur at a faster rate equal to1/4 of the initial delay time. Further reductions in current will stop when the backlight accuracy and matching have normalized.

When 4ms is selected, the 1st delay = 4ms, and the 2nd and all subsequent delays = 1ms. When 256µs is selected, the 1st delay = 256µs, and the 2nd and all subsequent delays = 64µs.

Register Map (continued)

ADP_EN Bit D4

This bit enables the ADP function. ADP is enabled when this bit is a logic one. ADP is disabled when this bit is a logic zero.

OLE_EN2 through OLE_EN0 Bits [D3:D1]

These bits enable Other Lighting Effects (OLE), including the auto-dim full and auto-dim partial, as shown in Table 25. Auto-dim functions are described in detail in the Applications Information section.

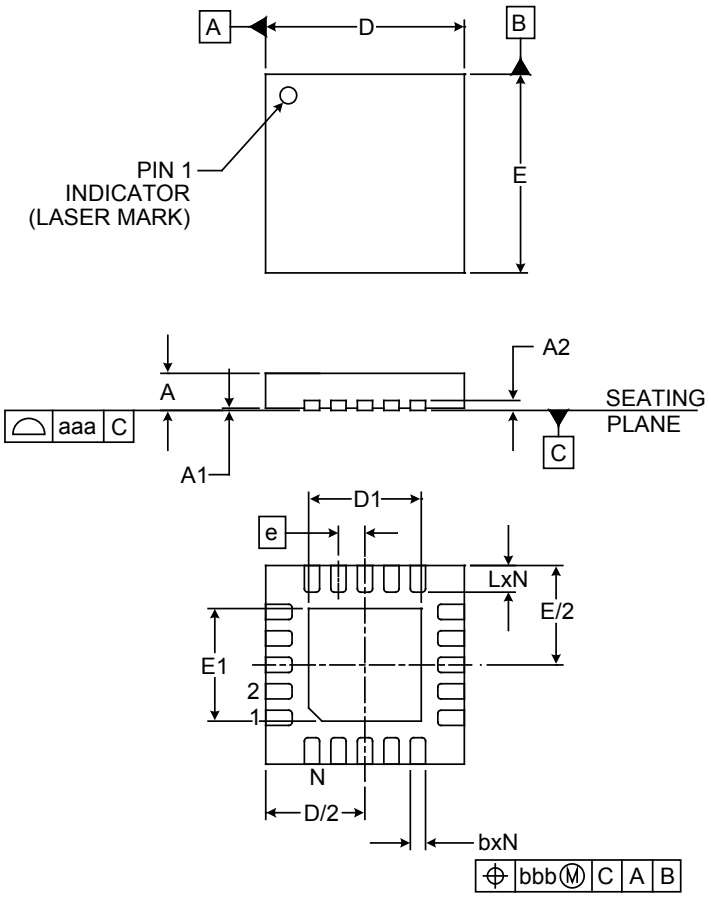
Table 25 — OLE Bits

OLE_EN2	OLE_EN1	OLE_EN0	Lighting Effect
0	0	0	Reserved (no effects)
0	0	1	Auto-dim full (group #1)
0	1	0	Auto-dim partial (group #1)
0	1	1	Reserved (no effects)
1	0	0	
1	0	1	
1	1	0	
1	1	1	

PWM_BYP Bit D0

When this bit is a logic zero, the PWM pin functions normally. When this bit is a logic one, the PWM pin is disabled, so that a high or low on the PWM pin has no effect.

Outline Drawing — MLPQ-UT-20 3x3

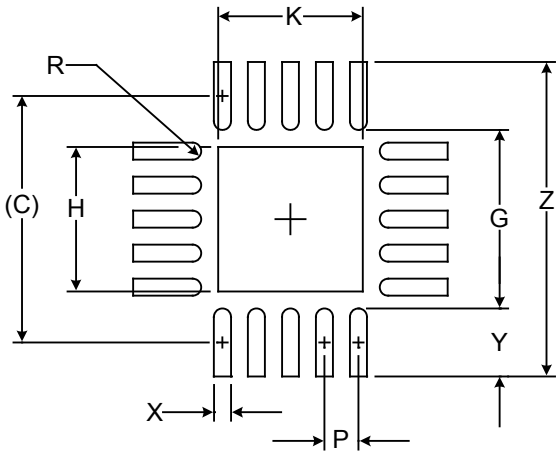


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.152)	
b	.006	.008	.010	0.15	0.20	0.25
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e		.016 BSC			0.40 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		20			20	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Land Pattern — MLPQ-UT-20 3x3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
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