1 to 4-Cell Li-Ion Battery Manager For Application Processors

BD99954MWV, BD99954GW

■ General Description

BD99954 is a Battery Management LSI for 1-4 cell Lithium-Ion secondary battery, and available in a 40pin 0.40 mm pitch 5.0 mm x 5.0 mm QFN package and small 41-ball 0.4mm pitch 2.6mm x 3.0mm Wafer-Level CSP package which is designed to meet high degree demands for space-constraint equipment such as Low profile Notebook PC, Tablets and other applications.

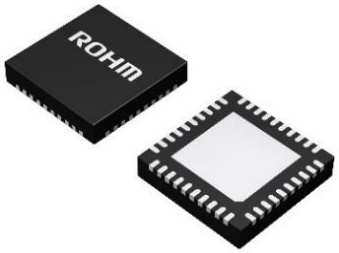
BD99954 provides a Dual-source Battery Charger, two port BC1.2 detection and a Battery Monitor with several alarm(INT#, PROCHOT#) outputs

■ Features

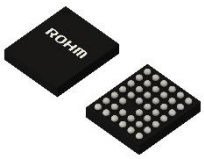
- **Dual-source Battery Charger**
  - High efficiency Step-Up/Down switching charger for 1-4 cell Li-Ion/Li-poly battery
  - Two separate input sources for USB-VBUS and DC adapter.
  - Two port BC1.2 detectors.
  - JEITA compliant charging profile
  - Programmable parameters for Preconditioning, Pre-charge current, and Fast-charge current
  - Programmable charging voltage
  - Programmable charge current
  - Programmable Switching Frequency: 600kHz to 1.2MHz
  - Support USB BCS 1.2, ACA, ID pin, OTG
  - USB-VBUS Over Voltage Protection
  - Over Voltage Battery Protection
  - Battery Short Circuit Detection
  - Power Path Management with charge pump gate driver
  - Flexibility power path control
  - Reverse Buck/Boost Option for USB/USB-PD
  - Bias voltage output for the external thermistor
  - PMON output
  - PROCHOT# output
  - Support Inhibit / Autonomous Charging
  - Battery Learn Function
  - Input Operating Range: 3.8V to 25V
- Voltage Measurement for Thermistor.
  - Bias voltage output for the external thermistor.
- SMBus Interface (Clock up friendly I2C) for Host communication
- Embedded OTPROM for initial settings

■ Packages

	Pitch	W	x D	x H
UQFN040V5050	0.4mm	5.0mm	x 5.0mm	x 1.0mm
UCSP55M3C 6 x 7balls	0.4mm	2.6mm	x 3.0mm	x 0.62mm



UQFN040V5050



UCSP55M3C

■ Applications

- Ultrabook
- Notebook PC
- Ultra-mobile PC
- Tablet PC

■ Structure

Silicon Monolithic Integrated Circuit

■ Line up matrix

Parts No.	Package
BD99954**MWV**	UQFN040V5050
BD99954**GW**	UCSP55M3C

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Notation

Category	Notation	Description
Unit	V	Volt (Unit of voltage)
	A	Ampere (Unit of current)
	Ω, Ohm	Ohm (Unit of resistance)
	F	Farad (Unit of capacitance)
	deg., degree	degree Celsius (Unit of Temperature)
	Hz	Hertz (Unit of frequency)
	s (lower case)	second (Unit of time)
	Min	minute (Unit of time)
	b, bit	bit (Unit of digital data)
	B, byte	1 byte = 8 bits
Unit prefix	M, mega-, mebi-	2^{20} = 1,048,576 (used with “bit” or “byte”)
	M, mega-, million-	10^{6} = 1,000,000 (used with “Ω” or “Hz”)
	K, kilo-, kibi-	2^{10} = 1,024 (used with “bit” or “byte”)
	k, kilo-	10^{3} = 1,000 (used with “Ω” or “Hz”)
	m, milli-	10^{-3}
	μ, micro-	10^{-6}
	n, nano-	10^{-9}
	p, pico-	10^{-12}
Numeric value	xxh, xxH	Hexadecimal number. “x”: any alphanumeric of 0 to 9 or A to F.
	Xxb	Binary number; “b” may be omitted. “x”: a number, 0 or 1 “_” is used as a nibble (4-bit) delimiter. (e.g. “0011_0101b” = “35h”)
Address	#xxh	Address in a hexadecimal number. “x”: any alphanumeric of 0 to 9 or A to F.
Data	bit[n]	n-th single bit in the multi-bit data.
	bit[n:m]	Bit range from bit[n] to bit[m].
Signal level	“H”, High	High level (over V_{IH} or V_{OH}) of logic signal.
	“L”, Low	Low level (under V_{IL} or V_{OL}) of logic signal.
	“Z”, “Hi-Z”	High impedance state of 3-state signal.

Reference

Name	Reference Document	Release Date	Publisher
I2C-bus	“UM10204: I^2C-bus specification and user manual Rev. 4”	Feb. 13, 2012	NXP Semiconductors
SMBus	System Management Bus (SMBus) Specification 3.0	Dec. 20, 2014	SBS-IF
JEITA Profile	“A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook-type Personal Computers”	Apr. 10, 2007	JEITA
USB BC	“Battery Charging Specification Revision 1.2”	Dec. 7, 2010	USB.org
Smart Battery Charger	Smart Battery Charger Specification Revision 1.1	Dec. 11, 1998	SBS-IF
USB 2.0	Universal Serial Bus Specification Revision 2.0	Jul. 26, 2013	USB.org
USB 3.1	Universal Serial Bus Revision 3.1 Specification Rev. 1.0	Aug. 11, 2014	USB.org
USB PD	USB Power Delivery Specification Rev. 2.0 V1.0	Apr. 27, 2000	USB.org

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1. Introduction

BD99954 is a Battery Manager IC for 1-4Cell Lithium-Ion / Lithium-Ion polymer secondary battery pack used in portable equipment such as Tablets, Ultra books or others.

BD99954 includes a Battery Charger, two port BC1.2 detection, a Battery Monitor for voltage, current, temperature and alarm(INT#, PROCHOT#) Controller. Figure 1-1 shows the Typical Application Circuit.

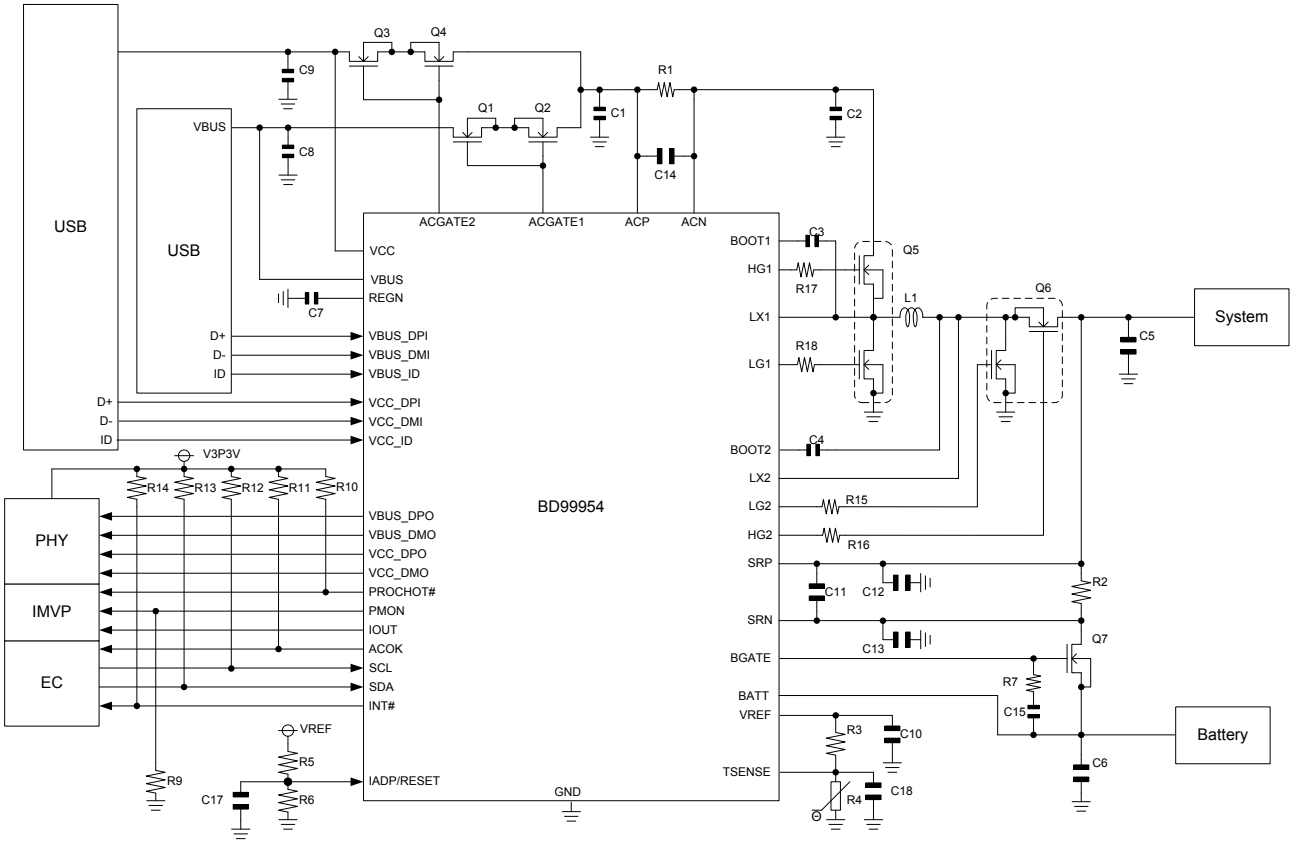


Figure 1-1 Block Diagram

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2. Signal Description

Table 2-1 Signal Description

Pin No.	Ball No. [CSP]	Pin Name	Function
1	B2	VBUS	USB Power Supply
2	A2	VCC	DC Power Supply
3	D3	ACOK	AC adapter voltage detection open drain output.
4	A3	INT#	Interrupt for I2C
5	B3	PROCHOT#	Active low open drain output of “processor hot” indicator. The charger IC monitors events like adapter current, battery discharge current. Once any event in PROCHOT# profile is triggered, a minimum 10ms pulse is asserted.
6	A4	ACN	Input current sense resistor negative input.
7	A5	ACP	Input current sense resistor positive input.
8	B4	ACGATE1	Charge pump output to drive adapter input n-channel MOSFET s. The ACGATE1 voltage is 5V above VBUS during AC adapter insertion.
9	B5	ACGATE2	Charge pump output to drive adapter input n-channel MOSFET s. The ACGATE2 voltage is 5V above VCC during AC adapter insertion.
10	A6	IADP/RESET	Default Input Current Limit Setting pin and System resistor reset pin.
11	B6	VBUS_DMI	VBUS side USB D- Input / Output
12	C4	VBUS_DPI	VBUS side USB D+ Input / Output
13	C5	VBUS_DMO	VBUS side USB D- Output / Input
14	C6	VBUS_DPO	VBUS side USB D+ Output / Input
15	D5	VBUS_ID	VBUS side USB ID pin input
16	D6	VCC_DMI	VCC side USB D- Input / Output
17	D4	VCC_DPI	VCC side USB D+ Input / Output
18	E6	VCC_DMO	VCC side USB D- Output / Input
19	F6	VCC_DPO	VCC side USB D+ Output / Input
20	G6	VCC_ID	VCC side USB ID pin input
21	E5	SCL	SMBus Clock Input
22	F5	SDA	SMBus Data Input / Output
23	G5	PMON	Buffered total system power current output. Place a resistor between PMON pin and GND.
24	F4	IOUT	Buffered adapter or charge current output selectable with SMBus command.
25	G4	VREF	1.5V LDO Output
26	E3	TSENSE	Battery temperature monitor pin. Active low battery present input signal. LOW indicates battery is present, and HIGH indicates the battery is absent and the charging stop.
27	G3	BATT	Battery Voltage Input
28	F3	BGATE	Gate Control Output
29	G2	SRN	Charge current sense resistor negative input.
30	G1	SRP	Charge current sense resistor positive input.
31	F2	GND	Ground
32	F1	HG2	DC/DC Boost side High Side Gate Driver
33	E2	LX2	DC/DC Boost side Inductor Connection
34	E1	BOOT2	DC/DC Boost side Driver Voltage Output
35	D2	LG2	DC/DC Boost side Low Side Gate Driver
36	D1	LG1	DC/DC Buck side Low Side Gate Driver
37	C1	BOOT1	DC/DC Buck side Driver Voltage Output
38	C2	LX1	DC/DC Buck side Inductor Connection
39	B1	HG1	DC/DC Buck side High Side Gate Driver
40	A1	REGN	LDO Output

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3. Pin Configuration

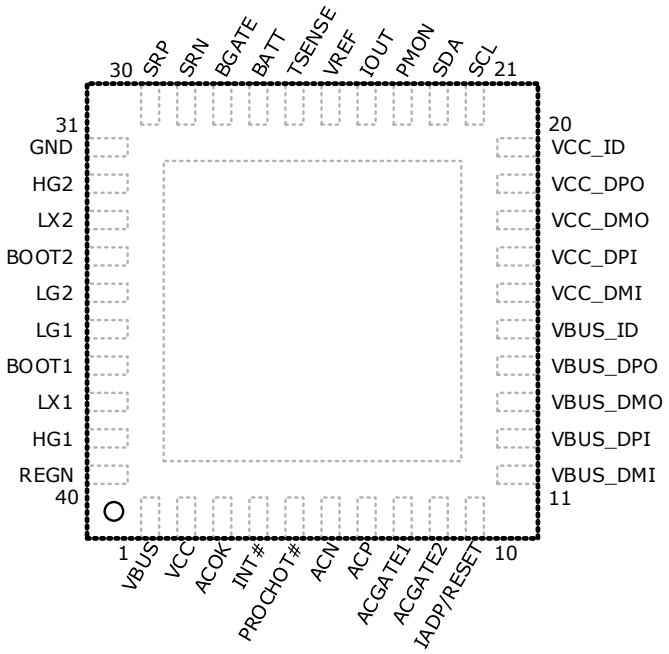


Figure 3-1 Pin Configuration in BD99954MWV (Top View)

	1	2	3	4	5	6
G	SRP	SRN	BATT	VREF	PMON	VCC_ID
F	HG2	GND	BGATE	IOUT	SDA	VCC_DPO
E	BOOT2	LX2	TSENSE	N/C	SCL	VCC_DMO
D	LG1	LG2	ACOK	VCC_DPI	VBUS_ID	VCC_DMI
C	BOOT1	LX1		VBUS_DPI	VBUS_DMO	VBUS_DPO
B	HG1	VBUS	PROCHOT#	ACGATE1	ACGATE2	VBUS_DMI
A	REGN	VCC	INT#	ACN	ACP	IADP/RESET

Figure 3-2 Pin Configuration in BD99954GW (Bottom View)

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4. Absolute Maximum Rating

		Value
Voltage range (with respect to GND)	VBUS, VCC, SRN, SRP, ACN, ACP, BATT	-0.3 to 28V
	LX1, LX2	-2 to 28V
	ACGATE1, ACGATE2, BGATE, BOOT1, BOOT2, HG1, HG2	-0.3 to 32V
	LX1-BOOT1,LX2-BOOT2	-0.3 to 6V
	ACP-ACN, SRP-SRN	-0.3 to 0.3 V
	VBUS_DPI, VBUS_DMI, VBUS_ID, VBUS_DPO, VBUS_DMO, VCC_DPI, VCC_DMI, VCC_ID, VCC_DPO, VCC_DMO, ACOK, REGN, INT#, PROCHOT#, IOUT, PMON, SCL, SDA, LG1, LG2	-0.3 to 7.0 V
	TSENSE, IADP/RESET, VREF	-0.3 to 2.1 V
Junction temperature		150℃
Storage temperature		-50 to 150℃

5. Thermal Resistance (Note 1)

Parameter		Symbol	Thermal Resistance (Typ)			Unit
			1s(Note 4)	2s2p(Note5)	4s5p(Note7)	
	UQFN040V5050					
Junction to Ambient		θ_{JA}	113.6	24.5	-	°C/W
Junction to Top Characterization Parameter(Note 2)		Ψ_{JT}	8	3	-	°C/W
	UCSP55M3C					
Power	Dissipation(Note3)	θ_{JA}	-	-	0.97	W

*(Note 1)*Based on JESD51-2A(Still-Air) only BD99954MWV
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Derate by 78.1mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board)
*(Note 4)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 5)*Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note6)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 6) This thermal via connects with the copper pattern of all layers..

*(Note 7)*Using a PCB board

Layer Number of Measurement Board	Material	Board Size
9 Layers	FR-4	63mm x 55mm x 1.6mmt

6. Recommended Operating Condition

	MIN	MAX	Unit
VBUS	3.8	25	V
VCC	3.8	25	V
BATT	0	19.2	V
IIN	-	16	A
ISYS	-	16	A
ICHARGE	-	16	A

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Operating Temperature range	-30	85	℃

7. Function Descriptions

7.1. Block Diagram

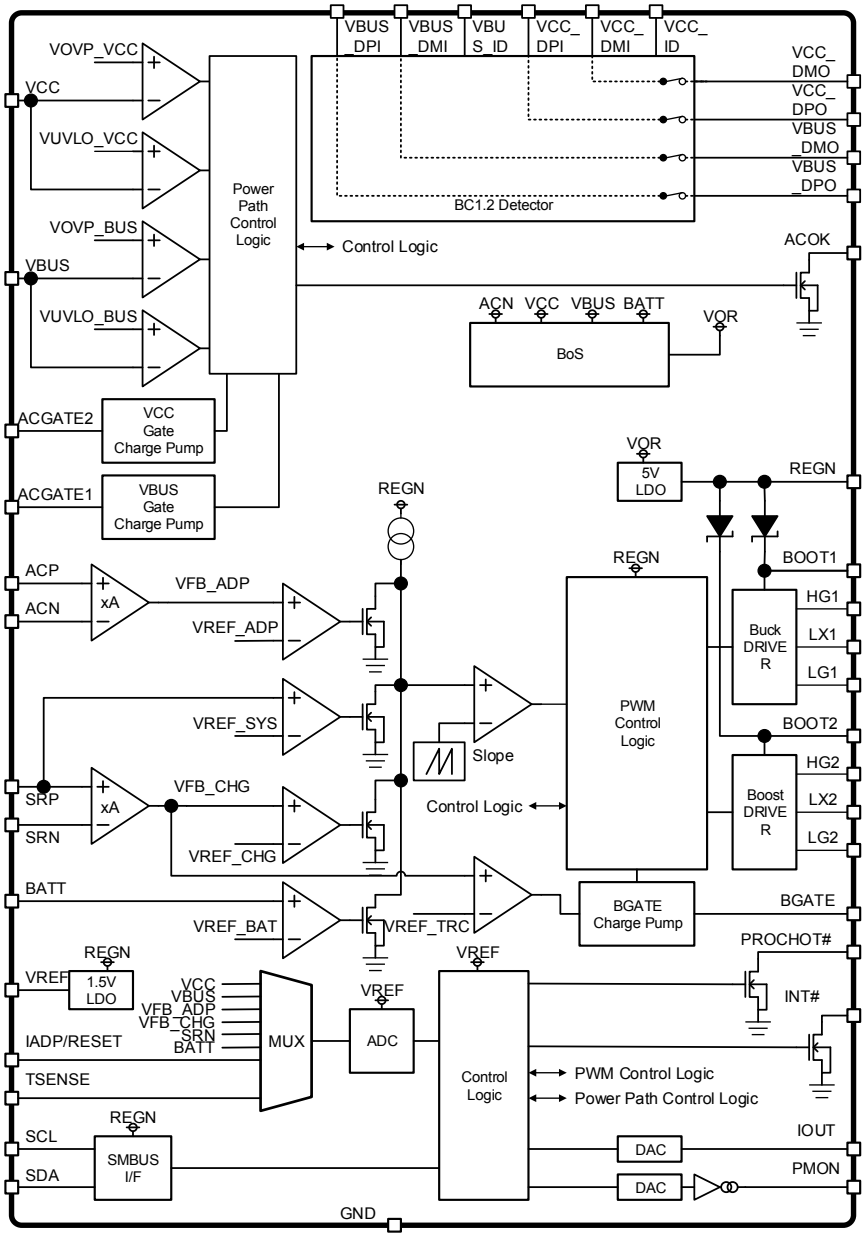


Figure 7-1 Block diagram

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7.2. External Characteristics for Battery Charger

Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Adapter Standby Current 1	I_{ADP1}	-	1.0	1.5	mA	Charge Pump ON
Adapter Operating Current 2	I_{ADP2}	-	4.0	8.0	mA	Charge Pump ON Not Switching
Battery Standby Current (VBUS=VCC=0.0V)	I_{BATT1}	-	50.0	100.0	μA	BGATE Charge Pump ON REG0x7Ch[2:0]=5h
Battery Standby Current (VBUS=VCC=0.0V)	I_{BATT2}	-	25.0	50.0	μA	BGATE Charge Pump OFF Deep Sleep mode REG0x7Ch[2:0]=6h SDA=SCL=0V
Battery Standby Current (VBUS=VCC=0.0V)	I_{BATT3}	-	125	200	μA	BGATE Charge Pump ON PROCHOT only VSYS [1msec/S] REG0x7Ch[2:0]=2h
Battery Standby Current (VBUS=VCC=0.0V)	I_{BATT4}	-	150	290	μA	BGATE Charge Pump ON PROCHOT only VSYS [250μsec/S] REG0x7Ch[2:0]=1h
Battery Current (VBUS=VCC=0.0V)	I_{BATT5}	-	700	900	μA	BGATE Charge Pump ON with PROCHOT Monitored System voltage and Battery current REG0x7Ch[2:0]=0h
SMBus Operation Frequency	FSMB	10	-	400	kHz	
REGN Output Voltage	V_{REGN}	5.0	5.2	5.4	V	
REGN External output current	V_{REGN_LD}	10	-	-	mA	
REGN UVLO Voltage	V_{REGN_UVLO}	2.375	2.5	2.625	V	Detecting REGN falling edge
REGN UVLO Hysteresis Range	V_{REGN_UVLO}	50	100	200	mV	Detecting REGN rising edge
LDO Output Voltage	V_{REF}	1.455	1.5	1.55	V	IVREF=1mA
VREF UVLO release Voltage	V_{REF_UVLO}	1.35	1.40	1.45	V	Detecting VREF rising edge
VREF UVLO Hysteresis Range	$V_{REF_UVLO_hys}$	25	50	100	mV	Detecting VREF falling edge
<PMON>						
Power Monitor Amplifier Gain (IPMON)/(VACP×IACP + VBAT×IBAT)	G_{PMON}	-	16	-	μA/W	REG0x25h[2:0]=6h 6.25W Setting
		-	8	-	μA/W	REG0x25h[2:0]=5h 12.5W Setting
		-	4	-	μA/W	REG0x25h[2:0]=4h 25W Setting
		-	2	-	μA/W	REG0x25h[2:0]=3h 50W Setting
		-	1	-	μA/W	REG0x25h[2:0]=2h 100W Setting
		-	0.5	-	μA/W	REG0x25h[2:0]=1h 200W Setting
		-	0.25	-	μA/W	REG0x25h[2:0]=0h 400W Setting
	I_{PMON}	-5	-	+5	%	IPMON=50uA
PMON Maximum Current	$I_{PMONMAX}$	-	-	200	μA	
<IOUT>						
IADP Voltage Accuracy	G_{IADP}	-	20	-	V/V	(VIADP)/(VACP- VACN)
	V_{IOUT1}	802.8	819.2	835.6	mV	(VACP- VACN)=40.96mV
	V_{IOUT2}	393.2	409.6	426	mV	(VACP- VACN)=20.48mV
	V_{IOUT3}	174.1	204.8	235.5	mV	(VACP- VACN)=10.24mV
	V_{IOUT4}	81.92	102.4	122.9	mV	(VACP- VACN)=5.12mV
	V_{IOUT5}	-	51.2	-	mV	(VACP- VACN)=2.56mV
	V_{IOUT6}	-	25.6	-	mV	(VACP- VACN)=1.28mV
IDCHG Voltage Accuracy	G_{IDCHG}	-	16	-	V/V	(VIDCHG)/(VSRN- VSRP)
	V_{IDCHG1}	622.6	655.4	688.2	mV	(VSRN- VSRP)=40.96mV
	V_{IDCHG2}	298.2	327.7	357.2	mV	(VSRN- VSRP)=20.48mV
	V_{IDCHG3}	122.9	163.8	204.8	mV	(VSRN- VSRP)=10.24mV
	V_{IDCHG4}	41	81.9	122.9	mV	(VSRN- VSRP)=5.12mV

Note: Resister address refer to extended commands

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7.3. DC Input & Over Voltage Protection (OVP)

7.3.1. Outline

- Dual-input for the battery charger source: USB VBUS and VCC
- 25V over voltage protection.
- One of two DC input selection (exclusive)
- Effective input is selected by the control registers, VCC as default.

7.3.2. Electrical Characteristics

Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
VCC Input Operating Range	V_{CCRNG}	3.8	-	25	V	
VCC UVLO Release Voltage	V_{CC_UVLO}	3.7	3.8	3.9	V	VCC rising
VCC UVLO Hysteresis Range	$V_{CC_UVLO_hys}$	80	130	180	mV	VCC falling
VCC OVP Detection Voltage	V_{CC_OVP}	25.0	25.5	26.0	V	VCC rising
VCC OVP Hysteresis Range	$V_{CC_OVP_hys}$	100	150	200	mV	VCC falling
USB Input Operating Range	V_{USBRNG}	3.8	-	25	V	
VBUS_UVLO Release Voltage	V_{BUS_UVLO}	3.7	3.8	3.9	V	VBUS rising
VBUS UVLO Hysteresis Range	$V_{BUS_UVLO_hys}$	80	130	180	mV	VBUS falling
VBUS OVP Detection Voltage	V_{BUS_OVP}	25.0	25.5	26	V	VBUS rising
VBUS OVP Hysteresis Range	$V_{BUS_OVP_hys}$	100	150	200	mV	VBUS falling
VACOK Output “L” Voltage	V_{OK_ON}	-	-	1.0	V	I(VACOK) =1mA
VACOK Leakage Current	I_{OKL}	-	-	1	μA	VACOK = 5V
VBUS Reverse Output turn-on Time	T_{VBUS_ON}	-	5	10	msec	
Voltage Output down-off Time	T_{VBUS_OFF}	-	1	5	μsec	

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7.4. USB Detection

7.4.1. Outline

- USB Charger port detection and USB ID
- Supports USB BC 1.2, USB ACA, USB ID pin, USB OTG, and PD plug detection.
- Integrated analog switch supports USB HS (480Mbps).

7.4.2. Electrical Characteristics

Table 7-1 Electrical Characteristics for USB Detection

(Ta=25°C, BATT=3.6V, VBUS=5.0V)

Item	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
<USB Charger Detection>						
VDP_SRC voltage (output voltage for D+)	VDP_SRC	0.5	0.6	0.7	V	Io=0 to 200uA
VDM_SRC voltage (output voltage for D-)	VDM_SRC	0.5	0.6	0.7	V	Io=0 to 200uA
RCD resistance (D+ pull up resistance)	RCD	75	100	125	kΩ	
USB port un-detection resistance (Host D+ pull down resistance)	RHDP	100	-	-	kΩ	
VDAT_REF voltage (D+/D- detection voltage)	VDAT_REF	0.3	0.35	0.4	V	HDPR/HDML voltage rising
VLGC voltage (D+/D- detection voltage)	VLGC	1.2	1.4	1.6	V	HDPR/HDML voltage rising
D+ sink current	IDP_SINK	50	85	150	μA	V(HDPR) = 0.6V
D- sink current	IDM_SINK	50	85	150	μA	V(HDML) = 0.6V
<USB Switch (DP, DM)>						
Switch on-state resistance	RON_USBSW	-	5	10	Ω	VIN=3.3V or 0V
Switch off-state leakage current	IIOFF_USB	-3	-	3	μA	VIN=3.3V or 0V VBUS=OPEN
Switch capacitance	CSW	-	6	-	pF	USBSW ON
USB Switch start-up time	TUPUSB	-	-	1	ms	USBSW OFF→ON

(Ta=25°C, VBAT=3.6V, VBUS=5.0V)

Item	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
<USB ID>						
Pull-down detection resistance	RIDopen	1000	-	-	kΩ	USB ID removal detection
	RID1	-	797	-	kΩ	
	RID2	-	557	-	kΩ	
	RID3	-	440	-	kΩ	
	RID4	-	390	-	kΩ	
	RID5	-	287	-	kΩ	
	RID6	-	200	-	kΩ	
	RID7	-	180	-	kΩ	
	RID8	-	124	-	kΩ	
	RID9	-	102	-	kΩ	
	RID10	-	68	-	kΩ	
	RID11	-	47	-	kΩ	
	RID12	-	36.5	-	kΩ	
	RID13	-	1	-	kΩ	
	RID14	-	0	50	Ω	GND level detection
COMPH detection voltage ratio	RatioH	85	90	95	%	Ratio = 100xV(ID)/VCCIN [%] ID port voltage rising

Note: The pull-down resistance is designed in 5 % accuracy to comply with the standard of MCPC (Mobile Computing Promotion Consortium), except the 1kΩ resistor for RID_GND. The RID_GND resistance complies with the MHL (Mobile High-definition Link) standard in 20 % accuracy.

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7.5. DC/DC Converter

7.5.1. - Outline

- Input Current Limit value setting: 96 mA to 16352 mA for VBUS and VCC
- Charger supply voltage anti-collapse control.
- Low power mode support
- Include thermal protection and shutdown

7.5.2. Electrical Characteristics

Table 7-2 Electrical Characteristics for DC/DC Converter
Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
<INPUT CURRENT>						
USB 500mA Current Accuracy	I_{USB500}	398	448	500	mA	REG0x07h/08h=01C0h
USB 900mA Current Accuracy	I_{USB900}	764	832	900	mA	REG0x07h/08h=0340h
BC1.2 1500mA Current Accuracy	$I_{USB1500}$	1380	1440	1500	mA	REG0x07h/08h=05A0h
USB-PD 3A Current Accuracy	$I_{USB3000}$	2824	2912	3000	mA	REG0x07h/08h=0B60h
USB-PD 5A Current Accuracy	$I_{USB5000}$	4792	4896	5000	mA	REG0x07h/08h=1320h
Input Current Setting Range	I_{ADPRNG}	96	-	16352	mA	REG0x07h or REG0x08h
Charge Current Setting LSB	I_{ADPLSB}	-	32	-	mA	
Input Current Accuracy (10mΩ current sense resistor)	I_{ADP1}	-2%	4096	+2%	mA	
	I_{ADP2}	-3%	2048	+3%	mA	
	I_{ADP3}	-5%	1024	+5%	mA	
	I_{ADP4}	-10%	512	+10%	mA	
IADP/RESET pin input Voltage range	$V_{ADPTRNG}$	0.1	-	1.4	V	
IADP/RESET pin Current setting Range	$I_{ADPTRNG}$	128	-	5120	mA	
IADP/RESET pin Current setting step	$I_{ADPSTEP}$	-	512	-	mA	
RESET Detection Voltage	Vreset_det	-	-	0.22	V	IADP/RESET voltage falling
RESET release Voltage	Vreset_rel	0.44	-	-	V	IADP/RESET voltage rising
RESET Detection duration time	T_{RESET}	100	-	-	µsec	
<MINIMUM SYSTEM VOLTAGE>						
Minimum System Voltage Setting Range	V_{MSVRNG}	2.560	-	19.2	V	VSYSREG_SET=2,560 ~ 19,200mV, 64mV steps.
Minimum System Voltage Setting LSB	V_{MSVLSB}	-	64	-	mV	
Minimum System Voltage accuracy	V_{MSV1}	-2.0%	3.072	+2.0%	V	REG0x11h=0C00h
	V_{MSV2}	-1.0%	6.144	+1.0%	V	REG0x11h=1800h
	V_{MSV3}	-2.0%	9.216	+2.0%	V	REG0x11h=2400h
	V_{MSV4}	-2.0%	12.288	+2.0%	V	REG0x11h=3000h
<Anti-Collapse Voltage>						
VBUS Anti-Collapse Threshold Voltage Range	V_{anti_VBUS}	3.84	-	25.0	V	REG0x0Dh
Anti-Collapse Threshold Voltage Accuracy	$V_{anti_VBUS_acc}$	-100	-	+100	mV	
VCC Anti-Collapse Threshold Voltage Range	V_{anti_VCC}	3.84	-	25.0	V	REG0x0Eh
Anti-Collapse Threshold Voltage Accuracy	$V_{anti_VCC_acc}$	-100	-	+100	mV	
<Switching Frequency>						
Switching Frequency 1	FOSC1	510	600	690	kHz	REG0x0Ch[3:2]=00b
Switching Frequency 2	FOSC2	770	860	950	kHz	REG0x0Ch[3:2]=01b
Switching Frequency 3	FOSC3	850	1000	1150	kHz	REG0x0Ch[3:2]=10b
Switching Frequency 4	FOSC4	1020	1200	1380	kHz	REG0x0Ch[3:2]=11b
<DRIVER>						
HRDV1 PMOS RON	R_{HDRV1P}	-	6.0	10.0	Ω	
HRDV1 NMOS RON	R_{HDRV1N}	-	0.7	1.3	Ω	
LRDV1 PMOS RON	R_{LDRV1P}	-	7.5	12.0	Ω	
LRDV1 NMOS RON	R_{LDRV1N}	-	0.9	1.4	Ω	
HRDV2 PMOS RON	R_{HDRV2P}	-	6.0	10.0	Ω	
HRDV2 NMOS RON	R_{HDRV2N}	-	0.7	1.3	Ω	
LRDV2 PMOS RON	R_{LDRV2P}	-	7.5	12.0	Ω	
LRDV2 NMOS RON	R_{LDRV2N}	-	0.9	1.4	Ω	

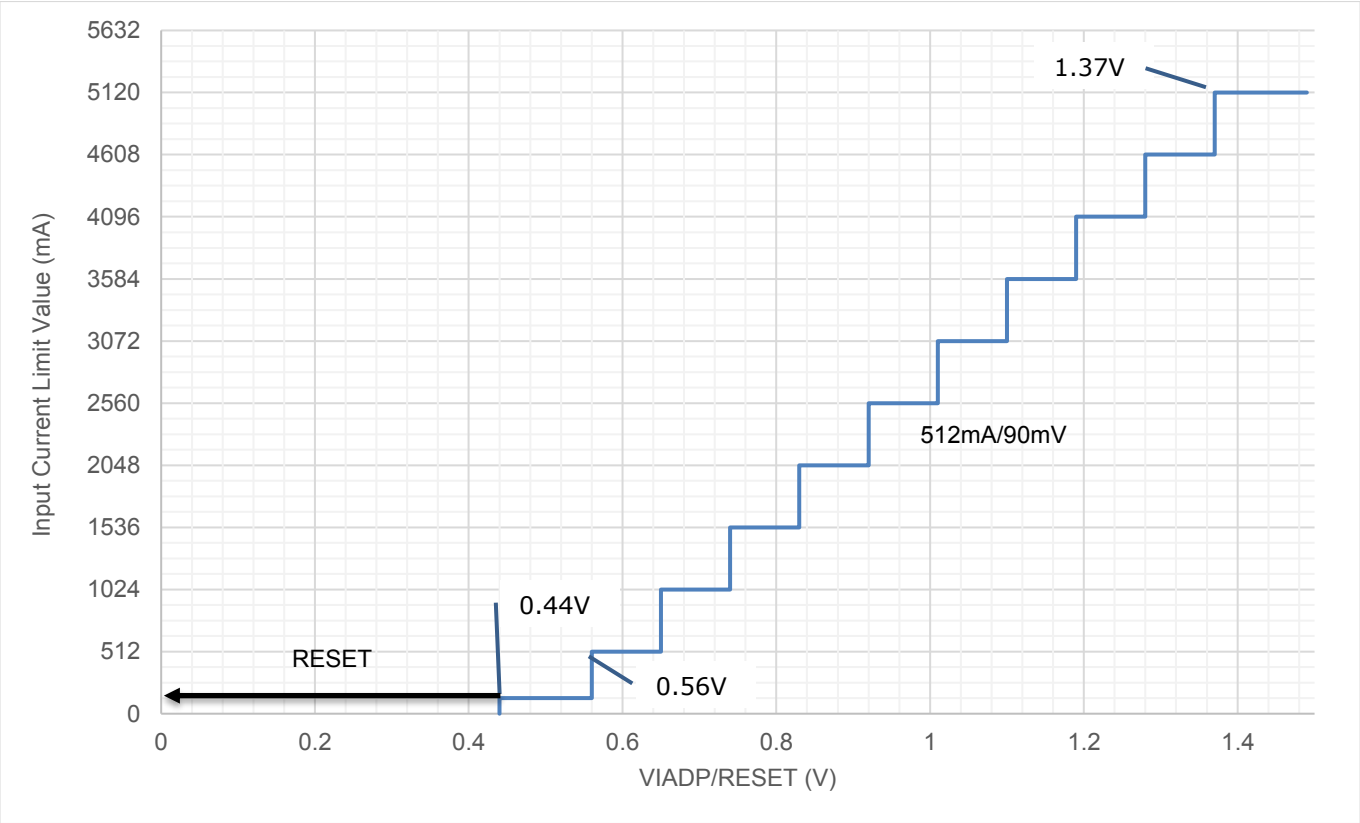
Note: Resister address refer to extended commands

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7.5.3. Detailed IADP input current limit settings

- Input Current limit is set by external IADP/RESET pin.
- This function is enabled by VM_CTRL_SET.EXTIADPEN bit =1.
- Once the charger reset is released when this function is enabled, the corresponding input current value which depends on the IADP/RESET voltage will be stored to the SEL_ILIM_VAL register. And this is used as the input current limit. It can be overwritten through SMBus.

Table 7-3 IADP pin Input Current Limit settings



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7.6. Charger

7.6.1. - Outline

- Supports battery insertion and removal detection.
- Controls the VSYS output voltage with a deeply discharged battery.
- JEITA compliant Battery Charging Profile with thermal control of the charging current and voltage settings by measuring the temperature from the external thermistor
- Supports battery supplement mode
- Automatic or manual control of the Watch Dog Timer (via software) while Pre–charging and Fast-charging

7.6.2. Electrical Characteristics

Table 7-4 Electrical Characteristics for Charger

Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

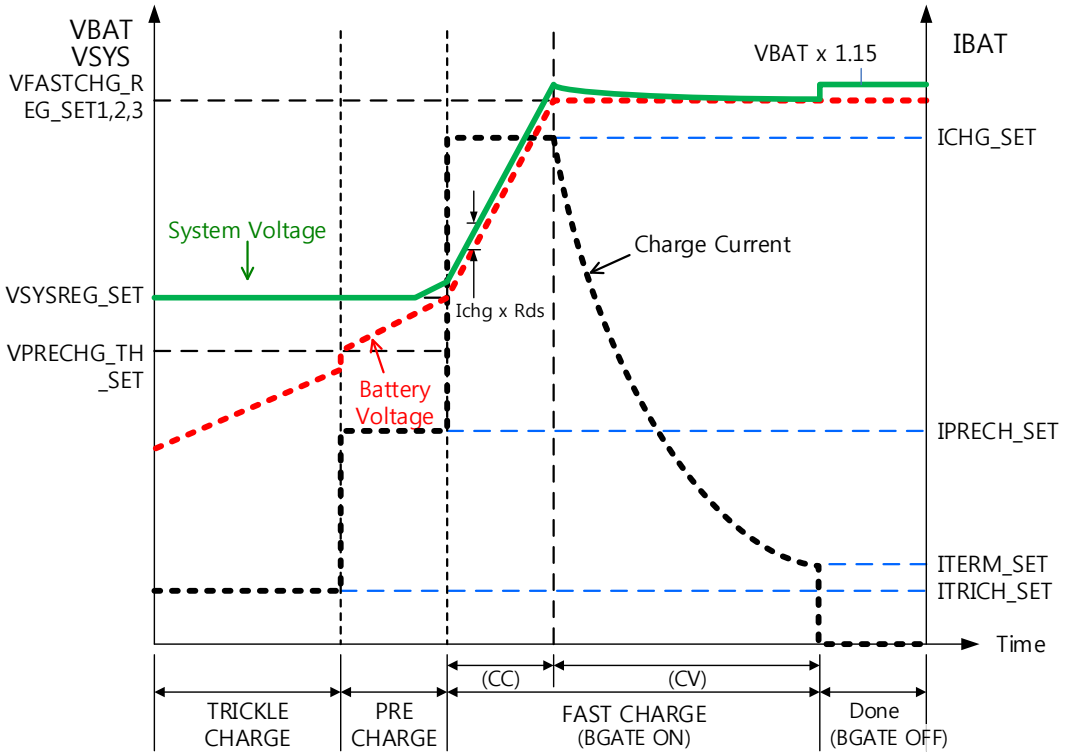
Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Battery Input Operating Range1	V_{BATRNG}	0.0	-	19.2	V	With Adapter Input
Battery Input Operating Range1	V_{BATRNG}	2.5	-	19.2	V	Without Adapter Input
<CHARGE VOLTAGE>						
Charge Voltage Setting Range	V_{CVRNG}	2.560	-	19.200	V	REG0x1A, REG0x1Bh or REG0x1Ch
Charge Voltage Setting LSB	V_{CVLSB}	-	16	-	mV	
Charge Voltage accuracy	V_{CV1S}	-0.5%	4.192	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=1060h
	V_{CV2S}	-0.5%	8.400	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=20D0h
	V_{CV3S}	-0.5%	12.592	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=3130h
	V_{CV4S}	-0.5%	16.800	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=41A0h
VBAT OVP Detection range	V_{OVPRNG}	2.56	-	19.2	V	REG0x1Dh
<CHARGE CURRENT>						
Charge Current Setting Range	I_{CHGRNG}	0	-	16384	mA	REG0x16h
Charge Current Setting LSB	I_{CHGLSB}	-	64	-	mA	
Charge Current accuracy (10mΩ current sense resistor, BATT > Minimum System Voltage)	I_{CHG1}	-2%	4096	+2%	mA	REG0x16h=1000h
	I_{CHG2}	-3%	2048	+3%	mA	REG0x16h=0800h
	I_{CHG3}	-5%	1024	+5%	mA	REG0x16h=0400h
	I_{CHG4}	-20%	256	+20%	mA	REG0x16h=0100h
	I_{CHG5}	-40%	128	+40%	mA	REG0x16h=0080h
Trickle Charge Current Setting Range	$I_{TRCCHGRNG}$	0	256	1024	mA	REG0x14h or REG0x15h
Trickle Charge Current Setting LSB	$I_{TRCCHGLSB}$	-	64	-	mA	
Maximum Trickle Charge Current (10mΩ current sense resistor, BATT < Minimum System Voltage)	I_{CHG6}	-	1024	-	mA	REG0x14h or REG0x15h
<Thermal Control>						
Battery Temperature Threshold HOT1	V_{TH_HOT1}	-	45	-	°C	OTP Programmable REG0x45h
Battery Temperature Threshold HOT2	V_{TH_HOT2}	-	50	-	°C	OTP Programmable REG0x44h
Battery Temperature Threshold HOT3	V_{TH_HOT3}	-	58	-	°C	OTP Programmable REG0x43h
Battery Temperature Threshold COLD1	V_{TH_COLD1}	-	10	-	°C	OTP Programmable REG0x42h
Battery Temperature Threshold COLD2	V_{TH_COLD2}	-	2	-	°C	OTP Programmable REG0x41h
Battery Temperature Measurement Acc	Tbat	-2	-	+2	°C	
Battery Open Detection Voltage	V_{TH_OPN}	-	V_{REF}*0.95	-	V	
<Battery Short Current Detection>						
Battery Short Current Detection	$I_{BATSHORT}$	0	-	25,000	mA	REG0x1Fh
Battery Short Current Duration time	$T_{BATSHORT}$	4	-	1020	msec	REG0x10h[15:8]
<Watchdog Timer>						
Pre Charging Time	T_{PRE}	13.0	14.5	16	min	
Fast Charging Time	T_{FAST}	196	218	240	min	
High Temperature Protection Time	T_{HTPRO}	108	120	132	min	Over 58°C
Charging Termination Delay Time	T_{TOPOFF}	13	15	17	sec	

Note: Resister address refer to extended commands

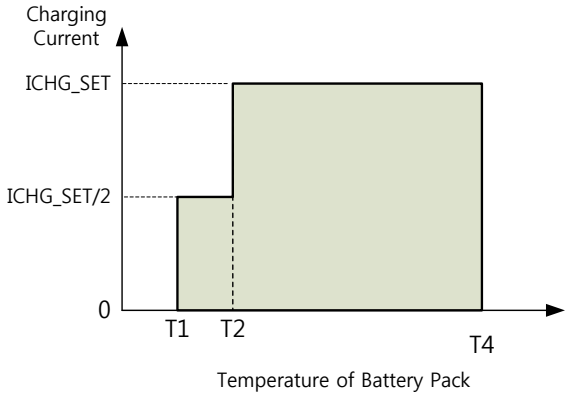
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7.6.3. Battery Charging Profile

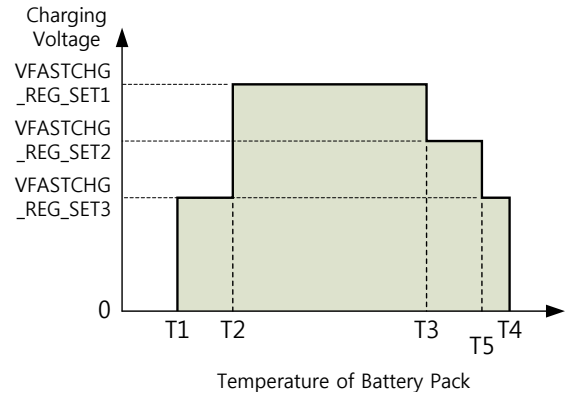
Figure 7-5 Battery Charging Profile



The charging current is controlled by the battery temperature measured from the external thermistor.
In the low-temperature condition, the charging current is reduced to a half of the setting value (ICHG_SET).



The charging voltage is also **reduced by the temperature** as **set by** the **control registers, VFASTCHG_REG_SET1/2/3**.



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7.7. Reverse DC/DC Converter

7.7.1. Outline

- Charger provides a voltage output (Reverse Buck/Boost) via VBUS or/and VCC when an USB OTG device is connected.

7.7.2. Electrical Characteristics

Table 7-6 Electrical Characteristics for Reverse Buck/Boost

Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
<OUTPUT CURRENT Limit>						
Output Current Limit Setting Range	$I_{RADPRNG}$	0	4096	8128	mA	REG0x09h
Output Current Limit Setting LSB	$I_{RADPLSB}$	-	32	-	mA	
Output Current Limit Accuracy (10mΩ current sense resistor)	I_{RADP1}	-2%	4096	+2%	mA	REG0x09h=1000h
	I_{RADP2}	-3%	2048	+3%	mA	REG0x09h=0800h
	I_{RADP3}	-5%	1024	+5%	mA	REG0x09h=0400h
	I_{RADP4}	-10%	512	+10%	mA	REG0x09h=0200h
<Output VOLTAGE>						
Output Voltage Setting 1	V_{ROUT1}	4.95	5.0	5.05	V	REG0x19h=1380h
Output Voltage Setting 2	V_{ROUT2}	5.15	5.2	5.25	V	REG0x19h=1440h
Output Voltage Setting 3	V_{ROUT3}	8.91	9.0	9.09	V	REG0x19h=2340h
Output Voltage Setting 4	V_{ROUT4}	11.88	12.0	12.12	V	REG0x19h=2F00h
Output Voltage Setting 5	V_{ROUT5}	19.8	20.0	20.2	V	REG0x19h=4E40h
Output Voltage Setting Range	$V_{ROUTRNG}$	4.032	-	22.016	V	REG0x19h
Output Voltage Setting LSB	$V_{ROUTLSB}$	-	64	-	mV	
VBUS Buck/Boost Output Short Circuit Protection.	$V_{R}scp$	-	VBUS_UVLO VCC_UVLO	-	V	
VBUS Buck/Boost OVP Voltage	$V_{R}ovp$	-	V_{ROUT} x 1.1	-	V	
VBUS Buck/Boost OVP Detection Hysteresis Range	$V_{R}ovp_hys$	-	V_{ROUT} x 1.05	-	mV	

Note: Resister address refer to extended commands

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7.8. 12-bit ADC

7.8.1. Outline

- 12-bit Successive Approximation Register A/D Converter
- Input Voltage range: 2.0 to 19.2V (BATT)
- Input Voltage range: 2.0 to 25V (VBUS, VCC, ACP, SRP)
- Input Voltage range: 0.1 to 1.4V (TSENSE)
- Input Voltage range: 0.1 to 1.4V (IADP/RESET)
- Current monitor range: 0.3 to 16.384A (IACP)
- Current monitor range: 0.3 to 25A (IBAT)

7.8.2. Electrical Characteristics

Table 7-7 Electrical Characteristics for 12-bit SAR-ADC

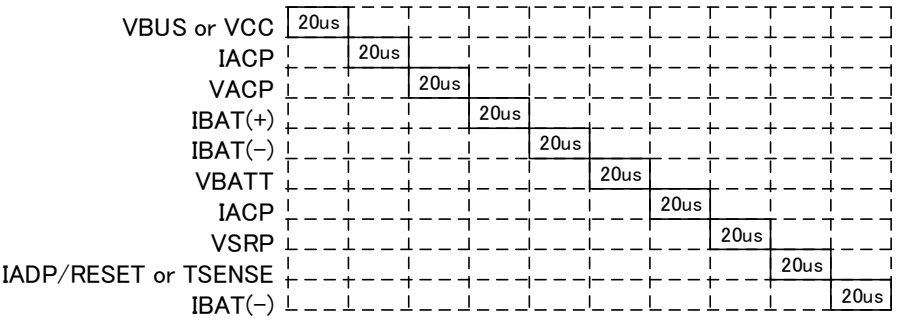
(Unless otherwise specified, Ta=25°C, VREF=1.5V)

Parameter	Symbol	Specification			Unit	Condition
		Min	Typ	Max		
<12-bit SAR ADC>						
Resolution	RES	-	-	12	bit	
Conversion Period	TCONV	-	20	-	µs	
Gain Error 1	Gerr1	−1.1	-	+1.1	%	BATT,VBUS,VCC,ACP, SRP=5V and 15V
Gain Error 2	Gerr2	−1.1	-	+1.1	%	TSENSE,IADP/RESET =0.5V and 1.0V
Gain Error 3	Gerr3	−1.1	-	+1.1	%	IACP,IBAT=1.5A and 8A
VOffset error	Voffset	-110		110	mV	
IOffset error	Ioffset	-110	-	110	mA	

7.8.3. Functions

SAR-ADC measures the 10 following factors by time sharing. These factors can be disabled by SMBus command.
The actual value and the 2-sample moving average value are read by SMBus command.

#	Factor	Conversion Period	Conversion Interval
1	VBUS or VCC	20us	VBUS 400us VCC 400us
2	IACP	20us	200us
3	VACP	20us	200us
4	IBAT(+)	20us	200us
5	IBAT(-)	20us	200us
6	VBATT	20us	200us
7	IACP	20us	200us
8	VSRP	20us	200us
9	IADP/RESET or TSENSE	20us	IADP/RESET 200us TSENSE 1s
10	IBAT(-)	20us	200us



The power calculation of PMON is carried out from IACP, VACP, IBAT, VBATT.

PACP = IACP * VACP
PBAT = IBAT * VBATT
PMON = PACP + PBATT

PMON power change can be observed when the value is stable longer than the “Conversion Interval”, 200us.

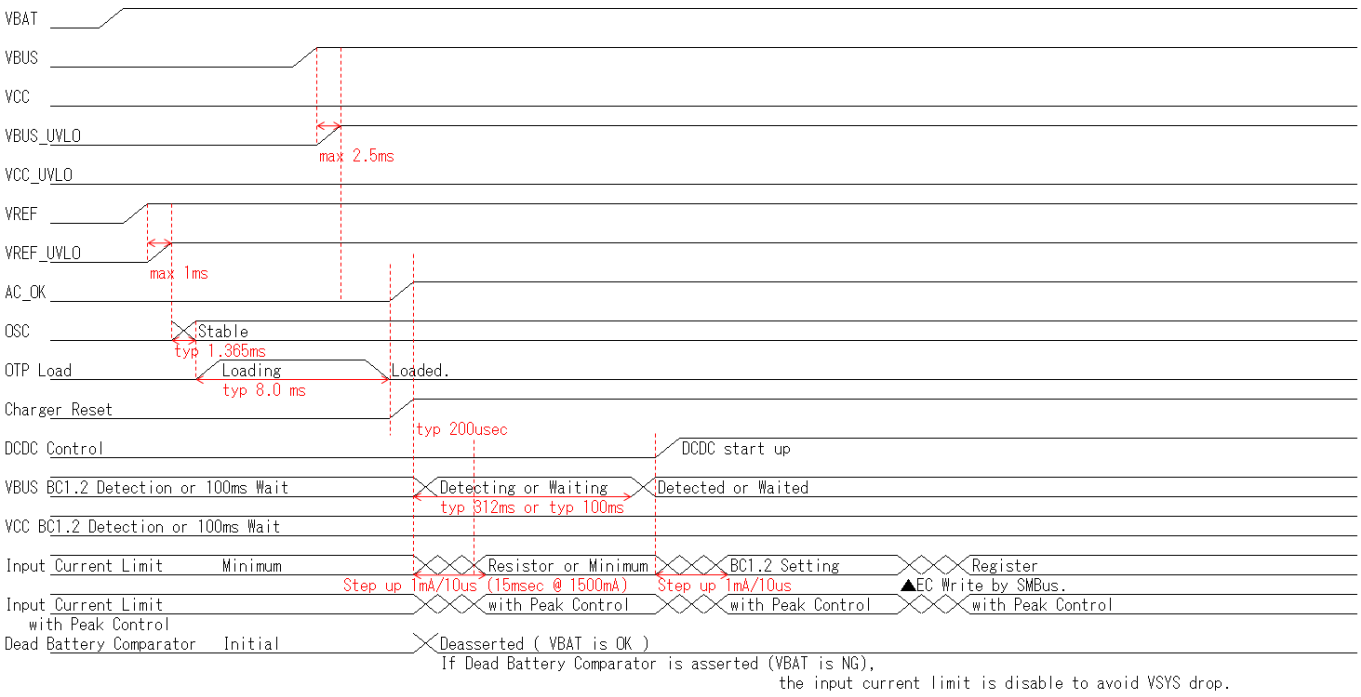
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7.9. Power On

Whenever BD99954 receives power from the adapter or battery, BD99954 wakes up and starts loading data from the OTP. After OTP loading is completed, BD99954 is in standby position.

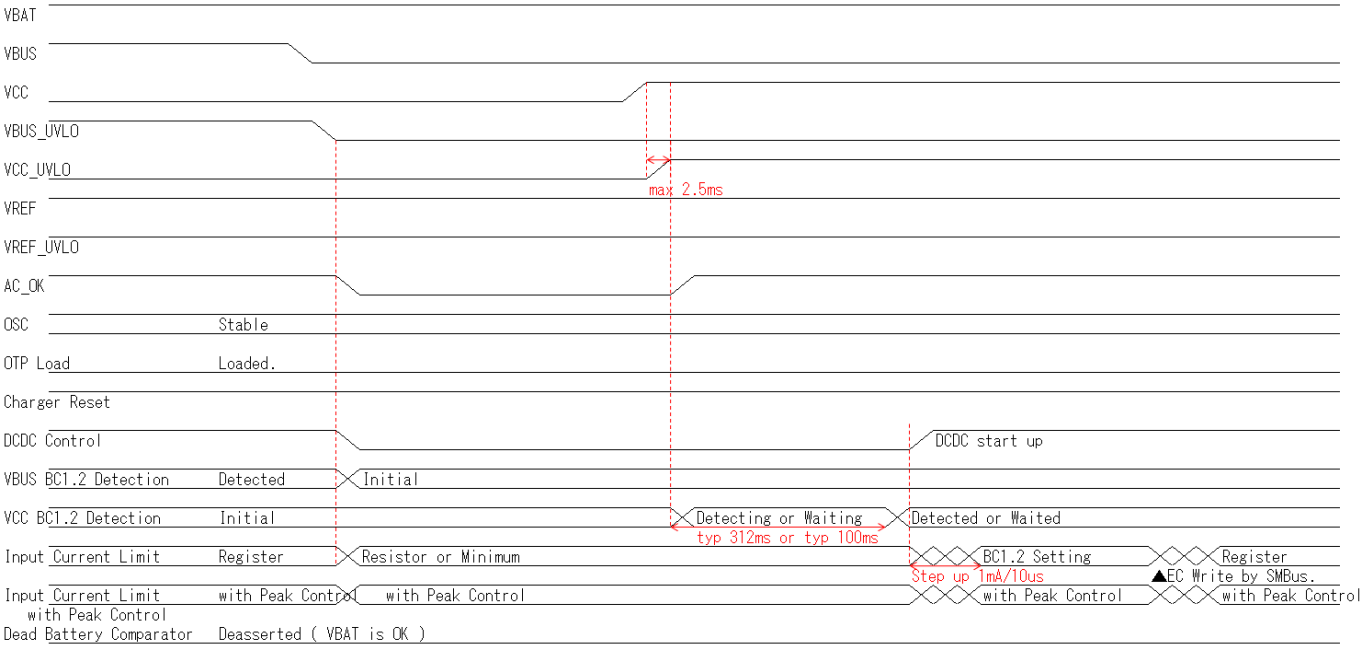
7.9.1. VBAT power on and VBUS/VCC plugged-in

At the first VBAT power on, BD99954 starts OTP loading. And when VBUS or VCC is eventually plugged in, BD99954sserts ACOK and starts the BC1.2 Detection sequence. After the BC1.2 Detection is completed, BD99954 limits the input current, reflects the BC1.2 setting and starts charging.



7.9.2. VBUS/VCC plugged-off

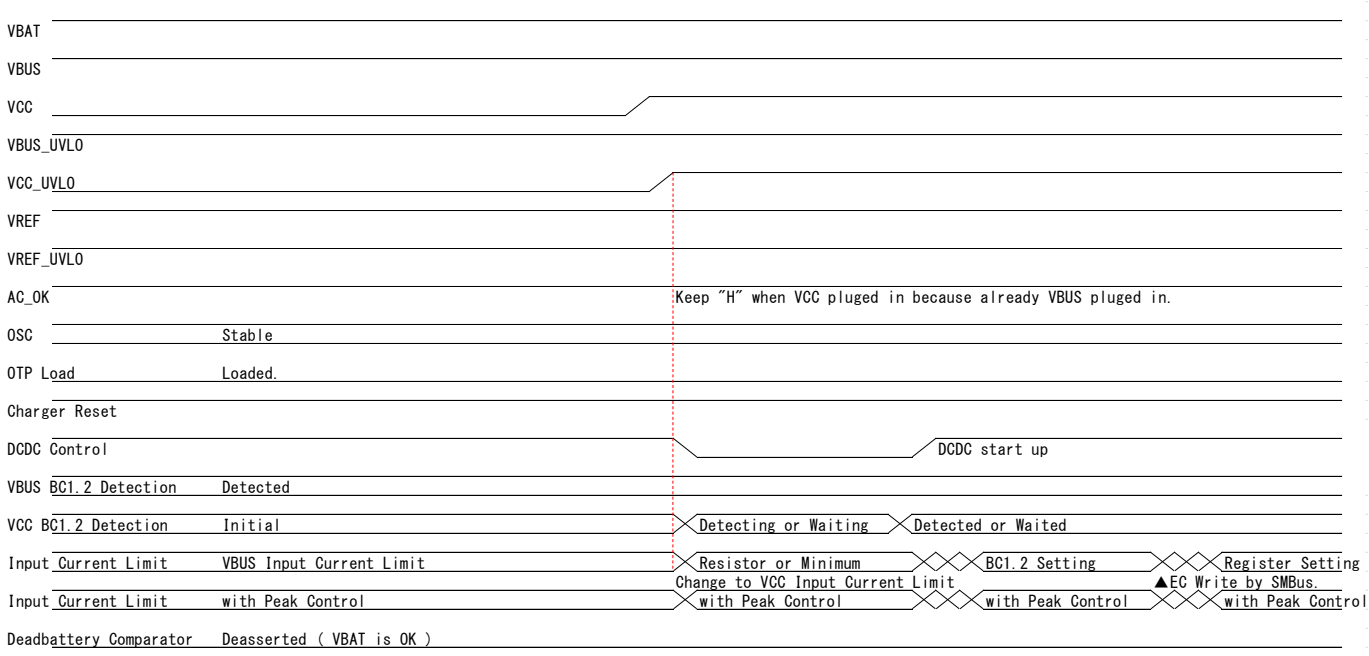
When VBUS plugged off, BD99954 deasserts AC_OK and limits input current as IADP external pin or minimum setting (it is programmable). And then VBUS or VCC plugged in again, BD99954sserts AC_OK and starts BC1.2 detection.



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7.9.3. VBUS and VCC plugged in

When VBUS plugged in and then VCC plugged in, BD99954 selects VBUS or VCC with priority setting. If VCC is 1st priority (programmable), BD99954 changes power source from VBUS to VCC. If VBUS is 1st priority BD99954 keeps power source VBUS. Each case AC_OK keeps “H”.



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8. Control Specification

BD99954 has several control registers to set configurations or to sense the hardware status for the internal function operations. Host is able to write to or read from the control registers via SMBus (friendly I2C).

8.1. SMBus Communication

BD99954 operates in slave mode on the SMBus and supports Layer 2 communication protocol.

8.1.1. SMBus Slave Address

Slave Address for the BD99954 is 0001_001.

The register address is set by “Slave Address”. The “Slave Address” is also used as the start address of contiguous addressing for multiple write or read access.

8.2. SMBus Protocols

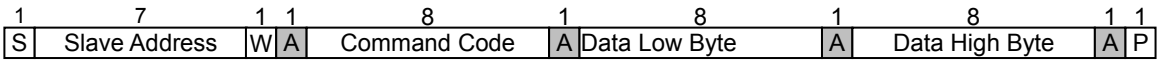
The following is a description of the various SMBus protocols. BD99954 supports the protocols defined in this section. BD99954 does not support all the protocols defined in the SMBus Specification. The results returned by such a device to a protocol it does not support is undefined.
Below is a key to the protocol diagrams in this section. Not all protocol elements will be presented in every command. For instance, not all packets are required to include the packet error code.

S	Start Condition
Sr	Repeated Start Condition
Rd	Read (bit value of 1)
Wr	Write (bit value of 0)
x	Shown under a field indicates that that field is required to have the value of ‘x’
A	Acknowledge (this bit position may be‘0’ for an ACK)
N	Acknowledge (this bit position may be‘1’ for a NACK)
P	Stop Condition
PEC	Packet Error Code
	Master (SMBus Host) to Slave
	Slave (SMBus Device) to Master

BD99954 supports following protocols.
- ✧ Write Word
- ✧ Read Word

8.2.1. Write Word

The first byte of a Write Word access is the command code. The next are the high data byte and low data byte to be written. In this example the master asserts the slave device address followed by the write bit. The device acknowledges and the master delivers the command code. The slave again acknowledges before the master sends the data bytes. The slave acknowledges each byte, and the entire transaction is finished with a STOP condition.
BD99954 does not support PEC.

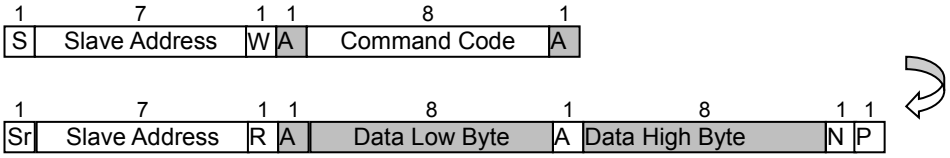


SMBus Write Word

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8.2.2. Read Word

Reading data is slightly more complicated than writing data. First the host must write a command to the slave device. Then it must follow that command with a repeated START condition to denote a read from that device's address. The slave then returns one high and low byte of data.
Note that there is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer. BD99954 does not support PEC.



SMBus Read Word

8.2.3. SMBus Communication Timing Waveforms and Timing Specification

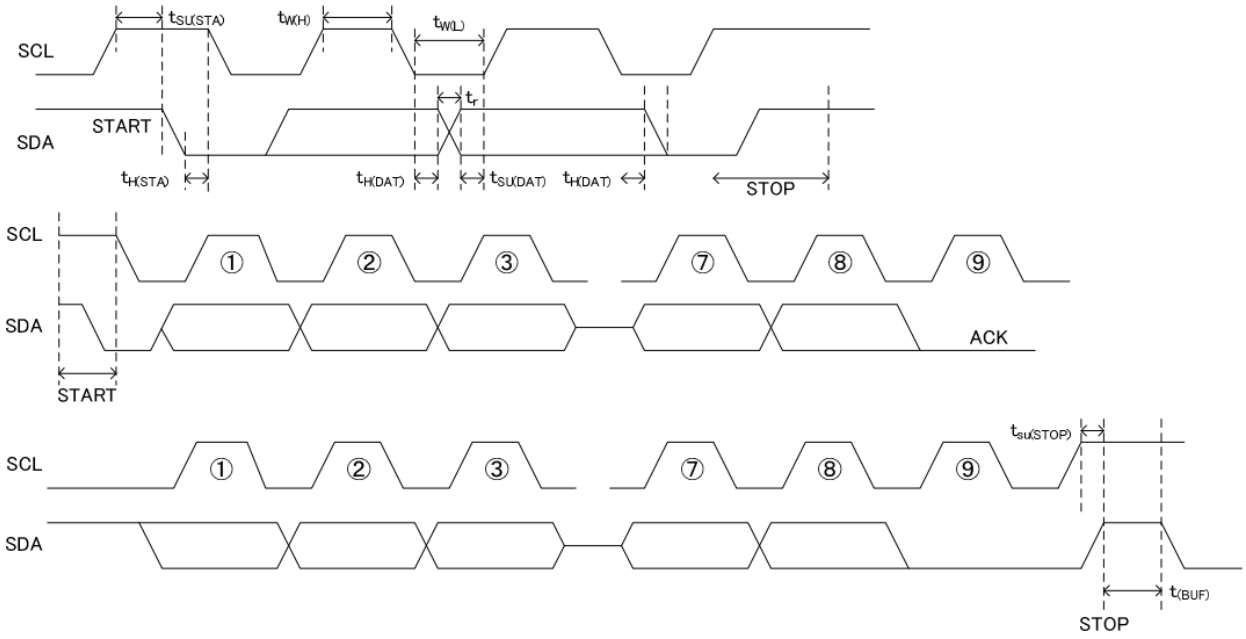


Table 8-1 Electrical Characteristics for SMBus Timing Specification
(Unless otherwise specified, Ta=25°C, VREF=1.5V)

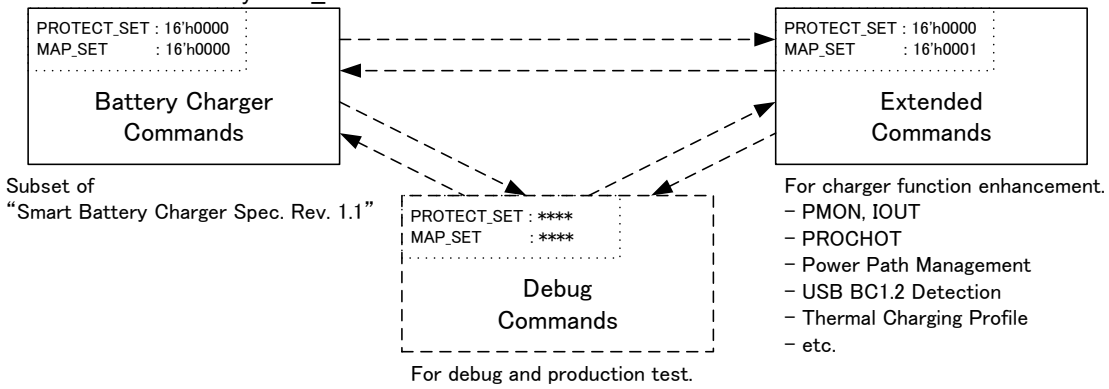
Parameter	Symbol	Specification			Unit	Condition
		Min	Typ	Max		
<SMBus>						
SMBus Frequency	F_{SMBus}	10	-	400	kHz	
SDA/SCL Input Low Voltage	V_{INL}	0.0	-	0.8	V	
SDA/SCL Input High Voltage	V_{INH}	2.1	-	5.5	V	
SDA Hold Time from SCL	$T_{H(DAT)}$	250	-	-	ns	
SDA Setup Time from SCL	$T_{SU(DAT)}$	300	-	-	ns	
Start Condition Hold Time from SCL	$T_{H(STA)}$	4	-	-	µs	
Start Condition Setup Time from SCL	$T_{SU(STA)}$	4.7	-	-	µs	
Stop Condition Setup Time from SCL	$T_{SU(STOP)}$	4	-	-	µs	
Bus Free Time	T_{BUF}	4.7	-	-	µs	

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8.3. Command Code

BD99954 has 3 command maps, "Battery Charger Commands", "Extended Commands" and "Debug Commands". All commands are addressed within 00h ~ 7Fh address area. And 80h ~ FFh address is a mirror of 00h ~ 7Fh.

"Battery Charger Commands" is a subset of "Smart Battery Charger Specification Revision 1.1."
"Extended Commands" is for charger function enhancement.
"Debug Commands" are used for debug purpose or in production test.
These are selectable by MAP_SET command.



8.3.1. Battery Charger Commands

Following is a table of "Battery Charger Commands" which BD99954 supports. "Battery Charger Commands" is subset of "Smart Battery Charger Specification Revision 1.1."
Note: Reserved command should not be accessed. If accessed, operation is not guaranteed.

Code	Command	Protocols	Byte Size	Description
14h	ChargingCurrent	Read/Write Word	2	The Battery, System Host or other master device sends the desired charging rate (mA). This command is a mirror of ICHG_SET command of the extended command.
15h	ChargingVoltage	Read/Write Word	2	The Battery, System Host or other master device sends the desired charging voltage to the Smart Battery Charger (mV). This command is a mirror of VFASTCHG_REG_SET1 command of the extended command.
3Ch	IBUS_LIM_SET	Read/Write Word	2	VBUS Input Current Limit Setting. This command is a mirror of IBUS_LIM_SET command of the extended command.
3Dh	ICC_LIM_SET	Read/Write Word	2	VCC Input Current Limit Setting. This command is a mirror of ICC_LIM_SET command of the extended command.
3Eh	PROTECT_SET	Read/Write Word	2	Access Un-protect Setting for Address 3Fh This command is a mirror of PROTECT_SET command of the extended command.
3Fh	MAP_SET	Read/Write Word	2	Change Command Code Map. This command is a mirror of MAP_SET command of the extended command.

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8.3.2. Extended Commands

Following is a table of "Extended Commands" which BD99954 supports. "Extended Commands" is for charger function enhancement.

Note: Reserved command should not be accessed. If accessed, operation is not guaranteed.

Code	Command	Protocols	Byte Size	Description
00h	CHGSTM_STATUS	Read Word	2	Charger State Machine Status
01h	VBAT/VSYS_STATUS	Read Word	2	VBAT and VSYS Status
02h	VBUS/VCC_STATUS	Read Word	2	VBUS and VCC Status
03h	CHGOP_STATUS	Read Word	2	Charger Operation Status
04h	WDT_STATUS	Read Word	2	Charger WDT and Thermal WDT Status
05h	CUR_ILIM_VAL	Read Word	2	Actual Input Current Limit
06h	SEL_ILIM_VAL	Read Word	2	Selected Input Current Limit
07h	IBUS_LIM_SET	Read/Write Word	2	VBUS Input Current Limit Setting
08h	ICC_LIM_SET	Read/Write Word	2	VCC Input Current Limit Setting
09h	IOTG_LIM_SET	Read/Write Word	2	OTG Output Current Limit Setting
0Ah	VIN_CTRL_SET	Read/Write Word	2	VBUS and VCC Control Setting
0Bh	CHGOP_SET1	Read/Write Word	2	Charger Operation Control Setting 1
0Ch	CHGOP_SET2	Read/Write Word	2	Charger Operation Control Setting 2
0Dh	VBUSCLPS_TH_SET	Read/Write Word	2	VBUS Collapse Detect Threshold Voltage Setting
0Eh	VCCCLPS_TH_SET	Read/Write Word	2	VCC Collapse Detect Threshold Voltage Setting
0Fh	CHGWDT_SET	Read/Write Word	2	Charger WDT Setting
10h	BATTWDT_SET	Read/Write Word	2	Battery temperature and Battery short current WDT Setting
11h	VSYSREG_SET	Read/Write Word	2	VSYS Regulation Setting
12h	VSYSVAL_THH_SET	Read/Write Word	2	VSYS Valid Threshold High Setting (Hysteresis)
13h	VSYSVAL_THL_SET	Read/Write Word	2	VSYS Valid Threshold Low Setting (Hysteresis)
14h	ITRICH_SET	Read/Write Word	2	Trickle-charge Current Setting
15h	IPRECH_SET	Read/Write Word	2	Pre-charge Current Setting
16h	ICHG_SET	Read/Write Word	2	Fast-charge Current Setting
17h	ITERM_SET	Read/Write Word	2	Charge Termination Current Setting
18h	VPRECHG_TH_SET	Read/Write Word	2	Pre-charge Voltage Threshold Setting
19h	VRBOOST_SET	Read/Write Word	2	Reverse Buck Boost Voltage Setting
1Ah	VFASTCHG_REG_SET1	Read/Write Word	2	Fast Charge Voltage Regulation Setting 1
1Bh	VFASTCHG_REG_SET2	Read/Write Word	2	Fast Charge Voltage Regulation Setting 2 (Hot 1)
1Ch	VFASTCHG_REG_SET3	Read/Write Word	2	Fast Charge Voltage Regulation Setting 3 (Hot 2)
1Dh	VRECHG_SET	Read/Write Word	2	Re-charge Battery Voltage Setting
1Eh	VBATOVP_SET	Read/Write Word	2	Battery Over Voltage Protection Setting
1Fh	IBATSHORT_SET	Read/Write Word	2	Battery Short Current Protection Setting
20h	PROCHOT_CTRL_SET	Read/Write Word	2	PROCHOT# pin Control Setting
21h	PROCHOT_ICRIT_SET	Read/Write Word	2	Peak Input Current Threshold Setting for PROCHOT#
22h	PROCHOT_INORM_SET	Read/Write Word	2	Average Input Current Threshold Setting for PROCHOT#
23h	PROCHOT_IDCHG_SET	Read/Write Word	2	Dis-charge Current Threshold Setting for PROCHOT#
24h	PROCHOT_VSYS_SET	Read/Write Word	2	VSYS Voltage Threshold Setting for PROCHOT#
25h	PMON_IOUT_CTRL_SET	Read/Write Word	2	PMON and IOUT Output Control Setting
26h	PMON_DACIN_VAL	Read Word	2	PMON DAC Input Value
27h	IOUT_DACIN_VAL	Read Word	2	IOUT DAC Input Value
28h	VCC_UCD_SET	Read/Write Word	2	BC1.2 Charger Detector on the VCC side Setting
29h	VCC_UCD_STATUS	Read Word	2	BC1.2 Charger Detect Status on the VCC side
2Ah	VCC_IDD_STATUS	Read Word	2	ID Detect Status on the VCC side
2Bh	VCC_UCD_FCTRL_SET	Read/Write Word	2	BC1.2 Charger Detector on the VCC side Manual Control Setting
2Ch	VCC_UCD_FCTRL_EN	Read/Write Word	2	BC1.2 Charger Detector on the VCC side Manual Control Enable
2Dh	(reserved)	-	-	-
2Eh	(reserved)	-	-	-
2Fh	(reserved)	-	-	-
30h	VBUS_UCD_SET	Read/Write Word	2	BC1.2 Charger Detector on the VBUS side Setting
31h	VBUS_UCD_STATUS	Read Word	2	BC1.2 Charger Detect Status on the VBUS side
32h	VBUS_IDD_STATUS	Read Word	2	ID Detect Status
33h	VBUS_UCD_FCTRL_SET	Read/Write Word	2	BC1.2 Charger Detector on the VBUS side Manual Control Setting

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Code	Command	Protocols	Byte Size	Description
34h	VBUS_UCD_FCTRL_EN	Read/Write Word	2	BC1.2 Charger Detector on the VBUS side Manual Control Enable
35h	(reserved)	-	2	-
36h	(reserved)	-	-	-
37h	(reserved)	-	-	-
38h	CHIP_ID	Read Word	2	Chip ID
39h	CHIP_REV	Read Word	2	Chip Revision
3Ah	IC_SET1	Read/Write Word	2	1-Cell mode setting, ACP discharge control and ACOK control setting.
3Bh	IC_SET2	Read/Write Word	2	IC Setting Register for debug and production test.
3Ch	SYSTEM_STATUS	Read Word	2	System Power-on Status
3Dh	SYSTEM_CTRL_SET	Read/Write Word	2	Software reset and re-load OTP
3Eh	PROTECT_SET	Read/Write Word	2	Access Un-protect Setting for Address FCh and FEh
3Fh	MAP_SET	Read/Write Word	2	Change Command Code Map to Debug Command Code Map
40h	VM_CTRL_SET	Read/Write Word	2	SAR-ADC Measurement Control Setting
41h	THERM_WINDOW_SET1	Read/Write Word	2	JEITA Temperature Window Setting 1
42h	THERM_WINDOW_SET2	Read/Write Word	2	JEITA Temperature Window Setting 2
43h	THERM_WINDOW_SET3	Read/Write Word	2	JEITA Temperature Window Setting 3
44h	THERM_WINDOW_SET4	Read/Write Word	2	JEITA Temperature Window Setting 4
45h	THERM_WINDOW_SET5	Read/Write Word	2	JEITA Temperature Window Setting 5
46h	IBATP_TH_SET	Read/Write Word	2	Battery Current (Charge) Interrupt Threshold Setting
47h	IBATM_TH_SET	Read/Write Word	2	Battery Current (Dis-charge) Interrupt Threshold Setting
48h	VBAT_TH_SET	Read/Write Word	2	Battery Voltage Interrupt Threshold Setting
49h	THERM_TH_SET	Read/Write Word	2	Battery Temperature Interrupt Threshold Setting
4Ah	IACP_TH_SET	Read/Write Word	2	Input Current (between ACP-ACN) Interrupt Threshold Setting
4Bh	VACP_TH_SET	Read/Write Word	2	Input Voltage (ACP) Interrupt Threshold Setting
4Ch	VBUS_TH_SET	Read/Write Word	2	VBUS Voltage Interrupt Threshold Setting
4Dh	VCC_TH_SET	Read/Write Word	2	VCC Voltage Interrupt Threshold Setting
4Eh	VSYS_TH_SET	Read/Write Word	2	VSYS Voltage Interrupt Threshold Setting
4Fh	EXTIADP_TH_SET	Read/Write Word	2	IADP (Input current Limit setting pin) Voltage Interrupt Threshold Setting
50h	IBATP_VAL	Read Word	2	Battery Current (Charge) Measurement Value
51h	IBATP_AVE_VAL	Read Word	2	Battery Current (Charge) Measurement Average Value
52h	IBATM_VAL	Read Word	2	Battery Current (Dis-charge) Measurement Value
53h	IBATM_AVE_VAL	Read Word	2	Battery Current (Dis-charge) Measurement Average Value
54h	VBAT_VAL	Read Word	2	Battery Voltage Measurement Value
55h	VBAT_AVE_VAL	Read Word	2	Battery Voltage Measurement Average Value
56h	THERM_VAL	Read/Write Word	2	Temperature Measurement Value
57h	VTH_VAL	Read Word	2	Thermistor Measurement Voltage Value
58h	IACP_VAL	Read Word	2	Input Current (between ACP-ACN) Measurement Value
59h	IACP_AVE_VAL	Read Word	2	Input Current (between ACP-ACN) Measurement Average Value
5Ah	VACP_VAL	Read Word	2	Input Voltage (ACP) Measurement Value
5Bh	VACP_AVE_VAL	Read Word	2	Input Voltage (ACP) Measurement Average Value
5Ch	VBUS_VAL	Read Word	2	VBUS Voltage Measurement Value
5Dh	VBUS_AVE_VAL	Read Word	2	VBUS Voltage Measurement Average Value
5Eh	VCC_VAL	Read Word	2	VCC Voltage Measurement Value
5Fh	VCC_AVE_VAL	Read Word	2	VCC Voltage Measurement Average Value
60h	VSYS_VAL	Read Word	2	VSYS Voltage Measurement Value
61h	VSYS_AVE_VAL	Read Word	2	VSYS Voltage Measurement Average Value
62h	EXTIADP_VAL	Read Word	2	IADP (Input current Limit setting pin) Voltage Measurement Value
63h	EXTIADP_AVE_VAL	Read Word	2	IADP (Input current Limit setting pin) Voltage Measurement Average Value
64h	VACPCLPS_TH_SET	Read/Write Word	2	VACP Collapse Detect Threshold Voltage Setting
65h	(reserved)	-	-	-
66h	(reserved)	-	-	-
67h	(reserved)	-	-	-
68h	INT0_SET	Read/Write Word	2	1st Level Interrupt Setting
69h	INT1_SET	Read/Write Word	2	2nd Level Interrupt Setting 1 (VBUS)
6Ah	INT2_SET	Read/Write Word	2	2nd Level Interrupt Setting 2 (VCC)

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Code	Command	Protocols	Byte Size	Description
6Bh	INT3_SET	Read/Write Word	2	2nd Level Interrupt Setting 3 (Battery)
6Ch	INT4_SET	Read/Write Word	2	2nd Level Interrupt Setting 4 (VSYS)
6Dh	INT5_SET	Read/Write Word	2	2nd Level Interrupt Setting 5 (Charger)
6Eh	INT6_SET	Read/Write Word	2	2nd Level Interrupt Setting 6 (Charger)
6Fh	INT7_SET	Read/Write Word	2	2nd Level Interrupt Setting 7 (SAR-ADC)
70h	INT0_STATUS	Read/Write Word	2	1st Level Interrupt Status
71h	INT1_STATUS	Read/Write Word	2	2nd Level Interrupt Status 1 (VBUS)
72h	INT2_STATUS	Read/Write Word	2	2nd Level Interrupt Status 2 (VCC)
73h	INT3_STATUS	Read/Write Word	2	2nd Level Interrupt Status 3 (Battery)
74h	INT4_STATUS	Read/Write Word	2	2nd Level Interrupt Status 4 (VSYS)
75h	INT5_STATUS	Read/Write Word	2	2nd Level Interrupt Status 5 (Charger)
76h	INT6_STATUS	Read/Write Word	2	2nd Level Interrupt Status 6 (Charger)
77h	INT7_STATUS	Read/Write Word	2	2nd Level Interrupt Status 7 (SAR-ADC)
78h	REG0	Read/Write Word	2	Reserved Register 0 (for future use)
79h	REG1	Read/Write Word	2	Reserved Register 1 (for future use)
7Ah	OTPREG0	Read/Write Word	2	Input current limit degradation setting.
7Bh	OTPREG1	Read/Write Word	2	Reserved OTP-loaded Register 1 (for future use)
7Ch	SMBREG	Read/Write Word	2	Power Save Mode Setting.
7Dh	(reserved)	-	-	-
7Eh	(reserved)	-	-	-
7Fh	DEBUG_MODE_SET	Read/Write Word	2	Debug Mode Setting

8.3.3. Debug Commands

Following is a table of "Debug Commands" which BD99954 supports. "Debug Commands" is used for debug purpose or in production test.

Note: Reserved command should not be accessed. If accessed, operation is not guaranteed.

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8.4. Battery Charger Commands Description

Following is a description of " Battery Charger Commands " that are supported by BD99954.

8.4.1. ChargingCurrent

The Battery, System Host or other master device sends the desired charging rate (mA).

Command Code: 14h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	ICHG_SET[13]	Charging current setting. 0 to 16,320mA, 64mA steps.
12	ICHG_SET[12]	
11	ICHG_SET[11]	
10	ICHG_SET[10]	
9	ICHG_SET[9]	
8	ICHG_SET[8]	
7	ICHG_SET[7]	
6	ICHG_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.4.2. ChargingVoltage

The Battery, System Host or other master device sends the desired charging voltage to the Smart Battery Charger (mV).

Command Code: 15h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VFASTCHG_REG_SET1[14]	Charging Regulation Voltage. 3,072 to 19,200mV, 16mV steps. The register range : 0 to 32,752mV. But the actual range : 3,072 to 19,200mV.
13	VFASTCHG_REG_SET1[13]	
12	VFASTCHG_REG_SET1[12]	
11	VFASTCHG_REG_SET1[11]	
10	VFASTCHG_REG_SET1[10]	
9	VFASTCHG_REG_SET1[9]	
8	VFASTCHG_REG_SET1[8]	
7	VFASTCHG_REG_SET1[7]	
6	VFASTCHG_REG_SET1[6]	
5	VFASTCHG_REG_SET1[5]	
4	VFASTCHG_REG_SET1[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.4.3. IBUS_LIM_SET

VBUS Input Current Limit Setting

Command Code: 3Ch
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	IBUS_LIM_SET1[13]	VBUS input current limitation. 0 to 16,352mA, 32mA steps.
12	IBUS_LIM_SET1[12]	
11	IBUS_LIM_SET1[11]	
10	IBUS_LIM_SET1[10]	
9	IBUS_LIM_SET1[9]	
8	IBUS_LIM_SET1[8]	
7	IBUS_LIM_SET1[7]	
6	IBUS_LIM_SET1[6]	
5	IBUS_LIM_SET1[5]	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.4.4. ICC_LIM_SET

VCC Input Current Limit Setting

Command Code: 3Dh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	ICC_LIM_SET1[13]	VCC input current limitation. 0 to 16,352mA, 32mA steps.
12	ICC_LIM_SET1[12]	
11	ICC_LIM_SET1[11]	
10	ICC_LIM_SET1[10]	
9	ICC_LIM_SET1[9]	
8	ICC_LIM_SET1[8]	
7	ICC_LIM_SET1[7]	
6	ICC_LIM_SET1[6]	
5	ICC_LIM_SET1[5]	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.4.5. PROTECT_SET

Access Un-protect Setting for the “debug command map” (debug and production test only)

Command Code: 3Eh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	PROTECT_SET[15]	Access Un-protect Setting for the “debug command map” (debug and production test only)
14	PROTECT_SET[14]	
13	PROTECT_SET[13]	
12	PROTECT_SET[12]	
11	PROTECT_SET[11]	
10	PROTECT_SET[10]	
9	PROTECT_SET[9]	
8	PROTECT_SET[8]	
7	PROTECT_SET[7]	
6	PROTECT_SET[6]	
5	PROTECT_SET[5]	
4	PROTECT_SET[4]	
3	PROTECT_SET[3]	
2	PROTECT_SET[2]	
1	PROTECT_SET[1]	
0	PROTECT_SET[0]	

8.4.6. MAP_SET

Change Command Code Map

Command Code: 3Fh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	MAP_SET [15]	Change Command Code Map
14	MAP_SET [14]	
13	MAP_SET[13]	
12	MAP_SET[12]	
11	MAP_SET[11]	
10	MAP_SET[10]	
9	MAP_SET[9]	
8	MAP_SET[8]	
7	MAP_SET[7]	
6	MAP_SET[6]	
5	MAP_SET[5]	
4	MAP_SET[4]	
3	MAP_SET[3]	
2	MAP_SET[2]	
1	MAP_SET[1]	
0	MAP_SET[0]	

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8.5. Extended Commands Description

Following is a description of "Extended Commands" that are supported by BD99954.

8.5.1. CHGSTM_STATUS

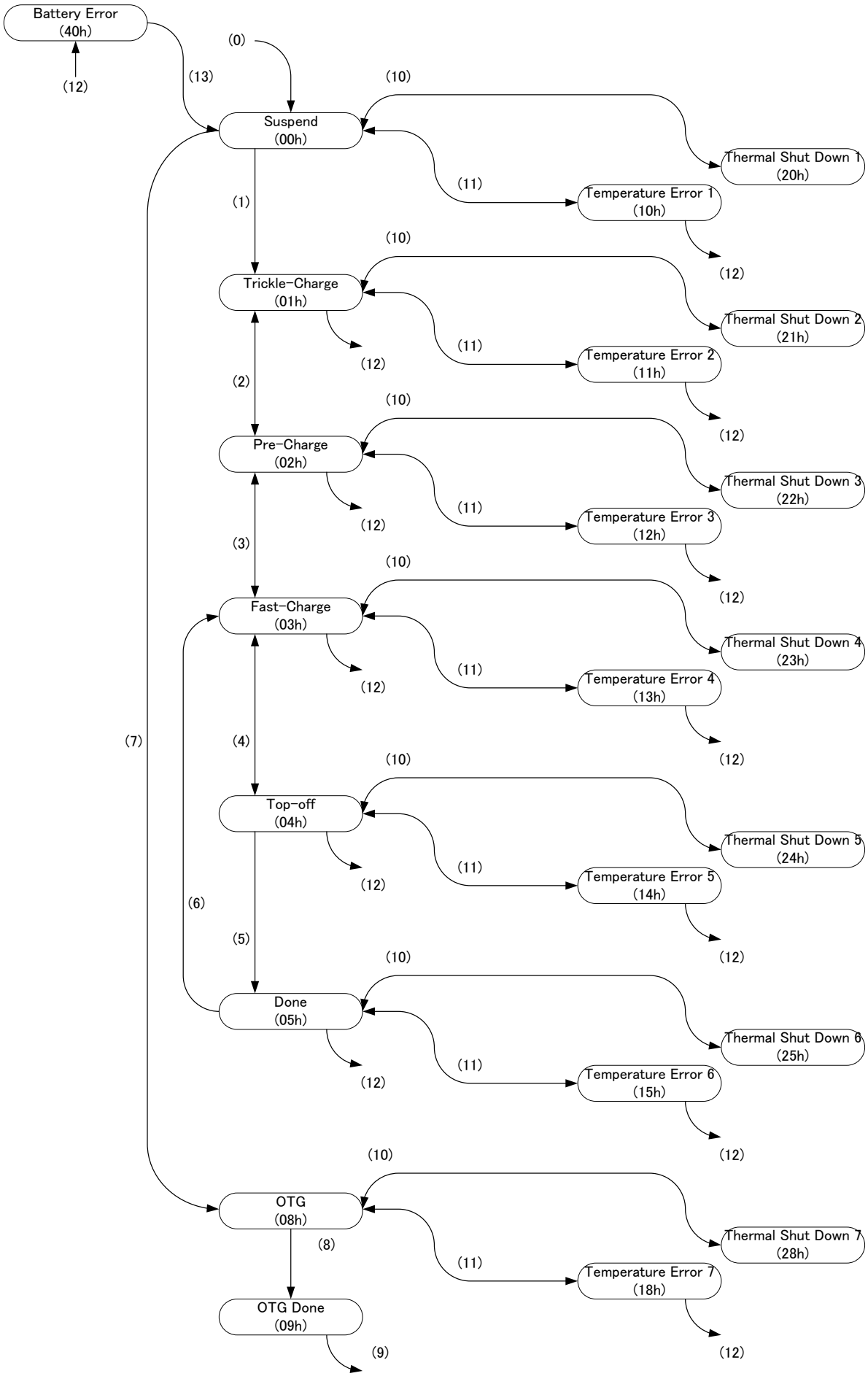
Charger State Machine Status

Command Code: 00h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	PREV_CHGSTM_STATE[6]	The previous state of the charger state-machine.
13	PREV_CHGSTM_STATE[5]	
12	PREV_CHGSTM_STATE[4]	
11	PREV_CHGSTM_STATE[3]	
10	PREV_CHGSTM_STATE[2]	
9	PREV_CHGSTM_STATE[1]	
8	PREV_CHGSTM_STATE[0]	
7	reserved	
6	CHGSTM_STATE[6]	The current state of the charger state-machine.
5	CHGSTM_STATE[5]	
4	CHGSTM_STATE[4]	
3	CHGSTM_STATE[3]	
2	CHGSTM_STATE[2]	
1	CHGSTM_STATE[1]	
0	CHGSTM_STATE[0]	

State definition. **CHGSTM_STATE** **PREV_CHGSTM_STATE**	State Name	Description
00h	Suspend	Suspend charging
01h	Trickle-Charge	Trickle-charging
02h	Pre-Charge	Pre-charging
03h	Fast-Charge	Fast Charging
04h	Top-off	Reached to Termination Current
05h	Done	Charging finished
08h	OTG	USB On The Go (Reverse Buck Boost Operation)
09h	OTG Done	OTG Done
10h	Temperature Error 1	Out of standard temperature while Suspend State
11h	Temperature Error 2	Out of standard temperature while Trickle-Charge State
12h	Temperature Error 3	Out of standard temperature while Pre-Charge State
13h	Temperature Error 4	Out of standard temperature while Fast-Charge State
14h	Temperature Error 5	Out of standard temperature while Top-off State
15h	Temperature Error 6	Out of standard temperature while after Top-off State (DONE)
18h	Temperature Error 7	Out of standard temperature while OTG State
20h	Thermal Shut Down 1	Thermal Shut Down while Suspend State
21h	Thermal Shut Down 2	Thermal Shut Down while Trickle-Charge State
22h	Thermal Shut Down 3	Thermal Shut Down while Pre-Charge State
23h	Thermal Shut Down 4	Thermal Shut Down while Fast-Charge State
24h	Thermal Shut Down 5	Thermal Shut Down while Top-off State
25h	Thermal Shut Down 6	Thermal Shut Down after Top-off State (DONE)
28h	Thermal Shut Down 7	Thermal Shut Down while OTG State
40h	Battery Error	Battery Error

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Arc #	Condition to next state	back to previous state
(0)	CHG_EN is 0, disabled or USB_SUS is 1, suspended. or VBUS and VCC and VACP are undetected or disabled. or Thermistor is open. or Power Path is changed. or Anti-collapse is occurred. or VSYS SCP timer is expired (20ms).	-----
(1)	VBUS or VCC or VACP detected. and SDP_CHG_TRIG bit set if SDP_CHG_TRIG_EN=1 and SDP port detected. and Charge enable. and DCDC Soft-started. and State Transition Timer expired (25ms). and No anti-collapse occurred. and No Vsys short occurred.	-----
(2)	VBAT > VPRECHG_TH_SET and State Transition Timer expired (25ms).	- VBAT <= VPRECHG_TH_SET and State Transition Timer expired (25ms).
(3)	VBAT > VSYSREG_SET and AUTO_FST=1 and State Transition Timer expired (25ms).	VBAT <= VSYSREG_SET and State Transition Timer expired (25ms).
(4)	ITERM comparotor asserted. and AUTO_TOF=1 and VBAT > Re-charge Battery Voltage and State Transition Timer expired (25ms).	ITERM comparotor deasserted or VBAT <= Re-charge Battery Voltage and State Transition Timer expired (25ms).
(5)	Charging Termination Timer expired (15s).	-----
(6)	-----	VBAT <= Re-charge Battery Voltage and State Transition Timer expired (25ms).
(7)	OTG Device is detected or VRBOOST_EN is enabled. and VRBOOST_TRIG=1 and VBUS and VCC and VACP is undetected. and Power Path with OTG Device is enabled, VBUS_EN/VCC_EN=1 and State Transition Timer expired (25ms).	-----
(8)	OTG Device is undetected or VRBOOST_EN is disabled or VRBOOST_TRIG=0. and State Transition Timer expired (25ms).	-----
(9)	State Transition Timer expired (25ms). and Reverse Buck Boost Voltage is under UVLO level.	-----
(10)	TSD comparator asserted.	TSD comparator de-asserted. and State Transition Timer expired (25ms).
(11)	Thermal range is HOT3 or COLD2. and State Transition Timer expired (25ms).	Thermal range isn't HOT3 and COLD2. and State Transition Timer expired (25ms).
(12)	Charger WDT is expired or Thermal WDT is expired or VBAT >= Battery Over voltage	-----
(13)	<Charging> VBAT < Battery Over voltage and Charge is disabled or suspended. Or VBUS and VCC and VACP are undetected or disabled. Or Thermistor is open. Or Power Path is changed. <OTG> OTG Device is undetected or RBOOST_EN is disabled. or USB_SUS=1, suspended.	-----

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8.5.2. VBAT/VSYS_STATUS

VBAT and VSYS Status

Command Code: 01h
Bus Protocol: Read Word

Bit	Symbol	Description
15	VSYS_OV	VSYS over-voltage status. “1”: VSYS > VSYS_OVP / “0”: VSYS < VSYS_OVP
14	VSYS_SSD	DCDC Soft-Start completion status. “1”: Soft-Start finished / “0”: Not finished.
13	VSYS_SCP	VSYS short-circuit detection status. “1”: VSYS SCP timer expired. / “0”: Normal operation.
12	VSYS_UVN	VSYS UVLO detection status. “1”: Low voltage. / “0”: Normal voltage.
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	reserved	
6	IBAT_SHORT	Battery short-circuits detection status. “1”: Battery Short Current Detected / “0”: Normal operation
5	reserved	
4	reserved	
3	VBAT_OV	VBAT over-voltage Status. “1”: VBAT > VBAT_OVP / “0”: VBAT < VBAT_OVP with Hysteresis
2	reserved	
1	reserved	
0	DEAD_BAT	Dead Battery status. “1”: Dead Battery, VBAT < VSYSREG_SET, Detected / “0”: Normal operation, VBAT >= VSYSREG_SET.

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8.5.3. VBUS/VCC_STATUS

VBUS and VCC Status

Command Code: 02h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	VACP_DET	VACP_detection status. “1”: VACP detected (over UVLO level) / “0”: not detected or low level.
11	VCC_OVP	VCC/VACP over-voltage status. "1":VCC > VCC_OVP / "0":Normal voltage. (When VCC_EN = 1) "1":VACP > VCC_OVP / "0":Normal voltage. (When VCC_EN = VBUS_EN = 0)
10	ILIM_VCC_MOD	VCC/VACP input current limit control status. “1”: VCC input current limit controlled. / “0”: No. (When VCC_EN = 1) “1”: VACP input current limit controlled. / “0”: No. (When VCC_EN = VBUS_EN = 0)
9	VCC_CLPS	VCC/VACP anti-collapse status. “1”: VCC Anti-collapse / “0”: normal operation. (When VCC_EN = 1) “1”: VACP Anti-collapse / “0”: normal operation. (When VCC_EN = VBUS_EN = 0)
8	VCC_DET	VCC detection status. “1”: VCC detected (over UVLO level) / “0”: not detected or low level.
7	reserved	
6	reserved	
5	reserved	
4	reserved	
3	VBUS_OVP	VBUS over -voltage status. “1”: VBUS > VBUS_OVP / “0”: Normal voltage.
2	ILIM_VBUS_MOD	VBUS current limit control statusStatus. “1”: Limit controlled. / “0”: No.
1	VBUS_CLPS	VBUS anti-collapse status. “1”: Anti-collapse / “0”: normal operation.
0	VBUS_DET	VBUS detection status. “1”: VBUS detected (over UVLO level) / “0”: not detected or low level.

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8.5.4. CHGOP_STATUS

Charger Operation Status

Command Code: 03h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	BATTEMP[2]	Battery temperature range and the thermistor status. Please see next table.
9	BATTEMP[1]	
8	BATTEMP[0]	
7	reserved	
6	VRECHG_DET	Re-charge voltage detection status. “1”: VBAT < VRECHG_SET / “0”: VBAT keeps enough voltage.
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	RBOOST_UV	Reverse Buck Boost UVLO detection status. “1”: Normal voltage. / “0”: Low voltage.
0	RBOOSTS	Reverse Buck Boost status. “1”: Boosting / “0”: Not boosting.

BAT_TEMP	Temperature Range	Description
0h	Room Temp	T2 < Tbat < T3
1h	HOT1	T3 < Tbat < T5
2h	HOT2	T5 < Tbat < T4
3h	HOT3	T4 < Tbat
4h	COLD1	T1 < Tbat < T2
5h	COLD2	Tbat < T1
6h	Temp. Disable	Disable thermal control (No Thermistor)
7h	Battery Open	TSENSE_BAT port is open.

Register Name	Description	Default Value	Note
TMPTHR1A[7:0]	Lower threshold of T1	C6h (2 deg.)	T1 in JEITA profile
TMPTHR1B[7:0]	Upper threshold of T1	C3h (5 deg.)	T1 in JEITA profile
TMPTHR2A[7:0]	Lower threshold of T2	BEh (10 deg.)	T2 in JEITA profile
TMPTHR2B[7:0]	Upper threshold of T2	BBh (13 deg.)	T2 in JEITA profile
TMPTHR3A[7:0]	Lower threshold of T3	9Eh (42 deg.)	T3 in JEITA profile
TMPTHR3B[7:0]	Upper threshold of T3	9Bh (45 deg.)	T3 in JEITA profile
TMPTHR4A[7:0]	Lower threshold of T4	91h (55 deg.)	T4 in JEITA profile
TMPTHR4B[7:0]	Upper threshold of T4	8Eh (58 deg.)	T4 in JEITA profile
TMPTHR5A[7:0]	Lower threshold of T5	9Dh (47 deg.)	Between T3 and T4
TMPTHR5B[7:0]	Upper threshold of T5	96h (50 deg.)	Between T3 and T4

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8.5.5. WDT_STATUS

Charger WDT and Battery Temperature WDT Status

Command Code: 04h
Bus Protocol: Read Word

Bit	Symbol	Description
15	THERMWDT_VAL[7]	Current Battery Temperature Watch-dog Timer Count Value 0 to 255 minutes, 1-minute steps.
14	THERMWDT_VAL[6]	
13	THERMWDT_VAL[5]	
12	THERMWDT_VAL[4]	
11	THERMWDT_VAL[3]	
10	THERMWDT_VAL[2]	
9	THERMWDT_VAL[1]	
8	THERMWDT_VAL[0]	
7	CHGWDT_VAL[7]	Current Charge Watch-dog Timer Count Value For pre-charging, 0 to 255 minutes, 1-minute steps. For fast-charging, 0 to 1020 minutes, 4-minutes steps.
6	CHGWDT_VAL[6]	
5	CHGWDT_VAL[5]	
4	CHGWDT_VAL[4]	
3	CHGWDT_VAL[3]	
2	CHGWDT_VAL[2]	
1	CHGWDT_VAL[1]	
0	CHGWDT_VAL[0]	

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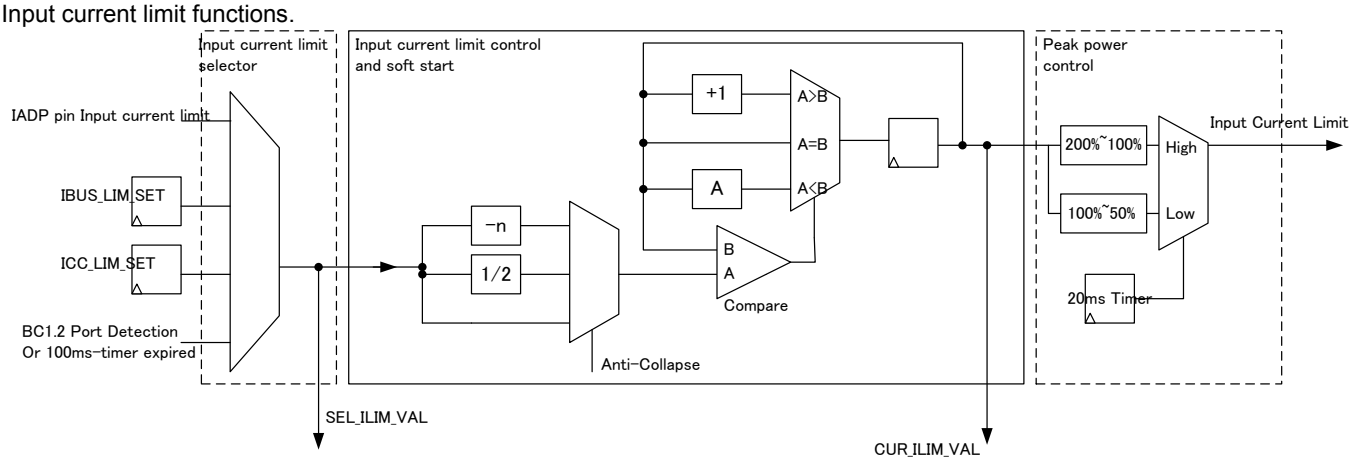
8.5.6. CUR_ILIM_VAL

Actual Input Current Limit

Command Code: 05h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	CUR_ILIM_VAL[13]	Current Input Current Limit Value 0 to 16,383mA, 1mA steps.
12	CUR_ILIM_VAL[12]	
11	CUR_ILIM_VAL[11]	
10	CUR_ILIM_VAL[10]	
9	CUR_ILIM_VAL[9]	
8	CUR_ILIM_VAL[8]	
7	CUR_ILIM_VAL[7]	
6	CUR_ILIM_VAL[6]	
5	CUR_ILIM_VAL[5]	
4	CUR_ILIM_VAL[4]	
3	CUR_ILIM_VAL[3]	
2	CUR_ILIM_VAL[2]	
1	CUR_ILIM_VAL[1]	
0	CUR_ILIM_VAL[0]	

Input current limit functions.



Input current limit selector:
The “Input current limit selector” block selects an original input current limit from the register setting or detected BC1.2, DCP/CDP/SDP, result.

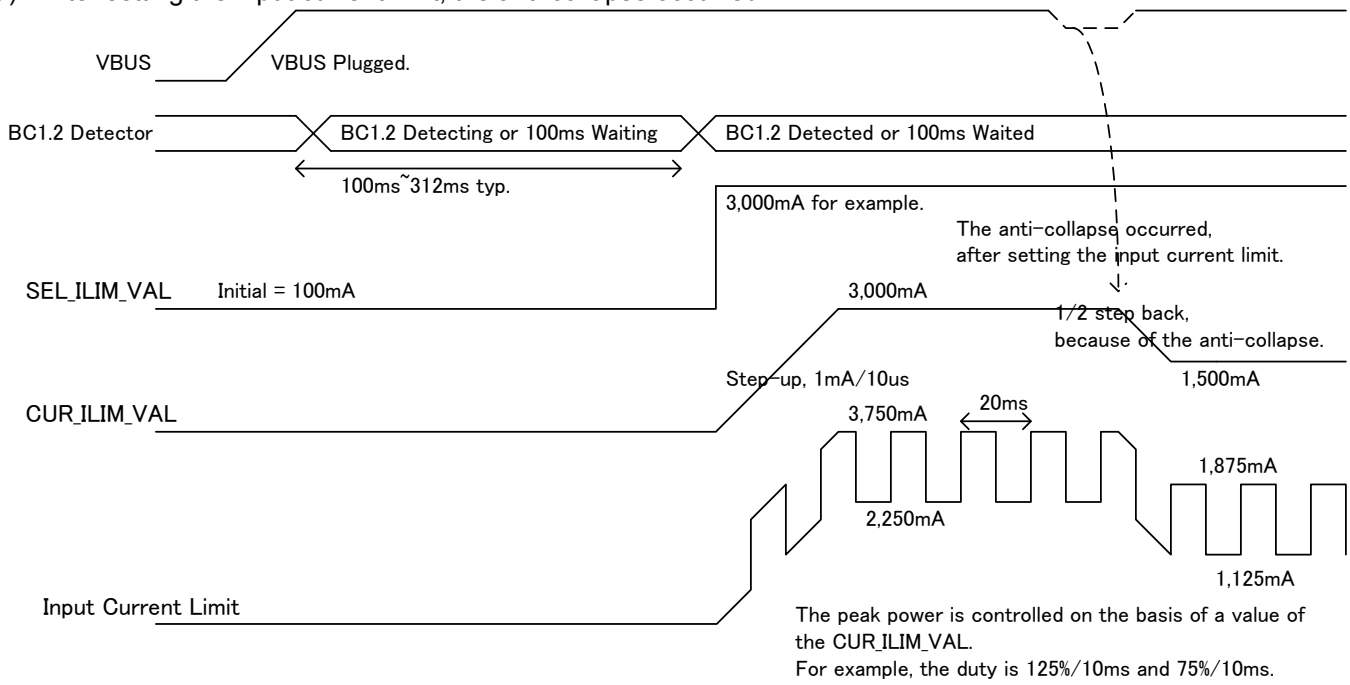
Input current limit control and soft start:
The “Input current limit control and soft start” block controls the input current limit slope 1mA/10us for soft start. And this block modifies the input current limit, -N or 1/2, when the anti-collapse occurs.

Peak power control:
The “Peak power control” block controls the peak of the input current limit. It is defined by VIN_CTRL_SET.PPC_CAP[1:0] and PPC_SUB_CAP[1:0] registers.

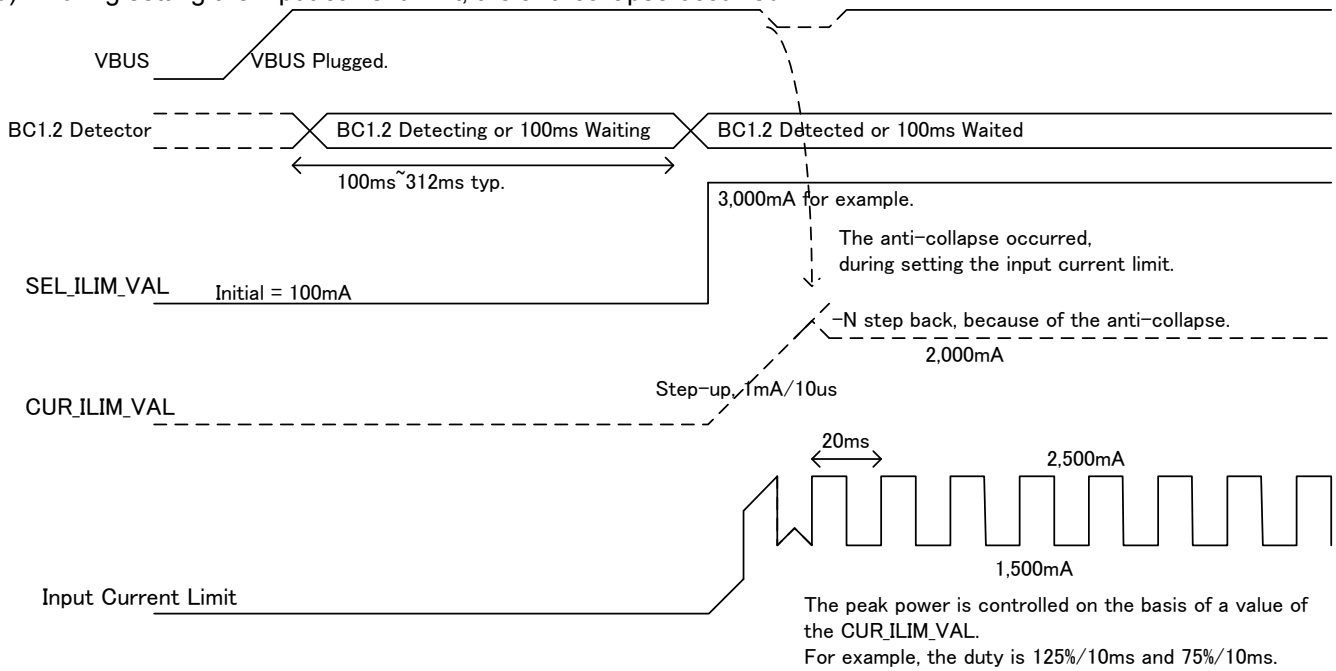
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Sample case timing chart: Input current limit with peak control.

a) After setting the input current limit, the anti-collapse occurred.

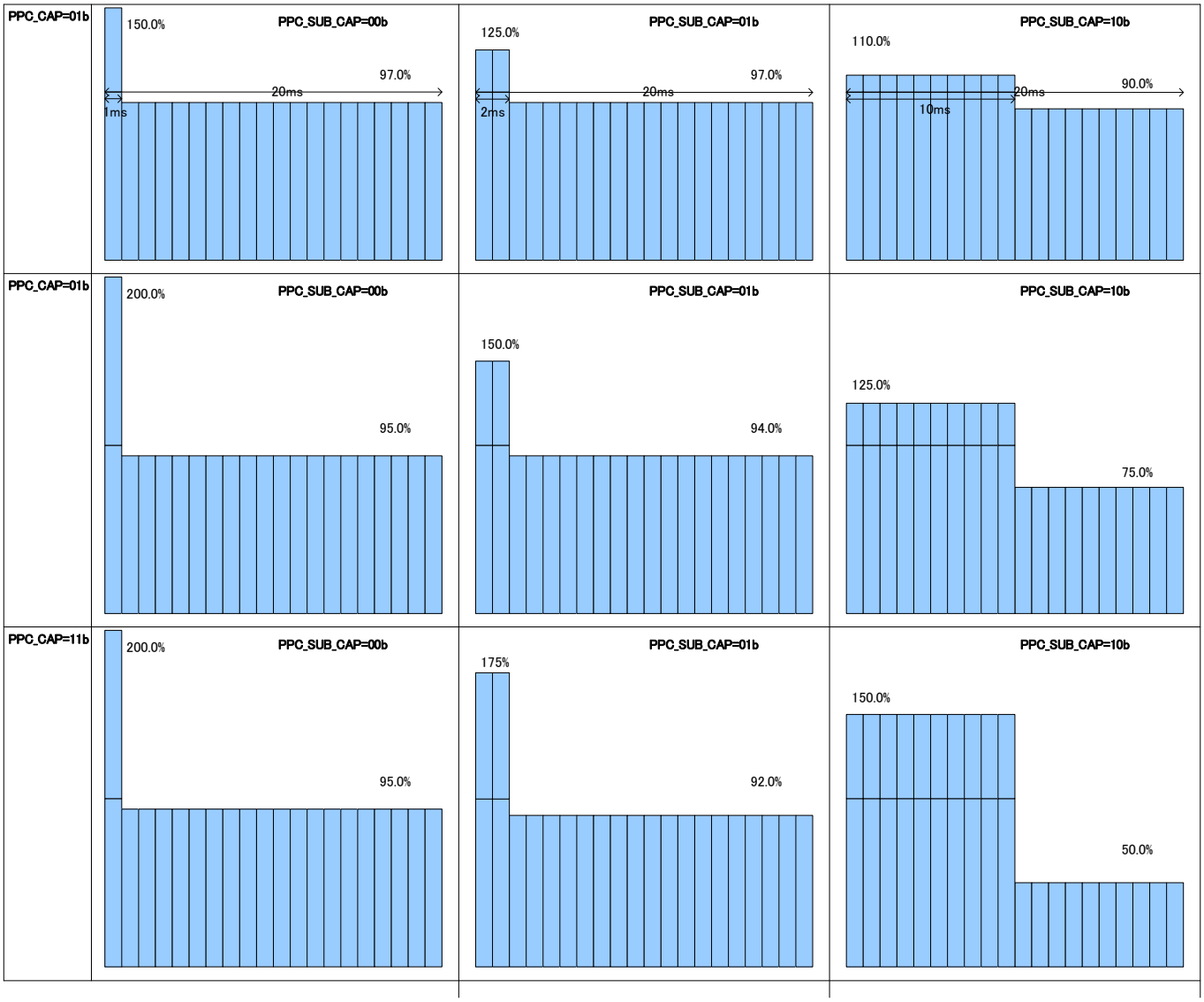


b) During setting the input current limit, the anti-collapse occurred.



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Peak input current control operation is defined by VIN_CTRL_SET.PPC_CAP[1:0] and PPC_SUB_CAP[1:0] as belowdemonstrates.



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8.5.7. SEL_ILIM_VAL

Selected Input Current Limit

Command Code: 06h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	SEL_ILIM_VAL[13]	Selected Input Current Limit Setting 0 to 16,383mA, 1mA steps.
12	SEL_ILIM_VAL[12]	
11	SEL_ILIM_VAL[11]	
10	SEL_ILIM_VAL[10]	
9	SEL_ILIM_VAL[9]	
8	SEL_ILIM_VAL[8]	
7	SEL_ILIM_VAL[7]	
6	SEL_ILIM_VAL[6]	
5	SEL_ILIM_VAL[5]	
4	SEL_ILIM_VAL[4]	
3	SEL_ILIM_VAL[3]	
2	SEL_ILIM_VAL[2]	
1	SEL_ILIM_VAL[1]	
0	SEL_ILIM_VAL[0]	

8.5.8. IBUS_LIM_SET

VBUS Input Current Limit Setting

Command Code: 07h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	IBUS_LIM_SET[13]	VBUS input current limitation. 0 to 16,352mA, 32mA steps.
12	IBUS_LIM_SET[12]	
11	IBUS_LIM_SET[11]	
10	IBUS_LIM_SET[10]	
9	IBUS_LIM_SET[9]	
8	IBUS_LIM_SET[8]	
7	IBUS_LIM_SET[7]	
6	IBUS_LIM_SET[6]	
5	IBUS_LIM_SET[5]	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.5.9. ICC_LIM_SET

VCC/VACP Input Current Limit Setting

Command Code: 08h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	ICC_LIM_SET[13]	VCC input current limitation. (When VCC_EN=1) VACP input current limitation. (When VCC_EN=VBUS_EN=0) 0 to 16,352mA, 32mA steps.
12	ICC_LIM_SET[12]	
11	ICC_LIM_SET[11]	
10	ICC_LIM_SET[10]	
9	ICC_LIM_SET[9]	
8	ICC_LIM_SET[8]	
7	ICC_LIM_SET[7]	
6	ICC_LIM_SET[6]	
5	ICC_LIM_SET[5]	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.10. IOTG_LIM_SET

OTG Output Current Limit Setting

Command Code: 09h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	IOTG_LIM_SET[13]	VBUS/VCC output current limit when OTG. 0 to 16,352mA, 32mA steps.
12	IOTG_LIM_SET[12]	
11	IOTG_LIM_SET[11]	
10	IOTG_LIM_SET[10]	
9	IOTG_LIM_SET[9]	
8	IOTG_LIM_SET[8]	
7	IOTG_LIM_SET[7]	
6	IOTG_LIM_SET[6]	
5	IOTG_LIM_SET[5]	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.5.11. VIN_CTRL_SET

VBUS and VCC Control Setting

Command Code: 0Ah
Bus Protocol: Read/Write Word

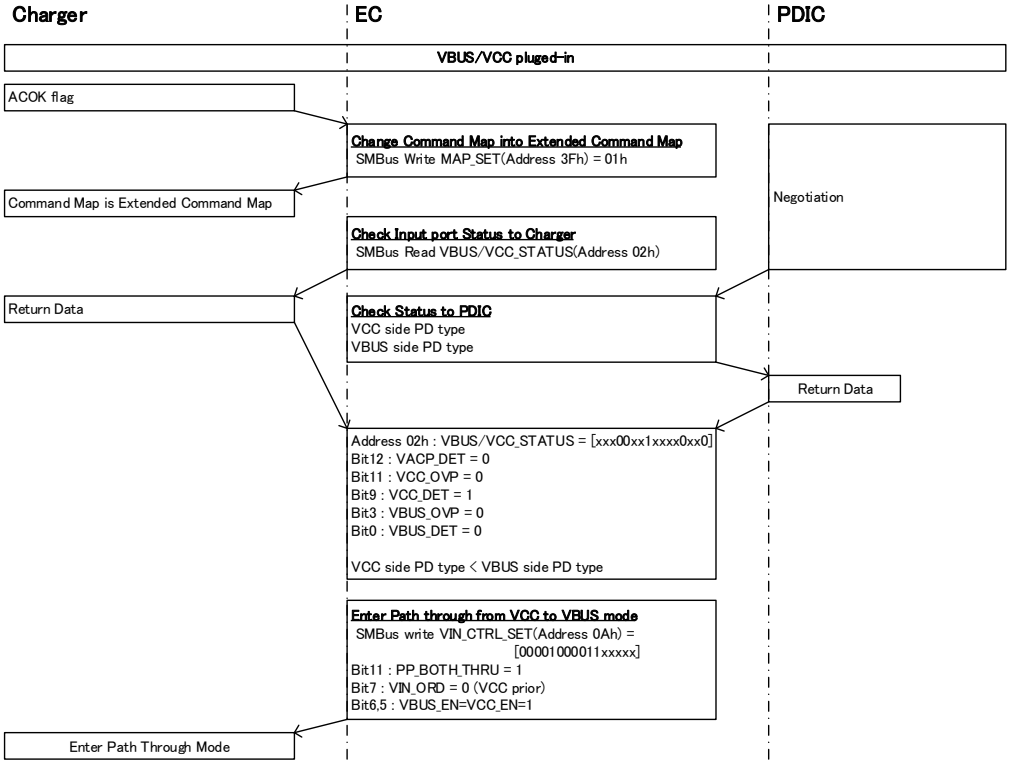
Bit	Symbol	Description
15	OTG_BOTH_EN	"Enabling OTG reverse buck boost output to VBUS and VCC both. “1”: Enable / “0”: Disable." When OTG_BOTH_EN=1 and VBUS_EN=VCC_EN=1, OTG reverse buck boost output same voltage at VBUS and VCC, VBUS=VCC=VRBOOST_SEL[14:6].
14	VRBOOST_TRIG	Reverse buck Boost operation Trigger. “1”: Trigger/ “0”; No trigger
13	VRBOOST_EN[1]	Enabling VCC Reverse buck Boost operation. “1”: Enable / “0”: Disable.
12	VRBOOST_EN[0]	Enabling VBUS Reverse buck Boost operation. “1”: Enable / “0”: Disable.
11	PP_BOTH_THRU	"Enabling output to VBUS and VCC both. “1”: Enable / “0”: Disable." When PP_BOTH_THRU=1 and VBUS_EN=VCC_EN=1, VIN_ORD=0 : Power path output same voltage from VCC to VBUS, VIN_ORD=1 : Power path output same voltage from VBUS to VCC.
10	reserved	
9	reserved	
8	reserved	
7	VIN_ORD	VBUS / VCC input priority. “1”: VBUS prior / “0”: VCC prior.
6	VBUS_EN	Enabling VBUS input. “1”: Enable / “0”: Disable.
5	VCC_EN	Enabling VCC input. “1”: Enable / “0”: Disable.
4	VSYS_PRIORITY	Disabling the input current limit for avoiding VSYS drop when VBAT is the dead-battery, VBAT is < VSYSREG_SET. “1”: Disable the input current limit / “0”: Enable the input current limit.
3	PPC_SUB_CAP[1]	Power source peak current sub-capability
2	PPC_SUB_CAP[0]	
1	PPC_CAP[1]	Power source peak current capability
0	PPC_CAP[0]	

PPC_CAP	PPC_SUB_CAP	Overload Capabilities Description
00b	*b	Peak current equals (IBUS_LIM_SET or ICC_LIM_SET) .
01b	00b	Peak current equals 150.0% (IBUS_LIM_SET or ICC_LIM_SET) for 1ms. Low current equals 97.0% (IBUS_LIM_SET or ICC_LIM_SET) for 19ms.
	01b	Peak current equals 125.0% (IBUS_LIM_SET or ICC_LIM_SET) for 2ms. Low current equals 97.0% (IBUS_LIM_SET or ICC_LIM_SET) for 18ms.
	10b	Peak current equals 110.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms. Low current equals 90.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms.
10b	00b	Peak current equals 200.0% (IBUS_LIM_SET or ICC_LIM_SET) for 1ms. Low current equals 95.0% (IBUS_LIM_SET or ICC_LIM_SET) for 19ms.
	01b	Peak current equals 150.0% (IBUS_LIM_SET or ICC_LIM_SET) for 2ms. Low current equals 94.0% (IBUS_LIM_SET or ICC_LIM_SET) for 18ms.
	10b	Peak current equals 125.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms. Low current equals 75.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms.
11b	00b	Peak current equals 200.0% (IBUS_LIM_SET or ICC_LIM_SET) for 1ms. Low current equals 95.0% (IBUS_LIM_SET or ICC_LIM_SET) for 19ms.
	01b	Peak current equals 175.0% (IBUS_LIM_SET or ICC_LIM_SET) for 2ms. Low current equals 92.0% (IBUS_LIM_SET or ICC_LIM_SET) for 18ms.
	10b	Peak current equals 150.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms. Low current equals 50.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms.

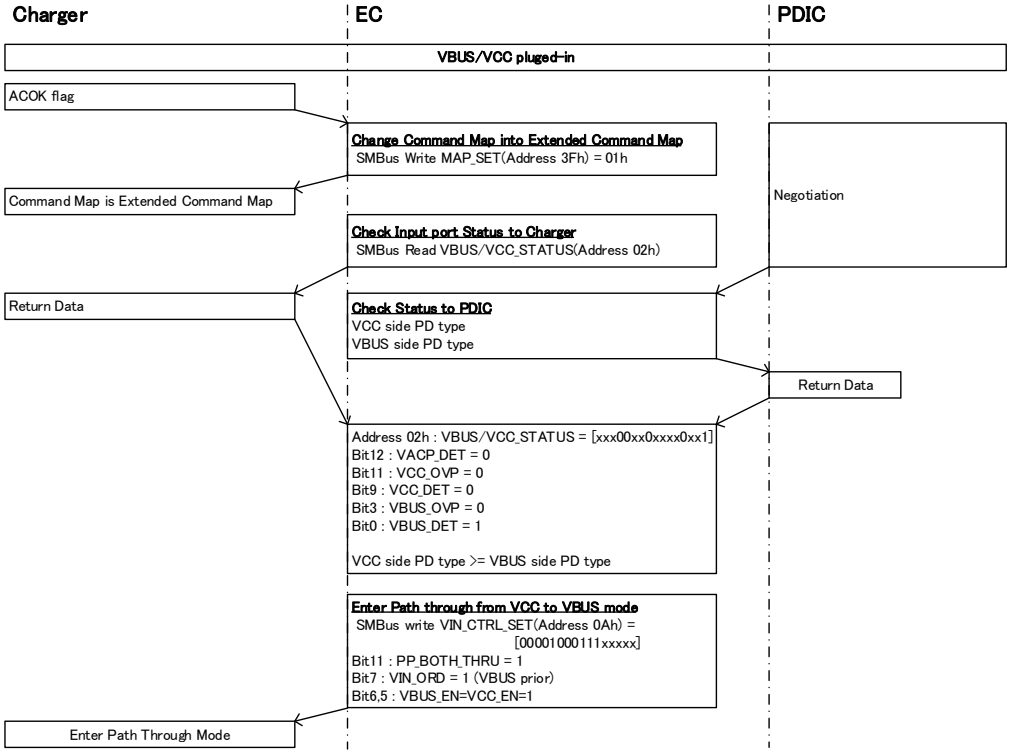
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Power Path Controll Flow chart
Path through mode : ON

✧ Power supply from VCC to VBUS

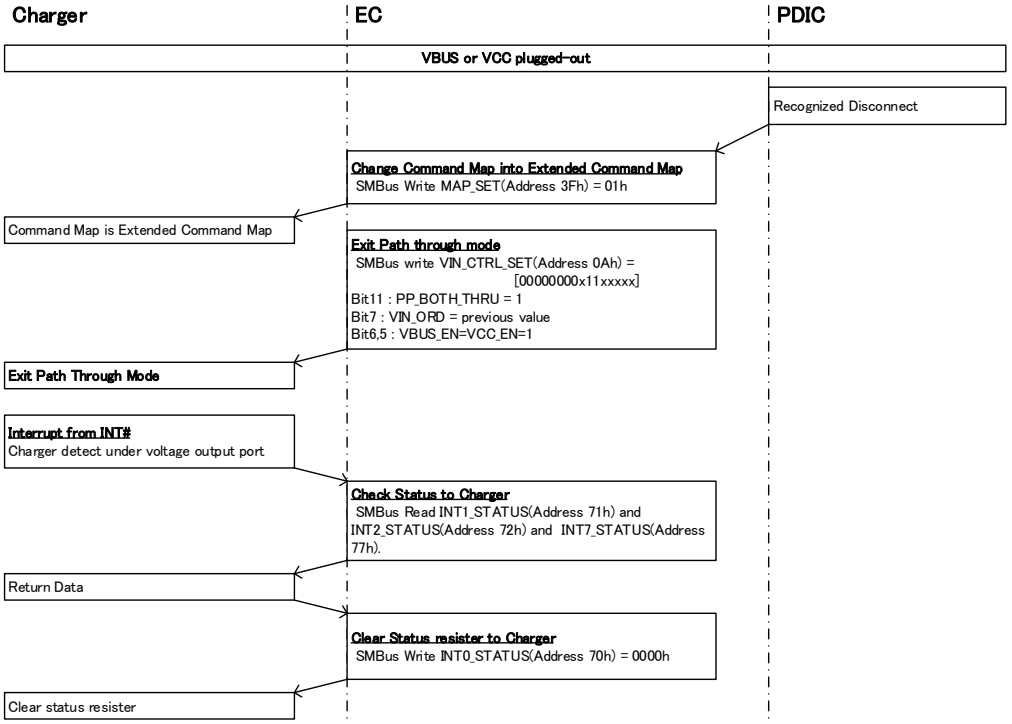


✧ Power supply from VBUS to VCC

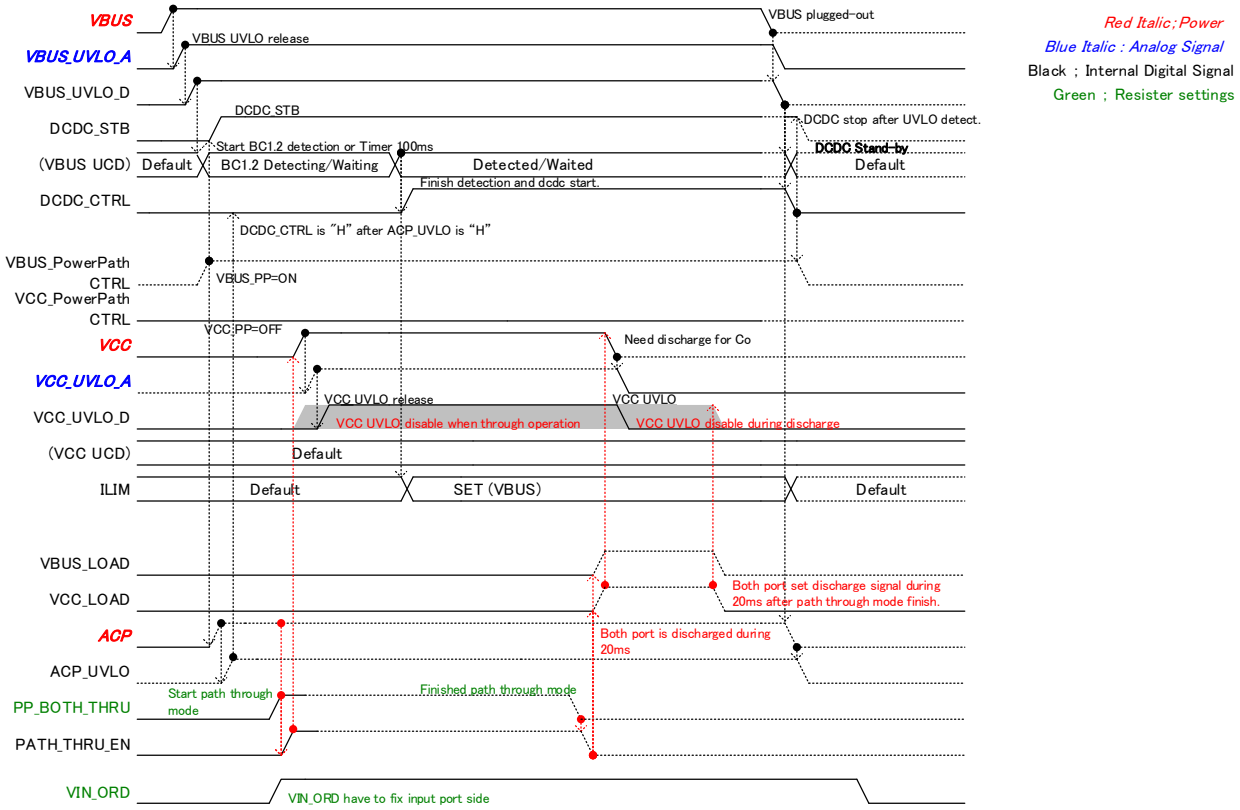


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Path through mode : OFF



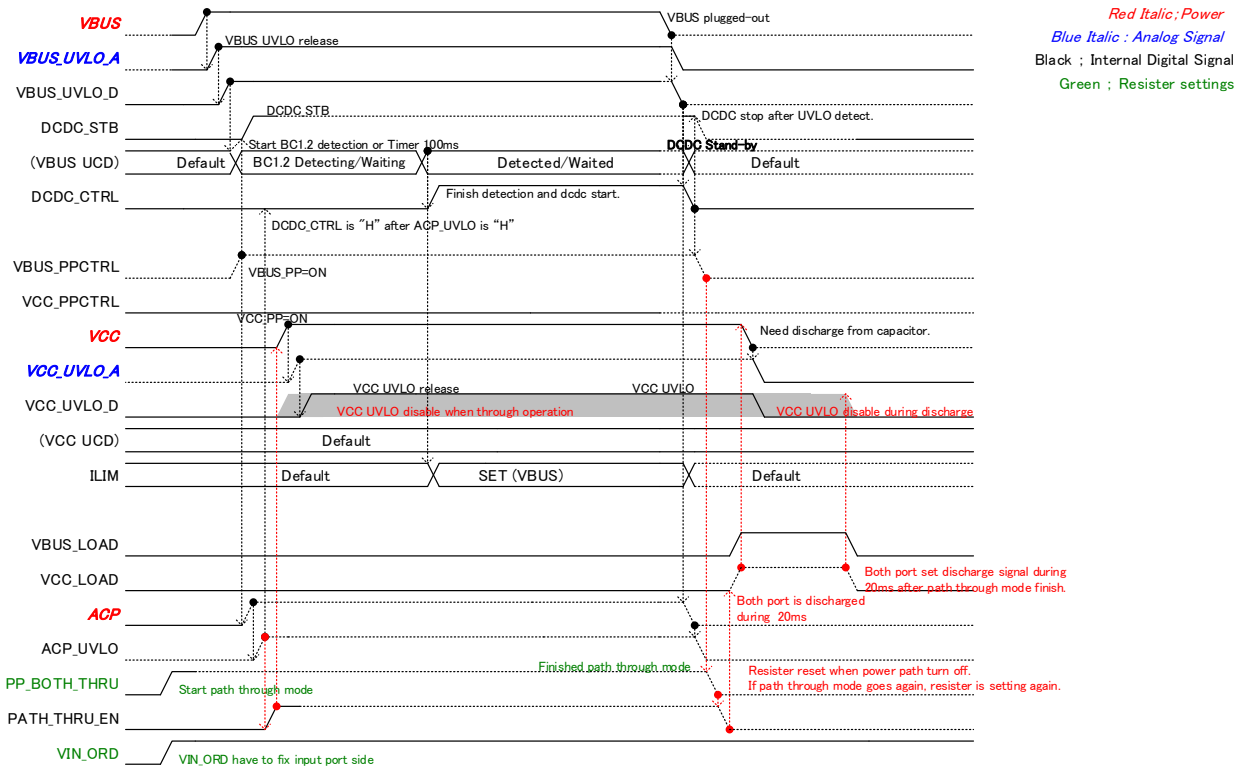
✧ Timing Chart
Path Through mode after VBUS input



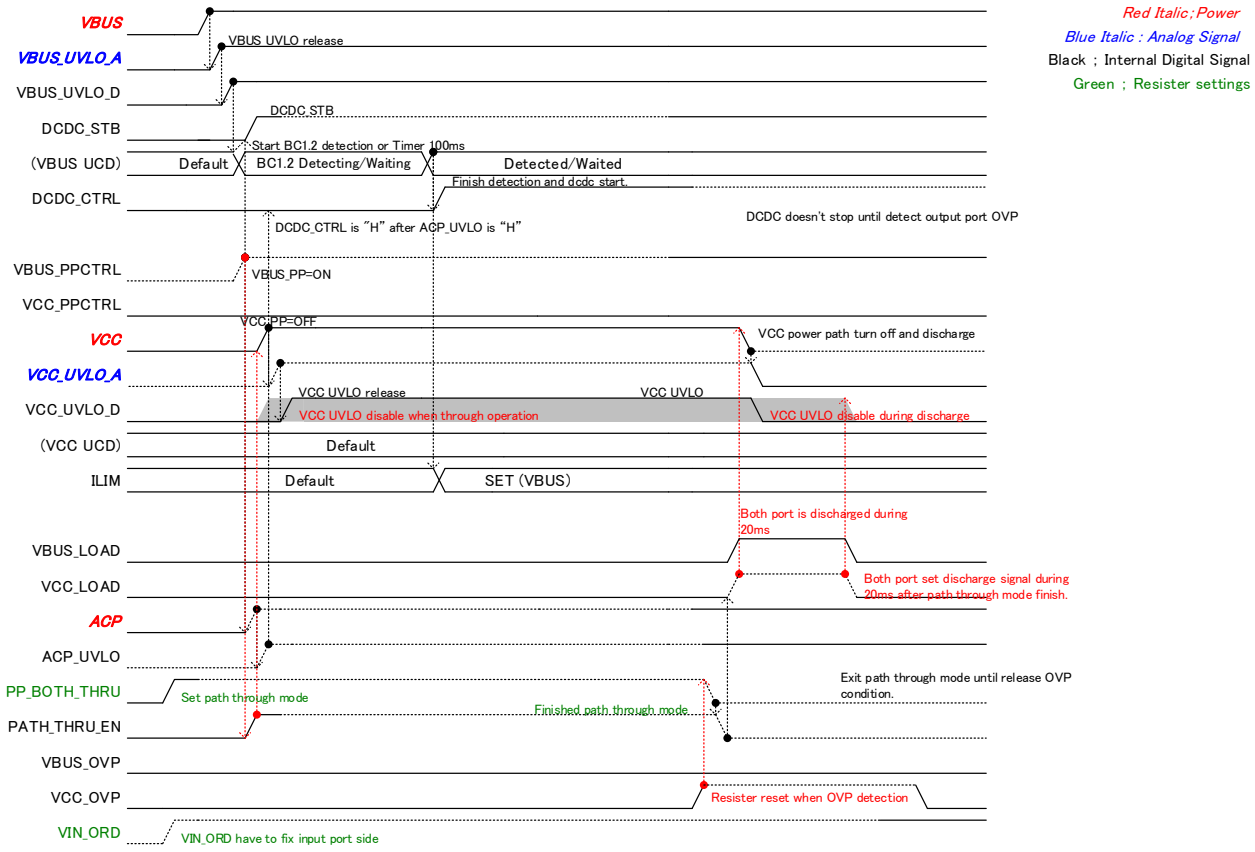
Red Italic ; Power
Blue Italic : Analog Signal
Black ; Internal Digital Signal
Green ; Resister settings

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VBUS path through mode after resister setting

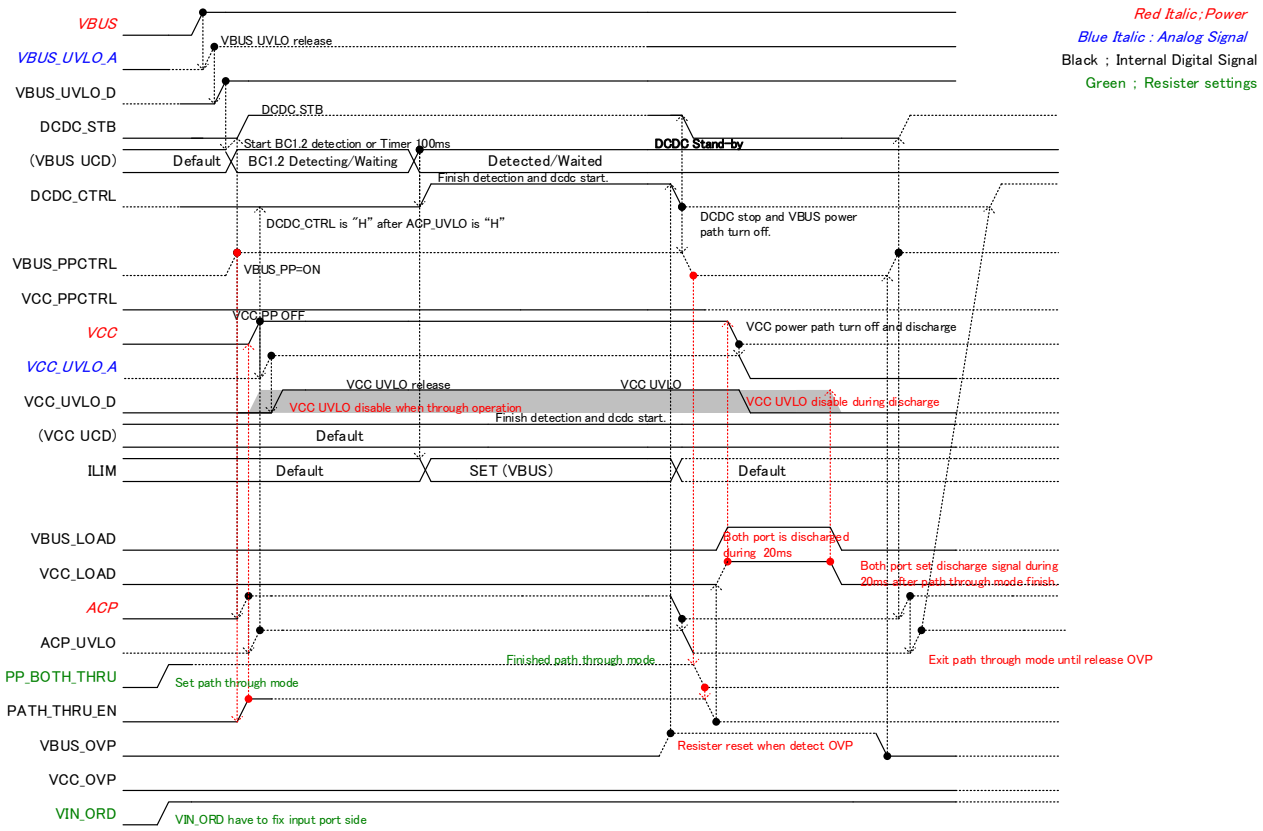


Detect OVP at Output port

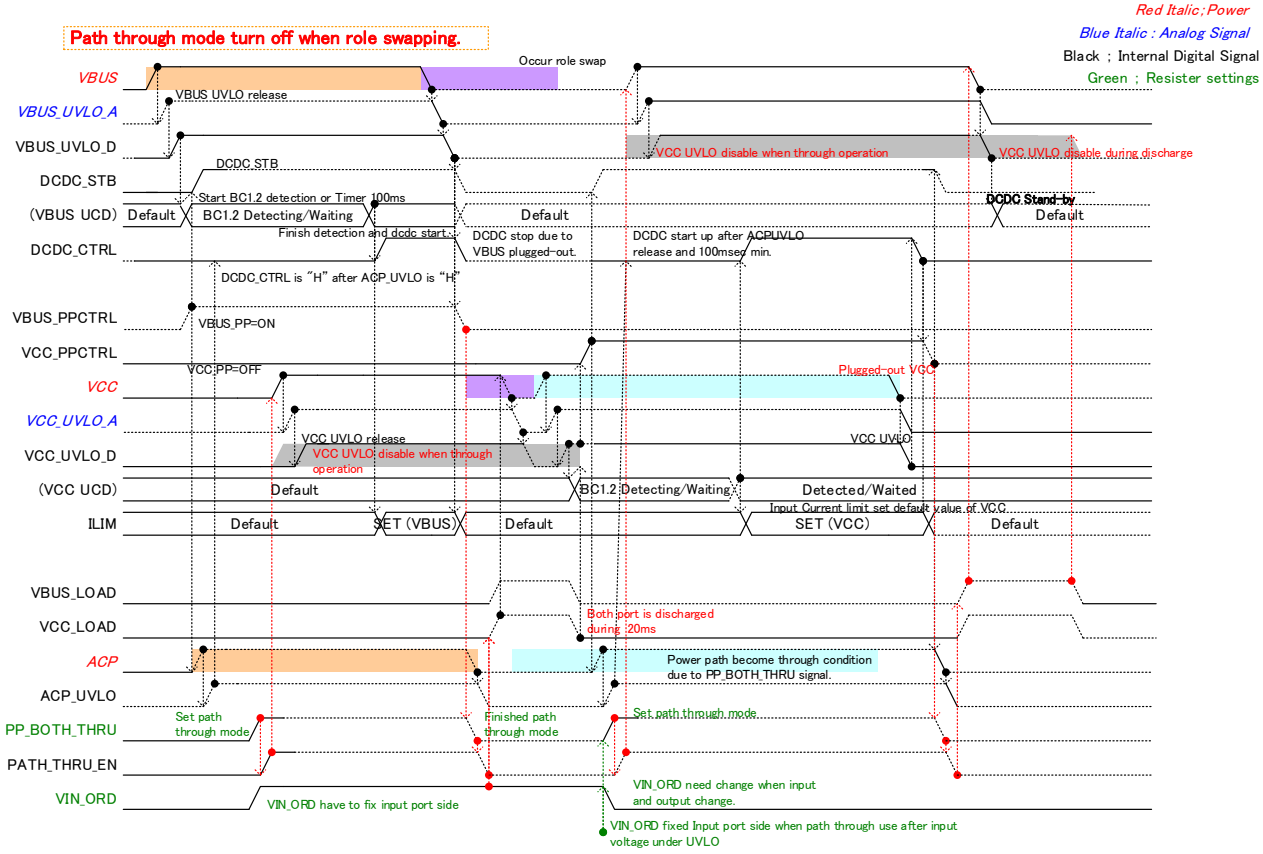


Detect OVP at Input port

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Role swap from VBUS to VCC when path through mode



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8.5.12. CHGOP_SET1

Charger Operation Control Setting 1

Command Code: 0Bh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	DCP_2500_SEL	Select current limitation when DCP charger attached.
14	SDP_500_SEL	Select current limitation when SDP charger attached.
13	ILIM_AUTO_DISEN	Disable automatic limitation of the input current. “1”: Disable / “0”: Enable.
12	reserved	
11	VCC_BC_DISEN	Disable charging trigger by BC1.2 detection. If this bit is "1: disable", after 100ms when VBUS/VCC plugged in, BD99954 starts charging without BC1.2 detection. “1”: Disable / “0”: Enable.
10	VBUS_BC_DISEN	Disable charging trigger by BC1.2 detection. If this bit is "1: disable", after 100ms when VBUS/VCC plugged in, BD99954 starts charging without BC1.2 detection. “1”: Disable / “0”: Enable.
9	SDP_CHG_TRIG_EN	Enable the charging trigger after SDP charger attached. “1”: Enable SDP_CHG_TRIG bit as charging trigger / “0”: Disable SDP_CHG_TRIG bit as charging trigger.
8	SDP_CHG_TRIG	Charging trigger after SDP charger attached. “1”: Start charging / “0”: Not start charging.
7	reserved	
6	AUTO_TOF	Top-off transition mode. This bit is trigger to move to the top-off charge state. This bit is only effective when the charging state transitions from fast-charge to top-off charge. “1”: Auto control / “0”: Manual control.
5	AUTO_FST	Fast charging transition mode. This bit is only effective when the charging state transitions from pre-charge to fast-charge. “1”: Auto control / “0”: Manual control.
4	reserved	
3	AUTO_RECH	Automatic re-charging mode. “1”: Auto control / “0”: Manual control.
2	reserved	
1	reserved	
0	reserved	

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8.5.13. CHGOP_SET2

Charger Operation Control Setting 2

Command Code: 0Ch
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	ILIM_RESET_EN	Enabling the input current limit re-setting when starting fast charge. “1”: Enable. / “0”: Disable.
13	DCDC_1MS_SEL[1]	Select ILIM re-setting step period. 00b: 10us/ 01b: 50us/ 10b: 100us/ 11b: 1ms
12	DCDC_1MS_SEL[0]	
11	reserved	
10	SEL_ILIM_DIV	Select ILIM drop width when Anti-collapse. or VBAT<VIN comparator asserted. “1”: The input current limit drop into 1/4. / “0”: 1/2.
9	reserved	
8	BATT_LEARN	Enabling Battery Learning operation, suspend charging and DC/DC convertor. This bit is cleared automatically when VBAT is the dead battery, VBAT < VSYSREG_SET. “1”: Enable / “0”: Disable.
7	CHG_EN	Enabling Charger operation. “1”: Enable / “0”: Disable.
6	USB_SUS	Suspend USB charging and DC/DC convertor. “1”: Suspend / “0”: Active.
5	CHOP_SS_INIT	Initialization value for CHOP_SS (Chopper Mode during DCDC soft start.) "1": Chopper Mode during DCDC soft start / "0": Synchronized Mode. This register is "Read-Only" and is loaded from OTP.
4	CHOP_ALL_INIT	Initialization value for CHOP_ALL (Continuous Chopper Mode.) "1": Always in Chopper Mode / "0": Synchronized Mode. This register is "Read-Only" and is loaded from OTP.
3	DCDC_CLK_SEL[1]	DCDC Clock Select. 00b: 600kHz (H:L=1:1)/ 01b: 857kHz (H:L=3:4)/ 10b: 1000kHz (H:L=1:2)/ 11b: 1200kHz (H:L=2:3)
2	DCDC_CLK_SEL[0]	
1	CHOP_SS	Enable operation in Chopper Mode during DCDC soft start. "1": Chopper Mode during DCDC soft start / "0": Synchronized Mode. Initial value is loaded from CHOP_SS_INIT during DCDC standby.
0	CHOP_ALL	Force continuous Chopper Mode operation. "1": Continuous Chopper Mode / "0" Synchronized Mode. Initial value is loaded from CHOP_ALL_INIT during DCDC standby.

8.5.14. VBUSCLPS_TH_SET

VBUS Collapse Detect Threshold Voltage Setting

Command Code: 0Dh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VBUSCLPS_TH_SET[14]	VBUS Anti-collapse entry voltage threshold. 3,840 to 32,640mV, 128mV steps. The register range : 0 to 32,640mV. But the actual range : 3,840 to 25,088mV. “00h”setting disables VBUS collapse detection.
13	VBUSCLPS_TH_SET[13]	
12	VBUSCLPS_TH_SET[12]	
11	VBUSCLPS_TH_SET[11]	
10	VBUSCLPS_TH_SET[10]	
9	VBUSCLPS_TH_SET[9]	
8	VBUSCLPS_TH_SET[8]	
7	VBUSCLPS_TH_SET[7]	
6	reserved	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.5.15. VCCCLPS_TH_SET

VCC Collapse Detect Threshold Voltage Setting

Command Code: 0Eh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VCCCLPS_TH_SET[14]	VCC Anti-collapse entry voltage threshold 3,840 to 32,640mV, 128mV steps. The register range : 0 to 32,640mV. But the actual range : 3,840 to 25,088mV. “00h”setting disables VCC collapse detection.
13	VCCCLPS_TH_SET[13]	
12	VCCCLPS_TH_SET[12]	
11	VCCCLPS_TH_SET[11]	
10	VCCCLPS_TH_SET[10]	
9	VCCCLPS_TH_SET[9]	
8	VCCCLPS_TH_SET[8]	
7	VCCCLPS_TH_SET[7]	
6	reserved	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.16. CHGWDT_SET

Charger WDT Setting

Command Code: 0Fh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	WDT_FST[7]	Watch Dog Timer setting for Fast Charging. 4 to 1020 minutes range, 4-minute steps. “00h”setting stops this timer.
14	WDT_FST[6]	
13	WDT_FST[5]	
12	WDT_FST[4]	
11	WDT_FST[3]	
10	WDT_FST[2]	
9	WDT_FST[1]	
8	WDT_FST[0]	
7	WDT_PRE[7]	Watch Dog Timer setting for Pre-charging. 1 to 255 minutes range, 1-minute steps. “00h”setting stops this timer.
6	WDT_PRE[6]	
5	WDT_PRE[5]	
4	WDT_PRE[4]	
3	WDT_PRE[3]	
2	WDT_PRE[2]	
1	WDT_PRE[1]	
0	WDT_PRE[0]	

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8.5.17. BATTWDT_SET

Battery Temperature and Battery short current WDT Setting

Command Code: 10h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	WDT_IBAT_SHORT[7]	Watch Dog Timer setting for Battery Short Current. 4 to 1020 ms range, 4ms steps. “00h”setting stops this timer.
14	WDT_IBAT_SHORT[6]	
13	WDT_IBAT_SHORT[5]	
12	WDT_IBAT_SHORT[4]	
11	WDT_IBAT_SHORT[3]	
10	WDT_IBAT_SHORT[2]	
9	WDT_IBAT_SHORT[1]	
8	WDT_IBAT_SHORT[0]	
7	WDT_THERM[7]	Watch Dog Timer setting for Battery Temperature. 1 to 255 minutes range, 1-minute steps. “00h”setting stops this timer.
6	WDT_THERM[6]	
5	WDT_THERM[5]	
4	WDT_THERM[4]	
3	WDT_THERM[3]	
2	WDT_THERM[2]	
1	WDT_THERM[1]	
0	WDT_THERM[0]	

8.5.18. VSYSREG_SET

VSYS Regulation Setting

Command Code: 11h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VSYSREG_SET[14]	VSYS regulation voltage setting and threshold voltage from Pre-charging to Fast-charging. 2,560 to 19,200mV, 64mV steps. The register range : 0 to 32,704mV. But the actual range : 2,560 to 19,200mV.
13	VSYSREG_SET[13]	
12	VSYSREG_SET[12]	
11	VSYSREG_SET[11]	
10	VSYSREG_SET[10]	
9	VSYSREG_SET[9]	
8	VSYSREG_SET[8]	
7	VSYSREG_SET[7]	
6	VSYSREG_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.5.19. VSYSVAL_THH_SET

VSYS Valid Threshold High Setting (Hysteresis)

Command Code: 12h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VSYSVAL_THH_SET[14]	VSYS voltage rising detection threshold with hysteresis. 2,560 to 19,200mV, 64mV steps. The register range : 0 to 32,704mV. But the actual range : 2,560 to 19,200mV.
13	VSYSVAL_THH_SET[13]	
12	VSYSVAL_THH_SET[12]	
11	VSYSVAL_THH_SET[11]	
10	VSYSVAL_THH_SET[10]	
9	VSYSVAL_THH_SET[9]	
8	VSYSVAL_THH_SET[8]	
7	VSYSVAL_THH_SET[7]	
6	VSYSVAL_THH_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.20. VSYSVAL_THL_SET

VSYS Valid Threshold Low Setting (Hysteresis)

Command Code: 13h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VSYSVAL_THL_SET[14]	VSYS voltage falling detection threshold with hysteresis. 2,560 to 19,200mV, 64mV steps. The register range : 0 to 32,704mV. But the actual range : 2,560 to 19,200mV.
13	VSYSVAL_THL_SET[13]	
12	VSYSVAL_THL_SET[12]	
11	VSYSVAL_THL_SET[11]	
10	VSYSVAL_THL_SET[10]	
9	VSYSVAL_THL_SET[9]	
8	VSYSVAL_THL_SET[8]	
7	VSYSVAL_THL_SET[7]	
6	VSYSVAL_THL_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.5.21. ITRICH_SET

Trickle-charge Current Setting

Command Code: 14h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	ITRICH_SET[10]	Trickle-charging current setting. 0 to 1,024mA, 64mA steps. The register range : 0 to 1,984mA. But the actual range : 0 to 1,024mA.
9	ITRICH_SET[9]	
8	ITRICH_SET[8]	
7	ITRICH_SET[7]	
6	ITRICH_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.22. IPRECH_SET

Pre-charge Current Setting

Command Code: 15h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	IPRECH_SET[10]	Pre-charging current setting. 0 to 1,024mA, 64mA steps. The register range : 0 to 1,984mA. But the actual range : 0 to 1,024mA.
9	IPRECH_SET[9]	
8	IPRECH_SET[8]	
7	IPRECH_SET[7]	
6	IPRECH_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.5.23. ICHG_SET

Fast-charge Current Setting

Command Code: 16h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	ICHG_SET[13]	Fast-charging current setting. 0 to 16,320mA, 64mA steps.
12	ICHG_SET[12]	
11	ICHG_SET[11]	
10	ICHG_SET[10]	
9	ICHG_SET[9]	
8	ICHG_SET[8]	
7	ICHG_SET[7]	
6	ICHG_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.24. ITERM_SET

Charge Termination Current Setting

Command Code: 17h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	ITERM_SET[10]	Charging Termination Current. 0 to 1,024mA, 64mA steps. The register range : 0 to 1,984mA. But the actual range : 0 to 1,024mA.
9	ITERM_SET[9]	
8	ITERM_SET[8]	
7	ITERM_SET[7]	
6	ITERM_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.5.25. VPRECHG_TH_SET

Pre-charge Voltage Threshold Setting

Command Code: 18h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VPRECHG_TH_SET[14]	Threshold voltage from Trickle-charging to Pre-charging 2,048 to 19,200mV, 64mV steps. The register range : 0 to 32,704mV. But the actual range : 2,048 to 19,200mV.
13	VPRECHG_TH_SET[13]	
12	VPRECHG_TH_SET[12]	
11	VPRECHG_TH_SET[11]	
10	VPRECHG_TH_SET[10]	
9	VPRECHG_TH_SET[9]	
8	VPRECHG_TH_SET[8]	
7	VPRECHG_TH_SET[7]	
6	VPRECHG_TH_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.26. VRBOOST_SET

Reverse buck boost voltage Setting

Command Code: 19h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VRBOOST_SET[14]	Reverse buck boost voltage setting. 4,032 to 22,016mV, 64mV steps. The register range : 0 to 32,704mV. But the actual range : 4,032 to 22,016mV.
13	VRBOOST_SET[13]	
12	VRBOOST_SET[12]	
11	VRBOOST_SET[11]	
10	VRBOOST_SET[10]	
9	VRBOOST_SET[9]	
8	VRBOOST_SET[8]	
7	VRBOOST_SET[7]	
6	VRBOOST_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.5.27. VFASTCHG_REG_SET1

Fast Charge Voltage Regulation Setting 1

Command Code: 1Ah
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VFASTCHG_REG_SET1[14]	Fast Charging Regulation Voltage. 2,560 to 19,200mV, 16mV steps. The register range : 0 to 32,752mV. But the actual range : 2,560 to 19,200mV.
13	VFASTCHG_REG_SET1[13]	
12	VFASTCHG_REG_SET1[12]	
11	VFASTCHG_REG_SET1[11]	
10	VFASTCHG_REG_SET1[10]	
9	VFASTCHG_REG_SET1[9]	
8	VFASTCHG_REG_SET1[8]	
7	VFASTCHG_REG_SET1[7]	
6	VFASTCHG_REG_SET1[6]	
5	VFASTCHG_REG_SET1[5]	
4	VFASTCHG_REG_SET1[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.28. VFASTCHG_REG_SET2

Fast Charge Voltage Regulation Setting 2 (Hot 1)

Command Code: 1Bh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VFASTCHG_REG_SET2[14]	Fast Charging Regulation Voltage for the JEITA temperature range T3-T5. 2,560 to 19,200mV, 16mV steps. The register range : 0 to 32,752mV. But the actual range : 2,560 to 19,200mV.
13	VFASTCHG_REG_SET2[13]	
12	VFASTCHG_REG_SET2[12]	
11	VFASTCHG_REG_SET2[11]	
10	VFASTCHG_REG_SET2[10]	
9	VFASTCHG_REG_SET2[9]	
8	VFASTCHG_REG_SET2[8]	
7	VFASTCHG_REG_SET2[7]	
6	VFASTCHG_REG_SET2[6]	
5	VFASTCHG_REG_SET2[5]	
4	VFASTCHG_REG_SET2[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.5.29. VFASTCHG_REG_SET3

Fast Charge Voltage Regulation Setting 3 (Hot 2)

Command Code: 1Ch
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VFASTCHG_REG_SET3[14]	Fast Charging Regulation Voltage for the JEITA temperature range T5-T4 and T1-T2. 2,560 to 19,200mV, 16mV steps. The register range : 0 to 32,752mV. But the actual range : 2,560 to 19,200mV.
13	VFASTCHG_REG_SET3[13]	
12	VFASTCHG_REG_SET3[12]	
11	VFASTCHG_REG_SET3[11]	
10	VFASTCHG_REG_SET3[10]	
9	VFASTCHG_REG_SET3[9]	
8	VFASTCHG_REG_SET3[8]	
7	VFASTCHG_REG_SET3[7]	
6	VFASTCHG_REG_SET3[6]	
5	VFASTCHG_REG_SET3[5]	
4	VFASTCHG_REG_SET3[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.30. VRECHG_SET

Re-charge Battery Voltage Setting

Command Code: 1Dh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VRECHG_SET[14]	Re-charge Battery Voltage. 2,560 to 19,200mV, 16mV steps. The register range : 0 to 32,752mV. But the actual range : 2,560 to 19,200mV.
13	VRECHG_SET[13]	
12	VRECHG_SET[12]	
11	VRECHG_SET[11]	
10	VRECHG_SET[10]	
9	VRECHG_SET[9]	
8	VRECHG_SET[8]	
7	VRECHG_SET[7]	
6	VRECHG_SET[6]	
5	VRECHG_SET[5]	
4	VRECHG_SET[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

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8.5.31. VBATOVP_SET

Battery Over Voltage Protection Setting

Command Code: 1Eh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VBATOVP_SET[14]	Battery over-voltage detection threshold. 2,560 to 19,200mV, 16mV steps. The register range : 0 to 32,752mV. But the actual range : 2,560 to 19,200mV.
13	VBATOVP_SET[13]	
12	VBATOVP_SET[12]	
11	VBATOVP_SET[11]	
10	VBATOVP_SET[10]	
9	VBATOVP_SET[9]	
8	VBATOVP_SET[8]	
7	VBATOVP_SET[7]	
6	VBATOVP_SET[6]	
5	VBATOVP_SET[5]	
4	VBATOVP_SET[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.32. IBATSHORT_SET

Battery Short Current Protection Setting

Command Code: 1Fh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	IBATM_SHORT_SET[14]	Battery Short Current Protection Threshold 0 to 25,000mA, 1mA steps. The register range : 0 to 32,752mA. But the actual range : 0 to 25,000mA.
13	IBATM_SHORT_SET[13]	
12	IBATM_SHORT_SET[12]	
11	IBATM_SHORT_SET[11]	
10	IBATM_SHORT_SET[10]	
9	IBATM_SHORT_SET[9]	
8	IBATM_SHORT_SET[8]	
7	IBATM_SHORT_SET[7]	
6	IBATM_SHORT_SET[6]	
5	IBATM_SHORT_SET[5]	
4	IBATM_SHORT_SET[4]	
3	IBATM_SHORT_SET[3]	
2	IBATM_SHORT_SET[2]	
1	IBATM_SHORT_SET[1]	
0	IBATM_SHORT_SET[0]	

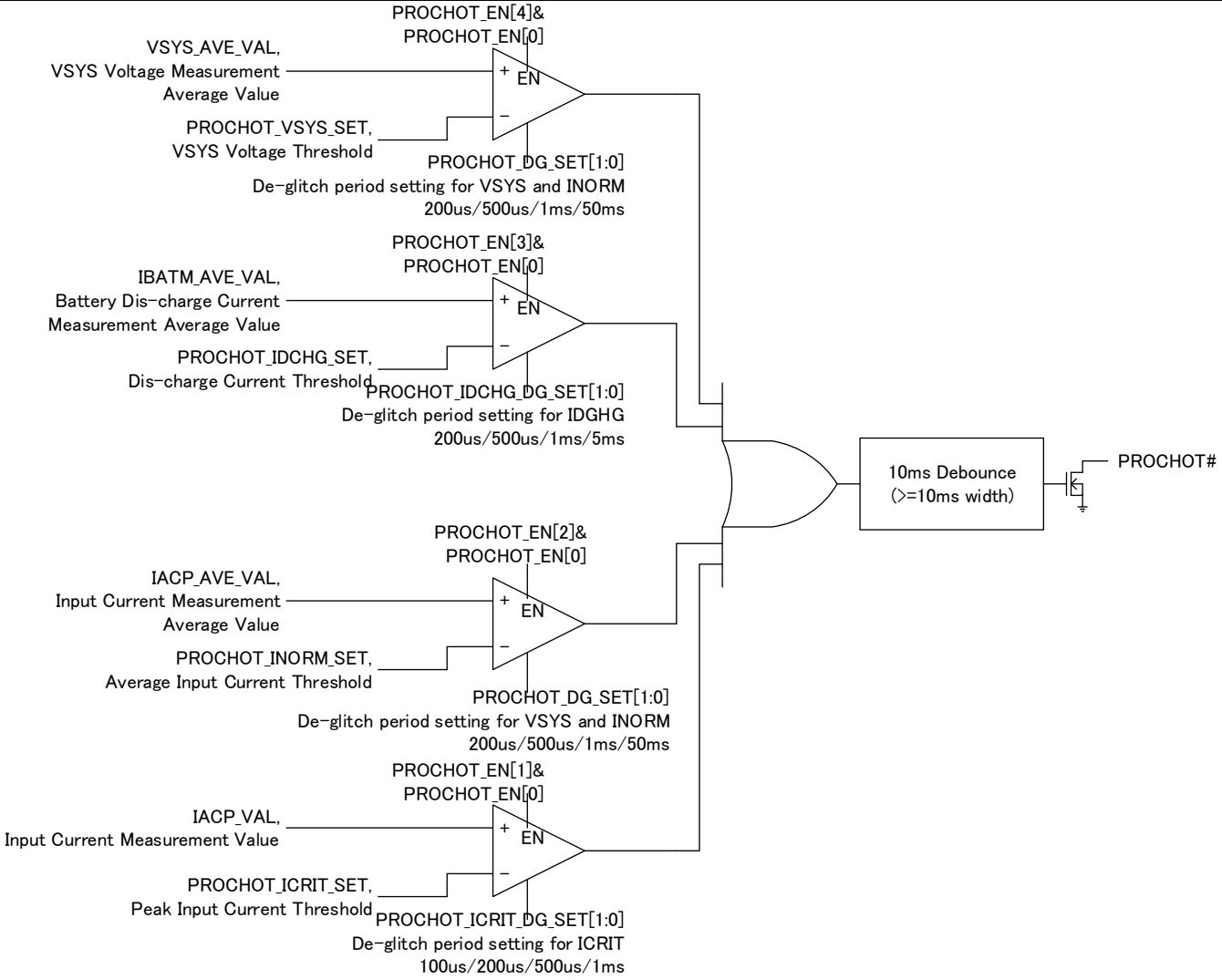
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8.5.33. PROCHOT_CTRL_SET

PROCHOT# pin Control Setting

Command Code: 20h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	PROCHOT_DG_SET[1]	PROCHOT# de-glitch period (VSYS, INORM) setting.
14	PROCHOT_DG_SET[0]	00b: 200us/ 01b: 500us/ 10b:1ms/ 11b:50ms
13	reserved	
12	reserved	
11	PROCHOT_ICRIT_DG_SET[1]	PROCHOT# de-glitch period (ICRIT) setting.
10	PROCHOT_ICRIT_DG_SET[0]	00b: 100us/ 01b: 200us/ 10b: 500us/ 11b:1ms
9	PROCHOT_IDCHG_DG_SET[1]	PROCHOT# de-glitch period (IDCHG) setting.
8	PROCHOT_IDCHG_DG_SET[0]	00b: 200us/ 01b: 500us/ 10b:1ms/ 11b:5ms
7	reserved	
6	reserved	
5	reserved	
4	PROCHOT_EN[4]	PROCHOT# 2nd level enable (VSYS)
3	PROCHOT_EN[3]	PROCHOT# 2nd level enable (IDCHG)
2	PROCHOT_EN[2]	PROCHOT# 2nd level enable (INORM)
1	PROCHOT_EN[1]	PROCHOT# 2nd level enable (ICRIT)
0	PROCHOT_EN[0]	PROCHOT# 1st level enable



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8.5.34. PROCHOT_ICRIT_SET

Peak Input Current Threshold Setting for PROCHOT#

Command Code: 21h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	PROCHOT_ICRIT_SET[14]	Peak Input Current Threshold for PROCHOT# 0 to 16,384mA, 1mA steps. The register range : 0 to 32,752mA. But the actual range : 0 to 16,383mA.
13	PROCHOT_ICRIT_SET[13]	
12	PROCHOT_ICRIT_SET[12]	
11	PROCHOT_ICRIT_SET[11]	
10	PROCHOT_ICRIT_SET[10]	
9	PROCHOT_ICRIT_SET[9]	
8	PROCHOT_ICRIT_SET[8]	
7	PROCHOT_ICRIT_SET[7]	
6	PROCHOT_ICRIT_SET[6]	
5	PROCHOT_ICRIT_SET[5]	
4	PROCHOT_ICRIT_SET[4]	
3	PROCHOT_ICRIT_SET[3]	
2	PROCHOT_ICRIT_SET[2]	
1	PROCHOT_ICRIT_SET[1]	
0	PROCHOT_ICRIT_SET[0]	

8.5.35. PROCHOT_INORM_SET

Average Input Current Threshold Setting for PROCHOT#

Command Code: 22h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	PROCHOT_INORM_SET[14]	Average Input Current Threshold for PROCHOT# 0 to 16,384mA, 1mA steps. The register range : 0 to 32,752mA. But the actual range : 0 to 16,383mA.
13	PROCHOT_INORM_SET[13]	
12	PROCHOT_INORM_SET[12]	
11	PROCHOT_INORM_SET[11]	
10	PROCHOT_INORM_SET[10]	
9	PROCHOT_INORM_SET[9]	
8	PROCHOT_INORM_SET[8]	
7	PROCHOT_INORM_SET[7]	
6	PROCHOT_INORM_SET[6]	
5	PROCHOT_INORM_SET[5]	
4	PROCHOT_INORM_SET[4]	
3	PROCHOT_INORM_SET[3]	
2	PROCHOT_INORM_SET[2]	
1	PROCHOT_INORM_SET[1]	
0	PROCHOT_INORM_SET[0]	

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8.5.36. PROCHOT_IDCHG_SET

Dis-charge Current Threshold Setting for PROCHOT#

Command Code: 23h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	PROCHOT_IDCHG_SET[13]	Dis-charge Current Threshold for PROCHOT#
13	PROCHOT_IDCHG_SET[14]	0 to 25,000mA, 1mA steps.
12	PROCHOT_IDCHG_SET[12]	The register range: 0 to 32,752mA.
11	PROCHOT_IDCHG_SET[11]	But the actual range: 0 to 25,000mA.
10	PROCHOT_IDCHG_SET[10]	
9	PROCHOT_IDCHG_SET[9]	
8	PROCHOT_IDCHG_SET[8]	
7	PROCHOT_IDCHG_SET[7]	
6	PROCHOT_IDCHG_SET[6]	
5	PROCHOT_IDCHG_SET[5]	
4	PROCHOT_IDCHG_SET[4]	
3	PROCHOT_IDCHG_SET[3]	
2	PROCHOT_IDCHG_SET[2]	
1	PROCHOT_IDCHG_SET[1]	
0	PROCHOT_IDCHG_SET[0]	

8.5.37. PROCHOT_VSYS_SET

VSYS Voltage Threshold Setting for PROCHOT#

Command Code: 24h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	PROCHOT_VSYS_SET[14]	VSYS Voltage Threshold for PROCHOT#
13	PROCHOT_VSYS_SET[13]	0 to 19,200mV, 1mV steps.
12	PROCHOT_VSYS_SET[12]	The register range : 0 to 32,752mV.
11	PROCHOT_VSYS_SET[11]	But the actual range : 0 to 19,200mV.
10	PROCHOT_VSYS_SET[10]	
9	PROCHOT_VSYS_SET[9]	
8	PROCHOT_VSYS_SET[8]	
7	PROCHOT_VSYS_SET[7]	
6	PROCHOT_VSYS_SET[6]	
5	PROCHOT_VSYS_SET[5]	
4	PROCHOT_VSYS_SET[4]	
3	PROCHOT_VSYS_SET[3]	
2	PROCHOT_VSYS_SET[2]	
1	PROCHOT_VSYS_SET[1]	
0	PROCHOT_VSYS_SET[0]	

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8.5.38. PMON_IOUT_CTRL_SET

PMON and IOUT Output Control Setting

Command Code: 25h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	IMON_INSEL	IOUT Input source select. 0b: Measurement Average Value/ 1b: Measurement Value
8	PMON_INSEL	PMON Input source select. 0b: Measurement Average Value/ 1b: Measurement Value
7	IOUT_OUT_EN	IOUT enable. “1”: Enable / “0”: Disable.
6	IOUT_SOURCE_SEL	IOUT source select. “1”: Input Current / “0”: Battery Dis-charge Current.
5	IOUT_GAIN_SET[1]	IOUT gain select. 00b: 5V/V / 01b: 10V/V / 10b: 20V/V/ 11b: 40V/V
4	IOUT_GAIN_SET[0]	
3	PMON_OUT_EN	PMON Enable. “1”: Enable / “0”: Disable.
2	PMON_GAIN_SET[2]	PMON gain select. 0h: x1/ 1h: x2/ 2h: x4/ 3h: x8/ 4h: x16/ 5h: x32/ 6h: x64
1	PMON_GAIN_SET[1]	
0	PMON_GAIN_SET[0]	

8.5.39. PMON_DACIN_VAL

PMON DAC Input Value (for debug and production test)

Command Code: 26h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	PMON_DACIN_VAL[9]	PMON DAC Input Value (for debug and production test)
8	PMON_DACIN_VAL[8]	
7	PMON_DACIN_VAL[7]	
6	PMON_DACIN_VAL[6]	
5	PMON_DACIN_VAL[5]	
4	PMON_DACIN_VAL[4]	
3	PMON_DACIN_VAL[3]	
2	PMON_DACIN_VAL[2]	
1	PMON_DACIN_VAL[1]	
0	PMON_DACIN_VAL[0]	

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8.5.40. IOUT_DACIN_VAL

IOUT DAC Input Value (for debug and production test)

Command Code: 27h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	IOUT_DACIN_VAL[11]	IOUT DAC Input Value (for debug and production test)
10	IOUT_DACIN_VAL[10]	
9	IOUT_DACIN_VAL[9]	
8	IOUT_DACIN_VAL[8]	
7	IOUT_DACIN_VAL[7]	
6	IOUT_DACIN_VAL[6]	
5	IOUT_DACIN_VAL[5]	
4	IOUT_DACIN_VAL[4]	
3	IOUT_DACIN_VAL[3]	
2	IOUT_DACIN_VAL[2]	
1	IOUT_DACIN_VAL[1]	
0	IOUT_DACIN_VAL[0]	

8.5.41. VCC_UCD_SET

BC1.2 Charger Detector on the VCC side Setting

Command Code: 28h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	BCSRETRY	Trigger for re-trial of the USB Charger Port detection. “1”: Start detection / “0”: Release the operation.
11	reserved	
10	reserved	
9	reserved	
8	ADCRTRY	Trigger for re-trial of USB ID Resistor detection. “1”: Start detection / “0”: Release the operation.
7	USBDETEN	Enabling USB Charger port detection. “1”: Enable / “0”: Disable.
6	IDRDETEN	Enabling USB ID Resistor detection. “1”: Enable / “0”: Disable.
5	ENUMRDY	Setting USB Enumeration to Ready. “1”: Skip Secondary Detection / “0”: Normal operation.
4	ADCPOLEN	USB ID input polling enable. “1”: Enable (always detection) / “0”: Disable.
3	DCDMODE	DCD timeout period setting. “1”: 1280 ms / “0”: 640 ms.
2	reserved	
1	USB_SW_EN	Enabling automatic USB-Switch control. “1”: Enable (auto) / “0”: Disable (manual).
0	USB_SW	USB Switch manual control. “1”: Switch ON / “0”: Switch OFF.

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8.5.42. VCC_UCD_STATUS

BC1.2 Charger Detect Status on the VCC side

Command Code: 29h
Bus Protocol: Read Word

Bit	Symbol	Description
15	DCDFAIL	DCD (USB Data Contact Detection) failed (timeout) status. “1”: Failed / “0”: Succeeded.
14	reserved	
13	CHGPORT[1]	USB Charger Port Detection result. 00b: No charger port/ 01b: SDP/ 10b: CDP/ 11b: DCP
12	CHGPORT[0]	
11	PUPDET	Pull-up detected at Primary Detection after DCDFAIL. “1”: Detected / “0”: Not detected.
10	reserved	
9	reserved	
8	reserved	
7	VBUS_VLD	USB VBUS valid voltage detection status. “1”: Valid / “0”: Not valid.
6	CHGDET	USB Charger Port detection status. “1”: Detected / “0”: Not detected.
5	reserved	
4	reserved	
3	OTGDET	USB OTG Device detection status. “1”: Detected / “0”: Not detected.
2	reserved	
1	reserved	
0	reserved	

	CHGDET	PUPDET	DCDFAIL	CHGPORT[1]	CHGPORT[0]
VBUS Open	0	0	0	0	0
SDP	0	0	0	0	1
CDP	1	0	0	1	0
DCP	1	0	0	1	1
Pull-up Port	0	1	1	0	1
Open Port	0	0	1	0	1
Unstable Port	0	0	1	0	1

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8.5.43. VCC_IDD_STATUS

ID Detect Status on the VCC side

Command Code: 2Ah
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	reserved	
6	VBINOP	VBUS voltage status while ID detection. “1”: Normal voltage / “0”: Abnormal voltage.
5	EXTID	Check MHL ID (1k Ohm) detection support. “1”: Supported / “0”: Not supported.
4	IDRDET	USB ID Resistor contact detection status. “1”: Detected (contacted) / “0”: Not detected (removed).
3	INDO[3]	USB ID detection result.
2	INDO[2]	
1	INDO[1]	
0	INDO[0]	

INDO	ID Resistance	Detected Port/Device
0h	0 - 10Ω	RID_GND (OTG)
1h	36.5kΩ	RID_C (ACA_C, SDP)
2h	47kΩ	-
3h	68kΩ	RID_B (ACA_B, DCP)
4h	102kΩ	-
5h	124kΩ	RID_A (ACA_A, CDP)
6h	180kΩ	-
7h	200kΩ	RID_FLOAT
8h	287kΩ	-
9h	390kΩ	-
Ah	440kΩ	-
Bh	557kΩ	-
Ch	797kΩ	-
Dh	>1MΩ	-
Eh	1KΩ	(MHL)
Fh	Illegal ID	Unknown

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8.5.44. VCC_UCD_FCTRL_SET

BC1.2 Charger Detector on the VCC side Manual Control Setting

Command Code: 2Bh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	UCDSWEN	In normal operation, please don't set these registers.
9	RREF_EN	
8	DPPU_EN	
7	DPREF_EN	
6	DMREF_EN	
5	DPDET_EN	
4	DMDET_EN	
3	DPSINK_EN	
2	DMSINK_EN	
1	DP_BUFF_EN	
0	DM_BUFF_EN	

8.5.45. VCC_UCD_FCTRL_EN

BC1.2 Charger Detector on the VCC side Manual Control Enable

Command Code: 2Ch
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	EXTCLKENBL	In normal operation, please don't set these registers.
14	PLSTESTEN	
13	reserved	
12	reserved	
11	reserved	
10	UCDSWEN_TSTENB	In normal operation, please don't set these registers.
9	RREF_EN_TSTENB	
8	DPPU_EN_TSTENB	
7	DPREF_EN_TSTENB	
6	DMREF_EN_TSTENB	
5	DPDET_EN_TSTENB	
4	DMDET_EN_TSTENB	
3	DPSINK_EN_TSTENB	
2	DMSINK_EN_TSTENB	
1	DP_BUFF_EN_TSTENB	
0	DM_BUFF_EN_TSTENB	

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8.5.46. VBUS_UCD_SET

BC1.2 Charger Detector on the VBUS side Setting

Command Code: 30h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	BCSRETRY	Trigger for re-trial of the USB Charger Port detection. “1”: Start detection / “0”: Release the operation.
11	reserved	
10	reserved	
9	reserved	
8	ADCRTRY	Trigger for re-trial of USB ID Resistor detection. “1”: Start detection / “0”: Release the operation.
7	USBDETEN	Enabling USB Charger port detection. “1”: Enable / “0”: Disable.
6	IDRDETEN	Enabling USB ID Resistor detection. “1”: Enable / “0”: Disable.
5	ENUMRDY	Setting USB Enumeration to Ready. “1”: Skip Secondary Detection / “0”: Normal operation.
4	ADCPOLEN	USB ID input polling enable. “1”: Enable (always detection) / “0”: Disable.
3	DCDMODE	DCD timeout period setting. “1”: 1280 ms / “0”: 640 ms.
2	reserved	
1	USB_SW_EN	Enabling automatic USB-Switch control. “1”: Enable (auto) / “0”: Disable (manual).
0	USB_SW	USB Switch manual control. “1”: Switch ON / “0”: Switch OFF.

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8.5.47. VBUS_UCD_STATUS

BC1.2 Charger Detect Status on the VBUS side

Command Code: 31h
Bus Protocol: Read Word

Bit	Symbol	Description
15	DCDFAIL	DCD (USB Data Contact Detection) failed (timeout) status. “1”: Failed / “0”: Succeeded.
14	reserved	
13	CHGPORT[1]	USB Charger Port Detection result. 00b: No charger port/ 01b: SDP/ 10b: CDP/ 11b: DCP
12	CHGPORT[0]	
11	PUPDET	Pull-up detected at Primary Detection after DCDFAIL. “1”: Detected / “0”: Not detected.
10	reserved	
9	reserved	
8	reserved	
7	VBUS_VLD	USB VBUS valid voltage detection status. “1”: Valid / “0”: Not valid.
6	CHGDET	USB Charger Port detection status. “1”: Detected / “0”: Not detected.
5	reserved	
4	reserved	
3	OTGDET	USB OTG Device detection status. “1”: Detected / “0”: Not detected.
2	reserved	
1	reserved	
0	reserved	

	CHGDET	PUPDET	DCDFAIL	CHGPORT[1]	CHGPORT[0]
VBUS Open	0	0	0	0	0
SDP	0	0	0	0	1
CDP	1	0	0	1	0
DCP	1	0	0	1	1
Pull-up Port	0	1	1	0	1
Open Port	0	0	1	0	1
Unstable Port	0	0	1	0	1

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8.5.48. VBUS_IDD_STATUS

ID Detect Status on the VBUS side

Command Code: 32h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	reserved	
6	VBINOP	VBUS voltage status while ID detection. “1”: Normal voltage / “0”: Abnormal voltage.
5	EXTID	Check MHL ID (1k Ohm) detection support. “1”: Supported / “0”: Not supported.
4	IDRDET	USB ID Resistor contact detection status. “1”: Detected (contacted) / “0”: Not detected (removed).
3	INDO[3]	USB ID detection result.
2	INDO[2]	
1	INDO[1]	
0	INDO[0]	

INDO	ID Resistance	Detected Port/Device
0h	0 - 10Ω	RID_GND (OTG)
1h	36.5kΩ	RID_C (ACA_C, SDP)
2h	47kΩ	-
3h	68kΩ	RID_B (ACA_B, DCP)
4h	102kΩ	-
5h	124kΩ	RID_A (ACA_A, CDP)
6h	180kΩ	-
7h	200kΩ	RID_FLOAT
8h	287kΩ	-
9h	390kΩ	-
Ah	440kΩ	-
Bh	557kΩ	-
Ch	797kΩ	-
Dh	>1MΩ	-
Eh	1KΩ	(MHL)
Fh	Illegal ID	Unknown

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8.5.49. VBUS_UCD_FCTRL_SET

BC1.2 Charger Detector on the VBUS side Manual Control Setting

Command Code: 33h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	UCDSWEN	In normal operation, please don't set these registers.
9	RREF_EN	
8	DPPU_EN	
7	DPREF_EN	
6	DMREF_EN	
5	DPDET_EN	
4	DMDET_EN	
3	DPSINK_EN	
2	DMSINK_EN	
1	DP_BUFF_EN	
0	DM_BUFF_EN	

8.5.50. VBUS_UCD_FCTRL_EN

BC1.2 Charger Detector on the VBUS side Manual Control Enable

Command Code: 34h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	EXTCLKENBL	In normal operation, please don't set these registers.
14	PLSTESTEN	
13	reserved	
12	reserved	
11	reserved	
10	UCDSWEN_TSTENB	In normal operation, please don't set these registers.
9	RREF_EN_TSTENB	
8	DPPU_EN_TSTENB	
7	DPREF_EN_TSTENB	
6	DMREF_EN_TSTENB	
5	DPDET_EN_TSTENB	
4	DMDET_EN_TSTENB	
3	DPSINK_EN_TSTENB	
2	DMSINK_EN_TSTENB	
1	DP_BUFF_EN_TSTENB	
0	DM_BUFF_EN_TSTENB	

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8.5.51. CHIP_ID

Chip ID

Command Code: 38h
Bus Protocol: Read Word

Bit	Symbol	Description
15	CHIP_ID[15]	Chip ID
14	CHIP_ID[14]	
13	CHIP_ID[13]	
12	CHIP_ID[12]	
11	CHIP_ID[11]	
10	CHIP_ID[10]	
9	CHIP_ID[9]	
8	CHIP_ID[8]	
7	CHIP_ID[7]	
6	CHIP_ID[6]	
5	CHIP_ID[5]	
4	CHIP_ID[4]	
3	CHIP_ID[3]	
2	CHIP_ID[2]	
1	CHIP_ID[1]	
0	CHIP_ID[0]	

8.5.52. CHIP_REV

Chip Revision

Command Code: 39h
Bus Protocol: Read Word

Bit	Symbol	Description
15	CHIP_REV[15]	Chip Revision
14	CHIP_REV[14]	
13	CHIP_REV[13]	
12	CHIP_REV[12]	
11	CHIP_REV[11]	
10	CHIP_REV[10]	
9	CHIP_REV[9]	
8	CHIP_REV[8]	
7	CHIP_REV[7]	
6	CHIP_REV[6]	
5	CHIP_REV[5]	
4	CHIP_REV[4]	
3	CHIP_REV[3]	
2	CHIP_REV[2]	
1	CHIP_REV[1]	
0	CHIP_REV[0]	

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8.5.53. IC_SET1

ACP discharge control and ACOK control setting.

Command Code: 3Ah
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	ONE_CELL_MODE	1 cell battery mode. “1”: 1 cell battery mode/ “0”: 2~4 cells battery mode “1”:VFASTCHG_REG_SET1, 2, 3 set less than 4.6V and VSYSREG_SET set less than 5.0V “0”:VSYSREG_SET set more than 5.0V
10	reserved	
9	VACP_AUTO_DISCHG	VACP Auto Discharge control is enable when the Power path is changed. “1”: VACP Auto discharge control is enabled./ “0”: Disabled.
8	VACP_LOAD	VACP Discharge control when the VACP power path is plugged off. “1”: VACP load on and discharged./ “0”: VACP load off.
7	reserved	
6	reserved	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	ACOK_POL	ACOK open drain output polarity control. “1”: ACOK polarity is inverted, L=Asserted, Hi-z=Deasserted. / “0”: ACOK polarity is normal, L=Deasserted, Hi-z=Asserted.
0	ACOK_DISEN	ACOK open drain output disable. “1”: Disable, ACOK is Hi-z. / “0”: Enable.

8.5.54. IC_SET2

Debug Setting Register (for debug and production test)

Command Code: 3Bh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	DEBUG_SET[8]	Debug Setting (for debug and production test)
7	DEBUG_SET[7]	Debug Setting (for debug and production test)
6	DEBUG_SET[6]	Debug Setting (for debug and production test)
5	DEBUG_SET[5]	Debug Setting (for debug and production test)
4	DEBUG_SET[4]	Debug Setting (for debug and production test)
3	reserved	
2	reserved	
1	reserved	
0	DEBUG_SET[0]	Debug Setting (for debug and production test)

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8.5.55. SYSTEM_STATUS

System Power-on Status

Command Code: 3Ch
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	reserved	
6	MONRST_STATE	Reset status for MONRST. “1”: Reset asserted / “0”: Reset released.
5	ALMRST_STATE	Reset status for ALMRST. “1”: Reset asserted / “0”: Reset released.
4	CHGRST_STATE	Reset status for CHGRST. “1”: Reset asserted / “0”: Reset released.
3	reserved	
2	reserved	
1	OTPLD_STATE	OTPROM loading status. “1” shows the OTPROM loading is finished./ “0”: not finished.
0	ALLRST_STATE	Reset status for ALLRST. “1”: Reset asserted / “0”: Reset released.

8.5.56. SYSTEM_CTRL_SET

Software reset and reload OTP

Command Code: 3Dh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	reserved	
6	MONRST	Writing “1” resets Voltage Meter block and the status registers. But the setting registers are not initialized. Writing “0” releases reset operation.
5	ALMRST	Writing “1” resets Interrupt block and the status registers. But the setting registers are not initialized. Writing “0” releases reset operation.
4	CHGRST	Writing “1” resets Battery Charger block and USB Detector block and the status registers. But the setting registers are not initialized. Writing “0” releases reset operation.
3	reserved	
2	reserved	
1	OTPLD	Writing “1” starts to load the OTPROM data into the internal registers. OTPROM data is loaded automatically for power-on sequence. But if necessary, user is able to reload the OTPROM data by writing this bit “1”.
0	ALLRST	Writing “1” resets Voltage Meter block, Interrupt block, Battery Charger block and USB Detector blocks and the status registers. But the setting registers are not initialized. Writing “0” release reset operation.

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8.5.57. PROTECT_SET

Access Un-protect Setting for Address 3Fh

Command Code: 3Eh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	PROTECT_SET[15]	Access Un-protect Setting for the “debug command map” (debug and production test only)
14	PROTECT_SET[14]	
13	PROTECT_SET[13]	
12	PROTECT_SET[12]	
11	PROTECT_SET[11]	
10	PROTECT_SET[10]	
9	PROTECT_SET[9]	
8	PROTECT_SET[8]	
7	PROTECT_SET[7]	
6	PROTECT_SET[6]	
5	PROTECT_SET[5]	
4	PROTECT_SET[4]	
3	PROTECT_SET[3]	
2	PROTECT_SET[2]	
1	PROTECT_SET[1]	
0	PROTECT_SET[0]	

8.5.58. MAP_SET

Change Command Code Map

Command Code: 3Fh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	MAP_SET[15]	Change Command Code Map
14	MAP_SET[14]	
13	MAP_SET[13]	
12	MAP_SET[12]	
11	MAP_SET[11]	
10	MAP_SET[10]	
9	MAP_SET[9]	
8	MAP_SET[8]	
7	MAP_SET[7]	
6	MAP_SET[6]	
5	MAP_SET[5]	
4	MAP_SET[4]	
3	MAP_SET[3]	
2	MAP_SET[2]	
1	MAP_SET[1]	
0	MAP_SET[0]	

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8.5.59. VM_CTRL_SET

SAR-ADC Measurement Control Setting

Command Code: 40h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	ADCINTERVAL[1]	SAR-ADC Operating Interval Setting.
14	ADCINTERVAL[0]	00b: No Interval/ 01b: 1ms/ 10b: 10ms/ 11b: 100msec
13	ADCMOD[1]	Operation Mode Setting
12	ADCMOD[0]	00b: Power Down/ 01b: Normal Operation
11	ADCTMOD[1]	Test Mode Setting
10	ADCTMOD[0]	00b: Normal Operation/ 01b: Test Mode
9	EXTIADPEN	IADP (Input current Limit setting pin) voltage measurement. “1”: Enable / “0”: Disable.
8	VSYSENB	VSYS voltage measurement. “1”: Enable / “0”: Disable.
7	VCCENB	VCC voltage measurement. “1”: Enable / “0”: Disable.
6	VBUSENB	VBUS voltage measurement. “1”: Enable / “0”: Disable.
5	VACPENB	VACP voltage measurement. “1”: Enable / “0”: Disable.
4	IACPENB	IACP voltage measurement. “1”: Enable / “0”: Disable.
3	THERMENB	TSENSE voltage measurement. “1”: Enable / “0”: Disable.
2	VBATENB	VBAT voltage measurement. “1”: Enable / “0”: Disable.
1	IBATMENB	IBATM current (discharge) measurement. “1”: Enable / “0”: Disable.
0	IBATPENB	IBATP current (current) measurement. “1”: Enable / “0”: Disable.

8.5.60. THERM_WINDOW_SET1

JEITA Battery Temperature Window Setting 1

Command Code: 41h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TMPTHR1B[7]	Upper threshold of T1, JEITA profile. (200-THERM1B [7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps.
14	TMPTHR1B[6]	
13	TMPTHR1B[5]	
12	TMPTHR1B[4]	
11	TMPTHR1B[3]	
10	TMPTHR1B[2]	
9	TMPTHR1B[1]	
8	TMPTHR1B[0]	
7	TMPTHR1A[7]	Lower threshold of T1, JEITA profile. (200-THERM1A [7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps.
6	TMPTHR1A[6]	
5	TMPTHR1A[5]	
4	TMPTHR1A[4]	
3	TMPTHR1A[3]	
2	TMPTHR1A[2]	
1	TMPTHR1A[1]	
0	TMPTHR1A[0]	

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8.5.61. THERM_WINDOW_SET2

JEITA Battery Temperature Window Setting 2
Command Code: 42h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TMPTHR2B[7]	Upper threshold of T2, JEITA profile. (200-THERM2B [7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps.
14	TMPTHR2B[6]	
13	TMPTHR2B[5]	
12	TMPTHR2B[4]	
11	TMPTHR2B[3]	
10	TMPTHR2B[2]	
9	TMPTHR2B[1]	
8	TMPTHR2B[0]	
7	TMPTHR2A[7]	Lower threshold of T2, JEITA profile. (200-THERM2A [7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps.
6	TMPTHR2A[6]	
5	TMPTHR2A[5]	
4	TMPTHR2A[4]	
3	TMPTHR2A[3]	
2	TMPTHR2A[2]	
1	TMPTHR2A[1]	
0	TMPTHR2A[0]	

8.5.62. THERM_WINDOW_SET3

JEITA Battery Temperature Window Setting 3

Command Code: 43h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TMPTHR3B[7]	Upper threshold of T3, JEITA profile. (200-THERM3B [7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps.
14	TMPTHR3B[6]	
13	TMPTHR3B[5]	
12	TMPTHR3B[4]	
11	TMPTHR3B[3]	
10	TMPTHR3B[2]	
9	TMPTHR3B[1]	
8	TMPTHR3B[0]	
7	TMPTHR3A[7]	Lower threshold of T3, JEITA profile. (200-THERM3A [7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps.
6	TMPTHR3A[6]	
5	TMPTHR3A[5]	
4	TMPTHR3A[4]	
3	TMPTHR3A[3]	
2	TMPTHR3A[2]	
1	TMPTHR3A[1]	
0	TMPTHR3A[0]	

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8.5.63. THERM_WINDOW_SET4

JEITA Battery Temperature Window Setting 4

Command Code: 44h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TMPTHR4B[7]	Upper threshold of T4, JEITA profile. (200-THERM4B [7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps.
14	TMPTHR4B[6]	
13	TMPTHR4B[5]	
12	TMPTHR4B[4]	
11	TMPTHR4B[3]	
10	TMPTHR4B[2]	
9	TMPTHR4B[1]	
8	TMPTHR4B[0]	
7	TMPTHR4A[7]	Lower threshold of T4, JEITA profile. (200-THERM4A [7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps.
6	TMPTHR4A[6]	
5	TMPTHR4A[5]	
4	TMPTHR4A[4]	
3	TMPTHR4A[3]	
2	TMPTHR4A[2]	
1	TMPTHR4A[1]	
0	TMPTHR4A[0]	

8.5.64. THERM_WINDOW_SET5

JEITA Battery Temperature Window Setting 5

Command Code: 45h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TMPTHR5B[7]	Upper threshold of T5, between T3 and T4. (200-THERM5B [7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps.
14	TMPTHR5B[6]	
13	TMPTHR5B[5]	
12	TMPTHR5B[4]	
11	TMPTHR5B[3]	
10	TMPTHR5B[2]	
9	TMPTHR5B[1]	
8	TMPTHR5B[0]	
7	TMPTHR5A[7]	Lower threshold of T5, between T3 and T4. (200-THERM5A [7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps.
6	TMPTHR5A[6]	
5	TMPTHR5A[5]	
4	TMPTHR5A[4]	
3	TMPTHR5A[3]	
2	TMPTHR5A[2]	
1	TMPTHR5A[1]	
0	TMPTHR5A[0]	

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8.5.65. IBATP_TH_SET

Battery Current (Charge) Interrupt Threshold Setting

Command Code: 46h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	IBATP_TH_SET[14]	Battery Current (Charge) Interrupt Threshold. 0 to 25,000mA, 1mA steps. The register range : 0 to 32,752mA. But the actual range : 0 to 25,000mA.
13	IBATP_TH_SET[13]	
12	IBATP_TH_SET[12]	
11	IBATP_TH_SET[11]	
10	IBATP_TH_SET[10]	
9	IBATP_TH_SET[9]	
8	IBATP_TH_SET[8]	
7	IBATP_TH_SET[7]	
6	IBATP_TH_SET[6]	
5	IBATP_TH_SET[5]	
4	IBATP_TH_SET[4]	
3	IBATP_TH_SET[3]	
2	IBATP_TH_SET[2]	
1	IBATP_TH_SET[1]	
0	IBATP_TH_SET[0]	

8.5.66. IBATM_TH_SET

Battery Current (Dis-charge) Interrupt Threshold Setting

Command Code: 47h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	IBATM_TH_SET[14]	Battery Current (Dis-charge) Interrupt Threshold. 0 to 25,000mA, 1mA steps. The register range : 0 to 32,752mA. But the actual range : 0 to 25,000mA.
13	IBATM_TH_SET[13]	
12	IBATM_TH_SET[12]	
11	IBATM_TH_SET[11]	
10	IBATM_TH_SET[10]	
9	IBATM_TH_SET[9]	
8	IBATM_TH_SET[8]	
7	IBATM_TH_SET[7]	
6	IBATM_TH_SET[6]	
5	IBATM_TH_SET[5]	
4	IBATM_TH_SET[4]	
3	IBATM_TH_SET[3]	
2	IBATM_TH_SET[2]	
1	IBATM_TH_SET[1]	
0	IBATM_TH_SET[0]	

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8.5.67. VBAT_TH_SET

Battery Voltage Interrupt Threshold Setting

Command Code: 48h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VBAT_TH_SET[14]	Battery Voltage Interrupt Threshold. 0 to 19,200mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 19,200mV.
13	VBAT_TH_SET[13]	
12	VBAT_TH_SET[12]	
11	VBAT_TH_SET[11]	
10	VBAT_TH_SET[10]	
9	VBAT_TH_SET[9]	
8	VBAT_TH_SET[8]	
7	VBAT_TH_SET[7]	
6	VBAT_TH_SET[6]	
5	VBAT_TH_SET[5]	
4	VBAT_TH_SET[4]	
3	VBAT_TH_SET[3]	
2	VBAT_TH_SET[2]	
1	VBAT_TH_SET[1]	
0	VBAT_TH_SET[0]	

8.5.68. THERM_TH_SET

Battery Temperature Interrupt Threshold Setting

Command Code: 49h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	THERM_TH_SET[7]	Battery Temperature Interrupt Threshold Setting (200-THERM_TH_SET[7:0]) deg-C. -55 to 200 deg-C range, 1 deg-C steps.
6	THERM_TH_SET[6]	
5	THERM_TH_SET[5]	
4	THERM_TH_SET[4]	
3	THERM_TH_SET[3]	
2	THERM_TH_SET[2]	
1	THERM_TH_SET[1]	
0	THERM_TH_SET[0]	

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8.5.69. IACP_TH_SET

Input Current (between ACP-ACN) Interrupt Threshold Setting

Command Code: 4Ah
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	IACP_TH_SET[14]	Input Current (between ACP-ACN) Interrupt Threshold. 0 to 16,384mA, 1mA steps. The register range : 0 to 32,752mA. But the actual range : 0 to 16,383mA.
13	IACP_TH_SET[13]	
12	IACP_TH_SET[12]	
11	IACP_TH_SET[11]	
10	IACP_TH_SET[10]	
9	IACP_TH_SET[9]	
8	IACP_TH_SET[8]	
7	IACP_TH_SET[7]	
6	IACP_TH_SET[6]	
5	IACP_TH_SET[5]	
4	IACP_TH_SET[4]	
3	IACP_TH_SET[3]	
2	IACP_TH_SET[2]	
1	IACP_TH_SET[1]	
0	IACP_TH_SET[0]	

8.5.70. VACP_TH_SET

Input Voltage (ACP) Interrupt Threshold Setting

Command Code: 4Bh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VACP_TH_SET[14]	Input Voltage (ACP) Interrupt Threshold. 0 to 25,600mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 25,600mV.
13	VACP_TH_SET[13]	
12	VACP_TH_SET[12]	
11	VACP_TH_SET[11]	
10	VACP_TH_SET[10]	
9	VACP_TH_SET[9]	
8	VACP_TH_SET[8]	
7	VACP_TH_SET[7]	
6	VACP_TH_SET[6]	
5	VACP_TH_SET[5]	
4	VACP_TH_SET[4]	
3	VACP_TH_SET[3]	
2	VACP_TH_SET[2]	
1	VACP_TH_SET[1]	
0	VACP_TH_SET[0]	

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8.5.71. VBUS_TH_SET

VBUS Voltage Interrupt Threshold Setting

Command Code: 4Ch
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VBUS_TH_SET[14]	VBUS Voltage Interrupt Threshold. 0 to 25,600mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 25,600mV.
13	VBUS_TH_SET[13]	
12	VBUS_TH_SET[12]	
11	VBUS_TH_SET[11]	
10	VBUS_TH_SET[10]	
9	VBUS_TH_SET[9]	
8	VBUS_TH_SET[8]	
7	VBUS_TH_SET[7]	
6	VBUS_TH_SET[6]	
5	VBUS_TH_SET[5]	
4	VBUS_TH_SET[4]	
3	VBUS_TH_SET[3]	
2	VBUS_TH_SET[2]	
1	VBUS_TH_SET[1]	
0	VBUS_TH_SET[0]	

8.5.72. VCC_TH_SET

VCC Voltage Interrupt Threshold Setting

Command Code: 4Dh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VCC_TH_SET[14]	VCC Voltage Interrupt Threshold. 0 to 25,600mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 25,600mV.
13	VCC_TH_SET[13]	
12	VCC_TH_SET[12]	
11	VCC_TH_SET[11]	
10	VCC_TH_SET[10]	
9	VCC_TH_SET[9]	
8	VCC_TH_SET[8]	
7	VCC_TH_SET[7]	
6	VCC_TH_SET[6]	
5	VCC_TH_SET[5]	
4	VCC_TH_SET[4]	
3	VCC_TH_SET[3]	
2	VCC_TH_SET[2]	
1	VCC_TH_SET[1]	
0	VCC_TH_SET[0]	

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8.5.73. VSYS_TH_SET

VSYS Voltage Interrupt Threshold Setting

Command Code: 4Eh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VSYS_TH_SET[14]	VSYS Voltage Interrupt 0 to 19,200mV, 1mV steps. The register range : 0 to 32,752mV. But the actual range : 0 to 19,200mV.
13	VSYS_TH_SET[13]	
12	VSYS_TH_SET[12]	
11	VSYS_TH_SET[11]	
10	VSYS_TH_SET[10]	
9	VSYS_TH_SET[9]	
8	VSYS_TH_SET[8]	
7	VSYS_TH_SET[7]	
6	VSYS_TH_SET[6]	
5	VSYS_TH_SET[5]	
4	VSYS_TH_SET[4]	
3	VSYS_TH_SET[3]	
2	VSYS_TH_SET[2]	
1	VSYS_TH_SET[1]	
0	VSYS_TH_SET[0]	

8.5.74. EXTIADP_TH_SET

IADP (Input current Limit setting pin) Voltage Interrupt Threshold Setting

Command Code: 4Fh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	EXTIADP_TH_SET[11]	IADP (Input current Limit setting pin) voltage Interrupt (for Debug use)
10	EXTIADP_TH_SET[10]	
9	EXTIADP_TH_SET[9]	
8	EXTIADP_TH_SET[8]	
7	EXTIADP_TH_SET[7]	
6	EXTIADP_TH_SET[6]	
5	EXTIADP_TH_SET[5]	
4	EXTIADP_TH_SET[4]	
3	EXTIADP_TH_SET[3]	
2	EXTIADP_TH_SET[2]	
1	EXTIADP_TH_SET[1]	
0	EXTIADP_TH_SET[0]	

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8.5.75. IBATP_VAL

Battery Current (Charge) Measurement Value

Command Code: 50h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IBATP_VAL[14]	Battery Current (Charge) Measurement Value 0 to 25,000mA, 1mA steps.
13	IBATP_VAL[13]	
12	IBATP_VAL[12]	
11	IBATP_VAL[11]	
10	IBATP_VAL[10]	
9	IBATP_VAL[9]	
8	IBATP_VAL[8]	
7	IBATP_VAL[7]	
6	IBATP_VAL[6]	
5	IBATP_VAL[5]	
4	IBATP_VAL[4]	
3	IBATP_VAL[3]	
2	IBATP_VAL[2]	
1	IBATP_VAL[1]	
0	IBATP_VAL[0]	

8.5.76. IBATP_AVE_VAL

Battery Current (Charge) Measurement Average Value

Command Code: 51h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IBATP_AVE_VAL[14]	Battery Current (Charge) Measurement Average Value 0 to 25,000mA, 1mA steps.
13	IBATP_AVE_VAL[13]	
12	IBATP_AVE_VAL[12]	
11	IBATP_AVE_VAL[11]	
10	IBATP_AVE_VAL[10]	
9	IBATP_AVE_VAL[9]	
8	IBATP_AVE_VAL[8]	
7	IBATP_AVE_VAL[7]	
6	IBATP_AVE_VAL[6]	
5	IBATP_AVE_VAL[5]	
4	IBATP_AVE_VAL[4]	
3	IBATP_AVE_VAL[3]	
2	IBATP_AVE_VAL[2]	
1	IBATP_AVE_VAL[1]	
0	IBATP_AVE_VAL[0]	

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8.5.77. IBATM_VAL

Battery Current (Dis-charge) Measurement Value

Command Code: 52h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IBATM_VAL[14]	Battery Current (Dis-charge) Measurement Value 0 to 25,000mA, 1mA steps.
13	IBATM_VAL[13]	
12	IBATM_VAL[12]	
11	IBATM_VAL[11]	
10	IBATM_VAL[10]	
9	IBATM_VAL[9]	
8	IBATM_VAL[8]	
7	IBATM_VAL[7]	
6	IBATM_VAL[6]	
5	IBATM_VAL[5]	
4	IBATM_VAL[4]	
3	IBATM_VAL[3]	
2	IBATM_VAL[2]	
1	IBATM_VAL[1]	
0	IBATM_VAL[0]	

8.5.78. IBATM_AVE_VAL

Battery Current (Dis-charge) Measurement Average Value

Command Code: 53h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IBATM_AVE_VAL[14]	Battery Current (Dis-charge) Measurement Average Value 0 to 25,000mA, 1mA steps.
13	IBATM_AVE_VAL[13]	
12	IBATM_AVE_VAL[12]	
11	IBATM_AVE_VAL[11]	
10	IBATM_AVE_VAL[10]	
9	IBATM_AVE_VAL[9]	
8	IBATM_AVE_VAL[8]	
7	IBATM_AVE_VAL[7]	
6	IBATM_AVE_VAL[6]	
5	IBATM_AVE_VAL[5]	
4	IBATM_AVE_VAL[4]	
3	IBATM_AVE_VAL[3]	
2	IBATM_AVE_VAL[2]	
1	IBATM_AVE_VAL[1]	
0	IBATM_AVE_VAL[0]	

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8.5.79. VBAT_VAL

Battery Voltage Measurement Value

Command Code: 54h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VBAT_VAL[14]	Battery Voltage Measurement Value 0 to 19,200mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 19,200mV.
13	VBAT_VAL[13]	
12	VBAT_VAL[12]	
11	VBAT_VAL[11]	
10	VBAT_VAL[10]	
9	VBAT_VAL[9]	
8	VBAT_VAL[8]	
7	VBAT_VAL[7]	
6	VBAT_VAL[6]	
5	VBAT_VAL[5]	
4	VBAT_VAL[4]	
3	VBAT_VAL[3]	
2	VBAT_VAL[2]	
1	VBAT_VAL[1]	
0	VBAT_VAL[0]	

8.5.80. VBAT_AVE_VAL

Battery Voltage Measurement Average Value

Command Code: 55h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VBAT_AVE_VAL[14]	Battery Voltage Measurement Average Value 0 to 19,200mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 19,200mV.
13	VBAT_AVE_VAL[13]	
12	VBAT_AVE_VAL[12]	
11	VBAT_AVE_VAL[11]	
10	VBAT_AVE_VAL[10]	
9	VBAT_AVE_VAL[9]	
8	VBAT_AVE_VAL[8]	
7	VBAT_AVE_VAL[7]	
6	VBAT_AVE_VAL[6]	
5	VBAT_AVE_VAL[5]	
4	VBAT_AVE_VAL[4]	
3	VBAT_AVE_VAL[3]	
2	VBAT_AVE_VAL[2]	
1	VBAT_AVE_VAL[1]	
0	VBAT_AVE_VAL[0]	

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8.5.81. THERM_VAL

Thermistor Temperature Measurement Value

Command Code: 56h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	THERM_VAL[7]	Temperature Measurement Value (200-THERM_VAL[7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps. Write Word access is available when VM_CTRL_SET.THERMENB bit = 0.
6	THERM_VAL[6]	
5	THERM_VAL[5]	
4	THERM_VAL[4]	
3	THERM_VAL[3]	
2	THERM_VAL[2]	
1	THERM_VAL[1]	
0	THERM_VAL[0]	

8.5.82. VTH_VAL

Thermistor Measurement Voltage Value

Command Code: 57h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	VTH_VAL[11]	Thermistor Measurement Voltage Value (for Debug use)
10	VTH_VAL[10]	
9	VTH_VAL[9]	
8	VTH_VAL[8]	
7	VTH_VAL[7]	
6	VTH_VAL[6]	
5	VTH_VAL[5]	
4	VTH_VAL[4]	
3	VTH_VAL[3]	
2	VTH_VAL[2]	
1	VTH_VAL[1]	
0	VTH_VAL[0]	

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8.5.83. IACP_VAL

Input Current (between ACP-ACN) Measurement Value

Command Code: 58h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IACP_VAL[14]	Input Current (between ACP-ACN) Measurement Value 0 to 16,384mA, 1mA steps.
13	IACP_VAL[13]	
12	IACP_VAL[12]	
11	IACP_VAL[11]	
10	IACP_VAL[10]	
9	IACP_VAL[9]	
8	IACP_VAL[8]	
7	IACP_VAL[7]	
6	IACP_VAL[6]	
5	IACP_VAL[5]	
4	IACP_VAL[4]	
3	IACP_VAL[3]	
2	IACP_VAL[2]	
1	IACP_VAL[1]	
0	IACP_VAL[0]	

8.5.84. IACP_AVE_VAL

Input Current (between ACP-ACN) Measurement Average Value

Command Code: 59h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IACP_AVE_VAL[14]	Input Current (between ACP-ACN) Measurement Average Value 0 to 16,384mA, 1mA steps.
13	IACP_AVE_VAL[13]	
12	IACP_AVE_VAL[12]	
11	IACP_AVE_VAL[11]	
10	IACP_AVE_VAL[10]	
9	IACP_AVE_VAL[9]	
8	IACP_AVE_VAL[8]	
7	IACP_AVE_VAL[7]	
6	IACP_AVE_VAL[6]	
5	IACP_AVE_VAL[5]	
4	IACP_AVE_VAL[4]	
3	IACP_AVE_VAL[3]	
2	IACP_AVE_VAL[2]	
1	IACP_AVE_VAL[1]	
0	IACP_AVE_VAL[0]	

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8.5.85. VACP_VAL

Input Voltage (ACP) Measurement Value

Command Code: 5Ah
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VACP_VAL[14]	Input Voltage (ACP) Measurement Value 0 to 25,600mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 25,600mV.
13	VACP_VAL[13]	
12	VACP_VAL[12]	
11	VACP_VAL[11]	
10	VACP_VAL[10]	
9	VACP_VAL[9]	
8	VACP_VAL[8]	
7	VACP_VAL[7]	
6	VACP_VAL[6]	
5	VACP_VAL[5]	
4	VACP_VAL[4]	
3	VACP_VAL[3]	
2	VACP_VAL[2]	
1	VACP_VAL[1]	
0	VACP_VAL[0]	

8.5.86. VACP_AVE_VAL

Input Voltage (ACP) Measurement Average Value

Command Code: 5Bh
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VACP_AVE_VAL[14]	Input Voltage (ACP) Measurement Average Value 0 to 25,600mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 25,600mV.
13	VACP_AVE_VAL[13]	
12	VACP_AVE_VAL[12]	
11	VACP_AVE_VAL[11]	
10	VACP_AVE_VAL[10]	
9	VACP_AVE_VAL[9]	
8	VACP_AVE_VAL[8]	
7	VACP_AVE_VAL[7]	
6	VACP_AVE_VAL[6]	
5	VACP_AVE_VAL[5]	
4	VACP_AVE_VAL[4]	
3	VACP_AVE_VAL[3]	
2	VACP_AVE_VAL[2]	
1	VACP_AVE_VAL[1]	
0	VACP_AVE_VAL[0]	

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8.5.87. VBUS_VAL

VBUS Voltage Measurement Value

Command Code: 5Ch
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VBUS_VAL[14]	VBUS Voltage Measurement Value 0 to 25,600mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 25,600mV.
13	VBUS_VAL[13]	
12	VBUS_VAL[12]	
11	VBUS_VAL[11]	
10	VBUS_VAL[10]	
9	VBUS_VAL[9]	
8	VBUS_VAL[8]	
7	VBUS_VAL[7]	
6	VBUS_VAL[6]	
5	VBUS_VAL[5]	
4	VBUS_VAL[4]	
3	VBUS_VAL[3]	
2	VBUS_VAL[2]	
1	VBUS_VAL[1]	
0	VBUS_VAL[0]	

8.5.88. VBUS_AVE_VAL

VBUS Voltage Measurement Average Value

Command Code: 5Dh
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VBUS_AVE_VAL[14]	VBUS Voltage Measurement Average Value 0 to 25,600mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 25,600mV.
13	VBUS_AVE_VAL[13]	
12	VBUS_AVE_VAL[12]	
11	VBUS_AVE_VAL[11]	
10	VBUS_AVE_VAL[10]	
9	VBUS_AVE_VAL[9]	
8	VBUS_AVE_VAL[8]	
7	VBUS_AVE_VAL[7]	
6	VBUS_AVE_VAL[6]	
5	VBUS_AVE_VAL[5]	
4	VBUS_AVE_VAL[4]	
3	VBUS_AVE_VAL[3]	
2	VBUS_AVE_VAL[2]	
1	VBUS_AVE_VAL[1]	
0	VBUS_AVE_VAL[0]	

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8.5.89. VCC_VAL

VCC Voltage Measurement Value

Command Code: 5Eh
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VCC_VAL[14]	VCC Voltage Measurement Value 0 to 25,600mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 25,600mV.
13	VCC_VAL[13]	
12	VCC_VAL[12]	
11	VCC_VAL[11]	
10	VCC_VAL[10]	
9	VCC_VAL[9]	
8	VCC_VAL[8]	
7	VCC_VAL[7]	
6	VCC_VAL[6]	
5	VCC_VAL[5]	
4	VCC_VAL[4]	
3	VCC_VAL[3]	
2	VCC_VAL[2]	
1	VCC_VAL[1]	
0	VCC_VAL[0]	

8.5.90. VCC_AVE_VAL

VCC Voltage Measurement Average Value

Command Code: 5Fh
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VCC_AVE_VAL[14]	VCC Voltage Measurement Average Value 0 to 25,600mV, 1mV steps. The register range : 0 to 32,767mV. But the actual range : 0 to 25,600mV.
13	VCC_AVE_VAL[13]	
12	VCC_AVE_VAL[12]	
11	VCC_AVE_VAL[11]	
10	VCC_AVE_VAL[10]	
9	VCC_AVE_VAL[9]	
8	VCC_AVE_VAL[8]	
7	VCC_AVE_VAL[7]	
6	VCC_AVE_VAL[6]	
5	VCC_AVE_VAL[5]	
4	VCC_AVE_VAL[4]	
3	VCC_AVE_VAL[3]	
2	VCC_AVE_VAL[2]	
1	VCC_AVE_VAL[1]	
0	VCC_AVE_VAL[0]	

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8.5.91. VSYS_VAL

VSYS Voltage Measurement Value

Command Code: 60h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VSYS_VAL[14]	VSYS Voltage Measurement Value 0 to 19,200mV, 1mV steps. The register range : 0 to 32,752mV. But the actual range : 0 to 19,200mV.
13	VSYS_VAL[13]	
12	VSYS_VAL[12]	
11	VSYS_VAL[11]	
10	VSYS_VAL[10]	
9	VSYS_VAL[9]	
8	VSYS_VAL[8]	
7	VSYS_VAL[7]	
6	VSYS_VAL[6]	
5	VSYS_VAL[5]	
4	VSYS_VAL[4]	
3	VSYS_VAL[3]	
2	VSYS_VAL[2]	
1	VSYS_VAL[1]	
0	VSYS_VAL[0]	

8.5.92. VSYS_AVE_VAL

VSYS Voltage Measurement Average Value

Command Code: 61h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VSYS_AVE_VAL[14]	VSYS Voltage Measurement Average Value 0 to 19,200mV, 1mV steps. The register range : 0 to 32,752mV. But the actual range : 0 to 19,200mV.
13	VSYS_AVE_VAL[13]	
12	VSYS_AVE_VAL[12]	
11	VSYS_AVE_VAL[11]	
10	VSYS_AVE_VAL[10]	
9	VSYS_AVE_VAL[9]	
8	VSYS_AVE_VAL[8]	
7	VSYS_AVE_VAL[7]	
6	VSYS_AVE_VAL[6]	
5	VSYS_AVE_VAL[5]	
4	VSYS_AVE_VAL[4]	
3	VSYS_AVE_VAL[3]	
2	VSYS_AVE_VAL[2]	
1	VSYS_AVE_VAL[1]	
0	VSYS_AVE_VAL[0]	

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8.5.93. EXTIADP_VAL

IADP (Input current Limit setting pin) Voltage Measurement Value

Command Code: 62h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	EXTIADP_VAL[11]	IADP (Input current Limit setting pin) voltage Measurement Value (for Debug use)
10	EXTIADP_VAL[10]	
9	EXTIADP_VAL[9]	
8	EXTIADP_VAL[8]	
7	EXTIADP_VAL[7]	
6	EXTIADP_VAL[6]	
5	EXTIADP_VAL[5]	
4	EXTIADP_VAL[4]	
3	EXTIADP_VAL[3]	
2	EXTIADP_VAL[2]	
1	EXTIADP_VAL[1]	
0	EXTIADP_VAL[0]	

8.5.94. EXTIADP_AVE_VAL

IADP (Input current Limit setting pin) Voltage Measurement Average Value

Command Code: 63h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	EXTIADP_AVE_VAL[11]	IADP (Input current Limit setting pin) voltage Measurement Average Value (for Debug use)
10	EXTIADP_AVE_VAL[10]	
9	EXTIADP_AVE_VAL[9]	
8	EXTIADP_AVE_VAL[8]	
7	EXTIADP_AVE_VAL[7]	
6	EXTIADP_AVE_VAL[6]	
5	EXTIADP_AVE_VAL[5]	
4	EXTIADP_AVE_VAL[4]	
3	EXTIADP_AVE_VAL[3]	
2	EXTIADP_AVE_VAL[2]	
1	EXTIADP_AVE_VAL[1]	
0	EXTIADP_AVE_VAL[0]	

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8.5.95. VACPCLPS_TH_SET

VACP Collapse Detect Threshold Voltage Setting

Command Code: 64h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VACPCLPS_TH_SET[14]	VACP Anti-collapse entry voltage threshold. 3,840 to 32,640mV, 128mV steps. The register range: 0 to 32,640mV. But the actual range: 3,840 to 25,088mV. “00h”setting disables VACP collapse detection.
13	VACPCLPS_TH_SET[13]	
12	VACPCLPS_TH_SET[12]	
11	VACPCLPS_TH_SET[11]	
10	VACPCLPS_TH_SET[10]	
9	VACPCLPS_TH_SET[9]	
8	VACPCLPS_TH_SET[8]	
7	VACPCLPS_TH_SET[7]	
6	reserved	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.96. INT0_SET

1st Level Interrupt Setting

Command Code: 68h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	INT7_EN	2nd Level Interrupt 7 (SAR-ADC) Enable. “1”: Enable / “0”: Disable.
6	INT6_EN	2nd Level Interrupt 6 (Charger) Enable. “1”: Enable / “0”: Disable.
5	INT5_EN	2nd Level Interrupt 5 (Charger) Enable. “1”: Enable / “0”: Disable.
4	INT4_EN	2nd Level Interrupt 4 (VSYS) Enable. “1”: Enable / “0”: Disable.
3	INT3_EN	2nd Level Interrupt 3 (Battery) Enable. “1”: Enable / “0”: Disable.
2	INT2_EN	2nd Level Interrupt 2 (VCC) Enable. “1”: Enable / “0”: Disable.
1	INT1_EN	2nd Level Interrupt 1 (VBUS) Enable. “1”: Enable / “0”: Disable.
0	INT0_EN	1st Level Interrupt Enable. “1”: Enable / “0”: Disable.

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8.5.97. INT1_SET

2nd Level Interrupt Setting 1 (VBUS)

Command Code: 69h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	VBUS_RBUV_DET	Enabling interrupt of entering to VBUS reverse buck boost voltage low. “1”: Enable / “0”: Disable.
14	VBUS_RBUV_RES	Enabling interrupt of exit from VBUS reverse buck boost voltage low. “1”: Enable / “0”: Disable.
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VBUS_TH_DET	Enabling interrupt VBUS Voltage > VBUS_TH_SET. “1”: Enable / “0”: Disable.
8	VBUS_TH_RES	Enabling interrupt VBUS Voltage <= VBUS_TH_SET. “1”: Enable / “0”: Disable.
7	reserved	
6	VBUS_IIN_MOD	Enabling interrupt of VBUS input current-limit modified. “1”: Enable / “0”: Disable.
5	VBUS_OV_DET	Enabling interrupt of VBUS over voltage detected. “1”: Enable / “0”: Disable.
4	VBUS_OV_RES	Enabling interrupt of VBUS over voltage resumed “1”: Enable / “0”: Disable.
3	VBUS_CLPS_DET	Enabling interrupt of entering to VBUS Anti-collapse operation. “1”: Enable / “0”: Disable.
2	VBUS_CLPS RES	Enabling interrupt of exit from VBUS Anti-collapse operation. “1”: Enable / “0”: Disable.
1	VBUS_DET	Enabling interrupt of VBUS detect. “1”: Enable / “0”: Disable.
0	VBUS_RES	Enabling interrupt of VBUS removal. “1”: Enable / “0”: Disable.

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8.5.98. INT2_SET

2nd Level Interrupt Setting 2 (VCC)

Command Code: 6Ah
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	VCC_RBUV_DET	Enabling interrupt of entering to VCC reverse buck boost voltage low. “1”: Enable / “0”: Disable.
14	VCC_RBUV_RES	Enabling interrupt of exit from VCC reverse buck boost voltage low. “1”: Enable / “0”: Disable.
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VCC_TH_DET	Interrupt VCC Voltage > VCC_TH_SET. “1”: Enable / “0”: Disable.
8	VCC_TH_RES	Interrupt VCC Voltage <= VCC_TH_SET. “1”: Enable / “0”: Disable.
7	reserved	
6	VCC_IIN_MOD	Interrupt of VCC/VACP input current-limit modified. “1”: Enable / “0”: Disable. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
5	VCC_OVP_DET	Interrupt of VCC over voltage detected. “1”: Enable / “0”: Disable.
4	VCC_OVP_RES	Interrupt of VCC over voltage resumed “1”: Enable / “0”: Disable.
3	VCC_CLPS_DET	Interrupt of entering to VCC/VACP Anti-collapse operation. “1”: Enable / “0”: Disable. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
2	VCC_CLPS_RES	Interrupt of exit from VCC/VACP Anti-collapse operation. “1”: Enable / “0”: Disable. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
1	VCC_DET	Interrupt of VCC detect. “1”: Enable / “0”: Disable.
0	VCC_RES	Interrupt of VCC removal. “1”: Enable / “0”: Disable.

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8.5.99. INT3_SET

2nd Level Interrupt Setting 3 (Battery)

Command Code: 6Bh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TH_DET	Interrupt of the thermistor detected. “1”: Enable / “0”: Disable.
14	TH_RMV	Interrupt of the thermistor removal. “1”: Enable / “0”: Disable.
13	reserved	
12	reserved	
11	TMP_OUT_DET	Interrupt of the thermistor out of the charging range. “1”: Enable / “0”: Disable.
10	TMP_OUT_RES	Interrupt of the thermistor in to the charging range. “1”: Enable / “0”: Disable.
9	VBAT_TH_DET	Interrupt VBAT Voltage > VBAT_TH_SET. “1”: Enable / “0”: Disable.
8	VBAT_TH_RES	Interrupt VBAT Voltage <= VBAT_TH_SET. “1”: Enable / “0”: Disable.
7	IBAT_SHORT_DET	Interrupt of Battery over current detected. “1”: Enable / “0”: Disable.
6	IBAT_SHORT_RES	Interrupt of Battery over current resumed. “1”: Enable / “0”: Disable.
5	VBAT_OV_DET	Interrupt of VBAT over voltage detected. “1”: Enable / “0”: Disable.
4	VBAT_OV_RES	Interrupt of VBAT over voltage resumed. “1”: Enable / “0”: Disable.
3	BAT_ASSIST_DET	Interrupt of Entering to Battery-assist mode. “1”: Enable / “0”: Disable.
2	BAT_ASSIST_RES	Interrupt of Exiting from Battery-assist mode. “1”: Enable / “0”: Disable.
1	reserved	
0	reserved	

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8.5.100. INT4_SET

2nd Level Interrupt Setting 4 (VSYS)

Command Code: 6Ch
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VSYS_TH_DET	Interrupt VSYS Voltage > VSYS_TH_SET. “1”: Enable / “0”: Disable.
8	VSYS_TH_RES	Interrupt VSYS Voltage <= VSYS_TH_SET. “1”: Enable / “0”: Disable.
7	reserved	
6	reserved	
5	VSYS_OV_DET	Interrupt of VSYS over voltage detected. “1”: Enable / “0”: Disable.
4	VSYS_OV_RES	Interrupt of VSYS over voltage resumed. “1”: Enable / “0”: Disable.
3	VSYS_SHT_DET	Interrupt of VSYS short circuit detected. “1”: Enable / “0”: Disable.
2	VSYS_SHT_RES	Interrupt of VSYS short circuit resumed. “1”: Enable / “0”: Disable.
1	VSYS_UV_DET	Interrupt of VSYS under voltage detected. “1”: Enable / “0”: Disable.
0	VSYS_UV_RES	Interrupt of VSYS under voltage resumed. “1”: Enable / “0”: Disable.

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8.5.101. INT5_SET

2nd Level Interrupt Setting 5 (Charger)

Command Code: 6Dh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	OTP_LOAD_DONE	Interrupt of OTP load done. “1”: Enable / “0”: Disable.
12	PWR_ON	Interrupt of Power-on. “1”: Enable / “0”: Disable.
11	EXTIADP_TRNS	Interrupt IADP voltage range transition. “1”: Enable / “0”: Disable.
10	reserved	
9	EXTIADP_TH_DET	Interrupt IADP (Input current Limit setting pin) voltage > EXTIADP_TH_SET. “1”: Enable / “0”: Disable.
8	EXIADP_TH_RES	Interrupt IADP (Input current Limit setting pin) voltage <= EXTIADP_TH_SET. “1”: Enable / “0”: Disable.
7	BAT_MNT_DET	Interrupt of entering to Battery Maintenance charging. “1”: Enable / “0”: Disable.
6	BAT_MNT_RES	Interrupt of exit from Battery Maintenance charging. “1”: Enable / “0”: Disable.
5	TSD_DET	Interrupt of the TSD detected. “1”: Enable / “0”: Disable.
4	TSD_RES	Interrupt of the TSD resumed. “1”: Enable / “0”: Disable.
3	CHGWDT_EXP	Interrupt of Charger Watchdog Timer expired. “1”: Enable / “0”: Disable.
2	THERMWDT_EXP	Interrupt of Battery Temperature Watchdog Timer expired. “1”: Enable / “0”: Disable.
1	TMP_TRNS	Interrupt of the Battery Temperature range transition. “1”: Enable / “0”: Disable.
0	CHG_TRNS	Interrupt of Charger-State transition. “1”: Enable / “0”: Disable.

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8.5.102. INT6_SET

2nd Level Interrupt Setting 6 (Charger)

Command Code: 6Eh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	VBUS_UCD_PORT_DET	Interrupt of USB Port contact detected on the VBUS side. “1”: Enable / “0”: Disable.
12	VBUS_UCD_UCHG_DET	Interrupt of USB Charger detected on the VBUS side. “1”: Enable / “0”: Disable.
11	VBUS_UCD_URID_RMV	Interrupt of USB ID contact removed on the VBUS side. “1”: Enable / “0”: Disable.
10	VBUS_UCD_OTG_DET	Interrupt of USB OTG device detected on the VBUS side. “1”: Enable / “0”: Disable.
9	reserved	
8	VBUS_UCD_URID_MOD	Interrupt of USB ID resistance change on the VBUS side. “1”: Enable / “0”: Disable.
7	reserved	
6	reserved	
5	VCC_UCD_PORT_DET	Interrupt of USB Port contact detected on the VCC side. “1”: Enable / “0”: Disable.
4	VCC_UCD_UCHG_DET	Interrupt of USB Charger detected on the VCC side. “1”: Enable / “0”: Disable.
3	VCC_UCD_URID_RMV	Interrupt of USB ID contact removed on the VCC side. “1”: Enable / “0”: Disable.
2	VCC_UCD_OTG_DET	Interrupt of USB OTG device detected on the VCC side. “1”: Enable / “0”: Disable.
1	reserved	
0	VCC_UCD_URID_MOD	Interrupt of USB ID resistance change on the VCC side. “1”: Enable / “0”: Disable.

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8.5.103. INT7_SET

2nd Level Interrupt Setting 7 (SAR-ADC)

Command Code: 6Fh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	PROCHOT_DET	Interrupt of PROCHOT# asserted. “1”: Enable / “0”: Disable.
14	PROCHOT_RES	Interrupt of PROCHOT# de-asserted. “1”: Enable / “0”: Disable.
13	reserved	
12	reserved	
11	VACP_DET	Interrupt of VACP detect. “1”: Enable / “0”: Disable.
10	VACP_RES	Interrupt of VACP removal. “1”: Enable / “0”: Disable.
9	VACP_TH_DET	Interrupt Input Voltage (ACP) Voltage > VACP_TH_SET. “1”: Enable / “0”: Disable.
8	VACP_TH_RES	Interrupt Input Voltage (ACP) Voltage <= VACP_TH_SET. “1”: Enable / “0”: Disable.
7	IACP_TH_DET	Interrupt Input Current (between ACP-ACN) > IACP_TH_SET. “1”: Enable / “0”: Disable.
6	IACP_THE_RES	Interrupt Input Current (between ACP-ACN) <= IACP_TH_SET. “1”: Enable / “0”: Disable.
5	THERM_TH_DET	Interrupt TSENSE Voltage > THERM_TH_SET. “1”: Enable / “0”: Disable.
4	THERM_TH_RES	Interrupt TSENSE Voltage <= THERM_TH_SET. “1”: Enable / “0”: Disable.
3	IBATM_TH_DET	Interrupt Battery Current (Dis-charge) > IBATM_TH_SET. “1”: Enable / “0”: Disable.
2	IBATM_TH_RES	Interrupt Battery Current (Dis-charge) <= IBATM_TH_SET. “1”: Enable / “0”: Disable.
1	IBATP_TH_DET	Interrupt Battery Current (Charge) > IBATP_TH_SET. “1”: Enable / “0”: Disable.
0	IBATP_TH_RES	Interrupt Battery Current (Charge) <= IBATP_TH_SET. “1”: Enable / “0”: Disable.

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8.5.104. INT0_STATUS

1st Level Interrupt Status

Command Code: 70h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	INT7_STATUS	2nd Level Interrupt 7 (SAR-ADC) Status. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
6	INT6_STATUS	2nd Level Interrupt 6 (Charger) Status. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
5	INT5_STATUS	2nd Level Interrupt 5 (Charger) Status. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
4	INT4_STATUS	2nd Level Interrupt 4 (VSYS) Status. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
3	INT3_STATUS	2nd Level Interrupt 3 (Battery) Status. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
2	INT2_STATUS	2nd Level Interrupt 2 (VCC) Status. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
1	INT1_STATUS	2nd Level Interrupt 1 (VBUS) Status. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
0	INT0_STATUS	1st Level Interrupt Status. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.

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8.5.105. INT1_STATUS

2nd Level Interrupt Status 1 (VBUS)

Command Code: 71h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	VBUS_RBUV_DET	Interrupt status of entering to VBUS reverse buck boost voltage low. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
14	VBUS_RBUV_RES	Interrupt status of exit from VBUS reverse buck boost voltage low. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VBUS_TH_DET	Interrupt status VBUS Voltage > VBUS_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
8	VBUS_TH_RES	Interrupt status VBUS Voltage <= VBUS_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
7	reserved	
6	VBUS_IIN_MOD	Interrupt status of VBUS input current-limit modified. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
5	VBUS_OV_DET	Interrupt status of VBUS over voltage detected. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
4	VBUS_OV_RES	Interrupt status of VBUS over voltage resumed. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
3	VBUS_CLPS_DET	Interrupt status of entering to VBUS Anti-collapse operation. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
2	VBUS_CLPS RES	Interrupt status of exit from VBUS Anti-collapse operation. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
1	VBUS_DET	Interrupt status of VBUS detect. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
0	VBUS_RES	Interrupt status of VBUS removal. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.

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8.5.106. INT2_STATUS

2nd Level Interrupt Status 2 (VCC)

Command Code: 72h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	VCC_RBUV_DET	Interrupt status of entering to VCC reverse buck boost voltage low. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
14	VCC_RBUV_RES	Interrupt status of exit from VCC reverse buck boost voltage low. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VCC_TH_DET	Interrupt status VCC Voltage > VCC_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
8	VCC_TH_RES	Interrupt status VCC Voltage <= VCC_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
7	reserved	
6	VCC_IIN_MOD	Interrupt status of VCC/VACP input current-limit modified. “1”: Event occurred / “0”: No event. “1-Write”: Status clear. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
5	VCC_OVP_DET	Interrupt status of VCC over voltage detected. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
4	VCC_OVP_RES	Interrupt status of VCC over voltage resumed. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
3	VCC_CLPS_DET	Interrupt status of entering to VCC/VACP Anti-collapse operation. “1”: Event occurred / “0”: No event. “1-Write”: Status clear. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
2	VCC_CLPS_RES	Interrupt status of exit from VCC/VACP Anti-collapse operation. “1”: Event occurred / “0”: No event. “1-Write”: Status clear. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
1	VCC_DET	Interrupt status of VCC detect. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
0	VCC_RES	Interrupt status of VCC removal. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.

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8.5.107. INT3_STATUS

2nd Level Interrupt Status 3 (Battery)

Command Code: 73h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TH_DET	Interrupt status of the thermistor detected. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
14	TH_RMV	Interrupt status of the thermistor removal. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
13	reserved	
12	reserved	
11	TMP_OUT_DET	Interrupt status of the thermistor out of the charging range. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
10	TMP_OUT_RES	Interrupt status of the thermistor in to the charging range. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
9	VBAT_TH_DET	Interrupt status VBAT Voltage > VBAT_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
8	VBAT_TH_RES	Interrupt status VBAT Voltage <= VBAT_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
7	IBAT_SHORT_DET	Interrupt status of Battery over current detected. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
6	IBAT_SHORT_RES	Interrupt status of Battery over current resumed. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
5	VBAT_OV_DET	Interrupt status of VBAT over voltage detected. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
4	VBAT_OV_RES	Interrupt status of VBAT over voltage resumed. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
3	BAT_ASSIST_DET	Interrupt status of Entering to Battery-assist mode. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
2	BAT_ASSIST_RES	Interrupt status of Exiting from Battery-assist mode. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
1	reserved	
0	reserved	

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8.5.108. INT4_STATUS

2nd Level Interrupt Status 4 (VSYS)

Command Code: 74h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VSYS_TH_DET	Interrupt status VSYS Voltage > VSYS_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
8	VSYS_TH_RES	Interrupt status VSYS Voltage <= VSYS_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
7	reserved	
6	reserved	
5	VSYS_OV_DET	Interrupt status of VSYS over voltage detected. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
4	VSYS_OV_RES	Interrupt status of VSYS over voltage resumed. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
3	VSYS_SHT_DET	Interrupt status of VSYS short circuit detected. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
2	VSYS_SHT_RES	Interrupt status of VSYS short circuit resumed. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
1	VSYS_UV_DET	Interrupt status of VSYS under voltage detected. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
0	VSYS_UV_RES	Interrupt status of VSYS under voltage resumed. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.

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8.5.109. INT5_STATUS

2nd Level Interrupt Status 5 (Charger)

Command Code: 75h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	OTP_LOAD_DONE	Interrupt status of OTP load done. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
12	PWR_ON	Interrupt status of Power-on. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
11	EXTIADP_TRNS	Interrupt status of IADP voltage range transition. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
10	reserved	
9	EXTIADP_TH_DET	Interrupt status of IADP (Input current Limit setting pin) voltage > EXTIADP_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
8	EXIADP_TH_RES	Interrupt status of IADP (Input current Limit setting pin) voltage <= EXTIADP_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
7	BAT_MNT_DET	Interrupt status of entering to Battery Maintenance charging. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
6	BAT_MNT_RES	Interrupt status of exit from Battery Maintenance charging. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
5	TSD_DET	Interrupt status of the TSD detected. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
4	TSD_RES	Interrupt status of the TSD resumed. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
3	CHGWDT_EXP	Interrupt status of Charger Watchdog Timer expired. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
2	THERMWDT_EXP	Interrupt status of Battery Temperature Watchdog Timer expired. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
1	TMP_TRNS	Interrupt status of Temperature range transition. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
0	CHG_TRNS	Interrupt status of Charger-State transition. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.

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8.5.110. INT6_STATUS

2nd Level Interrupt Status 6 (Charger)

Command Code: 76h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	VBUS_UCD_PORT_DET	Interrupt status of USB Port contact detected on the VBUS side. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
12	VBUS_UCD_UCHG_DET	Interrupt status of USB Charger detected on the VBUS side. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
11	VBUS_UCD_URID_RMV	Interrupt status of USB ID contact removed on the VBUS side. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
10	VBUS_UCD_OTG_DET	Interrupt status of USB OTG device detected on the VBUS side. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
9	reserved	
8	VBUS_UCD_URID_MOD	Interrupt status of USB ID resistance change on the VBUS side. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
7	reserved	
6	reserved	
5	VCC_UCD_PORT_DET	Interrupt status of USB Port contact detected on the VCC side. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
4	VCC_UCD_UCHG_DET	Interrupt status of USB Charger detected on the VCC side. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
3	VCC_UCD_URID_RMV	Interrupt status of USB ID contact removed on the VCC side. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
2	VCC_UCD_OTG_DET	Interrupt status of USB OTG device detected on the VCC side. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
1	reserved	
0	VCC_UCD_URID_MOD	Interrupt status of USB ID resistance change on the VCC side. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.

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8.5.111. INT7_STATUS

2nd Level Interrupt Status 7 (SAR-ADC)

Command Code: 77h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	PROCHOT_DET	Interrupt status of PROCHOT# asserted. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
14	PROCHOT_RES	Interrupt status of PROCHOT# de-asserted. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
13	reserved	
12	reserved	
11	VACP_DET	Interrupt status of VACP detect. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
10	VACP_RES	Interrupt status of VACP removal. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
9	VACP_TH_DET	Interrupt status Input Voltage (ACP) Voltage > VADP_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
8	VACP_TH_RES	Interrupt status Input Voltage (ACP) Voltage <= VADP_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
7	IACP_TH_DET	Interrupt status Input Current (between ACP-ACN) > IADP_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
6	IACP_THE_RES	Interrupt status Input Current (between ACP-ACN) <= IADP_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
5	THERM_TH_DET	Interrupt status TSENSE Voltage > THERM_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
4	THERM_TH_RES	Interrupt status TSENSE Voltage <= THERM_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
3	IBATM_TH_DET	Interrupt status Battery Current (Dis-charge) > IBATM_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
2	IBATM_TH_RES	Interrupt status Battery Current (Dis-charge) <= IBATM_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
1	IBATP_TH_DET	Interrupt status Battery Current (Charge) > IBATP_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
0	IBATP_TH_RES	Interrupt status Battery Current (Charge) <= IBATP_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.

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8.5.112. REG0

Reserved Register 0 (for future use)

Command Code: 78h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	RESERVE_REG0[15]	Reserved Register 0 (for future use)
14	RESERVE_REG0[14]	
13	RESERVE_REG0[13]	
12	RESERVE_REG0[12]	
11	RESERVE_REG0 [11]	
10	RESERVE_REG0 [10]	
9	RESERVE_REG0 [9]	
8	RESERVE_REG0 [8]	
7	RESERVE_REG0 [7]	
6	RESERVE_REG0 [6]	
5	RESERVE_REG0 [5]	
4	RESERVE_REG0 [4]	
3	RESERVE_REG0 [3]	
2	RESERVE_REG0 [2]	
1	RESERVE_REG0 [1]	
0	RESERVE_REG0 [0]	

8.5.113. REG1

Reserved Register 1 (for future use)

Command Code: 79h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	RESERVE_REG1[15]	Reserved Register 1 (for future use)
14	RESERVE_REG1[14]	
13	RESERVE_REG1[13]	
12	RESERVE_REG1[12]	
11	RESERVE_REG1[11]	
10	RESERVE_REG1[10]	
9	RESERVE_REG1[9]	
8	RESERVE_REG1[8]	
7	RESERVE_REG1[7]	
6	RESERVE_REG1[6]	
5	RESERVE_REG1[5]	
4	RESERVE_REG1[4]	
3	RESERVE_REG1[3]	
2	RESERVE_REG1[2]	
1	RESERVE_REG1[1]	
0	RESERVE_REG1[0]	

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8.5.114. OTPREG0

Input current limit degradation setting. For ditails, please see 8.5.6. CUR_ILIM_VAL.

Command Code: 7Ah
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	RESERVE_OTPREG0[15]	Reserved OTP-loaded Register 0 (for future use)
14	RESERVE_OTPREG0[14]	
13	RESERVE_OTPREG0[13]	
12	RESERVE_OTPREG0[12]	
11	ILIM_DECREASE[11]	Input current limit degradation setting when anti-collapse occurs.
10	ILIM_DECREASE[10]	
9	ILIM_DECREASE[9]	
8	ILIM_DECREASE[8]	
7	ILIM_DECREASE[7]	
6	ILIM_DECREASE[6]	
5	ILIM_DECREASE[5]	
4	ILIM_DECREASE[4]	
3	ILIM_DECREASE[3]	
2	ILIM_DECREASE[2]	
1	ILIM_DECREASE[1]	
0	ILIM_DECREASE[0]	

8.5.115. OTPREG1

Reserved OTP-loaded Register 1 (for future use)

Command Code: 7Bh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	RESERVE_OTPREG1[15]	Reserved OTP-loaded Register 1 (for future use)
14	RESERVE_OTPREG1[14]	
13	RESERVE_OTPREG1[13]	
12	RESERVE_OTPREG1[12]	
11	RESERVE_OTPREG1[11]	
10	RESERVE_OTPREG1[10]	
9	RESERVE_OTPREG1[9]	
8	RESERVE_OTPREG1[8]	
7	RESERVE_OTPREG1[7]	
6	RESERVE_OTPREG1[6]	
5	RESERVE_OTPREG1[5]	
4	RESERVE_OTPREG1[4]	
3	RESERVE_OTPREG1[3]	
2	RESERVE_OTPREG1[2]	
1	RESERVE_OTPREG1[1]	
0	RESERVE_OTPREG1[0]	

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8.5.116. SMBREG

Power Save Mode Setting.

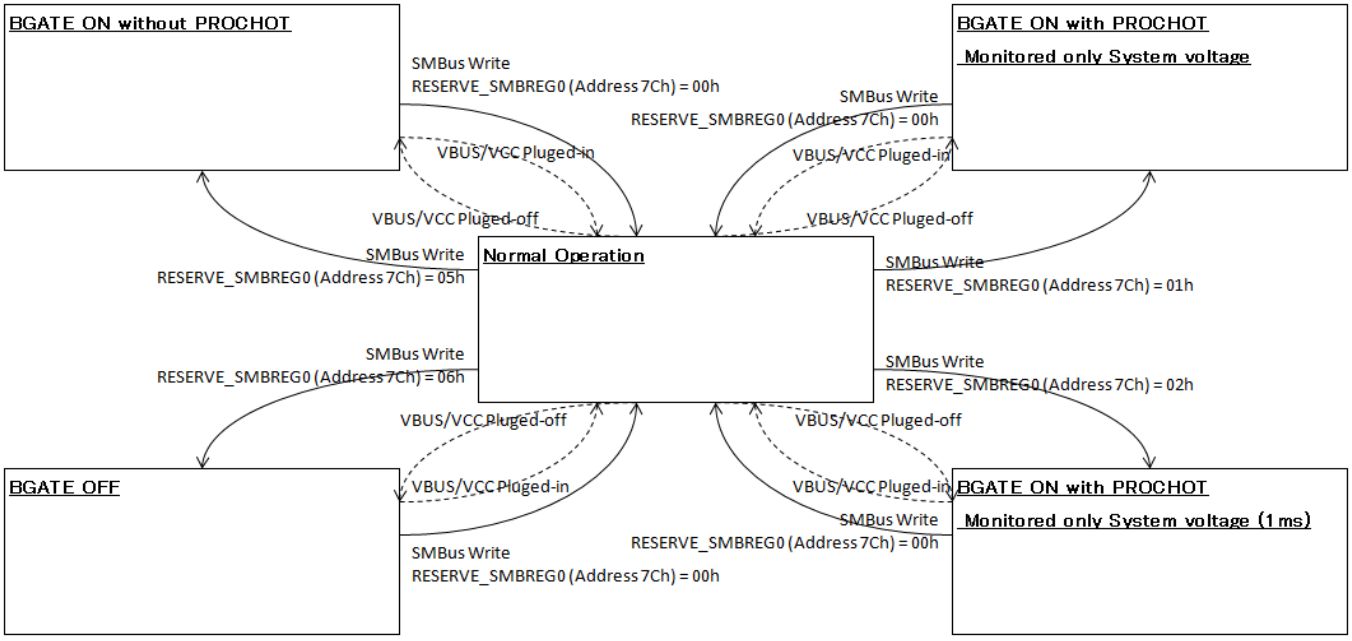
Command Code: 7Ch
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	SMBREG[15]	Reserved SMBus Clock Domain Register (for future use)
14	SMBREG[14]	
13	SMBREG[13]	
12	SMBREG[12]	
11	SMBREG[11]	
10	SMBREG[10]	
9	SMBREG[9]	
8	SMBREG[8]	
7	SMBREG[7]	
6	SMBREG[6]	
5	SMBREG[5]	
4	SMBREG[4]	
3	SMBREG[3]	
2	POWER_SAVE_MODE[2]	Power Save Mode Setting. 0h: Normal Operation 1h: BGATE ON with PROCHOT# Monitored only System voltage/ 2h: BGATE ON with PROCHOT# Monitored only System voltage (1ms)/ 5h: BGATE ON without PROCHOT#// 6h: BGATE OFF/ Other: reserved.
1	POWER_SAVE_MODE[1]	
0	POWER_SAVE_MODE[0]	

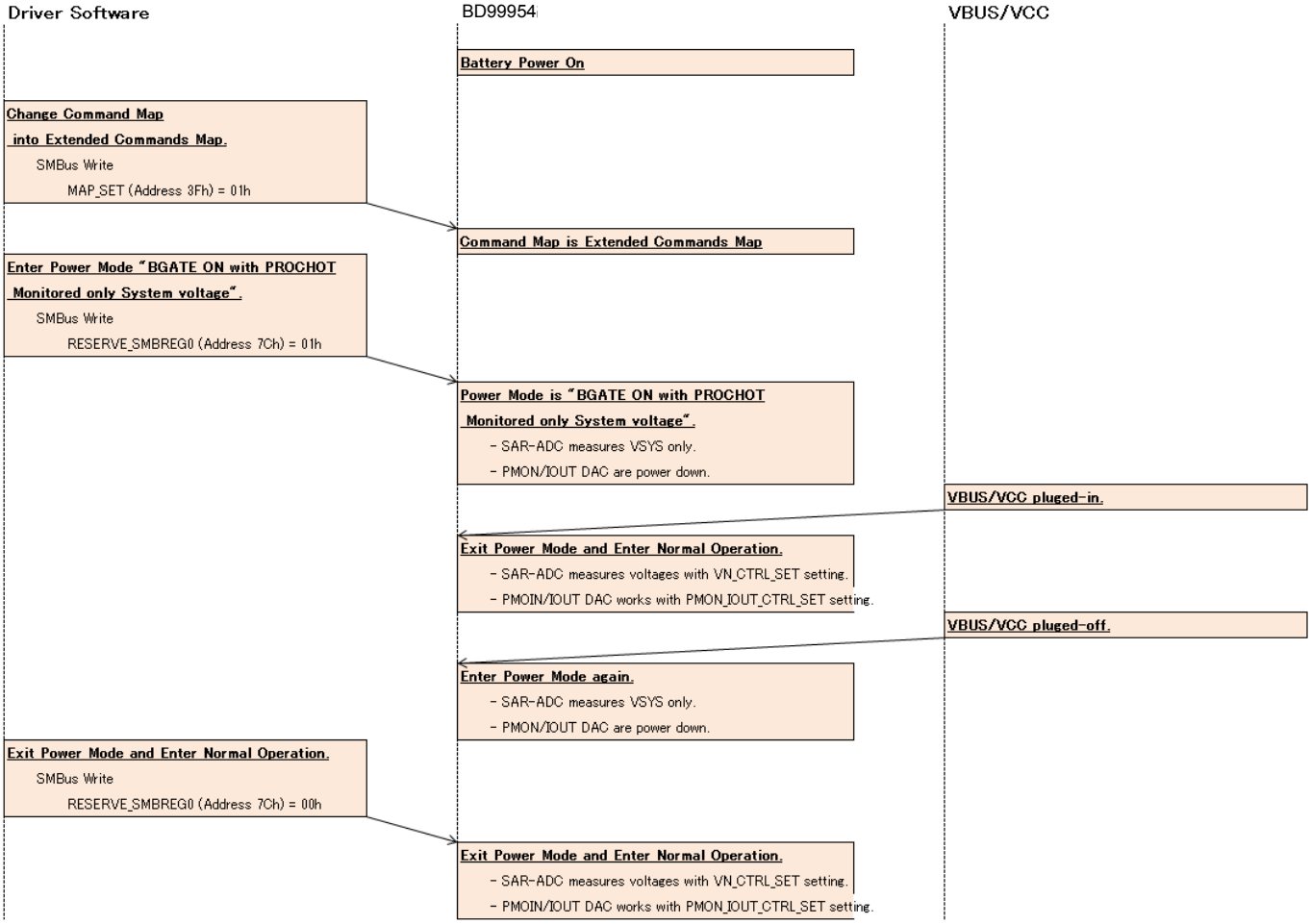
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BD99954 enters into 4 power modes by SMBus writing RESERVE_SMBREG0SMBREG.POWER_SAVE_MODE[2:0] register. And BD99954 exits from a power mode by SMBus clearing RESERVE_SMBREG0SMBREG.POWER_SAVE_MODE[2:0] register.

If BD99954 is in a power mode, BD99954 exits from power mode automatically by VBUS/VCC plugged-in and goes back to power mode automatically by VBUS/VCC plugged-off.

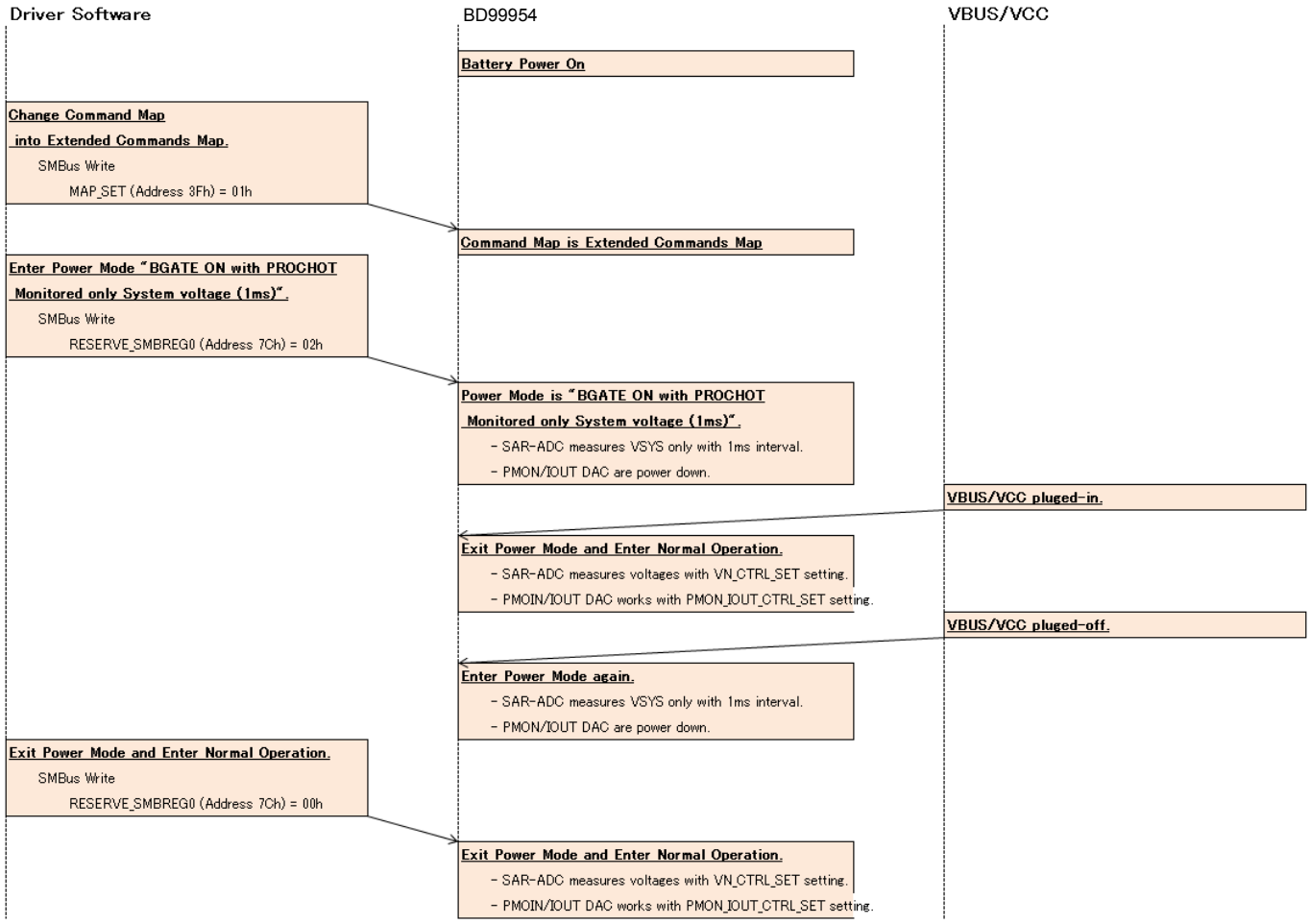


POWER_SAVE_MODE[2:0]=1h: (BGATE ON with PROCHOT# Monitored only System voltage) sample operation flow.



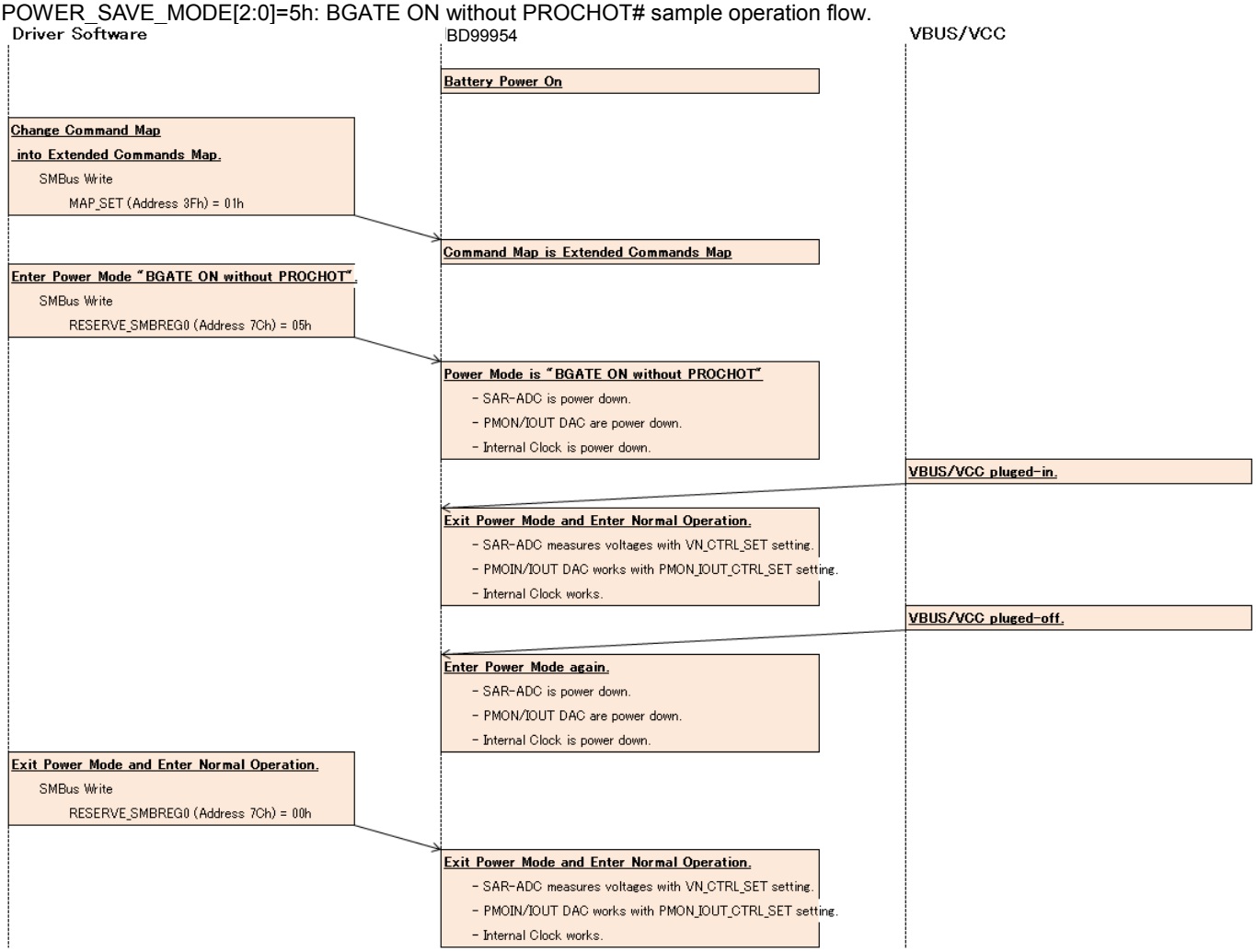
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POWER_SAVE_MODE[2:0] =2h: BGATE ON with PROCHOT# Monitored only System voltage (1ms interval) sample operation flow.



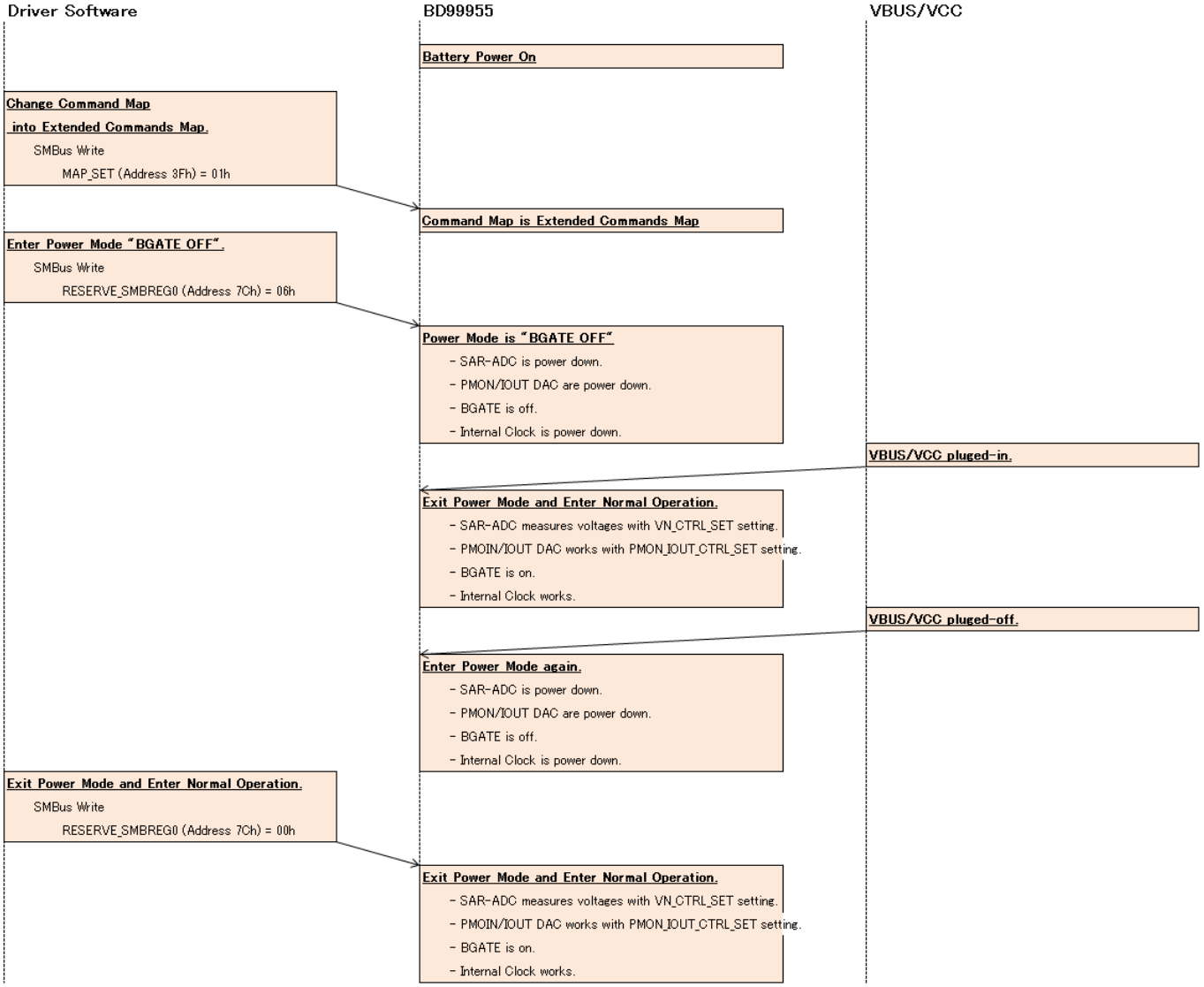
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POWER_SAVE_MODE[2:0]=5h: BGATE ON without PROCHOT# sample operation flow.



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POWER_SAVE_MODE[2:0]=6h: BGATE OFF sample operation flow.



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8.5.117. DEBUG_MODE_SET

Debug Mode Setting

Command Code: 7Fh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	DEBUG_MODE_SET[15]	Debug Mode Setting
14	DEBUG_MODE_SET[14]	
13	DEBUG_MODE_SET[13]	
12	DEBUG_MODE_SET[12]	
11	DEBUG_MODE_SET[11]	
10	DEBUG_MODE_SET[10]	
9	DEBUG_MODE_SET[9]	
8	DEBUG_MODE_SET[8]	
7	DEBUG_MODE_SET[7]	
6	DEBUG_MODE_SET[6]	
5	DEBUG_MODE_SET[5]	
4	DEBUG_MODE_SET[4]	
3	DEBUG_MODE_SET[3]	
2	DEBUG_MODE_SET[2]	
1	DEBUG_MODE_SET[1]	
0	DEBUG_MODE_SET[0]	

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8.6. Resister Default Value

Register Address	Address Name	Read/ Write	OTP	Bit																OTP/POR Value(HEX)	OTP/POR Value(DEC)	Unit [V,mA,min]
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
00h	CHGSTM_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
01h	VBAT/VSYS_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
02h	VBUS/VCC_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
03h	CHGOP_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
04h	WDT_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
05h	CUR_ILIM_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
06h	SEL_ILIM_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
07h	IBUS_LIM_SET	R/W	Yes	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	05C0	1472	mA
08h	ICC_LIM_SET	R/W	Yes	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	05C0	1472	mA
09h	IOTG_LIM_SET	R/W	Yes	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	05E0	1504	mA
0Ah	VIN_CTRL_SET	R/W	Yes	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	00E0	-	HEX
0Bh	CHGOP_SET1	R/W	Yes	0	1	1	0	1	1	0	0	0	1	1	0	1	0	0	0	6C68	-	HEX
0Ch	CHGOP_SET2	R/W	Yes	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	002E	-	HEX
0Dh	VBUSCLPS_TH_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	V
0Eh	VCCCLPS_TH_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	V
0Fh	CHGWDT_SET	R/W	Yes	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	3010	192,16	min
10h	BATTWDT_SET	R/W	Yes	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0630	24,48	min
11h	VSYSREG_SET	R/W	Yes	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	2300	8.96	V
12h	VSYSVAL_THH_SET	R/W	Yes	0	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	1580	5.504	V
13h	VSYSVAL_THL_SET	R/W	Yes	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0	1340	4.928	V
14h	ITRICH_SET	R/W	Yes	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0100	256	mA
15h	IPRECH_SET	R/W	Yes	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0100	256	mA
16h	ICHG_SET	R/W	Yes	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0A00	2560	mA
17h	ITERM_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	mA
18h	VPRECHG_TH_SET	R/W	Yes	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0800	2.048	V
19h	VRBOOST_SET	R/W	Yes	0	0	0	1	0	0	1	1	1	1	0	0	0	0	0	0	13C0	5.056	V
1Ah	VFASTCHG_REG_SET1	R/W	Yes	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	20D0	8.4	V
1Bh	VFASTCHG_REG_SET2	R/W	Yes	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	20D0	8.4	V
1Ch	VFASTCHG_REG_SET3	R/W	Yes	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	20D0	8.4	V
1Dh	VRECHG_SET	R/W	Yes	0	0	0	1	1	1	1	1	1	0	1	1	0	0	0	0	1FB0	8.112	V
1Eh	VBATOVP_SET	R/W	Yes	0	0	1	0	0	0	1	0	1	1	0	1	0	0	0	0	22D0	8.912	V
1Fh	IBATSHORT_SET	R/W	Yes	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000	16384	mA
20h	PROCHOT_CTRL_SET	R/W	Yes	0	1	0	0	0	1	0	1	0	0	0	1	1	0	0	1	4519	-	HEX
21h	PROCHOT_ICRIT_SET	R/W	Yes	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	2710	10000	mA
22h	PROCHOT_INORM_SET	R/W	Yes	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	1388	5000	mA
23h	PROCHOT_IDCHG_SET	R/W	Yes	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000	16384	mA
24h	PROCHOT_VSYS_SET	R/W	Yes	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0	1340	4.928	V
25h	PMON_IOUT_CTRL_SET	R/W	Yes	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	0	00AC	-	HEX
26h	PMON_DACIN_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
27h	IOUT_DACIN_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
28h	VCC_UCD_SET	R/W	Yes	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	00D0	-	HEX
29h	VCC_UCD_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
2Ah	VCC_IDD_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
2Bh	VCC_UCD_FCTRL_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
2Ch	VCC_UCD_FCTRL_EN	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX

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Register Address	Address Name	Read/ Write	OTP	Bit																OTP/POR Value(HEX)	OTP/POR Value(DEC)	Unit [V,mA,min]
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
30h	VBUS_UCD_SET	R/W	Yes	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	00D0	-	HEX
31h	VBUS_UCD_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
32h	VBUS_IDD_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
33h	VBUS_UCD_FCTRL_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
34h	VBUS_UCD_FCTRL_EN	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
38h	CHIP_ID	R	Yes	0	0	0	0	0	0	1	1	0	1	0	0	0	1	1	0	0346	-	HEX
39h	CHIP_REV	R	Yes	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0009	-	HEX
3Ah	IC_SET1	R/W	Yes	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0200	-	HEX
3Bh	IC_SET2																					
3Ch	SYSTEM_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
3Dh	SYSTEM_CTRL_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
3Eh	PROTECT_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
3Fh	MAP_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
40h	VM_CTRL_SET	R/W	Yes	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	13FF	-	HEX
41h	THERM_WINDOW_SET1	R/W	Yes	1	1	0	0	0	0	1	1	1	1	0	0	0	1	1	0	C3C6	5,2	℃
42h	THERM_WINDOW_SET2	R/W	Yes	1	0	1	1	1	0	1	1	1	0	1	1	1	1	1	0	BBBE	13,10	℃
43h	THERM_WINDOW_SET3	R/W	Yes	1	0	0	1	1	0	1	1	1	0	0	1	1	1	1	0	9B9E	45,42	℃
44h	THERM_WINDOW_SET4	R/W	Yes	1	0	0	0	1	1	1	0	1	0	0	1	0	0	0	1	8E91	58,55	℃
45h	THERM_WINDOW_SET5	R/W	Yes	1	0	0	1	0	1	1	0	1	0	0	1	1	0	0	1	9699	50,47	℃
46h	IBATP_TH_SET	R/W	Yes	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1	0	1656	5718	mA
47h	IBATM_TH_SET	R/W	Yes	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000	16384	mA
48h	VBAT_TH_SET	R/W	Yes	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1800	6.144	V
49h	THERM_TH_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0032	150	℃
4Ah	IACP_TH_SET	R/W	Yes	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	1388	5000	mA
4Bh	VACP_TH_SET	R/W	Yes	0	0	0	0	1	1	1	0	1	1	0	1	1	0	0	0	0ED8	3.8	V
4Ch	VBUS_TH_SET	R/W	Yes	0	0	0	0	1	1	1	0	1	1	0	1	1	0	0	0	0ED8	3.8	V
4Dh	VCC_TH_SET	R/W	Yes	0	0	0	0	1	1	1	0	1	1	0	1	1	0	0	0	0ED8	3.8	V
4Eh	VSYS_TH_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	V
4Fh	EXTIADP_TH_SET	R/W	Yes	0	0	0	0	0	1	1	1	0	1	1	1	0	1	1	1	0777	1.911	V
50h	IBATP_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
51h	IBATP_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
52h	IBATM_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
53h	IBATM_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
54h	VBAT_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
55h	VBAT_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
56h	THERM_VAL	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
57h	VTH_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
58h	IACP_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
59h	IACP_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Ah	VACP_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Bh	VACP_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Ch	VBUS_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Dh	VBUS_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Eh	VCC_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Fh	VCC_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
60h	VSYS_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX

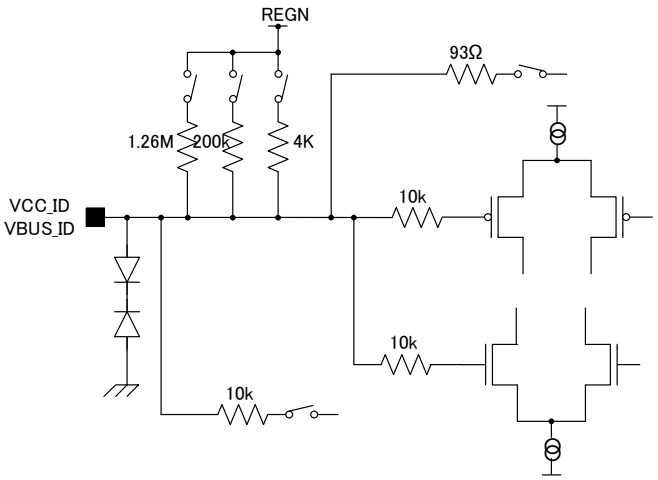
* Product structure: Silicon monolithic integrated circuit. ** This product is not designed to protect against radioactive rays.
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Register Address	Address Name	Read/ Write	OTP	Bit																OTP/POR Value(HEX)	OTP/POR Value(DEC)	Unit [V,mA,min]
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
61h	VSYS_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
62h	EXTIADP_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
63h	EXTIADP_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
64h	VACPCLPS_TH_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	V
68h	INT0_SET	R/W	Yes	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	00FF	-	HEX
69h	INT1_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Ah	INT2_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Bh	INT3_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Ch	INT4_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Dh	INT5_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Eh	INT6_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Fh	INT7_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
70h	INT0_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
71h	INT1_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
72h	INT2_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
73h	INT3_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
74h	INT4_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
75h	INT5_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
76h	INT6_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
77h	INT7_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
78h	RESERVE_REG0	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
79h	RESERVE_REG1	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
7Ah	OTPREG0	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	mA
7Bh	OTPREG1	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
7Ch	RESERVE_SMBREG0	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
7Dh	(reserved)	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
7Eh	(reserved)	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
7Fh	DEBUG_MODE_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX

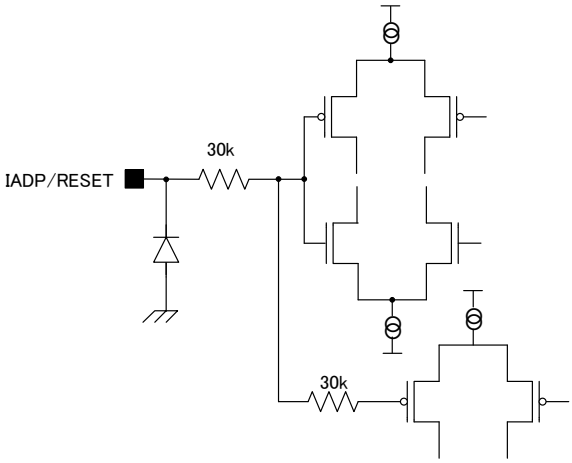
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9. I/O Equivalent circuit diagram

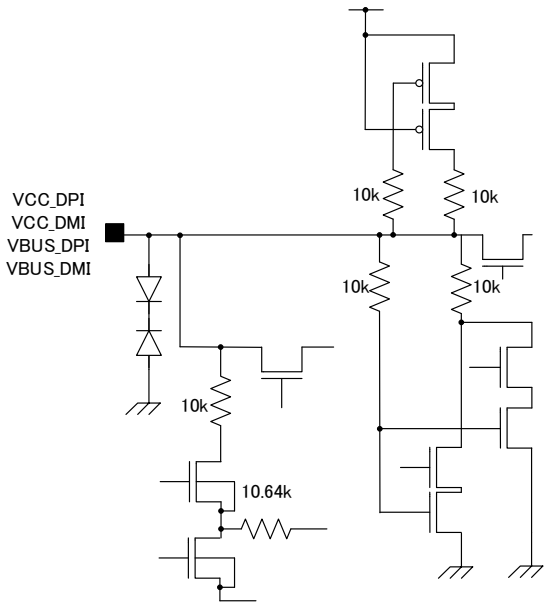
VCC_ID, VBUS_ID



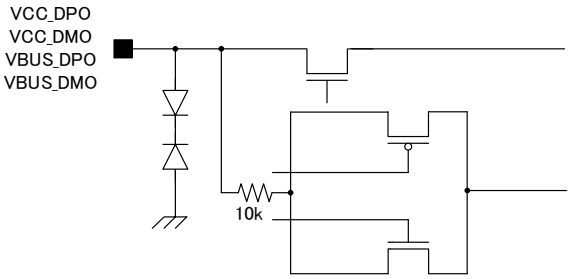
IADP/RESET



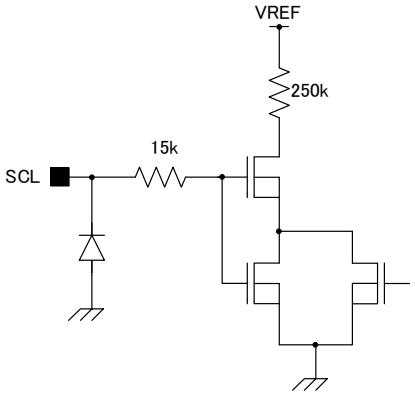
VCC_DPI, VCC_DMI, VBUS_DPI, VBUS_DMI



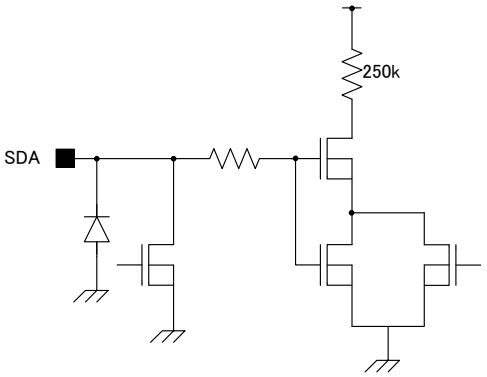
VCC_DPO, VCC_DMO, VBUS_DPO, VBUS_DMO



SCL



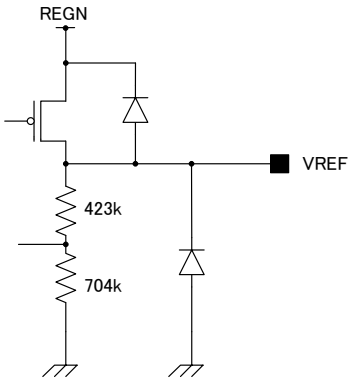
SDA



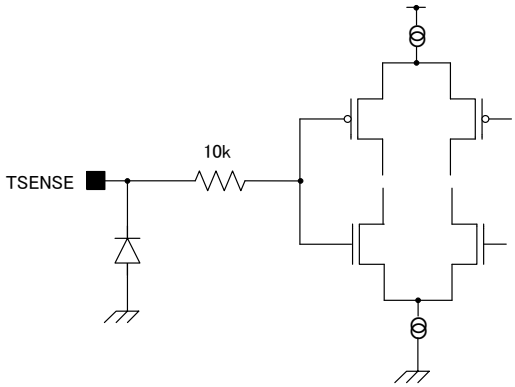
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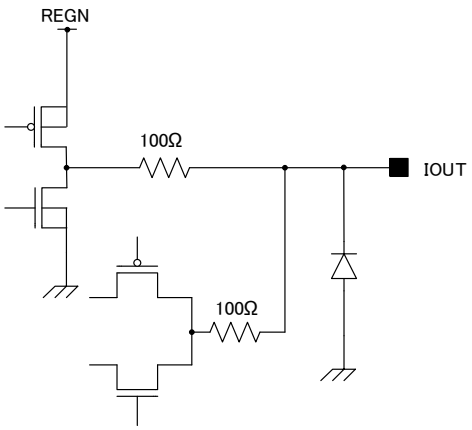
VREF



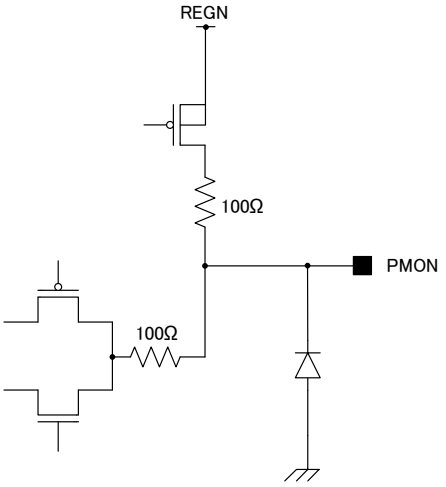
TSENSE



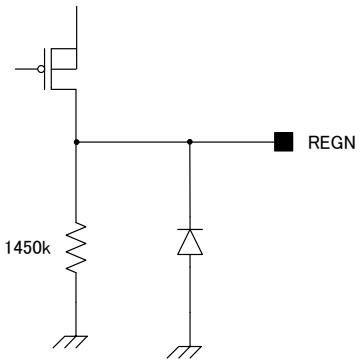
IOUT



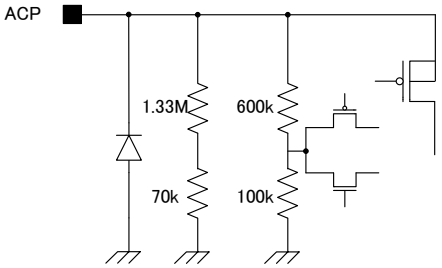
PMON



REGN



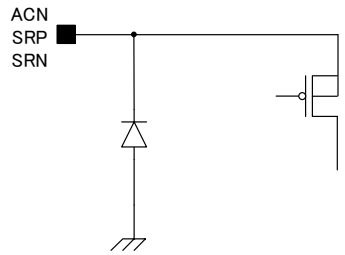
ACP



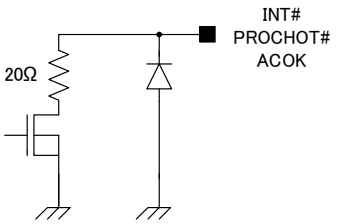
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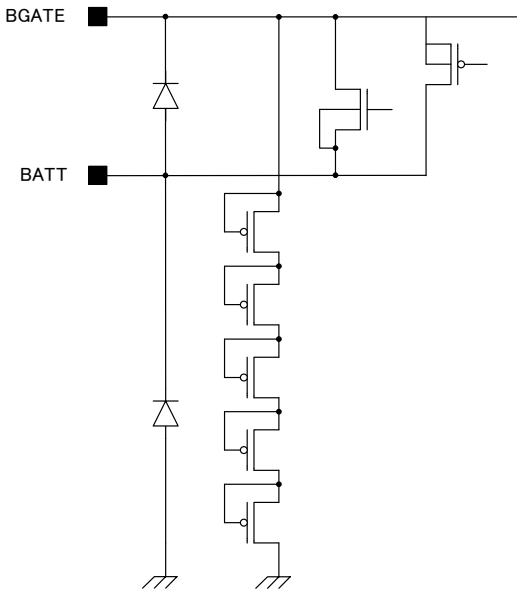
ACN, SRP, SRN



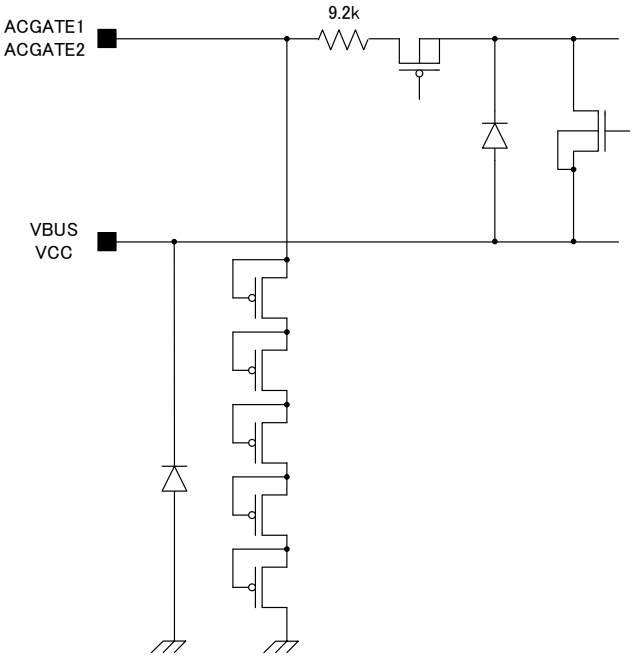
INT#, PROCHOT#, ACOK



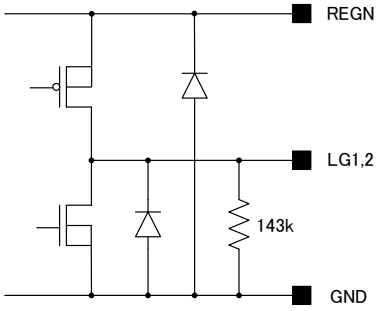
BGATE, BATT



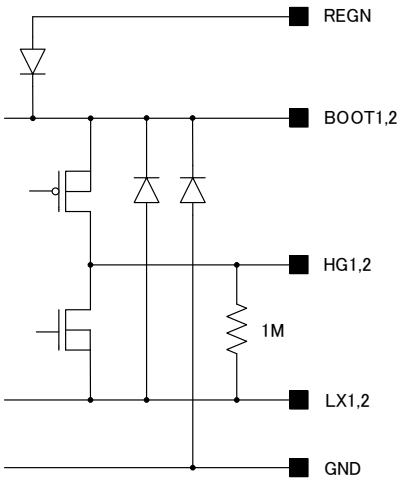
ACGATE1, ACGATE2, VBUS, VCC



LG1, LG2

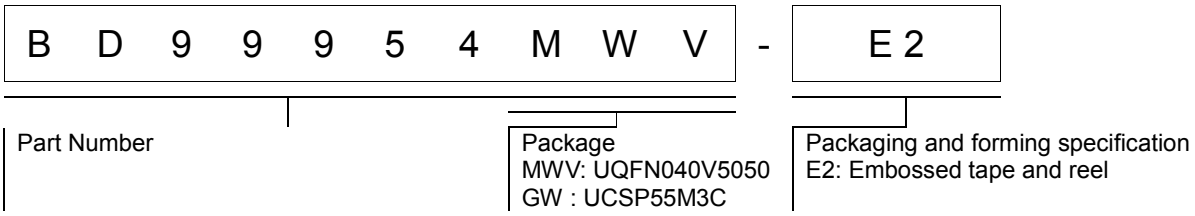


BOOT1, BOOT2, HG1, HG2, LX1, LX2

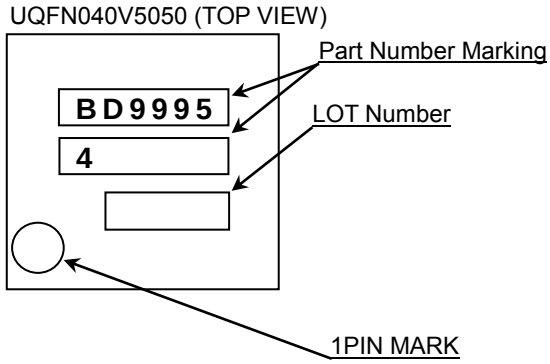


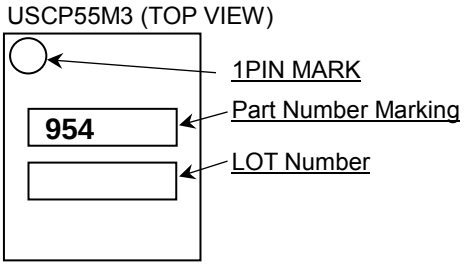
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10. Ordering Information



11. Marking Diagrams





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12. Physical Dimension Tape and Reel Information

Package Name	UQFN040V5050

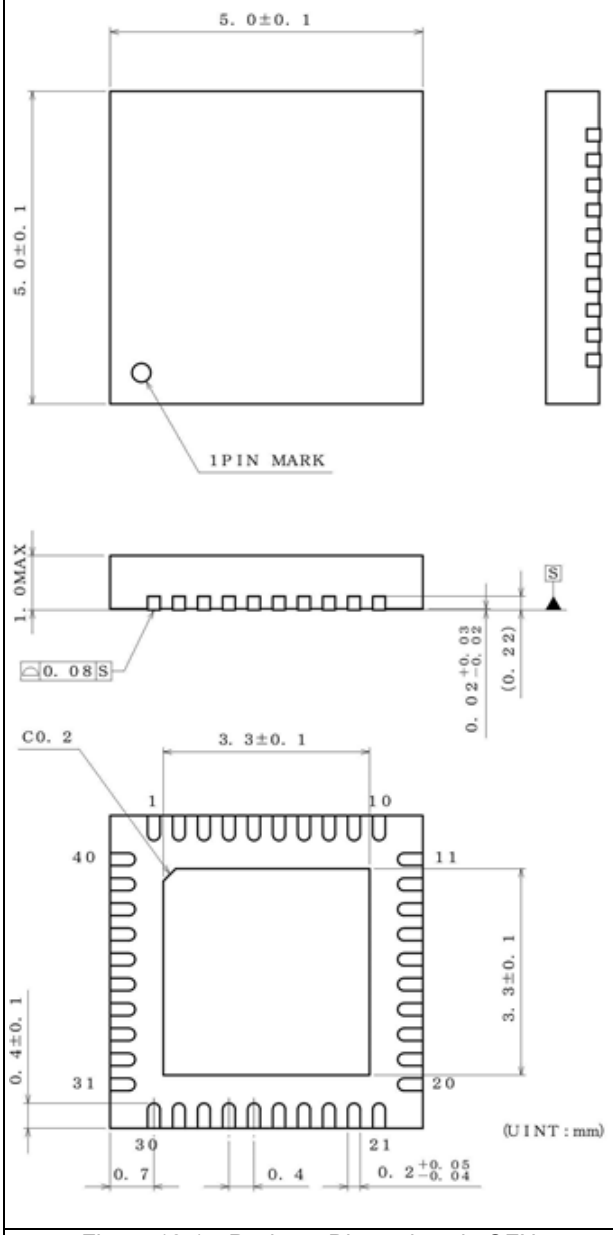


Figure 12-1 Package Dimensions in QFN

Package Name	UCSP55M3C

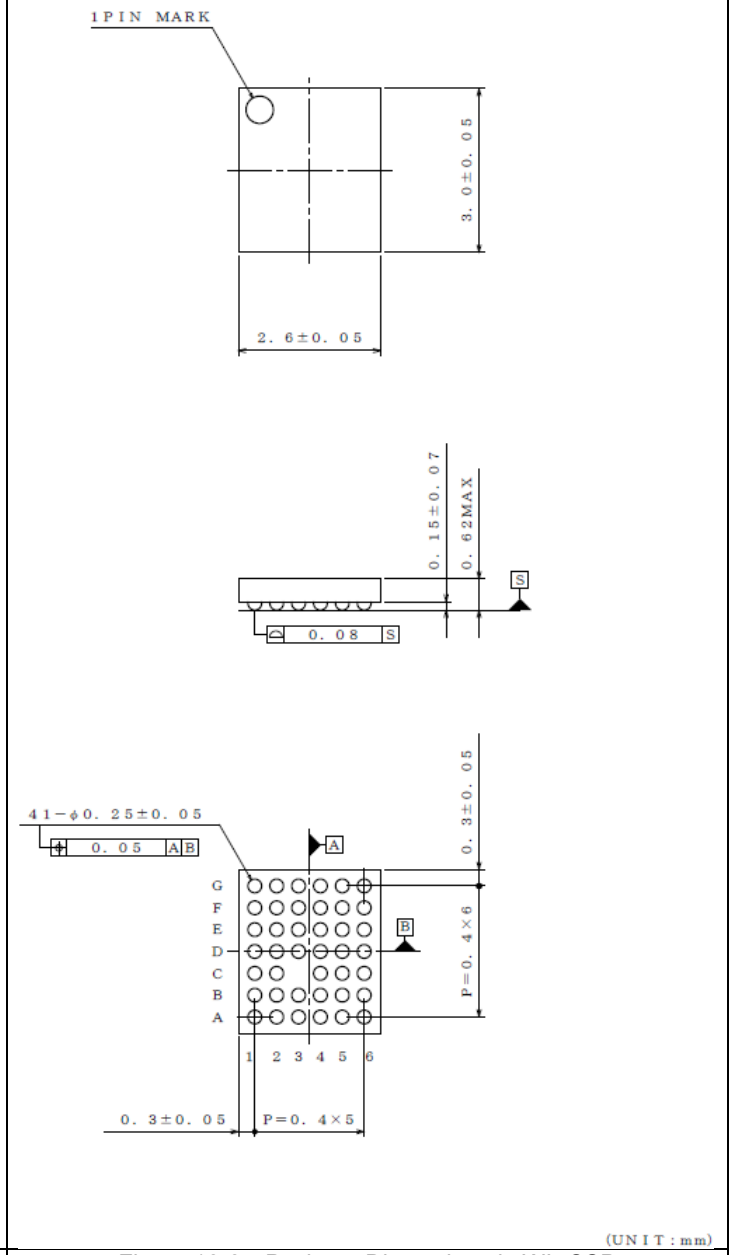


Figure 12-2 Package Dimensions in WL-CSP

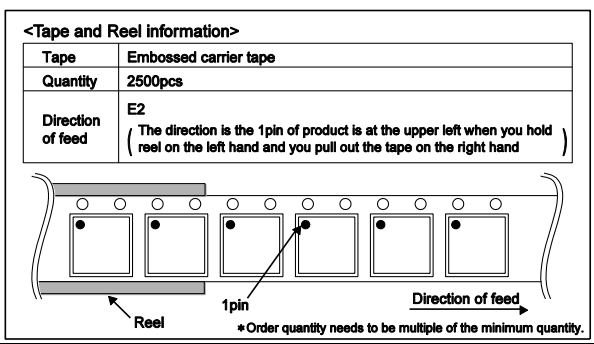


Figure 12-3 Tape and Reel Information in QFN

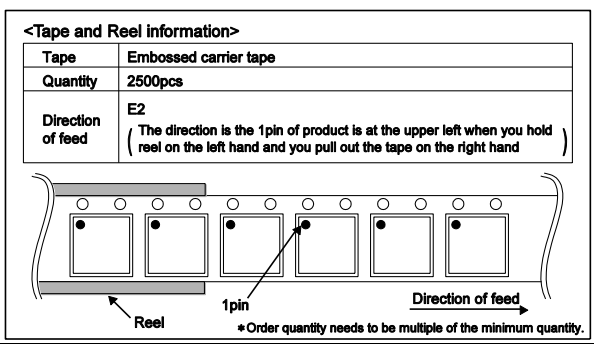


Figure 12-4 Tape and Reel Information in WL-CSP

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13. Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

OR

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

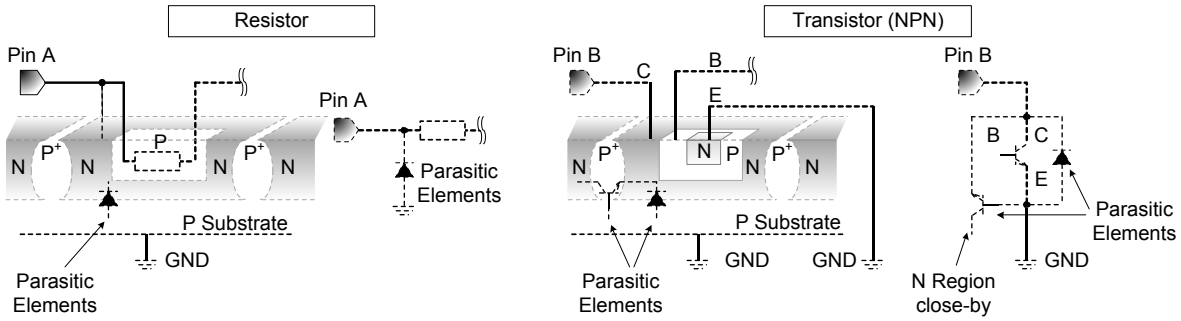


Figure xx. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

17. Disturbance light (only BD99954GW**)**

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

18. Thermal Pad (only BD99954MWV**)**

Thermal pad connect GND terminal or open.

19. Power Path Sequece

This product is capable of turning both VCC and VBUS power paths ON simultaneously.
Please immediately turn the simultaneous power path ON if one of the VCC or VBUS port has been disconnected and simultaneous ON is not needed.
If the simultaneous power path is not turned off immediately, and a new device is connected to the disconnected port, there is a possibility that this device gets damaged.
In that case, ROHM cannot assume responsibility for the damage.

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Operational Notes – continued

20. VBUS overshoot

There is possibility of voltage overshoot on VCC or VBUS inputs depending on settings and conditions for the following parameters: input voltage (VBUS and VCC), input voltage for IADP (set by external voltage divider), total system capacitance and respective ESR.

Please refer carefully to this datasheet and the separate application notes when making selection of those parameters and register settings to properly match your design.

* Product structure: Silicon monolithic integrated circuit. ** This product is not designed to protect against radioactive rays.
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Revision History

Revision Number	Description	Revision Date
001	Initial release.	12. Jul. 2017

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

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