# TLV62569 采用 SOT 封装的 2A 高效同步降压转换器

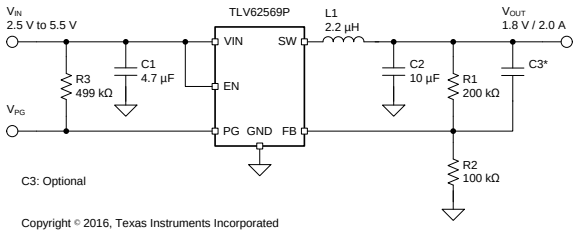
## 1 特性

- 效率高达 95%
- 低 $R_{DS(ON)}$，可在 100mΩ 和 60mΩ 之间切换
- 输入电压范围：2.5V 至 5.5V
- 可调输出电压：0.6V 至 $V_{IN}$
- 针对轻载效率的省电模式
- 针对最低压降的 100% 占空比
- 35µA 静态工作电流
- 1.5MHz 典型开关频率
- 电源正常输出
- 过流保护
- 内部软启动
- 热关断保护
- 采用小外形尺寸晶体管 (SOT) 封装
- 与 TLV62568 引脚兼容
- 使用 TLV62569 并借助 WEBENCH® Power Designer 创建定制设计方案

## 2 应用

- 通用负载点 (POL) 电源
- 机顶盒
- 网络视频摄像头
- 无线路由器
- 硬盘

简化电路原理图




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## 3 说明

TLV62569 器件是一款同步降压 DC-DC 转换器，专门针对高效和紧凑型解决方案进行了优化。该器件集成的开关能够提供高达 2A 的输出电流。

在中等负载或重载条件下，该器件运行在脉宽调制 (PWM) 模式下，开关频率为 1.5MHz。在轻载情况下，该器件自动进入节能模式 (PSM)，从而在整个负载电流范围内保持高效率。关断时，流耗减少至 2µA 以下。

TLV62569 的输出电压可通过一个外部电阻分压器进行调节。内部软启动电路可限制启动期间的浪涌电流。此外， 还内置了 诸如输出过流保护、热关断保护和电源正常输出等其他特性。该器件提供 SOT23 和 SOT563 两种封装。

器件信息(1)

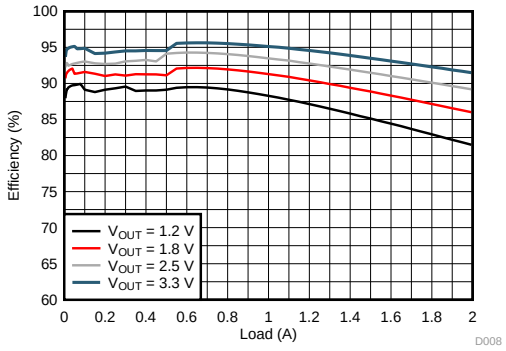
| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TLV62569DBV | SOT23 (5) | 2.90mm x 2.80mm |
| TLV62569PDDC | SOT23 (6) | |
| TLV62569DRL | SOT563 (6) | 1.60mm x 1.60mm |
| TLV62569PDRL | SOT563 (6) | |

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

器件比较

| 器件编号 | 功能 | 标记符号 |
|---|---|---|
| TLV62569DBV | - | 16AF |
| TLV62569PDDC | 电源正常 | 7G |
| TLV62569DRL | - | 19D |
| TLV62569PDRL | 电源正常 | 19E |

**5V 输入电压下的效率**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision B (July 2017) to Revision C** — **Page**

- 已更改 TLV62569DRL 和 TLV62569PDRL 更改为生产状态。 ... 1
- 已添加 在器件比较表中添加了 TLV62569DRL 和 TLV62569PDRL 的标记符号 ... 1
- Added DRL package thermal information ... 4
- Corrected editorial error of EN pin threshold voltage ... 4
- Added current limit for TLV62569DRL and TLV62569PDRL ... 5
- 已添加 TLV62569PDRL layout example ... 13

**Changes from Revision A (March 2017) to Revision B** — **Page**

- 已更改 TLV62569PDDC 更改为生产状态 ... 1
- 器件比较表移至第 1 页 ... 1
- Added DDC package thermal information ... 4
- Added startup time of TLV62569PDDC ... 4

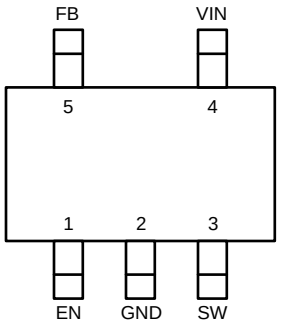
**Changes from Original (December 2016) to Revision A** — **Page**

- 已添加 WEBENCH® 模型 ... 1

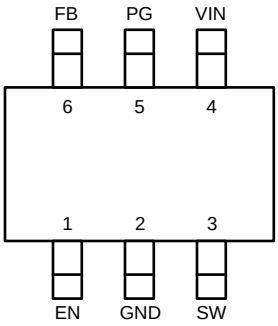

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# 5 Pin Configuration and Functions

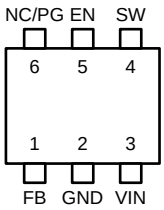
SOT23-5
DBV Package
(Top View)




SOT23-6
DDC Package
(Top View)




SOT563-6
DRL Package
(Top View)




**Pin Functions**

| PIN NUMBER | | | | I/O/PWR | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | SOT23-5 | SOT23-6 | SOT563-6 | | |
| EN | 1 | 1 | 5 | I | Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating. |
| GND | 2 | 2 | 2 | PWR | Ground pin. |
| SW | 3 | 3 | 4 | PWR | Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin. |
| VIN | 4 | 4 | 3 | PWR | Power supply voltage input. |
| PG | - | 5 | 6 | O | Power good open drain output pin for TLV62569P. The pull-up resistor should not be connected to any voltage higher than 5.5V. If it's not used, leave the pin floating. |
| FB | 5 | 6 | 1 | I | Feedback pin for the internal control loop. Connect this pin to an external feedback divider. |
| NC | - | - | 6 | O | No connection pin for TLV62569DRL. The pin can be connected to the output or the ground. Or leave it floating. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage(2) | VIN, EN, PG | –0.3 | 6 | V |
| | SW (DC) | –0.3 | $V_{IN}$+0.3 | V |
| | SW (AC, less than 10ns)(3) | –3.0 | 9 | V |
| | FB | –0.3 | 5.5 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and the device is not switching. Functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching

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## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | ±500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions (1)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.5 | | 5.5 | V |
| $V_{OUT}$ | Output voltage | 0.6 | | $V_{IN}$ | V |
| $I_{OUT}$ | Output current | 0 | | 2 | A |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |
| $I_{SINK_PG}$ | Sink current at PG pin | | | 1 | mA |

(1) Refer to the *Application and Implementation* section for further information.

## 6.4 Thermal Information

| THERMAL METRIC (1) | | DBV (5 Pins) | DDC (6 Pins) | DRL (6 Pins) | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 188.2 | 106.2 | 146.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 137.5 | 52.9 | 51.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 41.2 | 31.2 | 27.0 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 31.4 | 11.3 | 2.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 40.6 | 31.6 | 27.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

$V_{IN}$ = 5.0 V, $T_J$ = 25°C, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_Q$ | Quiescent current into VIN pin | Not switching | | 35 | | uA |
| $I_{SD}$ | Shutdown current into VIN pin | EN = 0 V | | 0.1 | 2 | µA |
| $V_{UVLO}$ | Under voltage lock out | $V_{IN}$ falling | | 2.3 | 2.45 | V |
| | Under voltage lock out hysteresis | | | 100 | | mV |
| $T_{JSD}$ | Thermal shutdown | Junction temperature rising | | 150 | | °C |
| | | Junction temperature falling | | 130 | | |
| **LOGIC INTERFACE** | | | | | | |
| $V_{IH}$ | High-level threshold at EN pin | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V | | 0.95 | 1.2 | V |
| $V_{IL}$ | Low-level threshold at EN pin | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V | 0.4 | 0.85 | | V |
| $t_{SS}$ | Soft startup time | TLV62569DBV | | 800 | | µs |
| | | TLV62569PDDC, TLV62569DRL, TLV62569PDRL | | 900 | | |
| $V_{PG}$ | Power good threshold | $V_{FB}$ rising, referenced to $V_{FB}$ nominal | | 95% | | |
| | | $V_{FB}$ falling, referenced to $V_{FB}$ nominal | | 90% | | |
| $V_{PG,OL}$ | Power good low-level output voltage | $I_{SINK}$ = 1 mA | | | 0.4 | V |
| $I_{PG,LKG}$ | Input leakage current into PG pin | $V_{PG}$ = 5.0 V | | 0.01 | | µA |
| $t_{PG,DLY}$ | Power good delay time | $V_{FB}$ falling | | 40 | | µs |
| **OUTPUT** | | | | | | |
| $V_{FB}$ | Feedback regulation voltage | | 0.588 | 0.6 | 0.612 | V |


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## Electrical Characteristics (continued)

$V_{IN}$ = 5.0 V, $T_J$ = 25°C, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{DS(on)}$ | High-side FET on resistance | | | 100 | | mΩ |
| | Low-side FET on resistance | | | 60 | | |
| $I_{LIM}$ | High-side FET current limit | TLV62569DBV, TLV62569PDDC | 3 | | | A |
| | | TLV62569DRL, TLV62569PDRL | 2.5 | | | |
| $f_{SW}$ | Switching frequency | $V_{OUT}$ = 2.5 V | | 1.5 | | MHz |

## 6.6 Typical Characteristics

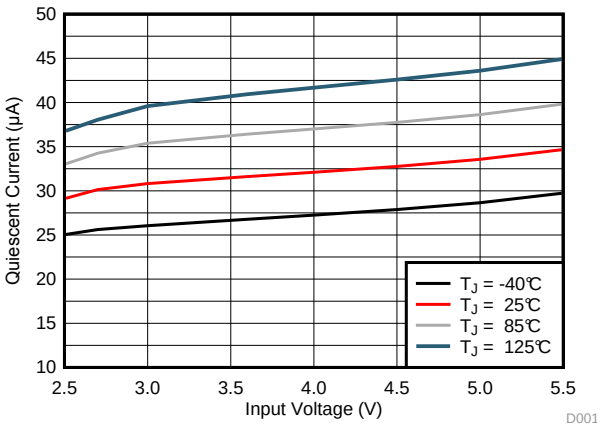



图 1. Quiescent Current vs Input Voltage

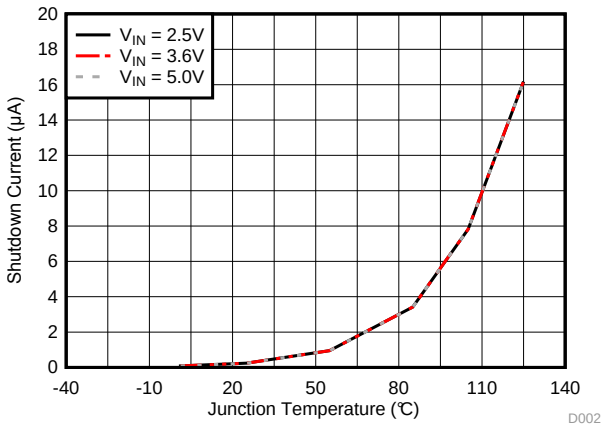



图 2. Shutdown Current vs Junction Temperature

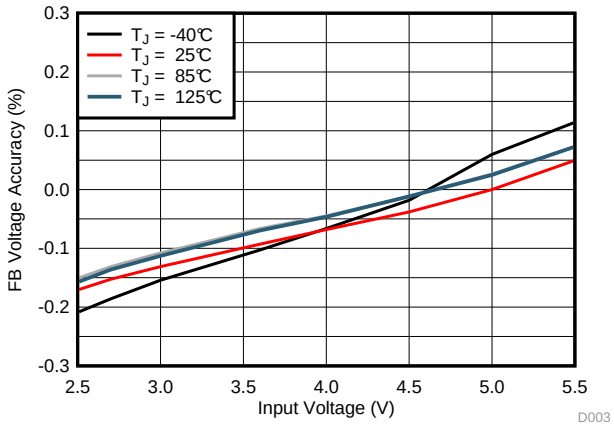



图 3. FB Voltage Accuracy

# 7 Detailed Description

## 7.1 Overview

The TLV62569 is a high-efficiency synchronous step-down converter. The device operates with an adaptive off time with peak current control scheme. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the $V_{IN}/V_{OUT}$ ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

## 7.2 Functional Block Diagrams

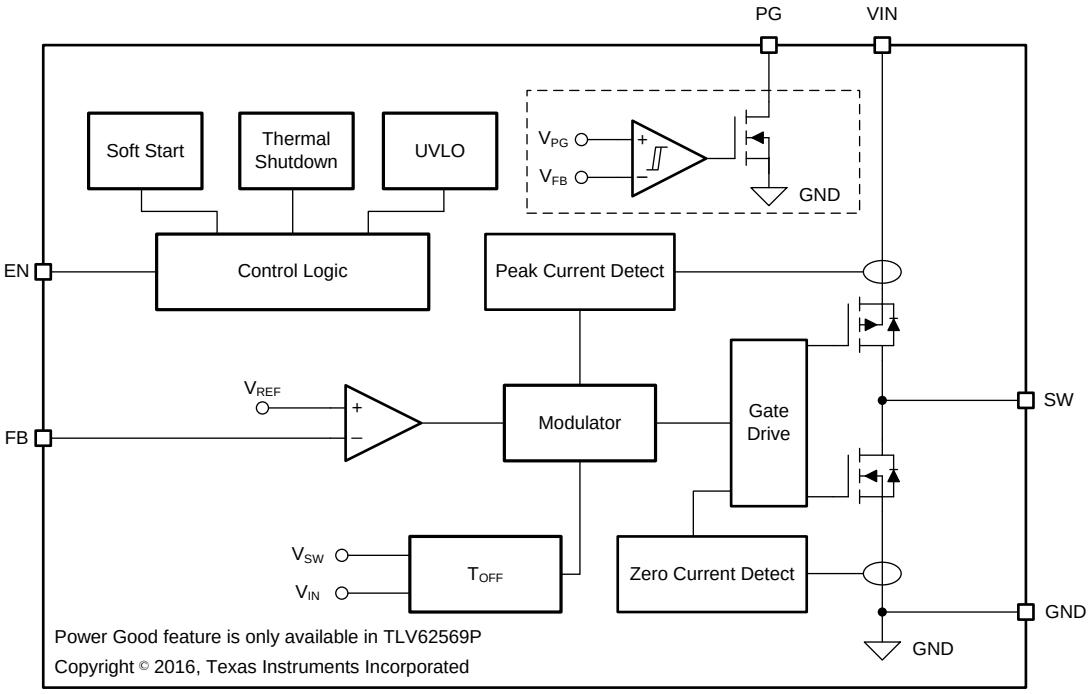



**图 4. TLV62569 Functional Block Diagram**

## 7.3 Feature Description

### 7.3.1 Power Save Mode

The device automatically enters Power Save Mode to improve efficiency at light load when the inductor current becomes discontinuous. In Power Save Mode, the converter reduces switching frequency and minimizes current consumption. In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor.

### 7.3.2 100% Duty Cycle Low Dropout Operation

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$ = High side FET on-resistance
- $R_L$ = Inductor ohmic resistance (DCR)


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## Feature Description (接下页)

### 7.3.3 Soft Startup

After enabling the device, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during a startup time. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TLV62569 is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

### 7.3.4 Switch Current Limit

The switch current limit prevents the device from high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition. The TLV62569 adopts the peak current control by sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off and low-side switch is turned on to ramp down the inductor current with an adaptive off-time.

### 7.3.5 Under Voltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than $V_{UVLO}$ with $V_{HYS_UVLO}$ hysteresis.

### 7.3.6 Thermal Shutdown

The device enters thermal shutdown once the junction temperature exceeds the thermal shutdown rising threshold, $T_{JSD}$. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

## 7.4 Device Functional Modes

### 7.4.1 Enabling/Disabling the Device

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

### 7.4.2 Power Good

The TLV62569P has a power good output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

**表 1. PG Pin Logic**

| DEVICE CONDITIONS | | LOGIC STATUS | |
|---|---|---|---|
| | | HIGH Z | LOW |
| Enable | EN = High, $V_{FB} \geq V_{PG}$ | √ | |
| | EN = High, $V_{FB} \leq V_{PG}$ | | √ |
| Shutdown | EN = Low | | √ |
| Thermal Shutdown | $T_J > T_{JSD}$ | | √ |
| UVLO | 1.4 V < $V_{IN}$ < $V_{UVLO}$ | | √ |
| Power Supply Removal | $V_{IN} \leq$ 1.4 V | √ | |

# 8 Application and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

## 8.2 Typical Application

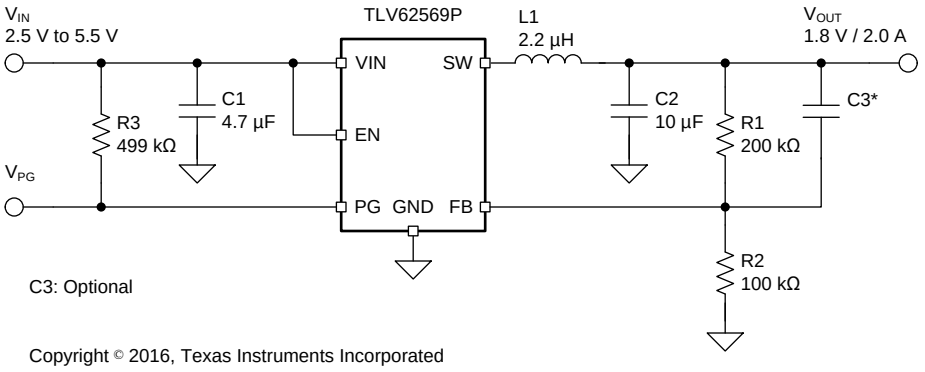



**图 5. TLV62569 1.8-V Output Application**

### 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

**表 2. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage | 2.5 V to 5.5 V |
| Output voltage | 1.8 V |
| Maximum output current | 2.0 A |

表 3 lists the components used for the example.

**表 3. List of Components**

| REFERENCE | DESCRIPTION | MANUFACTURER(1) |
|---|---|---|
| C1 | 4.7 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A475KA73L | Murata |
| C2 | 10 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A106KE51L | Murata |
| L1 | 2.2 µH, Power Inductor, size 4mmx4mm, XAL4020-222ME | Coilcraft |
| R1,R2,R3 | Chip resistor,1%,size 0603 | Std. |
| C3 | Optional, 6.8 pF if it is needed | Std. |

(1) See *Third-party Products Disclaimer*

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the TLV62569 device with the WEBENCH® Power Designer.


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1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### 8.2.2.2 Setting the Output Voltage

An external resistor divider is used to set output voltage according to 公式 2.

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 200 kΩ for R2. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

A feed forward capacitor, C3 improves the loop bandwidth to make a fast transient response (shown in 图 19). 6.8-pF capacitance is recommended for R2 of 100-kΩ resistance. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289.

#### 8.2.2.3 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 4 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

**表 4. Matrix of Output Capacitor and Inductor Combinations**

| $V_{OUT}$ [V] | L [µH](1) | $C_{OUT}$ [µF](2) | | | | |
|---|---|---|---|---|---|---|
| | | 4.7 | 10 | 22 | 2 x 22 | 100 |
| 0.6 ≤ $V_{OUT}$ < 1.2 | 1 | | | | + | |
| | 2.2 | | | | ++(3) | |
| 1.2 ≤ $V_{OUT}$ < 1.8 | 1 | | | + | + | |
| | 2.2 | | | ++(3) | + | |
| 1.8 ≤ $V_{OUT}$ | 1 | | + | + | + | |
| | 2.2 | | ++(3) | + | + | |

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

#### 8.2.2.4 Inductor Selection

The main parameters for inductor selection is inductor value and then saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 公式 3 is given:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (3)$$

where:

- $I_{OUT,MAX}$ is the maximum output current
- $\Delta I_L$ is the inductor current ripple
- $f_{SW}$ is the switching frequency
- L is the inductor value

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor.

#### 8.2.2.5 Input and Output Capacitor Selection

The architecture of the TLV62569 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 4.7-µF input capacitance is sufficient; a larger value reduces input voltage ripple.

The TLV62569 is designed to operate with an output capacitor of 10 µF to 47 µF, as outlined in 表 4.

### 8.2.3 Application Performance Curves

$V_{IN}$ = 5 V, $V_{OUT}$ = 1.8 V, L = 2.2 µH, $T_A$ = 25 °C, unless otherwise noted.

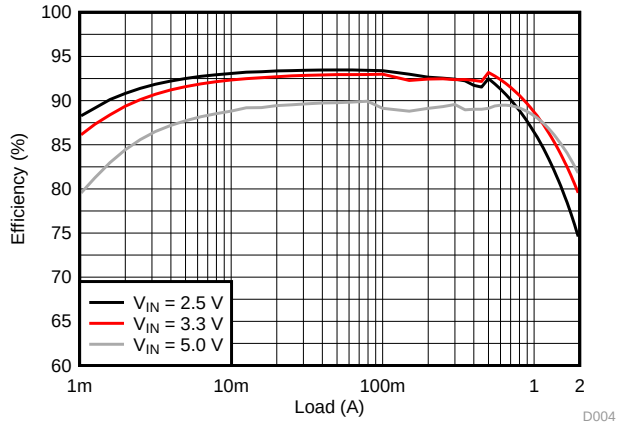



图 6. 1.2-V Output Efficiency

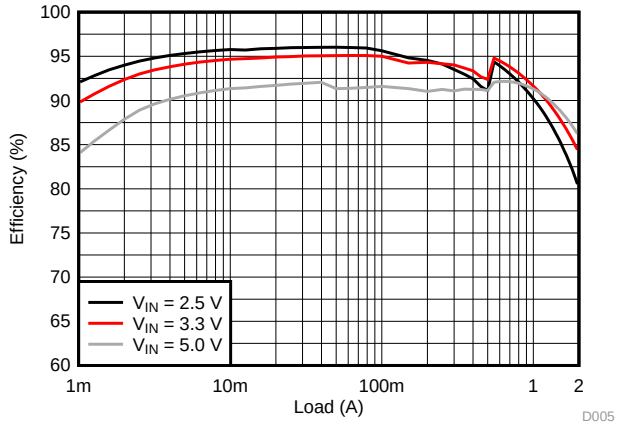



图 7. 1.8-V Output Efficiency


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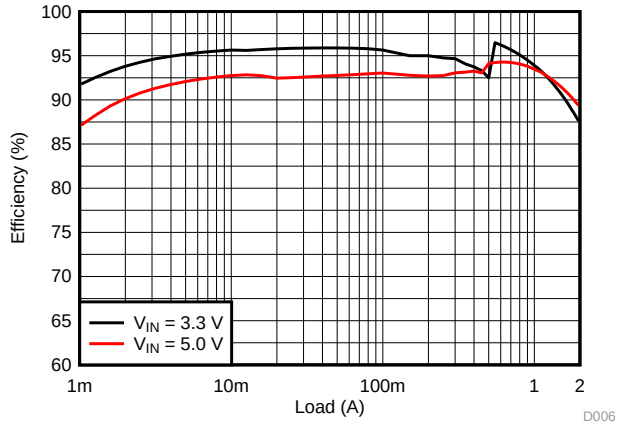



图 8. 2.5-V Output Efficiency

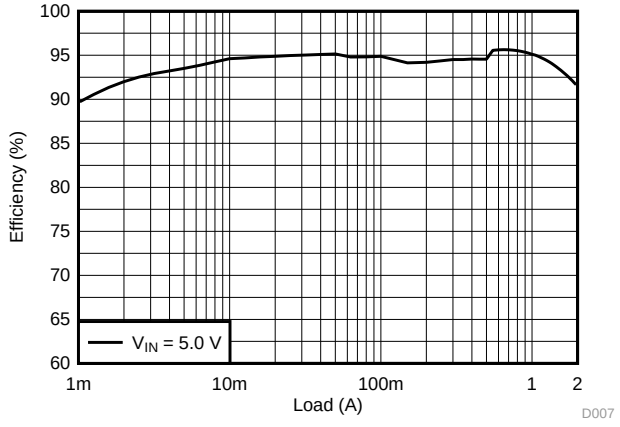
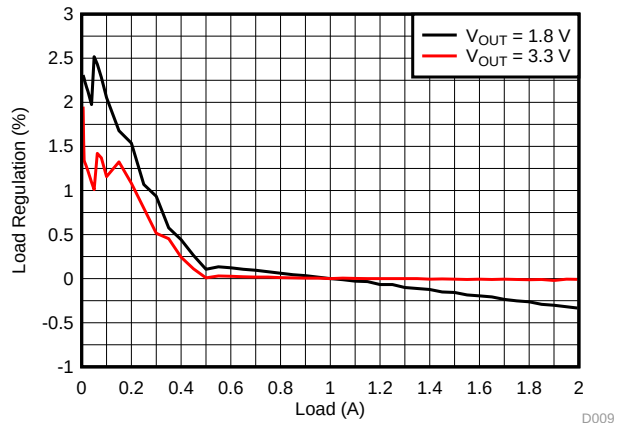
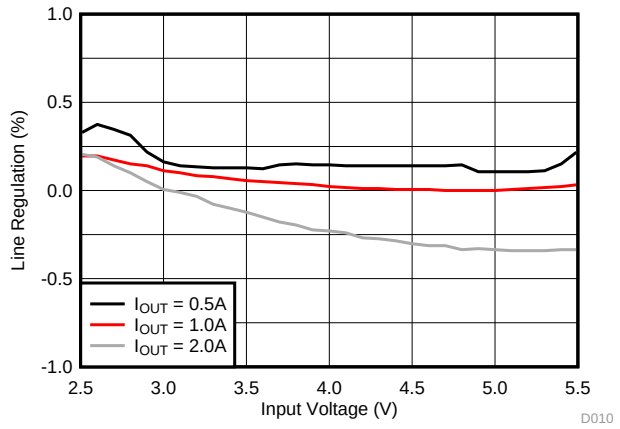



图 9. 3.3-V Output Efficiency



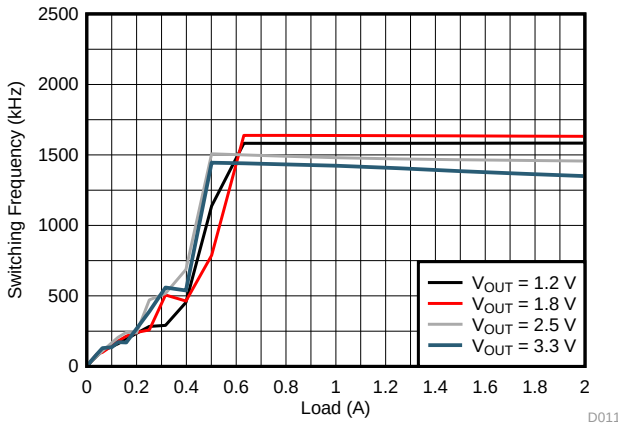

$V_{IN}$ = 5 V

图 10. Load Regulation



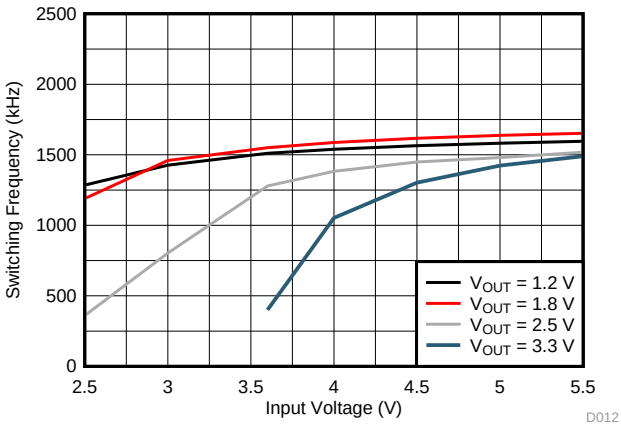

$V_{OUT}$ = 1.8 V

图 11. Line Regulation



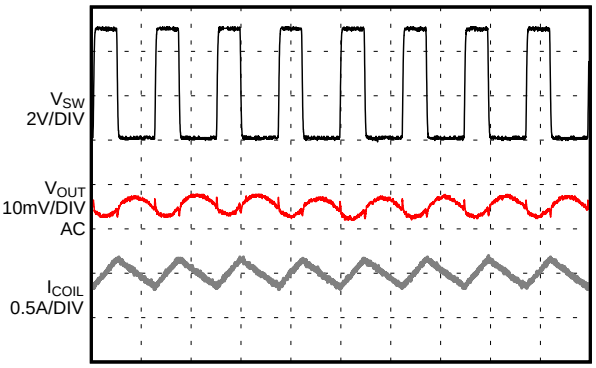

$V_{IN}$ = 5 V

图 12. Switching Frequency vs Load



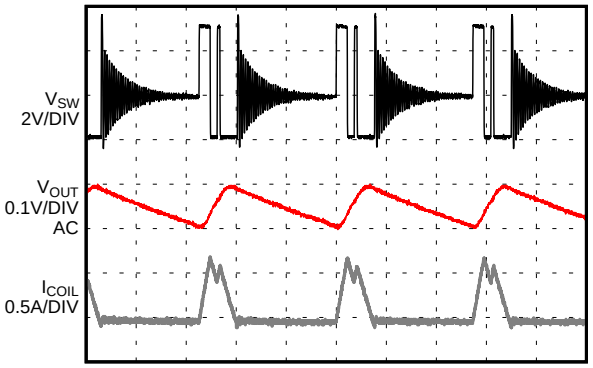

$I_{OUT}$ = 1 A

图 13. Switching Frequency vs Input Voltage



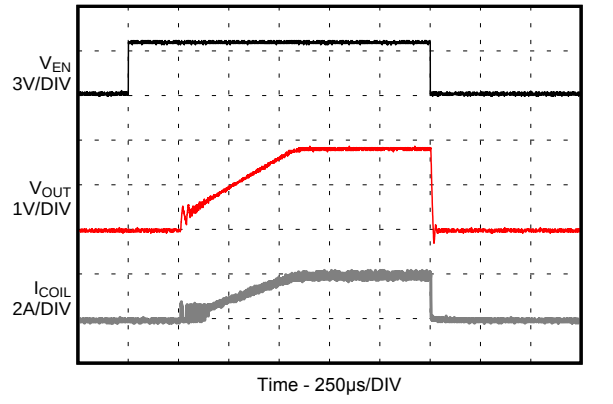

$I_{OUT}$ = 1 A

**图 14. PWM Operation**



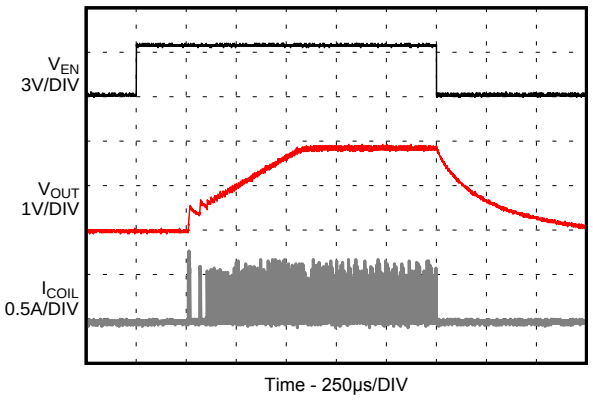

$I_{OUT}$ = 0.1 A

**图 15. Power Save Mode Operation**



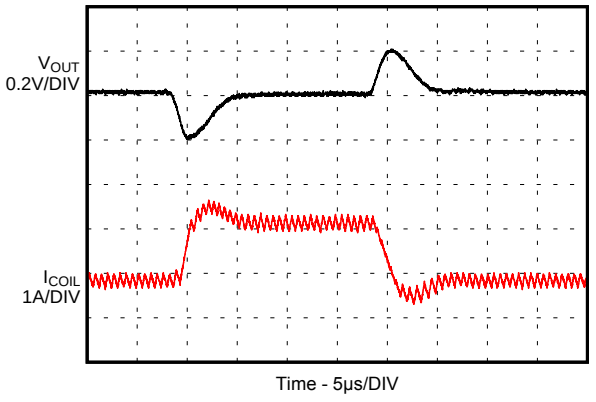

$I_{OUT}$ = 2 A

**图 16. Startup and Shutdown with Load**



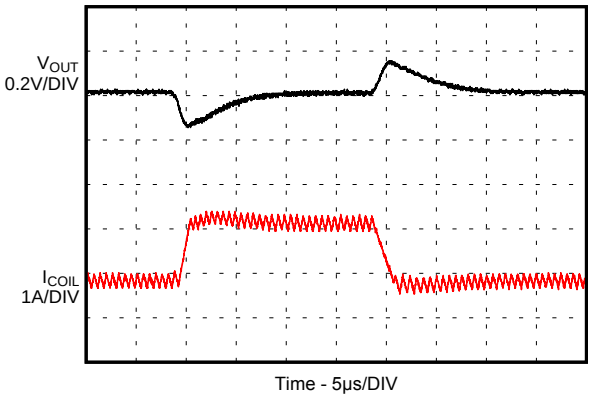

$I_{OUT}$ = 0.1 A

**图 17. Startup and Shutdown with Load**




Load Step 0.8 A to 2 A, 1A/µs slew rate

**图 18. Load Transient**




Load Step 0.8 A to 2 A, 1A/µs slew rate C3 = 6.8 pF

**图 19. Load Transient**

## 9 Power Supply Recommendations

The power supply to the TLV62569 must have a current rating according to the supply voltage, output voltage and output current.


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# 10 Layout

## 10.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TLV62569 device.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
- The sense traces connected to FB are signal traces. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- GND layers might be used for shielding.

## 10.2 Layout Example

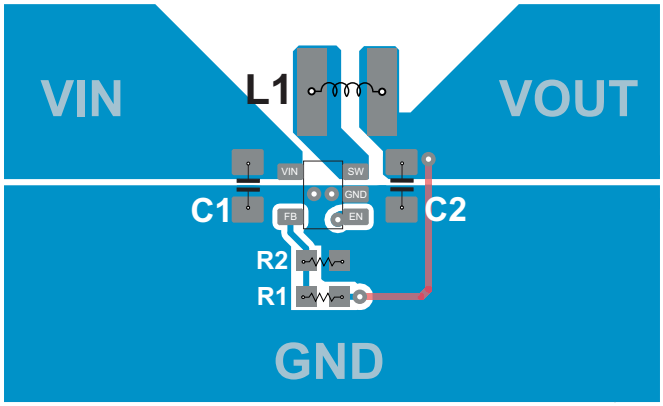



图 20. TLV62569DBV Layout

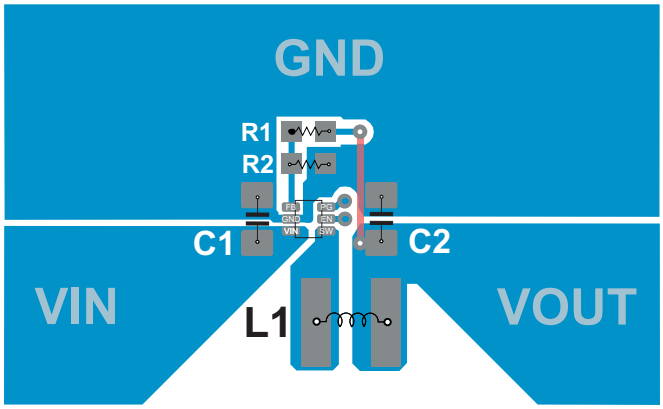



图 21. TLV62569PDRL Layout

## 10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

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# 11 器件和文档支持

## 11.1 器件支持

### 11.1.1 Third-Party Products Disclaimer

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### 11.1.2 开发支持

#### *11.1.2.1 使用 WEBENCH® 工具创建定制设计*

请单击此处，借助 WEBENCH® Power Designer 并使用 TLV62569 器件定制设计方案

1. 在开始阶段键入输出电压 ($V_{IN}$)、输出电压 ($V_{OUT}$) 和输出电流 ($I_{OUT}$) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

## 11.2 文档支持

### 11.2.1 相关文档

*应用报告《半导体和 IC 封装热指标》*（文件编号：SPRA953）

*应用报告《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》*（文件编号：SZZA017）

## 11.3 接收文档更新通知

要接收文档更新通知，请转至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 11.4 社区资源

**下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。**

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**设计支持** ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

## 11.5 商标

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WEBENCH is a registered trademark of Texas Instruments.
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## 11.6 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。


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### 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV62569DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 16AF |
| TLV62569DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 16AF |
| TLV62569DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 16AF |
| TLV62569DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 16AF |
| TLV62569DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 16AF |
| TLV62569DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 16AF |
| TLV62569DRLR | Active | Production | SOT-5X3 (DRL) \| 6 | 3000 \| LARGE T&R | Yes | Call TI \| Sn | Level-1-260C-UNLIM | -40 to 125 | 19D |
| TLV62569DRLR.A | Active | Production | SOT-5X3 (DRL) \| 6 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 19D |
| TLV62569DRLT | Active | Production | SOT-5X3 (DRL) \| 6 | 250 \| SMALL T&R | Yes | Call TI \| Sn | Level-1-260C-UNLIM | -40 to 125 | 19D |
| TLV62569DRLT.A | Active | Production | SOT-5X3 (DRL) \| 6 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 19D |
| TLV62569PDDCR | Active | Production | SOT-23-THIN (DDC) \| 6 | 3000 \| LARGE T&R | Yes | Call TI \| Sn | Level-1-260C-UNLIM | -40 to 125 | (6D9, 6DW) |
| TLV62569PDDCR.A | Active | Production | SOT-23-THIN (DDC) \| 6 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (6D9, 6DW) |
| TLV62569PDDCT | Active | Production | SOT-23-THIN (DDC) \| 6 | 250 \| SMALL T&R | Yes | Call TI \| Sn | Level-1-260C-UNLIM | -40 to 125 | (6D9, 6DW) |
| TLV62569PDDCT.A | Active | Production | SOT-23-THIN (DDC) \| 6 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (6D9, 6DW) |
| TLV62569PDRLR | Active | Production | SOT-5X3 (DRL) \| 6 | 3000 \| LARGE T&R | Yes | Call TI \| Sn | Level-1-260C-UNLIM | -40 to 125 | 19E |
| TLV62569PDRLR.A | Active | Production | SOT-5X3 (DRL) \| 6 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 19E |
| TLV62569PDRLT | Active | Production | SOT-5X3 (DRL) \| 6 | 250 \| SMALL T&R | Yes | Call TI \| Sn | Level-1-260C-UNLIM | -40 to 125 | 19E |
| TLV62569PDRLT.A | Active | Production | SOT-5X3 (DRL) \| 6 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 19E |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

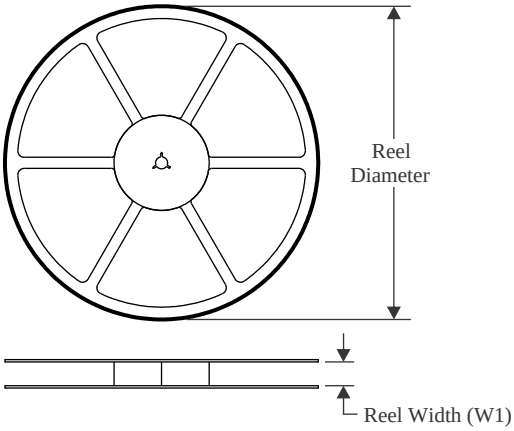
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

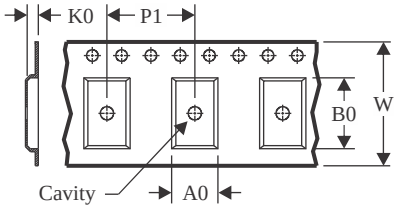
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

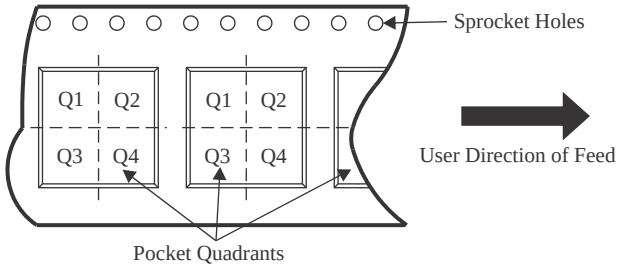



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

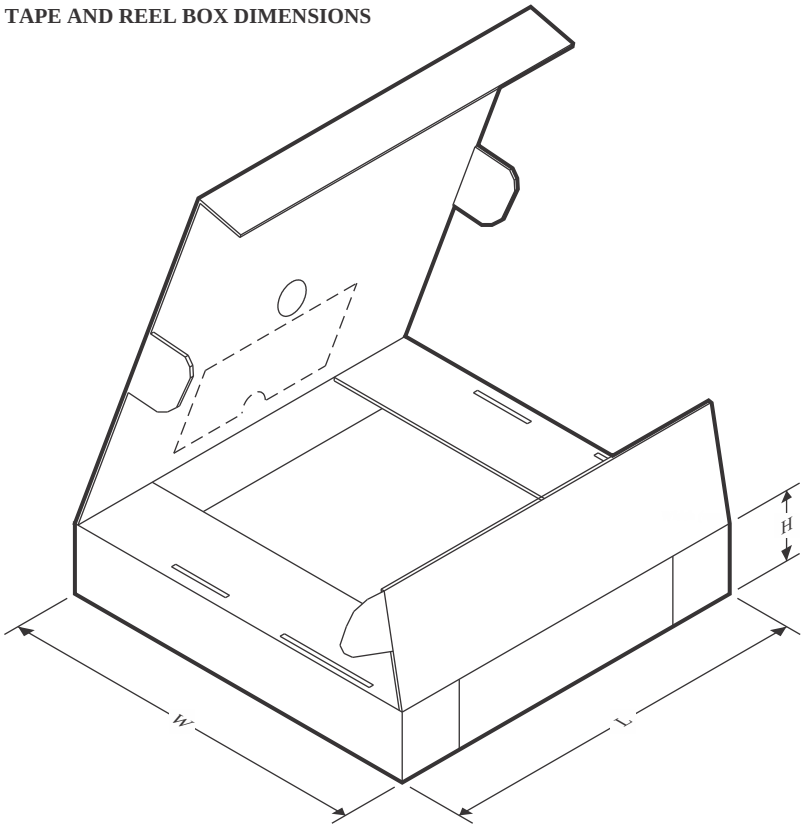



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV62569DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV62569DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV62569DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV62569DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV62569DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV62569DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV62569DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV62569DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV62569DRLR | SOT-5X3 | DRL | 6 | 3000 | 180.0 | 8.4 | 2.0 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |
| TLV62569DRLR | SOT-5X3 | DRL | 6 | 3000 | 180.0 | 8.4 | 1.8 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |
| TLV62569DRLT | SOT-5X3 | DRL | 6 | 250 | 180.0 | 8.4 | 2.0 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |
| TLV62569DRLT | SOT-5X3 | DRL | 6 | 250 | 180.0 | 8.4 | 1.8 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |
| TLV62569PDDCR | SOT-23-THIN | DDC | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV62569PDDCT | SOT-23-THIN | DDC | 6 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV62569PDRLR | SOT-5X3 | DRL | 6 | 3000 | 180.0 | 8.4 | 1.8 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV62569PDRLR | SOT-5X3 | DRL | 6 | 3000 | 180.0 | 8.4 | 2.0 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |
| TLV62569PDRLT | SOT-5X3 | DRL | 6 | 250 | 180.0 | 8.4 | 2.0 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |
| TLV62569PDRLT | SOT-5X3 | DRL | 6 | 250 | 180.0 | 8.4 | 1.8 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

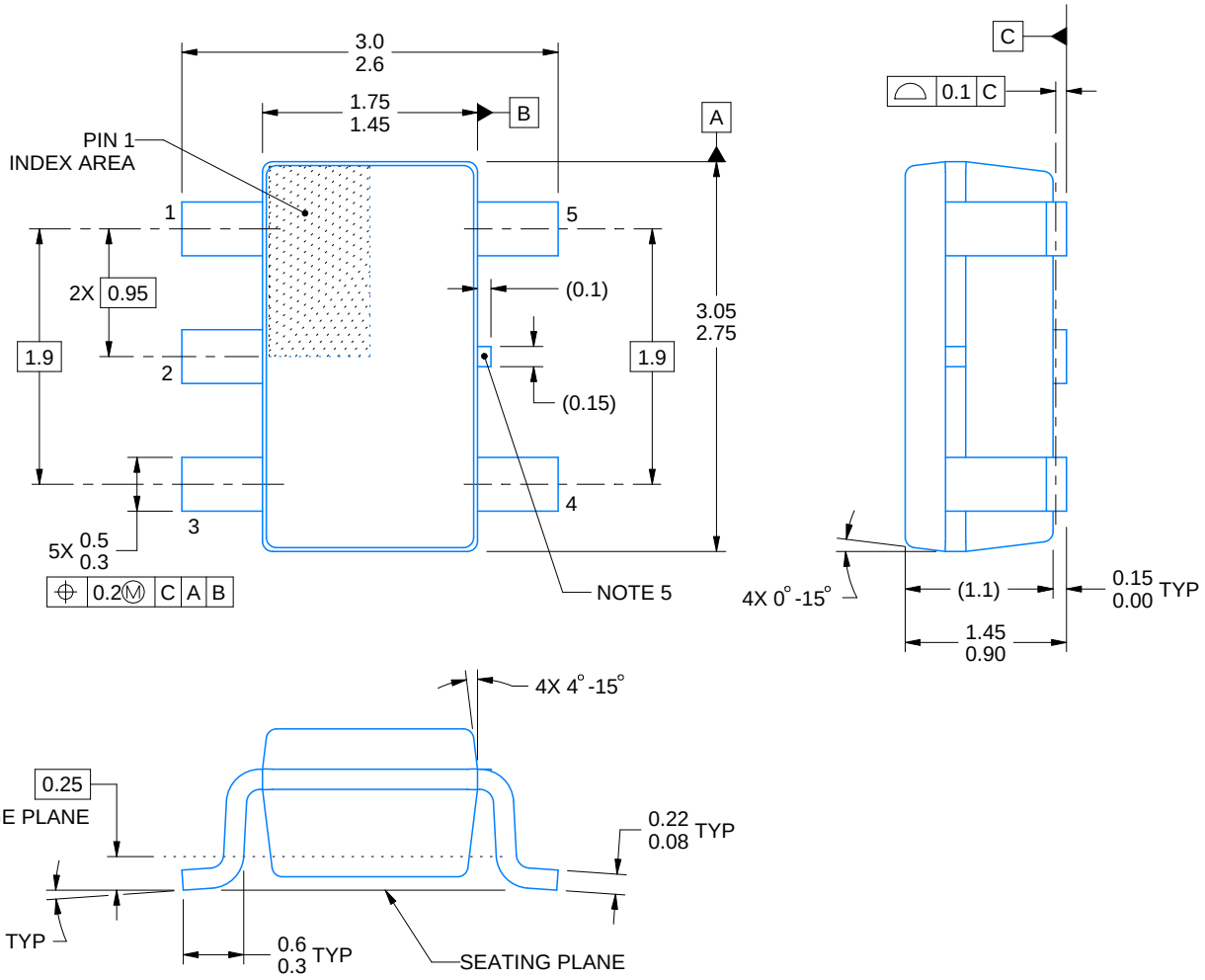
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV62569DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62569DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62569DBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TLV62569DBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62569DBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62569DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV62569DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV62569DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV62569DRLR | SOT-5X3 | DRL | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62569DRLR | SOT-5X3 | DRL | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62569DRLT | SOT-5X3 | DRL | 6 | 250 | 210.0 | 185.0 | 35.0 |
| TLV62569DRLT | SOT-5X3 | DRL | 6 | 250 | 210.0 | 185.0 | 35.0 |
| TLV62569PDDCR | SOT-23-THIN | DDC | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62569PDDCT | SOT-23-THIN | DDC | 6 | 250 | 210.0 | 185.0 | 35.0 |
| TLV62569PDRLR | SOT-5X3 | DRL | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62569PDRLR | SOT-5X3 | DRL | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV62569PDRLT | SOT-5X3 | DRL | 6 | 250 | 210.0 | 185.0 | 35.0 |
| TLV62569PDRLT | SOT-5X3 | DRL | 6 | 250 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

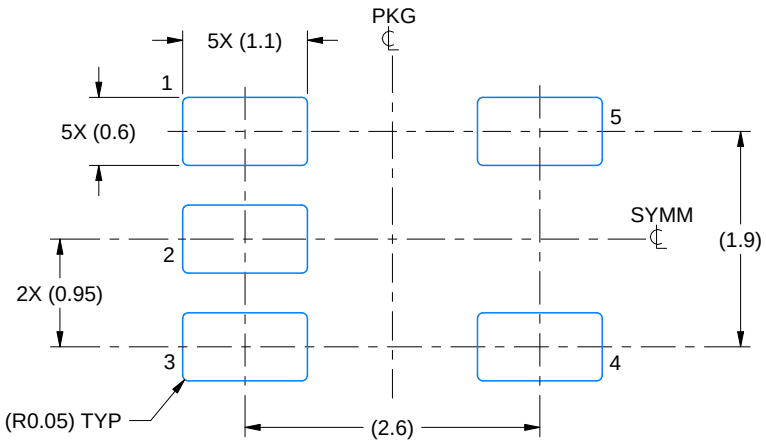
SMALL OUTLINE TRANSISTOR



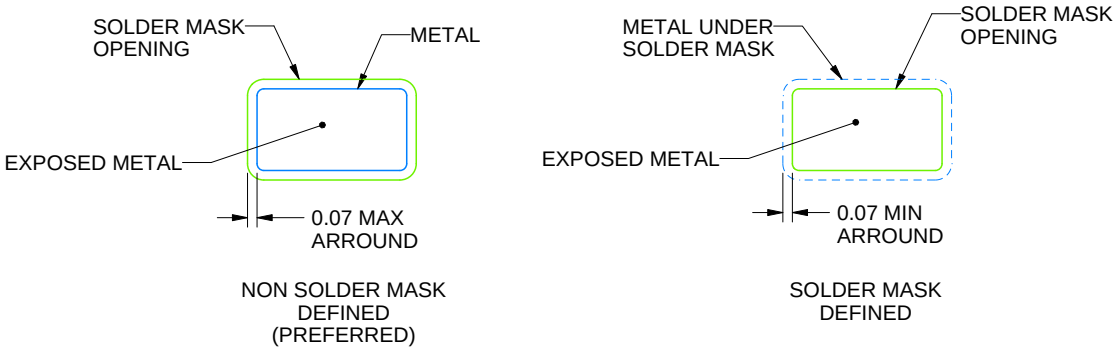

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

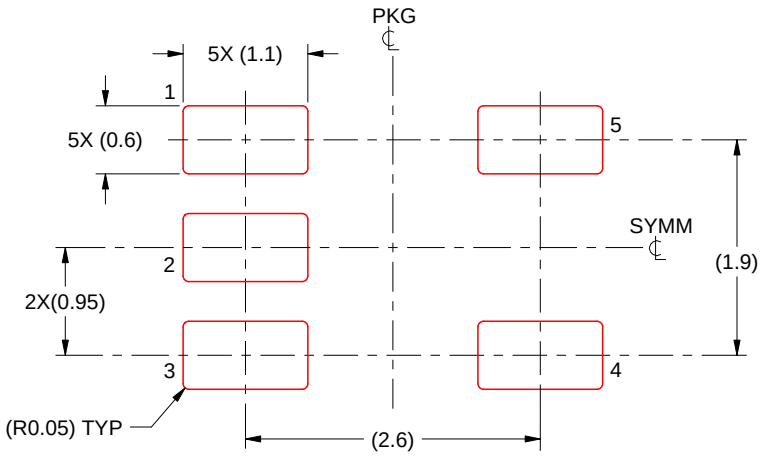



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

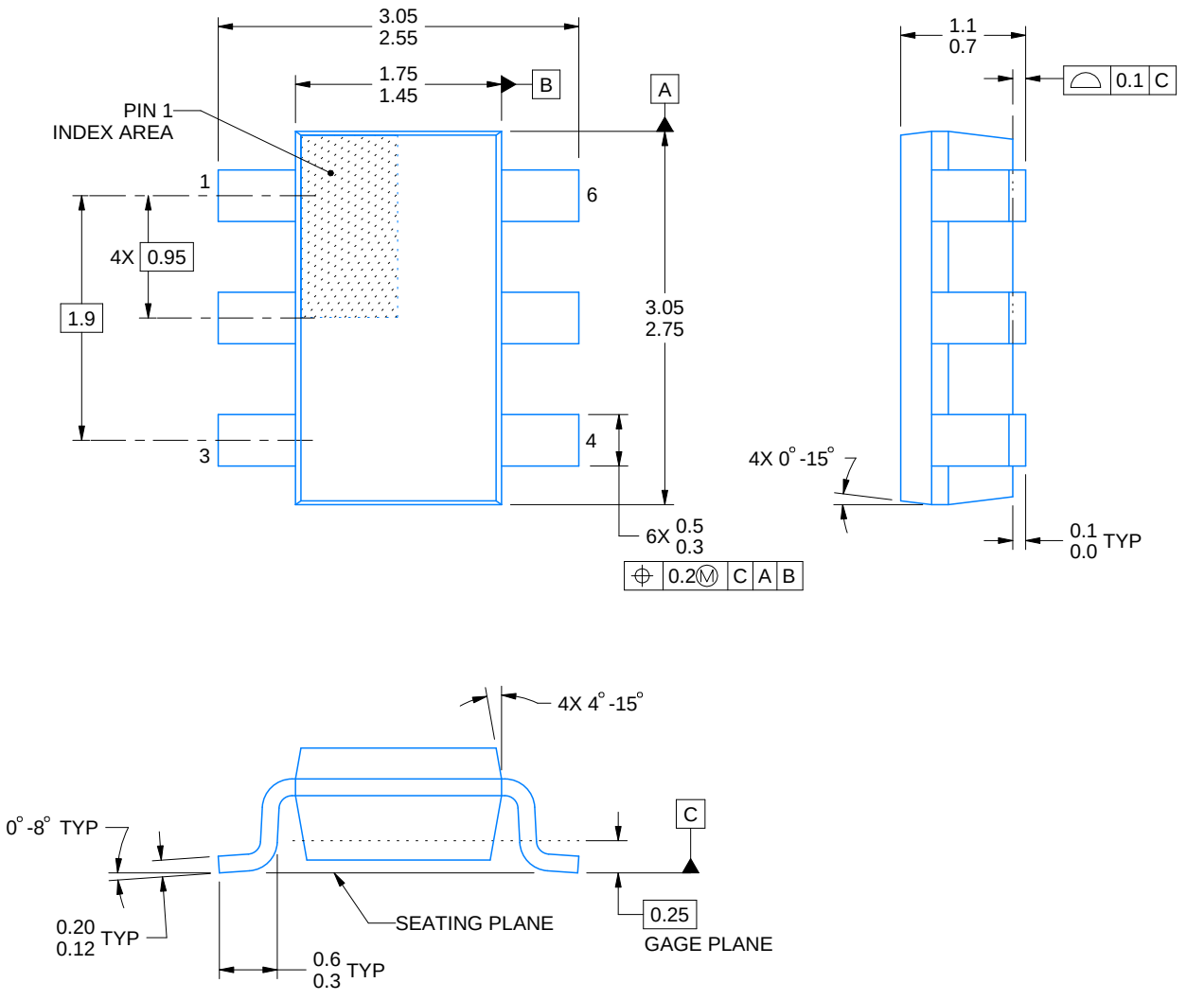
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DDC0006A

## SOT-23 - 1.1 max height

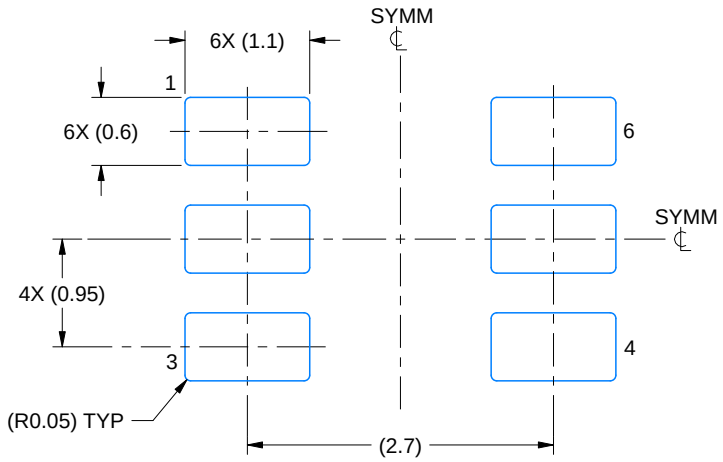
SMALL OUTLINE TRANSISTOR



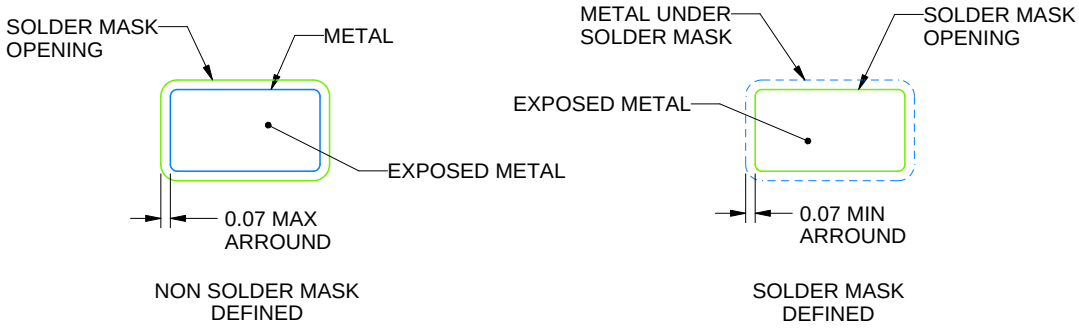

4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.




LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

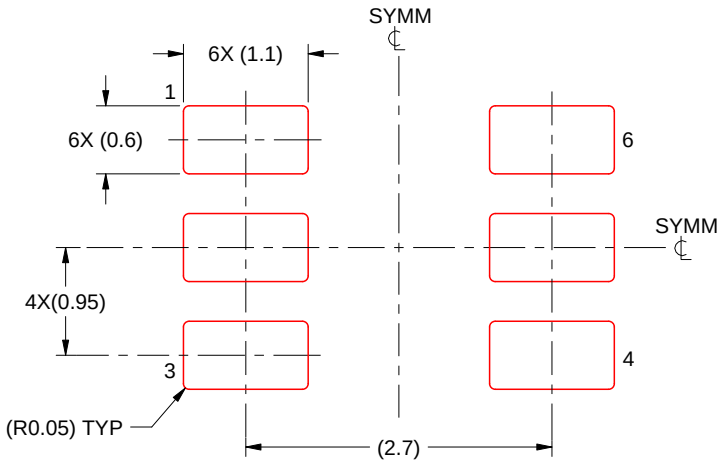



SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

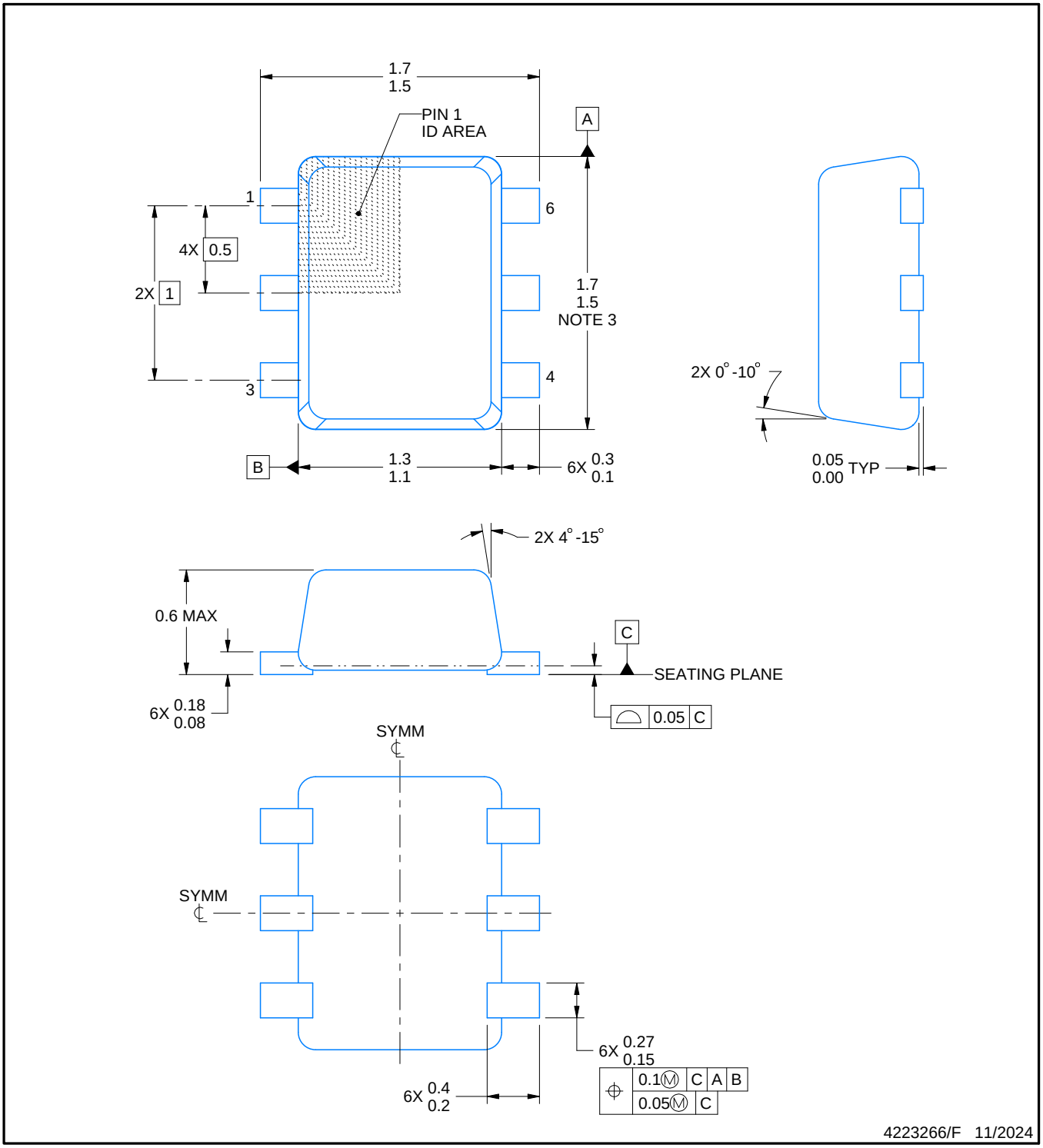


# PACKAGE OUTLINE

## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




NOTES:

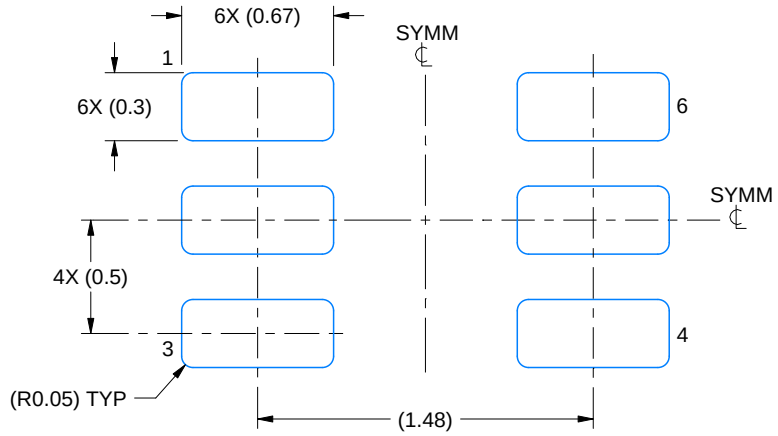
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

# EXAMPLE BOARD LAYOUT

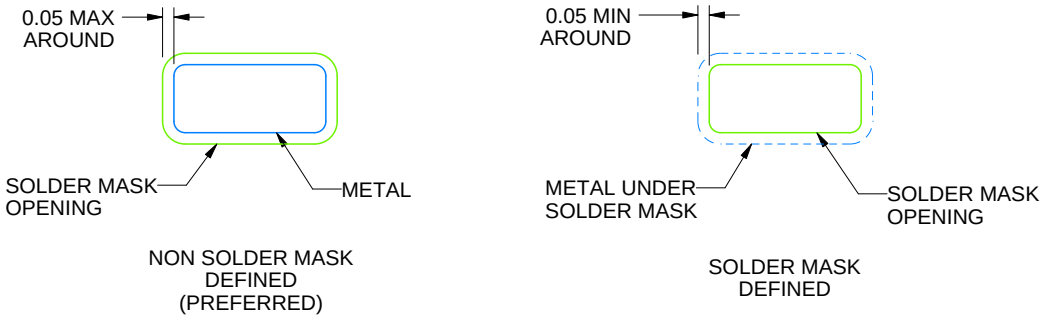
## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




LAND PATTERN EXAMPLE
SCALE:30X




SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

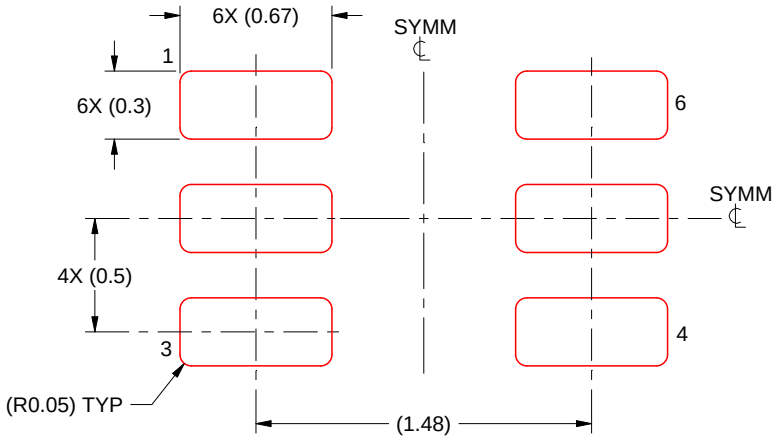
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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