SONY

Diagonal 6.09 mm (Type 1/3) CMOS Solid-state Image Sensor with Square Pixel for Color Cameras

IMX225LQR-C

Description

The IMX225LQR-C is a diagonal 6.09 mm (Type 1/3) CMOS active pixel type solid-state image sensor with a square pixel array and 1.27 M effective pixels. This chip operates with analog 3.3 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters. This chip features an electronic shutter with variable charge-integration time.
(Applications: Surveillance cameras)

Features

- ◆ CMOS active pixel type dots
- ◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆ Input frequency: 54 MHz / 27 MHz / 74.25 MHz / 37.125 MHz
- ◆ Number of recommended recording pixels: 1280 (H) × 960 (V) approx. 1.23M pixel
- ◆ Readout mode
  Quad VGA All-pixel scan mode / Horizontal / Vertical 2 × 2 binning mode
  Horizontal / Vertical 1 / 2 Subsampling mode / Window cropping mode / 720p-HD readout mode
  Vertical / Horizontal direction: normal / inverted readout mode
- ◆ Readout rate
  Maximum frame rate in Quad VGA mode: 120 frame / s
- ◆ Wide dynamic range (WDR) function
  Multiple exposure WDR
- ◆ Variable-speed shutter function (resolution 1H units)
- ◆ 10-bit / 12-bit A/D converter
- ◆ Conversion gain switching (HCG Mode / LCG Mode)
- ◆ CDS / PGA function
  0 dB to 30 dB: Analog Gain 30 dB (step pitch 0.1 dB)
  30.1 dB to 72 dB: Analog Gain 30 dB + Digital Gain 0.1 to 42 dB (step pitch 0.1 dB)
- ◆ Supports I/O switching
  CMOS logic parallel SDR output
  Low voltage LVDS (150 m Vp-p) serial (1 ch / 2 ch / 4 ch switching) DDR output
  CSI-2 serial data output (1 Lane / 2 Lane / 4 Lane, RAW10 / RAW12 output)
- ◆ Recommended lens F number: 2.8 or more (Close side)
- ◆ Recommended exit pupil distance: –30 mm to –∞

Exmor™

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Device Structure

- ◆ CMOS image sensor
- ◆ Image size
  Type 1/3
- ◆ Total number of pixels
  1312 (H) × 993 (V) approx. 1.30 M pixels
- ◆ Number of effective pixels
  1305 (H) × 977 (V) approx. 1.27 M pixels
- ◆ Number of active pixels
  1297 (H) × 977 (V) approx. 1.27 M pixels
- ◆ Number of recommended recording pixels
  1280 (H) × 960 (V) approx. 1.23 M pixels
- ◆ Unit cell size
  3.75 µm (H) × 3.75 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 4 pixels, rear 0 pixels
  Vertical (V) direction : Front 16 pixels, rear 0 pixels
- ◆ Dummy
  Horizontal (H) direction: Front 0 pixels, rear 3 pixels
  Vertical (V) direction : Front 0 pixels, rear 0 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog 3.3 V)	AV_{DD}	-0.3	4.0	V	-
Supply voltage (interface 1.8 V)	OV_{DD}	-0.3	3.3	V	-
Supply voltage (digital 1.2 V)	DV_{DD}	-0.3	2.0	V	-
Input voltage	VI	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Operating temperature	Topr	-30	85	˚C	-
Storage temperature	Tstg	-40	85	˚C	-

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 3.3 V)	AV_{DD}	3.15	3.30	3.45	V
Supply voltage (Interface 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (digital 1.2 V)	DV_{DD}	1.10	1.20	1.30	V

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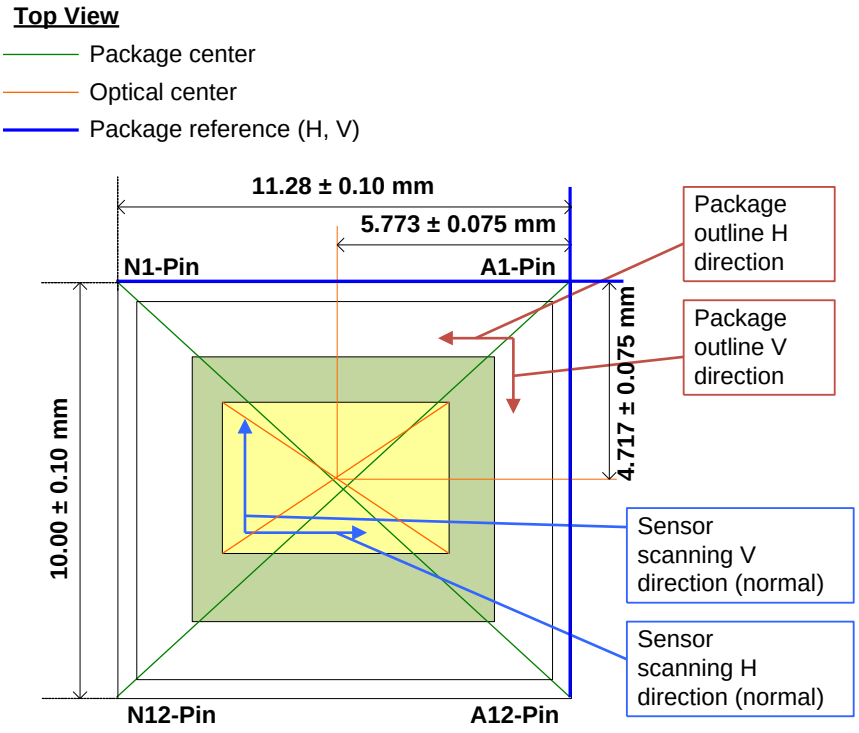
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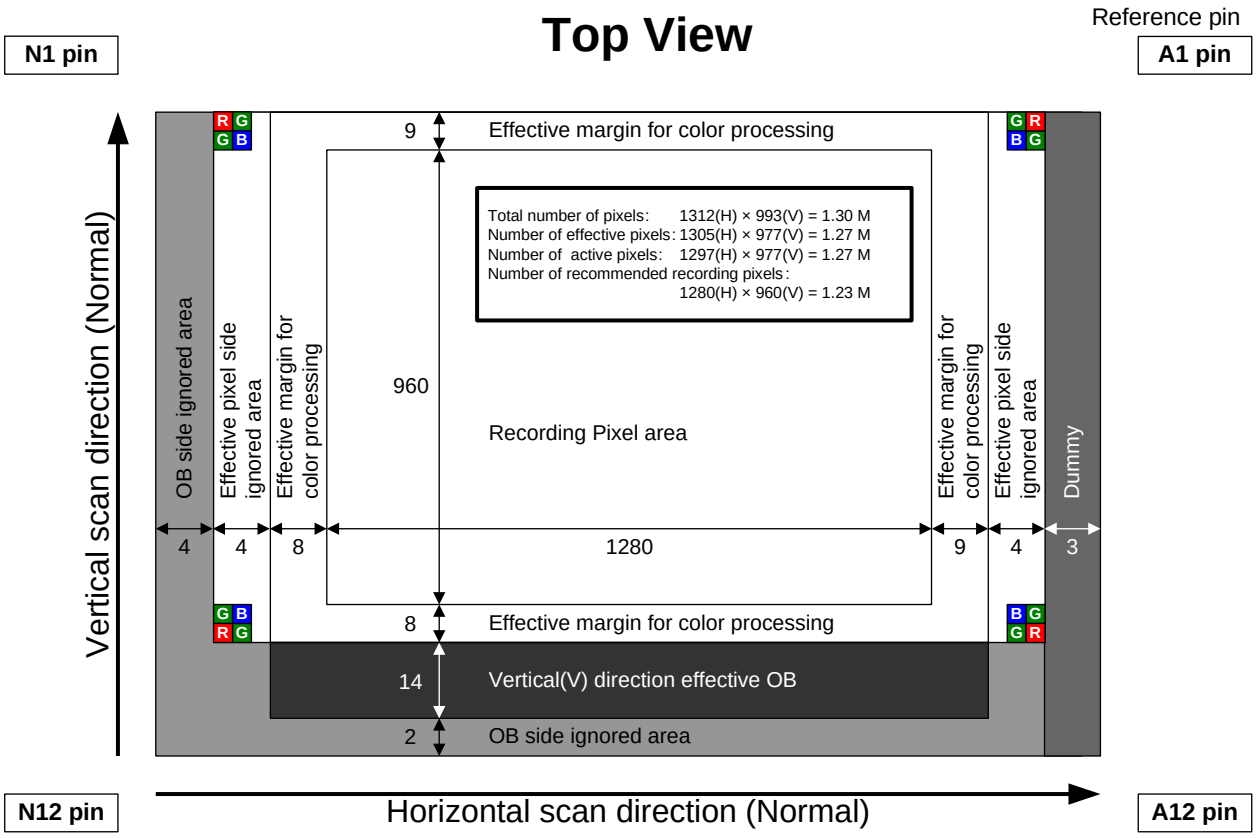
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Optical Center



Optical Center

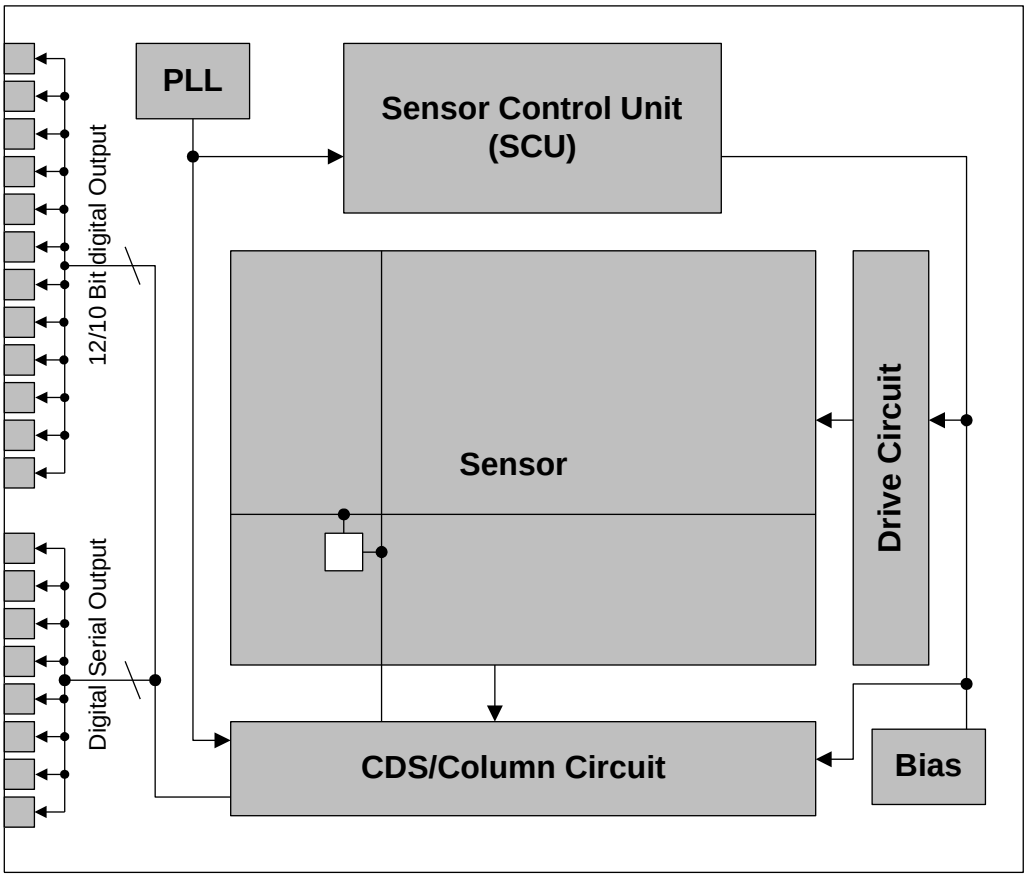
Pixel Arrangement



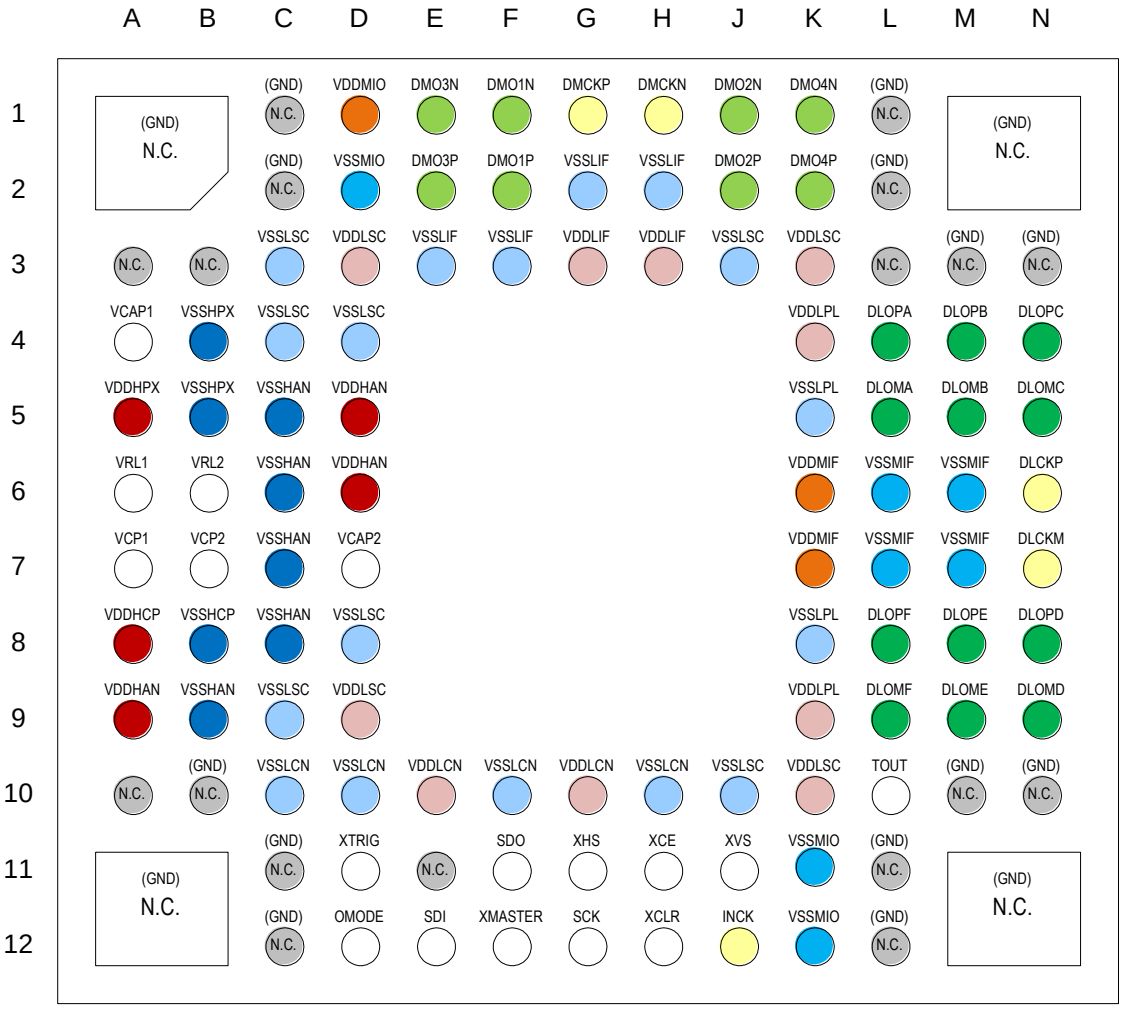
* Reference pin number is consecutive numbering of package pin array.
See the Pin Configuration for the number of each pin.

Pixel Arrangement (Top View)

Block Diagram and Pin Configuration



Block Diagram



*The N.C. pin that is shown with (GND) can be connected to GND, and the pin that not been described have to open.

Pin Configuration (Bottom View)

Pin Desctiption

No.	Pin No.	I/O	Analog /Digital	Symbol	zDescription	Remarks
1	A1	—	—	N.C.	—	GND connectable
2	A3	—	—	N.C.	—	OPEN
3	A4	O	A	VCAP1	Reference pin	—
4	A5	Power	A	VDDHPX	3.3V power supply	—
5	A6	I	A	VRL1	Connected to VCP1 pin.	—
6	A7	O	A	VCP1	Connected to VRL1 pin.	—
7	A8	Power	A	VDDHCP	3.3V power supply	—
8	A9	Power	A	VDDHAN	3.3V power supply	—
9	A10	—	—	N.C.	—	OPEN
10	A12	—	—	N.C.	—	GND connectable
11	B3	—	—	N.C.	—	OPEN
12	B4	GND	A	VSSHPX	3.3V GND	—
13	B5	GND	A	VSSHPX	3.3V GND	—
14	B6	I	A	VRL2	Connected to VCP2.	—
15	B7	O	A	VCP2	Connected to VRL2.	—
16	B8	GND	A	VSSHCP	3.3V GND	—
17	B9	GND	A	VSSHAN	3.3V GND	—
18	B10	—	—	N.C.	—	GND connectable
19	C1	—	—	N.C.	—	GND connectable
20	C2	—	—	N.C.	—	GND connectable
21	C3	GND	D	VSSLSC	1.2V GND	—
22	C4	GND	D	VSSLSC	1.2V GND	—
23	C5	GND	A	VSSHAN	3.3V GND	—
24	C6	GND	A	VSSHAN	3.3V GND	—
25	C7	GND	A	VSSHAN	3.3V GND	—
26	C8	GND	A	VSSHAN	3.3V GND	—
27	C9	GND	D	VSSLSC	1.2V GND	—
28	C10	GND	D	VSSLCN	1.2V GND	—
29	C11	—	—	N.C.	—	GND connectable
30	C12	—	—	N.C.	—	GND connectable
31	D1	Power	D	VDDMIO	1.8V power supply	—
32	D2	GND	D	VSSMIO	1.8V GND	—
33	D3	Power	D	VDDLSC	1.2V power supply	—
34	D4	GND	D	VSSLSC	1.2V GND	—
35	D5	Power	A	VDDHAN	3.3V power supply	—
36	D6	Power	A	VDDHAN	3.3V power supply	—
37	D7	O	A	VCAP2	Reference pin	—
38	D8	GND	D	VSSLSC	1.2V GND	—
39	D9	Power	D	VDDLSC	1.2V power supply	—
40	D10	GND	D	VSSLCN	1.2V GND	—
41	D11	I	D	XTRIG	TEST input pin.	—
42	D12	I	D	OMODE	Serial output interface selection High: LVDS / Low: CSI-2	High: OV_{DD} Low: GND
43	E1	O	D	DMO3N	CSI-2 output 3-Lane	—
44	E2	O	D	DMO3P	CSI-2 output 3-Lane	—
45	E3	GND	D	VSSLIF	1.2V GND	—
46	E10	Power	D	VDDLCN	1.2V power supply	—
47	E11	—	—	N.C.	—	OPEN
48	E12	I/O	D	SDI	Communication input 4-wire: SDI pin / I2C: SDA pin	—

No.	Pin No.	I/O	Analog /Digital	Symbol	zDescription	Remarks
49	F1	O	D	DMO1N	CSI-2 output 1-Lane	—
50	F2	O	D	DMO1P	CSI-2 output 1-Lane	—
51	F3	GND	D	VSSLIF	1.2V GND	—
52	F10	GND	D	VSSLCN	1.2V GND	—
53	F11	O	D	SDO	Communication output 4-wire: SDO pin / I2C: Open	—
54	F12	I	D	XMASTER	Master / Slave selection High: Slave mode / Low: Master mode	High: OV_{DD} Low: GND
55	G1	O	D	DMCKP	CSI-2 output clock	—
56	G2	GND	D	VSSLIF	1.2V GND	—
57	G3	Power	D	VDDLIF	1.2V power supply	—
58	G10	Power	D	VDDLCN	1.2V power supply	—
59	G11	I/O	D	XHS	Horizontal sync signal	—
60	G12	I	D	SCK	Communication clock 4-wire: SCK pin. / I2C: SCL pin.	—
61	H1	O	D	DMCKN	CSI-2 output clock	—
62	H2	GND	D	VSSLIF	1.2V GND	—
63	H3	Power	D	VDDLIF	1.2V power supply	—
64	H10	GND	D	VSSLCN	1.2V GND	—
65	H11	I	D	XCE	Coommunication enable 4-wire: XCE pin. / I2C: Fixed to High	—
66	H12	I	D	XCLR	System clear (Normal: High / Clear: Low)	—
67	J1	O	D	DMO2N	CSI-2 output 2-Lane	—
68	J2	O	D	DMO2P	CSI-2 output 2-Lane	—
69	J3	GND	D	VSSLSC	1.2V GND	—
70	J10	GND	D	VSSLSC	1.2V GND	—
71	J11	I/O	D	XVS	Vertical sync signal	—
72	J12	I	D	INCK	Master clock input	—
73	K1	O	D	DMO4N	CSI-2 output 4-Lane	—
74	K2	O	D	DMO4P	CSI-2 output 4-Lane	—
75	K3	Power	D	VDDLSC	1.2V power supply	—
76	K4	Power	D	VDDLPL	1.2V power supply	—
77	K5	GND	D	VSSLPL	1.2V GND	—
78	K6	Power	D	VDDMIF	1.8V power supply	—
79	K7	Power	D	VDDMIF	1.8V power supply	—
80	K8	GND	D	VSSLPL	1.2V GND	—
81	K9	Power	D	VDDLPL	1.2V power supply	—
82	K10	Power	D	VDDLSC	1.2V power supply	—
83	K11	GND	D	VSSMIO	1.8V GND	—
84	K12	GND	D	VSSMIO	1.8V GND	—

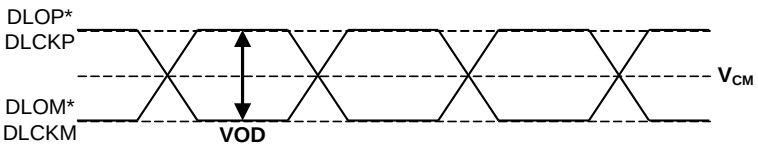
No.	Pin No.	I/O	Analog /Digital	Symbol	zDescription	Remarks
85	L1	—	—	N.C.	—	GND connectable
86	L2	—	—	N.C.	—	GND connectable
87	L3	—	—	N.C.	—	OPEN
88	L4	O	D	DLOPA	CMOS output / LVDS output	—
89	L5	O	D	DLOMA	CMOS output / LVDS output	—
90	L6	GND	D	VSSMIF	1.8V GND	—
91	L7	GND	D	VSSMIF	1.8V GND	—
92	L8	O	D	DLOPF	CMOS output / LVDS output	—
93	L9	O	D	DLOMF	CMOS output / LVDS output	—
94	L10	O	D	TOUT	TEST output pin	—
95	L11	—	—	N.C.	—	GND connectable
96	L12	—	—	N.C.	—	GND connectable
97	M3	—	—	N.C.	—	GND connectable
98	M4	O	D	DLOPB	CMOS output / LVDS output	—
99	M5	O	D	DLOMB	CMOS output / LVDS output	—
100	M6	GND	D	VSSMIF	1.8V GND	—
101	M7	GND	D	VSSMIF	1.8V GND	—
102	M8	O	D	DLOPE	CMOS output / LVDS output	—
103	M9	O	D	DLOME	CMOS output / LVDS output	—
104	M10	—	—	N.C.	—	GND connectable
105	N1	—	—	N.C.	—	GND connectable
106	N3	—	—	N.C.	—	GND connectable
107	N4	O	D	DLOPC	CMOS output / LVDS output	—
108	N5	O	D	DLOMC	CMOS output / LVDS output	—
109	N6	O	D	DLCKP	CMOS data clock / LVDS data clock	—
110	N7	O	D	DLCKM	LVDS data clock	—
111	N8	O	D	DLOPD	CMOS output / LVDS output	—
112	N9	O	D	DLOMD	CMOS output / LVDS output	—
113	N10	—	—	N.C.	—	GND connectable
114	N12	—	—	N.C.	—	GND connectable

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	analog	VDDHx	AV_{DD}	—	3.15	3.30	3.45	V
	Interface	VDDMx	OV_{DD}	—	1.70	1.80	1.90	V
	digital	VDDLx	DV_{DD}	—	1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK XMASTER OMODE SCK SDI XCE XTRIG	VIH	XVS / XHS Slave Mode	$0.8OV_{DD}$	—	—	V
			VIL		—	—	$0.2OV_{DD}$	V
Digital output voltage		DLOP [A:F] DLOM [A:F] DLCKP DLCKM	VOH	IOH = -2 mA	OV_{DD}-0.4	—	—	V
			VOL	IOL = 2 mA	—	—	0.4	V
			VCM	Low voltage LVDS	—	$OV_{DD}/2$	—	V
			VOD	Low voltage LVDS (Termination resistance: 100 Ω)	100	150	220	mV
		XHS XVS SDO TOUT	VOH	XVS / XHS Master Mode	OV_{DD}-0.4	—	—	V
			VOL		—	—	0.4	V

LVDS output



Current Consumption

Item	pin	Symbol	Typ.		Max.		Unit
			Standard luminous intensity	Saturated luminous intensity	Standard luminous intensity	Saturated luminous intensity	
Operating current Low voltage LVDS serial 4 ch 12 bit 60 frame / s Quad VGA All pixel scan mode	VDDH	IAV_{DD}	54	54	81	81	mA
	VDDM	IOV_{DD}	10	10	15	15	mA
	VDDL	IDV_{DD}	65	81	92	115	mA
Operating current MIPI CSI-2 / 4 lane 12 bit 60 frame / s Quad VGA All pixel scan mode	VDDH	IAV_{DD}	54	54	81	81	mA
	VDDM	IOV_{DD}	1	1	5	5	mA
	VDDL	IDV_{DD}	86	102	119	146	mA
Operating current CMOS parallel SDR 12 bit 30 frame / s Quad VGA All pixel scan mode	VDDH	IAV_{DD}	54	54	81	81	mA
	VDDM	IOV_{DD}	19	19	47	47	mA
	VDDL	IDV_{DD}	45	53	73	91	mA
Standby current	VDDH	IAV_{DD}_STB	—		0.1		mA
	VDDM	IOV_{DD}_STB	—		0.1		mA
	VDDL	IDV_{DD}_STB	—		4.8		mA

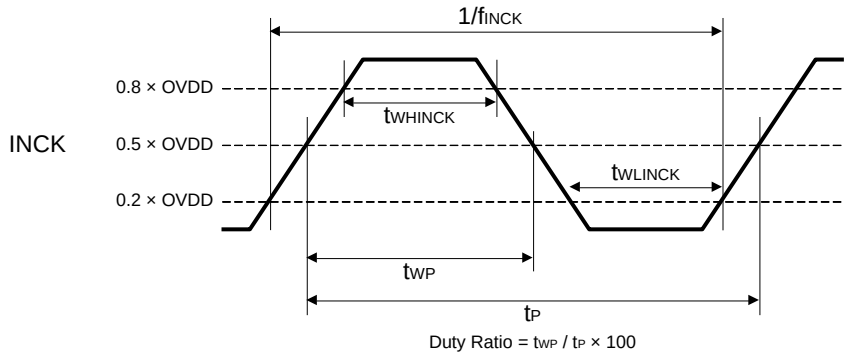
Operating current: (Typ.) Supply voltage3.3 V / 1.8 V / 1.2 V, Tj = 25 ˚C
(Max.) Supply voltage3.45 V / 1.9 V / 1.3 V, Tj = 60 ˚C, worst state of internal circuit operating current consumption,

Standby: (Max.) Supply voltage3.45 V / 1.9 V / 1.3 V, Tj = 60 ˚C, INCK: 0 V,
The device in the light-obstructed state.

Standard luminous intensity: luminous intensity at 1/3 of the sensor saturated
Saturated luminous intensity: luminous intensity when the sensor is saturated.

AC Characteristics

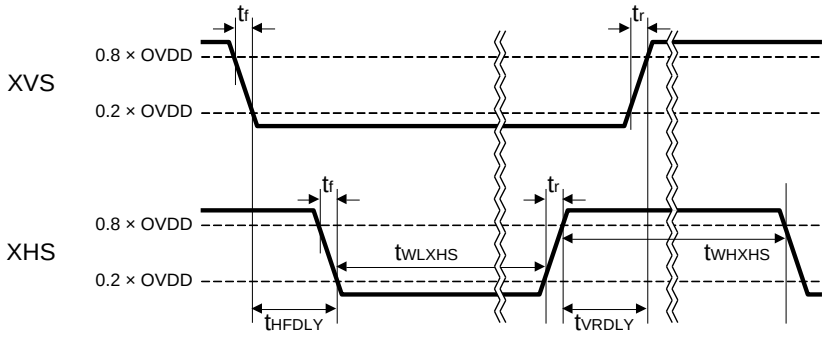
Master Clock Waveform (INCK)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 27 MHz, 54 MHz, 37.125 MHz, 74.25 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	f_{INCK} = 27 MHz, 54 MHz, 37.125 MHz, 74.25 MHz
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	f_{INCK} = 27 MHz, 54 MHz, 37.125 MHz, 74.25 MHz
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}

*The INCK fluctuation affects the frame rate.

XVS / XHS Input Characteristics In Slave Mode (DMODE pin = High)



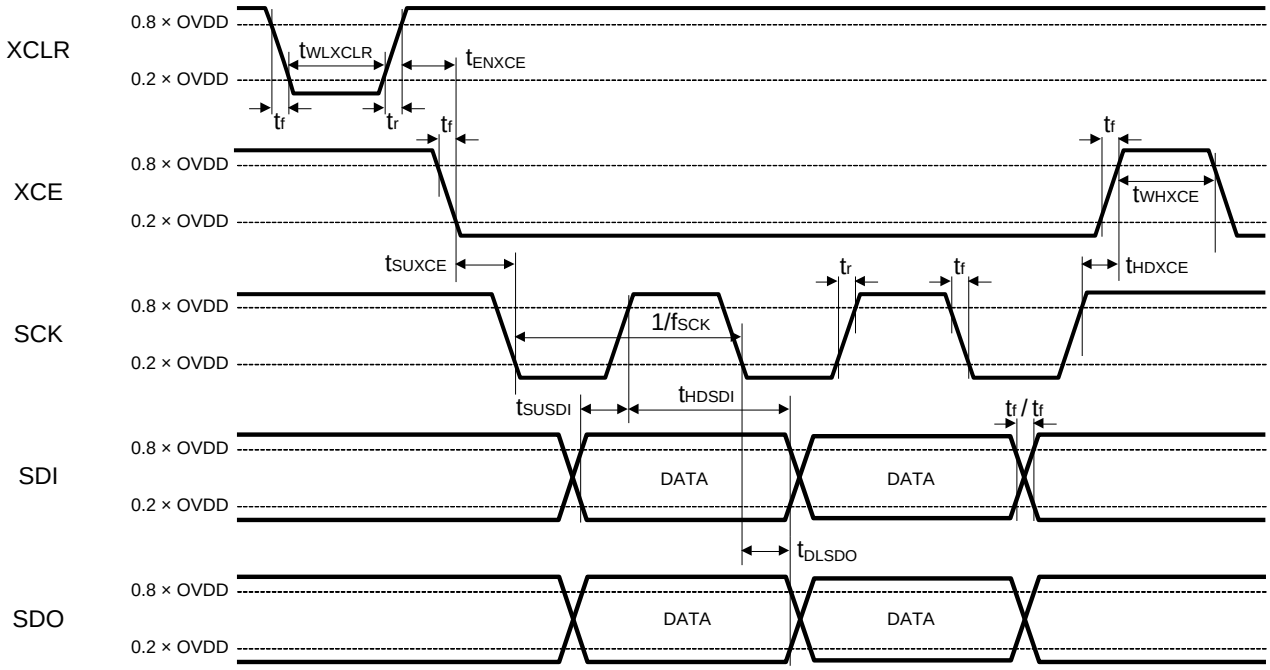
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	4 / f_{INCK}	—	—	ns	—
XHS High level pulse width	t_{WHXHS}	4 / f_{INCK}	—	—	ns	—
XVS - XHS fall width	t_{HFDLY}	1 / f_{INCK}	—	—	ns	—
XHS - XVS rise width	t_{VRDLY}	1 / f_{INCK}	—	—	ns	—
XVS, XHS rise time	t_r	—	—	5	ns	20 % to 80 %
XVS, XHS fall time	t_f	—	—	5	ns	80 % to 20 %

XVS / XHS Input Characteristics In Master Mode (DMODE pin = Low, CMOS Output)

* XVS and XHS cannot be used for the sync signal to pixels.
Be sure to detect sync code to detect the start of effective pixels in 1 line.
For the output waveforms in master mode, see the item of “Slave Mode and Master Mode”

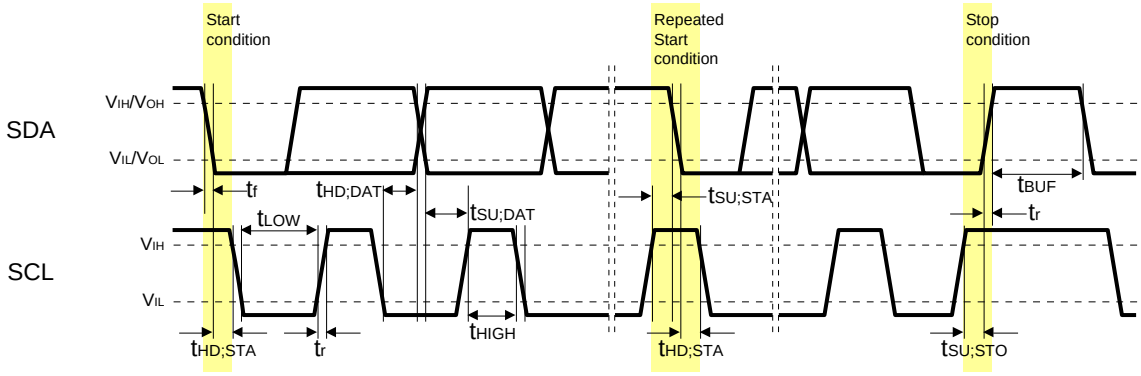
Serial Communication

4-wire



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	13.5	MHz	—
XCLR Low level pulse width	t_{WLXCLR}	4 / f_{INCK}	—	—	ns	—
XCE effective margin	t_{ENXCE}	20	—	—	µs	—
XCE input set-up time	t_{SUXCE}	20	—	—	ns	—
XCE input hold time	t_{HDXCE}	20	—	—	ns	—
XCE High level pulse width	t_{WHXCE}	20	—	—	ns	—
SDI input set-up time	t_{SUSDI}	10	—	—	ns	—
SDI input hold time	t_{HDSDI}	10	—	—	ns	—
SDO output delay time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF
Rise time of each input signal	t_r	—	—	5	ns	20 % to 80 %
Fall time of each input signal	t_f	—	—	5	ns	80 % to 20 %

I²C



I²C Specification

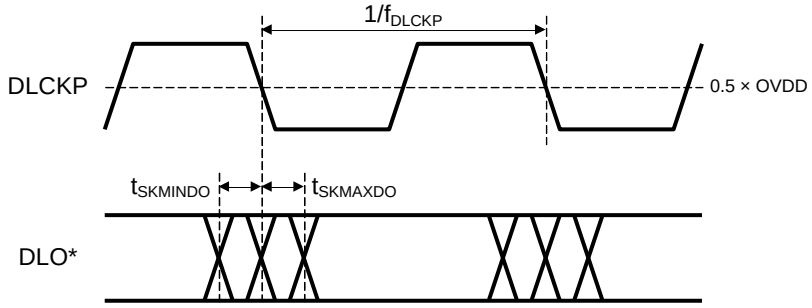
Item	Symbol	Min.	Typ.	Max.	Unit	条件
Low level input voltage	VIL	-0.3	—	0.3 × OVDD	V	—
High level input voltage	VIH	0.7 × OVDD	—	1.9	V	—
Low level input voltage	VOL	0	—	0.2 × OVDD	V	OVDD < 2 V, Sink 3 mA
High level input voltage	VOH	0.8 × OVDD	—	—	V	—
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF, 0.7 × OVDD – 0.3 × OVDD
Input current	Ii	-10	—	10	µA	0.1 × OVDD – 0.9 × OVDD
Capacitance for SCK (SCL) /SDI (SDA)	Ci	—	—	10	pF	—

I²C AC Charateristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	µs
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	—	—	ns
Rise time of both SDA and SCL signals	t_r	—	—	300	ns
Fall time of both SDA and SCL signals	t_f	—	—	300	ns
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	µs
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	µs

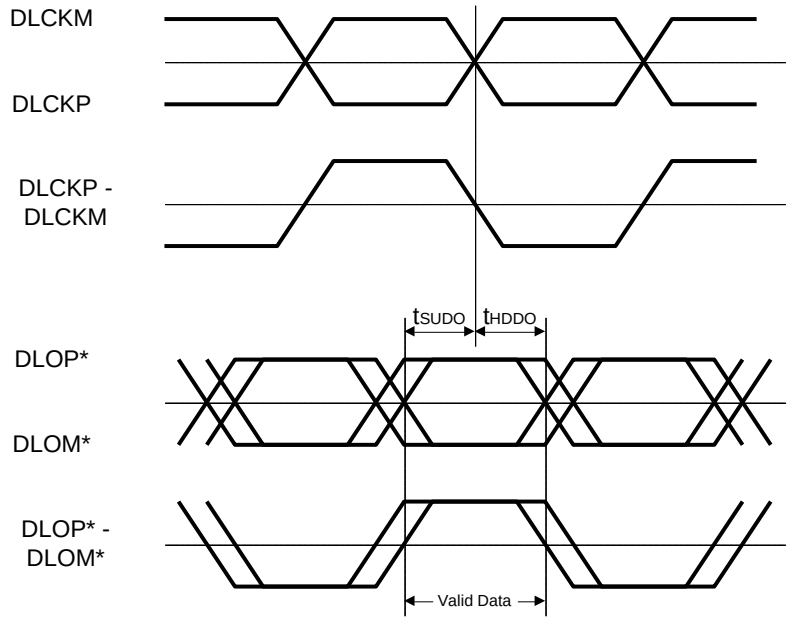
DLCKP / DLCKM, DLOP / DLOM

CMOS Outputs



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DLCKP frequency	f_{DLCKP}	—	—	74.25	MHz	—
DLCKP clock duty	—	40	50	60	%	—
DLCKP - DLO skew Max.	$t_{SKMAXDO}$	—	—	2	ns	Output load capacitance: 20 pF
DLCKP - DLO skew Min.	$t_{SKMINDO}$	—	—	2	ns	Output load capacitance: 20 pF

Low Voltage LVDS DDR Output

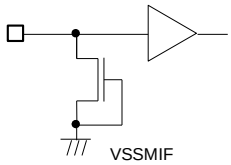
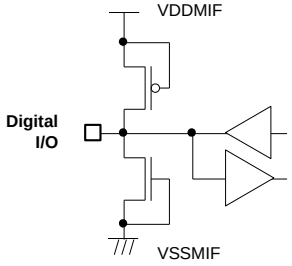
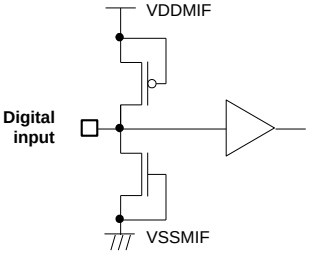
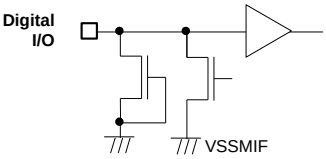
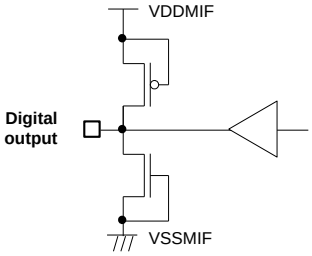
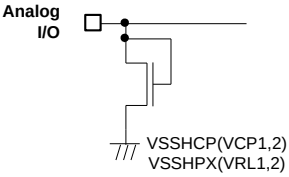
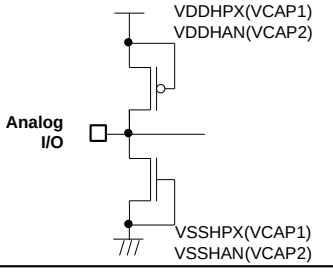
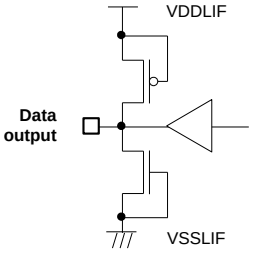
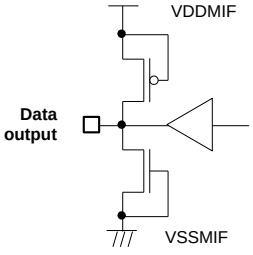


(Output load capacitance: 8 pF)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DLCKP/DLCKM clock duty	—	40	50	60	%	DLCK = 297 MHz (Max.)
DLO set-up time	t_{SUDO}	400	—	—	ps	Data Rate 297 MHz DDR
DLO hold time	t_{HDDO}	400	—	—	ps	Data Rate 297 MHz DDR

I/O Equivalent Circuit Diagram

□ : External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
INCK		XVS XHS	
XCLR XCE XMASTER OMODE XTRIG		SDI SCK	
SDO			
VCP1 VCP2 VRL1 VRL2		VCAP1 VCAP2	
DMOxP DMOxN DMCKP DMCKN X=1 to 4		DLOPx DLOMx DLCKP DLCKM TOUT x=A to F	

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

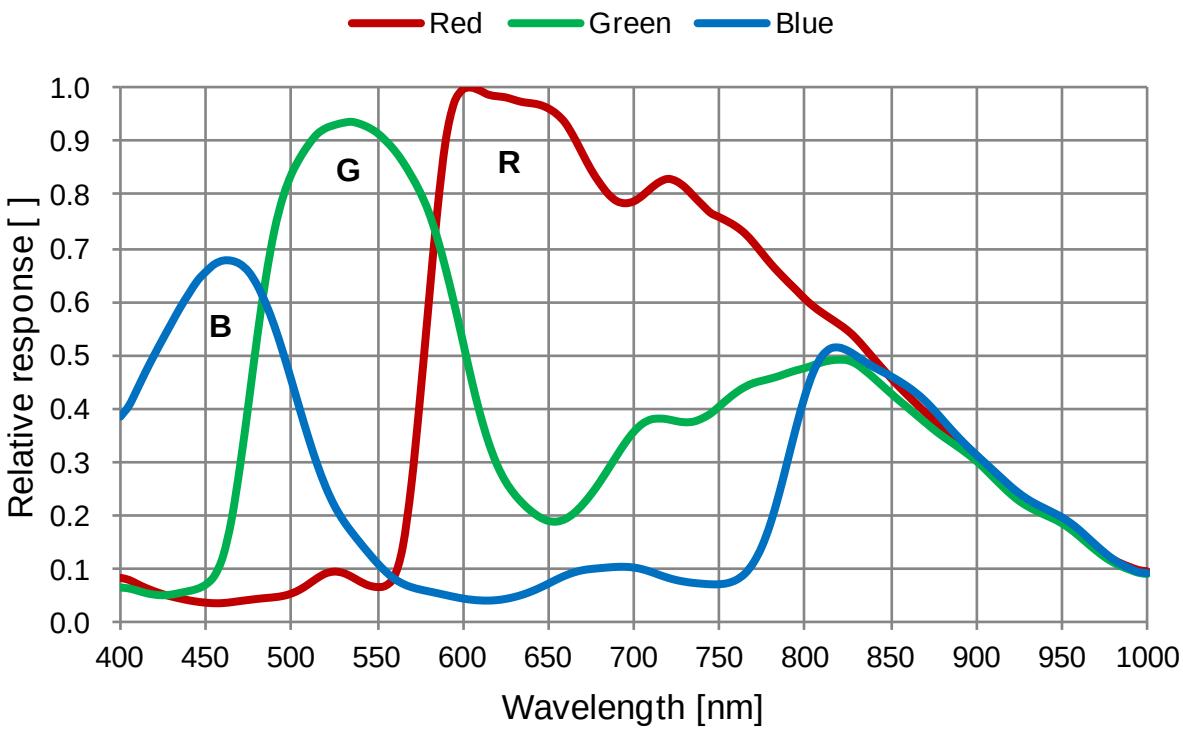


Image Sensor Characteristics

(AV_{DD} = 3.3 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, All-pixel scan mode, 12 bit 30 frame/s, Gain: 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		S	6472 (2040)	7456 (2350)	—	Digit (mV)	1	1/30 s storage 12 bit converted value HCG mode
			3236 (1020)	3728 (1175)	—	Digit (mV)		1/30 s storage 12 bit converted value LCG mode
Sensitivity ratio	R / G	RG	0.56	—	0.71	—	2	—
	B / G	BG	0.31	—	0.46	—		—
Saturation signal		Vsat	3839 (1210)	—	—	Digit (mV)	3	12 bit converted value LCG mode
Video signal shading		SH	—	—	25	%	4	—
Vertical line		VL	—	—	90	μV	5	12 bit converted value LCG mode
Dark signal		Vdt	—	—	0.48 (0.15)	Digit (mV)	6	1/30 s storage 12 bit converted value LCG mode
Dark signal shading		ΔVdt	—	—	0.48 (0.15)	Digit (mV)	7	1/30 s storage 12 bit converted value LCG mode
Conversion efficiency ratio		Rcg	1.8	2	2.2	—	—	HCG mode / LCG mode

Note)

1. Converted value into mV using 1Digit = 0.3152 mV for 12-bit output and 1Digit = 1.261 mV for 10-bit output.
2. The video signal shading is the measured value in the wafer status (including color filter) and does not include characteristics of the seal glass.
3. The characteristics above apply to effective pixel area that is shown below.

Zone Definition

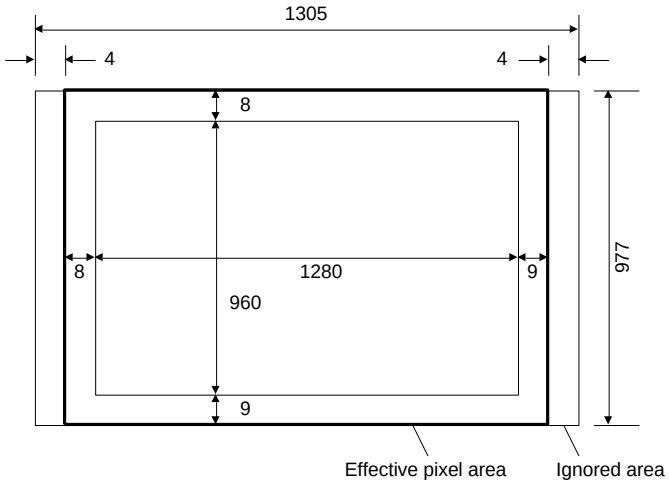


Image Sensor Characteristics Measurement Method

Measurement Conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr / Gb channel signal output or the R / B channel signal output of the measurement system.

Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance - 30 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   Sg = (VGr + VGb) / 2 × 100/30 [mV]

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to 1175 mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and the B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   VG = (VGr + VGb) / 2
   RG = VR / VG
   BG = VB / VG

3. Saturation signa l
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 500 mV, measure the average values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 1175 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   SH = (Gmax – Gmin) / 1175 × 100 [%]

5. Vertical line
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, calculates each average output of Gr, Gb, R and B on respective columns. Calculates maximum value of difference with adjacent column on the same color (VL [μV]).

6. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

7. Dark signal shading
   After the measurement item 5, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

   ΔVdt = Vdmax – Vdmin [mV]

Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by 4-wire serial communication and I^2C communication. See the Register Map for the addresses and setting values to be set. Because the two communication systems are judged at the first communication, once they are judged, the communication cannot be switched until sensor reset. The pin for 4-wire serial communication and I^2C communication is shared, so the external pin XCE must be fixed to power supply side when using I^2C communication.

Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

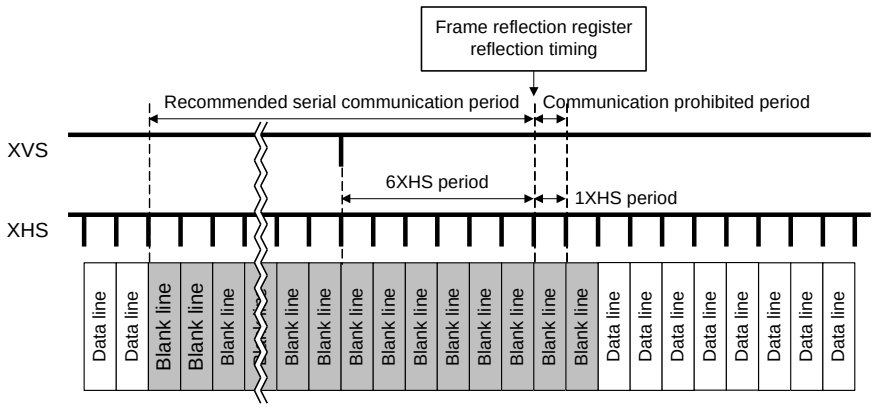
Chip ID	Start address	Data	Data	Data	…
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

Type and Description

Type	Description
ChipID	02h: Write to the Chip ID = 02h register 03h: Write to the Chip ID = 03h register 04h: Write to the Chip ID = 04h register 05h: Write to the Chip ID = 05h register 82h: Read from the Chip ID = 02h register 83h: Read from the Chip ID = 03h register 84h: Read from the Chip ID = 04h register 85h: Read from the Chip ID = 05h register
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

Register Communication Timing (4-wire)

Perform serial communication in sensor standby mode or within in the 6XHS period after the falling edge of XVS from the blanking line output start time after valid line of one frame is finished. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.) About REGHOLD register only, communication period is different than the other registers. For details, see section “Register Hold Settings”.



Register Write and Read (4-wire)

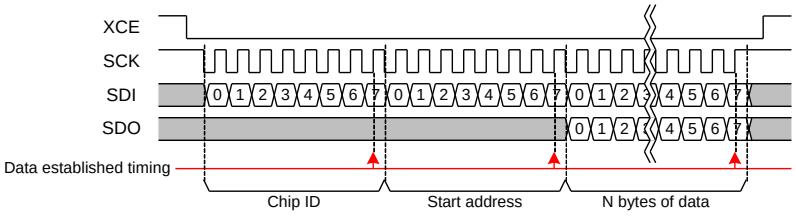
Follow the communication procedure below when writing registers.

1. Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
2. Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
3. Input Chip ID (CID = 02h or 03h or 04h or 05h) to the first byte. If the Chip ID differs, subsequent data is ignored.
4. Input the start address to the second byte. The address is automatically incremented.
5. Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
6. The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
7. Set XCE High to end communication.

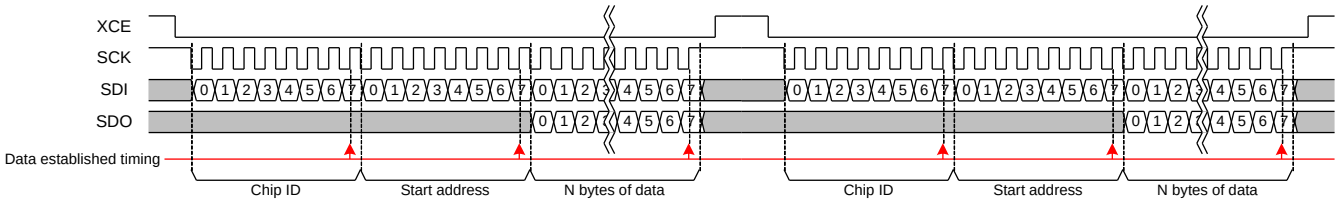
Follow the communication procedure below when reading registers.

1. Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
2. Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
3. Input Chip ID (CID = 82h or 83h or 84h or 85h) to the first byte. If the Chip ID differs, subsequent data is ignored.
4. Input the start address to the second byte. The address is automatically incremented.
5. Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
6. The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
7. Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



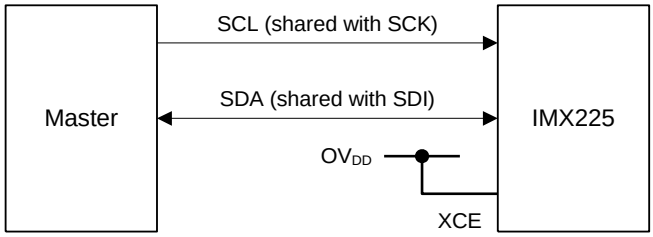
Serial Communication (Continuous Address)



Serial Communication (Discontinuous Address)

Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

SLAVE Address

MSB							LSB
0	0	1	1	0	1	0	R / W

* R/W is data direction bit

R / W

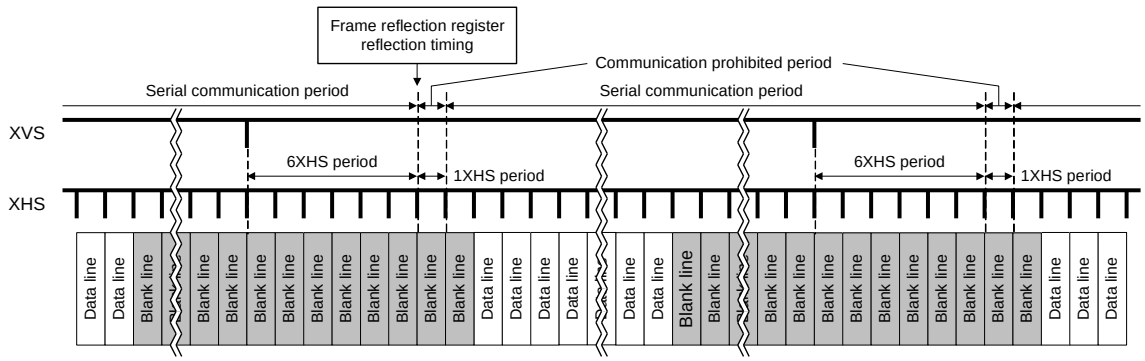
R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

I^2C pin description

Symbol	Pin No.	Remarks
SCL (Common to SCK)	G12	Serial clock input
SDA (Common to SDI)	E12	Serial data communication

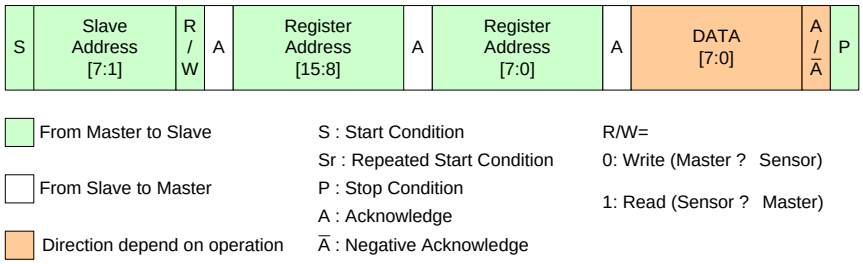
Register Communication Timing (I^2C)

In I^2C communication system, communication can be performed excluding during the period when communication is prohibited from the falling edge of XVS to 6H after (1H period). For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.) Using REG_HOLD function is recommended for register setting using I_2C communication. For REG_HOLD function, see “Register Transmission Setting” in “Description of Functions”. About REGHOLD register only, communication period is different than the other registers. For details, see section “Register Hold Settings”.



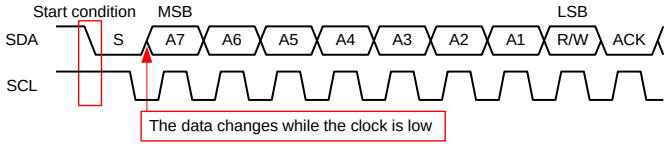
Communication Protocol

I^{2}C serial communication supports a 16-bit register address and 8-bit data message type.

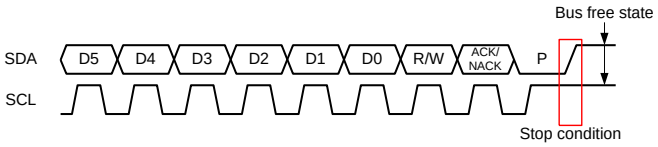


Communication Protocol

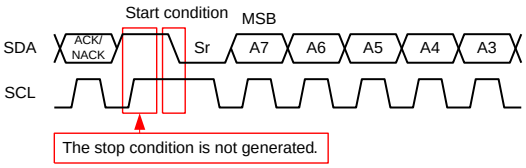
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / $\bar{A}$ (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SDL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

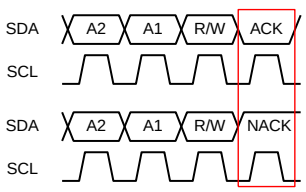


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.

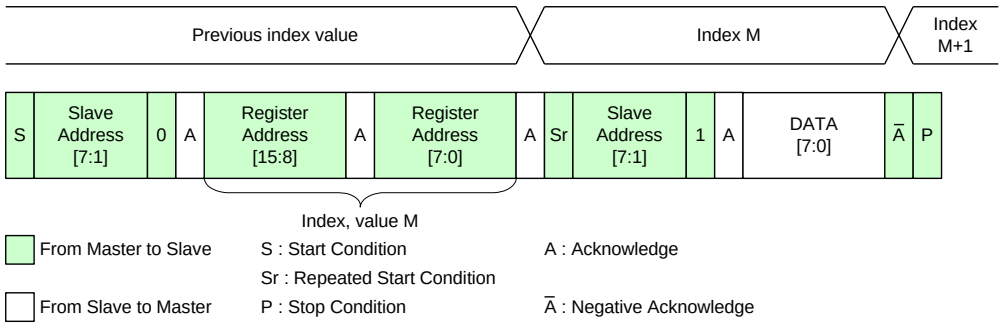


Acknowledge and Negative Acknowledge

Register Write and Read (I^2C)

Single Read from Random Location

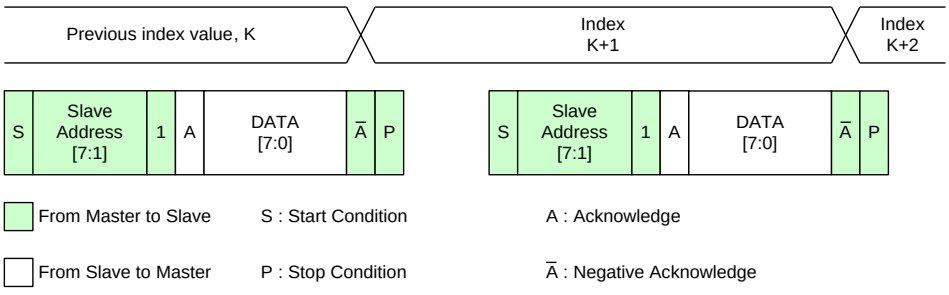
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data,it generates a Negative Acknowledge and the Stop Condition to end the communication



Single Read from Random Location

Single Read from Current Location

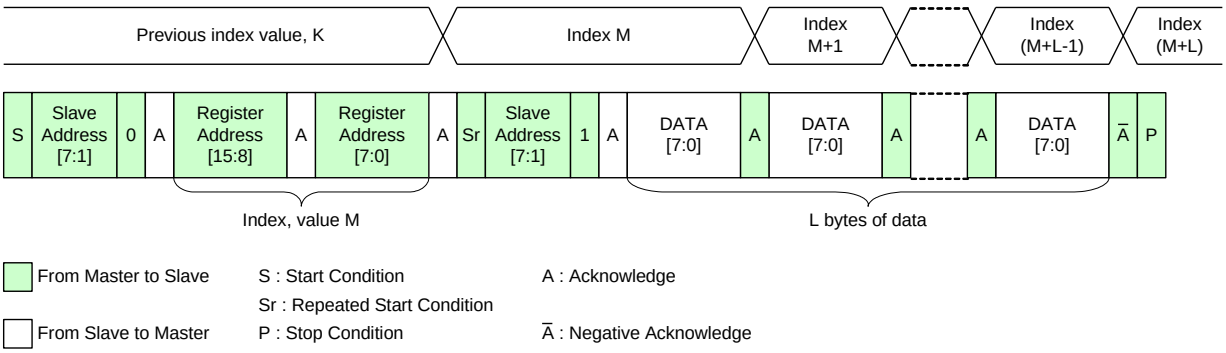
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

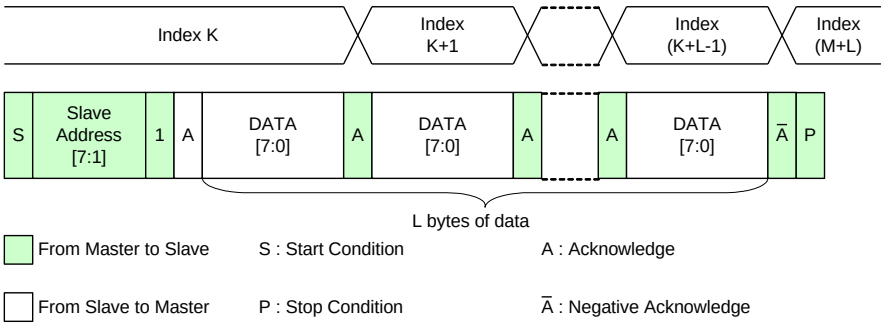
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

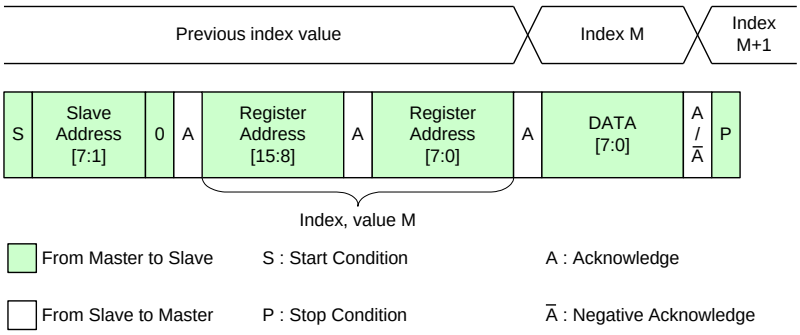
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

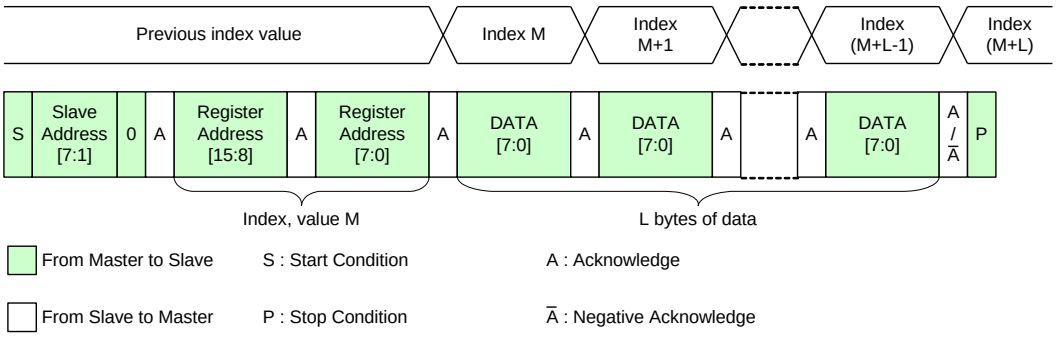
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

This sensor has a total of 1024 bytes (256 × 4) of registers, composed of registers with addresses 00h to FFh that correspond to Chip ID = 02h (write mode) / 82h (read mode), Chip ID = 03h (write mode) / 83h (read mode), Chip ID = 04h (write mode) / 84h (read mode), and Chip ID = 05h (write mode) / 85h (read mode). Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 1024 bytes.

The values must be changed from the default value, so initial setting after reset is required after power-on. There are two different register reflection timing. Values are reflected immediately after writing to register noted as “Immediately”, or at the frame reflection register reflection timing described in the item of “Register Communication Timing” in the section of “Setting Registers with Serial Communication” for registers noted as “V” in the Reflection timing column of the Register Map. For the immediate reflection registers other than belows, set them in sensor standby state.

STANDBY
REGHOLD
XMSTA
SW_RESET
XVSOUTSEL [1:0]
XHSOUTSEL [1:0]

Do not perform communication to addresses not listed in the Register Map. Doing so may result in operation errors. However, other registers that requires communication to address not listed above may be added, so addresses up to FEh should be supported for CID = 02h, 03h, 04h and 05h. (In I2C communication, address; 3000h to 30FFh, 3100h to 31FFh, 3200h to 32FFh, 3300h to 33FFh)

* For the register that is writing " * " to the setting value in description (Indicated by red letter), change the value from the default value after the reset.

** In Gain setting only, it is reflected on the next frame which was settings.

Registers corresponding to Chip ID = 02h in Write mode. (Read: Chip ID = 82h)

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
00h	3000h	0	STANDBY	Standby 0: Operating 1: Standby	1h	01h	Immediately
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
01h	3001h	0	REGHOLD	Register hold (Function not to update V reflection register) 0: Invalid 1: Valid	0h	00h	Immediately
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
02h	3002h	0	XMSTA	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1h	01h	Immediately
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
03h	3003h	0	SW_RESET	Software reset 0: Operating 1: Reset	0h	00h	Immediately
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
04h	3004h	[7:0]	—	Fixed to “10h”	10h	10h	—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
05h	3005h	0	ADBIT	AD conversion bits setting 0: 10 bit, 1: 12 bit	1h	01h	V
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
06h	3006h	0 1 2 3 4 5 6 7	MODE [7:0]	Drive mode setting (In WINMODE=1h, Set to value other than 00h is prohibited) 00h: All-pixel scan 22h: Horizontal / Vertical 2×2 binning 33h: Horizontal / Vertical 1/2 subsampling Others: Setting prohibited	00h	00h	V
07h	3007h	0	VREVERSE	Vertical (V) direction readout inversion control 0: Normal, 1: Inverted	0h	00h	V
		1	HREVERSE	Horizontal (H) direction readout inversion control 0: Normal, 1: Inverted	0h		V
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4 5 6	WINMODE [2:0]	Window mode setting 0: Quad VGA 1: HD720p 4: Window cropping from Quad VGA	0h		V
		7	—	Fixed to “0h”	0h		—
08h	3008h	[7:0]	—	Fixed to “00h”	00h	00h	—
09h	3009h	0 1	FRSEL [1:0]	Frame rate (Data rate) setting For details, see the register setting list in each operation mode.	1h	01h	V
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	FDG_SEL	Conversion gain switching 0: LCG Mode 1: HCG Mode	0h		V
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
0Ah	300Ah	0	BLKLEVEL [8:0]	LSB Black level offset value setting	0F0h	F0h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
0Bh	300Bh	0		MSB		00h	
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
0Ch	300Ch	[7:0]	—	Fixed to “00h”	00h	00h	—
0Dh	300Dh	[7:0]	—	Fixed to “00h”	00h	00h	—
0Eh	300Eh	[7:0]	—	Fixed to “01h”	01h	01h	—
0Fh	300Fh	[7:0]	—	Set to “00h” *	01h	01h	—
10h	3010h	[7:0]	—	Fixed to “01h”	01h	01h	—
11h	3011h	[7:0]	—	Fixed to “00h”	00h	00h	—
12h	3012h	[7:0]	—	Set to “2Ch” *	F0h	F0h	—
13h	3013h	[7:0]	—	Set to “01h” *	00h	00h	—
14h	3014h	0	GAIN [9:0]	LSB Gain setting (0.0 dB to 72.0 dB / 0.1 dB step)	000h	00h	V **
		1					
		2					
		3					
		4					
		5					
		6					
		7					
15h	3015h	0		MSB		00h	
		1					
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
16h	3016h	[7:0]	—	Set to “09h” *	08h	08h	—
17h	3017h	[7:0]	—	Fixed to “00h”	00h	00h	—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
18h	3018h	0	VMAX [16:0]	LSB When sensor master mode vertical span setting. (Number of operation lines count from 1) For details, see the item of "Slave Mode and Master Mode" in the section of "Description of Various Functions"	0044Ch	4Ch	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
19h	3019h	0				04h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
1Ah	301Ah	0	—	Fixed to “0h”	0h	00h	—
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
1Bh	301Bh	0	HMAX [13:0]	LSB When sensor master mode horizontal span setting. (Number of operation clocks count from 1) For details, see the item of "Slave Mode and Master Mode" in the section of "Description of Various Functions"	1194h	94h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Ch	301Ch	0				11h	
		1					
		2					
		3					
		4					
		5		MSB			
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
1Dh	301Dh	[7:0]	—	Set to “C2h” *	B2h	B2h	—
1Eh	301Eh	[7:0]	—	Fixed to “01h”	01h	01h	—
1Fh	301Fh	[7:0]	—	Fixed to “00h”	00h	00h	—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
20h	3020h	0	SHS1 [16:0]	LSB	00000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
21h	3021h	0		Storage time adjustment Designated in line units.		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
22h	3022h	0		MSB		00h	
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
23h to 35h	3023h to 3035h	[7:0] to [7:0]	—	Reserved	—	—	—
36h	3036h	0	WINWV_OB [4:0]	LSB In window cropping mode Cropping size designation (Vertical direction effective OB) MSB	10h	10h	V
		1					
		2					
		3					
		4					
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
37h	3037h	[7:0]	—	Fixed to “00h”	00h	00h	—
38h	3038h	0	WINPV [9:0]	LSB	000h	00h	V
		1					
		2					
		3					
		4		In window cropping mode Designation of upper left coordinate for cropping position (Vertical position)			
		5					
		6					
		7					
39h	3039h	0		MSB		00h	
		1					
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
3Ah	303Ah	0	WINWV [9:0]	LSB In window cropping mode Cropping size designation (Vertical direction	3D1h	D1h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Bh	303Bh	0				03h	
		1		MSB			
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
3Ch	303Ch	0	WINPH [10:0]	LSB In window cropping mode Designation of upper left coordinate for cropping position (horizontal position) Set to become the multiple of four	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Dh	303Dh	0				00h	
		1					
		2		MSB			
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
3Eh	303Eh	0	WINWH [10:0]	LSB In window cropping mode Cropping size designation (horizontal direction) Set to become the multiple of four	51Ch	1Ch	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Fh	303Fh	0				05h	
		1					
		2		MSB			
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
40h to 43h	3040h to 3043h	[7:0] to [7:0]	—	Reserved	—	—	—
44h	3044h	0	ODBIT	Number of output bit setting 0: 10 bit, 1: 12 bit * In CSI-2 mode (OMODE = Low), Fixed to “1h”.	1h	01h	Immediately
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	OPORTSEL [3:0]	Output interface selection (In CSI-2, don’t care. CSI-2 Interface will be selected by ChipID: 05h register.) 0h: Parallel CMOS SDR Ch: LVDS 1ch Dh: LVDS 2ch Eh: LVDS 4ch Others: Setting prohibited	0h		Immediately
		5					
		6					
		7					
45h	3045h	[7:0]	—	Fixed to "01h"	01h	01h	—
46h	3046h	0	—	Fixed to “0h”	0h	00h	—
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	XVSLNG [1:0]	XVS pulse width setting in master mode. (In slave mode, setting is invalid.) 0: 1H, 1: 2H, 2: 4H, 3: 8H	0h		Immediately
		5					
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
47h	3047h	0	—	Fixed to “0h”	0h	08h	—
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “1h”	1h		—
		4	XHSLNG [1:0]	XHS pulse width setting in master mode. (In slave mode, setting is invalid.) 0: Min. to 3: Max.	0h		Immediately
		5					
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
48h	3048h	[7:0]	—	Fixed to "00h"	00h	00h	—
49h	3049h	0	XVSOUTSEL [1:0]	XVS pin setting in master mode 0: Fixed to High 2: VSYNC output Others: Setting prohibited	0h	00h	Immediately
		1					
		2	XHSOUTSEL [1:0]	XHS pin setting in master mode 0: Fixed to High 2: HSYNC output Others: Setting prohibited	0h		Immediately
		3					
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
4Ah to 53h	304Ah to 3053h	[7:0] to [7:0]	—	Reserved	—	—	—
54h	3054h	[7:0]	—	CMOS / LVDS output: Fixed to “67h” CSI-2 output: Set to “66h”	67h	67h	Immediately
55h to 5Bh	3055h to 305Bh	[7:0] to [7:0]	—	Reserved	—	—	—
5Ch	305Ch	[7:0]	INCKSEL1	The value is set according to INCK.	2Ch	2Ch	Immediately
5Dh	305Dh	[7:0]	INCKSEL2	The value is set according to INCK.	10h	10h	Immediately
5Eh	305Eh	[7:0]	INCKSEL3	The value is set according to INCK.	2Ch	2Ch	Immediately
5Fh	305Fh	[7:0]	INCKSEL4	The value is set according to INCK.	10h	10h	Immediately
60h to 6Fh	3060h to 306Fh	[7:0] to [7:0]	—	Reserved	—	—	—
70h	3070h	[7:0]	—	Set to “02h” *	01h	01h	Immediately
71h	3071h	[7:0]	—	Set to “01h” *	00h	00h	Immediately
72h to 9Dh	3072h to 309Dh	[7:0] to [7:0]	—	Reserved	—	—	—
9Eh	309Eh	[7:0]	—	Set to “22h” *	20h	20h	Immediately
9Fh to A4h	309Fh to 30A4h	[7:0] to [7:0]	—	Reserved	—	—	—
A5h	30A5h	[7:0]	—	Set to “FBh” *	2Ah	2Ah	Immediately
A6h	30A6h	[7:0]	—	Set to “02h” *	00h	00h	Immediately
A7h to B2h	30A7h to 30B2h	[7:0] to [7:0]	—	Reserved	—	—	—
B3h	30B3h	[7:0]	—	Set to “FFh” *	7Fh	7Fh	Immediately
B4h	30B4h	[7:0]	—	Set to “01h” *	02h	02h	Immediately
B5h	30B5h	[7:0]	—	Set to “42h” *	41h	41h	Immediately
B6h to B7h	30B6h to 30B7h	[7:0] to [7:0]	—	Reserved	—	—	—
B8h	30B8h	[7:0]	—	Set to “10h” *	12h	12h	Immediately
B9h to C1h	30B9h to 30C1h	[7:0] to [7:0]	—	Reserved	—	—	—
C2h	30C2h	[7:0]	—	Set to “01h” *	03h	03h	Immediately
C3h to FFh	30C3h to 30FFh	[7:0] to [7:0]	—	Reserved	—	—	—

Registers corresponding to Chip ID = 03h in Write mode. (Read: Chip ID = 83h)

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
00h to 0Eh	3100h to 310Eh	[7:0] to [7:0]	—	Reserved	—	—	—
0Fh	310Fh	[7:0]	—	Set to “0Fh” *	16h	16h	Immediately
10h	3110h	[7:0]	—	Set to “0Eh” *	16h	16h	Immediately
11h	3111h	[7:0]	—	Set to “E7h” *	00h	00h	Immediately
12h	3112h	[7:0]	—	Set to “9Ch” *	00h	00h	Immediately
13h	3113h	[7:0]	—	Set to “83h” *	00h	00h	Immediately
14h	3114h	[7:0]	—	Set to “10h” *	00h	00h	Immediately
15h	3115h	[7:0]	—	Set to “42h” *	00h	00h	Immediately
16h to 27h	3116h to 3127h	[7:0] to [7:0]	—	Reserved	—	—	—
28h	3128h	[7:0]	—	Set to “1Eh” *	00h	00h	Immediately
29h to ECh	3129h to 31ECh	[7:0] to [7:0]	—	Reserved	—	—	—
EDh	31EDh	[7:0]	—	Set to “38h” *	0Eh	0Eh	Immediately
EFh to FFh	31EFh to 31FFh	[7:0] to [7:0]	—	Reserved	—	—	—

Registers corresponding to Chip ID = 04h in Write mode. (Read: Chip ID = 84h)

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
00h to 0Bh	3200h to 320Bh	[7:0] to [7:0]	—	Reserved	—	—	—
0Ch	320Ch	[7:0]	—	Set to “CFh” *	D4h	D4h	Immediately
0Dh to 4Bh	320Dh to 324Bh	[7:0] to [7:0]	—	Reserved	—	—	—
4Ch	324Ch	[7:0]	—	Set to “40h” *	D0h	D0h	Immediately
4Dh	324Dh	[7:0]	—	Set to “03h” *	01h	01h	Immediately
4Eh to 60h	324Eh to 3260h	[7:0] to [7:0]	—	Reserved	—	—	—
61h	3261h	[7:0]	—	Set to “E0h” *	70h	70h	Immediately
62h	3262h	[7:0]	—	Set to “02h” *	01h	01h	Immediately
63h to 6Dh	3263h to 326Dh	[7:0] to [7:0]	—	Reserved	—	—	—
6Eh	326Eh	[7:0]	—	Set to “2Fh” *	18h	18h	Immediately
6Fh	326Fh	[7:0]	—	Set to “30h” *	C0h	C0h	Immediately
70h	3270h	[7:0]	—	Set to “03h” *	01h	01h	Immediately
71h to 97h	3271h to 3297h	[7:0] to [7:0]	—	Reserved	—	—	—
98h	3298h	[7:0]	—	Set to “00h” *	40h	40h	Immediately
99h	3299h	[7:0]	—	Reserved	—	—	—
9Ah	329Ah	[7:0]	—	Set to “12h” *	E0h	E0h	Immediately
9Bh	329Bh	[7:0]	—	Set to “F1h” *	C0h	C0h	Immediately
9Ch	329Ch	[7:0]	—	Set to “0Ch” *	0Dh	0Dh	Immediately
9Dh to FFh	329Dh to 32FFh	[7:0] to [7:0]	—	Reserved	—	—	—

Registers corresponding to Chip ID = 05h in Write mode. (Read: Chip ID = 85h)
* These registers are set in CSI-2 interface only.

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
00h to 43h	3300h to 3343h	[7:0] to [7:0]	—	Reserved	—	—	—
44h	3344h	0	—	Fixed to “0h”	0h	20h	—
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	REPETITION [1:0]	* Refer to “Output signal Interface Control” section.	2h		Immediately
		5					
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
45h	3345h	[7:0]	—	Fixed to "00h"	00h	00h	—
46h	3346h	0	PHYSICAL_LANE_NUM [1:0]	Physically connect the Lane number	3h	03h	Immediately
		1					
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
47h to 52h	3347h to 3352h	[7:0] to [7:0]	—	Reserved	—	—	—
53h	3353h	0	OB_SIZE_V [5:0]	LSB Vertical (V) direction OB width setting. * Refer to each operating setting. MSB	0Eh	0Eh	Immediately
		1					
		2					
		3					
		4					
		5					
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
47h to 52h	3347h to 3352h	[7:0] to [7:0]	—	Reserved	—	—	—
57h	3357h	0	PIC_SIZE_V [12:0]	LSB Vertical (V) direction effective pixel width setting. * Refer to each operating setting.	03D1h	D1h	Immediately
		1					
		2					
		3					
		4					
		5					
		6					
		7					
58h	3358h	0				03h	
		1					
		2					
		3					
		4		MSB			
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
59h to 6Ah	3359h to 336Ah	[7:0] to [7:0]	—	Reserved	—	—	—
6Bh	336Bh	[7:0]	THSEXIT	Global timing setting	27h	27h	Immediately
6Ch	336Ch	[7:0]	TCLKPRE	Global timing setting	1Fh	1Fh	Immediately
6Dh to 7Ch	336Dh to 337Ch	[7:0] to [7:0]	—	Reserved	—	—	—
7Dh	337Dh	[7:0]	CSI_DT_FMT [15:0]	LSB RAW10: 0A0Ah / RAW12: 0C0Ch MSB	0C0Ch	0Ch	Immediately
7Eh	337Eh	[7:0]				0Ch	
7Fh	337Fh	0	CSI_LANE_MODE [1:0]	Lane number setting 0: 1Lane, 1: 2Lane, 3: 4Lane 2: Setting prohibited	3h	03h	Immediately
		1					
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
80h	3380h	[7:0]	INCK_FREQ1 [15:0]	LSB Master clock frequency 1B00h: INCK = 27 MHz 3600h: INCK = 54 MHz 2520h: INCK = 37.125 MHz 4A40h: INCK = 74.25MHz MSB	3600h	00h	Immediately
81h	3381h	[7:0]				36h	
82h	3382h	[7:0]	TCLKPOST	Global timing setting	57h	57h	Immediately
83h	3383h	[7:0]	THSPREPARE	Global timing setting	0Fh	0Fh	Immediately
84h	3384h	[7:0]	THSZERO	Global timing setting	27h	27h	Immediately
85h	3385h	[7:0]	THSTRAIL	Global timing setting	0Fh	0Fh	Immediately
86h	3386h	[7:0]	TCLKTRAIL	Global timing setting	0Fh	0Fh	Immediately
87h	3387h	[7:0]	TCLKPREPARE	Global timing setting	07h	07h	Immediately
88h	3388h	[7:0]	TCLKZERO	Global timing setting	37h	37h	Immediately
89h	3389h	[7:0]	TLPX	Global timing setting	1Fh	1Fh	Immediately
8Ah	338Ah	[7:0]	—	Fixed to "30h"	30h	30h	—
8Bh	338Bh	[7:0]	—	Fixed to "30h"	30h	30h	—
8Ch	338Ch	[7:0]	—	Fixed to "30h"	30h	30h	—
8Dh	338Dh	[7:0]	INCK_FREQ2 [10:0]	LSB Master clock frequency 13Dh: INCK = 27 MHz 279h: INCK = 54 MHz 1B4h: INCK = 37.125 MHz 367h: INCK = 74.25MHz MSB	367h	67h	Immediately
8Eh	338Eh	[2:0]				03h	
		[7:3]	—	Fixed to "00h"	00h		—
8Fh to FFh	338Fh to 33FFh	[7:0] to [7:0]	—	Reserved	—	—	—

Readout Drive mode

The table below lists the operating modes available with this sensor. (N/A: Not supported mode)

Window	Mode	INCK [MHz]	AD conversion [bit]	Output bit width [bit]	Frame rate [frame/s]	Data rate						
						Parallel CMOS [Mpixel/s]	Serial LVDS [Mbps/ch]			CSI-2 [Mbps/Lane]		
							1 ch	2ch	4 ch	1 Lane	2 Lane	4 Lane
Quad VGA	All pixel	27 54 37.125 74.25	10/12	10/12	30 / 25	74.25	594	297	148.5	594	297	148.5
			10/12	10/12	60 / 50	N/A	N/A	594	297	N/A	594	297
			10	10	120 / 100	N/A	N/A	N/A	594	N/A	N/A	594
	2×2 binning	27 54 37.125 74.25	10	12	30 / 25	18.5625	148.5	74.25	37.125	N/A	N/A	N/A
			10	12	60 / 50	N/A	N/A	148.5	74.25	N/A	N/A	N/A
			10	12	120 / 100	N/A	N/A	N/A	148.5	N/A	N/A	N/A
	1/2 subsampling	27 54 37.125 74.25	10/12	10/12	60 / 50	37.125	297	148.5	74.25	N/A	N/A	N/A
			10/12	10/12	120 / 100	N/A	N/A	297	148.5	N/A	N/A	N/A
			10	10	240 / 200	N/A	N/A	N/A	297	N/A	N/A	N/A
	Window cropping	27 54 37.125 74.25	10/12	10/12	*1	74.25	594	297	148.5	594	297	148.5
			10/12	10/12	*2	N/A	N/A	594	297	N/A	594	297
			10	10	*3	N/A	N/A	N/A	594	N/A	N/A	594
HD720p	All-pixel	37.125 74.25	10/12	10/12	30	37.125	594	297	148.5	594	297	148.5
			10/12	10/12	60	74.25	N/A	594	297	N/A	594	297
			10	10	120	N/A	N/A	N/A	594	N/A	N/A	594

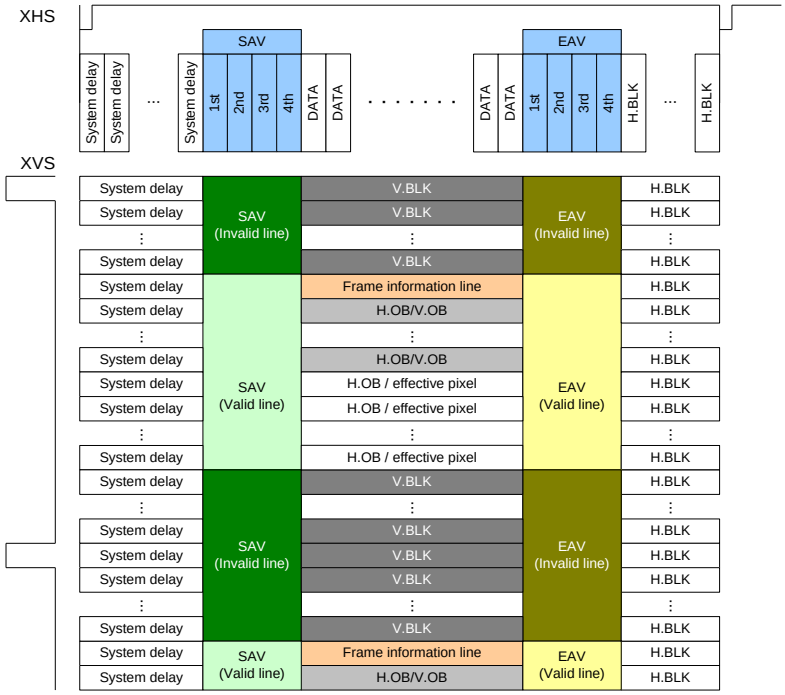
*1: FRSEL = 2h (In parallel CMOS output: FRSEL = 1h)
*2: FRSEL = 1h
*3: FRSEL = 0h

Window	Mode	INCK [MHz]	Frame rate [frame/s]	Recording pixels		Total number of pixels				1H period [µs]
				H [pixels]	V [lines]	H [pixels]			V [lines]	
						CMOS (10bit/ 12bit)	LVDS CSI-2 (10bit)	LVDS CSI-2 (12bit)		
Quad VGA	All-pixel	27 54 37.125 74.25	25	1280	960	2250	1800	1500	1320	30.303
			30			2250		1500	1100	
			50			N/A		1500	1320	15.152
			60			N/A		1500	1100	
			100			N/A		N/A	1320	7.576
			120			N/A		N/A	1100	
	2×2 binning	27 54 37.125 74.25	25	640	480	1125	N/A	750	660	60.606
			30			1125			550	
			50			N/A			660	30.303
			60			N/A			550	
			100			N/A			660	15.152
			120			N/A			550	
	1/2 subsampling	27 54 37.125 74.25	50	640	480	1125	900	750	660	30.303
			60			1125		750	550	
			100			N/A		750	660	15.152
			120			N/A		750	550	
			200			N/A		N/A	660	7.576
			240			N/A		N/A	550	
	Window cropping	27 54 37.125 74.25	*1	*4	*4	2250	1800	1500	*5	30.303
			*2			N/A		1500		15.152
			*3			N/A		N/A		7.576
HD720p	All-pixel	37.125 74.25	30	1280	720	1650	2640	2200	750	44.444
			60			1650		2200		22.222
			120			N/A		N/A		11.111

*1: FRSEL = 2h (In parallel CMOS output: FRSEL = 1h)
*2: FRSEL = 1h
*3: FRSEL = 0h
*4: Arbitrary value that was designated to cropping area
*5: Please refer to description of window cropping mode

Sync code (Parallel CMOS output / Serial LVDS output)

The sync code is added immediately before and after “dummy signal + OB signal + effective pixel data” and then output. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd.
(BLK: Blanking period)



Sync Code Output Timing

List of Sync Code

Sync code	1st code		2nd code		3rd code		4th code	
	10bit	12bit	10bit	12bit	10bit	12bit	10bit	12bit
SAV(Valid line)	3FFh	FFFh	000h	000h	000h	000h	200h	800h
EAV(Valid line)	3FFh	FFFh	000h	000h	000h	000h	274h	9D0h
SAV(Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2ACh	AB0h
EAV(Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2D8h	B60h

(Note 1) 10 bit is the value output to the DLOP/M [B:F] when the register ODBIT = 0 in parallel output.
(Note 2) 12 bit is the value output to the DLOP/M [A:F] when the register ODBIT = 1 in parallel output.
(Note 3) They are output to each channel seriously in MSB first when low-voltage LVDS serial.
For details, see the item of "Signal output" and "Output pin setting".

Sync Code Output Timing

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.

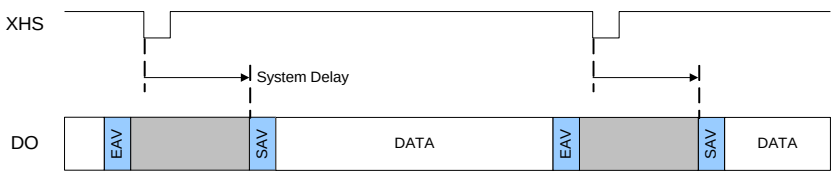


Image Data Output Format (CSI-2 output)

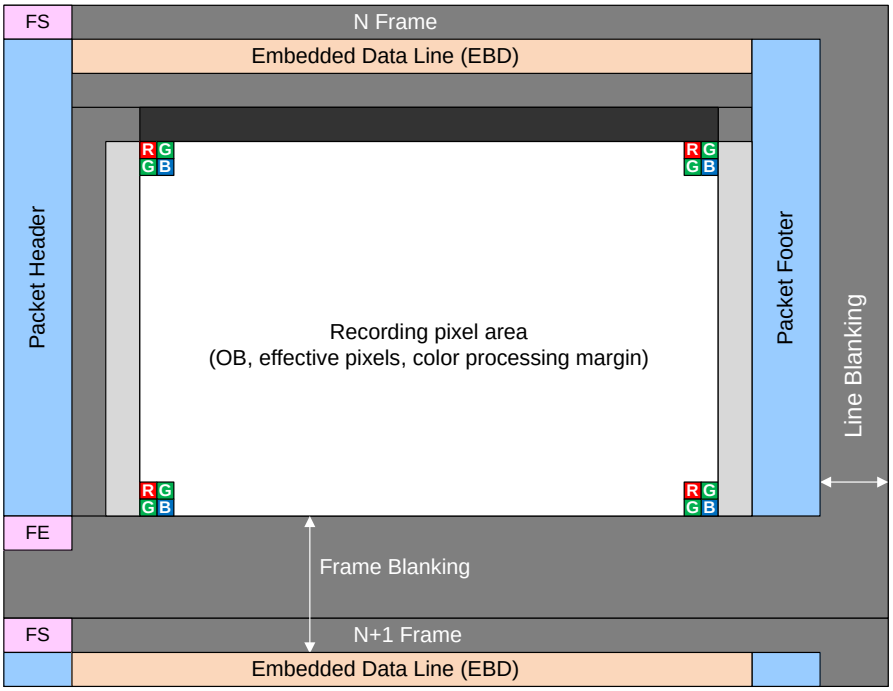
Frame Format

Each line of each image frame is output like the General Frame Format of CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Setting register (I^2C)	Description
00h	Frame Start Code	N/A	FS
01h	Frame End Code	N/A	FE
10h	NULL	N/A	Invalid data
12h	Embedded Data	N/A	Embedded data
2Bh	RAW10	Address: 7Dh, 7Eh (337Dh, 337Eh) CSI_DT_FMT [15:0]	0A0Ah
2Ch	RAW12		0C0Ch
37h	OB Data	N/A	Vertical OB line data

Frame Structure



Frame Structure of CSI-2 output

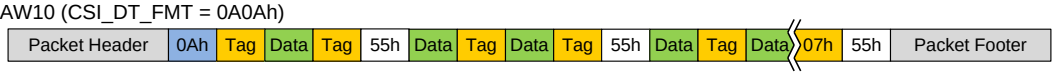
Embedded Data Line

The Embedded data line is output in a line following the sync code FS.

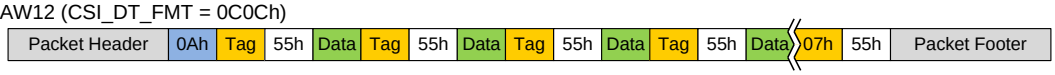
Embedded Data Format



RAW10 (CSI_DT_FMT = 0A0Ah)



RAW12 (CSI_DT_FMT = 0C0Ch)



The end of the address and the register value is determined according to the tags embedded in the data.

Embedded Data Line Tag

Tag	Data Byte Description
00h	Illegal Tag. If found; treat as end of Data.
07h	End of Data.
AAh	CCI Register Index MSB [15:8]
A5h	CCI Register Index LSB [7:0]
5Ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data.
55h	Auto increment the CCI index after the data byte – null data A CCI register does not exist for the current CCI index. The data byte value is the 07h.
FFh	Illegal Tag. If found; treat as end of Data.

Specific output examples are shown below. (4-wire: Chip ID = 05h)

Pixel	Address [HEX]		Data Byte Description	Value
	4-wire	I²C		
1	-		Data Format	0Ah
2				AAh
3			CCI Register Index MSB [15:8]	33h
4				A5h
5			CCI Register Index LSB [7:0]	95h
6				5Ah
7	95h	3395h		00h
8			REGHOLD value	5Ah
9	96h	3396h		[0]*
10				5Ah
11	97h	3397h	Fixed to “00h”	00h
12				5Ah
13	98h	3398h	Fixed to “00h”	00h
14				5Ah
15	99h	3399h	Fixed to “24h”	24h
16				5Ah
17	9Ah	339Ah	Fixed to “02h”	02h
18				5Ah
19	9Bh	339Bh	Fixed to “01h”	01h
20				5Ah
21	9Ch	339Ch	Fixed to “01h”	01h
22			Frame count	5Ah
23	9Dh	339Dh		[7:0]*
24				5Ah
25	9Eh	339Eh	Fixed to “01h”	01h
26				5Ah
27	9Fh	339Fh		[7:0]*
28			Black level setting value	5Ah
29	A0h	33A0h		[15:8]*
30				5Ah
31	A1h	33A1h	Data format RAW10: 0A0Ah	[7:0]*
32				5Ah
33	A2h	33A2h	RAW12: 0C0Ch	[15:8]*
34				5Ah
35	A3h	33A3h	Fixed to “00h”	00h
36				5Ah
37	A4h	33A4h	Fixed to “00h”	00h
38				5Ah
39	A5h	33A5h	Fixed to “00h”	00h
40				5Ah
41	A6h	33A6h	Fixed to “F0h”	F0h
42				5Ah
43	A7h	33A7h	Fixed to “00h”	00h
44				5Ah
45	A8h	33A8h	Fixed to “01h”	01h
46				5Ah
47	A9h	33A9h	Fixed to “00h”	00h
48				5Ah
49	AAh	33AAh	Fixed to “00h”	00h
50				5Ah
51	ABh	33ABh	Fixed to “00h”	00h
52				5Ah
53	ACh	33ACh	Fixed to “00h”	00h

Pixel	Address [HEX]		Data Byte Description	Value
	4-wire	I²C		
54				5Ah
55	ADh	33ADh	Fixed to “F0h”	F0h
56				5Ah
57	AEh	33AEh	Fixed to “00h”	00h
58				5Ah
59	AFh	33AFh	Fixed to “01h”	01h
60				5Ah
61	B0h	33B0h	Fixed to “00h”	00h
62				5Ah
63	B1h	33B1h	Fixed to “F0h”	F0h
64				5Ah
65	B2h	33B2h	Fixed to “00h”	00h
66				5Ah
67	B3h	33B3h	Gain Setting Value	[7:0]*
68				5Ah
69	B4h	33B4h		[15:8]*
70				5Ah
71	B5h	33B5h	Shutter setting value	[7:0]*
72				5Ah
73	B6h	33B6h		[15:8]*
74				5Ah
75	B7h	33B7h	Fixed to “00h”	00h
76				5Ah
77	B8h	33B8h	Fixed to “00h”	00h
78				5Ah
79	B9h	33B9h	Fixed to “00h”	00h
80				5Ah
81	BAh	33BAh	Fixed to “00h”	00h
82				5Ah
83	BBh	33BBh	Fixed to “00h”	00h
84				5Ah
85	BCh	33BCh	Fixed to “00h”	00h
86				5Ah
87	BDh	33BDh	Fixed to “00h”	00h
88				5Ah
89	BEh	33BEh	Fixed to “00h”	00h
90				5Ah
91	BFh	33BFh	Fixed to “00h”	00h
92				5Ah
93	C0h	33C0h	Fixed to “00h”	00h
94				5Ah
95	C1h	33C1h	Fixed to “00h”	00h
96				5Ah
97	C2h	33C2h	Fixed to “00h”	00h
98				5Ah
99	C3h	33C3h	Fixed to “00h”	00h
100				5Ah
101	C4h	33C4h	Fixed to “00h”	00h
102				5Ah
103	C5h	33C5h	Fixed to “00h”	00h
104				5Ah
105	C6h	33C6h	Fixed to “00h”	00h
106				5Ah
107	C7h	33C7h	Fixed to “00h”	00h

Pixel	Address [HEX]		Data Byte Description	Value
	4-wire	I²C		
108				5Ah
109	C8h	33C8h	Fixed to “00h”	00h
110				5Ah
111	C9h	33C9h	Vertical line value	[7:0]*
112			(VMAX)	5Ah
113	CAh	33CAh		[15:8]*
114				5Ah
115	CBh	33CBh	Fixed to “00h”	00h
116				5Ah
117	CCh	33CCh	Horizontal clock value	[7:0]*
118			(HMAX)	5Ah
119	CDh	33CDh		[15:8]*
20				5Ah
121	CEh	33CEh	Fixed to “00h”	00h
122				5Ah
123	CFh	33CFh	Fixed to “00h”	00h
124				5Ah
125	D0h	33D0h	Fixed to “00h”	00h
126				5Ah
127	D1h	33D1h	Fixed to “00h”	00h
128				5Ah
129	D2h	33D2h	Fixed to "9Bh"	9Bh
130				5Ah
131	D3h	33D3h	Fixed to "07h"	07h
132				5Ah
133	D4h	33D4h	Fixed to "C8h"	C8h
134				5Ah
135	D5h	33D5h	Fixed to "04h"	04h
136				5Ah
137	D6h	33D6h	Fixed to "9Ch"	9Ch
138				5Ah
139	D7h	33D7h	Fixed to "07h"	07h
140				5Ah
141	D8h	33D8h	Fixed to "C9h"	C9h
142				5Ah
143	D9h	33D9h	Fixed to "04h"	04h
144				5Ah
145	DAh	33DAh	Fixed to “00h”	00h
146				5Ah
147	DBh	33DBh	Fixed to “00h”	00h
148				5Ah
149	DCh	33DCh	Fixed to “00h”	00h
150				5Ah
151	DDh	33DDh	Fixed to “00h”	00h
152				5Ah
153	DEh	33DEh	Fixed to “00h”	00h
154				5Ah
155	DFh	33DFh	Fixed to “00h”	00h
156				5Ah
157	E0h	33E0h	Fixed to "1Bh"	1Bh
158				5Ah
159	E1h	33E1h	Fixed to "05h"	05h
160				5Ah
161	E2h	33E2h	Fixed to "D0h"	D0h

Pixel	Address [HEX]		Data Byte Description	Value
	4-wire	I²C		
162				5Ah
163	E3h	33E3h	Fixed to "03h"	03h
164				5Ah
165	E4h	33E4h	Fixed to "7Ch"	7Ch
166				5Ah
167	E5h	33E5h	Fixed to “01h”	01h
168				5Ah
169	E6h	33E6h	Fixed to "31h"	31h
170				5Ah
171	E7h	33E7h	Fixed to “01h”	01h
172				5Ah
173	E8h	33E8h	Fixed to "1Ch"	1Ch
174				5Ah
175	E9h	33E9h	Fixed to "05h"	05h
176				5Ah
177	EAh	33EAh	Fixed to "D1h"	D1h
178				5Ah
179	EBh	33EBh	Fixed to "03h"	03h
180				5Ah
181	ECh	33ECh	Fixed to “01h”	01h
182			Number of lane	5Ah
183	EDh	33EDh		[1:0]*
184				5Ah
185	EEh	33EEh	Fixed to “00h”	00h
186				5Ah
187	EFh	33EFh	Fixed to “00h”	00h
188				5Ah
189	F0h	33F0h	Fixed to "0Bh"	0Bh
190				5Ah
191	F1h	33F1h	Fixed to “00h”	00h
192				5Ah
193	F2h	33F2h	Fixed to "0Ch"	0Ch
194				5Ah
195	F3h	33F3h	Fixed to “00h”	00h
196				5Ah
197	F4h	33F4h	Fixed to “00h”	00h
198				5Ah
199	F5h	33F5h	Fixed to “00h”	00h
200				5Ah
201	F6h	33F6h	Fixed to "0Fh"	0Fh
202				5Ah
203	F7h	33F7h	Fixed to “00h”	00h
204				5Ah
205	F8h	33F8h	Fixed to "06h"	06h
206				5Ah
207	F9h	33F9h	Fixed to “00h”	00h
208				5Ah
209	FAh	33FAh	Fixed to "10h"	10h
210				5Ah
211	FBh	33FBh	Fixed to “00h”	00h
212				07h
213	—	—	End of Data.	07h
214				07h

* The value that shown in Data Byte Description is output.

Image Data Output Format

All-pixel scan mode (Quad VGA)

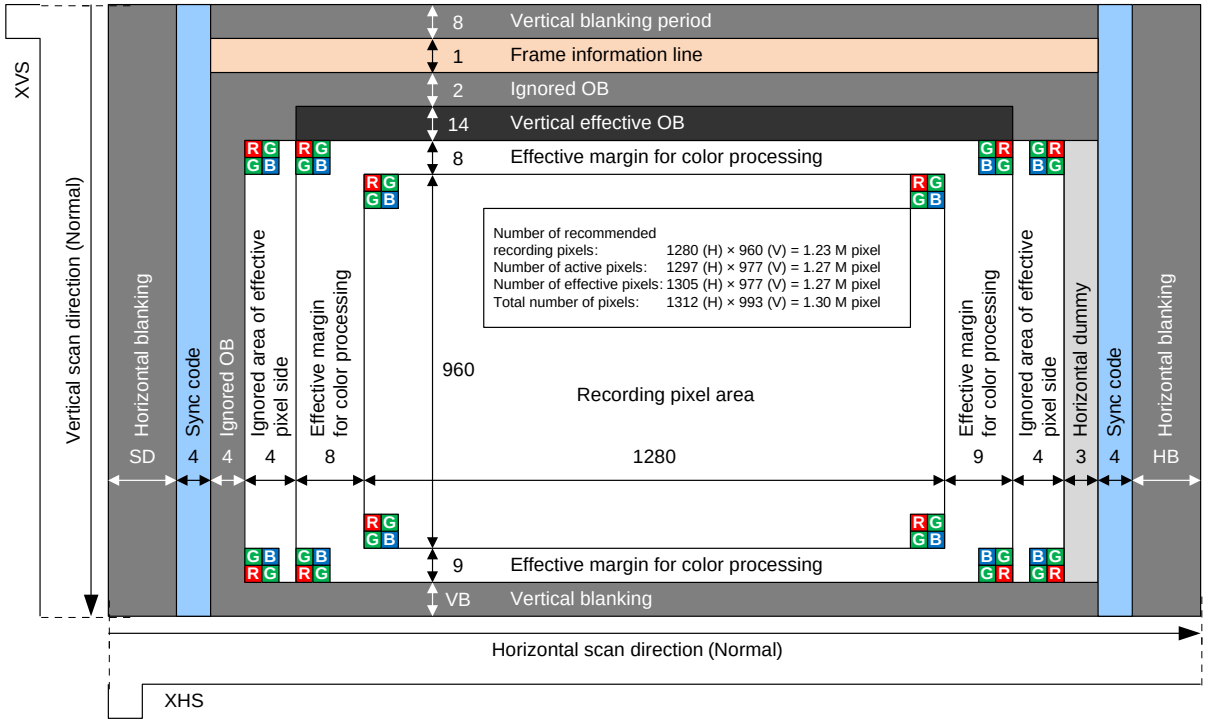
List of Setting Register for CMOS parallel / LVDS serial output

Address		bit	Register Name	Initial	CMOS	LVDS serial			Remarks
4-wire	I2C			Value	parallel	1 ch	2 ch	4 ch	
Chip ID: 02h									
05h	3005h	[0]	ADBIT	0h	0h / 1h				0: 10 bit, 1: 12 bit
06h	3006h	[7:0]	MODE	00h	00h				All-pixel scan
07h	3007h	[0]	VREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	0h				Quad-VGA
09h	3009h	[1:0]	FRSEL	1h	1h	2h			30 / 25 [frame/s]
					N/A	N/A	1h		60 / 50 [frame/s]
					N/A	N/A	N/A	0h	120 / 100 [frame/s]
		[4]	FDG_SEL	0h	0h / 1h				0: LCG mode, 1: HCG mode
18h	3018h	[7:0]	VMAX	44Ch	44Ch / 528h				44Ch: 30 / 60 / 120 [frame / s]
19h	3019h	[3:0]							528h: 25 / 50 / 100 [frame / s]
1Bh	301Bh	[7:0]	HMAX	1194h	1194h				30 / 25 [frame/s]
1Ch	301Ch	[5:0]			N/A	N/A	08CAh		60 / 50 [frame/s]
					N/A	N/A	N/A	465h	120 / 100 [frame/s]
44h	3044h	[1:0]	ODBIT	1h	0h / 1h				0: 10 bit, 1: 12 bit
		[7:4]	OPORTSEL	0h	0h	Ch	Dh	Eh	I/F selection
54h	3054h	[7:0]	—	67h	67h				CMOS / LVDS setting
5Ch	305Ch	[7:0]	INCKSEL1	2Ch	2Ch / 20h				Set according to INCK
5Dh	305Dh	[7:0]	INCKSEL2	10h	10h / 00h				Set according to INCK
5Eh	305Eh	[7:0]	INCKSEL3	2Ch	2Ch / 20h				Set according to INCK
5Fh	305Fh	[7:0]	INCKSEL4	10h	10h / 00h				Set according to INCK
60h to FFh	3060h to 30FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
Chip ID = 03h									
00h to FFh	3100h to 31FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
Chip ID = 04h									
00h to FFh	3200h to 32FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
ChipID = 05h									
00h to FFh	3300h to 33FFh	[7:0] to [7:0]	Changing the value is not necessary.						

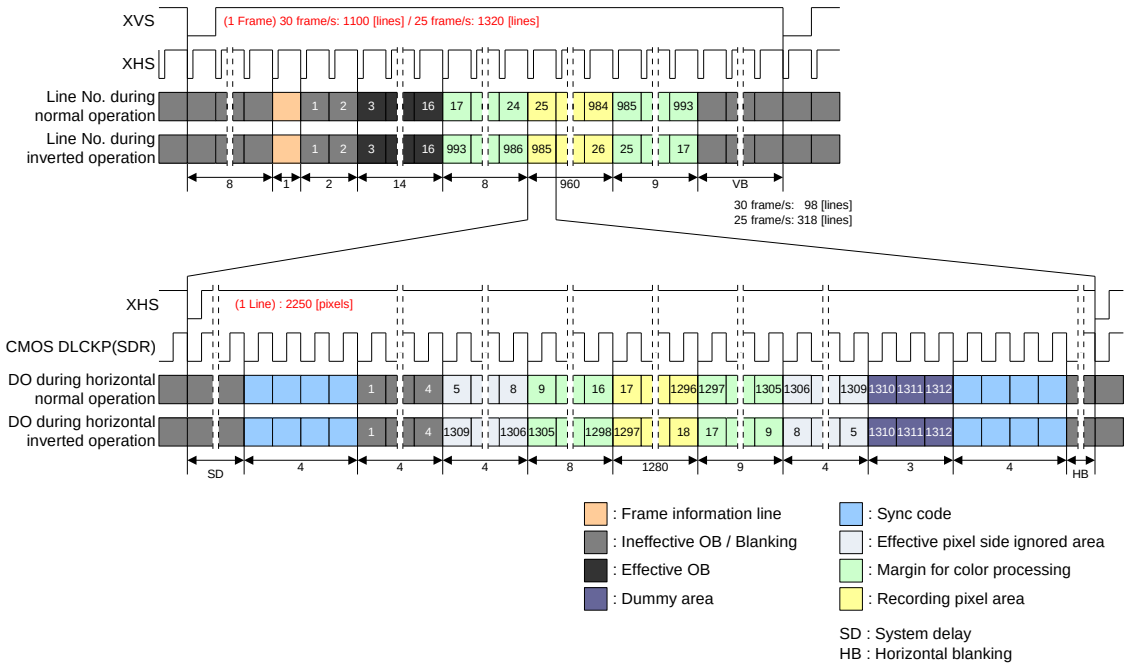
List of Setting Register for CSI-2 serial output

Address		bit	Register Name	Initial Value	CSI-2 serial						Remarks
					1 lane	2 lane		4 lane			
4-wire	I2C				30 / 25 [frame /s]	30 / 25 [frame /s]	60 / 50 [frame /s]	30 / 25 [frame /s]	60 / 50 [frame /s]	120 / 100 [frame /s]	
Chip ID: 02h											
05h	3005h	[0]	ADBIT	0h	0h / 1h						0: 10 bit, 1: 12 bit
06h	3006h	[7:0]	MODE	00h	00h						All-pixel scan
07h	3007h	[0]	VREVERSE	0h	0h / 1h						0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h						0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	0h						Quad-VGA
09h	3009h	[1:0]	FRSEL	1h	2h	2h	1h	2h	1h	0h	
		[4]	FDG_SEL	0h	0h / 1h						0: LCG mode, 1: HCG mode
18h	3018h	[7:0]	VMAX	44Ch	44Ch / 528h						44Ch: 30 / 60 / 120 [frame / s] 528h: 25 / 50 / 100 [frame / s]
19h	3019h	[3:0]									
1Bh	301Bh	[7:0]	HMAX	1194h	1194h	1194h	8CAh	1194h	8CAh	465h	H direction designated
1Ch	301Ch	[5:0]									
44h	3044h	[1:0]	ODBIT	1h	1h						In CSI-2, fixed to “1h”.
		[7:4]	OPORTSEL	0h	0h						In CSI-2, fixed to “0h”.
54h	3054h	[7:0]	—	67h	66h						CSI-2 setting
5Ch	305Ch	[7:0]	INCKSEL1	2Ch	2Ch / 20h						Set according to INCK
5Dh	305Dh	[7:0]	INCKSEL2	10h	10h / 00h						Set according to INCK
5Eh	305Eh	[7:0]	INCKSEL3	2Ch	2Ch / 20h						Set according to INCK
5Fh	305Fh	[7:0]	INCKSEL4	10h	10h / 00h						Set according to INCK
60h to FFh	3060h to 30FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.								
Chip ID = 03h											
00h to FFh	3100h to 31FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.								
Chip ID = 04h											
00h to FFh	3200h to 32FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.								

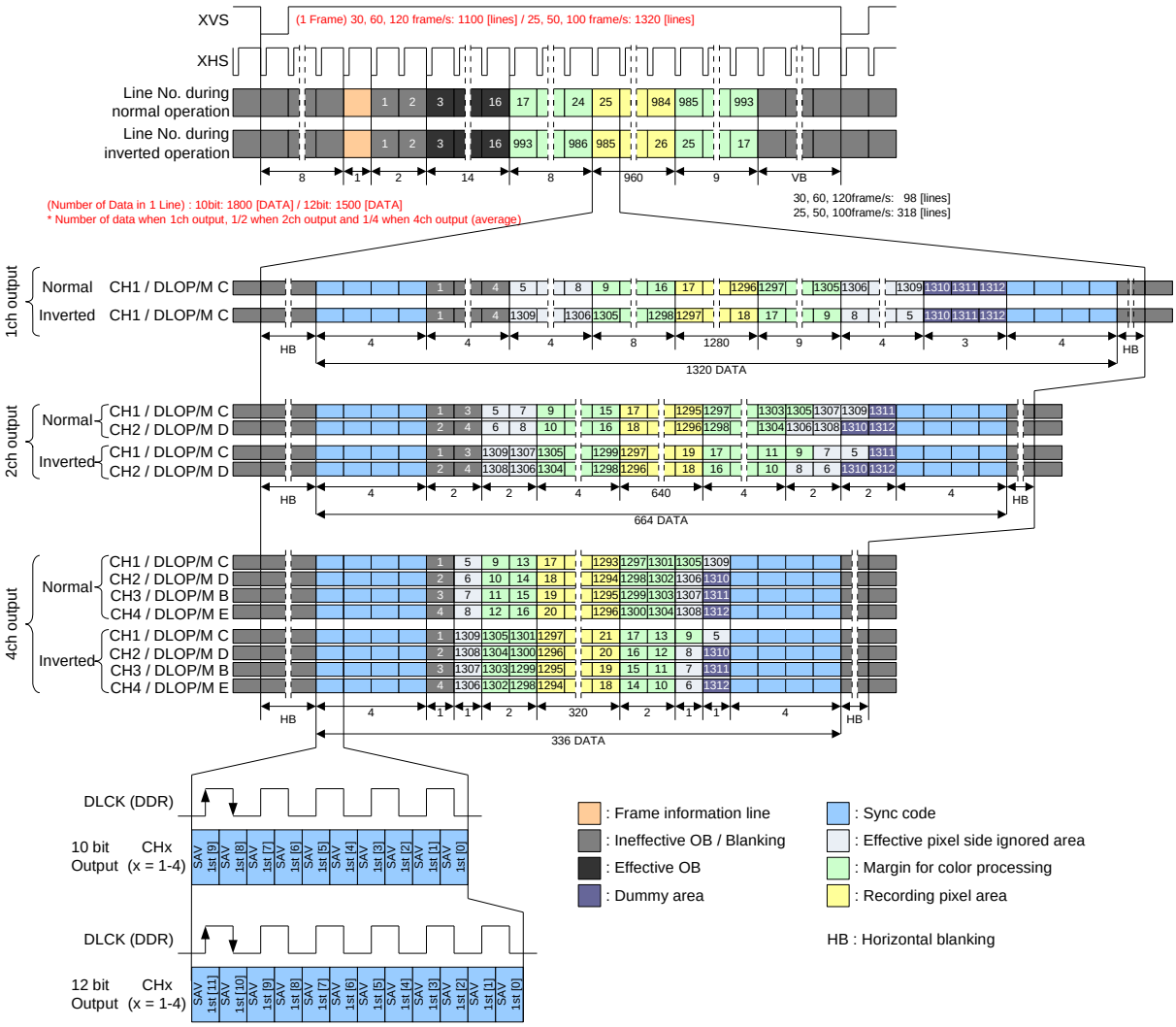
Address		bit	Register Name	Initial Value	CSI-2 serial						Remarks
					1 lane	2 lane		4 lane			
4-wire	I2C				30 / 25 [frame /s]	30 / 25 [frame /s]	60 / 50 [frame /s]	30 / 25 [frame /s]	60 / 50 [frame /s]	120 / 100 [frame /s]	
Chip ID = 05h											
				Data rate	594	297	594	148.5	297	594	[Mbps / Lane]
44h	3344h	[5:4]	REPETITION	2h	0h	1h	0h	2h	1h	0h	—
46h	3346h	[1:0]	PHYSICAL_ LANE_NUM	3h	0h	1h		3h			—
53h	3353h	[5:0]	OB_SIZE_V	Eh	Eh						—
57h	3357h	[7:0]	PIC_SIZE_V	3D1h	3D1h						—
58h	3358h	[4:0]									
6Bh	336Bh	[7:0]	THSEXIT	27h	57h	37h	57h	27h	37h	57h	Global timing
6Ch	336Ch	[7:0]	TCLKPRE	1Fh	1Fh						Global timing
7Dh	337Dh	[7:0]	CSI_DT_FMT	0C0Ch	0A0Ah / 0C0Ch						0A0Ah: RAW10 0C0Ch: RAW12
7Eh	337Eh	[7:0]									
7Fh	337Fh	[1:0]	CSI_LANE_ MODE	3h	0h	1h		3h			—
80h	3380h	[7:0]	INCK_FREQ1	3600h	27MHz: 1B00h 54MHz: 3600h 37.125MHz: 2520h 74.25MHz: 4A40h						Set according to INCK
81h	3381h	[7:0]									
82h	3382h	[7:0]	TCLKPOST	57h	6Fh	5Fh	6Fh	57h	5Fh	6Fh	Global timing
83h	3383h	[7:0]	THSPREPARE	0Fh	27h	17h	27h	0Fh	17h	27h	Global timing
84h	3384h	[7:0]	THSZERO	27h	4Fh	37h	4Fh	27h	37h	4Fh	Global timing
85h	3385h	[7:0]	THSTRAIL	0Fh	2Fh	17h	2Fh	0Fh	17h	2Fh	Global timing
86h	3386h	[7:0]	TCLKTRAIL	0Fh	2Fh	17h	2Fh	0Fh	17h	2Fh	Global timing
87h	3387h	[7:0]	TCLKPREPARE	07h	2Fh	17h	2Fh	07h	17h	2Fh	Global timing
88h	3388h	[7:0]	TCLKZERO	37h	9Fh	4Fh	9Fh	37h	4Fh	9Fh	Global timing
89h	3389h	[7:0]	TLPX	1Fh	37h	27h	37h	1Fh	27h	37h	Global timing
8Dh	338Dh	[7:0]	INCK_FREQ2	0367h	27MHz: 013Dh 54MHz: 0279h 37.125MHz: 01B4h 74.25MHz: 0367h						Set according to INCK
8Eh	338Eh	[7:0]									



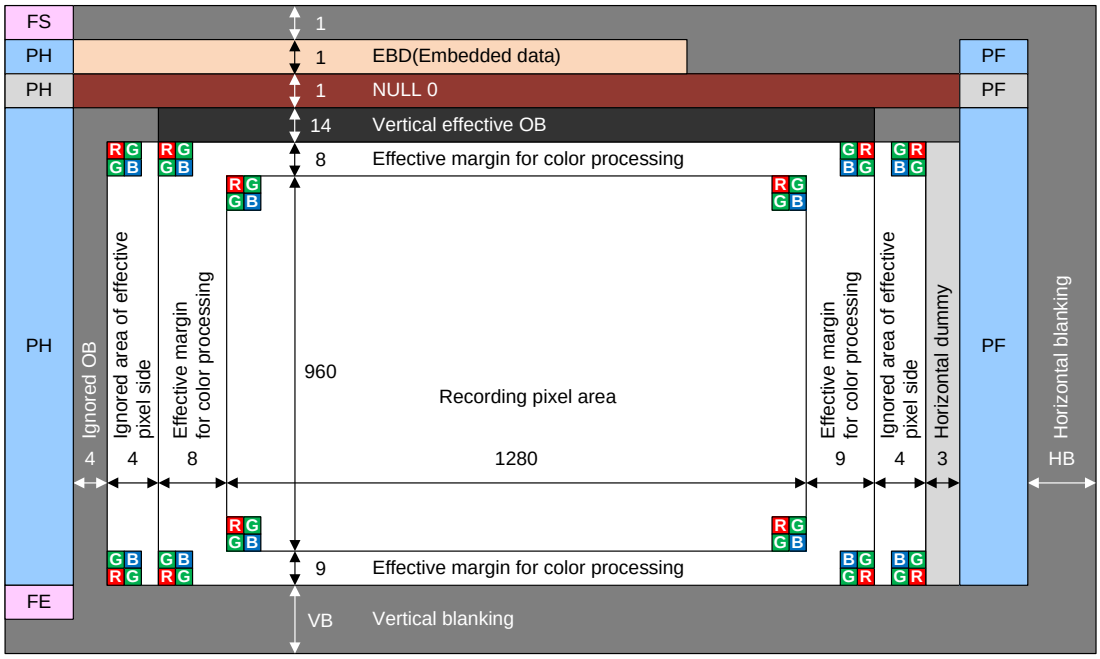
Pixel Array Image Drawing in Quad VGA mode (Parallel CMOS output / Serial LVDS output)



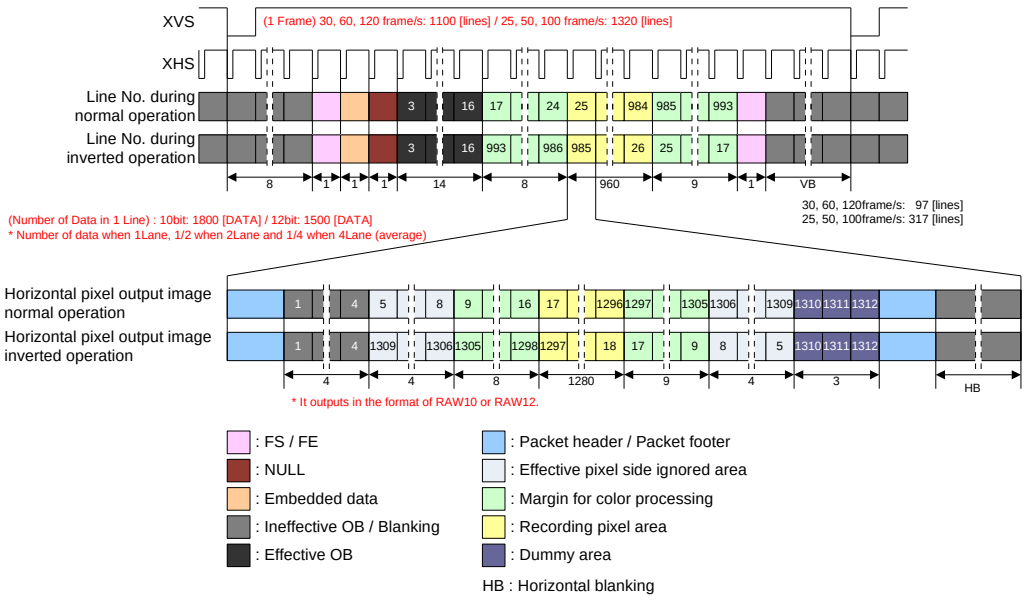
Drive Timing Chart for Quad VGA mode (Parallel CMOS output)



Drive Timing Chart for Quad VGA mode (Serial LVDS output)



Pixel Array Image Drawing in Quad VGA mode (CSI-2 serial output)

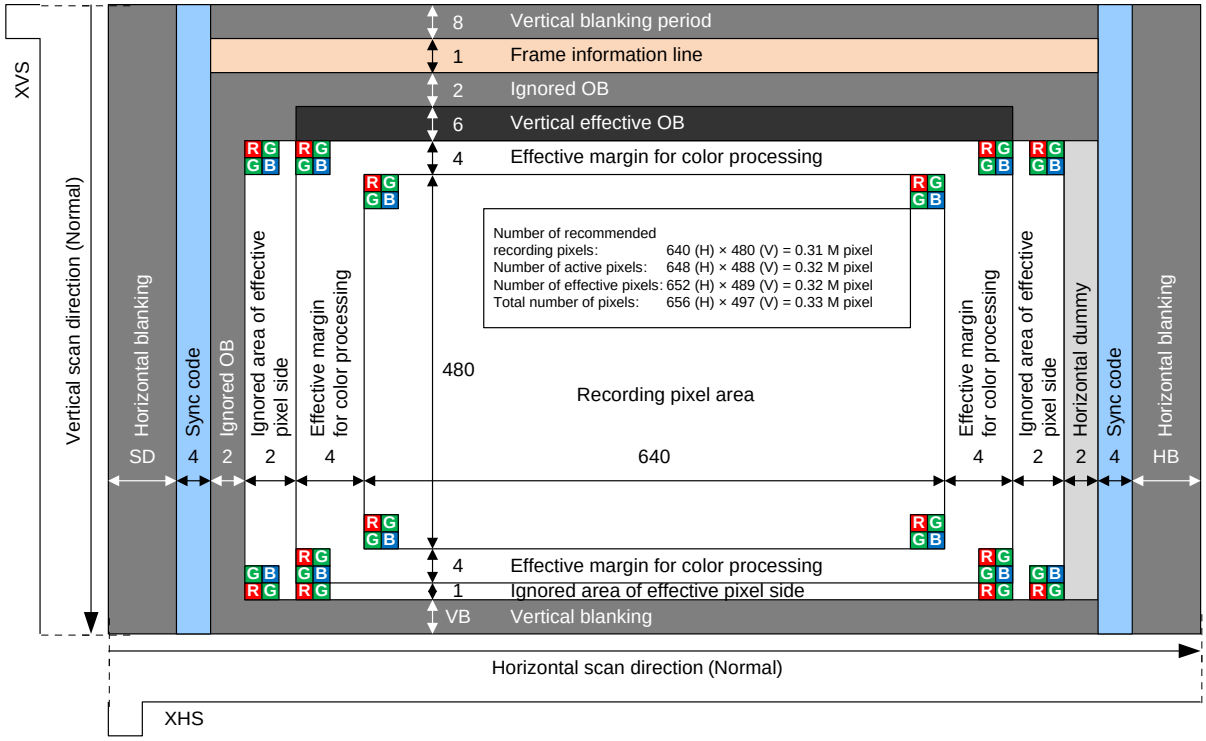


Drive Timing Chart for Quad VGA mode (CSI-2 serial output)

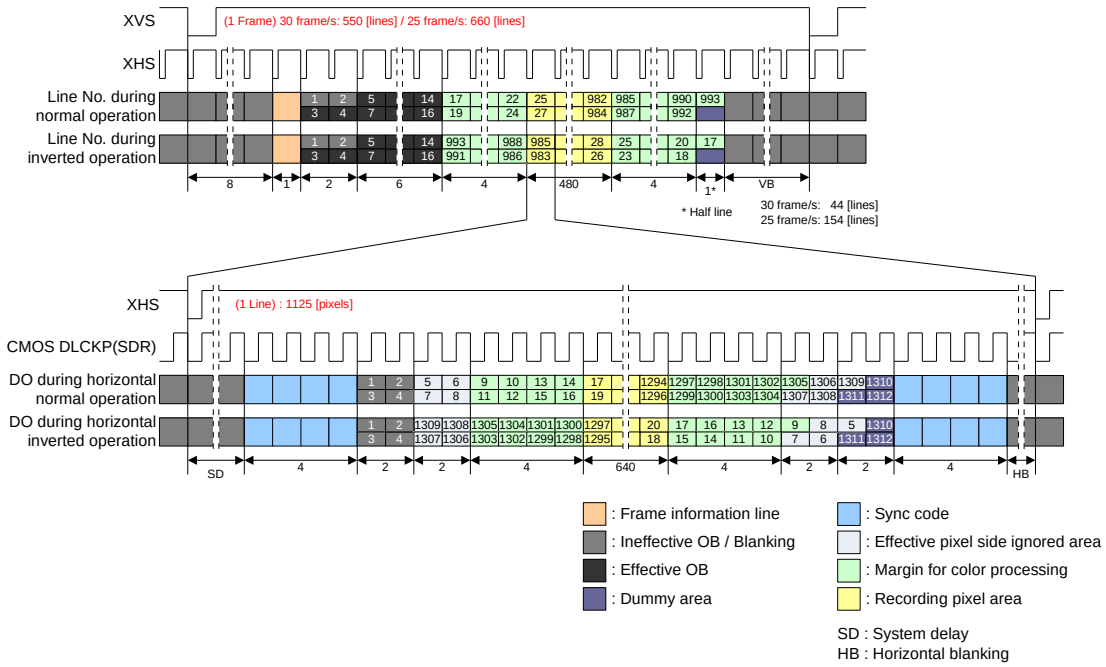
2×2 binning mode (Quad VGA)

List of Setting Register for CMOS parallel / LVDS serial output

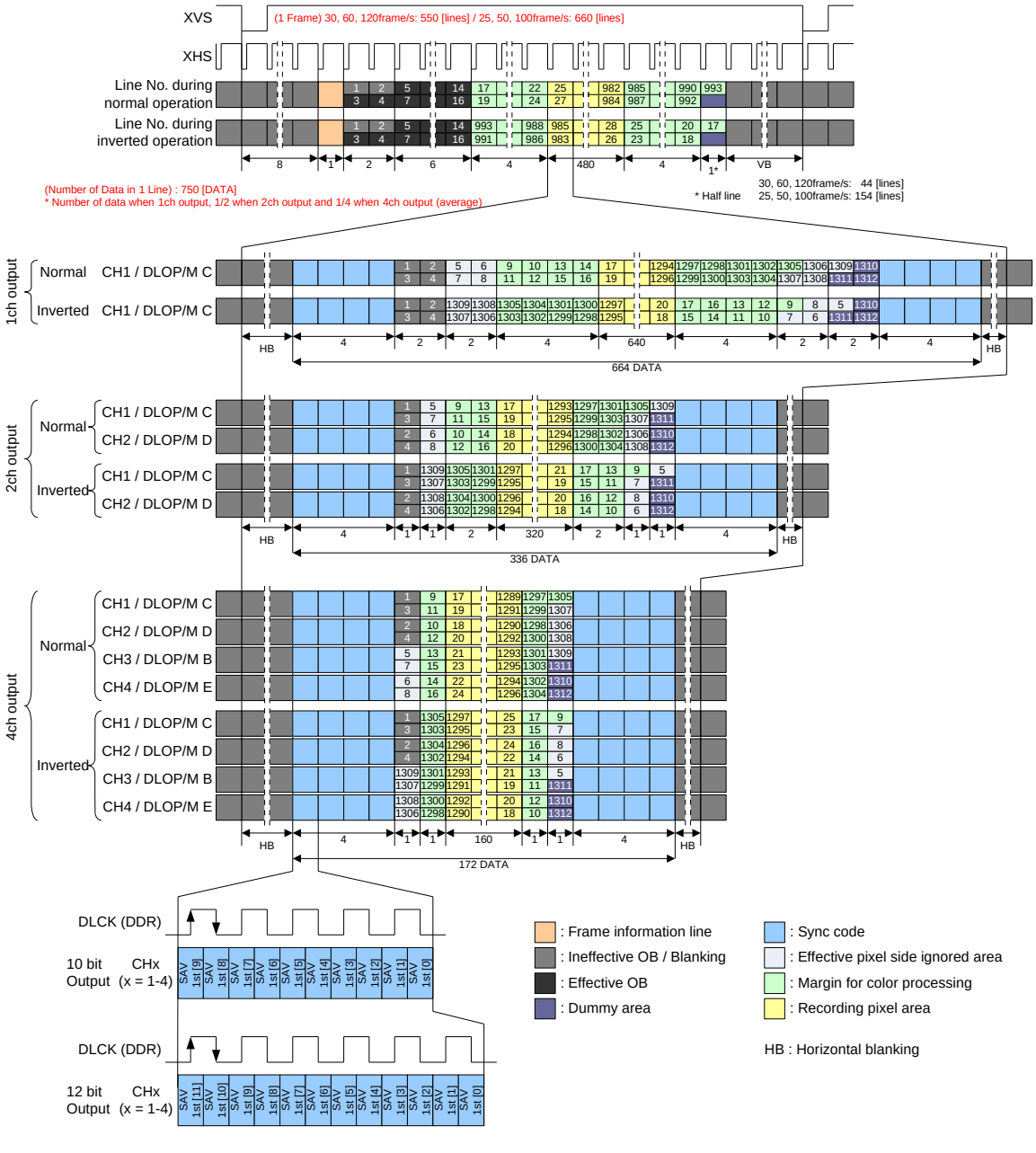
Address		bit	Register Name	Initial	CMOS	LVDS serial			Remarks
4-wire	I2C			Value	parallel	1 ch	2 ch	4 ch	
Chip ID: 02h									
05h	3005h	[0]	ADBIT	0h	0h				0: 10 bit, 1: 12 bit
06h	3006h	[7:0]	MODE	00h	22h				2×2 binning
07h	3007h	[0]	VREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	0h				Quad-VGA
09h	3009h	[1:0]	FRSEL	1h	1h	2h			30 / 25 [frame/s]
					N/A	N/A	1h		60 / 50 [frame/s]
					N/A	N/A	N/A	0h	120 / 100 [frame/s]
		[4]	FDG_SEL	0h	0h / 1h				0: LCG mode, 1: HCG mode
18h	3018h	[7:0]	VMAX	44Ch	226h / 294h				226h: 30 / 60 / 120 [frame / s]
19h	3019h	[3:0]							294h: 25 / 50 / 100 [frame / s]
1Bh	301Bh	[7:0]	HMAX	1194h	2328h				30 / 25 [frame/s]
					N/A	N/A	1194h		60 / 50 [frame/s]
1Ch	301Ch	[5:0]			N/A	N/A	N/A	8CAh	120 / 100 [frame/s]
44h	3044h	[1:0]	ODBIT	1h	1h				0: 10 bit, 1: 12 bit
		[7:4]	OPORTSEL	0h	0h	Ch	Dh	Eh	I/F selection
54h	3054h	[7:0]	—	67h	67h				CMOS / LVDS setting
5Ch	305Ch	[7:0]	INCKSEL1	2Ch	2Ch / 20h				Set according to INCK
5Dh	305Dh	[7:0]	INCKSEL2	10h	10h / 00h				Set according to INCK
5Eh	305Eh	[7:0]	INCKSEL3	2Ch	2Ch / 20h				Set according to INCK
5Fh	305Fh	[7:0]	INCKSEL4	10h	10h / 00h				Set according to INCK
60h to FFh	3060h to 30FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
Chip ID = 03h									
00h to FFh	3100h to 31FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
Chip ID = 04h									
00h to FFh	3200h to 32FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
ChipID = 05h									
00h to FFh	3300h to 33FFh	[7:0] to [7:0]	Changing the value is not necessary.						



Pixel Array Image Drawing in 2×2 binning mode (Parallel CMOS output / Serial LVDS output)



Drive Timing Chart for 2×2 binning mode (Parallel CMOS output)

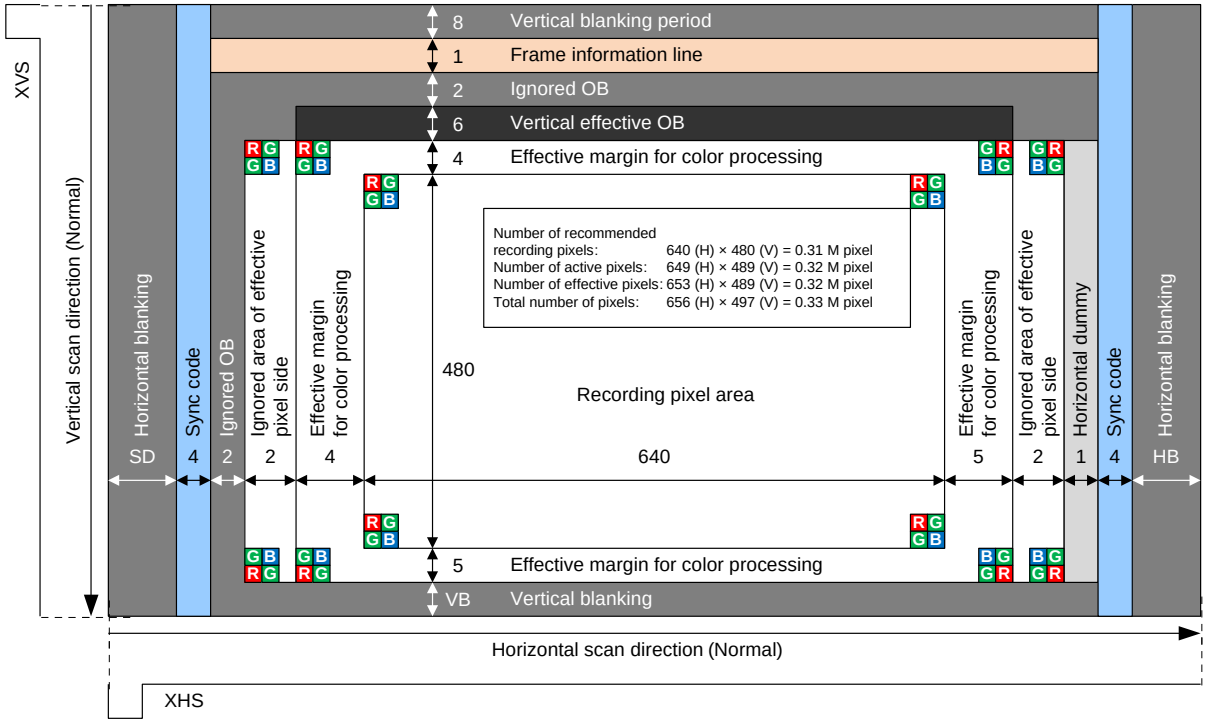


Drive Timing Chart for 2×2 binning mode (Serial LVDS output)

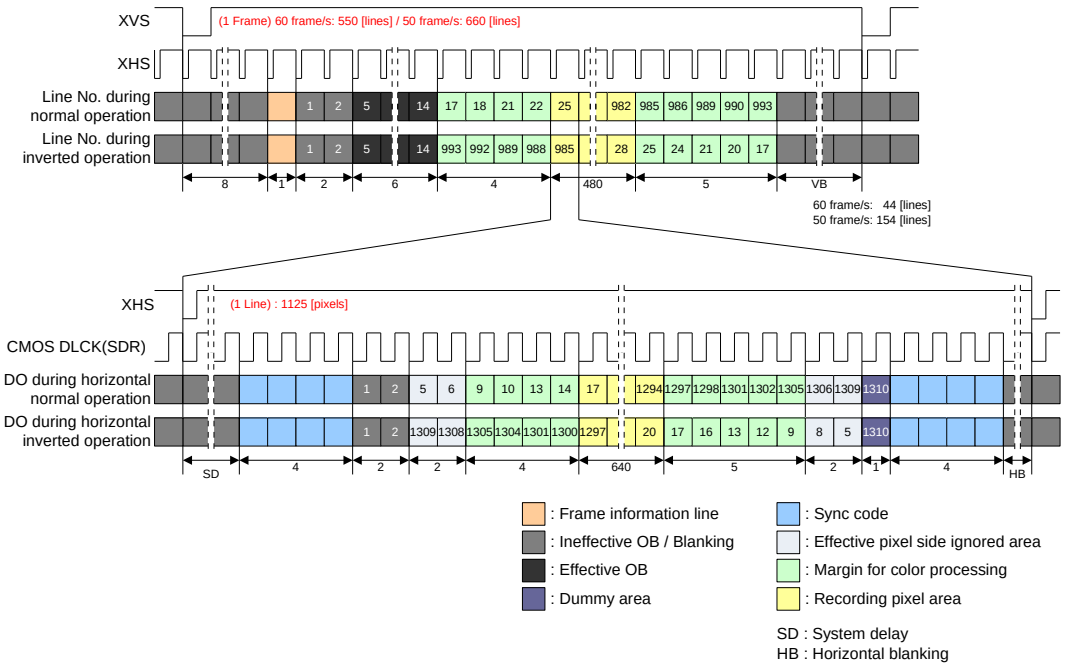
Horizontal / Vertical 1/2 subsampling mode (Quad VGA)

List of Setting Register for CMOS parallel / LVDS serial output

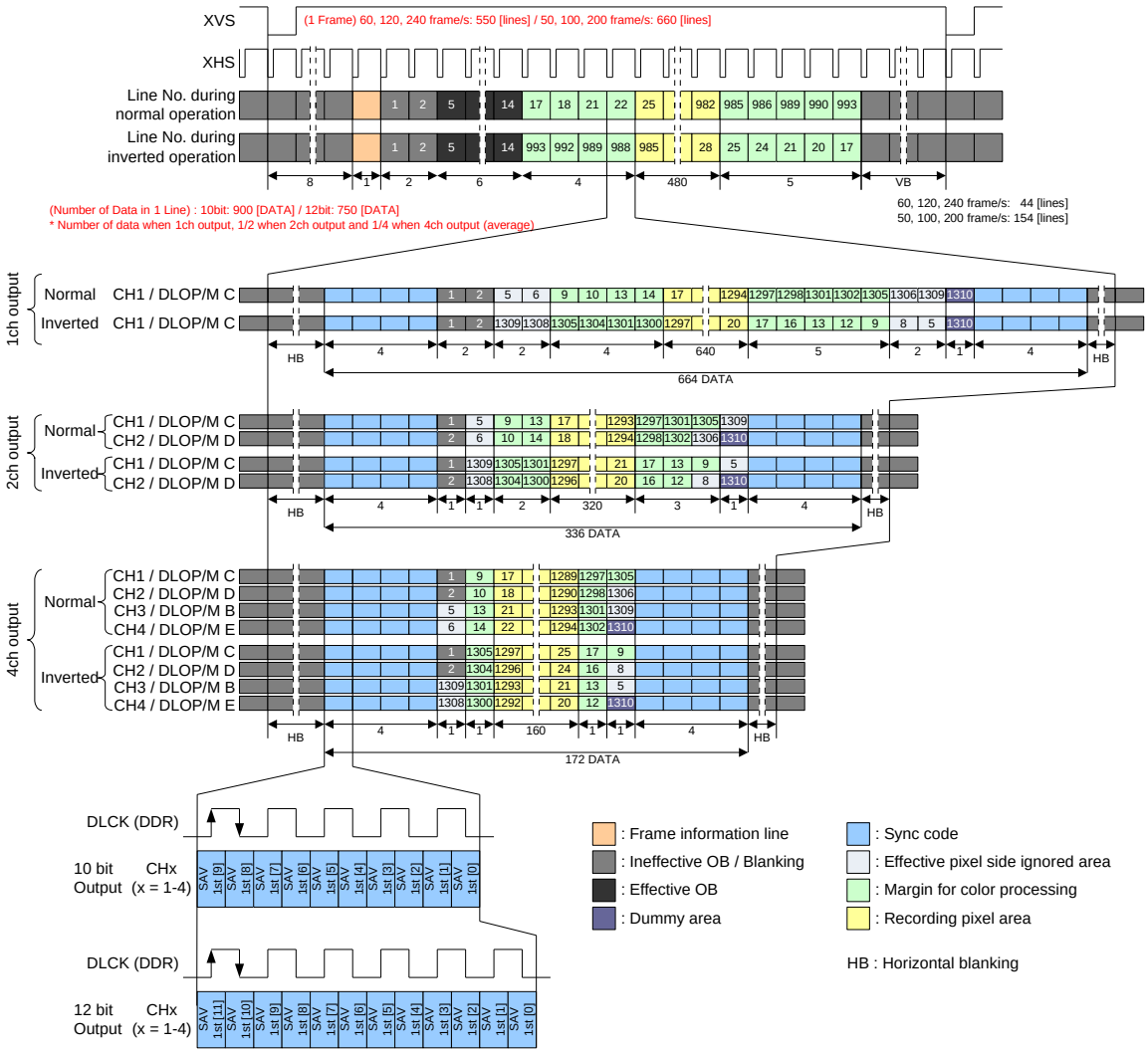
Address		bit	Register Name	Initial	CMOS	LVDS serial			Remarks
4-wire	I2C			Value	parallel	1 ch	2 ch	4 ch	
Chip ID: 02h									
05h	3005h	[0]	ADBIT	0h	0h / 1h				0: 10 bit, 1: 12 bit
06h	3006h	[7:0]	MODE	00h	33h				Horizontal / Vertical 1/2 subsampling
07h	3007h	[0]	VREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	0h				Quad-VGA
09h	3009h	[1:0]	FRSEL	1h	1h	2h			60 / 50 [frame/s]
					N/A	N/A	1h		120 / 100 [frame/s]
					N/A	N/A	N/A	0h	240 / 200 [frame/s]
		[4]	FDG_SEL	0h	0h / 1h				0: LCG mode, 1: HCG mode
18h	3018h	[7:0]	VMAX	44Ch	226h / 294h				226h: 60 / 120 / 240 [frame / s]
19h	3019h	[3:0]							294h: 50 / 100 / 200 [frame / s]
1Bh	301Bh	[7:0]	HMAX	1194h	1194h				60 / 50 [frame/s]
1Ch	301Ch	[5:0]			N/A	N/A	8CAh		120 / 100 [frame/s]
					N/A	N/A	N/A	465h	240 / 200 [frame/s]
44h	3044h	[1:0]	ODBIT	1h	0h / 1h				0: 10 bit, 1: 12 bit
		[7:4]	OPORTSEL	0h	0h	Ch	Dh	Eh	I/F selection
54h	3054h	[7:0]	—	67h	67h				CMOS / LVDS setting
5Ch	305Ch	[7:0]	INCKSEL1	2Ch	2Ch / 20h				Set according to INCK
5Dh	305Dh	[7:0]	INCKSEL2	10h	10h / 00h				Set according to INCK
5Eh	305Eh	[7:0]	INCKSEL3	2Ch	2Ch / 20h				Set according to INCK
5Fh	305Fh	[7:0]	INCKSEL4	10h	10h / 00h				Set according to INCK
60h to FFh	3060h to 30FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
Chip ID = 03h									
00h to FFh	3100h to 31FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
Chip ID = 04h									
00h to FFh	3200h to 32FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
ChipID = 05h									
00h to FFh	3300h to 33FFh	[7:0] to [7:0]	Changing the value is not necessary.						



Pixel Array Image Drawing in 1/2 subsampling mode (Parallel CMOS output / Serial LVDS output)



Drive Timing Chart for 1/2 subsampling mode (Parallel CMOS output)



Drive Timing Chart for 1/2 subsampling mode (Serial LVDS output)

Window Cropping Mode

Sensor signals are cut out and read out in arbitrary positions.
Cropping position is set, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from all-pixel scan mode and vertical, horizontal period and frame rate are fixed to the value for this mode. Pixels cropped by horizontal cropping setting are output with left justified and that extends the horizontal blanking period.
Window cropping image is shown in the figure below.
Cropping position is set, regarding effective pixel start position as origin (0, 0) in all pixel scan mode.
Only vertical width can be set for OB (horizontal width is the same as the Window cropping width).

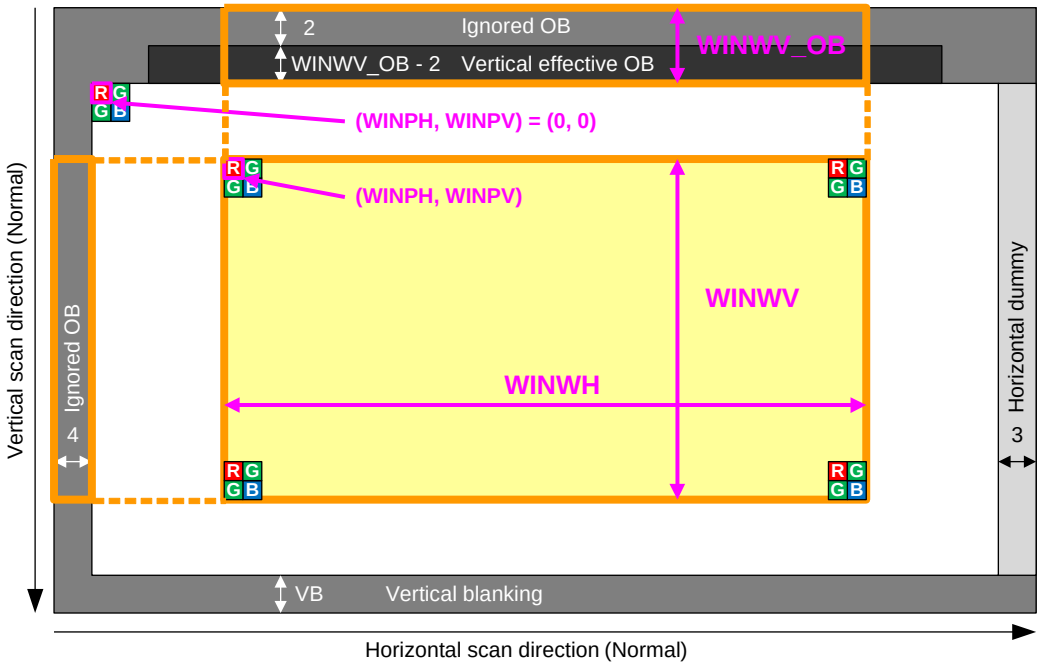


Image Drawing of Window Cropping Mode

Restrictions on Window cropping mode
The register settings should satisfy following conditions:

WINPH + WINWH ≤ 1304
368 ≤ WINWH
Set WINPH and WINWH to a multiple of 4.

V_{TTL} (Number of lines per frame or VMAX) ≥ WINWV_OB + WINWV + 9

However,
6 ≤ WINWV_OB ≤ 16
WINPV + WINWV ≤ 976
304 ≤ WINWV
OB_SIZE_V = WINWV_OB - 2 (In CSI-2 output)
PIC_SIZE_V = WINWV (In CSI-2 output)

Frame rate on Window cropping mode
Frame rate [frame/s] = 1 / (V_{TTL} × (1H period))

1H period (unit: [μs]) : Fix 1H time in a mode before cropping and calculate it by the value of "Number of INCK in 1H" in the table of "Operating Mode" and "List of Operation Modes and Output Rates".

List of Setting Register for CMOS parallel / LVDS serial output

Address		bit	Register Name	Initial Value	CMOS parallel	LVDS serial			Remarks
4-wire	I2C					1 ch	2 ch	4 ch	
Chip ID: 02h									
05h	3005h	[0]	ADBIT	0h	0h / 1h				0: 10 bit, 1: 12 bit
06h	3006h	[7:0]	MODE	00h	00h				All-pixel scan
07h	3007h	[0]	VREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	4h				Window cropping
09h	3009h	[1:0]	FRSEL	1h	1h	2h			—
					N/A	N/A	1h		—
					N/A	N/A	N/A	0h	—
		[4]	FDG_SEL	0h	0h / 1h				0: LCG mode, 1: HCG mode
18h	3018h	[7:0]	VMAX	44Ch	V_{TTL}				See previous page.
19h	3019h	[3:0]							
1Bh	301Bh	[7:0]	HMAX	1194h	1194h				*1 : 10bit / 12bit avairable
1Ch	301Ch	[5:0]			N/A	N/A	08CAh		*2: 10bit / 12bit avairable
					N/A	N/A	N/A	465h	*3: 10bit only
44h	3044h	[1:0]	ODBIT	1h	0h / 1h				0: 10 bit, 1: 12 bit
		[7:4]	OPORTSEL	0h	0h	Ch	Dh	Eh	I/F selection
54h	3054h	[7:0]	—	67h	67h				CMOS / LVDS setting
5Ch	305Ch	[7:0]	INCKSEL1	2Ch	2Ch / 20h				Set according to INCK
5Dh	305Dh	[7:0]	INCKSEL2	10h	10h / 00h				Set according to INCK
5Eh	305Eh	[7:0]	INCKSEL3	2Ch	2Ch / 20h				Set according to INCK
5Fh	305Fh	[7:0]	INCKSEL4	10h	10h / 00h				Set according to INCK
60h to FFh	3060h to 30FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
Chip ID = 03h									
00h to FFh	3100h to 31FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
Chip ID = 04h									
00h to FFh	3200h to 32FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
ChipID = 05h									
00h to FFh	3300h to 33FFh	[7:0] to [7:0]	Changing the value is not necessary.						

List of Setting Register for CSI-2 serial output

Address		bit	Register Name	Initial Value	CSI-2 serial						Remarks
					1 lane	2 lane		4 lane			
4-wire	I2C				*1 [frame /s]	*1 [frame /s]	*2 [frame /s]	*1 [frame /s]	*2 [frame /s]	*3 [frame /s]	
Chip ID: 02h											
05h	3005h	[0]	ADBIT	0h	0h / 1h						0: 10 bit, 1: 12 bit
06h	3006h	[7:0]	MODE	00h	00h						All-pixel scan
07h	3007h	[0]	VREVERSE	0h	0h / 1h						0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h						0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	4h						Window cropping
09h	3009h	[1:0]	FRSEL	1h	2h	2h	1h	2h	1h	0h	—
		[4]	FDG_SEL	0h	0h / 1h						0: LCG mode, 1: HCG mode
18h	3018h	[7:0]	VMAX	44Ch	V_{TTL}						See previous page
19h	3019h	[3:0]									
1Bh	301Bh	[7:0]	HMAX	1194h	1194h	1194h	8CAh	1194h	8CAh	465h	H direction designated
1Ch	301Ch	[5:0]									
44h	3044h	[1:0]	ODBIT	1h	1h						In CSI-2, fixed to “1h”.
		[7:4]	OPORTSEL	0h	0h						In CSI-2, fixed to “0h”.
54h	3054h	[7:0]	—	67h	66h						CSI-2 setting
5Ch	305Ch	[7:0]	INCKSEL1	2Ch	2Ch / 20h						Set according to INCK
5Dh	305Dh	[7:0]	INCKSEL2	10h	10h / 00h						Set according to INCK
5Eh	305Eh	[7:0]	INCKSEL3	2Ch	2Ch / 20h						Set according to INCK
5Fh	305Fh	[7:0]	INCKSEL4	10h	10h / 00h						Set according to INCK
60h to FFh	3060h to 30FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.								
Chip ID = 03h											
00h to FFh	3100h to 31FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.								
Chip ID = 04h											
00h to FFh	3200h to 32FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.								

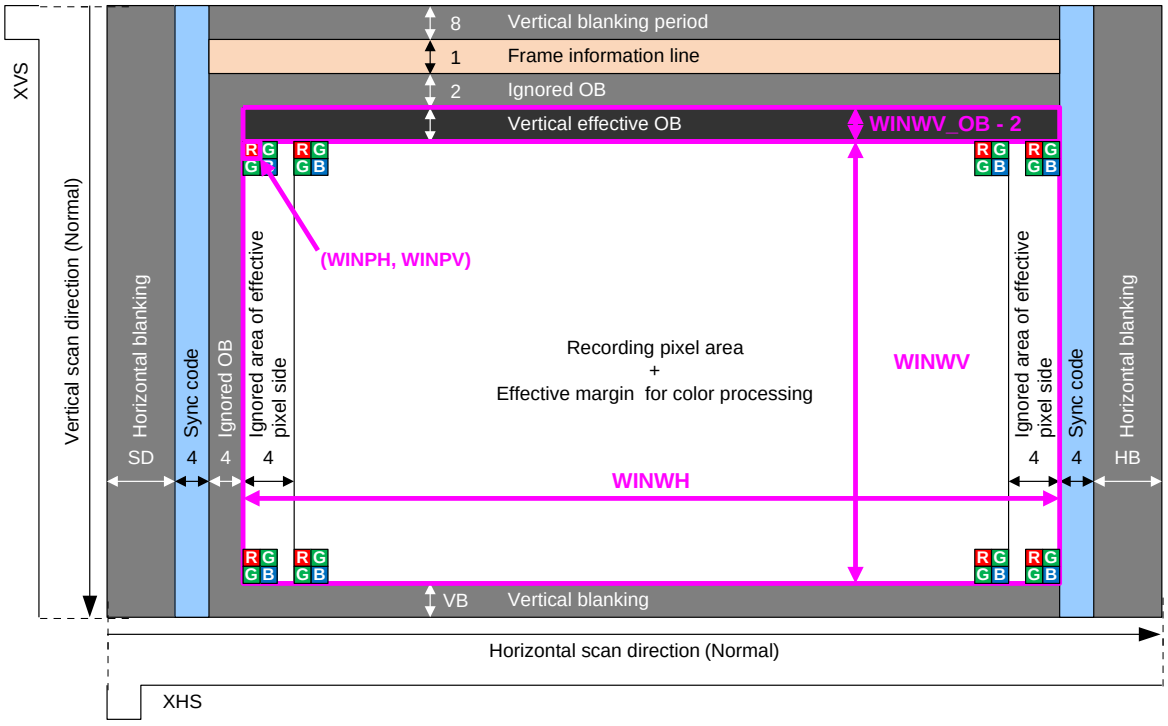
Address		bit	Register Name	Initial Value	CSI-2 serial						Remarks
					1 lane	2 lane		4 lane			
4-wire	I2C				*1 [frame /s]	*1 [frame /s]	*2 [frame /s]	*1 [frame /s]	*2 [frame /s]	*3 [frame /s]	
Chip ID = 05h											
			Data rate		594	297	594	148.5	297	594	[Mbps / Lane]
44h	3344h	[5:4]	REPETITION	2h	0h	1h	0h	2h	1h	0h	—
46h	3346h	[1:0]	PHYSICAL_ LANE_NUM	3h	0h	1h		3h			—
53h	3353h	[5:0]	OB_SIZE_V	Eh	Eh						—
57h	3357h	[7:0]	PIC_SIZE_V	3D1h	3D1h						—
58h	3358h	[4:0]									
6Bh	336Bh	[7:0]	THSEXIT	27h	57h	37h	57h	27h	37h	57h	Global timing
6Ch	336Ch	[7:0]	TCLKPRE	1Fh	1Fh						Global timing
7Dh	337Dh	[7:0]	CSI_DT_FMT	0C0Ch	0A0Ah / 0C0Ch						0A0Ah: RAW10 0C0Ch: RAW12
7Eh	337Eh	[7:0]									
7Fh	337Fh	[1:0]	CSI_LANE_ MODE	3h	0h	1h		3h			—
80h	3380h	[7:0]	INCK_FREQ1	3600h	27MHz: 1B00h 54MHz: 3600h 37.125MHz: 2520h 74.25MHz: 4A40h						Set according to INCK
81h	3381h	[7:0]									
82h	3382h	[7:0]	TCLKPOST	57h	6Fh	5Fh	6Fh	57h	5Fh	6Fh	Global timing
83h	3383h	[7:0]	THSPREPARE	0Fh	27h	17h	27h	0Fh	17h	27h	Global timing
84h	3384h	[7:0]	THSZERO	27h	4Fh	37h	4Fh	27h	37h	4Fh	Global timing
85h	3385h	[7:0]	THSTRAIL	0Fh	2Fh	17h	2Fh	0Fh	17h	2Fh	Global timing
86h	3386h	[7:0]	TCLKTRAIL	0Fh	2Fh	17h	2Fh	0Fh	17h	2Fh	Global timing
87h	3387h	[7:0]	TCLKPREPARE	07h	2Fh	17h	2Fh	07h	17h	2Fh	Global timing
88h	3388h	[7:0]	TCLKZERO	37h	9Fh	4Fh	9Fh	37h	4Fh	9Fh	Global timing
89h	3389h	[7:0]	TLPX	1Fh	37h	27h	37h	1Fh	27h	37h	Global timing
8Dh	338Dh	[7:0]	INCK_FREQ2	0367h	27MHz: 013Dh 54MHz: 0279h 37.125MHz: 01B4h 74.25MHz: 0367h						Set according to INCK
8Eh	338Eh	[7:0]									

The example of window cropping setting is shown below.
The frame rate is maximum setting as each image format. For adjust the frame rate, please extend the VMAX or the number of lines per frame.

Example of Window cropping Mode Setting

Image size	INCK [MHz]	Output Resolution [bit]	Frame rate [frame/s]	Number of recording pixels		Register setting [DEC] (HEX)						
				Horizontal	Vertical	FRSEL	HMAX	VMAX	WINPH	WINPV	WINWH	WINWV
VGA	27 54 37.125 74.25	10/12	63.2	640	480	2	4500d (1194h)	522d (20Ah)	320d (140h)	240d (F0h)	656d (290h)	496d (1F0h)
		10/12	126.4			1	2250d (8CAh)					
		10	252.9			0	1125d (465h)					
CIF	27 54 37.125 74.25	10/12	100.0	352	288	2	4500d (1194h)	330d (14Ah)	464d (1D0h)	336d (150h)	368d (170h)	304d (130h)
		10/12	200.0			1	2250d (8CAh)					
		10	400.0			0	1125d (465h)					

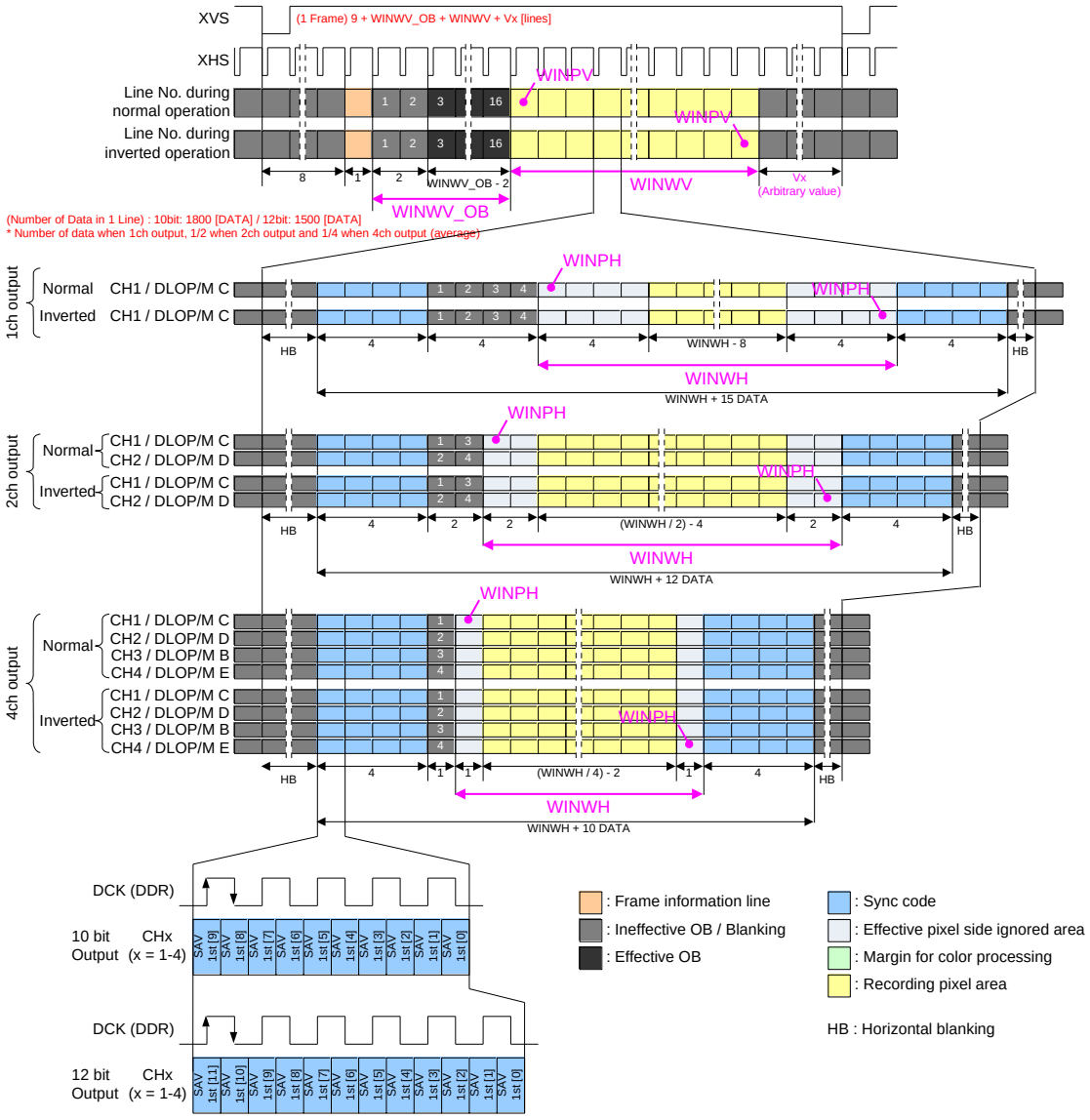
* These settings are when the ignored OB line is 2 lines and effective OB line is 14 lines.
* When the CSI-2 output, set the value that is set to register WINWV_OB to register PIC_SIZE_V.



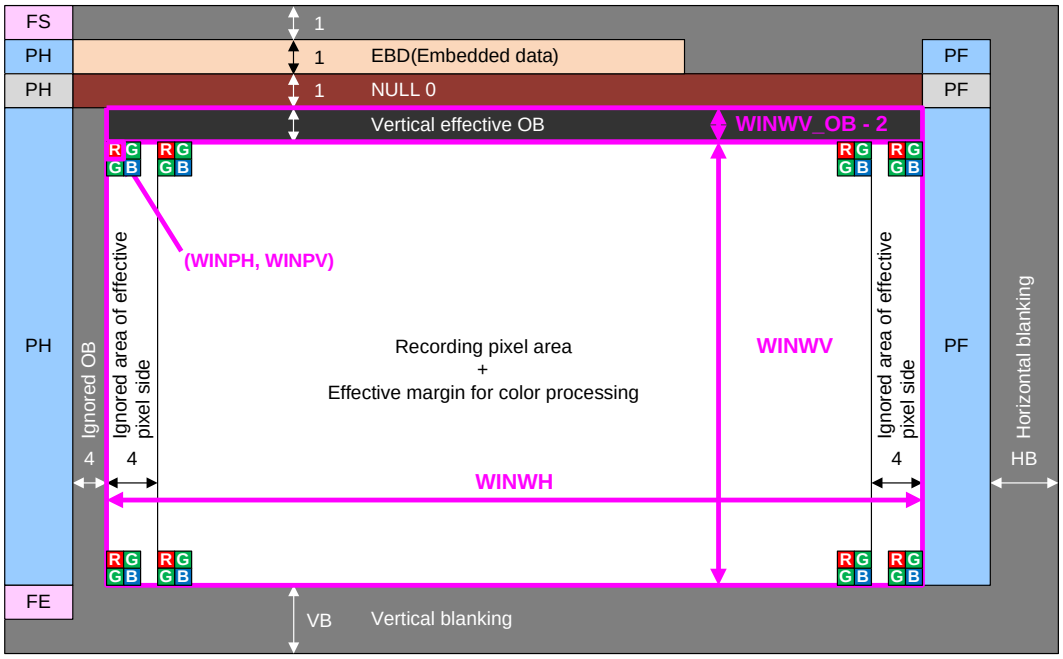
Pixel Array Image Drawing in Window Cropping mode (Parallel CMOS output / Serial LVDS output)



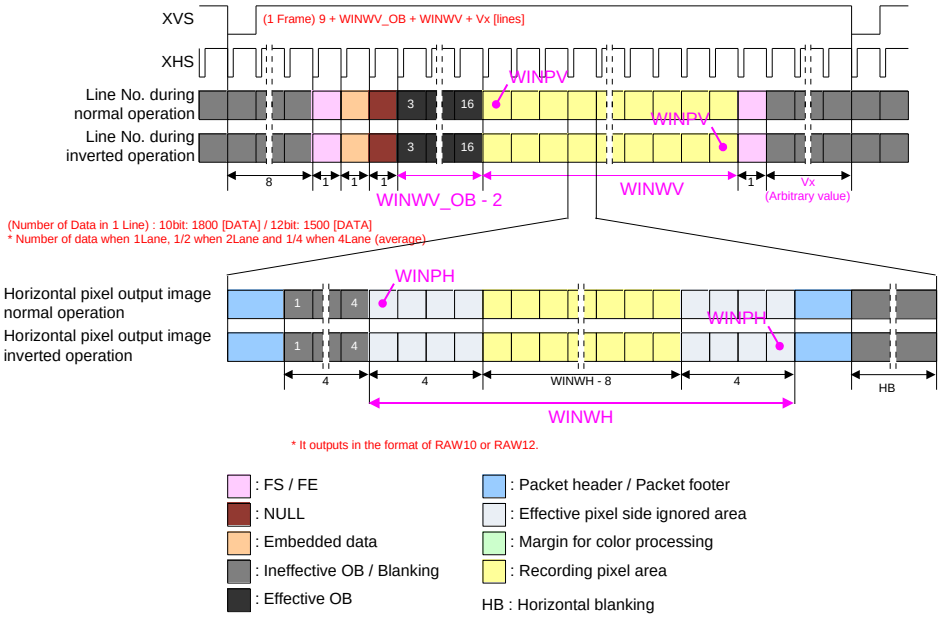
Drive Timing Chart for Window Cropping mode (Parallel CMOS output)



Drive Timing Chart for Window Cropping mode (Serial LVDS output)



Pixel Array Image Drawing in Window Cropping mode (CSI-2 serial output)



Drive Timing Chart for Window Cropping mode (CSI-2 serial output)

HD720p mode

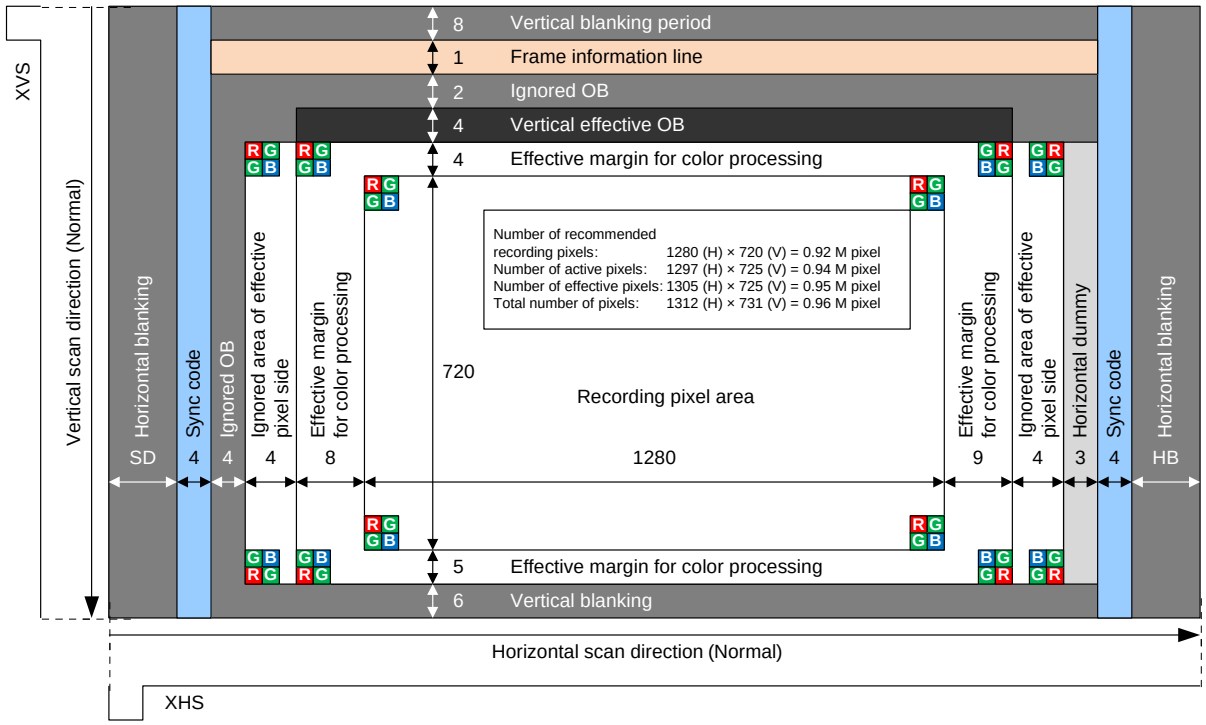
List of Setting Register for CMOS parallel / LVDS serial output

Address		bit	Register Name	Initial	CMOS	LVDS serial			Remarks
4-wire	I2C			Value	parallel	1 ch	2 ch	4 ch	
Chip ID: 02h									
05h	3005h	[0]	ADBIT	0h	0h / 1h				0: 10 bit, 1: 12 bit
06h	3006h	[7:0]	MODE	00h	00h				All-pixel scan
07h	3007h	[0]	VREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	1h				HD720p
09h	3009h	[1:0]	FRSEL	1h	2h	2h			30 [frame/s]
					1h	N/A	1h		60 [frame/s]
					N/A	N/A	N/A	0h	120 [frame/s]
		[4]	FDG_SEL	0h	0h / 1h				0: LCG mode, 1: HCG mode
18h	3018h	[7:0]	VMAX	44Ch	2EEh				30 / 60 / 120 [frame / s]
19h	3019h	[3:0]							
1Bh	301Bh	[7:0]	HMAX	1194h	19C8h				30 [frame/s]
1Ch	301Ch	[5:0]			CE4h	N/A	CE4h		60 [frame/s]
					N/A	N/A	N/A	672h	120 [frame/s]
44h	3044h	[1:0]	ODBIT	1h	0h / 1h				0: 10 bit, 1: 12 bit
		[7:4]	OPORTSEL	0h	0h	Ch	Dh	Eh	I/F selection
54h	3054h	[7:0]	—	67h	67h				CMOS / LVDS setting
5Ch	305Ch	[7:0]	INCKSEL1	2Ch	20h				Set according to INCK
5Dh	305Dh	[7:0]	INCKSEL2	10h	10h / 00h				Set according to INCK
5Eh	305Eh	[7:0]	INCKSEL3	2Ch	20h				Set according to INCK
5Fh	305Fh	[7:0]	INCKSEL4	10h	10h / 00h				Set according to INCK
60h to FFh	3060h to 30FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
Chip ID = 03h									
00h to FFh	3100h to 31FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
Chip ID = 04h									
00h to FFh	3200h to 32FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.						
ChipID = 05h									
00h to FFh	3300h to 33FFh	[7:0] to [7:0]	Changing the value is not necessary.						

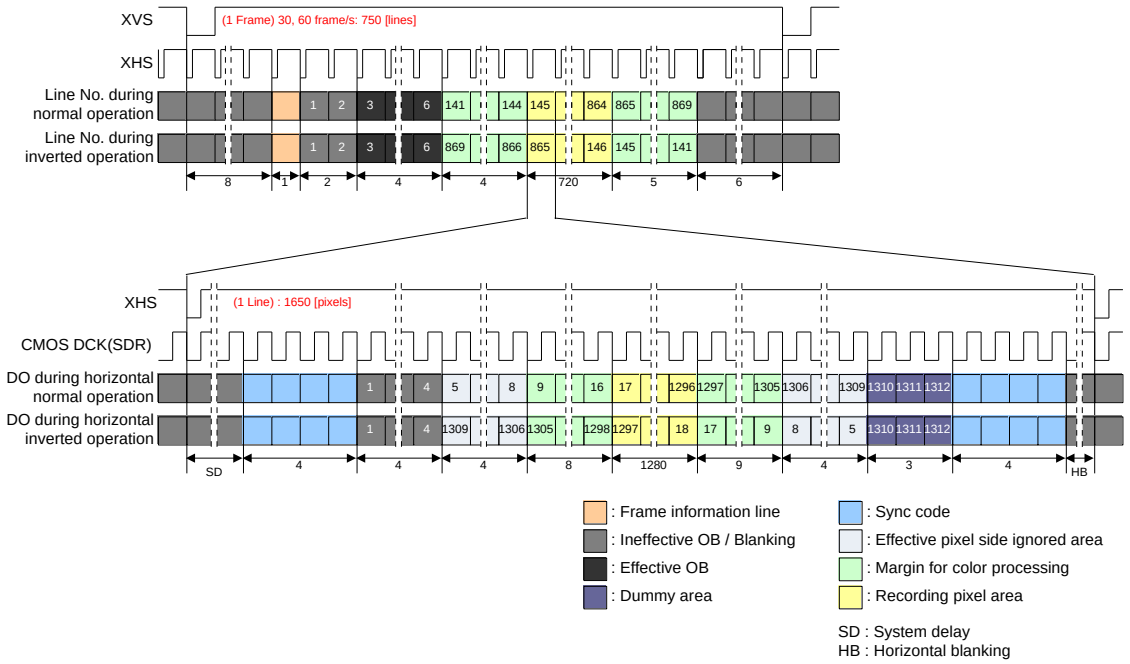
List of Setting Register for CSI-2 serial output

Address		bit	Register Name	Initial Value	CSI-2 serial						Remarks
					1 lane	2 lane		4 lane			
4-wire	I2C				30 [frame /s]	30 [frame /s]	60 [frame /s]	30 [frame /s]	60 [frame /s]	120 [frame /s]	
Chip ID: 02h											
05h	3005h	[0]	ADBIT	0h	0h / 1h						0: 10 bit, 1: 12 bit
06h	3006h	[7:0]	MODE	00h	00h						All-pixel scan
07h	3007h	[0]	VREVERSE	0h	0h / 1h						0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h						0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	1h						HD720p
09h	3009h	[1:0]	FRSEL	1h	2h	2h	1h	2h	1h	0h	—
		[4]	FDG_SEL	0h	0h / 1h						0: LCG mode, 1: HCG mode
18h	3018h	[7:0]	VMAX	44Ch	2EEh						30 / 60 / 120 [frame / s]
19h	3019h	[3:0]									
1Bh	301Bh	[7:0]	HMAX	1194h	19C8h	19C8h	CE4h	19C8h	CE4h	672h	H direction designated
1Ch	301Ch	[5:0]									
44h	3044h	[1:0]	ODBIT	1h	1h						In CSI-2, fixed to “1h”.
		[7:4]	OPORTSEL	0h	0h						In CSI-2, fixed to “0h”.
54h	3054h	[7:0]	—	67h	66h						CSI-2 setting
5Ch	305Ch	[7:0]	INCKSEL1	2Ch	20h						Set according to INCK
5Dh	305Dh	[7:0]	INCKSEL2	10h	10h / 00h						Set according to INCK
5Eh	305Eh	[7:0]	INCKSEL3	2Ch	20h						Set according to INCK
5Fh	305Fh	[7:0]	INCKSEL4	10h	10h / 00h						Set according to INCK
60h to FFh	3060h to 30FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.								
Chip ID = 03h											
00h to FFh	3100h to 31FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.								
Chip ID = 04h											
00h to FFh	3200h to 32FFh	[7:0] to [7:0]	Set register value that described on item “Register map”.								

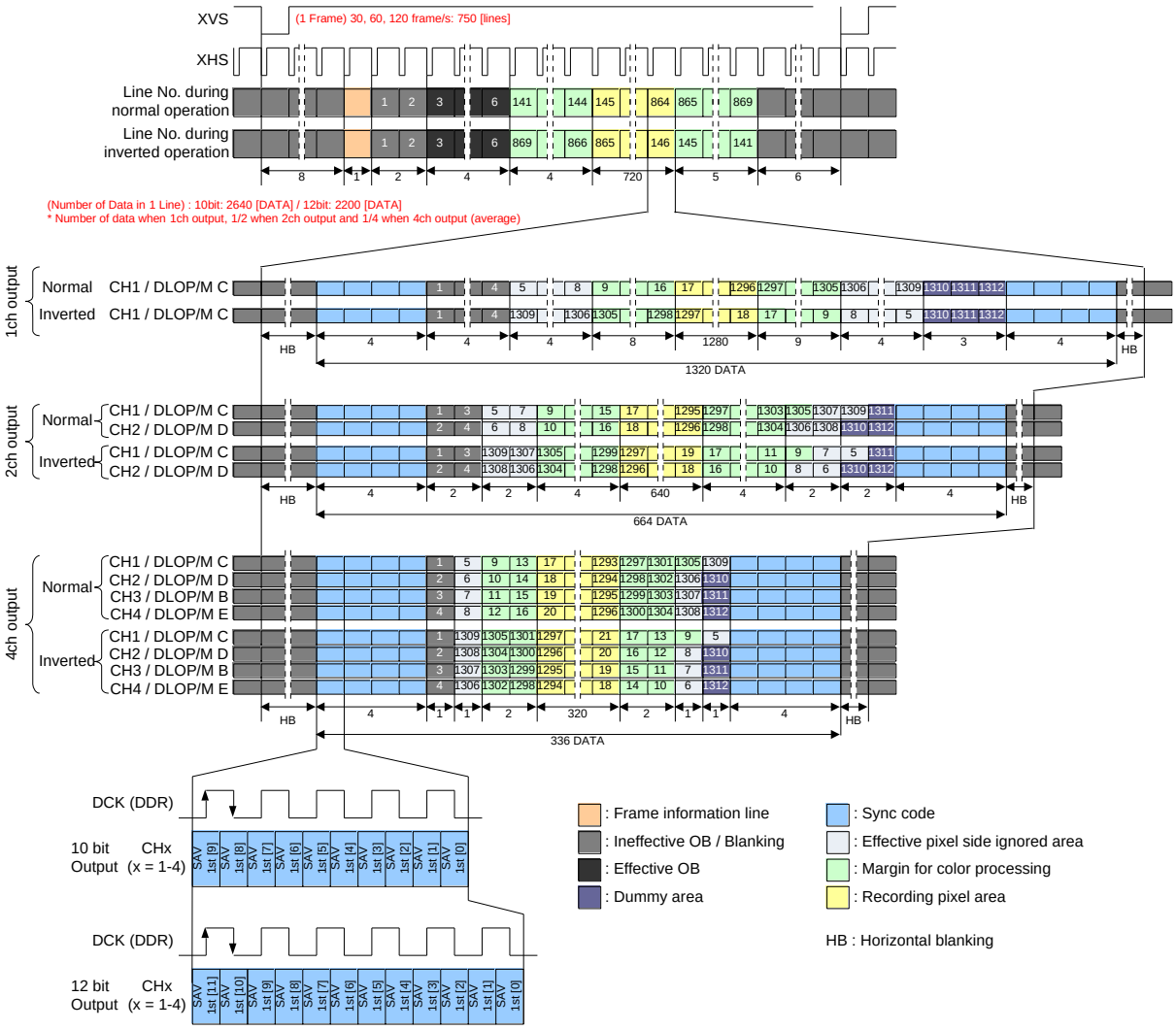
Address		bit	Register Name	Initial Value	CSI-2 serial						Remarks
					1 lane	2 lane		4 lane			
4-wire	I2C				30 [frame /s]	30 [frame /s]	60 [frame /s]	30 [frame /s]	60 [frame /s]	120 [frame /s]	
Chip ID = 05h											
			Data rate		594	297	594	148.5	297	594	[Mbps / Lane]
44h	3344h	[5:4]	REPETITION	2h	0h	1h	0h	2h	1h	0h	—
46h	3346h	[1:0]	PHYSICAL_ LANE_NUM	3h	0h	1h		3h			—
53h	3353h	[5:0]	OB_SIZE_V	Eh	4h						—
57h	3357h	[7:0]	PIC_SIZE_V	3D1h	2D9h						—
58h	3358h	[4:0]									
6Bh	336Bh	[7:0]	THSEXIT	27h	57h	37h	57h	27h	37h	57h	Global timing
6Ch	336Ch	[7:0]	TCLKPRE	1Fh	1Fh						Global timing
7Dh	337Dh	[7:0]	CSI_DT_FMT	0C0Ch	0A0Ah / 0C0Ch						0A0Ah: RAW10 0C0Ch: RAW12
7Eh	337Eh	[7:0]									
7Fh	337Fh	[1:0]	CSI_LANE_ MODE	3h	0h	1h		3h			—
80h	3380h	[7:0]	INCK_FREQ1	3600h	37.125MHz: 2520h 74.25MHz: 4A40h						Set according to INCK
81h	3381h	[7:0]									
82h	3382h	[7:0]	TCLKPOST	57h	6Fh	5Fh	6Fh	57h	5Fh	6Fh	Global timing
83h	3383h	[7:0]	THSPREPARE	0Fh	27h	17h	27h	0Fh	17h	27h	Global timing
84h	3384h	[7:0]	THSZERO	27h	4Fh	37h	4Fh	27h	37h	4Fh	Global timing
85h	3385h	[7:0]	THSTRAIL	0Fh	2Fh	17h	2Fh	0Fh	17h	2Fh	Global timing
86h	3386h	[7:0]	TCLKTRAIL	0Fh	2Fh	17h	2Fh	0Fh	17h	2Fh	Global timing
87h	3387h	[7:0]	TCLKPREPARE	07h	2Fh	17h	2Fh	07h	17h	2Fh	Global timing
88h	3388h	[7:0]	TCLKZERO	37h	9Fh	4Fh	9Fh	37h	4Fh	9Fh	Global timing
89h	3389h	[7:0]	TLPX	1Fh	37h	27h	37h	1Fh	27h	37h	Global timing
8Dh	338Dh	[7:0]	INCK_FREQ2	0367h	37.125MHz: 01B4h 74.25MHz: 0367h						Set according to INCK
8Eh	338Eh	[7:0]									



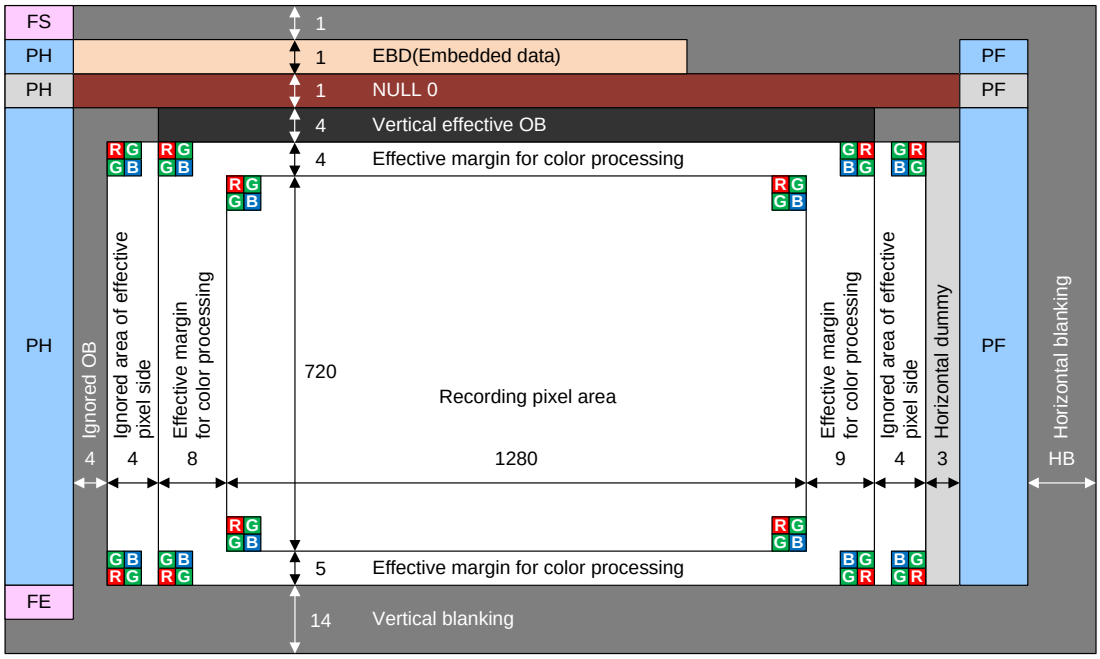
Pixel Array Image Drawing in HD720p mode (Parallel CMOS output / Serial LVDS output)



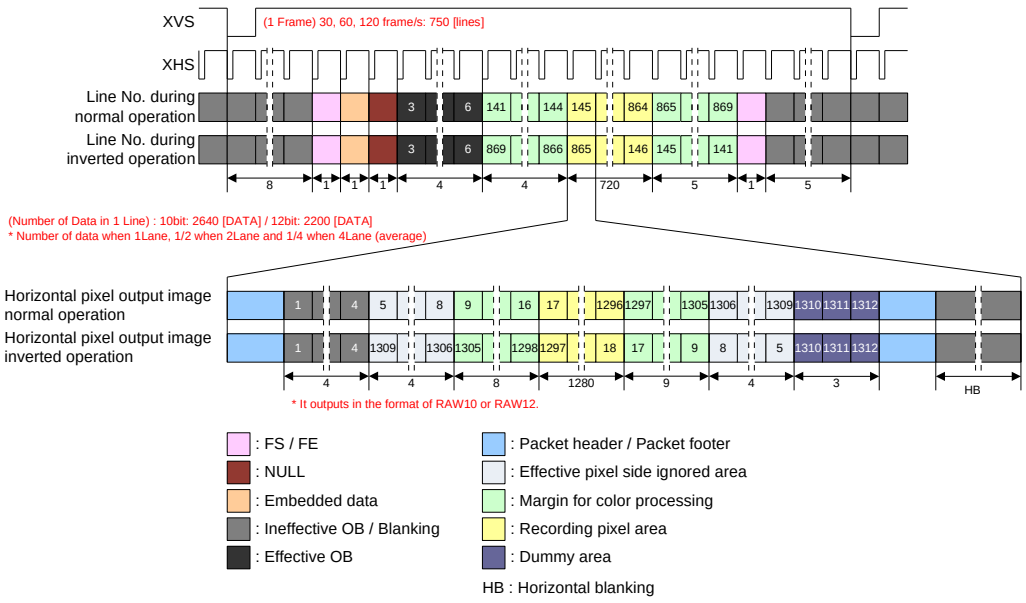
Drive Timing Chart for HD720p mode (Parallel CMOS output)



Drive Timing Chart for HD720p mode (Serial LVDS output)



Pixel Array Image Drawing in HD720p mode (CSI-2 serial output)



Drive Timing Chart for HD720p mode (CSI-2 serial output)

Description of Various Function

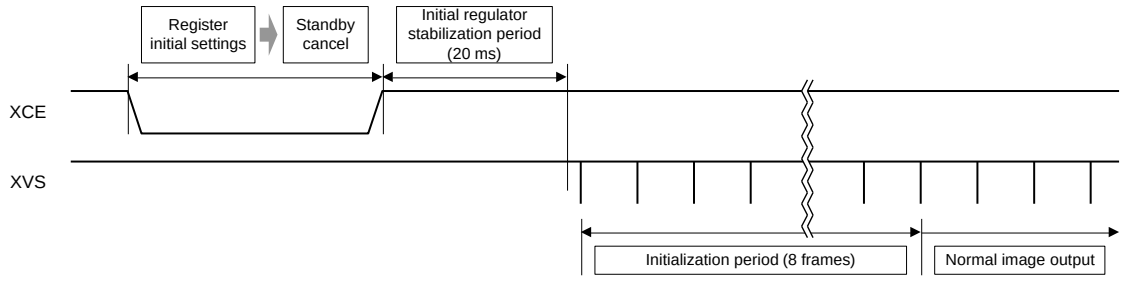
Standby Mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control STANDBY register. Standby mode is also established after power-on or other system reset operation.

List of Standby Mode Setting

Register name	Register details				Initial value	Setting value	Status	Remarks
	Register	ChipID	Address ( ): I^{2}C	bit				
STANDBY	—	02h	00h (3000h)	[0]	1	1	Standby	Register communication is executed in standby mode.
						0	Operating	

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (20 ms or more).



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)

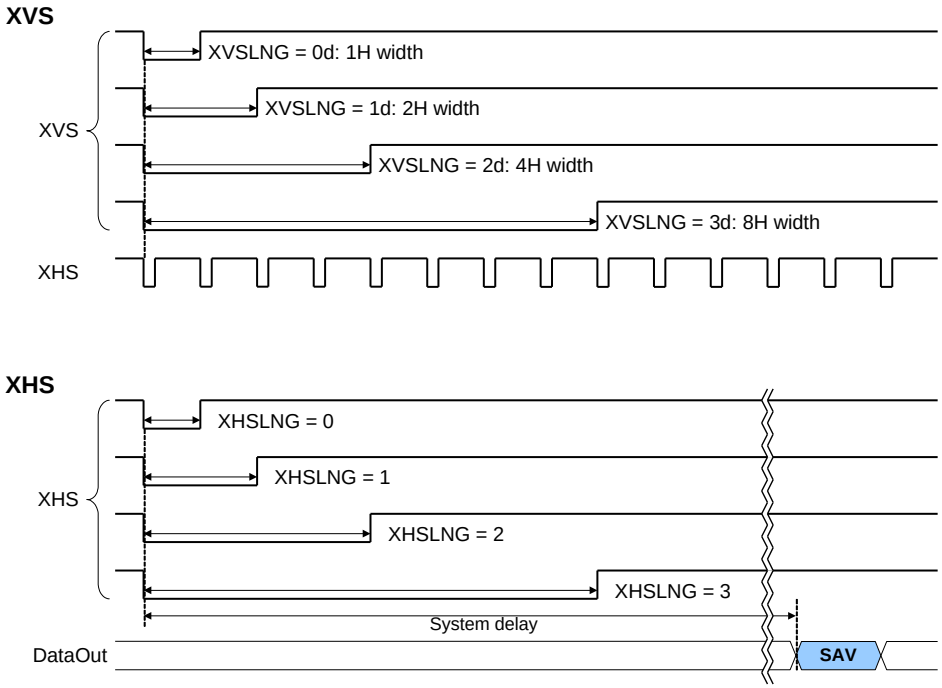
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Operating mode" for the number of output data line and 1H period.
Set the XMSTA register to “0” in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [16:0] register and the clock number in horizontal direction by the HMAX [13:0] register. See the description of Operation Mode for details of the section of “Operating Modes”.

List of Slave and Master Mode Setting

Pin name	Pin processing	Operating mode	Remarks
XMASTER pin	Fixed to Low	Master mode	High: OV_{DD}
	Fixed to High	Slave mode	Low: GND

List of Register in Master Mode

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Remarks
	Register	Address ( ): I^2C	bit			
XMSTA	—	02h (3002h)	[0]	1	1: Master operation ready 0: Master operation start	The master operation starts by setting 0.
VMAX [15:0]	VMAX [7:0]	18h (3018h)	[7:0]	0044Ch	See the item of each drive mode.	Line number per frame designated
	VMAX [15:8]	19h (3019h)	[7:0]			
	VMAX [16]	1Ah (301Ah)	[7:0]			
HMAX [13:0]	HMAX [7:0]	1Bh (301Bh)	[7:0]	1194h	See the item of each drive mode.	Clock number per line designated
	HMAX [13:8]	1Ch (301Ch)	[5:0]			
XVSLNG [1:0]	—	46h (3046h)	[5:4]	0h	0: 1H, 1: 2H, 2: 4H, 3: 8H	XVS low level pulse width designated
XHSLNG [1:0]	—	47h (3047h)	[5:4]	0h	0: Min.to 3: Max. See the next	XHS low level pulse width designated
XVSOUTSEL [1:0]	—	49h (3049h)	[1:0]	0h	0: Fixed to High 2: VSYNC output Others: Setting prohibited	—
XHSOUTSEL [1:0]	—		[3:2]	0h	0: Fixed to High 2: HSYNC output Others: Setting prohibited	—



XVS/XHS output waveform in sensor master mode

List of XHSLNG Register

	CMOS parallel output			LVDS serial output				
DCK	74.25 [MHz]	37.125 [MHz]	18.653 [MHz]	594 [Mbps / ch]	297 [Mbps / ch]	148.5 [Mbps / ch]	74.25 [Mbps / ch]	37.125 [Mbps / ch]
XHSLNG=0	8 clk	4 clk	2 clk	64 bit	32 bit	16 bit	8 bit	4 bit
XHSLNG=1	16 clk	8 clk	4 clk	128 bit	64 bit	32 bit	16 bit	8 bit
XHSLNG=2	32 clk	16 clk	8 clk	256 bit	128 bit	64 bit	32 bit	16 bit
XHSLNG=3	64 clk	32 clk	16 clk	512bit	256 bit	128 bit	64 bit	32 bit

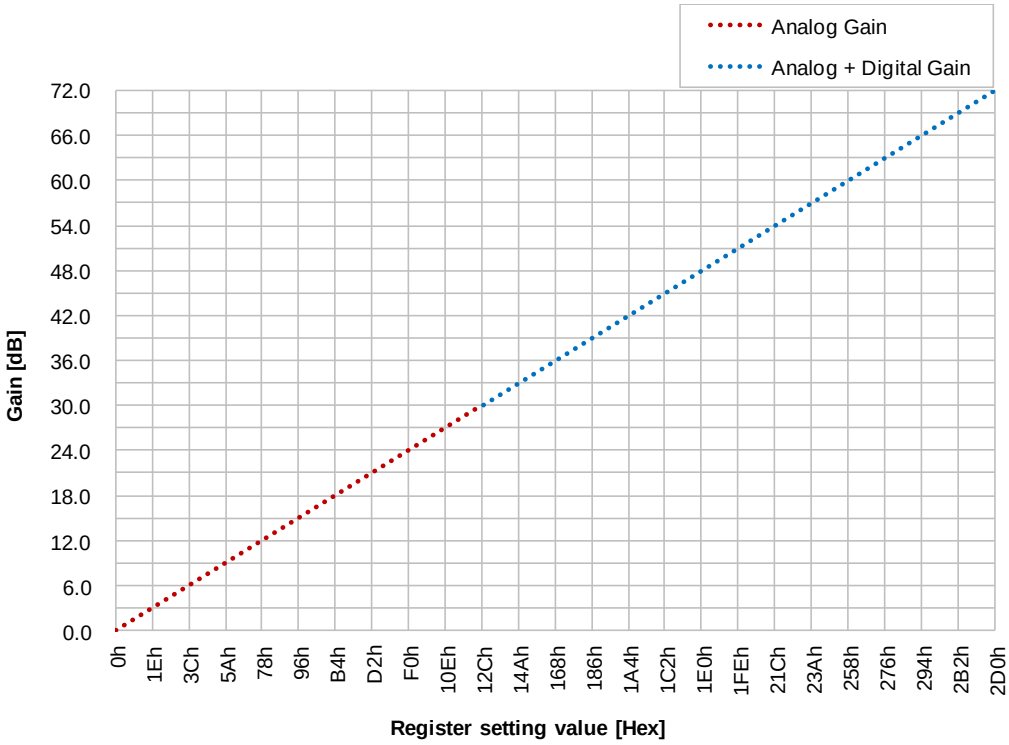
* In 2 × 2 binning mode, output values are 1/2.

The XVS and XHS are output in timing that set 0 to the register XMSTA. If set 0 to XMSTA during standby, the XVS and XHS are output just after standby is released. The XVS and XHS are output asynchronous with other input or output signals. In addition, the output signals are output with a undefined latency time (system delay) relative to the XHS. Therefore, refer to the sync codes output from the sensor and perform synchronization.

Gain Adjustment Function

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block. The total of analog gain and digital gain can be set up to 72 dB by the GAIN [9:0] register setting. The same setting is applied in all colors. The value which is ten times the gain is set to register.

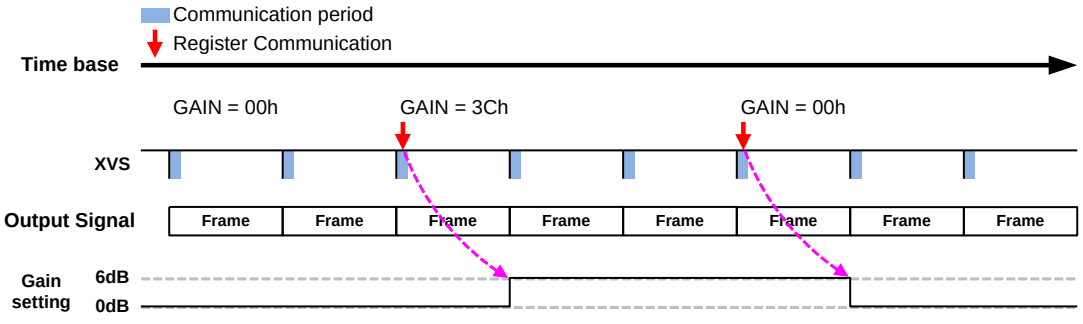
Example)
When set to 6 dB: 6 × 10 = 60d; GAIN [9:0] = 3Ch
When set to 12.8 dB: 12.8 × 10 = 128d; GAIN [9:0] = 80h



List of PGC Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Remarks
	Register	Address ( ): I²C	bit		Setting range	
GAIN [8:0]	GAIN [7:0]	14h (3014h)	[7:0]	000h	000h-2D0h (0d-720d)	Setting value: Gain [dB] × 10
	GAIN [9:8]	15h (3015h)	[1:0]			

The gain setting is reflected at the next frame that the communication is performed as shown below.



Gain Reflection Timing

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 1FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [8:0] register. When the BLKLEVEL setting is increased by 1 LSB, the black level is increased by 1 LSB.

Use with values shown below is recommended.
10-bit output: 03Ch (60d)
12-bit output: 0F0h (240d)

List of Black Level Adjustment Register

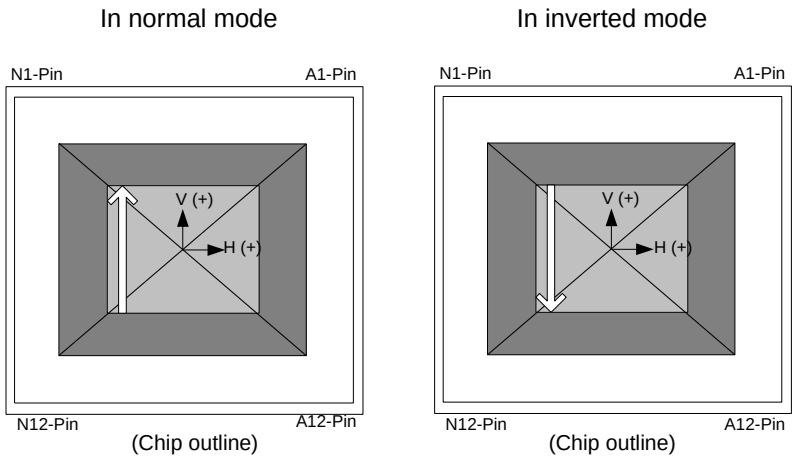
Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ): I^2C	bit		
BLKLEVEL [8:0]	BLKLEVEL [7:0]	0Ah (300Ah)	[7:0]	03Ch	000h～1FFh
	BLKLEVEL [8]	0Bh (300Bh)	[0]		

Normal Operation and Inverted Operation

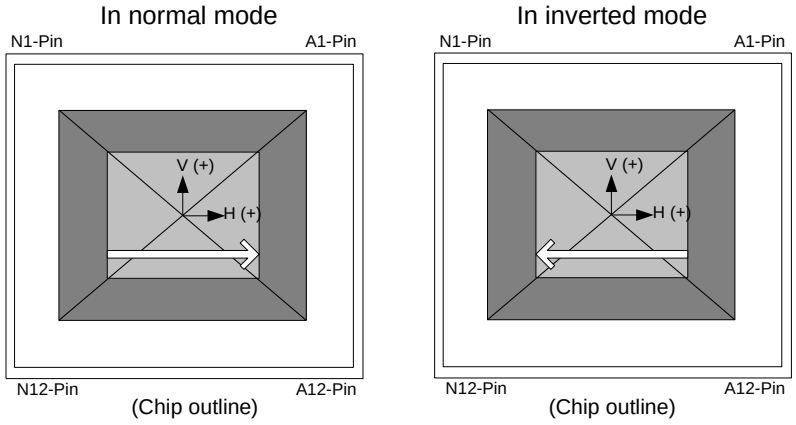
The sensor readout direction (normal / inverted) in vertical direction can be switched by the VREVERSE register setting and in horizontal direction can be switched by the HREVERSE register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes. One invalid frame is generated when reading immediately after the readout direction change in order to switch the normal operation and inversion between frames.

List of Drive Direction Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ): I^2C	bit		
VREVERSE	—	07h (3007h)	[0]	0h	0: Normal (Initial value) 1: Vertical Inverted
HREVERSE	—		[1]	0h	0: Normal (Initial value) 1: Horizontal Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period - (SHS1 + 1) × (1H period)

*1 The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).
*2 See “Operating Modes” for the 1H period.

In this section, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

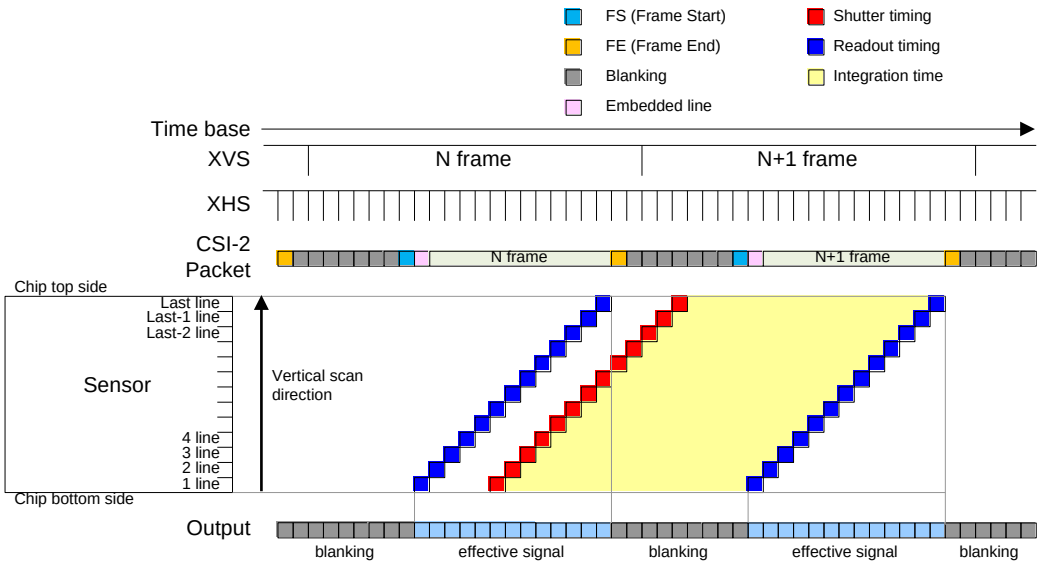


Image Drawing of Shutter Operation

Normal Exposure Operation (Controlling the Integration Time in 1H Units)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS1 [16:0] register. Set SHS1 [16:0] to a value between 2 and (Number of lines per frame - 1). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit.
When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX register. The number of lines per frame differs according to the operating mode.

List of integration time setting register in 1 H unit

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ): I^2C	bit		
SHS1 [16:0]	SHS1 [7:0]	20h (3020h)	[7:0]	00000h	Sets the shutter sweep time. 2 to (Number of lines per frame - 2) * Number of lines per frame -1 setting is prohibited
	SHS1 [15:8]	21h (3021h)	[7:0]		
	SHS1 [16]	22h (3022h)	[0]		
VMAX [16:0]	VMAX [7:0]	18h (3018h)	[7:0]	0044Ch	Sets the number of lines per frame (only in master mode). See “Operating Modes” for the setting value in each mode.
	VMAX [15:8]	19h (3019h)	[7:0]		
	VMAX [16]	1Ah (301Ah)	[0]		

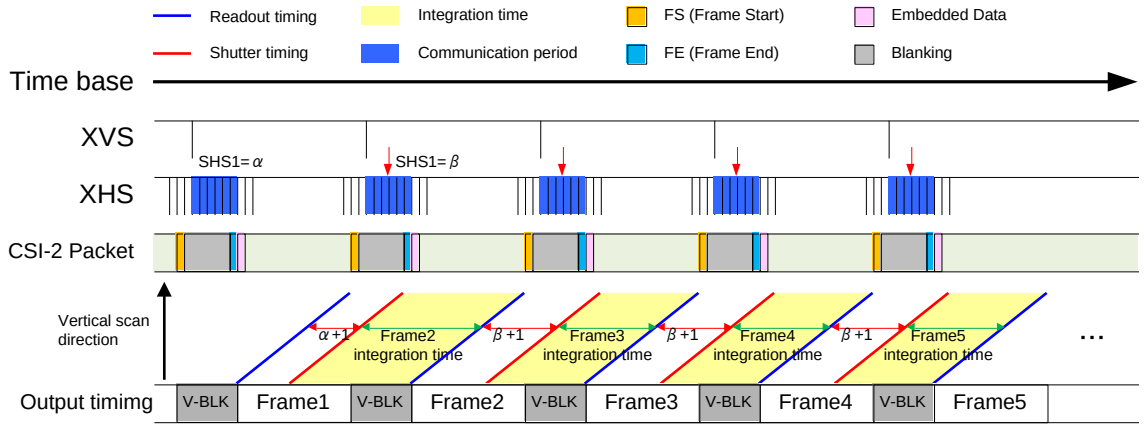


Image Drawing of Integration Time Control within a Frame

Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval. When the sensor is operating in master mode, it is done by designating a larger register VMAX [16:0] value compared to normal operation. When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount. The maximum VMAX and SHS1 [16:0] values are 131071d. When the number of lines per frame is set to the maximum value, the integration time in Quad VGA mode at 60 frame / s is approximately 1.9 s. However, set the upper limit of the long exposure operation to be one second. When set to a number of V lines or more than that noted for each operating mode, the imaging characteristics are not guaranteed during long exposure operation.

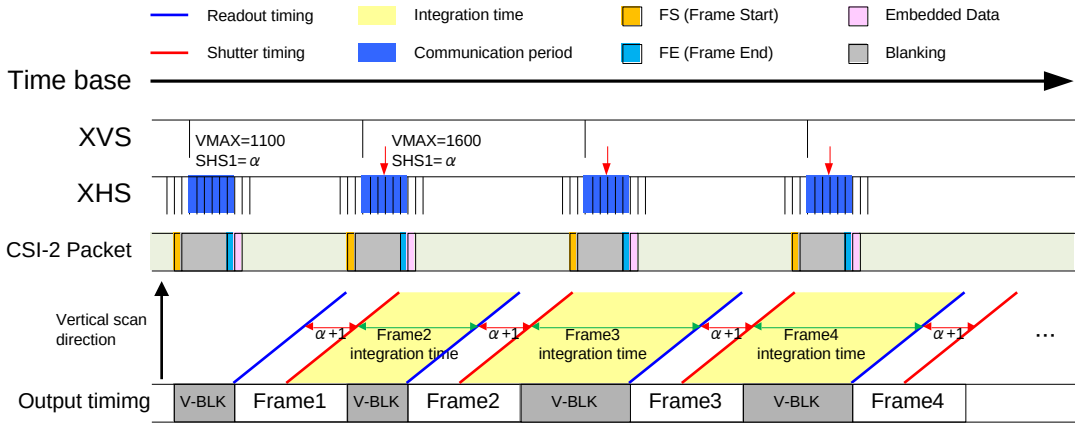


Image Drawing of Long Integration Time Control by Adjusting the Frame Period

Example of Integration Time Settings

The example of register setting for controlling the storage time is shown below.

Example of Integration Time Settings (In Quad VGA)

Operation	Sensor setting (register)		Integration time
	VMAX*	SHS1**	
Normal frame rate	1100	1100	Setting prohibited
		1099	Setting prohibited
		1098	1H
		⋮	⋮
		N	(1100 - (N + 1)) H
		⋮	⋮
		2	1097H
		1	Setting prohibited
		0	Setting prohibited
Long time exposure Operation (Control by Expanding the Number of Lines per Frame)	M	N	(M - (N + 1) H

* In sensor master mode. In slave mode, the interval is the same as XVS input.
** The SHS1 setting value (N) is set between “2” and “the VMAX value (M) – 2”.

Signal Output

Output Pin Settings

The output formats of this sensor support the following modes.

CMOS logic parallel SDR output
Low voltage LVDS serial (1 ch / 2 ch / 4 ch switching) DDR output
CSI-2 serial (1 Lane / 2 Lane / 4 Lane, RAW10 / RAW12) output

The switching for serial interface is made by the OMODE pin. Establish the OMODE pin status before canceling the system reset. (Do not switch this pin status during operation.) Each mode is set using the register OPORTSEL. The table below shows the output format settings.

List of Interface Switching

Pin name	Pin	Interface	Remarks
OMODE pin	Fixed to Low	CSI-2 serial	High: OVDD Low: GND
	Fixed to High	CMOS parallelSDR Low voltage LVDS serial	

List of Output Interface Setting Register

Register name	Register details (Chip ID = 02h)		Initial value	Setting value	Description
	Address ( ) : I^2C	bit			
OPORTSEL [3:0]	44h (3044h)	[7:4]	0h	0h	CMOS logic parallel SDR output
				Ch	Low voltage LVDS serial 1ch DDR
				Dh	Low voltage LVDS serial 2ch DDR
				Eh	Low voltage LVDS serial 4ch DDR
				0h	CSI-2 serial 1Lane
				0h	CSI-2 serial 2Lane
				0h	CSI-2 serial 4Lane
SCDEN	54h (3054h)	[0]	1h	0h	Sync code Disable (In CSI-2, must set to 0h.)
				1h	Sync code Enable (In CMOS parallel and in Low voltage LVDS serial, must set to 1h.)

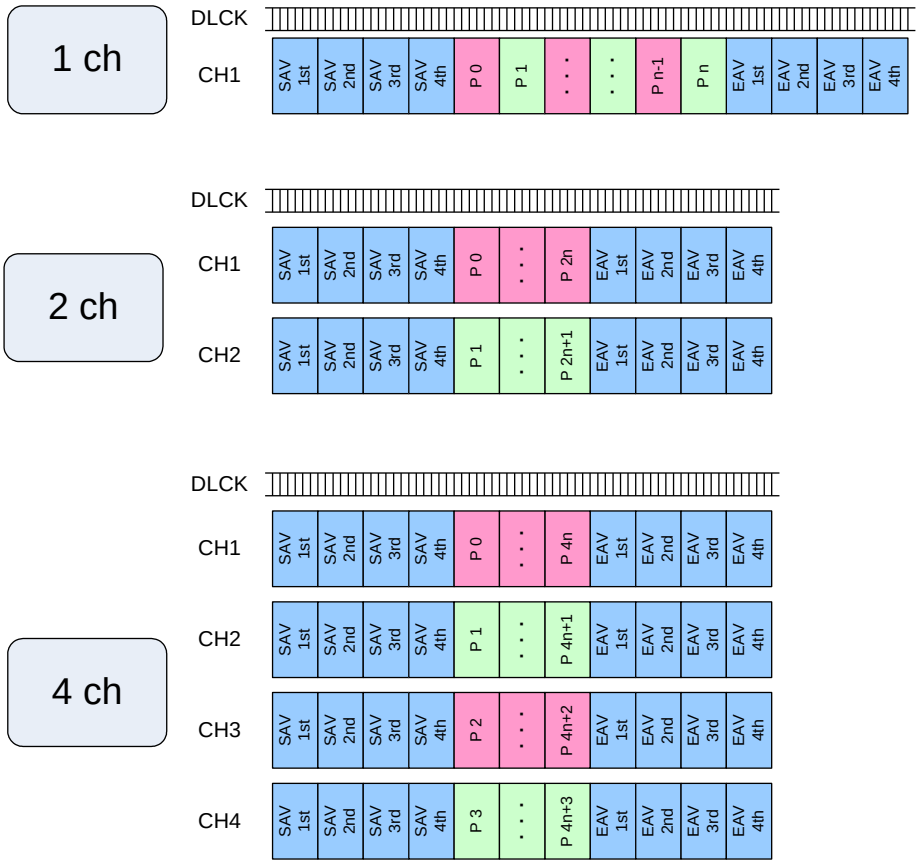
* In CMOS output, Clock is output from DLCKP pin. DLCKM pin is fixed to low level.
* In CSI-2 output, set registers thatdescribed in section “CSI-2 output setting”.

Each output pin is shown in the table below when setting low-voltage LVDS serial 1 ch / 2 ch / 4 ch output.

Output Pins for Low LVDS Serial and CMOS parallel

DLOP/DLOM	CMOS logic parallel SDR output		Low voltage LVDS serial DDR output		
	10bit	12bit	1 ch	2 ch	4 ch
DLOMF	DO9	DO11	Hi-Z	Hi-Z	Hi-Z
DLOPF	DO8	DO10	Hi-Z	Hi-Z	Hi-Z
DLOME	DO7	DO9	Hi-Z	Hi-Z	Ch4 / M
DLOPE	DO6	DO8	Hi-Z	Hi-Z	Ch4 / P
DLOMD	DO5	DO7	Hi-Z	Ch2 / M	Ch2 / M
DLOPD	DO4	DO6	Hi-Z	Ch2 / P	Ch2 / P
DLOMC	DO3	DO5	Ch1 / M	Ch1 / M	Ch1 / M
DLOPC	DO2	DO4	Ch1 / P	Ch1 / P	Ch1 / P
DLOMB	DO1	DO3	Hi-Z	Hi-Z	Ch3 / M
DLOPB	DO0	DO2	Hi-Z	Hi-Z	Ch3 / P
DLOMA	Low fixed	DO1	Hi-Z	Hi-Z	Hi-Z
DLOPA	Low fixed	DO0	Hi-Z	Hi-Z	Hi-Z

Low-voltage LVDS serial 1 ch / 2 ch / 4 ch output format is shown in the figure below.
When setting 1 ch, after four data of SAV is output in the order of CH1 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 respectively.
When setting 2 ch, after four data of SAV is output in the order of CH1 and CH2 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 and CH2 respectively.
When setting 4 ch, after four data of SAV is output in the order of CH1, CH2, CH3 and CH4 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1, CH2, CH3 and CH4 respectively.
Data is sent MSB first.
For details, see drive timing in each mode in the section of "Operation Mode".



Output Format of Low voltage LVDS Serial 1 ch / 2 ch / 4 ch

CSI-2 output

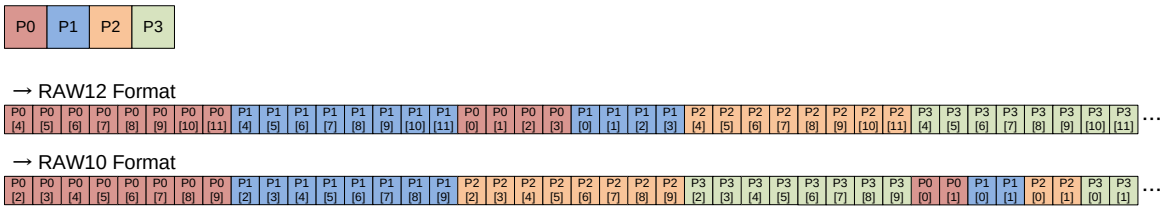
The output formats of this sensor support the following modes.

CSI-2 serial 1 Lane / 2 Lane / 4 Lane, RAW10 / RAW12

The 1 Lane / 2 Lane / 4 Lane serial signal output method using the IMX225LQR is described below.
Complied with the CSI-2, data is output using 1 Lane / 2 Lane / 4 Lane. The image data is output from the CSI-2 output pin. The DMO1P/DMO1N are called the Lane1 data signal, the DMO2P/DMO2N are called the Lane2 data signal, the DMO3P/DMO3N are called the Lane3 data signal, the DMO4P/DMO4N are called the Lane4 data signal. In addition, the clock signals are output from DMCKP/DMCKN of the CSI-2 pins.
In 1 Lane mode, data is output from Lane1. In 2 Lane mode, data is output from Lane1 and Lane2. In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4. The bit rate maximum value is 594 Mbps / Lane.
The select of RAW10 / RAW12 is set by the register: CSI_DT_FMT [15:0].
The number of output lanes is set by the register: CSI_LANE_MODE [1:0] and the number of lanes physically connected is set by PHYSICAL_LANE_NUM [1:0]. Unused lanes (when setting 1 lanes; DMO2P / DMO2N, DMO3P / DMO3N, DMO4P / DMO4N, when setting 2 lanes; DMO3P / DMO3N, DMO4P / DMO4N) are set to Hi-Z output by the setting. When the number of lanes more than CSI_LANE_MODE is set by PHYSICAL_LANE_NUM, unused lanes output signals conformed to MIPI standard.

Register name	Register details (Chip ID = 05h)		Initial value	Setting value	Description
	Address ( ): I^2C	bit			
CSI_DT_FMT [15:0]	7Dh (307Dh)	[7:0]	0C0Ch	0A0Ah	RAW10
	7Eh (307Eh)	[7:0]		0C0Ch	RAW12
PHYSICAL_LANE_NUM [1:0]	46h (3046h)	[1:0]	3h	0h	1Lane
				1h	2Lane
				2h	Setting prohibited
				3h	4Lane
CSI_LANE_MODE [1:0]	7Fh (307Fh)	[1:0]	3h	0h	1Lane
				1h	2Lane
				2h	Setting prohibited
				3h	4Lane

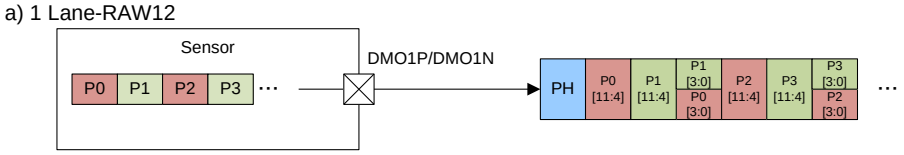
The formats of RAW12 and RAW10 are shown below.



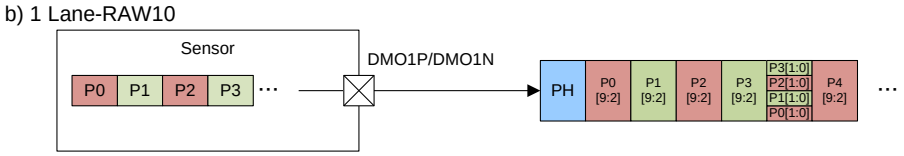
The Example of Format of RAW12 / RAW10

The each formal of 1 Lane, 2 Lane and 4 Lane are shown below.

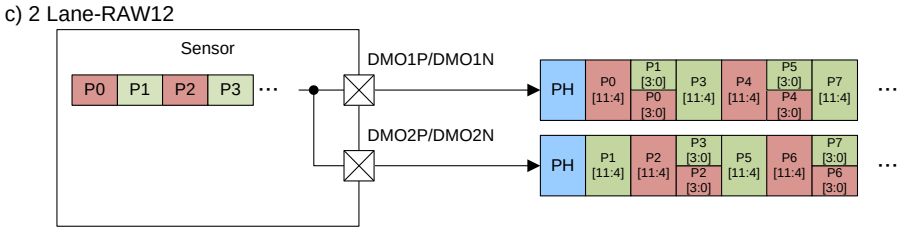
a) 1 Lane-RAW12



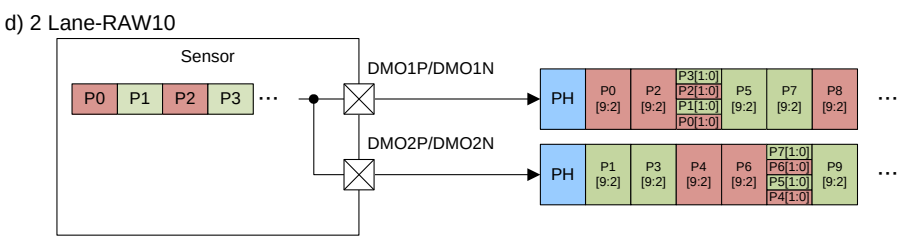
b) 1 Lane-RAW10



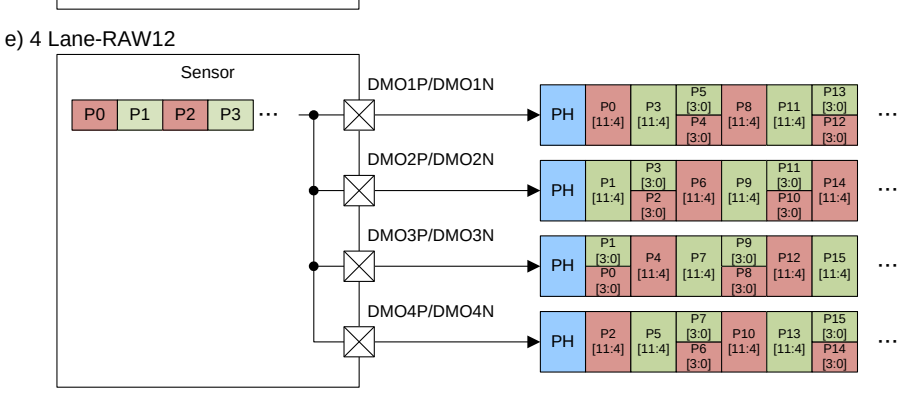
c) 2 Lane-RAW12



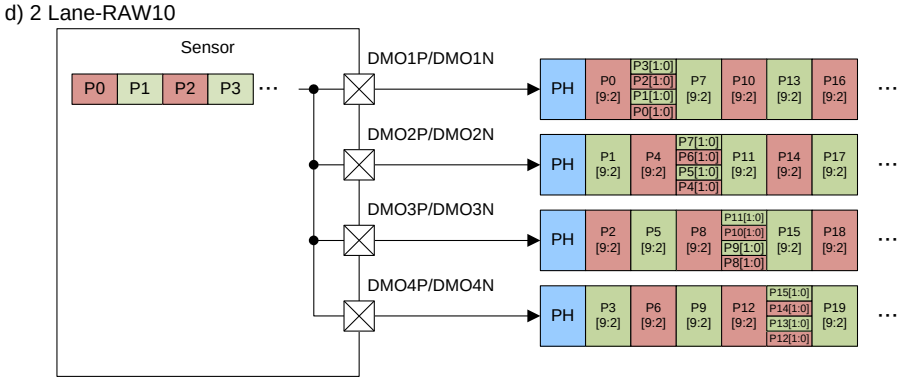
d) 2 Lane-RAW10



e) 4 Lane-RAW12



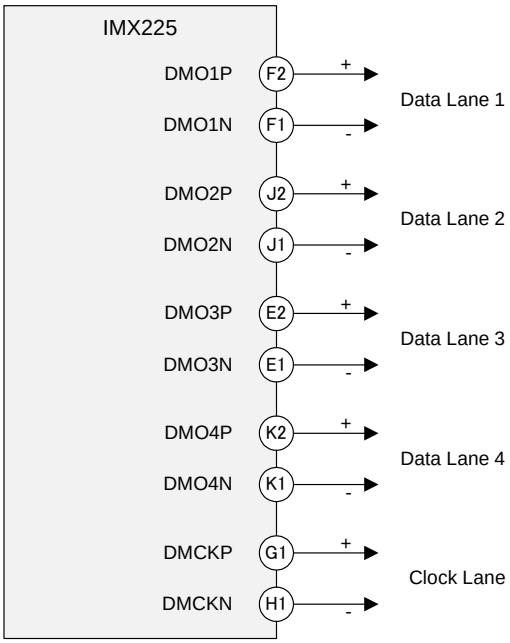
d) 2 Lane-RAW10



1 Lane / 2 Lane / 4 Lane Output Format

MIPI Transmitter

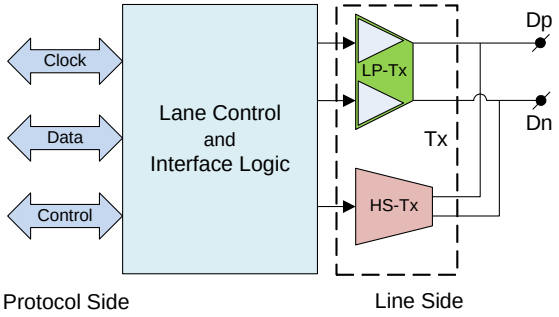
Output pins (DMO1P, DMO1N, DMO2P, DMO2N, DMO3P, DMO3N, DMO4P, DMO4N, DMCKP, DMCKN) are described in this section.



Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard
・MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.01.00
・MIPI Alliance Specification for D-PHY Version 1.00.00

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver. The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane are 594 Mbps / Lane.



Universal Lane Module Functions

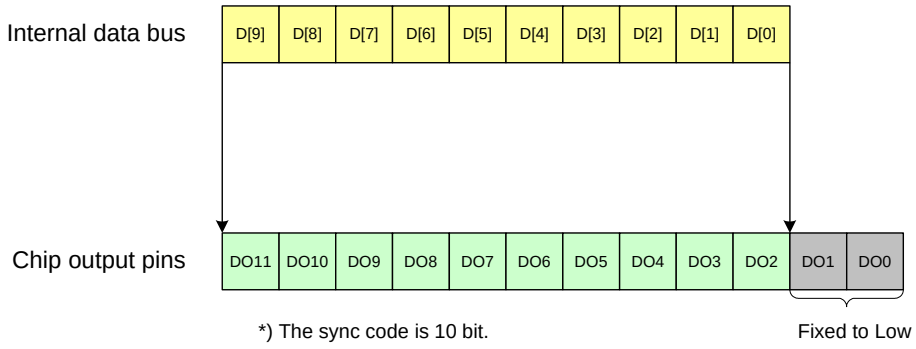
Output Pin Bit Width Selection

The output pin width can be selected from 10-bit or 12-bit output using the register ODBIT. In parallel output mode, when ODBIT = 0 (10-bit output), the lower 2 bits are fixed to Low level in CMOS output mode. Therefore, when using only 10 bits, the pins corresponding to the lower 2 bits can be left open on the board by setting ODBIT = 0. When low-voltage LVDS serial output, continuous data is output MSB first by 10-bit and 12-bit output setting respectively. 10-bits sync code are output when ODBIT = 0 (10-bit output), and 12-bit sync codes are output when ODBIT = 1 (12-bit output).

Output Pin Bit Width Selection Setting Register

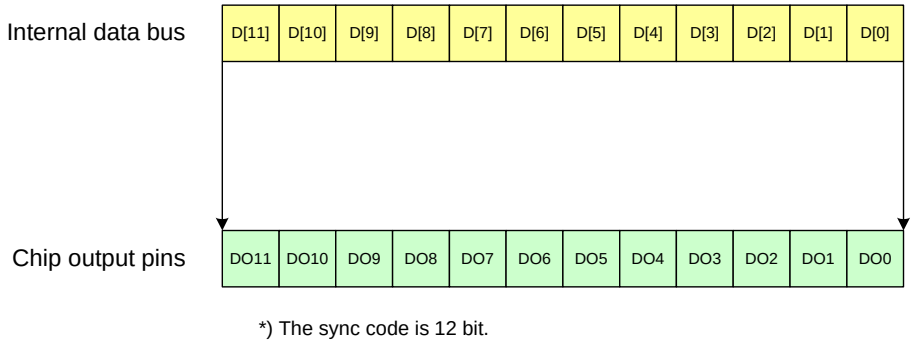
Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ): I^2C	bit		
ODBIT	—	44h (3044h)	[0]	0h	0: 10 bit 1: 12 bit

ODBIT = 0 (CMOS Parallel 10 bit output)



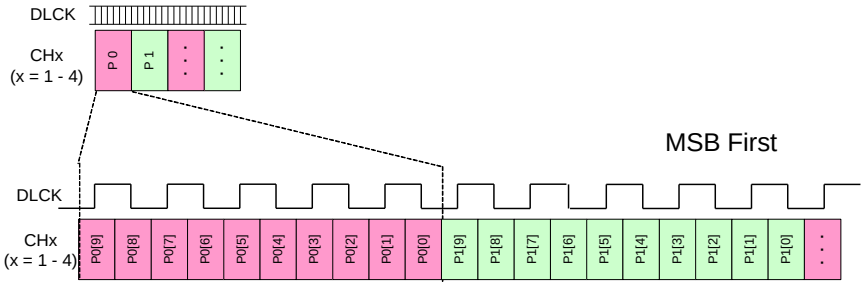
Bit Assignments in Parallel 10-bit Output Mode

ODBIT = 1 (CMOS Parallel 12 bit output)



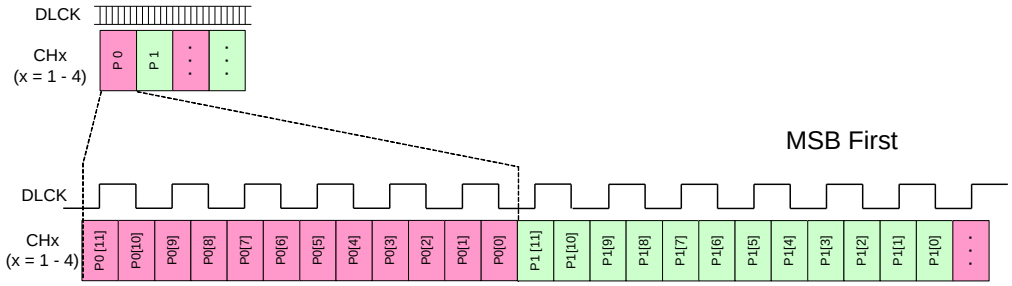
Bit Assignments in Parallel 12-bit Output Mode

ODBIT = 0 (Low voltage LVDS serial 10 bit output)



Example of Data format in low-voltage LVDS serial 10-bit output

ODBIT = 1 (Low voltage LVDS serial 12 bit output)



Example of Data format in low-voltage LVDS serial 12-bit output

Number of Internal A/D Conversion Bits Setting

The number of internal A/D conversion bits can be selected from 10 bits or 12 bits by the register ADBIT. See the section of “Operating Modes” for the correspondence with each mode.

List of Bit Width Selection

Register name	Register details Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ): I^2C	bit		
ADBIT	—	05h (3005h)	[0]	0h	0: 10 bit 1: 12 bit

Output Rate Setting

The sensor output rate is determined uniformly by the sensor operating mode and the output format. See the section of “Operating Modes” for the relationship between each setting and the frame rate, data rate and data bit rate. The registers related to mode setting are shown in the table below.

Related Registers for Setting Operation Mode

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ): I^2C	bit		
MODE [7:0]	—	06h (3006h)	[7:0]	00h	00h: All-pixel scan (Quad VGA, HD720p) 22h: 2×2 binning 33h: Horizontal / Vertical1/2 subsampling Others: Setting prohibited
WINMODE [0]	—	07h (3007h)	[6:4]	0h	0: Quad VGA 1: HD720p 4: Window cropping mode
FRSEL [1:0]	—	09h (3009h)	[1:0]	1h	0: 120 fps 1: 60 fps 2: 30 fps 3: Setting prohibited

Output Signal Range

CMOS parallel / Low voltage LVDS serial

The sensor output has either a 10-bit or 12-bit gradation, but output is not performed over the full range, and the maximum output value is the (3FFh - 1) value (10-bit output) and the (FFFh - 1) one (12-bit output). In addition, the minimum value is 001h. The output range for each output gradation is shown in the table below.
See the item of “Sync Codes” in the section of “Operating Modes” for the sync codes.

Output Gradation and Output Range

Output gradation	Output Value	
	Min.	Max,
10bit	001h	3FEh
12bit	001h	FFEh

CSI-2 serial

The sensor output has either a 10-bit or 12-bit gradation, and the maximum output value is the 3FFh value (10-bit output) and the FFFh one (12-bit output). In addition, the minimum value is 000h. The output range for each output gradation is shown in the table below.

Output Gradation and Output Range

Output gradation	Output Value	
	Min.	Max,
10bit	000h	3FFh
12bit	000h	FFFh

INCK Setting

The available operation mode varies according to INCK frequency. Input either 27 MHz or 54 MHz or 37.125 MHz or 74.25 MHz for INCK frequency. The INCK setting register and the list of INCK setting are shown in the table below.

INCK Setting Register

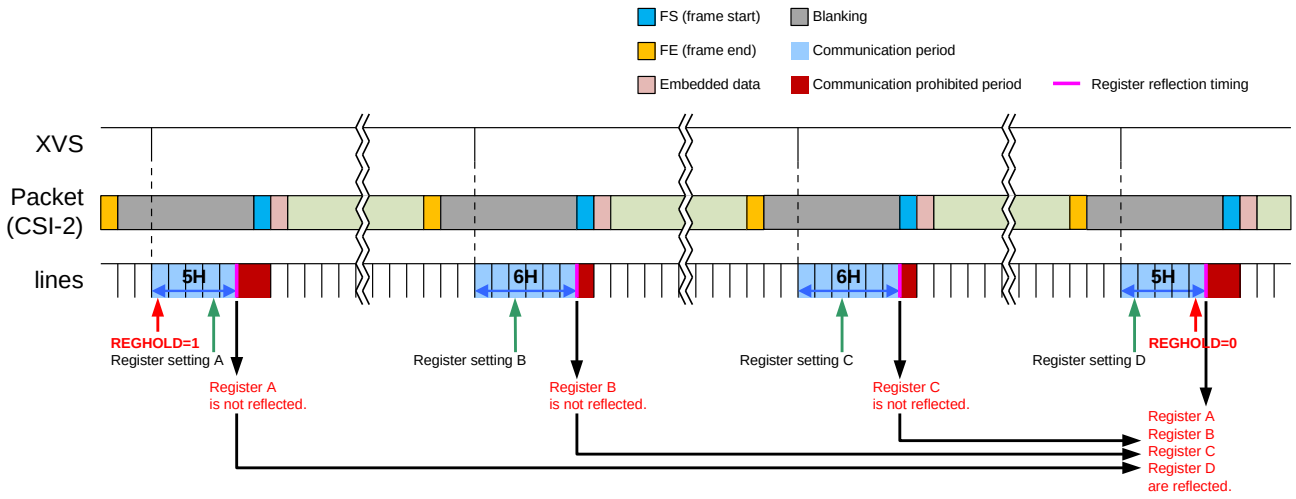
Register name	Register details (Chip ID = 02h)			Initial value	INCK			
	Register	Address ( ): I²C	bit		27 [MHz]	54 [MHz]	37.125 [MHz]	74.25 [MHz]
INCKSEL1	—	5Ch (305Ch)	[7:0]	2Ch	2Ch	2Ch	20h	20h
INCKSEL2	—	5Dh (305Dh)	[7:0]	10h	00h	10h	00h	10h
INCKSEL3	—	5Eh (305Eh)	[7:0]	2Ch	2Ch	2Ch	20h	20h
INCKSEL4	—	5Fh (305Fh)	[7:0]	10h	00h	10h	00h	10h

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register. In case of communicate to REGHOLD register only, communication period wil be 5H and communication prohibited period will be 2H.

Register Hold Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ): I²C	bit		
REGHOLD	—	01h (3001h)	[0]	0h	0: Invalid 1: Valid (Register hold)



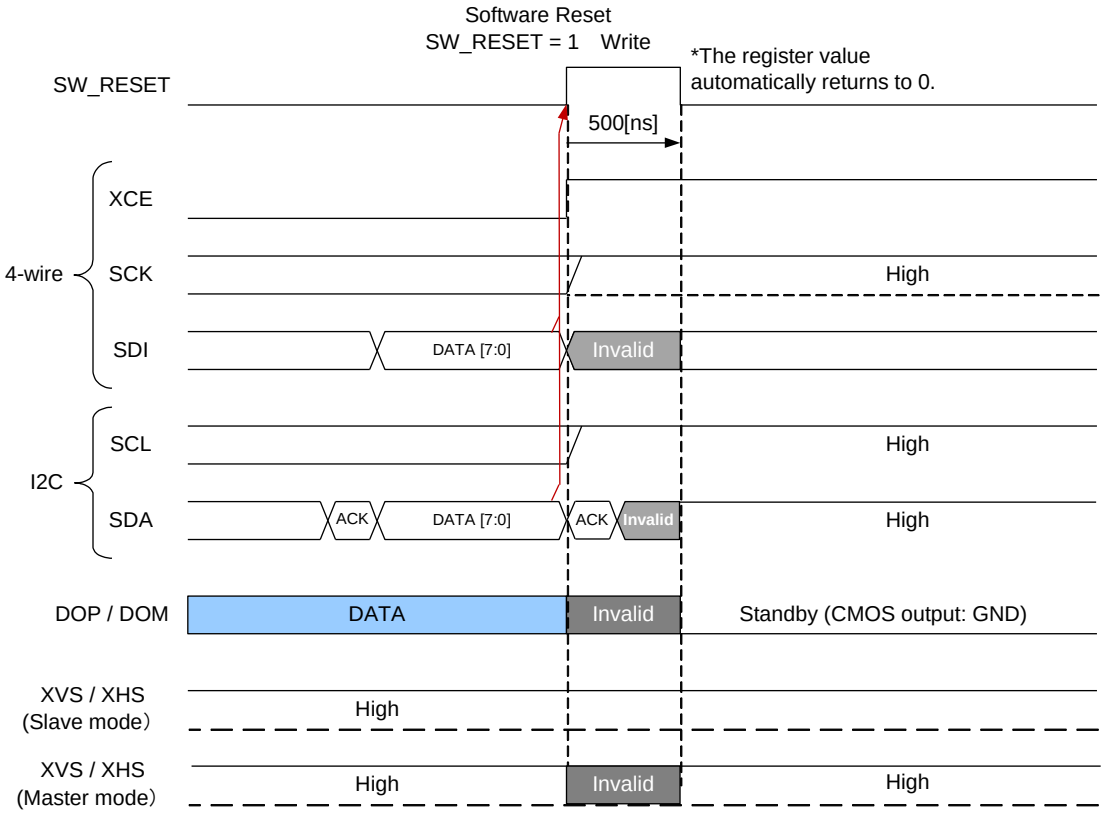
Register Hold Setting

Software Reset (CMOS parallel / Low voltage LVDS serial only)

This function is prohibited in CSI-2 output mode.
Software reset can be performed by register setting using the register SW_RESET.
Sensor reset is performed by setting SW_RESET = 1. However, the communication to continuous address cannot use. The registers become initial state and standby 500 ns after setting SW_RESET = 1. The SW_RESET signal returns to "0" automatically. DLOPA-F / DLOMA-F / DLCKP / DLCKM pins will become standby state of CMOS output (GND). The XVS and XHS output High in master mode. Input High to the XVS and XHS before setting SW_RESET = 1 in slave mode. Follow the sequence in the item of "Standby Mode" to perform register initial setting and standby cancel from standby state.

Software Reset Register Setting

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ): I^2C	bit		
SW_RESET	—	03h (3003h)	[0]	0h	0: Normal Operation 1: Reset



Software Reset

Mode Transitions

When changing the operating mode during sensor drive operation, set via sensor standby. However, these transitions that described below can be transitions without standby.

- ◆Change the number of vertical lines (In sensor master mode, change the VMAX. In sensor slave mode, change the period of XVS input.)
- ◆Horizontal and vertical scan direction. (When the vertical scan direction is changed, an invalid frame generates during transition.)
- ◆Change the HCG mode and LCG mode.
- ◆Change the mode between All-pixel scan and Window cropping. (However, It is case that transitions by not changing register HMAX and FRSEL. In addition, an invalid frame generates during transition.)

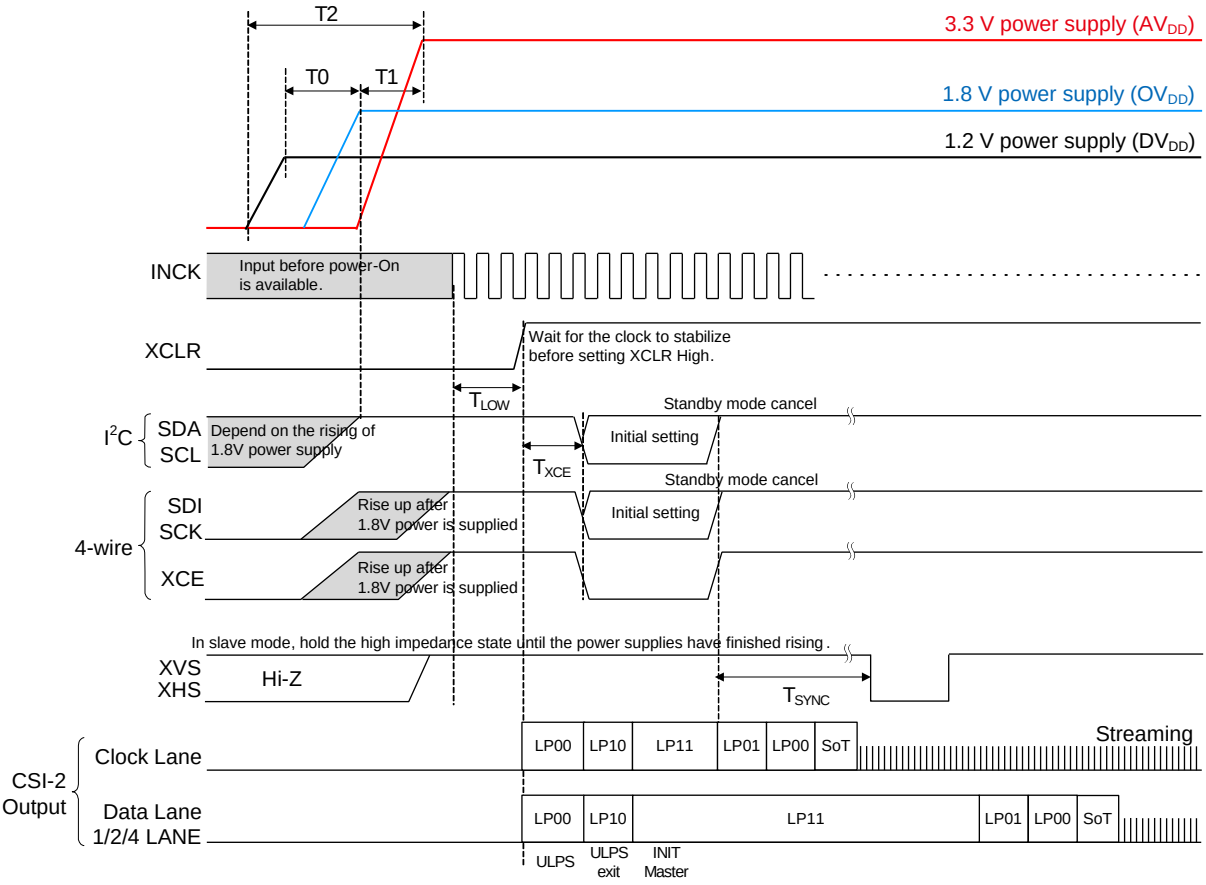
When changing input INCK frequency (register INCKSEL1, INCKSEL2, INCKSEL3, and INCKSEL4 change) or when operating mode transition that changes output bit width (register ODBIT) or output format (register OPORTSEL [3:0]), always start the operation via sensor standby after changing mode during standby following the standby cancel sequence.

When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

Power-on and Power-off Sequence

Power-on sequence

1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 3.3 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. Start master clock (INCK) input after turning On the power supplies.
3. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.) In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}).
4. The system clear is applied by setting XCLR to High level. However, the maser clock needs to stabilize before setting the XCLR pin to High level.
5. Make the sensor setting by register communication after the system clear. A period of 20 µs or more should be provided after setting XCLR High before inputting the communication enable signal XCE. In I^2C communication, XCE is fixed to High.

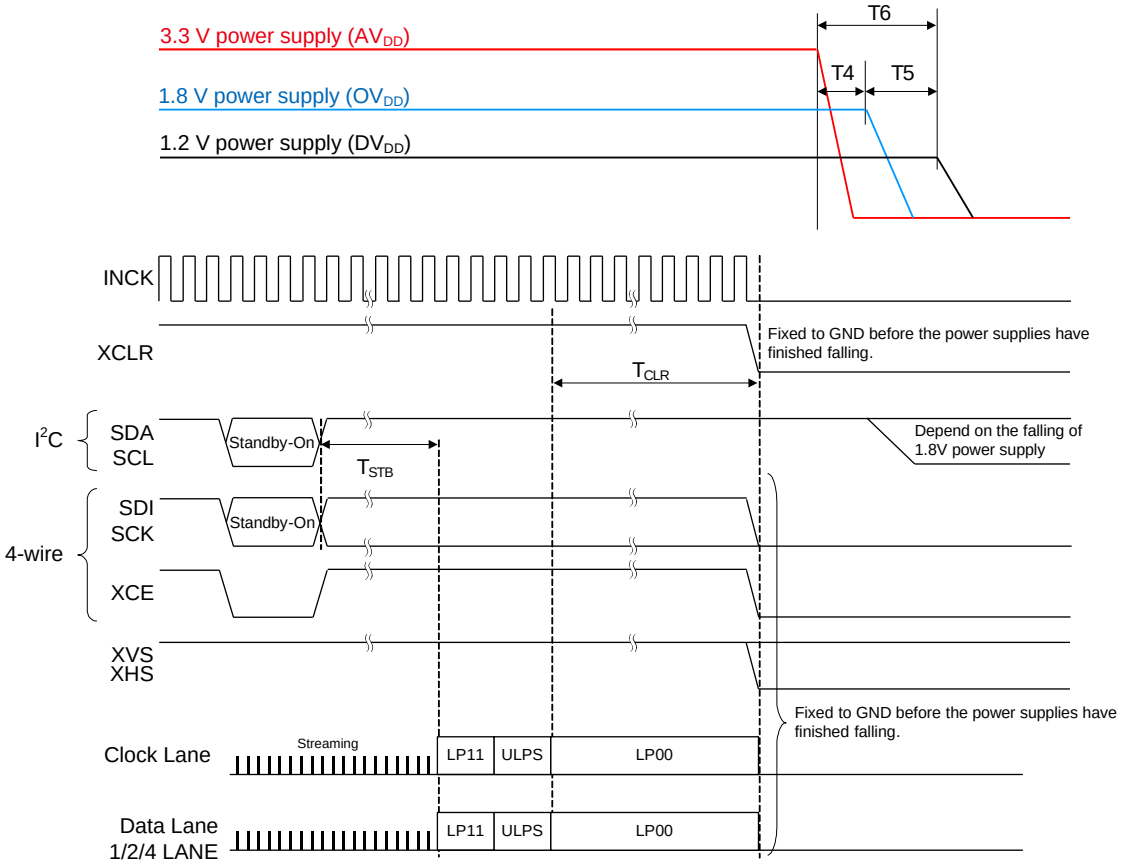


Power-on Sequence

Item	Symbol	Min.	Max.	Unit
1.2 V power supply rising → 1.8 V power supply rising	T0	0	—	ns
1.8 V power supply rising → 3.3 V power supply rising	T1	0	—	ns
Rising time of all power supply	T2	—	200	ms
INCK active → Clear OFF	T_{LOW}	500	—	ns
Clear OFF → Communication start	T_{XCE}	20	—	µs
Standby OFF (communication) → External input XHS,XVS (slave mode only)	T_{SYNC}	20	—	ms

Power-off sequence

Turn Off the power supplies so that the power supplies fall in order of 3.3 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should falling within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, OMODE, XVS, XHS) to 0 V before the 1.8 V power supply (OV_{DD}) falls.



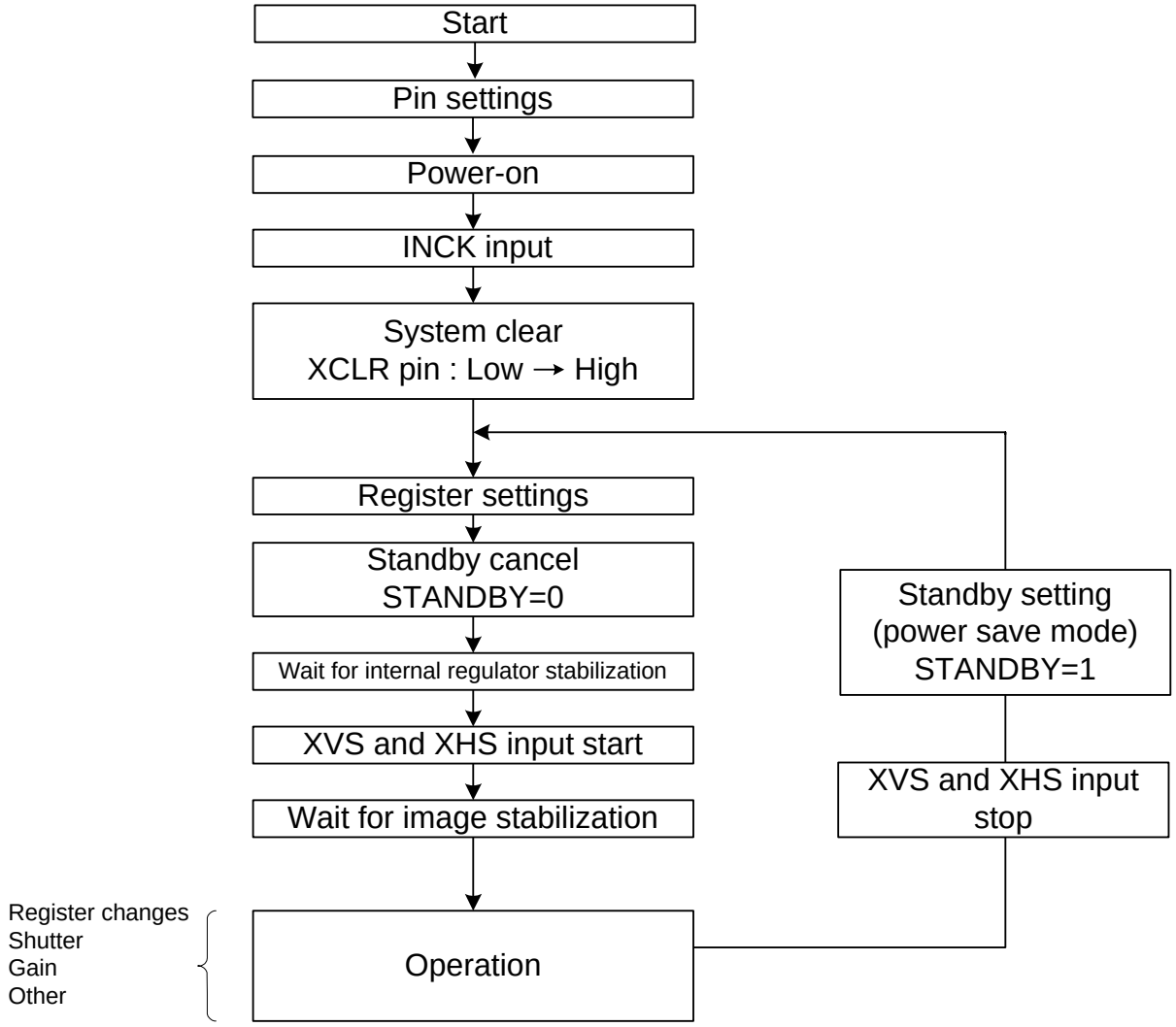
Power-off Sequence

Item	Symbol	Min.	Max.	Unit
Standby ON (communication) → LP11 mode start	T_{STB}	Until FE		—
LP00 → XCLR falling	T_{CLR}	128	—	cycle
3.3 V power shut down → 1.8 V power shut down	T4	0	—	ns
1.8 V power shut down → 1.2 V power shut down	T5	0	—	ns
Shut down time of all power supply	T6	—	200	ms

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

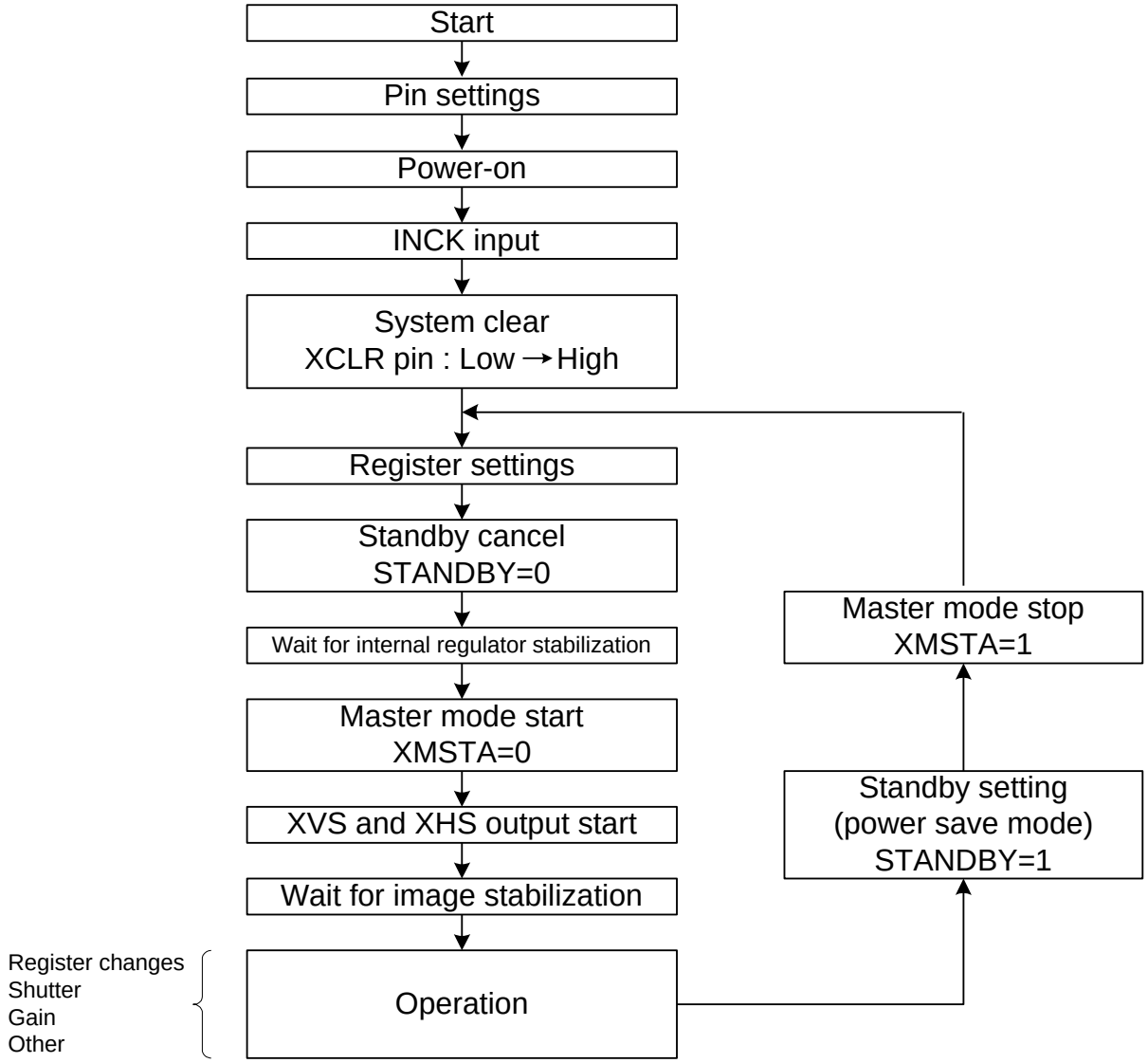
The figure below shows operating flow in sensor slave mode.
For details of "Power-on" to "Reset cancel", see the item of "Power-on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

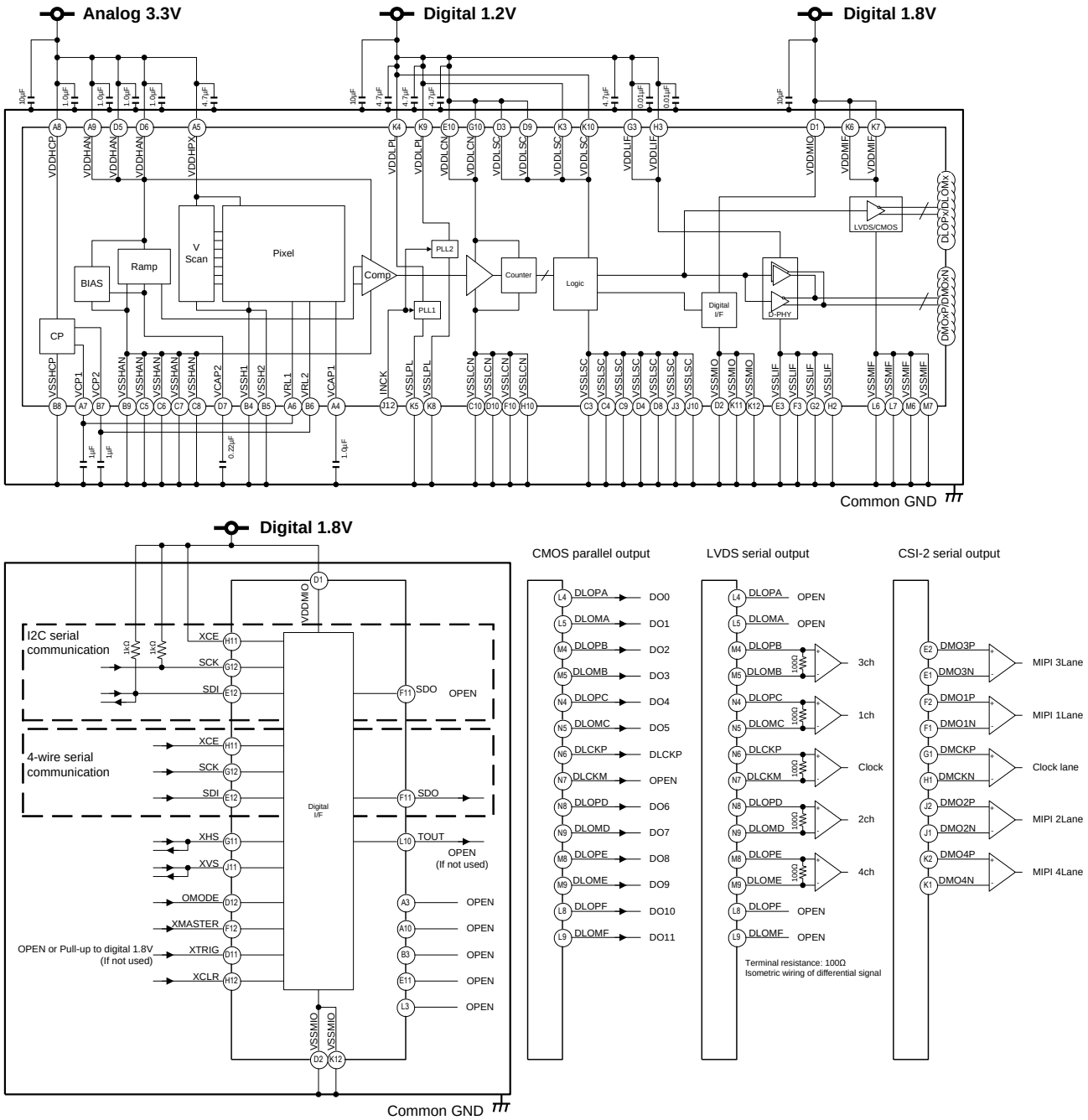
Setting Flow in Sensor Master Mode

The figure below shows operating flow in sensor master mode.
For details of "Power-on" to "Reset cancel", see the item of "Power on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
In master mode, “Master mode start” by setting register XMSTA to “0” after “Waiting for internal regulator stabilization”
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

Peripheral Circuit



Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

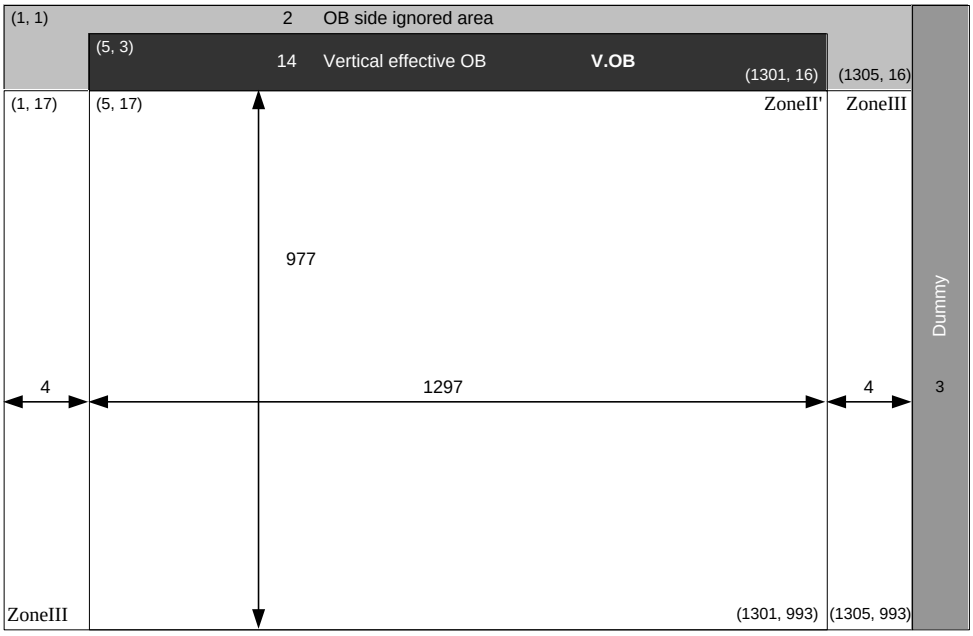
Spot Pixel Specifications

(AV_{DD} = 3.3 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, 30 frame/s, Gain: 0 dB, LCG mode)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30 % ≤ D	10	No evaluation criteria applied			1	—
White pixels in the dark	5.6 mV ≤ D	120		No evaluation criteria applied		2	1/30 s storage
Black pixels at signal saturated	D ≤ 968 mV	0	No evaluation criteria applied			3	—

Note) 1. Zone is specified based on all-pixel drive mode
2. D Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C / LCG mode)	Annual number of occurrence
5.6 mV or higher	16 pcs
10.0 mV or higher	9 pcs
24.0 mV or higher	4 pcs
50.0 mV or higher	2 pcs
72.0 mV or higher	1 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

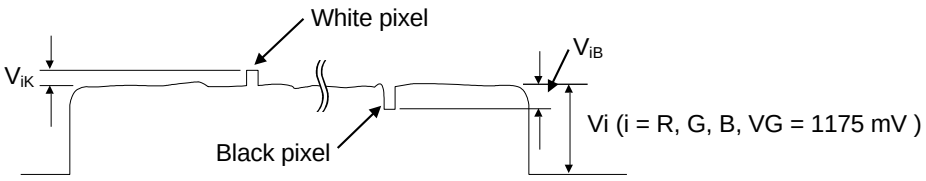
Material_No.03-0.0.8

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is 1175 mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

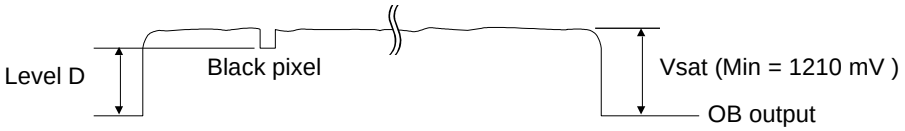
   Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of Vi) × 100 [%]



Signal output waveform of R / G / B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

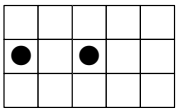
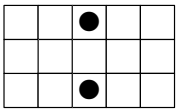


Signal output waveform of R / G / B channel

Spot Pixel Pattern Specification

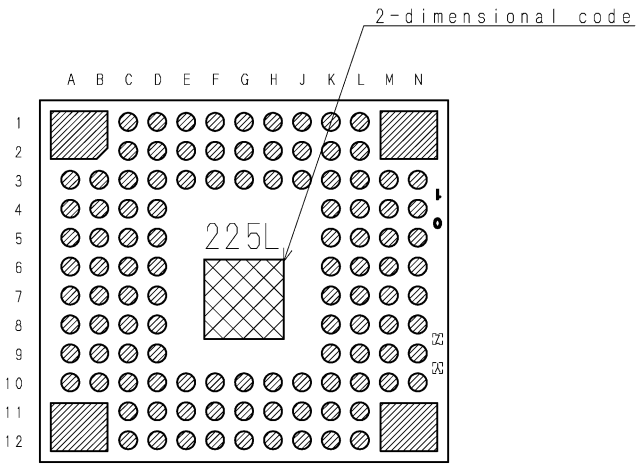
White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

No.	Pattern  It provides by color filter array described in the left.	White pixel Black pixel Bright pixel
1	 Same color	Rejected
2	 Same color	Rejected

Note) 1.”●” shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not judged to be rejected.)
2. When one or more spot pixels indicated “Rejected” is selected and removed.
3. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

Marking



Note:Following characters enter into "Y", and"Z". (No Au coat)
Y:In English upper case character, One character
Z:Number, single number

DRAWING No. AM-C225LQR(2D)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

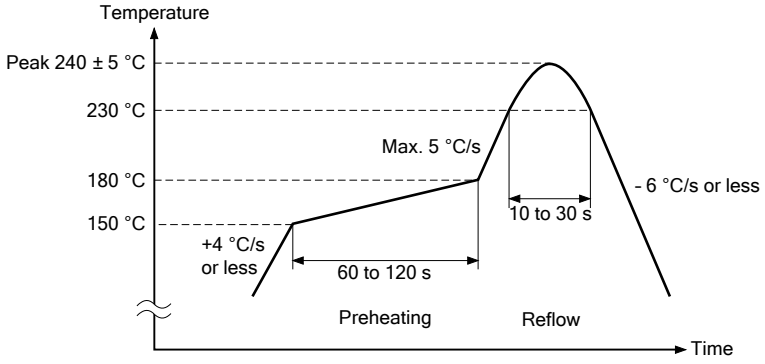
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

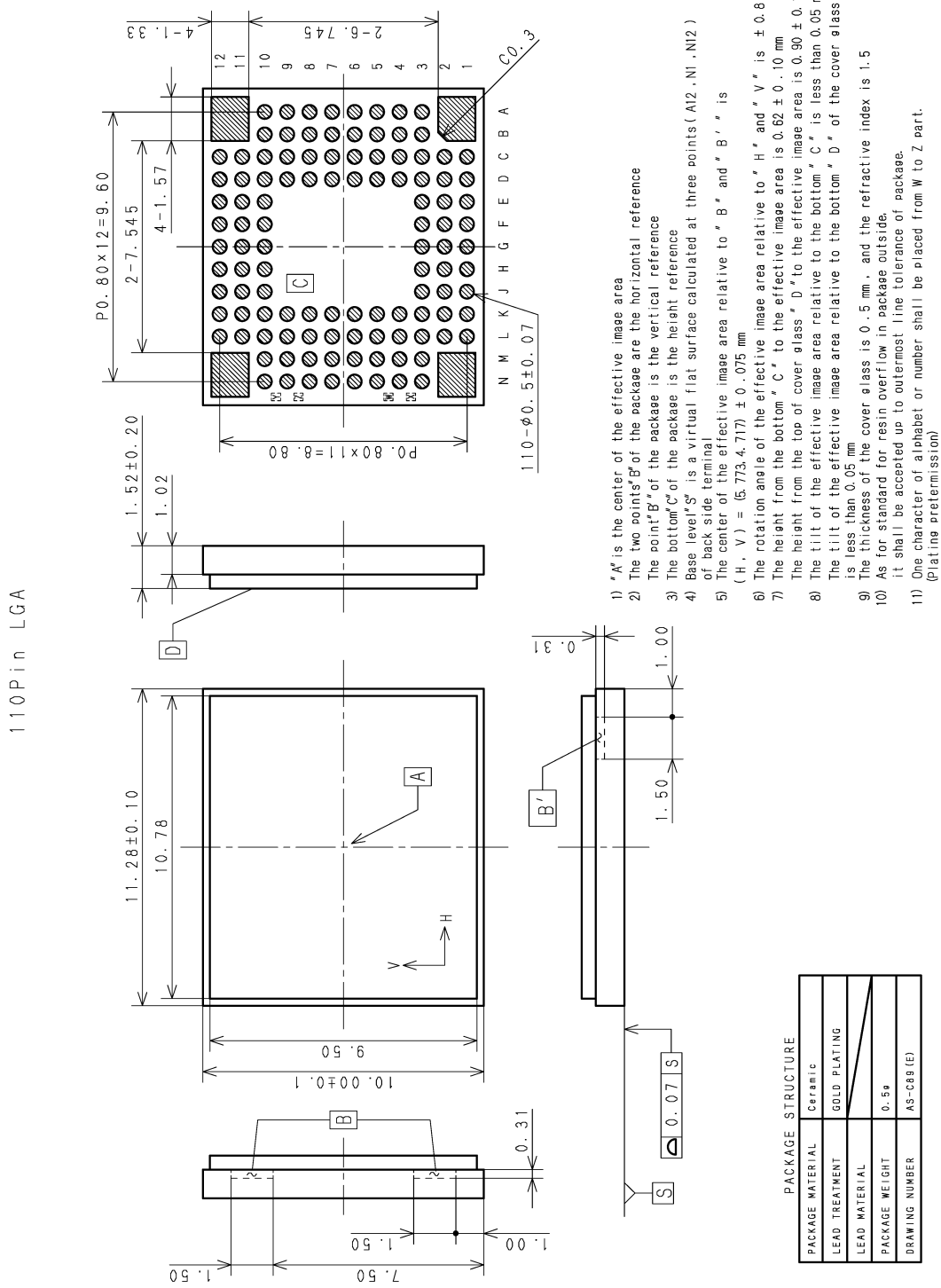
(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Package Outline

(Unit: mm)



Revision History

Date of change	Revision	Page	Contain of Change
18-Jul-14	0.1	—	First edition
18-Aug-14	0.2	23	Added the spectral sensitivity characteristics.
		24	Update the value of 1Digit.
		87 - 88	Corrected to minimum number of the register SHS (0 to 2).
		113	Added the package outline (TENTATIVE).
30-Sep-14	0.3	1	The description of WDR mode was added to the Features
		3	Updated the absolute maximum ratings; Topr, Tstg
		10 - 13	Updated pin names. About K11, change 1.2V-GND to 1.8V-GND.
		17	Addition: Added the Tr / Tf to AC characteristics of XVS / XHS in slave mode.
		22	Addition: I/O Equivalent Circuit Diagram
		24	Updated the image sensor characteristics.
		34	Addition: Added that the reflection of the gain is delayed.
		37	Addition: Initial setting register at address 16h
		42	Addition: Initial setting register at address B8h
		38 - 39,	Correction: Register bit width of VMAX and SHS1.
		71 - 73	Correction: Image drawing and drive timing in window cropping mode.
		80	Updated the stabilization time after standby released
		81, 87	Correction: Register bit width of VMAX and SHS1.
		83	Addition: Gain reflection timing
		87 - 88	Correction: Minimum setting value of SHS1.
		105	Updated pin names, decreased the capacitors.
		106	Addition: Zone definition
		113	Updated notes on handling
15-Dec-14	0.4	11	Correction pin name of B8.pin.
		15	Fill in the current comsumption value.
		24, 26	Fill in the characteristics value, add the vertical line.
		74	Add the HMAX value when CMOS parallel 60frame/s.
		102	Update the power-off sequence.
		106	Fil in the spot pixel specifications.
03-Feb-15	E15201	1	Update to official version.
		7	Update the tolerance of optical center.
		74	Correction to the setting value of FRSEL in CMOS parallel output / HD720p mode.
		77, 78	Correction to the image size in CMOS parallel and LVDS serial output / HD720p mode.
		89	Correction to the setting value of OPORTSEL in MIPI CSI-2 output.
		107	Update “Notice on White Pixels Specifications”.
		110	Update the Marking
		113	Update the package outline