# LM20323 36V, 3A 500 kHz Synchronous Buck Regulator

**Check for Samples: LM20323**

## FEATURES

- **4.5V to 36V Input Voltage Range**
- **3A Output Current, 5.2A Peak Current**
- **130 mΩ/110 mΩ Integrated Power MOSFETs**
- **93% Peak Efficiency with Synchronous Rectification**
- **1.5% Feedback Voltage Accuracy**
- **Current Mode Control, Selectable Compensation**
- **Fixed 500 kHz Switching Frequency**
- **Adjustable Output Voltage Down to 0.8V**
- **Compatible with Pre-biased Loads**
- **Programmable Soft-start with External Capacitor**
- **Precision Enable Pin with Hysteresis**
- **Integrated OVP, UVLO, PGOOD**
- **Internally Protected with Peak Current Limit, Thermal Shutdown and Restart**
- **Accurate Current Limit Minimizes Inductor Size**
- **Non-linear Current Mode Slope Compensation**
- **20-Pin HTSSOP Exposed Pad Package**

## APPLICATIONS

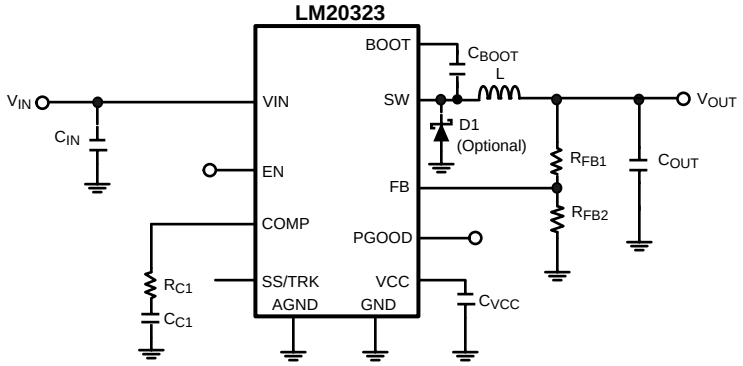
- **Simple to Design, high Efficiency Point of Load Regulation from a 4.5V to 36V Bus**
- **High Performance DSPs, FPGAs, ASICs and Microprocessors**
- **Communications Infrastructure, Automotive**

## DESCRIPTION

The LM20323 is a full featured 500kHz synchronous buck regulator capable of delivering up to 3A of load current. The current mode control loop is externally compensated with only two components, offering both high performance and ease of use. The device is optimized to work over the input voltage range of 4.5V to 36V making it well suited for high voltage systems.

The device features internal Over Voltage Protection (OVP) and Over Current Protection (OCP) circuits for increased system reliability. A precision Enable pin and integrated UVLO allows the turn-on of the device to be tightly controlled and sequenced. Startup inrush currents are limited by both an internally fixed and externally adjustable soft-start circuit. Fault detection and supply sequencing are possible with the integrated power good (PGOOD) circuit.

### Simplified Application Circuit




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## DESCRIPTION (CONTINUED)

The LM20323 is designed to work well in multi-rail power supply architectures. The output voltage of the device can be configured to track a higher voltage rail using the SS/TRK pin. If the output of the LM20323 is pre-biased at startup it will not sink current to pull the output low until the internal soft-start ramp exceeds the voltage at the feedback pin.

The LM20323 is offered in an exposed pad 20-pin HTSSOP package that can be soldered to the PCB, eliminating the need for bulky heatsinks.

### Connection Diagram

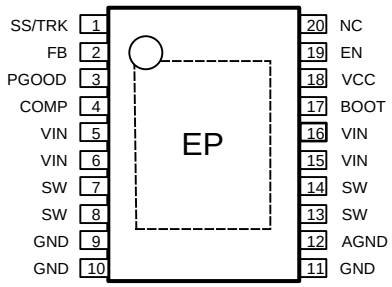



**Figure 1. 20-Pin HTSSOP, Top View**
**See PWP0020A Package**

**PIN DESCRIPTIONS**

| Pin(s) | Name | Description | Application Information |
|---|---|---|---|
| 1 | SS/TRK | Soft-Start or Tracking control input | An internal 4.5 µA current source charges an external capacitor to set the soft-start rate. The PWM can track to an external voltage ramp with a low impedance source. If left open, an internal 1 ms SS ramp is activated. |
| 2 | FB | Feedback input to the error amplifier from the regulated output | This pin is connected to the inverting input of the internal transconductance error amplifier. An 800 mV reference is internally connected to the non-inverting input of the error amplifier. |
| 3 | PGOOD | Power good output signal | Open drain output indicating the output voltage is regulating within tolerance. A pull-up resistor of 10 kΩ to 100 kΩ is recommended if this function is used. |
| 4 | COMP | Output of the internal error amplifier and input to the Pulse Width Modulator | The loop compensation network should be connected between the COMP pin and the AGND pin. |
| 5,6,15,16 | VIN | Input supply voltage | Nominal operating range: 4.5V to 36V. |
| 7,8,13,14 | SW | Switch pin | The drain terminal of the internal Synchronous Rectifier power NMOSFET and the source terminal of the internal Control power NMOSFET. |
| 9,10,11 | GND | Ground | Internal reference for the power MOSFETs. |
| 12 | AGND | Analog ground | Internal reference for the regulator control functions. |
| 17 | BOOT | Boost input for bootstrap capacitor | An internal diode from VCC to BOOT charges an external capacitor required from SW to BOOT to power the Control MOSFET gate driver. |
| 18 | VCC | Output of the high voltage linear regulator. The VCC voltage is regulated to approximately 5.5V. | VCC tracks VIN up to about 7.2V. Above VIN = 7.2V, VCC is regulated to approximately 5.5 Volts. A 0.1 µF to 1 µF ceramic decoupling capacitor is required. The VCC pin is an output only. |
| 19 | EN | Enable or UVLO input | An external voltage divider can be used to set the line undervoltage lockout threshold. If the EN pin is left unconnected, a 2 µA pull-up current source pulls the EN pin high to enable the regulator. |
| 20 | NC | No Connection | Recommend connecting this pin to GND. |
| EP | Exposed Pad | Exposed pad | Exposed metal pad on the underside of the package with a weak electrical connection to GND. Connect this pad to the PC board ground plane in order to improve heat dissipation. |


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)(2)

| | | |
|---|---|---|
| VIN to GND | | -0.3V to +38V |
| BOOT to GND | | -0.3V to +43V |
| BOOT to SW | | -0.3V to +7V |
| SW to GND | | -0.5V to +38V |
| SW to GND (Transient) | | -1.5V (< 20 ns) |
| FB, EN, SS/TRK, COMP, PGOOD to GND | | -0.3V to +6V |
| VCC to GND | | -0.3V to +8V |
| Storage Temperature | | -65°C to 150°C |
| ESD Rating | Human Body Model(3) | 2kV |

(1) Absolute Maximum Ratings indicate limits beyond witch damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor to each pin.

## Operating Ratings

| | |
|---|---|
| VIN to GND | +4.5V to +36V |
| Junction Temperature | −40°C to + 125°C |

## Electrical Characteristics

Unless otherwise stated, the following conditions apply: $V_{VIN}$ = 12V. Limits in standard type are for $T_J$ = 25°C only, limits in **bold face type** apply over the junction temperature ($T_J$) range of -40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{FB}$ | Feedback Pin Voltage | $V_{VIN}$ = 4.5V to 36V | **0.788** | 0.8 | **0.812** | V |
| $R_{HSW-DS(ON)}$ | High-Side MOSFET On-Resistance | $I_{SW}$ = 3A | | 130 | **225** | mΩ |
| $R_{LSW-DS(ON)}$ | Low-Side MOSFET On-Resistance | $I_{SW}$ = 3A | | 110 | **190** | mΩ |
| $I_Q$ | Operating Quiescent Current | $V_{VIN}$ = 4.5V to 36V | | 2.3 | **3** | mA |
| $I_{SD}$ | Shutdown Quiescent Current | $V_{EN}$ = 0V | | 150 | **180** | µA |
| $V_{UVLO}$ | VIN Under Voltage Lockout | Rising $V_{VIN}$ | **4** | 4.25 | **4.5** | V |
| $V_{UVLO(HYS)}$ | VIN Under Voltage Lockout Hysteresis | | | 350 | **450** | mV |
| $V_{VCC}$ | VCC Voltage | $I_{VCC}$ = -5 mA, $V_{EN}$ = 5V | | 5.5 | | V |
| $I_{SS}$ | Soft-Start Pin Source Current | $V_{SS}$ = 0V | **2** | 4.5 | **7** | µA |
| $V_{TRKACC}$ | Soft-Start/Track Pin Accuracy | $V_{SS}$ = 0.4V | **-10** | 5 | **15** | mV |
| $I_{BOOT}$ | BOOT Diode Leakage | $V_{BOOT}$ = 4V | | 10 | | nA |
| $V_{F-BOOT}$ | BOOT Diode Forward Voltage | $I_{BOOT}$ = -100 mA | | 0.9 | **1.1** | V |
| **Powergood** | | | | | | |
| $V_{FB(OVP)}$ | Over Voltage Protection Rising Threshold | $V_{FB(OVP)}$ / $V_{FB}$ | **107** | 110 | **112** | % |
| $V_{FB(OVP-HYS)}$ | Over Voltage Protection Hysteresis | $\Delta_{VFB(OVP)}$ / $V_{FB}$ | | 2 | **3** | % |
| $V_{FB(PG)}$ | PGOOD Threshold, $V_{OUT}$ Rising | $V_{FB(PG)}$ / $V_{FB}$ | **93** | 95 | **97** | % |
| $V_{FB(PG-HYS)}$ | PGOOD Hysteresis | $\Delta V_{FB(PG)}$ / $V_{FB}$ | | 2 | **3** | % |
| $T_{PGOOD}$ | PGOOD Delay | | | 20 | | µs |
| $I_{PGOOD(SNK)}$ | PGOOD Low Sink Current | $V_{PGOOD}$ = 0.5V | **0.6** | 1 | | mA |
| $I_{PGOOD(SRC)}$ | PGOOD High Leakage Current | $V_{PGOOD}$ = 5V | | 5 | **200** | nA |

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## Electrical Characteristics (continued)

Unless otherwise stated, the following conditions apply: $V_{VIN}$ = 12V. Limits in standard type are for $T_J$ = 25°C only, limits in **bold face type** apply over the junction temperature ($T_J$) range of -40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Oscillator** | | | | | | |
| $F_{SW1}$ | Switching Frequency | | **470** | 520 | **570** | kHz |
| $D_{MAX}$ | Maximum Duty Cycle | $I_{OUT}$ = 3A | | 70 | | % |
| **Error Amplifier** | | | | | | |
| $I_{FB}$ | Feedback Pin Bias Current | $V_{FB}$ = 1V | | 50 | | nA |
| $I_{COMP(SRC)}$ | COMP Output Source Current | $V_{FB}$ = 0V, $V_{COMP}$ = 0V | **200** | 400 | | µA |
| $I_{COMP(SNK)}$ | COMP Output Sink Current | $V_{FB}$ = 1.6V, $V_{COMP}$ = 1.6V | **200** | 350 | | µA |
| $g_m$ | Error Amplifier DC Transconductance | $I_{COMP}$ = -50 µA to +50 µA | **450** | 515 | **600** | µmho |
| $A_{VOL}$ | Error Amplifier Voltage Gain | COMP pin open | | 2000 | | V/V |
| GBW | Error Amplifier Gain-Bandwidth Product | COMP pin open | | 7 | | MHz |
| **Current Limit** | | | | | | |
| $I_{LIM}$ | Cycle By Cycle Positive Current Limit | | **4.3** | 5.2 | **6.0** | A |
| $I_{LIMNEG}$ | Cycle By Cycle Negative Current Limit | | | 2.8 | | A |
| $T_{ILIM}$ | Cycle By Cycle Current Limit Delay | | | 150 | | ns |
| **Enable** | | | | | | |
| $V_{IH_EN}$ | EN Pin Rising Threshold | | **1.2** | 1.25 | **1.3** | V |
| $V_{EN(HYS)}$ | EN Pin Hysteresis | | | 50 | | mV |
| $I_{EN}$ | EN Source Current | $V_{EN}$ = 0V, $V_{VIN}$ = 12V | | 2 | | µA |
| **Thermal Shutdown** | | | | | | |
| $T_{SD}$ | Thermal Shutdown | | | 170 | | °C |
| $T_{SD(HYS)}$ | Thermal Shutdown Hysteresis | | | 20 | | °C |
| **Thermal Resistance** | | | | | | |
| $\theta_{JC}$ | Junction to Case | | | 5.6 | | °C/W |
| $\theta_{JA}$ | Junction to Ambient(1) | 0 LFM airflow | | 27 | | °C/W |

(1) Measured on a 4 layer 2" x 2" PCB with 1 oz. copper weight inner layers and 2 oz. outer layers.


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## Typical Performance Characteristics

Unless otherwise specified: $V_{VIN}$ = 12V, $V_{OUT}$ = 3.3V, L= 5.6 µH, $C_{SS}$ = 100nF, $T_A$ = 25°C for efficiency curves, loop gain plots and waveforms, and $T_J$ = 25°C for all others.

**Efficiency vs. Load Current**

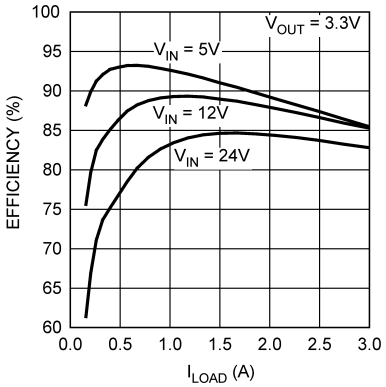



**Figure 2.**

**Error Amplifier Gain**

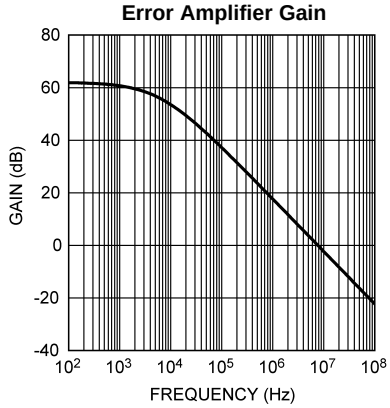



**Figure 3.**

**Error Amplifier Phase**

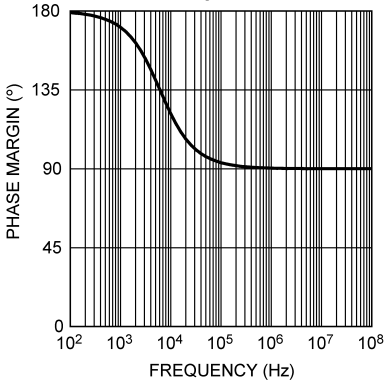



**Figure 4.**

**Line Regulation**

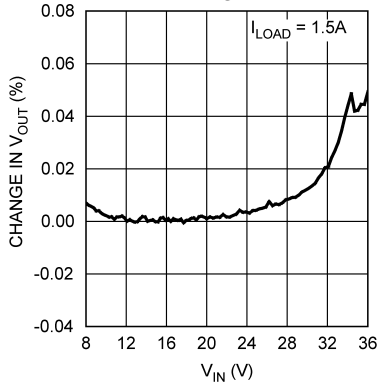



**Figure 5.**

**Load Regulation**

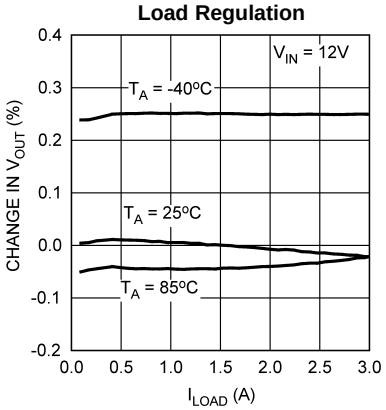



**Figure 6.**

**$V_{CC}$ vs. $V_{IN}$**

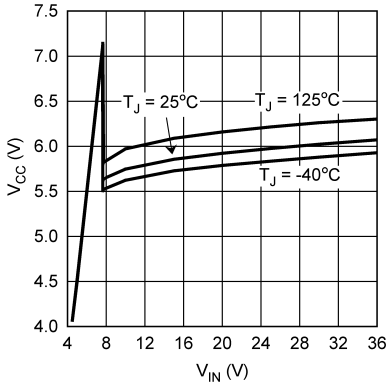



**Figure 7.**

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## Typical Performance Characteristics (continued)

Unless otherwise specified: $V_{VIN}$ = 12V, $V_{OUT}$ = 3.3V, L= 5.6 µH, $C_{SS}$ = 100nF, $T_A$ = 25°C for efficiency curves, loop gain plots and waveforms, and $T_J$ = 25°C for all others.

**Non-Switching $I_Q$ vs. $V_{IN}$**

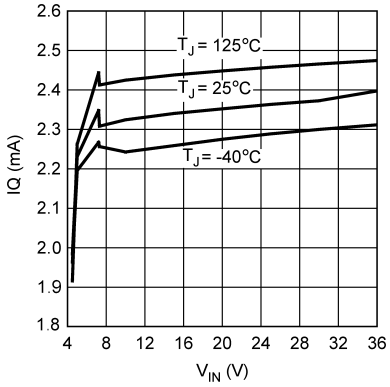



**Figure 8.**

**Shutdown $I_Q$ vs. $V_{IN}$**

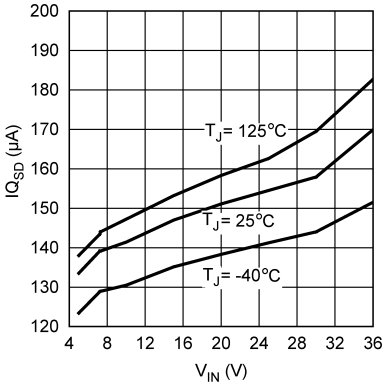



**Figure 9.**

**PGOOD Output Low Level Voltage vs. $I_{PGOOD}$**

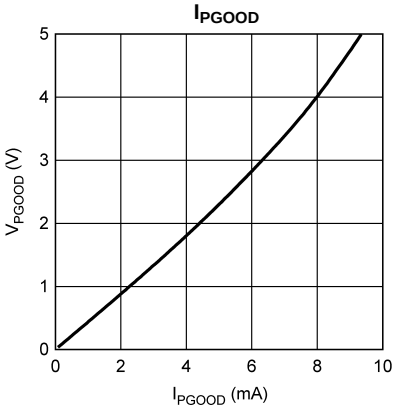



**Figure 10.**

**Enable Threshold and Hysteresis vs. Temperature**

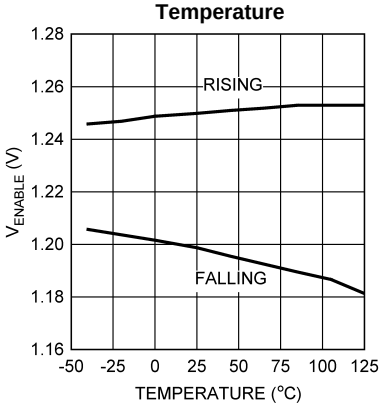



**Figure 11.**

**UVLO Threshold and Hysteresis vs. Temperature**

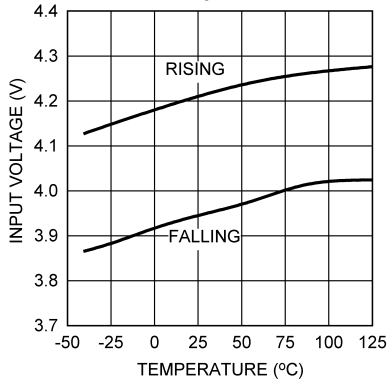



**Figure 12.**

**Enable Current vs. Temperature**

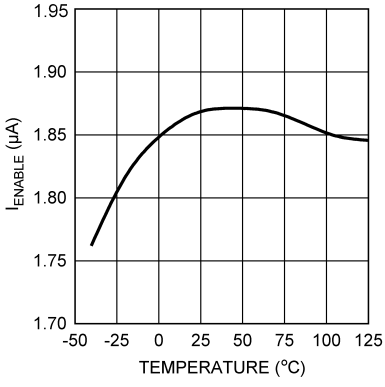



**Figure 13.**


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## Typical Performance Characteristics (continued)

Unless otherwise specified: $V_{VIN}$ = 12V, $V_{OUT}$ = 3.3V, L= 5.6 µH, $C_{SS}$ = 100nF, $T_A$ = 25°C for efficiency curves, loop gain plots and waveforms, and $T_J$ = 25°C for all others.

**Oscillator Frequency vs. $V_{IN}$**

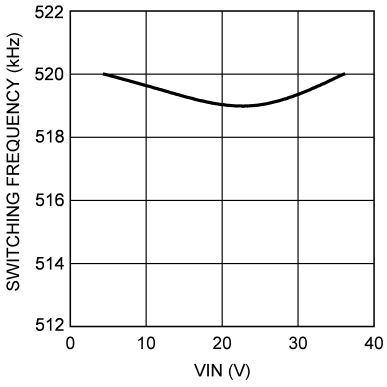



**Figure 14.**

**High-Side FET Resistance vs. Temperature**

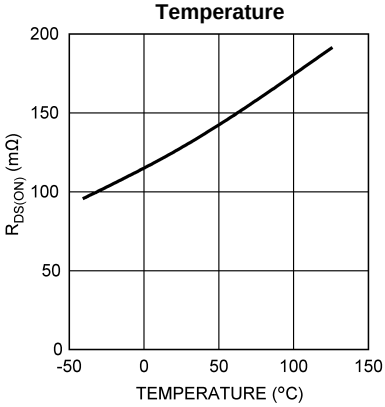



**Figure 15.**

**Load Transient Response**

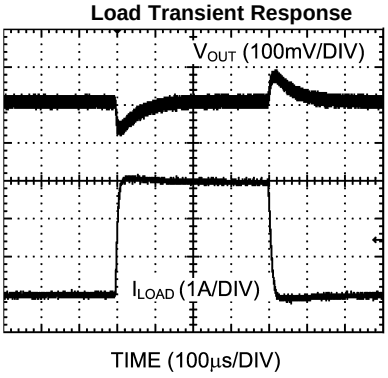



**Figure 16.**

**Low-Side FET Resistance vs. Temperature**

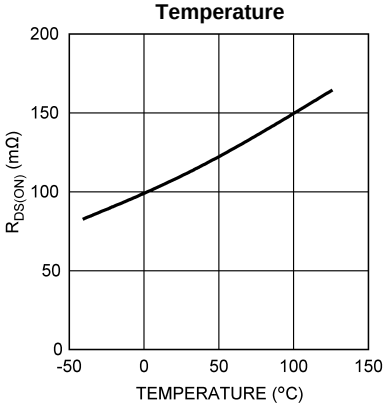



**Figure 17.**

**Peak Current Limit vs. Temperature**

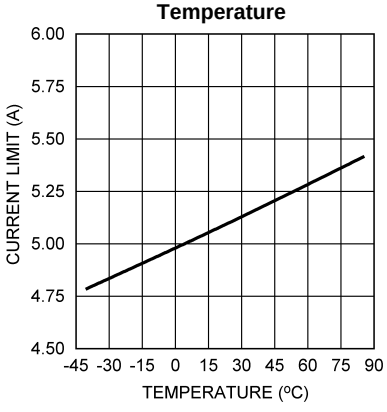



**Figure 18.**

**Startup with Prebiased Output**

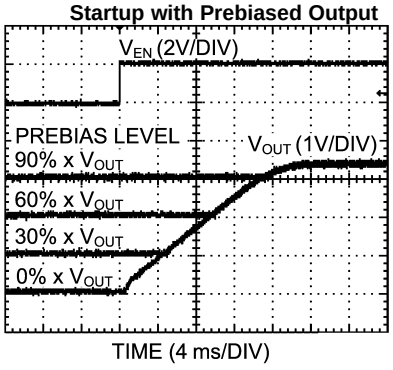


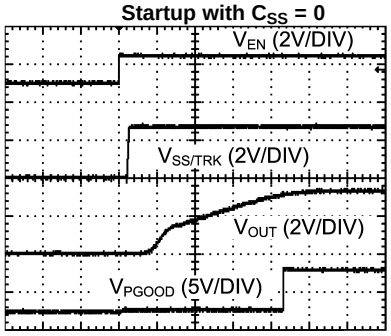

**Figure 19.**

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## Typical Performance Characteristics (continued)

Unless otherwise specified: $V_{VIN}$ = 12V, $V_{OUT}$ = 3.3V, L= 5.6 µH, $C_{SS}$ = 100nF, $T_A$ = 25°C for efficiency curves, loop gain plots and waveforms, and $T_J$ = 25°C for all others.

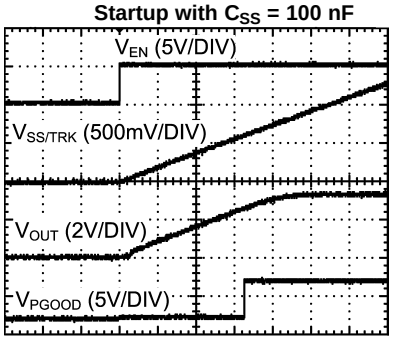
**Startup with $C_{SS}$ = 0**




TIME (200 µs/DIV)

**Figure 20.**

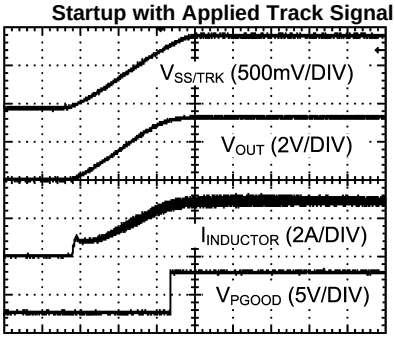
**Startup with $C_{SS}$ = 100 nF**




TIME (4 ms/DIV)

**Figure 21.**

**Startup with Applied Track Signal**

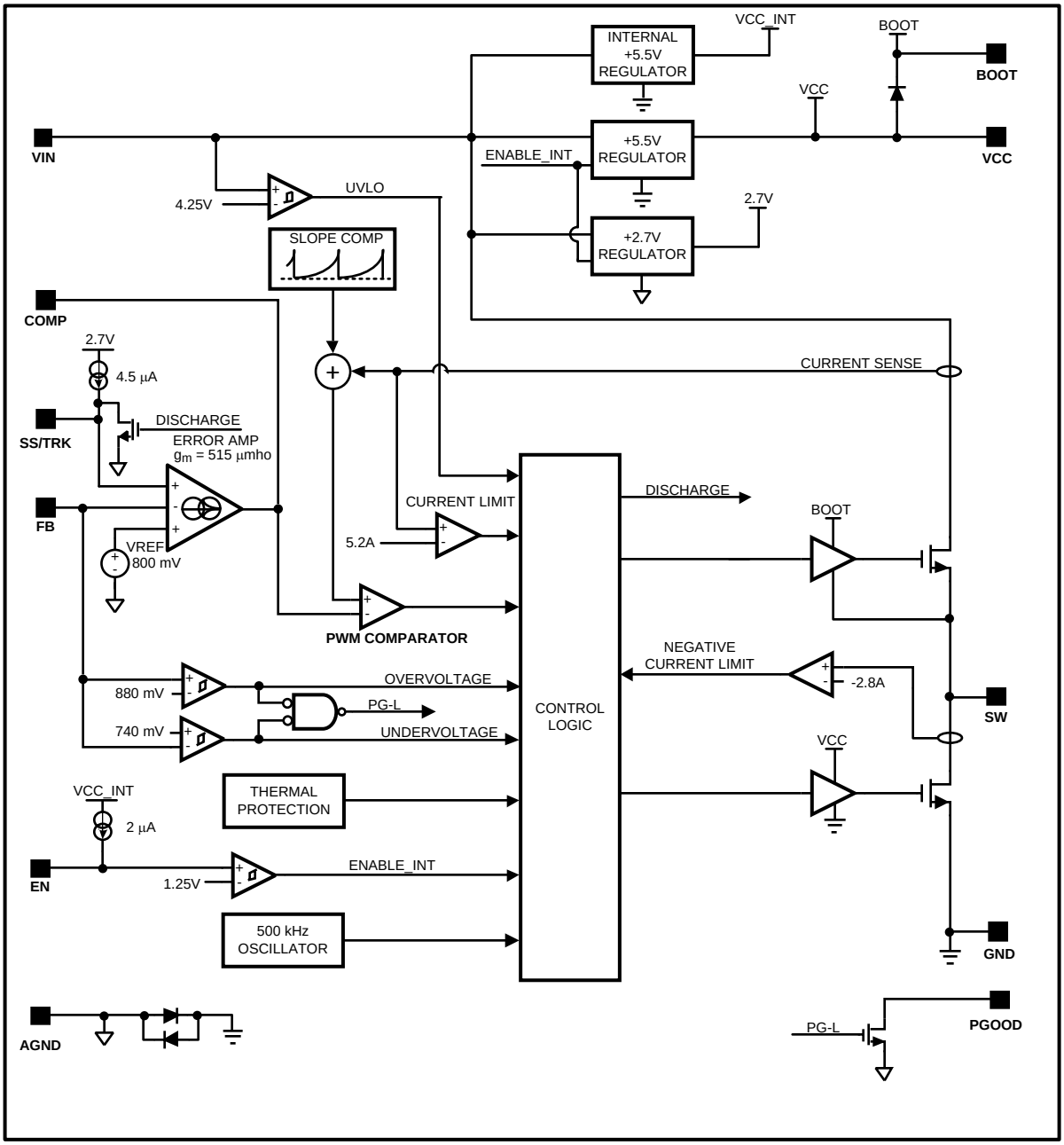



TIME (10 ms/DIV)

**Figure 22.**


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## Block Diagram



# OPERATION DESCRIPTION

## GENERAL

The LM20323 switching regulator features all of the functions necessary to implement an efficient buck regulator using a minimum number of external components. This easy to use regulator features two integrated switches and is capable of supplying up to 3A of continuous output current. The regulator utilizes peak current mode control with nonlinear slope compensation to optimize stability and transient response over the entire output voltage range. Peak current mode control also provides inherent line feed-forward, cycle-by-cycle current limiting and easy loop compensation. The 500kHz switching frequency minimizes the inductor size while keeping switching losses low allowing use of a small inductor while still achieving efficiencies as high as 93%. The precision internal voltage reference allows the output to be set as low as 0.8V. Fault protection features include: current limiting, thermal shutdown, over voltage protection, and shutdown capability. The device is available in the HTSSOP package featuring an exposed pad to aid thermal dissipation. The typical application circuit for the LM20323 is shown in Figure 23 in the design guide.

## PRECISION ENABLE

The enable (EN) pin allows the output of the device to be enabled or disabled with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.25V (typical). The EN pin has 50 mV of hysteresis and will disable the output when the enable voltage falls below 1.2V (typical). If the EN pin is not used, it should be disconnected so the internal 2 µA pull-up will default this function to the enabled condition. Since the enable pin has a precise turn-on threshold it can be used along with an external resistor divider network from $V_{IN}$ to configure the device to turn-on at a precise input voltage. The precision enable circuitry will remain active even when the device is disabled.

## PEAK CURRENT MODE CONTROL

In most cases, the peak current mode control architecture used in the LM20323 only requires two external components to achieve a stable design. The compensation can be selected to accommodate any capacitor type or value. The external compensation also allows the user to set the crossover frequency and optimize the transient performance of the device.

For duty cycles above 50% all peak current mode control buck converters require the addition of an artificial ramp to avoid sub-harmonic oscillation. This artificial linear ramp is commonly referred to as slope compensation. What makes the LM20323 unique is the amount of slope compensation will change depending on the output voltage. When operating at high output voltages the device will have more slope compensation than when operating at lower output voltages. This is accomplished in the LM20323 by using a non-linear parabolic ramp for the slope compensation. The parabolic slope compensation of the LM20323 is an improvement over the traditional linear slope compensation because it optimizes the stability of the device over the entire output voltage range.

## CURRENT LIMIT

The precise current limit enables the device to operate with smaller inductors that have lower saturation currents. When the peak inductor current reaches the current limit threshold, an over current event is triggered and the internal high-side FET turns off and the low-side FET turns on, allowing the inductor current to ramp down until the next switching cycle. For each sequential over-current event, the reference voltage is decremented and PWM pulses are skipped resulting in a current limit that does not aggressively fold back for brief over-current events, while at the same time providing frequency and voltage foldback protection during hard short circuit conditions.

## SOFT-START AND VOLTAGE TRACKING

The SS/TRK pin is a dual function pin that can be used to set the startup time or track an external voltage source. The startup or soft-start time can be adjusted by connecting a capacitor from the SS/TRK pin to ground. The soft-start feature allows the regulator output to gradually reach the steady state operating point, thus reducing stresses on the input supply and controlling startup current. If no soft-start capacitor is used the device defaults to the internal soft-start circuitry resulting in a startup time of approximately 1 ms. For applications that require a monotonic startup or utilize the PGOOD pin, an external soft-start capacitor is recommended. The SS/TRK pin can also be set to track an external voltage source. The tracking behavior can be adjusted by two external resistors connected to the SS/TRK pin as shown in Figure 28 in the design guide.


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## PRE-BIAS STARTUP CAPABILITY

The LM20323 is in a pre-biased state when it starts up with an output voltage greater than zero. This often occurs in many multi-rail applications such as when powering an FPGA, ASIC, or DSP. In these applications the output can be pre-biased through parasitic conduction paths from one supply rail to another. Even though the LM20323 is a synchronous converter, it will not pull the output low when a pre-bias condition exists. During start up the LM20323 will not sink current until the soft-start voltage exceeds the voltage on the FB pin. Since the device cannot sink current, it protects the load from damage that might otherwise occur if current is conducted through the parasitic paths of the load.

### POWER GOOD AND OVER VOLTAGE FAULT HANDLING

The LM20323 has built in under and over voltage comparators that control the power switches. Whenever there is an excursion in output voltage above the set OVP threshold, the part will terminate the present on-pulse, turn-on the low-side FET, and pull the PGOOD pin low. The low-side FET will remain on until either the FB voltage falls back into regulation or the negative current limit is triggered which in turn tri-states the FETs. If the output reaches the UVP threshold the part will continue switching and the PGOOD pin will be deasserted and go low. Typical values for the PGOOD resistor are on the order of 100 kΩ or less. To avoid false tripping during transient glitches the PGOOD pin has 20 µs of built in deglitch time to both rising and falling edges.

## UVLO

The LM20323 has an internal under-voltage lockout protection circuit that keeps the device from switching until the input voltage reaches 4.25V (typical). The UVLO threshold has 350 mV of hysteresis that keeps the device from responding to power-on glitches during start up. If desired the turn-on point of the supply can be changed by using the precision enable pin and a resistor divider network connected to $V_{IN}$ as shown in Figure 27 in the design guide.

## THERMAL PROTECTION

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the LM20323 tri-states the power FETs and resets soft-start. After the junction cools to approximately 150°C, the part starts up using the normal start up routine. This feature is provided to prevent catastrophic failures from accidental device overheating.

## Design Guide

This section walks the designer through the steps necessary to select the external components to build a fully functional power supply. As with any DC-DC converter numerous trade-offs are possible to optimize the design for efficiency, size, or performance. These will be taken into account and highlighted throughout this discussion. To facilitate component selection discussions the circuit shown in Figure 23 below may be used as a reference. Unless otherwise indicated, all formulas assume units of amps (A) for current, farads (F) for capacitance, henries (H) for inductance and volts (V) for voltages.

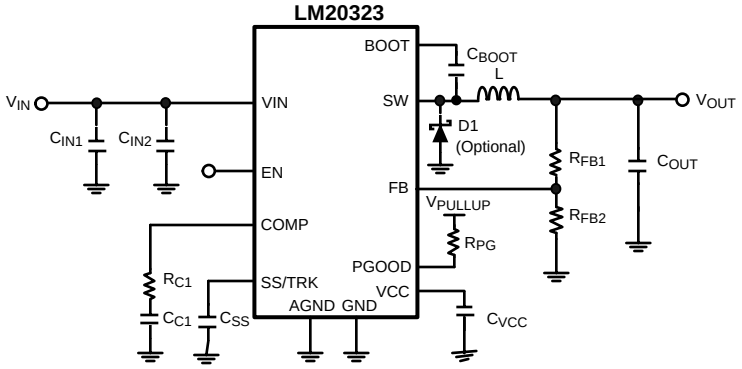



**Figure 23. Typical Application Circuit**

The first equation to calculate for any buck converter is duty-cycle. Ignoring conduction losses associated with the FETs and parasitic resistances it can be approximated by:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

## INDUCTOR SELECTION (L)

The inductor value is determined based on the operating frequency, load current, ripple current and duty cycle.

The inductor selected should have a saturation current rating greater than the peak current limit of the device. Keep in mind the specified current limit does not account for delay of the current limit comparator, therefore the current limit in the application may be higher than the specified value. To optimize the performance and prevent the device from entering current limit at maximum load, the inductance is typically selected such that the ripple current, $\Delta i_L$, is not greater than 30% of the rated output current. Figure 24 illustrates the switch and inductor ripple current waveforms. Once the input voltage, output voltage, operating frequency and desired ripple current are known, the minimum value for the inductor can be calculated by the formula shown below:

$$L_{MIN} = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta i_L \times f_{SW}} \quad (2)$$

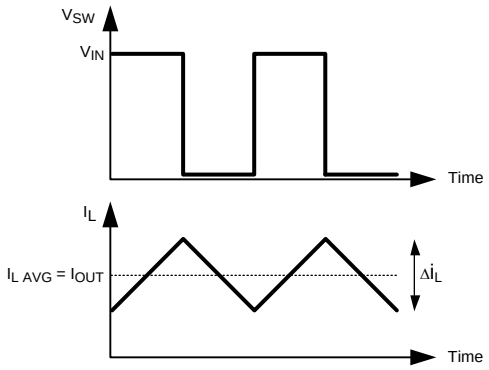



**Figure 24. Switch and Inductor Current Waveforms**

If needed, slightly smaller value inductors can be used, however, the peak inductor current, $I_{OUT} + \Delta i_L/2$, should be kept below the peak current limit of the device. In general, the inductor ripple current, $\Delta i_L$, should be more than 10% of the rated output current to provide adequate current sense information for the current mode control loop. If the ripple current in the inductor is too low, the control loop will not have sufficient current sense information and can be prone to instability.

## OUTPUT CAPACITOR SELECTION ($C_{OUT}$)

The output capacitor, $C_{OUT}$, filters the inductor ripple current and provides a source of charge for transient load conditions. A wide range of output capacitors may be used with the LM20323 that provide excellent performance. The best performance is typically obtained using ceramic, SP or OSCON type chemistries. Typical trade-offs are that the ceramic capacitor provides extremely low ESR to reduce the output ripple voltage and noise spikes, while the SP and OSCON capacitors provide a large bulk capacitance in a small volume for transient loading conditions.

When selecting the value for the output capacitor, the two performance characteristics to consider are the output voltage ripple and transient response. The output voltage ripple can be approximated by using the following formula:


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$$\Delta V_{OUT} = \Delta i_L \times \left[ R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right]$$

where

- $\Delta V_{OUT}$ (V) is the amount of peak to peak voltage ripple at the power supply output
- $R_{ESR}$ (Ω) is the series resistance of the output capacitor
- $f_{SW}$(Hz) is the switching frequency
- $C_{OUT}$ (F) is the output capacitance used in the design (3)

The amount of output ripple that can be tolerated is application specific; however a general recommendation is to keep the output ripple less than 1% of the rated output voltage. Keep in mind ceramic capacitors are sometimes preferred because they have very low ESR; however, depending on package and voltage rating of the capacitor the value of the capacitance can drop significantly with applied voltage. The output capacitor selection will also affect the output voltage droop during a load transient. The peak droop on the output voltage during a load transient is dependent on many factors; however, an approximation of the transient droop ignoring loop bandwidth can be obtained using the following equation:

$$V_{DROOP} = \Delta I_{OUTSTEP} \times R_{ESR} + \frac{L \times \Delta I_{OUTSTEP}^2}{C_{OUT} \times (V_{IN} - V_{OUT})}$$

where

- $C_{OUT}$ (F) is the minimum required output capacitance
- L (H) is the value of the inductor
- $V_{DROOP}$ (V) is the output voltage drop ignoring loop bandwidth considerations
- $\Delta I_{OUTSTEP}$ (A) is the load step change
- $R_{ESR}$ (Ω) is the output capacitor ESR
- $V_{IN}$ (V) is the input voltage
- $V_{OUT}$ (V) is the set regulator output voltage (4)

Both the tolerance and voltage coefficient of the capacitor should be examined when designing for a specific output ripple or transient droop target.

## INPUT CAPACITOR SELECTION

Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. In general it is recommended to use a ceramic capacitor for the input as they provide both a low impedance and small footprint. One important note is to use a good dielectric for the ceramic capacitor such as X5R or X7R. These provide better over temperature performance and also minimize the DC voltage derating that occurs on Y5V capacitors. The input capacitors $C_{IN1}$ and $C_{IN2}$ should be placed as close as possible to the VIN and GND pins on both sides of the device.

Non-ceramic input capacitors should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating is given by the relationship:

$$I_{IN\text{-}RMS} = I_{OUT} \sqrt{D(1 - D)} \quad (5)$$

As indicated by the RMS ripple current equation, highest requirement for RMS current rating occurs at 50% duty cycle. For this case, the RMS ripple current rating of the input capacitor should be greater than half the output current. For best performance, low ESR ceramic capacitors should be placed in parallel with higher capacitance capacitors to provide the best input filtering for the device.

## SETTING THE OUTPUT VOLTAGE ($R_{FB1}$, $R_{FB2}$)

The resistors $R_{FB1}$ and $R_{FB2}$ are selected to set the output voltage for the device. Table 1 provides suggestions for $R_{FB1}$ and $R_{FB2}$ for common output voltages.

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**Table 1. Suggested Values for $R_{FB1}$ and $R_{FB2}$**

| $R_{FB1}$(kΩ) | $R_{FB2}$(kΩ) | $V_{OUT}$ |
|---|---|---|
| short | open | 0.8 |
| 4.99 | 10 | 1.2 |
| 8.87 | 10.2 | 1.5 |
| 12.7 | 10.2 | 1.8 |
| 21.5 | 10.2 | 2.5 |
| 31.6 | 10.2 | 3.3 |
| 52.3 | 10 | 5.0 |

If different output voltages are required, $R_{FB2}$ should be selected to be between 4.99 kΩ to 49.9 kΩ and $R_{FB1}$ can be calculated using the equation below.

$$R_{FB1} = \left( \frac{V_{OUT}}{0.8} - 1 \right) \times R_{FB2} \quad (6)$$

## LOOP COMPENSATION ($R_{C1}$, $C_{C1}$)

The purpose of loop compensation is to meet static and dynamic performance requirements while maintaining adequate stability. Optimal loop compensation depends on the output capacitor, inductor, load and the device itself. Table 2 below gives values for the compensation network that will result in a stable system when using a 150 µF, 6.3V POSCAP (6TPB150MAZB) output capacitor.

**Table 2. Recommended Compensation for $C_{OUT}$ = 150 µF, $I_{OUT}$ = 3A**

| $V_{IN}$ | $V_{OUT}$ | L (µH) | $R_C$ (kΩ) | $C_{C1}$ (nF) |
|---|---|---|---|---|
| 12 | 5 | 6.8 | 45.3 | 4.7 |
| 12 | 3.3 | 5.6 | 32.4 | 4.7 |
| 12 | 2.5 | 4.7 | 30.9 | 3.3 |
| 12 | 1.5 | 3.3 | 19.1 | 3.3 |
| 12 | 1.2 | 2.2 | 21.5 | 2.2 |
| 12 | 0.8 | 1.5 | 15 | 2.2 |
| 5 | 3.3 | 2.2 | 29.4 | 2.2 |
| 5 | 2.5 | 3.3 | 37.4 | 2.2 |
| 5 | 1.5 | 2.2 | 26.7 | 2.2 |
| 5 | 1.2 | 2 | 22.1 | 2.2 |
| 5 | 0.8 | 1.5 | 15 | 2.2 |

If the desired solution differs from the table above the loop transfer function should be analyzed to optimize the loop compensation. The overall loop transfer function is the product of the power stage and the feedback network transfer functions. For stability purposes, the objective is to have a loop gain slope that is -20dB/decade from a very low frequency to beyond the crossover frequency. Figure 25 shows the transfer functions for power stage, feedback/compensation network, and the resulting compensated loop for the LM20323.


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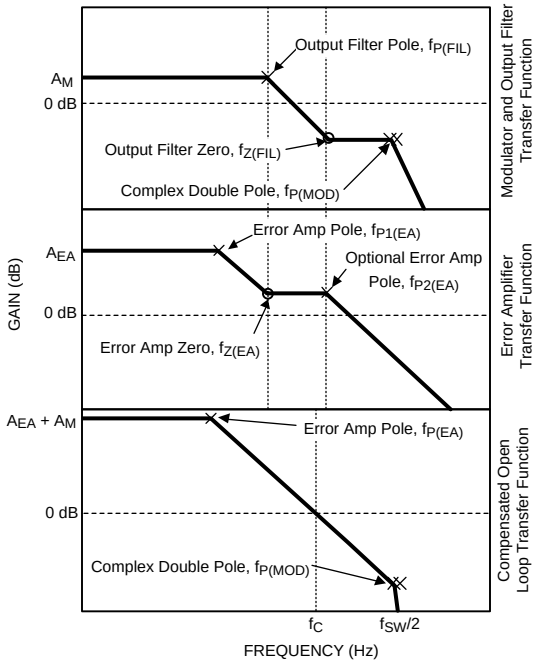



**Figure 25. LM20323 Loop Compensation**

The power stage transfer function is dictated by the modulator, output LC filter, and load; while the feedback transfer function is set by the feedback resistor ratio, error amp gain and external compensation network.

To achieve a -20dB/decade slope, the error amplifier zero, located at $f_{Z(EA)}$, should be positioned to cancel the output filter pole ($f_{P(FIL)}$).

Compensation of the LM20323 is achieved by adding an RC network as shown in Figure 26 below.

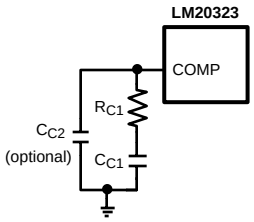



**Figure 26. Compensation Network for LM20323**

A good starting value for $C_{C1}$ for most applications is 2.2 nF. Once the value of $C_{C1}$ is chosen the value of $R_{C1}$ should be approximated using the equation below to cancel the output filter pole ($f_{P(FIL)}$) as shown in Figure 25.

$$R_{C1} = \left[ \frac{C_{C1}}{C_{OUT}} \times \left[ \frac{I_{OUT}}{V_{OUT}} + \frac{2 \times D}{f_{SW} \times L} \right] \right]^{-1} \quad (7)$$

A higher crossover frequency can be obtained, usually at the expense of phase margin, by lowering the value of $C_{C1}$ and recalculating the value of $R_{C1}$. Likewise, increasing $C_{C1}$ and recalculating $R_{C1}$ will provide additional phase margin at a lower crossover frequency. As with any attempt to compensate the LM20323 the stability of the system should be verified for desired transient droop and settling time.

For low duty cycle operation, when the on-time of the switch node is less than 200ns, an additional capacitor ($C_{C2}$) should be added from the COMP pin to AGND. The recommended value of this capacitor is 20pF. If low duty cycle jitter on the switch node is observed, the value of this capacitor can be increased to improve noise immunity; however, values much larger than 100pF will cause the pole $f_{P2(EA)}$ to move to a lower frequency degrading the loop stability.

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### BOOT CAPACITOR ($C_{BOOT}$)

The LM20323 integrates an N-channel buck switch and associated floating high voltage level shift / gate driver. This gate driver circuit works in conjunction with an internal diode and an external bootstrap capacitor. A 0.1 µF ceramic capacitor, connected with short traces between the BOOT pin and SW pin, is recommended. During the off-time of the buck switch, the SW pin voltage is approximately 0V and the bootstrap capacitor is charged from VCC through the internal bootstrap diode.

### SUB-REGULATOR BYPASS CAPACITOR ($C_{VCC}$)

The capacitor at the VCC pin provides noise filtering for the internal sub-regulator. The recommended value of $C_{VCC}$ should be no smaller than 0.1 µF and no greater than 1 µF. The capacitor should be a good quality ceramic X5R or X7R capacitor. In general, a 1 µF ceramic capacitor is recommended for most applications. The VCC regulator should not be used for other functions since it isn't protected against short circuit.

### SETTING THE START UP TIME ($C_{SS}$)

The addition of a capacitor connected from the SS pin to ground sets the time at which the output voltage will reach the final regulated value. Larger values for $C_{SS}$ will result in longer start up times. Table 3, shown below provides a list of soft start capacitors and the corresponding typical start up times.

**Table 3. Start Up Times for Different Soft-Start Capacitors**

| Start Up Time (ms) | $C_{SS}$ (nF) |
|---|---|
| 1 | none |
| 5 | 33 |
| 10 | 68 |
| 15 | 100 |
| 20 | 120 |

If different start up times are needed the equation shown below can be used to calculate the start up time.

$$t_{SS} = \frac{0.8V \times C_{SS}}{I_{SS}} \quad (8)$$

As shown above, the start up time is influenced by the value of the soft-start capacitor $C_{SS}$ and the 4.5 µA soft-start pin current $I_{SS}$.

While the soft-start capacitor can be sized to meet many start up requirements, there are limitations to its size. The soft-start time can never be faster than 1 ms due to the internal default 1 ms start up time. When the device is enabled there is an approximate time interval of 50 µs when the soft-start capacitor will be discharged just prior to the soft-start ramp. If the enable pin is rapidly pulsed or the soft-start capacitor is large there may not be enough time for $C_{SS}$ to completely discharge resulting in start up times less than predicted. To aid in discharging of soft-start capacitor during long disable periods an external 1MΩ resistor from SS/TRK to ground can be used without greatly affecting the start up time.

### USING PRECISION ENABLE AND POWER GOOD

The precision enable (EN) and power good (PGOOD) pins of the LM20323 can be used to address many sequencing requirements. The turn-on of the LM20323 can be controlled with the precision enable pin by using two external resistors as shown in Figure 27 .

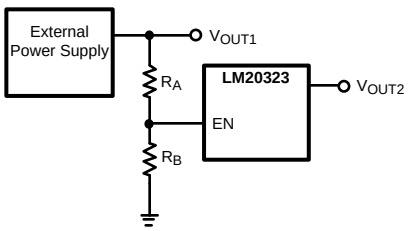



**Figure 27. Sequencing LM20323 with Precision Enable**


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The value for resistor $R_B$ can be selected by the user to control the current through the divider. Typically this resistor will be selected to be between 1 kΩ and 49.9 kΩ. Once the value for $R_B$ is chosen the resistor $R_A$ can be solved using the equation below to set the desired turn-on voltage.

$$R_A = \left( \frac{V_{TO}}{V_{IH_EN}} - 1 \right) \times R_B \quad (9)$$

When designing for a specific turn-on threshold ($V_{TO}$) the tolerance on the input supply, enable threshold ($V_{IH_EN}$), and external resistors need to be considered to ensure proper turn-on of the device.

The LM20323 features an open drain power good (PGOOD) pin to sequence external supplies or loads and to provide fault detection. This pin requires an external resistor ($R_{PG}$) to pull PGOOD high when the output is within the PGOOD tolerance window. Typical values for this resistor range from 10 kΩ to 100 kΩ.

## TRACKING AN EXTERNAL SUPPLY

By using a properly chosen resistor divider network connected to the SS/TRK pin, as shown in Figure 28, the output of the LM20323 can be configured to track an external voltage source to obtain a simultaneous or ratiometric start up.

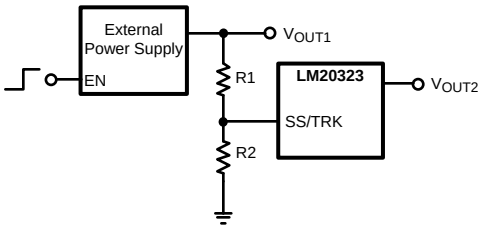



**Figure 28. Tracking an External Supply**

Since the soft-start charging current $I_{SS}$ is always present on the SS/TRK pin, the size of R2 should be less than 10 kΩ to minimize the errors in the tracking output. Once a value for R2 is selected the value for R1 can be calculated using appropriate equation in Figure 29, to give the desired start up. Figure 28 shows two common start up sequences; the top waveform shows a simultaneous start up while the waveform at the bottom illustrates a ratiometric start up.

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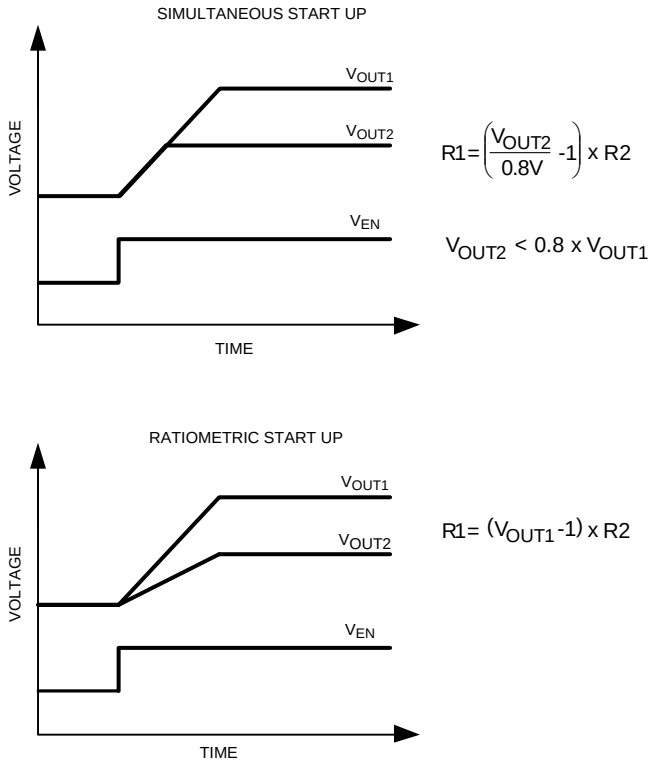



**Figure 29. Common Start Up Sequences**

A simultaneous start up is preferred when powering most FPGAs, DSPs, or other microprocessors. In these systems the higher voltage, $V_{OUT1}$, usually powers the I/O, and the lower voltage, $V_{OUT2}$, powers the core. A simultaneous start up provides a more robust power up for these applications since it avoids turning on any parasitic conduction paths that may exist between the core and the I/O pins of the processor.

The second most common power on behavior is known as a ratiometric start up. This start up is preferred in applications where both supplies need to be at the final value at the same time.

Similar to the soft-start function, the fastest start up possible is 1ms regardless of the rise time of the tracking voltage. When using the track feature the final voltage seen by the SS/TRACK pin should exceed 1V to provide sufficient overdrive and transient immunity.

## BENEFIT OF AN EXTERNAL SCHOTTKY

The LM20323 employs a 40ns dead time between conduction of the control and synchronous FETs in order to avoid the situation where both FETs simultaneously conduct, causing shoot-through current. During the dead time, the body diode of the synchronous FET acts as a free-wheeling diode and conducts the inductor current. The structure of the high voltage DMOS is optimized for high breakdown voltage, but this typically leads to inefficient body diode conduction due to the reverse recovery charge. The loss associated with the reverse recovery of the body diode of the synchronous FET manifests itself as a loss proportional to load current and switching frequency. The additional efficiency loss becomes apparent at higher input voltages and switching frequencies. One simple solution is to use a small 1A external Schottky diode between SW and GND as shown in Figure 34. The external Schottky diode effectively conducts all inductor current during the dead time, minimizing the current passing through the synchronous MOSFET body diode and eliminating reverse recovery losses.


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The external Schottky conducts currents for a very small portion of the switching cycle, therefore the average current is low. An external Schottky rated for 1A will improve efficiency by several percent in some applications. A Schottky rated at a higher current will not significantly improve efficiency and may be worse due to the increased reverse capacitance. The forward voltage of the synchronous MOSFET body diode is approximately 700 mV, therefore an external Schottky with a forward voltage less than or equal to 700 mV should be selected to ensure the majority of the dead time current is carried by the Schottky.

## THERMAL CONSIDERATIONS

The thermal characteristics of the LM20323 are specified using the parameter $\theta_{JA}$, which relates the junction temperature to the ambient temperature. Although the value of $\theta_{JA}$ is dependant on many variables, it still can be used to approximate the operating junction temperature of the device.

To obtain an estimate of the device junction temperature, one may use the following relationship:

$$T_J = P_D \times \theta_{JA} + T_A \quad (10)$$

and

$$P_D = P_{IN} \times (1 - \text{Efficiency}) - 1.1 \times (I_{OUT})^2 \times DCR$$

where

- $T_J$ is the junction temperature in °C
- $P_{IN}$ is the input power in Watts ($P_{IN} = V_{IN} \times I_{IN}$)
- $\theta_{JA}$ is the junction to ambient thermal resistance for the LM20323
- $T_A$ is the ambient temperature in °C
- $I_{OUT}$ is the output load current
- DCR is the inductor series resistance (11)

It is important to always keep the operating junction temperature ($T_J$) below 125°C for reliable operation. If the junction temperature exceeds 170°C the device will cycle in and out of thermal shutdown. If thermal shutdown occurs it is a sign of inadequate heatsinking or excessive power dissipation in the device.

Figure 30 and Figure 31 can be used as a guide to avoid exceeding the maximum junction temperature of 125°C provided an external 1A Schottky diode, such as Central Semiconductor's CMMSH1-40-NST, is used to improve reverse recovery losses.

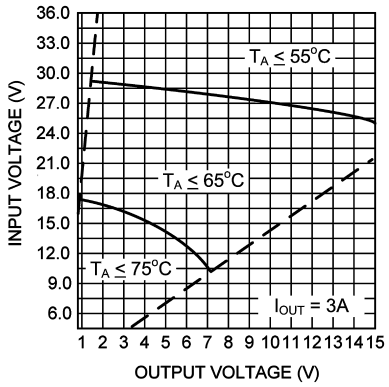



**Figure 30. Safe Thermal Operating Areas ($I_{OUT}$ = 3A)**

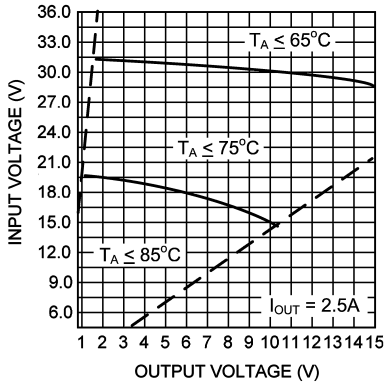



**Figure 31. Safe Thermal Operating Areas ($I_{OUT}$ = 2.5A)**

The dashed lines in the figures above show an approximation of the minimum and maximum duty cycle limitations; while, the solid lines define areas of operation for a given ambient temperature. This data for the figure was derived assuming the device is operating at 3A continuous output current on a 4 layer PCB with an copper area greater than 4 square inches exhibiting a thermal characteristic less than 27 °C/W. Since the internal losses are dominated by the FETs a slight reduction in current by 500mA allows for much larger regions of operation, as shown in Figure 31.

Figure 32, shown below, provides a better approximation of the $\theta_{JA}$ for a given PCB copper area. The PCB used in this test consisted of 4 layers: 1oz. copper was used for the internal layers while the external layers were plated to 2oz. copper weight. To provide an optimal thermal connection, a 5 x 4 array of 12 mil thermal vias located under the thermal pad was used to connect the 4 layers.

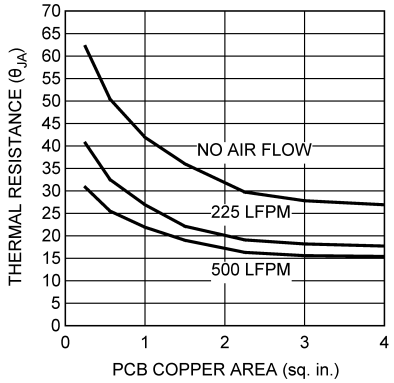



**Figure 32. Thermal Resistance vs PCB Area (4 Layer Board)**

## PCB LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability.

Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched at high slew rates. The first loop starts from the input capacitor, to the regulator VIN pin, to the regulator SW pin, to the inductor then out to the output capacitor and load. The second loop starts from the output capacitor ground, to the regulator GND pins, to the inductor and then out to the load (see Figure 33). To minimize both loop areas the input capacitor should be placed as close as possible to the VIN pin. Grounding for both the input and output capacitor should consist of a small localized top side plane that connects to GND and the exposed pad (EP). The inductor should be placed as close as possible to the SW pin and output capacitor.


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2. Minimize the copper area of the switch node. Since the LM20323 has the SW pins on opposite sides of the package it is recommended that the SW pins should be connected with a trace that runs around the package. The inductor should be placed at an equal distance from the SW pins using 100 mil wide traces to minimize capacitive and conductive losses.

3. Have a single point ground for all device grounds located under the EP. The ground connections for the compensation, feedback, and soft-start components should be connected together then routed to the EP pin of the device. The AGND pin should connect to GND under the EP. If not properly handled poor grounding can result in degraded load regulation or erratic switching behavior.

4. Minimize trace length to the FB pin. Since the feedback node can be high impedance the trace from the output resistor divider to FB pin should be as short as possible. This is most important when high value resistors are used to set the output voltage. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.

5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. Voltage accuracy at the load is important so make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

6. Provide adequate device heatsinking. For most 3A designs a four layer board is recommended. Use as many vias as is possible to connect the EP to the power plane heatsink. For best results use a 5x4 via array with a minimum via diameter of 12 mils. "Via tenting" with the solder mask may be necessary to prevent wicking of the solder paste applied to the EP. See the THERMAL CONSIDERATIONS section to ensure enough copper heatsinking area is used to keep the junction temperature below 125°C.

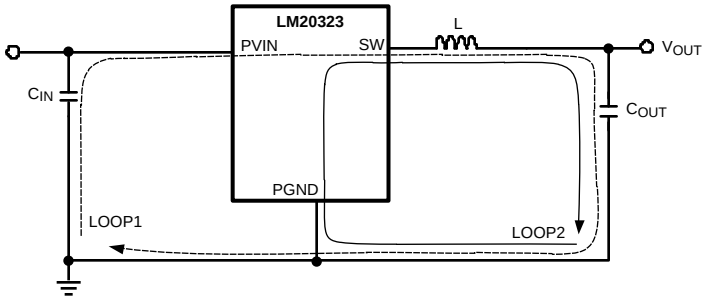



**Figure 33. Schematic of LM20323 Highlighting Layout Sensitive Nodes**

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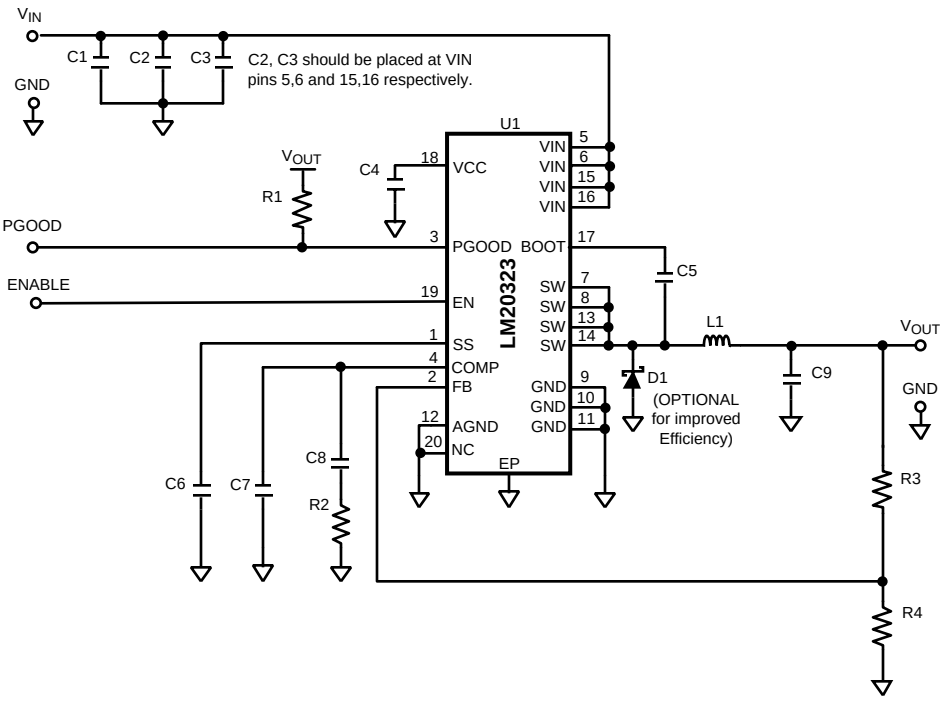



**Figure 34. Typical Application Schematic**

**Table 4. Bill of Materials ($V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 3A)**

| ID | Qty | Part Number | Size | Description | Vendor |
|---|---|---|---|---|---|
| U1 | 1 | LM20323MH | HTSSOP | IC, Switching Regulator | TI |
| C1 | 1 | C3225X5R1E226M | 1210 | 22µF, X5R, 25V, 20% | TDK |
| C2, C3 | 2 | GRM21BR61E475KA12L | 0805 | 4.7µF, X5R, 25V, 10% | MuRata |
| C5, C6 | 1 | C1608X7R1H104K | 0603 | 100nF, X7R, 50V, 10% | TDK |
| C4 | 1 | C1608X5R1A105K | 0603 | 1µF, X7R, 10V, 10% | TDK |
| C7 | 1 | C1608C0G1H100J | 0603 | 10pF, C0G, 50V, 5% | TDK |
| C8 | 1 | C1608C0G1H102J | 0603 | 1nF, C0G, 50V, 5% | TDK |
| C9 | 1 | 6TPB150MAZB | B | 150µF,POSCAP, 6.3V, 20% | Sanyo |
| D1 | 1 | CMMSH1-40-NST | SOD123 | Vr = 40V, Io = 1A, Vf = 0.55V | Central Semiconductor |
| L1 | 1 | IHLP4040DZER5R6M01 | IHLP4040 | 5.6µH, 0.018 Ohms, 16A | Vishay |
| R1, R4 | 2 | CRCW06031002F | 0603 | 10kΩ, 1% | Vishay |
| R2 | 1 | CRCW06034992F | 0603 | 49.9kΩ, 1% | Vishay |
| R3 | 1 | CRCW06033092F | 0603 | 30.9kΩ, 1% | Vishay |


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## REVISION HISTORY

| Changes from Revision B (April 2013) to Revision C | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 22 |

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM20323MH/NOPB | Active | Production | HTSSOP (PWP) \| 20 | 73 \| TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 20323MH |
| LM20323MH/NOPB.A | Active | Production | HTSSOP (PWP) \| 20 | 73 \| TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 20323MH |
| LM20323MHE/NOPB | Active | Production | HTSSOP (PWP) \| 20 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 20323MH |
| LM20323MHE/NOPB.A | Active | Production | HTSSOP (PWP) \| 20 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 20323MH |
| LM20323MHX/NOPB | Active | Production | HTSSOP (PWP) \| 20 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 20323MH |
| LM20323MHX/NOPB.A | Active | Production | HTSSOP (PWP) \| 20 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 20323MH |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

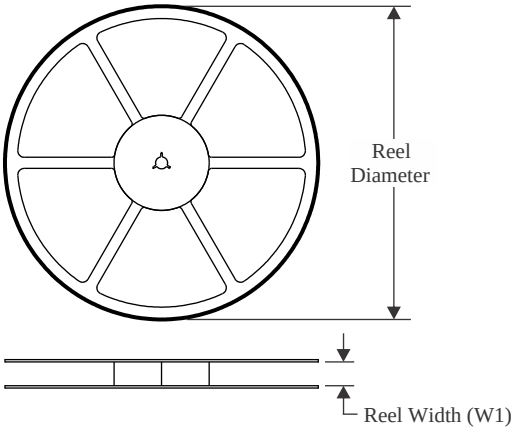
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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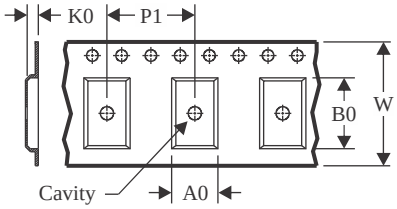
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

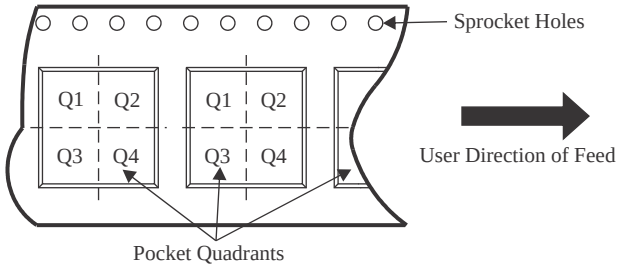



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

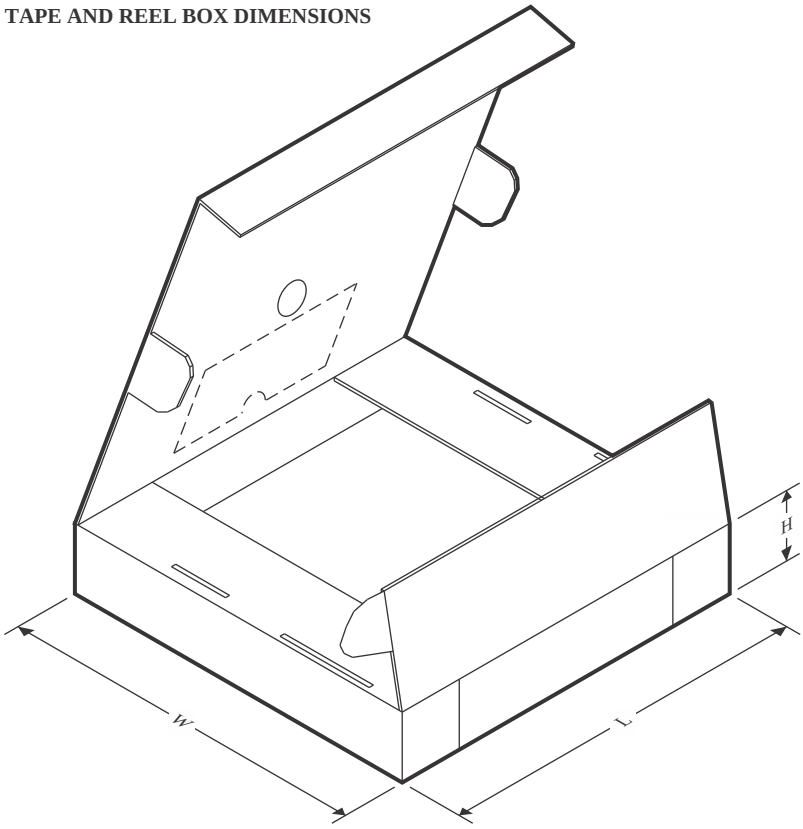
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM20323MHE/NOPB | HTSSOP | PWP | 20 | 250 | 178.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| LM20323MHX/NOPB | HTSSOP | PWP | 20 | 2500 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

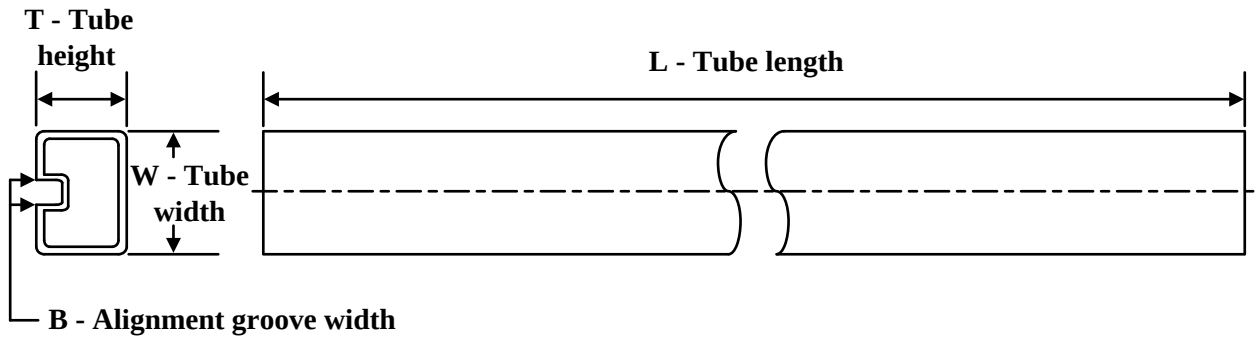
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

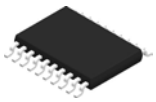
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM20323MHE/NOPB | HTSSOP | PWP | 20 | 250 | 210.0 | 185.0 | 35.0 |
| LM20323MHX/NOPB | HTSSOP | PWP | 20 | 2500 | 367.0 | 367.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM20323MH/NOPB | PWP | HTSSOP | 20 | 73 | 495 | 8 | 2514.6 | 4.06 |
| LM20323MH/NOPB.A | PWP | HTSSOP | 20 | 73 | 495 | 8 | 2514.6 | 4.06 |

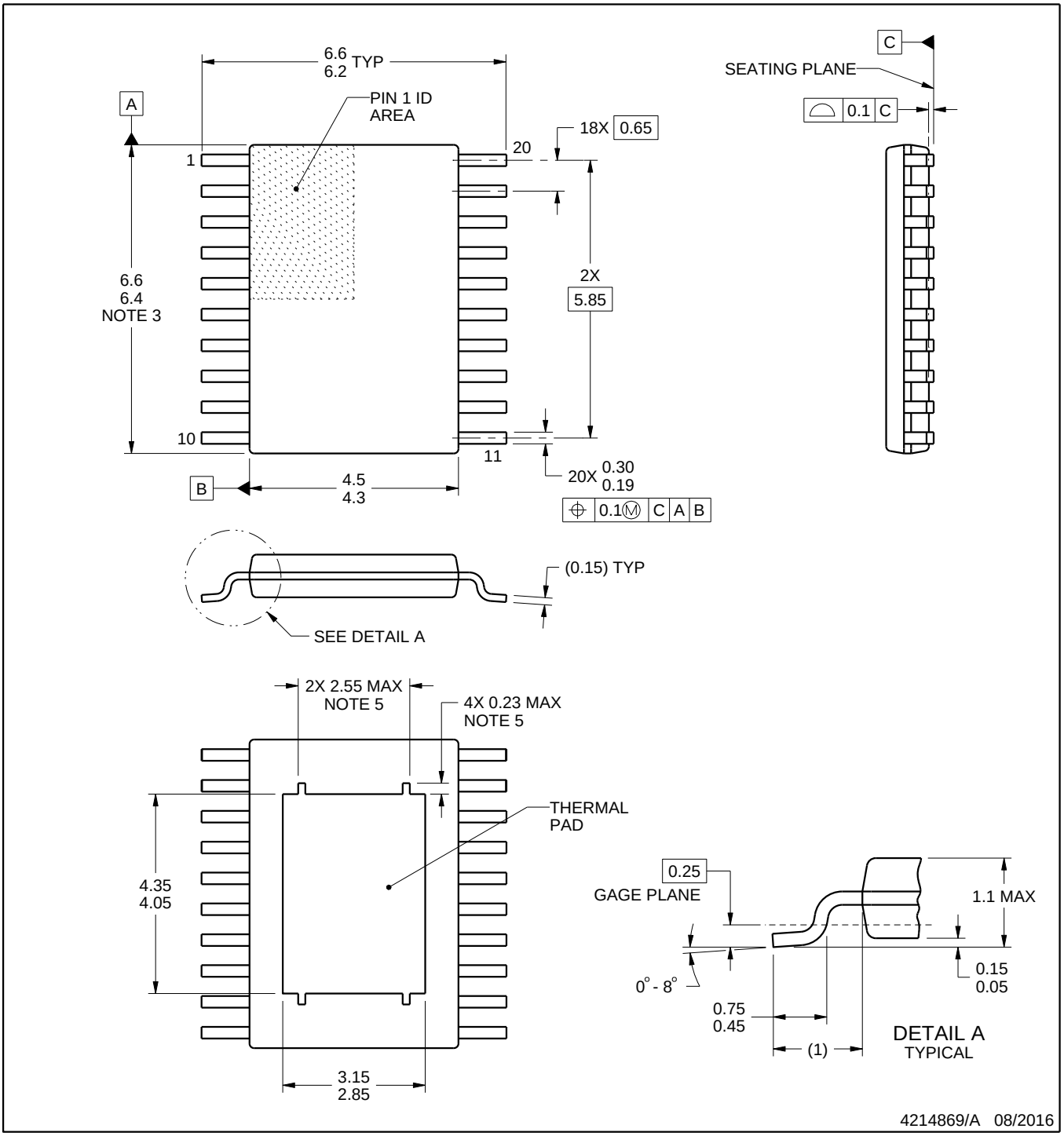


# PACKAGE OUTLINE

## PWP0020A

## PowerPAD™ TSSOP - 1.1 mm max height

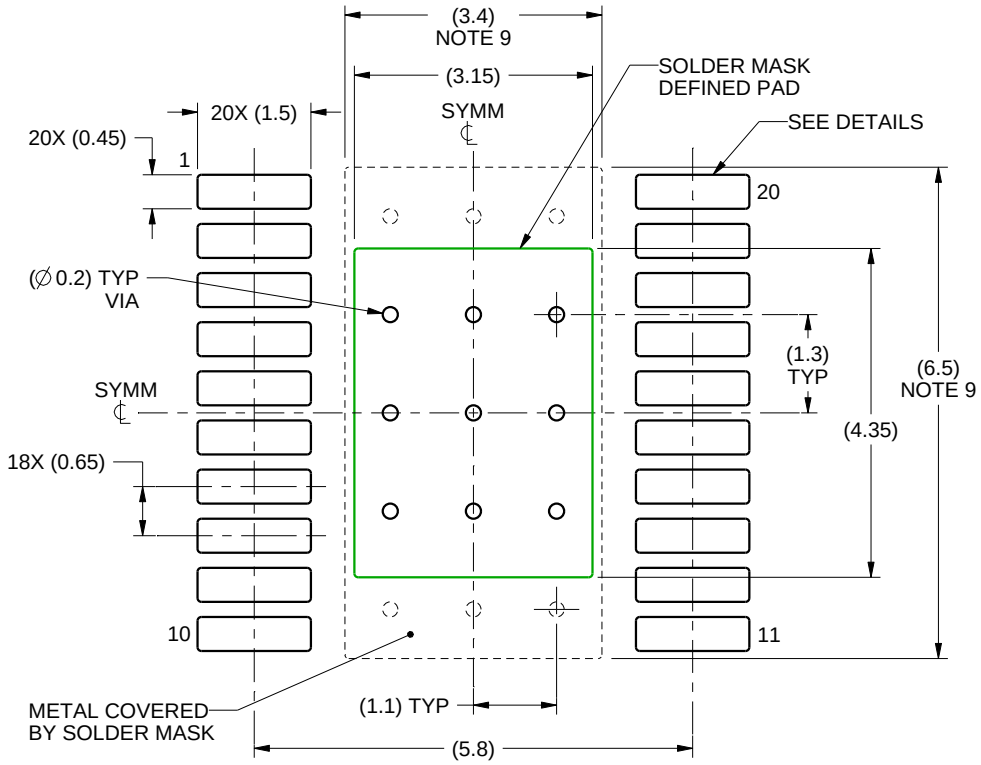
PLASTIC SMALL OUTLINE



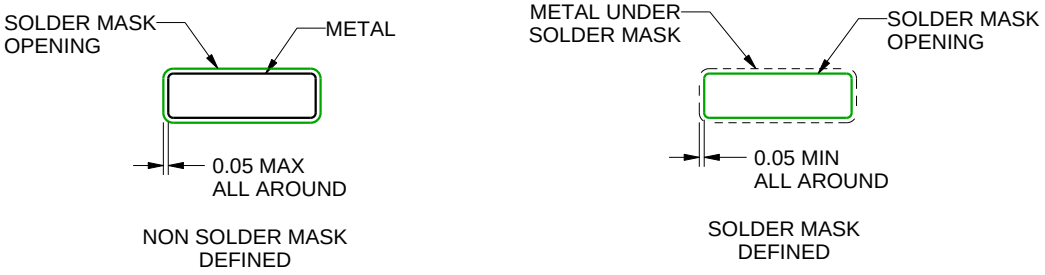

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.




LAND PATTERN EXAMPLE
SCALE:10X

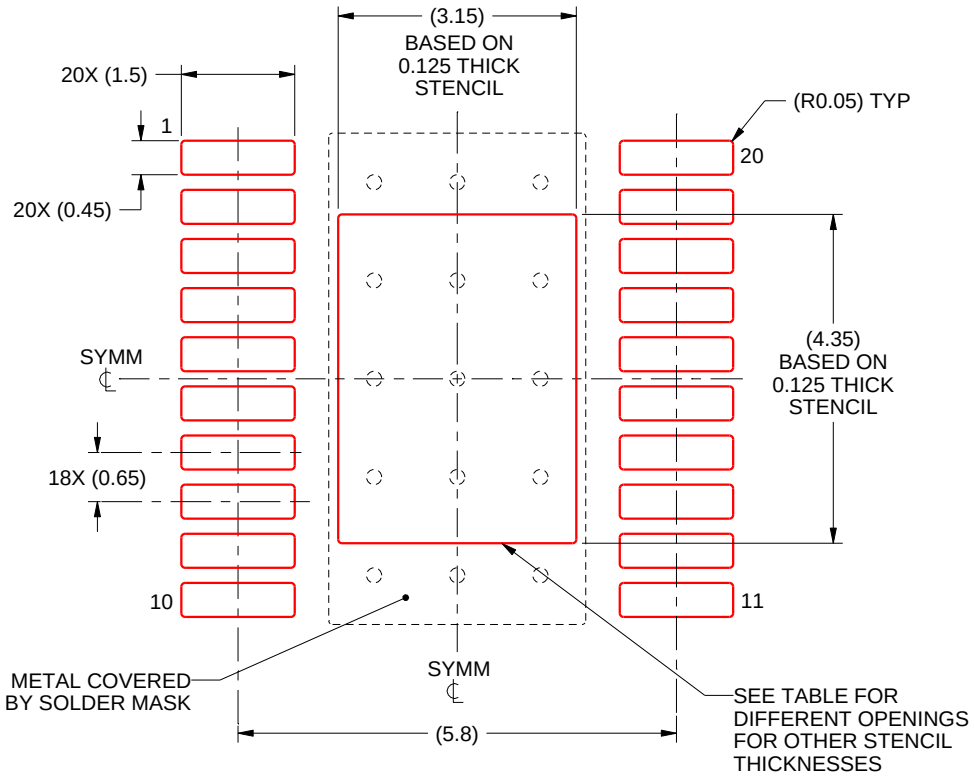



SOLDER MASK DETAILS
PADS 1-20

4214869/A 08/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.52 X 4.86 |
| 0.125 | 3.15 X 4.35 (SHOWN) |
| 0.15 | 2.88 X 3.97 |
| 0.175 | 2.66 X 3.68 |

4214869/A 08/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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