LM723QML Voltage Regulator

Check for Samples: LM723QML

FEATURES

- **150 mA Output Current Without External Pass Transistor**
- **Output Currents in Excess of 10A Possible by Adding External Transistors**
- **Input Voltage 40V Max**
- **Output Voltage Adjustable from 2V to 37V**
- **Can be Used as Either a Linear or a Switching Regulator**

DESCRIPTION

The LM723 is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

The LM723 is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

Connection Diagram

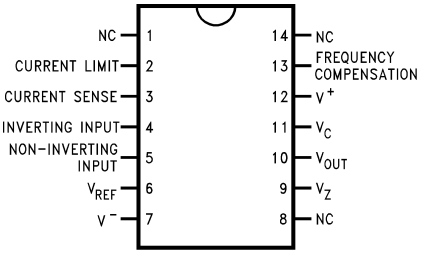
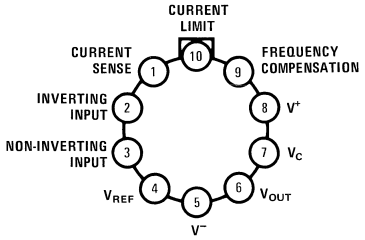


Figure 1. Dual-In-Line Package (Top View)
See Package J0014A



Note: Pin 5 connected to case.

Figure 2. Metal Can Package (Top View)
See Package LME0010C

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2005–2013, Texas Instruments Incorporated

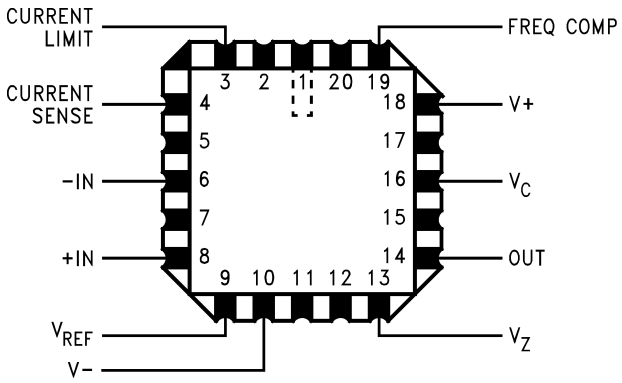
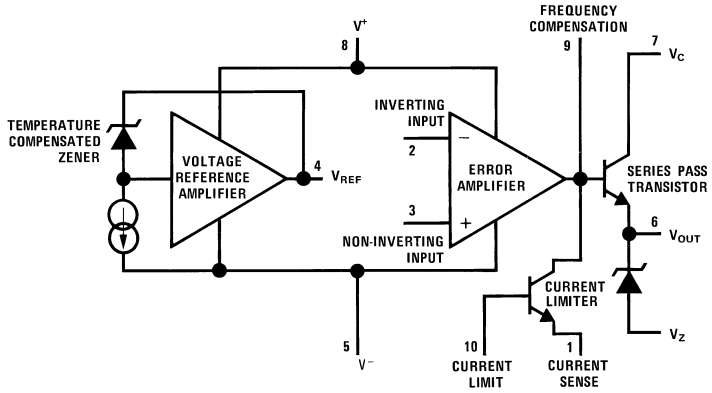


Figure 3. Top View
See Package NAJ0020A

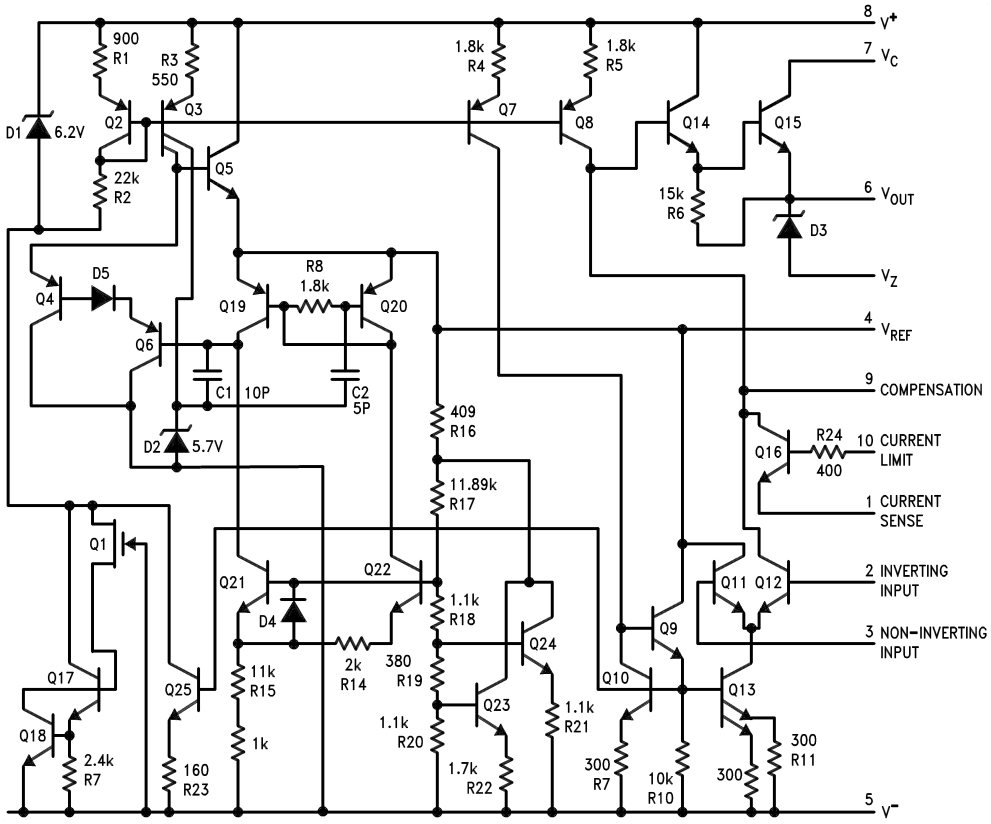
Equivalent Circuit



(1) Pin numbers refer to metal can package.

Copyright © 2005–2013, Texas Instruments Incorporated

Schematic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1]

Pulse Voltage from V^+ to V^- (50 ms)			50V
Continuous Voltage from V^+ to V^-			40V
Input-Output Voltage Differential			40V
Maximum Amplifier Input Voltage	Either Input		8.5V
	Differential		5V
Current from V_Z			25 mA
Current from V_{REF}			15 mA
Internal Power Dissipation Metal Can[2]	Cavity DIP[2]		900 mW 800 mW
	LCCC[2]		900 mW
Operating Temperature Range			$-55°C \le T_A \le +125°C$
Maximum T_J			+150°C
Storage Temperature Range			$-65°C \le T_A \le +150°C$
Lead Temperature (Soldering, 4 sec. max.)			300°C
Thermal Resistance	θ_{JA}	CDIP (Still Air)	100°C/W
		CDIP (500LF/ Min Air flow)	61°C/W
		Metal Can (Still Air)	156°C/W
		Metal Can (500LF/ Min Air flow)	89°C/W
		LCCC (Still Air)	96°C/W
		LCCC (500LF/ Min Air flow)	70°C/W
	θ_{JC}	CDIP	22°C/W
		Metal Can	37°C/W
		LCCC	27°C/W
ESD Tolerance[3]			500V

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For specified specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is less. See derating curves for maximum power rating above 25°C.

(3) Human body model, 1.5 kΩ in series with 100 pF.

Quality Conformance Inspection — MIL-STD-883, Method 5005 — Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Copyright © 2005–2013, Texas Instruments Incorporated

Electrical Characteristics

DC Parameters[1]

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{rline}	Line Regulation	12V ≤ V_{IN} ≤ 15V, V_{OUT} = 5V, I_L = 1mA		−0.1	0.1	%V_{OUT}	1
				−0.2	0.2	%V_{OUT}	2
				−0.3	0.3	%V_{OUT}	3
		12V ≤ V_{IN} ≤ 40V, V_{OUT} = 2V, I_L = 1mA		−0.2	0.2	%V_{OUT}	1
		9.5V ≤ V_{IN} ≤ 40V, V_{OUT} = 5V, I_L = 1mA		−0.3	0.3	%V_{OUT}	1
V_{rload}	Load Regulation	1mA ≤ I_L ≤ 50mA, V_{IN} = 12V, V_{OUT} = 5V		−0.15	0.15	%V_{OUT}	1
				−0.4	0.4	%V_{OUT}	2
				−0.6	0.6	%V_{OUT}	3
		1mA ≤ I_L ≤ 10mA, V_{IN} = 40V, V_{OUT} = 37V		−0.5	0.5	%V_{OUT}	1
		6mA ≤ I_L ≤ 12mA, V_{IN} = 10V, V_{OUT} = 7.5V		−0.2	0.2	%V_{OUT}	1
V_{REF}	Voltage Reference	I_{REF} = 1mA, V_{IN} = 12V		6.95	7.35	V	1
				6.9	7.4	V	2, 3
I_{SCD}	Standby Current	V_{IN} = 30V, I_L = I_{REF} = 0, V_{OUT} = V_{REF}		0.5	3	mA	1
				0.5	2.4	mA	2
				0.5	3.5	mA	3
I_{OS}	Short Circuit Current	V_{OUT} = 5V, V_{IN} =12V, R_{SC} = 10Ω, R_L = 0		45	85	mA	1
V_Z	Zener Voltage	V_{IN} = 40V, V_{OUT} = 7.15V, I_Z = 1mA	See[2] [3]	5.58	6.82	V	1
V_{OUT}	Output Voltage	V_{IN} = 12V, V_{OUT} = 5V, I_L = 1mA		4.5	5.5	V	1, 2, 3

(1) Unless otherwise specified, T_A = 25°C, V_{IN} = V^+ = V_C = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 kΩ connected as shown in Figure 15 Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.
(2) For metal can applications where V_Z is required, an external 6.2V zener diode should be connected in series with V_{OUT}.
(3) Tested for DIPS only.

Electrical Characteristics

AC Parameters[1]

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
Delta V_{OUT} / Delta V_{IN}	Ripple Rejection	f = 120H_Z, C_{REF} = 0, V_{INS} = 2V_{RMS}		55		dB	4
		f = 120H_Z, C_{REF} = 5μF, V_{INS} = 2V_{RMS}		67		dB	4

(1) Unless otherwise specified, T_A = 25°C, V_{IN} = V^+ = V_C = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 kΩ connected as shown in Figure 15 Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

Copyright © 2005–2013, Texas Instruments Incorporated

Typical Performance Characteristics

Load Regulation Characteristics with Current Limiting

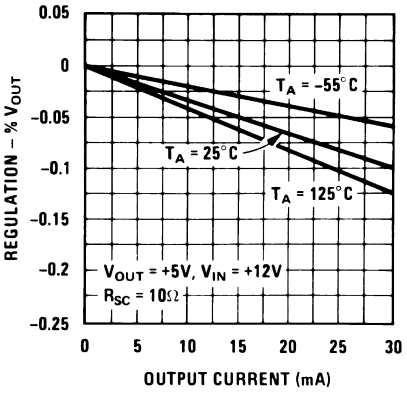


Figure 4.

Load Regulation Characteristics with Current Limiting

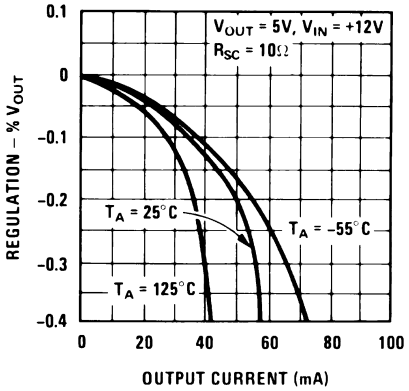


Figure 5.

Load & Line Regulation vs Input-Output Voltage Differential

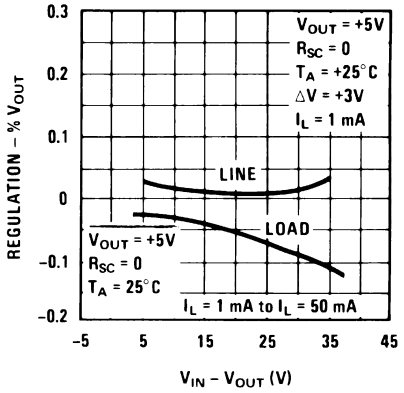


Figure 6.

Current Limiting Characteristics

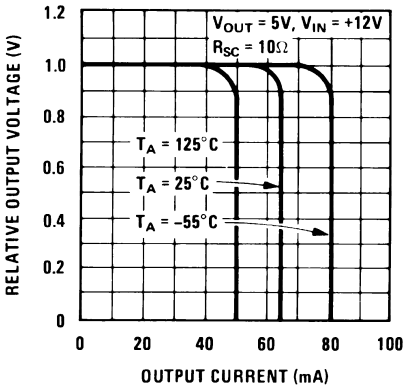


Figure 7.

Current Limiting Characteristics vs Junction Temperature

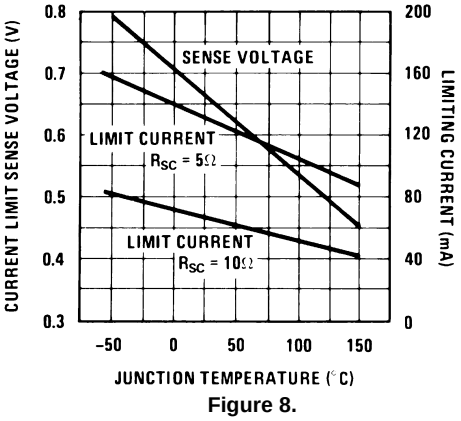


Figure 8.

Standby Current Drain vs Input Voltage

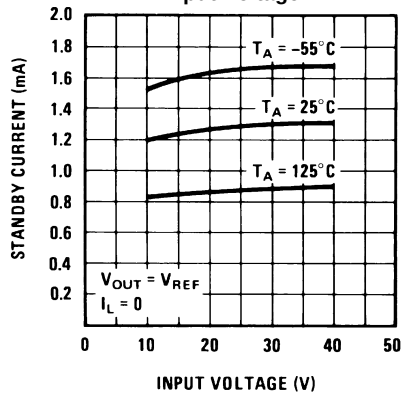


Figure 9.

Copyright © 2005–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Line Transient Response

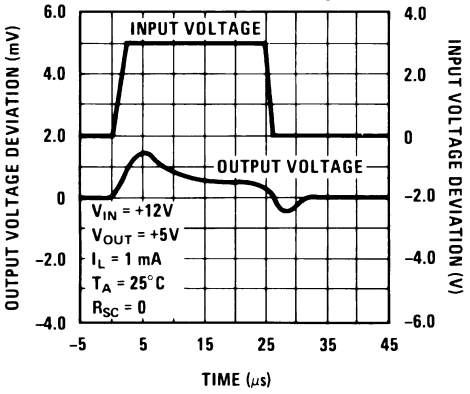


Figure 10.

Load Transient Response

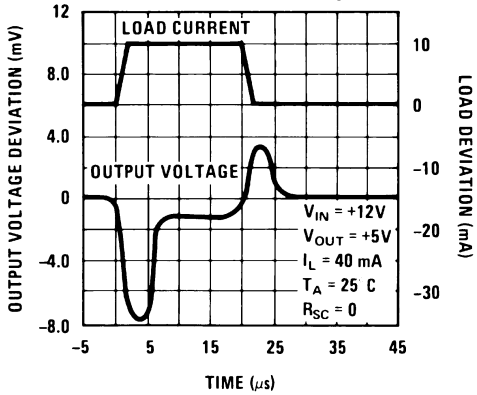


Figure 11.

Output Impedence vs Frequency

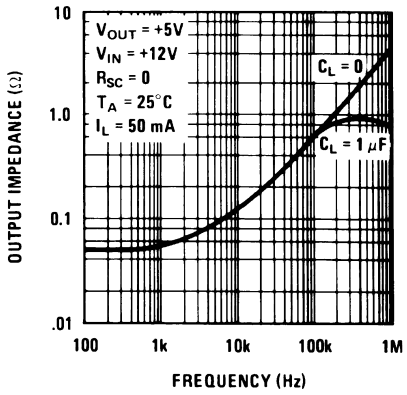


Figure 12.

Maximum Power Ratings

Noise vs Filter Capacitor (C_{REF} in Circuit of Figure 15 (Bandwidth 100 Hz to 10 kHz)

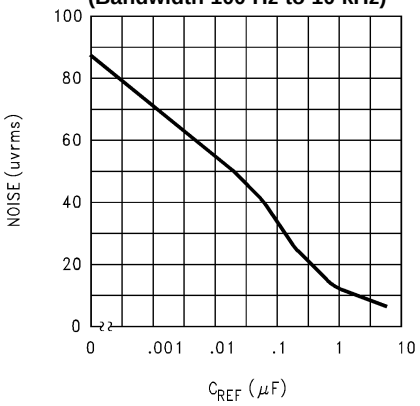


Figure 13.

Power Dissipation vs Ambient Temperature

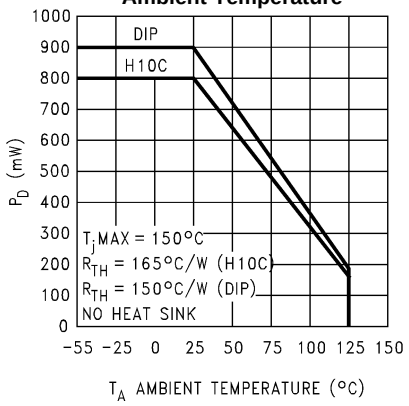


Figure 14.

Copyright © 2005–2013, Texas Instruments Incorporated

RESISTOR VALUES (KΩ) FOR STANDARD OUTPUT VOLTAGE

Positive	Applicable	Fixed		Output			Negative		Fixed		5% Output		
Output	Figures	Output		Adjustable			Output	Applicable	Output		Adjustable		
Voltage		±5%		±10%(1)			Voltage	Figures	±5%		±10%		
	See(2)	R1	R2	R1	P1	R2			R1	R2	R1	P1	R2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	0.75	0.5	2.2	−6(3)	3, (10)	3.57	2.43	1.2	0.5	0.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 9, 12)	1.87	7.15	0.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

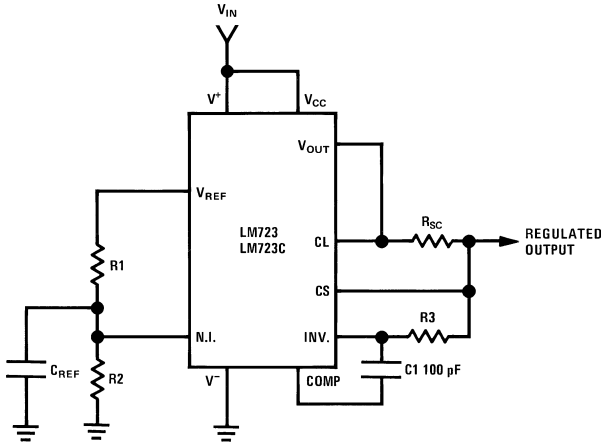
(1) Replace R1/R2 in figures with divider shown in Figure 27.
(2) Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp.
(3) V^+ and V_{CC} must be connected to a +3V or greater supply.

Table 1. Formulae for Intermediate Output Voltages

Outputs from +2 to +7 volts	Outputs from +4 to +250 volts	Current Limiting
(Figure 15, Figure 18, Figure 19, Figure 20, Figure 23, Figure 26)	(Figure 21)	
$V_{OUT} = \left(V_{REF} \times \frac{R2}{R1 + R2}\right)$ (1)	$V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R2 - R1}{R1}\right); R3 = R4$ (2)	$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$ (3)
Outputs from +7 to +37 volts	**Outputs from −6 to −250 volts**	**Foldback Current Limiting**
(Figure 16, Figure 18, Figure 19, Figure 20, Figure 23, Figure 26)	(Figure 17, Figure 22, Figure 24)	$I_{KNEE} = \left(\frac{V_{OUT}\,R3}{R_{SC}\,R4} + \frac{V_{SENSE}\,(R3 + R4)}{R_{SC}\,R4}\right)$
$V_{OUT} = \left(V_{REF} \times \frac{R1 + R2}{R2}\right)$ (5)	$V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R1 + R2}{R1}\right); R3 = R4$ (6)	$I_{SHORT\ CKT} = \left(\frac{V_{SENSE}}{R_{SC}} \times \frac{R3 + R4}{R4}\right)$ (4)

Copyright © 2005–2013, Texas Instruments Incorporated

Typical Applications

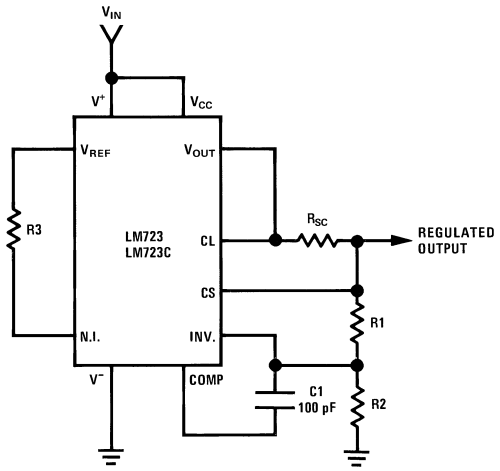


Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift.

Figure 15. Basic Low Voltage Regulator (V_{OUT} = 2 to 7 Volts)

Table 2. Basic Low Voltage Regulator (V_{OUT} = 2 to 7 Volts)

Typical Performance	
Regulated Output Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 50 mA)	1.5mV



Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

Figure 16. Basic High Voltage Regulator V_{OUT} = 7 to 37 Volts)

Table 3. Basic High Voltage Regulator V_{OUT} = 7 to 37 Volts)

Typical Performance	
Regulated Output Voltage	15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 50 mA)	4.5 mV

Copyright © 2005–2013, Texas Instruments Incorporated

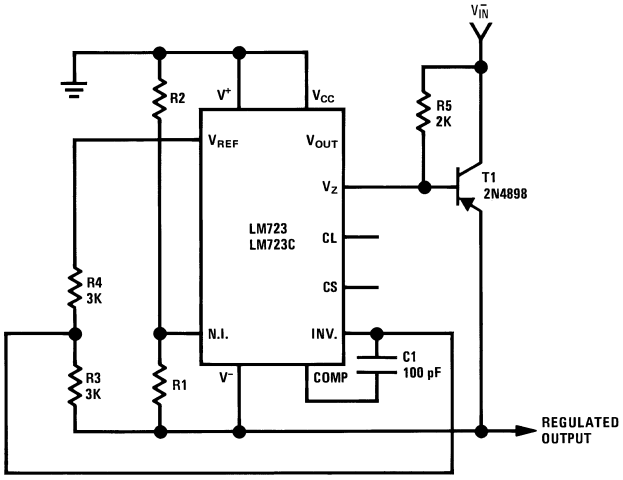


Figure 17. Negative Voltage Regulator

Table 4. Negative Voltage Regulator

Typical Performance	
Regulated Output Voltage	−15V
Line Regulation (ΔV_{IN} = 3V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

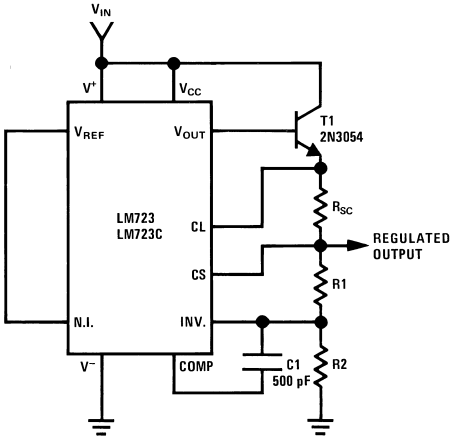


Figure 18. Positive Voltage Regulator - (External NPN Pass Transistor)

Table 5. Positive Voltage Regulator - (External NPN Pass Transistor)

Typical Performance	
Regulated Output Voltage	+15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 1A)	15 mV

Copyright © 2005–2013, Texas Instruments Incorporated

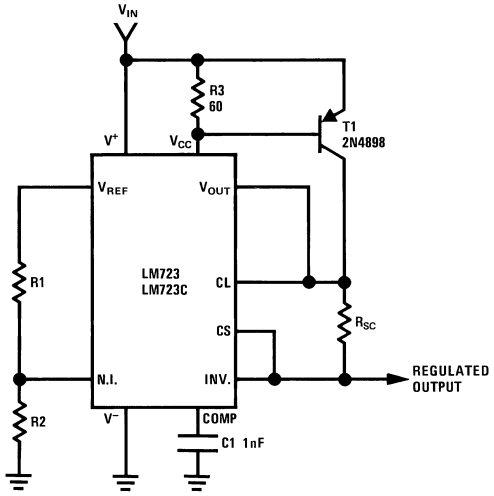


Figure 19. Positive Voltage Regulator – (External PNP Pass Transistor)

Table 6. Positive Voltage Regulator – (External PNP Pass Transistor)

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 1A)	5 mV

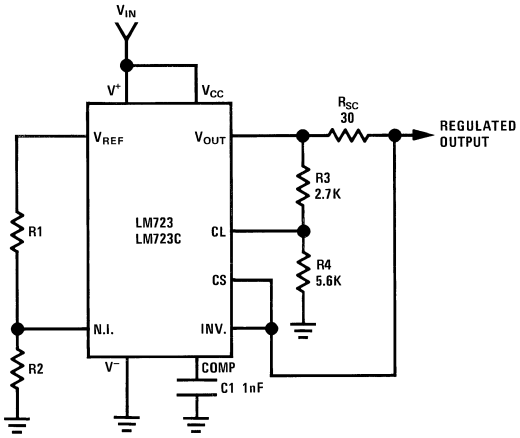


Figure 20. Foldback Current Limiting

Table 7. Foldback Current Limiting

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Short Circuit Current	20 mA

Copyright © 2005–2013, Texas Instruments Incorporated

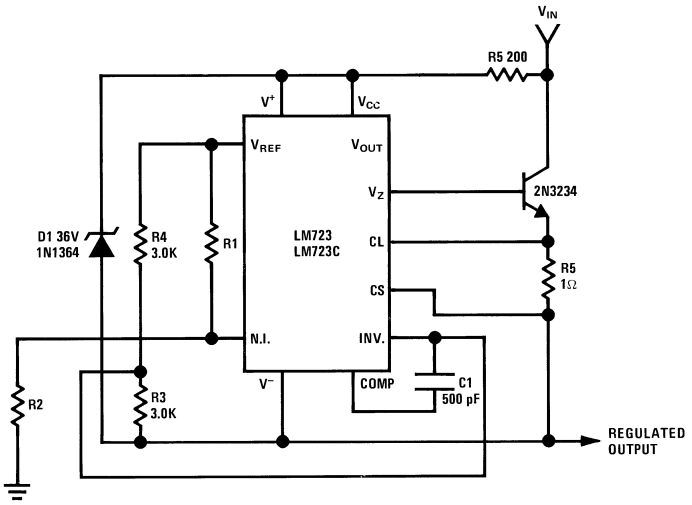


Figure 21. Positive Floating Regulator

Table 8. Positive Floating Regulator

Typical Performance	
Regulated Output Voltage	+50V
Line Regulation (ΔV_{IN} = 20V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

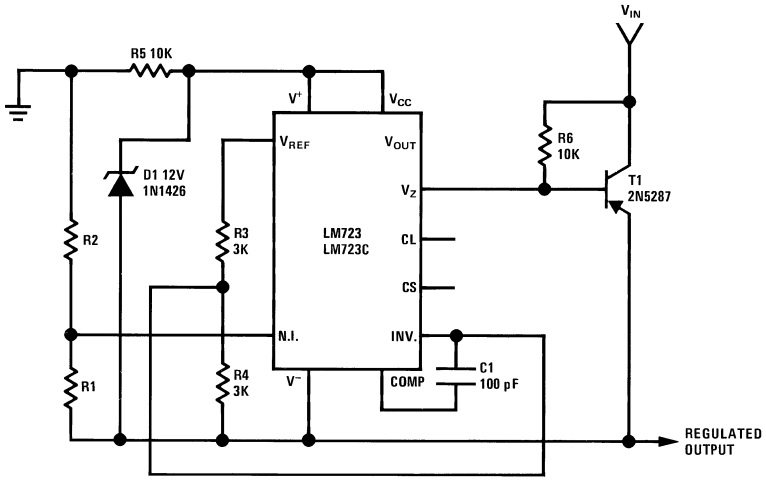


Figure 22. Negative Floating Regulator

Table 9. Negative Floating Regulator

Typical Performance	
Regulated Output Voltage	−100V
Line Regulation (ΔV_{IN} = 20V)	30 mV
Load Regulation (ΔI_L = 100 mA)	20 mV

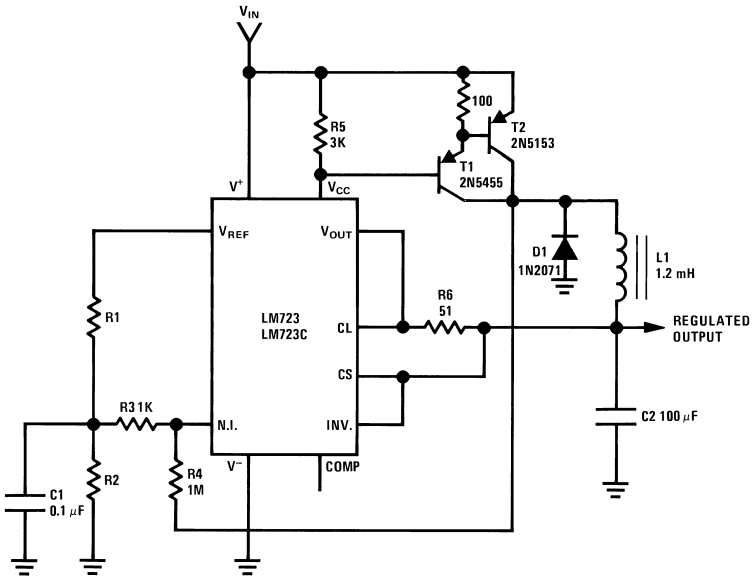


Figure 23. Positive Switching Regulator

Table 10. Positive Switching Regulator(1)

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 30V)	10 mV
Load Regulation (ΔI_L = 2A)	80 mV

(1) L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap

Copyright © 2005–2013, Texas Instruments Incorporated

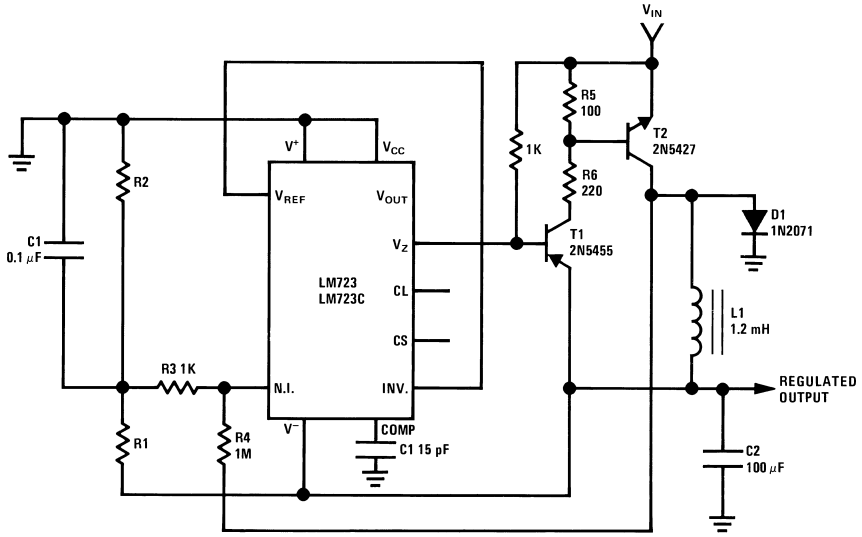
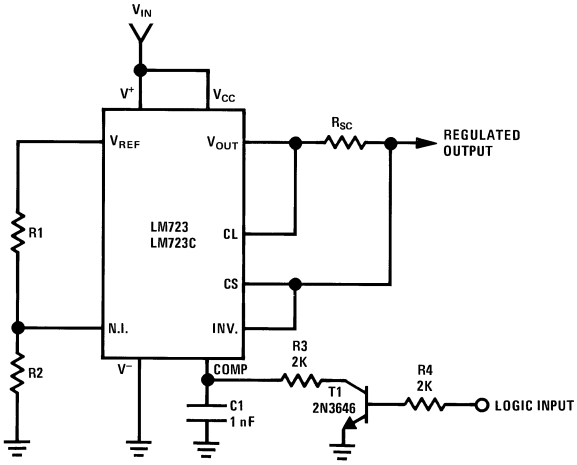


Figure 24. Negative Switching Regulator

Table 11. Negative Switching Regulator(1)

Typical Performance	
Regulated Output Voltage	−15V
Line Regulation (ΔV_{IN} = 20V)	8 mV
Load Regulation (ΔI_L = 2A)	6 mV

(1) L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap



Note: Current limit transistor may be used for shutdown if current limiting is not required.

Figure 25. Remote Shutdown Regulator with Current Limiting

Table 12. Remote Shutdown Regulator with Current Limiting

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

Copyright © 2005–2013, Texas Instruments Incorporated

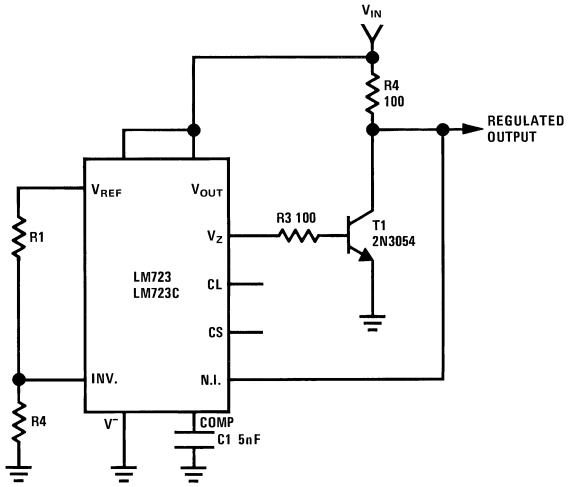
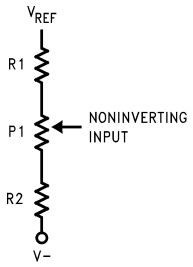


Figure 26. Shunt Regulator

Table 13. Shunt Regulator

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 10V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV



(1) Replace R1/R2 in figures with divider shown in Figure 27

Figure 27. Output Voltage Adjust

Revision History Section

Date Released	Revision	Section	Originator	Changes
02/15/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheet converted into one Corp. data sheet format. MNLM723-X, Rev. 1A0. MDS data sheet will be archived. AC and Drift parameters removed from specification because they only applied to the JAN B/S devices, covered in a separate datasheet.

Copyright © 2005–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	16

Copyright © 2005–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM723 MD8	Active	Production	DIESALE (Y) | 0	400 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM723E/883	Active	Production	LCCC (NAJ) | 20	50 | TUBE	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM723E /883 Q ACO /883 Q >T
LM723H/883	Active	Production	TO-100 (LME) | 10	20 | TRAY NON-STD	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM723H/883 Q ACO LM723H/883 Q >T
LM723J/883	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM723J/883 Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

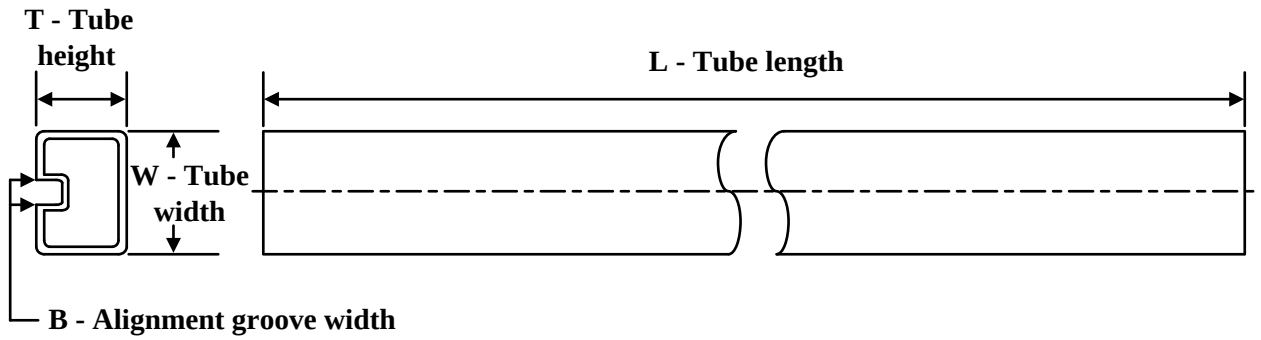
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

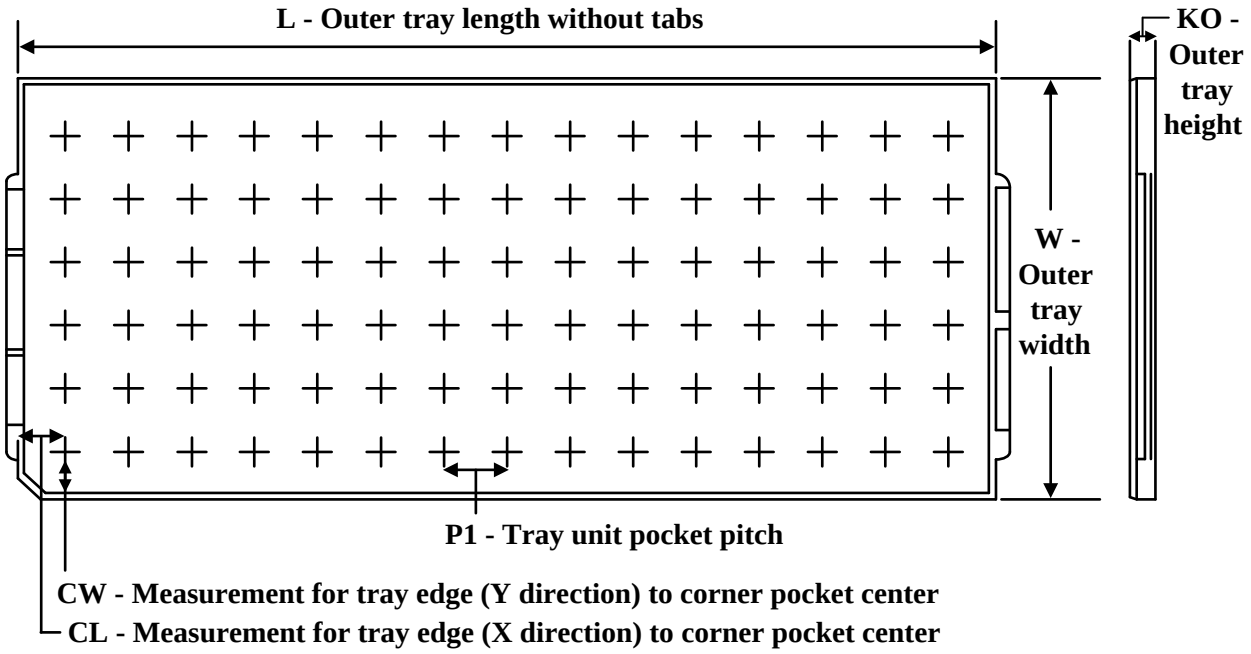
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM723E/883	NAJ	LCCC	20	50	470	11	3810	0
LM723J/883	J	CDIP	14	25	506.98	15.24	13440	NA

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

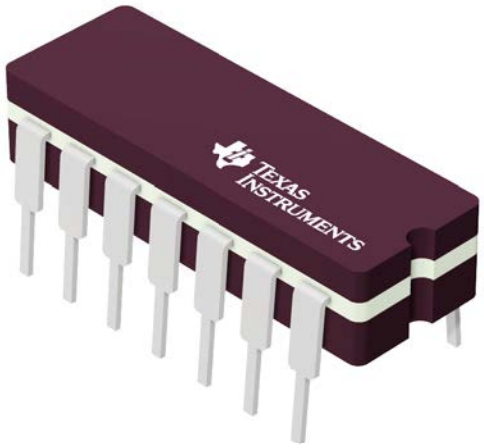
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LM723H/883	LME	TO-CAN	10	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

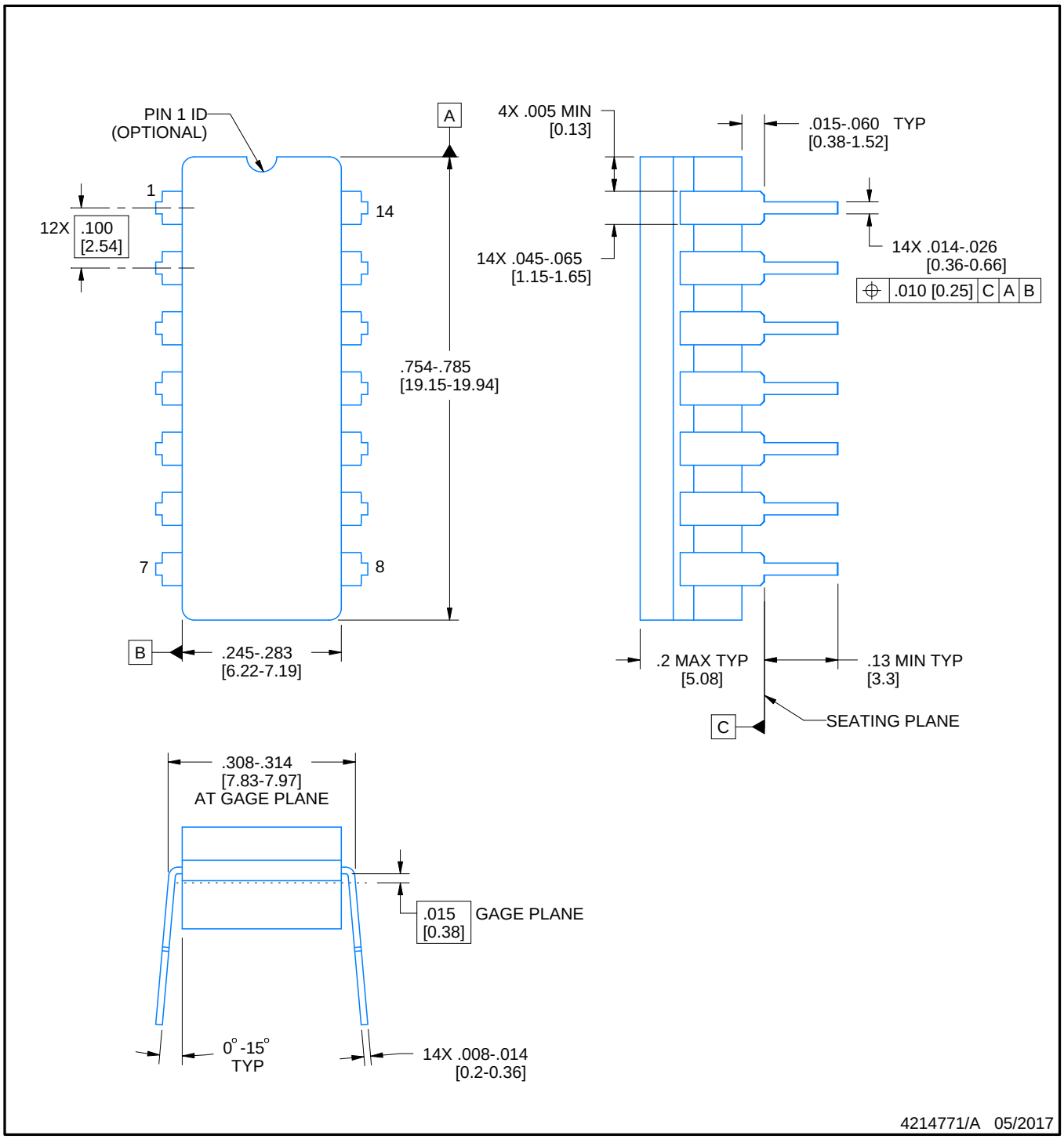


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

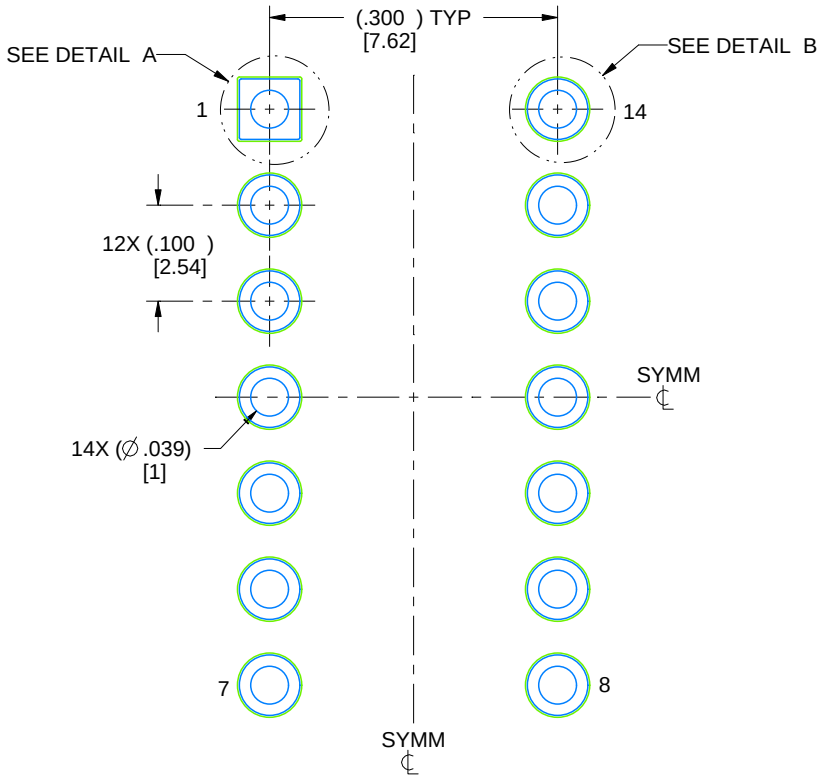
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

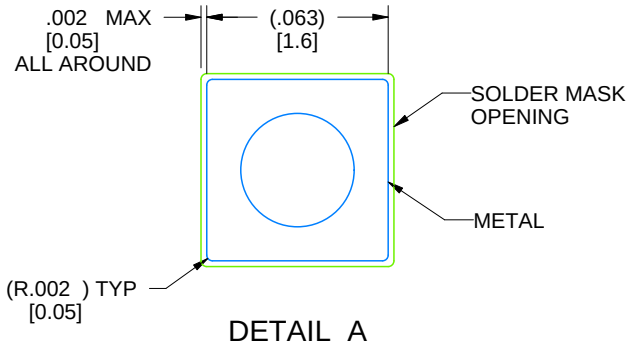
J0014A

CDIP - 5.08 mm max height

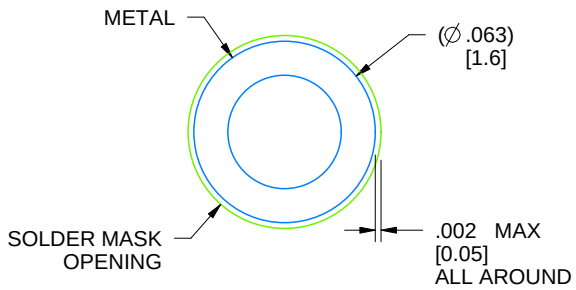
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



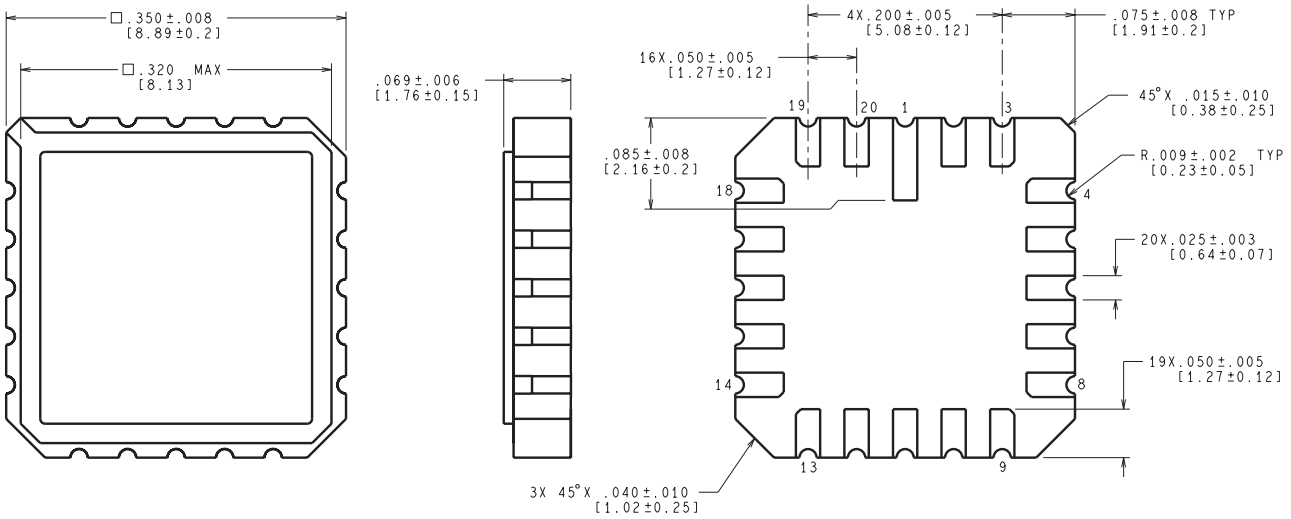
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

NAJ0020A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

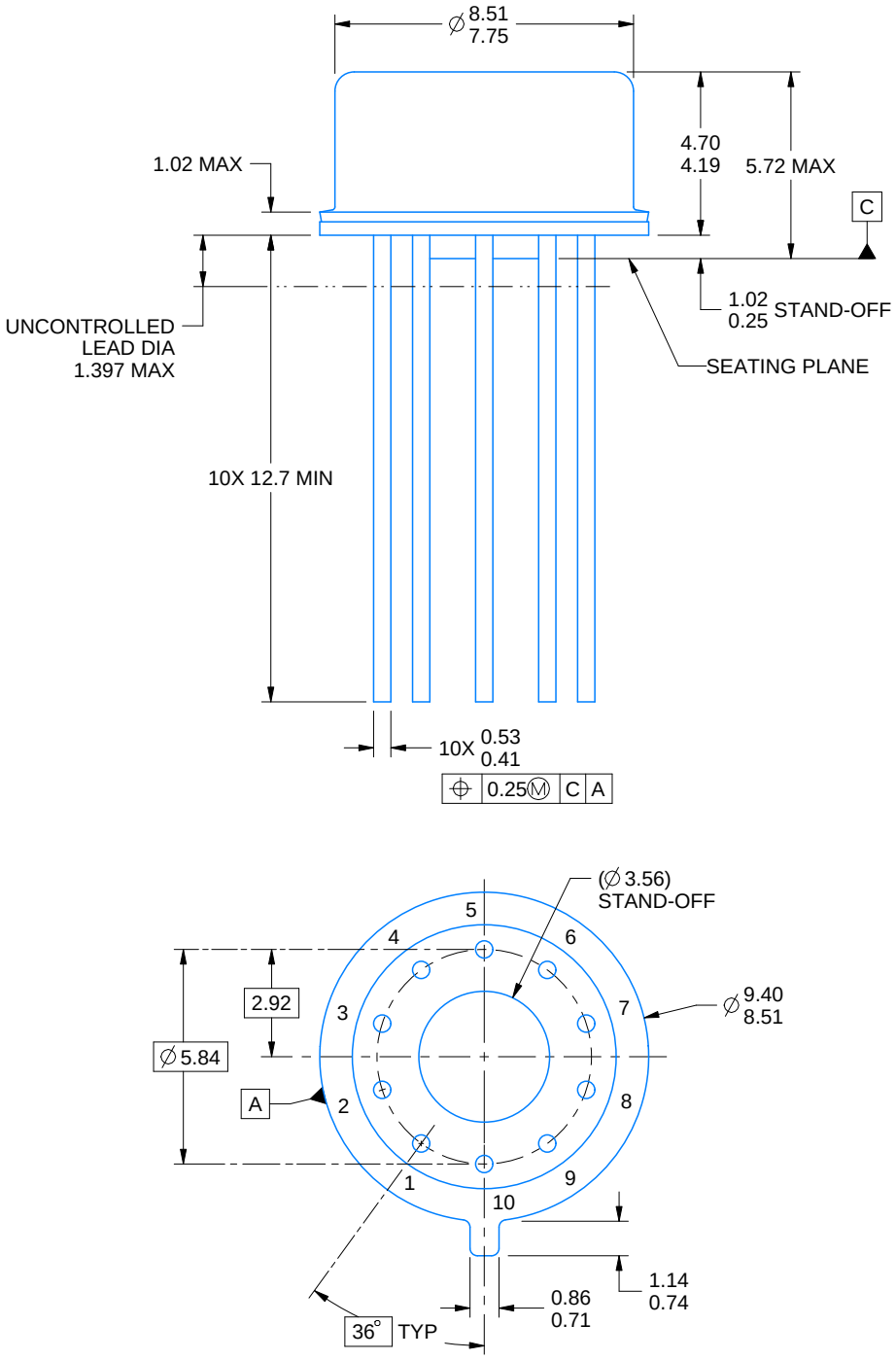
E20A (Rev F)

PACKAGE OUTLINE

LME0010A

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



4220604/B 09/2024

NOTES:

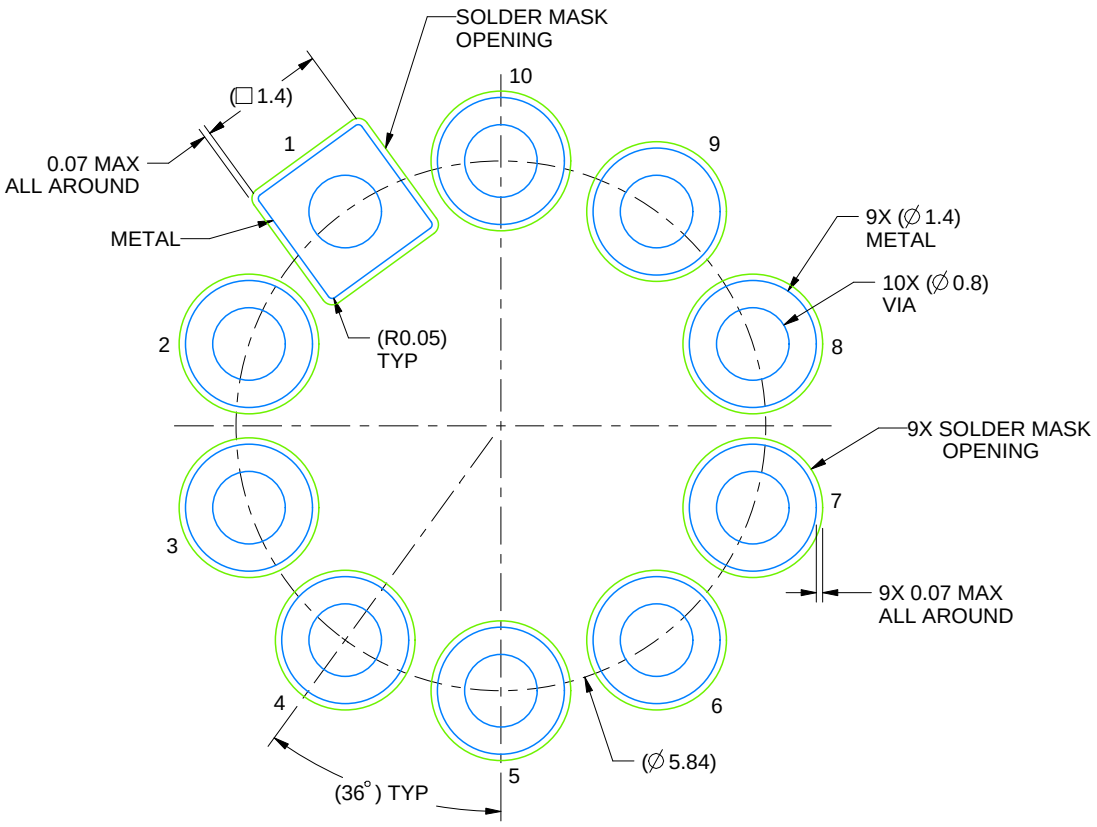
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-006/TO-100.

EXAMPLE BOARD LAYOUT

LME0010A

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220604/B 09/2024

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025