TPS2001D 限流配电开关

1 特性

- 单一电源开关系列
- 2 A 额定电流
- ±20% 精确、固定、恒定电流限制
- 快速过流响应：2μs
- 去尖峰脉冲故障报告
- 输出放电
- 反向电流阻断
- 内置软启动
- 环境温度范围：-40°C 至 85°C
- 经 UL 检测和认证以及 CB 认证-文件号E169910

2 应用

- USB 端口和集线器、笔记本电脑和台式计算机
- 高清数字电视
- 机顶盒
- 短路保护

3 说明

TPS2001D 配电开关专门用于可能会出现高电容负载和短路的 应用 ，例如 USB。

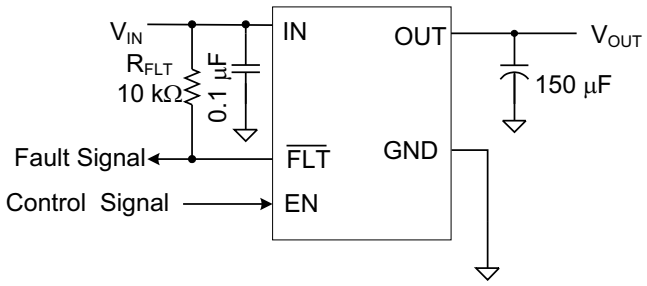
当输出负载超过电流限制阈值时，TPS2001D 通过运行在恒定电流模式下来将输出电流限制在安全的水平。这就在所有条件下提供了一个可预计的故障电流。发生输出短路后，快速过载响应时间有利于缓解 5V 主电源的压力以提供稳定电源。通过控制电源开关的上升时间和下降时间，可以大大减少开关切换期间的电流涌入。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS2001D	VSSOP (8)	3.00mm × 3.00mm
	SOT-23 (5)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型应用图



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4 修订历史记录

Changes from Original (July 2017) to Revision A **Page**

- Changed $R_{DS(on)}$ TYP from 72 to 66 and added MAX 77 for DBV package ... 5
- Added $R_{DS(on)}$ MAX 77 for DBV package for 2-A rated output, $–40°C \le (T_J , T_A) \le 85°C$ condition ... 5
- Changed $R_{DS(on)}$ TYP from 72 to 66 for DBV package for 2-A rated output, and added MAX 106 ... 6

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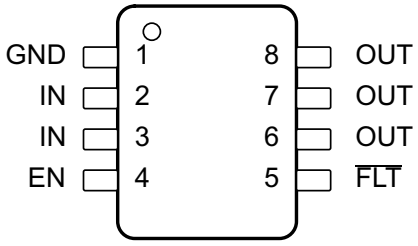
5 Device Comparison Table(1)

MAXIMUM OPERATING CURRENT	OUTPUT DISCHARGE	ENABLE
2 A	Yes	High

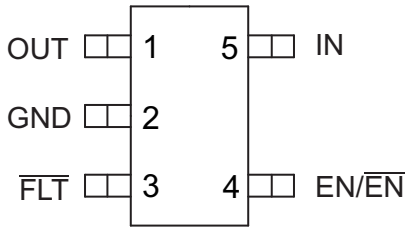
(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

6 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



DBV Package
5-Pin SOT-23
Top View



Pin Functions - DGK Package

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	4	I	Enable input, logic high turns on power switch
$\overline{\text{FLT}}$	5	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions
GND	1	—	Ground connection
IN	2, 3	PWR	Input voltage and power-switch drain; connect a 0.1-µF or greater ceramic capacitor from IN to GND close to the IC
OUT	6, 7, 8	PWR	Power-switch output, connect to load

Pin Functions - DBV Package

PIN		I/O	DESCRIPTION
NAME	NO.		
EN or $\overline{\text{EN}}$	4	I	Enable input, logic high turns on power switch
$\overline{\text{FLT}}$	3	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions
GND	2	—	Ground connection
IN	5	PWR	Input voltage and power-switch drain; connect a 0.1-µF or greater ceramic capacitor from IN to GND close to the IC
OUT	1	PWR	Power-switch output, connect to load

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Voltage on IN, OUT, EN, $\overline{FLT}$ (4)	–0.3	6	V
Voltage from IN to OUT	–6	6	V
Maximum junction temperature, T_J	Internally Limited		
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute maximum ratings apply over recommended junction temperature range.
(3) Voltages are with respect to GND unless otherwise noted.
(4) See *Input and Output Capacitance*.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		IEC 61000-4-2 contact discharge	±8000	
		IEC 61000-4-2 air-gap discharge(3)	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) V_{OUT} was surged on a PCB with input and output bypassing per the *典型应用图* on the first page (except input capacitor was 22 µF) with no device failures.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN	4.5		5.5	V
V_{EN}	Input voltage, EN	0		5.5	V
V_{IH}	High-level input voltage, EN	2			V
V_{IL}	Low-level input voltage, EN			0.7	V
I_{OUT}	Continuous output current, OUT(1)			2	A
T_J	Operating junction temperature	–40		125	°C
$I_{\overline{FLT}}$	Sink current into $\overline{FLT}$	0		5	mA

(1) Some package and current rating may request an ambient temperature derating of 85°C.

7.4 Thermal Information

THERMAL METRIC(1)		TPS2001D DBV (SOT-23) 5 PINS	TPS2001D DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220.4	205.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.7	94.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.9	126.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	24.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.2	125.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W
$R_{\theta JA}$Custom	See *Power DIssipation and Junction Temperature*	134.9	110.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics: $T_J = T_A = 25°C$

Unless otherwise noted: V_{IN} = 5 V, $V_{EN} = V_{IN}$, I_{OUT} = 0 A. See *Device Comparison Table*(1) for the rated current of each part number. Parametrics over a wider operational range are shown in *Electrical Characteristics: –40°C ≤ T_J ≤ 125°C*(2).

PARAMETER		TEST CONDITIONS(2)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(on)}$	Input – output resistance	2-A rated output, 25°C	DGK		72	84	mΩ
		2-A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DGK		66	98	mΩ
		2-A rated output, 25°C	DBV		66	77	mΩ
		2-A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DBV		66	90	mΩ
CURRENT LIMIT							
I_{OS}(3)	Current limit, See Figure 6	2-A rated output		2.35	2.9	3.4	A
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled	I_{OUT} = 0 A			0.01	1	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{IN} = 5.5 V, I_{OUT} = 0 A				2	
I_{SE}	Supply current, switch enabled	I_{OUT} = 0 A			60	70	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{IN} = 5.5 V, I_{OUT} = 0 A				85	
I_{lkg}	Leakage current	V_{OUT} = 0 V, V_{IN} = 5 V, disabled, measure I_{VIN}			0.05	1	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{OUT} = 0 V, V_{IN} = 5 V, disabled, measure I_{VIN}				2	
I_{REV}	Reverse leakage current	V_{OUT} = 5 V, V_{IN} = 0 V, measure I_{VOUT}			0.1	1	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{OUT} = 5 V, V_{IN} = 0 V, measure I_{VOUT}				5	
OUTPUT DISCHARGE							
R_{PD}	Output pulldown resistance(4)	$V_{IN} = V_{OUT}$ = 5 V, disabled		400	470	600	Ω

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(3) See *Current Limit* section for explanation of this parameter.
(4) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

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7.6 Electrical Characteristics: –40°C ≤ T_J ≤ 125°C

Unless otherwise noted:4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, I_{OUT} = 0 A, typical values are at 5 V and 25°C.

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(ON)}$	Input – output resistance	2-A rated output	DGK		72	112	mΩ
		2-A rated output	DBV		66	106	mΩ
ENABLE INPUT (EN)							
	Threshold	Input rising		1	1.45	2	V
	Hysteresis			0.07	0.13	0.2	V
	Leakage current	V_{EN} = 0 V or 5.5 V		–1	0	1	µA
CURRENT LIMIT							
I_{OS}(2)	Current limit, See Figure 20	2-A rated output		2.3	2.9	3.6	A
t_{IOS}	Short-circuit response time(3)	V_{IN} = 5 V (see Figure 6), One-half full load → R_{SHORT} = 50 mΩ, Measure from application to when current falls below 120% of final value			2		µs
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled	I_{OUT} = 0 A			0.01	10	µA
I_{SE}	Supply current, switch enabled	I_{OUT} = 0 A			65	90	µA
I_{REV}	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = 0 V, measure I_{VOUT}			0.2	20	µA
UNDERVOLTAGE LOCKOUT							
V_{UVLO}	Rising threshold	V_{IN}↑		3.5	3.75	4	V
	Hysteresis(3)	V_{IN}↓			0.14		V
$\overline{FLT}$							
	Output low voltage, $\overline{FLT}$	$I_{\overline{FLT}}$ = 1 mA				0.2	V
	OFF-state leakage	$V_{\overline{FLT}}$ = 5.5 V				1	µA
$t_{\overline{FLT}}$	$\overline{FLT}$ deglitch	$\overline{FLT}$ assertion or deassertion deglitch		6	9	12	ms
OUTPUT DISCHARGE							
R_{PD}	Output pulldown resistance	V_{IN} = 4 V, V_{OUT} = 5 V, disabled		350	560	1200	Ω
		V_{IN} = 5 V, V_{OUT} = 5 V, disabled		300	470	800	
THERMAL SHUTDOWN							
	Rising threshold (T_J)	In current limit		135			°C
		Not in current limit		155			
	Hysteresis (3)				20		

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) See *Current Limit* for explanation of this parameter.
(3) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.7 Timing Requirements: T_J = T_A = 25°C

				MIN	NOM	MAX	UNIT
ENABLE INPUT (EN)							
t_{ON}	Turnon time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↑. See Figure 1, Figure 3, and Figure 4		1.2	1.7	2.2	ms
t_{OFF}	Turnoff time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↓. See Figure 1, Figure 3, and Figure 4		1.7	2.1	2.5	ms
t_R	Rise time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V. See Figure 2		0.5	0.7	1	ms
t_F	Fall time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V. See Figure 2		0.3	0.43	0.55	ms

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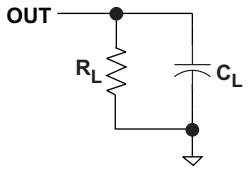


Figure 1. Output Rise and Fall Test Load

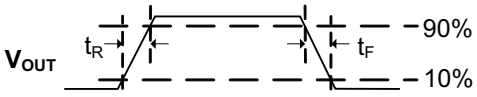


Figure 2. Power-On and Power-Off Timing

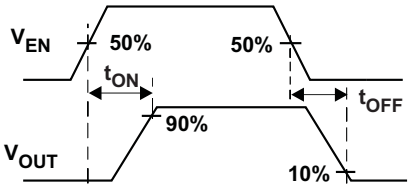


Figure 3. Enable Timing, Active High Enable

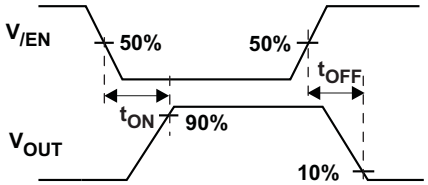


Figure 4. Enable Timing, Active Low Enable

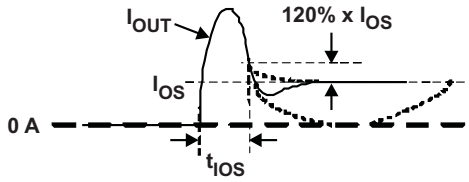


Figure 5. Output Short-Circuit Parameters

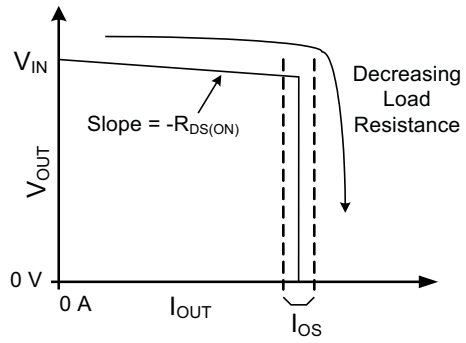


Figure 6. Output Characteristic Showing Current Limit

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7.8 Typical Characteristics

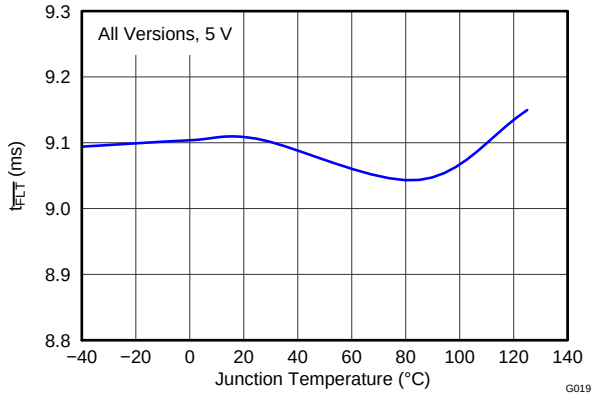


Figure 7. Deglitch Period ($T_{\overline{FLT}}$) vs Temperature

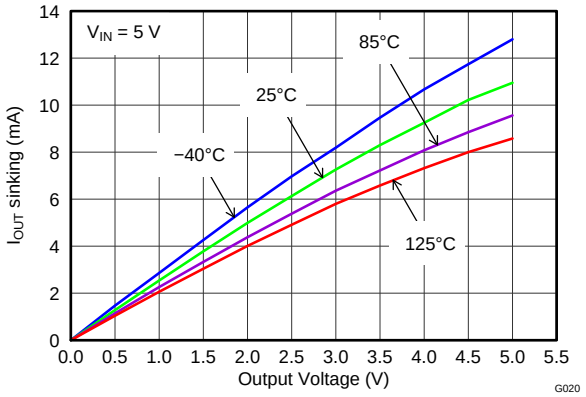


Figure 8. Output Discharge Current vs Output Voltage

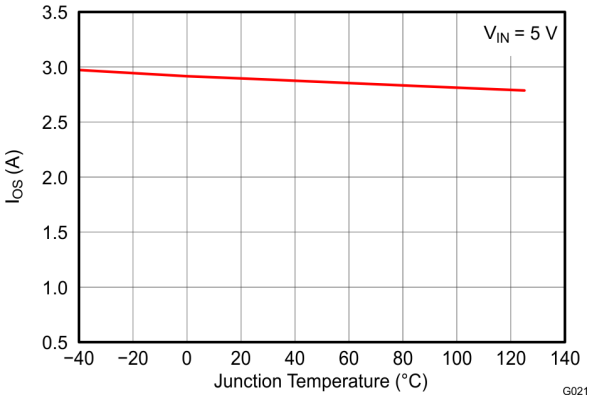


Figure 9. Short Circuit Current (I_{OS}) vs Temperature

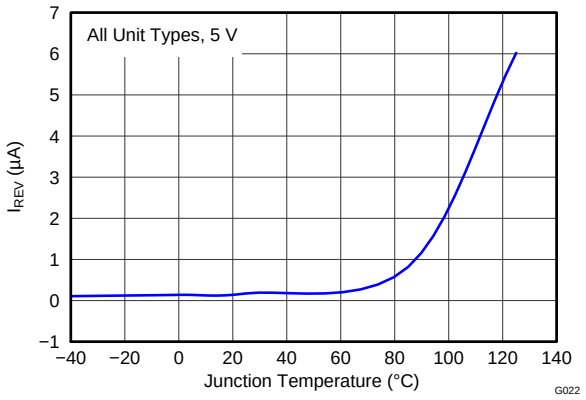


Figure 10. Reverse Leakage Current (I_{REV}) vs Temperature

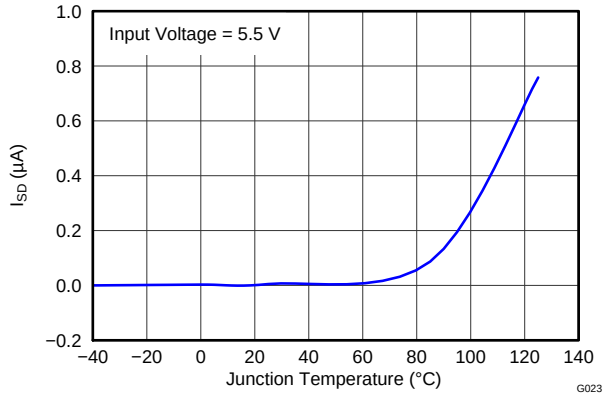


Figure 11. Disabled Supply Current (I_{SD}) vs Temperature

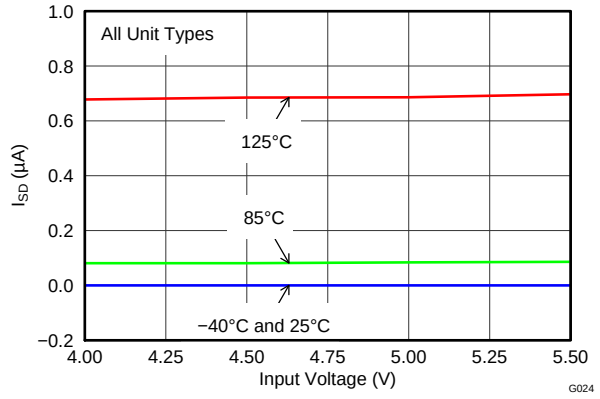


Figure 12. Disabled Supply Current (I_{SD}) vs Input Voltage

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Typical Characteristics (continued)

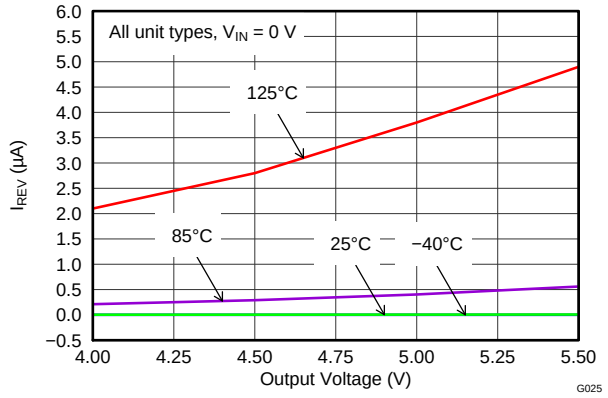


Figure 13. Reverse Leakage Current (I_{REV}) vs Output Voltage

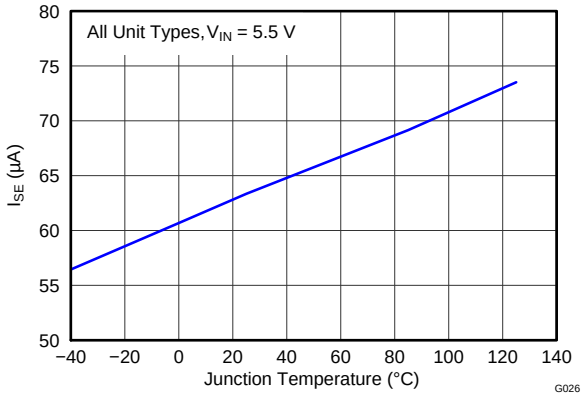


Figure 14. Enabled Supply Current (I_{SE}) vs Temperature

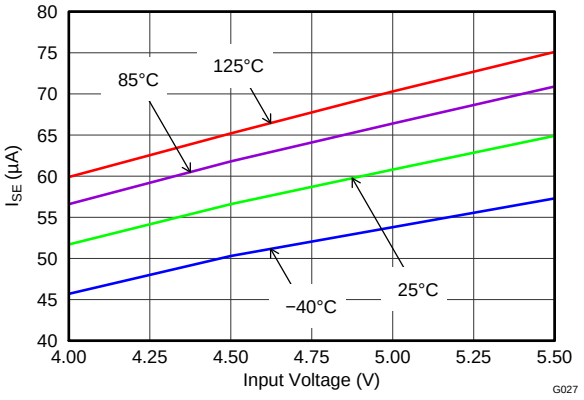


Figure 15. Enabled Supply Current (I_{SE}) vs Input Voltage

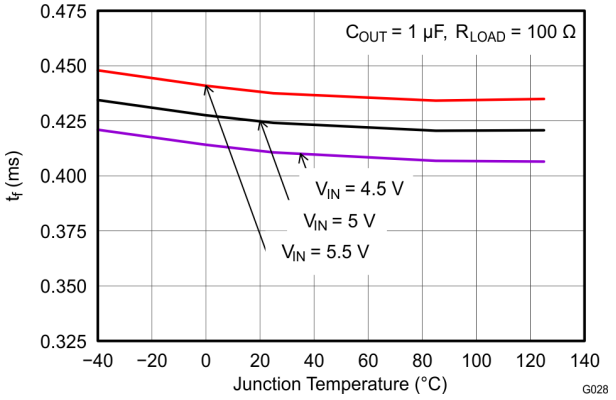


Figure 16. Output Fall Time (T_F) vs Temperature

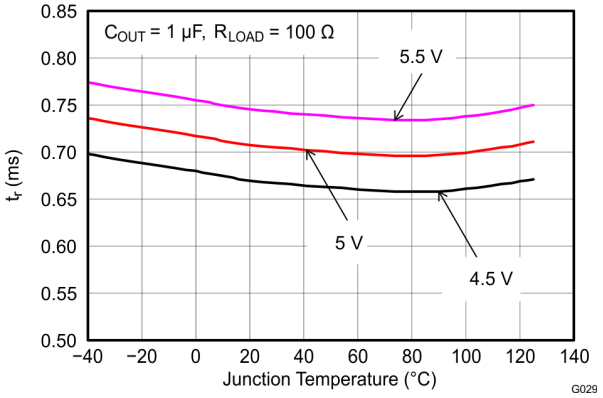


Figure 17. Output Rise Time (T_R) vs Temperature

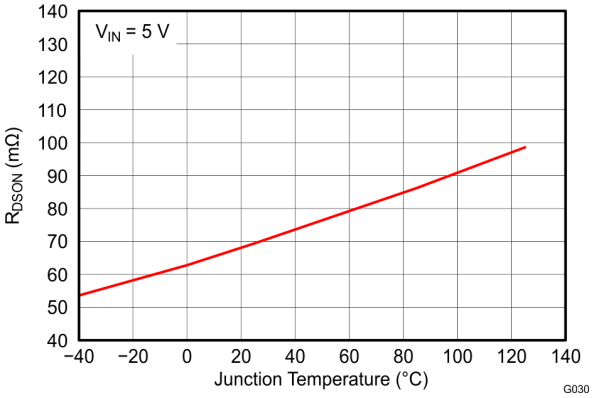


Figure 18. Input-Output Resistance ($R_{DS(ON)}$) vs Temperature

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8 Detailed Description

8.1 Overview

The TPS2001D is a current-limited, power-distribution switch providing 2-A continuous load current in 5-V circuits. The device uses an N-channel MOSFET for low resistance, maintaining voltage regulation to the load. It is designed for applications where short circuits or heavy capacitive loads are encountered. Device features include enable, reverse blocking when disabled, output discharge pulldown, overcurrent protection, overtemperature protection, and deglitched fault reporting.

8.2 Functional Block Diagram

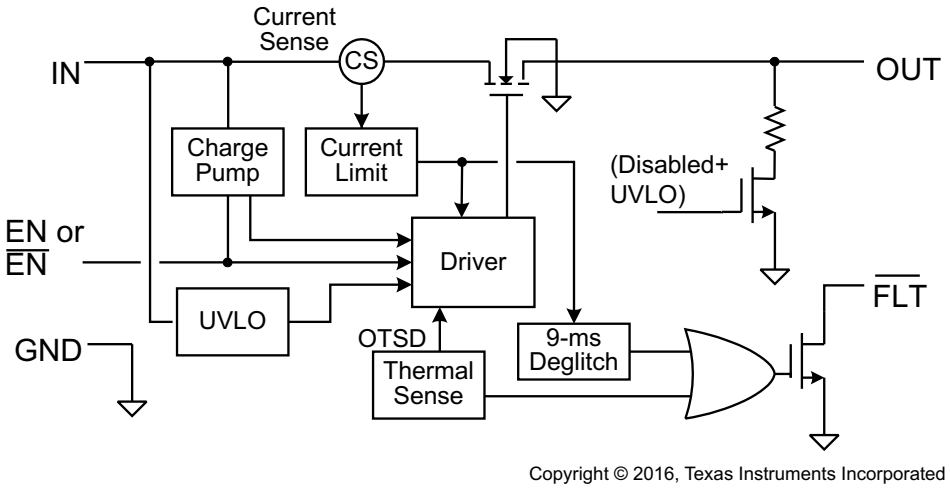


Figure 19. TPS2001D Block Diagram

8.3 Feature Description

8.3.1 Undervoltage Lockout

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted ON/OFF cycling due to input voltage drop from large current surges. $\overline{FLT}$ is high impedance when the TPS2001D is in UVLO.

8.3.2 Enable

The logic enable input (EN), controls the power switch, bias for the charge pump, driver, and other circuits. The supply current is reduced to less than 1 µA when the TPS2001D is disabled. Disabling the TPS2001D immediately clears an active $\overline{FLT}$ indication. The enable input is compatible with both TTL and CMOS logic levels.

The turnon and turnoff times (t_{ON}, t_{OFF}) are composed of a delay and a rise or fall time (t_R, t_F). The delay times are internally controlled. The rise time is controlled by both the TPS2001D and the external loading (especially capacitance). Its fall time is controlled by the loading (R and C), and the output discharge (R_{PD}). An output load consisting of only a resistor experiences a fall time set by the device. An output load with parallel R and C elements experiences a fall time determined by the (R × C) time constant if it is longer than the t_F.

The enable must not be left open, and may be tied to VIN or GND depending on the device.

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Feature Description (continued)

8.3.3 Internal Charge Pump

The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the gate driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionality. The MOSFET power switch blocks current from OUT to IN when turned off by the UVLO or disabled.

8.3.4 Current Limit

The device responds to overloads by limiting output current to the static I_{OS} levels shown in *Electrical Characteristics: $T_J = T_A = 25°C$*. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by ($I_{OS} \times R_{LOAD}$). Two possible overload conditions can occur. The first overload condition occurs when either:

1. input voltage is first applied, enable is true, and a short circuit is present (load which draws $I_{OUT} > I_{OS}$)
2. input voltage is present and the TPS2001D is enabled into a short circuit.

The output voltage is held near zero potential with respect to ground and the TPS2001D ramps the output current to I_{OS}. The TPS2001D limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within t_{IOS} (Figure 5 and Figure 6) when the specified overload (see *Electrical Characteristics: –40°C ≤ T_J ≤ 125°C*) is applied. The response speed and shape varies with the overload level, input circuit, and rate of application. The current limit response will vary between simply settling to I_{OS}, or turnoff and controlled return to I_{OS}. Similar to the previous case, the TPS2001D limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS2001D thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation [($V_{IN} – V_{OUT}$) × I_{OS}] driving the junction temperature up. The device turns off when the junction temperature exceeds 135°C (minimum) while in current limit. The device remains off until the junction temperature cools 20°C and then restarts.

There are two kinds of current limit profiles typically available in TI switch products that are similar to the TPS2001D. Many older designs have an output I vs V characteristic similar to the plot labeled *Current Limit with Peaking* in Figure 20. This type of limiting can be characterized by two parameters, the current limit corner (I_{OC}), and the short circuit current (I_{OS}). I_{OC} is often specified as a maximum value. The TPS2001D family of parts does not present noticeable peaking in the current limit, corresponding to the characteristic labeled *Flat Current Limit* in Figure 20. This is why the I_{OC} parameter is not present in *Electrical Characteristics: –40°C ≤ T_J ≤ 125°C*.

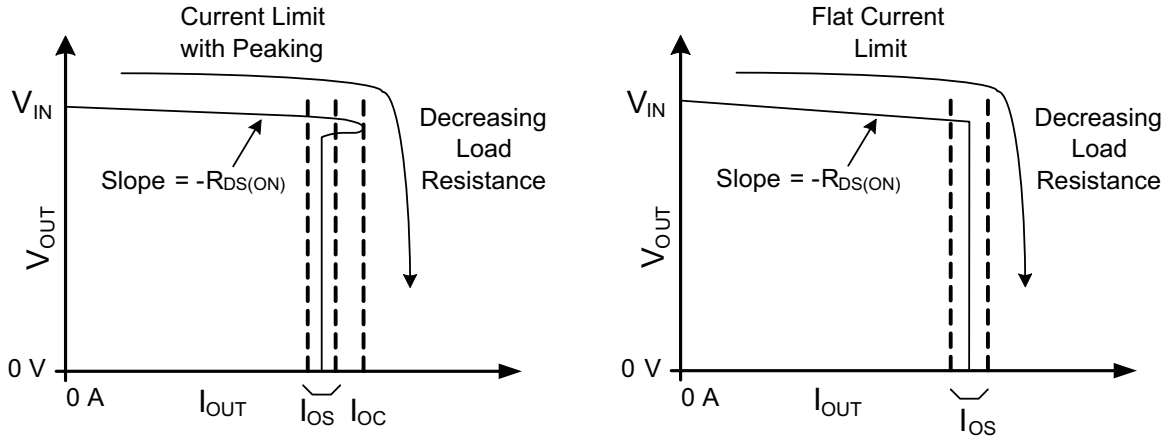


Figure 20. Current Limit Profiles

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Feature Description (continued)

8.3.5 $\overline{\text{FLT}}$

The $\overline{\text{FLT}}$ open-drain output is asserted (active low) during an overload or overtemperature condition. A 9-ms deglitch on both the rising and falling edges avoids false reporting at start-up and during transients. A current limit condition shorter than the deglitch period clears the internal timer upon termination. The deglitch timer does not integrate multiple short overloads and declare a fault. This is also true for exiting from a faulted state. An input voltage with excessive ripple and large output capacitance may interfere with operation of $\overline{\text{FLT}}$ around I_{OS} as the ripple drives the device in and out of current limit.

If the TPS2001D is in current limit and the overtemperature circuit goes active, $\overline{\text{FLT}}$ goes true immediately; however, the exiting this condition is deglitched. $\overline{\text{FLT}}$ is tripped just as the knee of the constant-current limiting is entered. Disabling the TPS2001D clears an active $\overline{\text{FLT}}$ as soon as the switch turns off. $\overline{\text{FLT}}$ is high impedance when the TPS2001D is disabled or in undervoltage lockout (UVLO).

8.3.6 Output Discharge

A 470-Ω (typical) output discharge dissipates stored charge and leakage current on OUT when the TPS2001D is in UVLO or disabled. The pulldown circuit loses bias gradually as V_{IN} decreases, causing a rise in the discharge resistance as V_{IN} falls towards 0 V. The output is be controlled by an external loadings when the device is in ULVO or disabled.

8.4 Device Functional Modes

There are no other functional modes.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS2001D current-limited power switch uses an N-channel MOSFET in applications requiring continuous load current. The device enters constant-current mode when the load exceeds the current limit threshold.

9.2 Typical Application

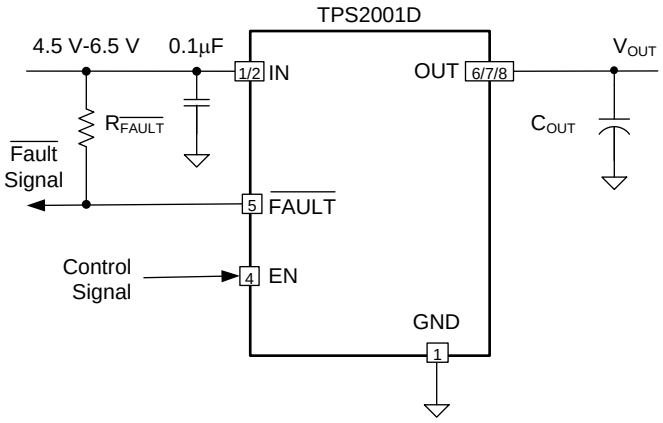


Figure 21. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the following input parameters:

1. The TPS2001D operates from a 5-V to ±0.5-V input rail.
2. What is the normal operation current, for example, the maximum allowable current drawn by portable equipment for USB 3.0 port is 900 mA, so the normal operation current is 900 mA, and the minimum current limit of power switch must exceed 900 mA to avoid false trigger during normal operation.
3. What is the maximum allowable current provided by up-stream power, the maximum current limit of power switch that must lower it to ensure power switch can protect the up-stream power when overload is encountered at the output of power switch.

9.2.2 Detailed Design Procedure

To begin the design process a few parameters must be decided upon. The designer must know the following:

1. Normal input operation voltage
2. Output continuous current
3. Maximum up-stream power supply output current

9.2.2.1 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, TI recommends placing a 0.1-µF or greater ceramic bypass capacitor between IN and GND, as close to the device as possible for local noise decoupling.

All protection circuits have the potential for input voltage overshoots and output voltage undershoots.

Typical Application (continued)

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power bus inductance and input capacitance when the IN terminal is high impedance (before turnon). Theoretically, the peak voltage is 2× the applied. The second cause is due to the abrupt reduction of output short-circuit current when the TPS2001D turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps; and, as the TPS2001D output is shorted. Applications with large input inductance (for example, connecting the evaluation board to the bench power-supply through long cables) may require large input capacitance to reduce the voltage overshoot from exceeding the absolute maximum voltage of the device. The fast current limit speed of the TPS2001D responding to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1 µF to 22 µF adjacent to the TPS2001D input aids in both speeding the response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5 V are permitted.

Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPS2001D has abruptly reduced OUT current. Energy stored in the inductance drives the OUT voltage down and potentially negative as it discharges. Applications with large output inductance (such as from a cable) benefit from use of a high-value output capacitor to control the voltage undershoot. When implementing USB standard applications, a 120-µF minimum output capacitance is required. Typically a 150-µF electrolytic capacitor is used, which is sufficient to control voltage undershoots. However, if the application does not require 120 µF of capacitance, and there is potential to drive the output negative, then TI recommends a minimum of 10-µF ceramic capacitance on the output. The voltage undershoot must be controlled to less than 1.5 V for 10 µs.

9.2.3 Application Curves

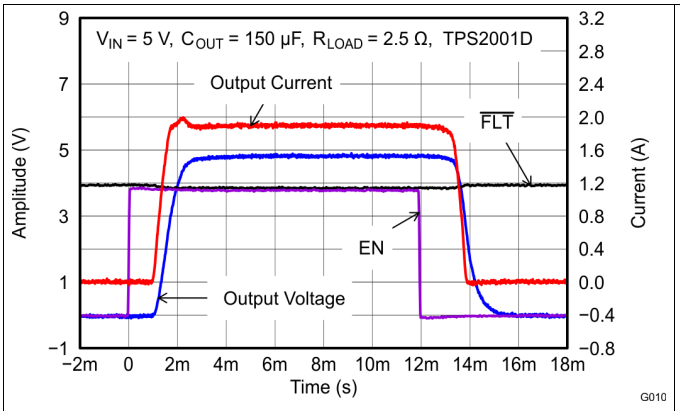


Figure 22. TPS2001D Turnon into 2.5 Ω

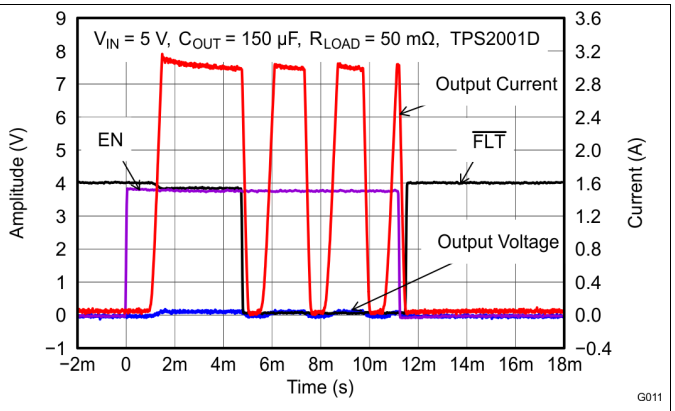


Figure 23. TPS2001D Enable into Short

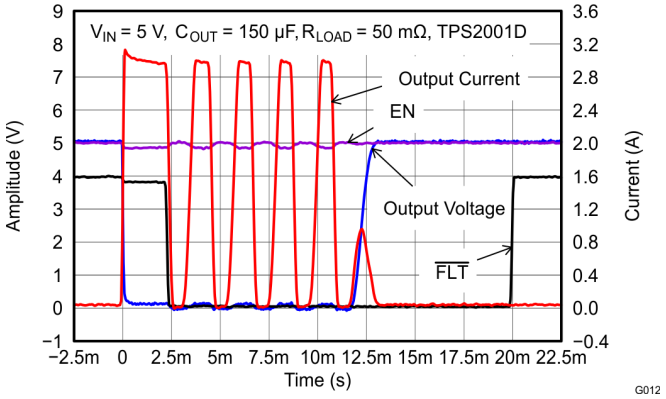


Figure 24. TPS2001D Pulsed Output Short

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10 Power Supply Recommendations

Design of the devices is for operation from an input voltage supply range of 4.5 V to 5.5 V. The current capability of the power supply should exceed the maximum current limit of the power switch.

11 Layout

11.1 Layout Guidelines

1. Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low inductance trace.
2. Place at least 10-µF low ESR ceramic capacitor near the OUT and GND pins, and make the connections using a low inductance trace.

11.2 Layout Example

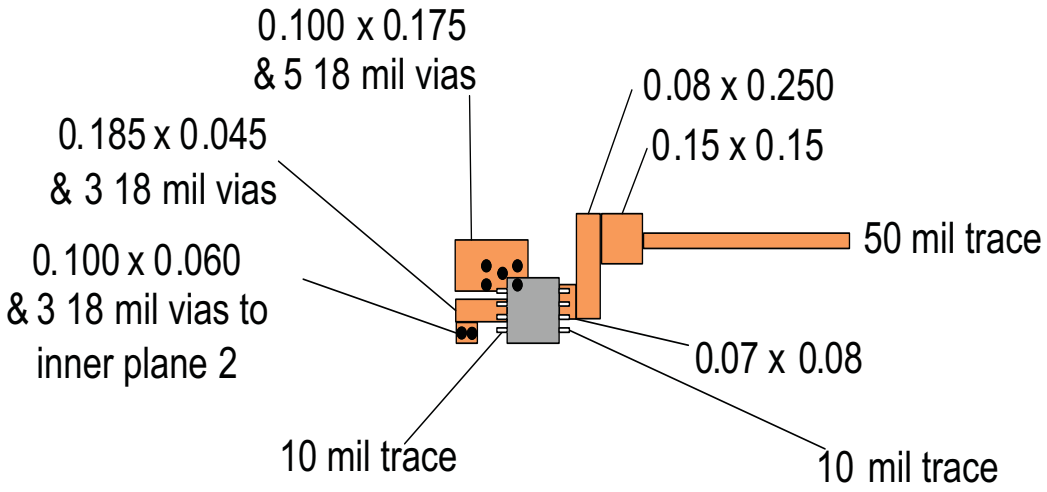


Figure 25. DGK Package PCB Layout Example

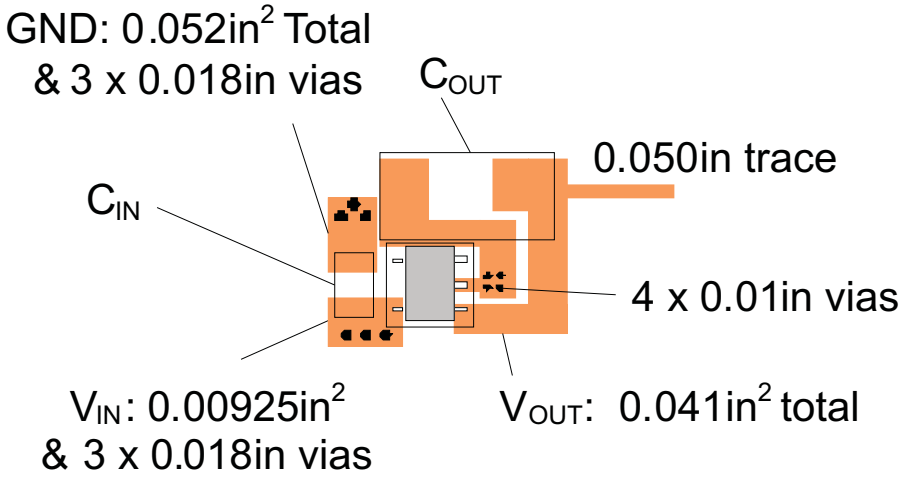


Figure 26. DBV Package PCB Layout Example

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11.3 Power Dissipation and Junction Temperature

It is good design practice to estimate power dissipation and maximum expected junction temperature of the TPS2001D. The system designer can control choices of package, proximity to other power dissipating devices, and printed-circuit board (PCB) design based on these calculations. These have a direct influence on maximum junction temperature. Other factors, such as airflow and maximum ambient temperature, are often determined by system considerations. It is important to remember that these calculations do not include the effects of adjacent heat sources, and enhanced or restricted air flow.

Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical. The lower junction temperatures achieved by soldering the pad improve the efficiency and reliability of both the TPS2001D part and the system. The following examples were used to determine the θ_{JA} Custom thermal impedances noted in *Thermal Information*. They were based on use of the JEDEC high-k circuit board construction (2 signal and 2 plane) with 4, 1-oz. copper weight, layers.

The θ_{JA} is 110.3°C/W. These values may be used in Equation 1 to determine the maximum junction temperature.

As shown in Equation 1, the following procedure requires iteration because power loss is due to the internal MOSFET $I^2 \times R_{DS(ON)}$, and $R_{DS(ON)}$ is a function of the junction temperature. As an initial estimate, use the $R_{DS(ON)}$ at 125°C from the *Typical Characteristics*, and the preferred package thermal resistance for the preferred board construction from the *Thermal Information* table.

$$T_J = T_A + ((I_{OUT}^2 \times R_{DS(ON)}) \times \theta_{JA}) \quad (1)$$

where

- I_{OUT} = rated OUT pin current (A)
- $R_{DS(ON)}$ = Power switch ON-resistance at an assumed T_J (Ω)
- T_A = Maximum ambient temperature (°C)
- T_J = Maximum junction temperature (°C)
- θ_{JA} = Thermal resistance (°C/W)

If the calculated T_J is substantially different from the original assumption, estimate a new value of $R_{DS(ON)}$ using the typical characteristic plot and recalculate.

If the resulting T_J is not less than 125°C, try a PCB construction or a package with lower θ_{JA}.

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12 器件和文档支持

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2001DDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1E6L
TPS2001DDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1E6L
TPS2001DDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1E6L
TPS2001DDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1E6L
TPS2001DDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1D6K
TPS2001DDGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1D6K
TPS2001DDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1D6K
TPS2001DDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1D6K

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

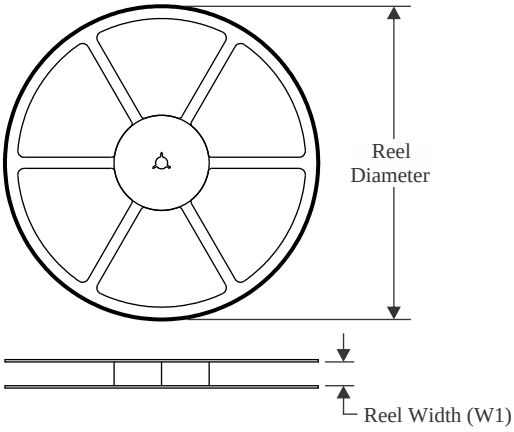
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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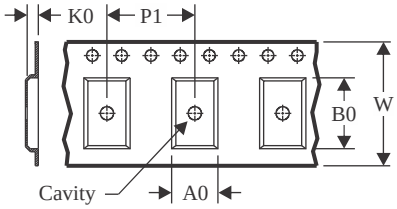
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

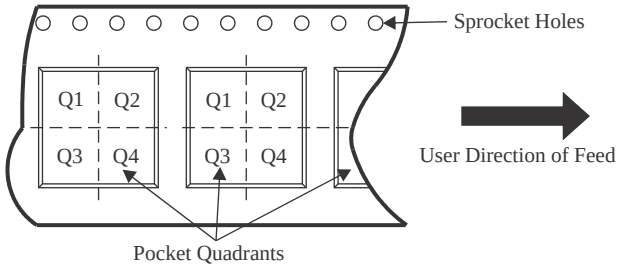


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

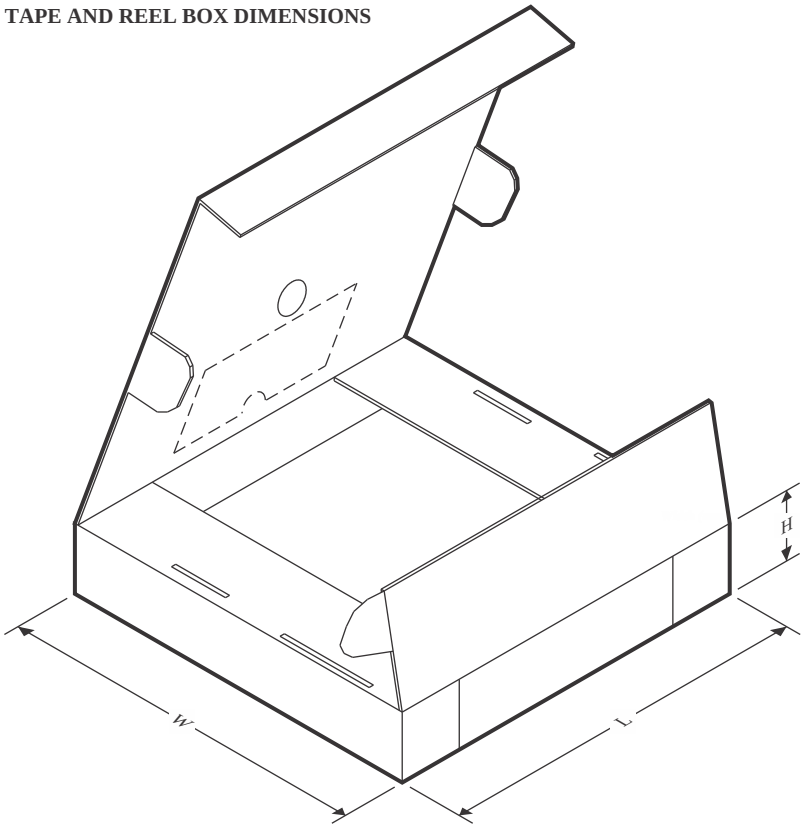
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2001DDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2001DDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2001DDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2001DDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2001DDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

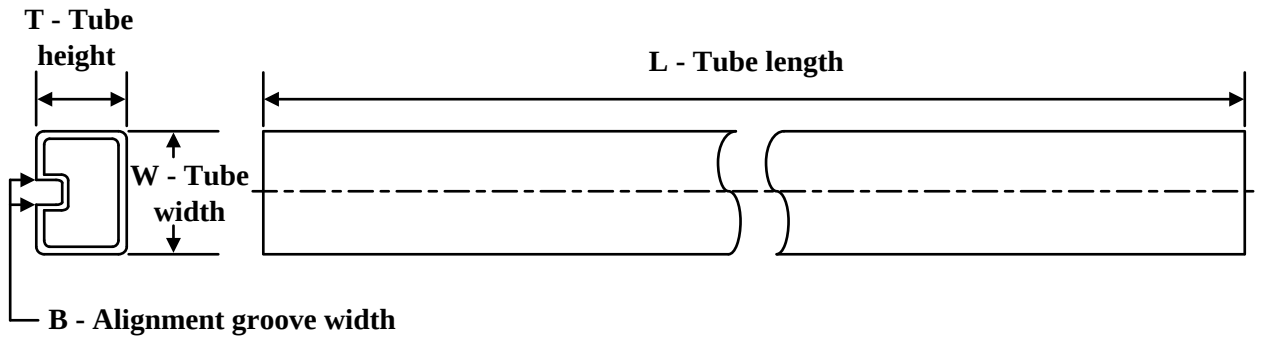
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2001DDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2001DDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2001DDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS2001DDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
TPS2001DDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

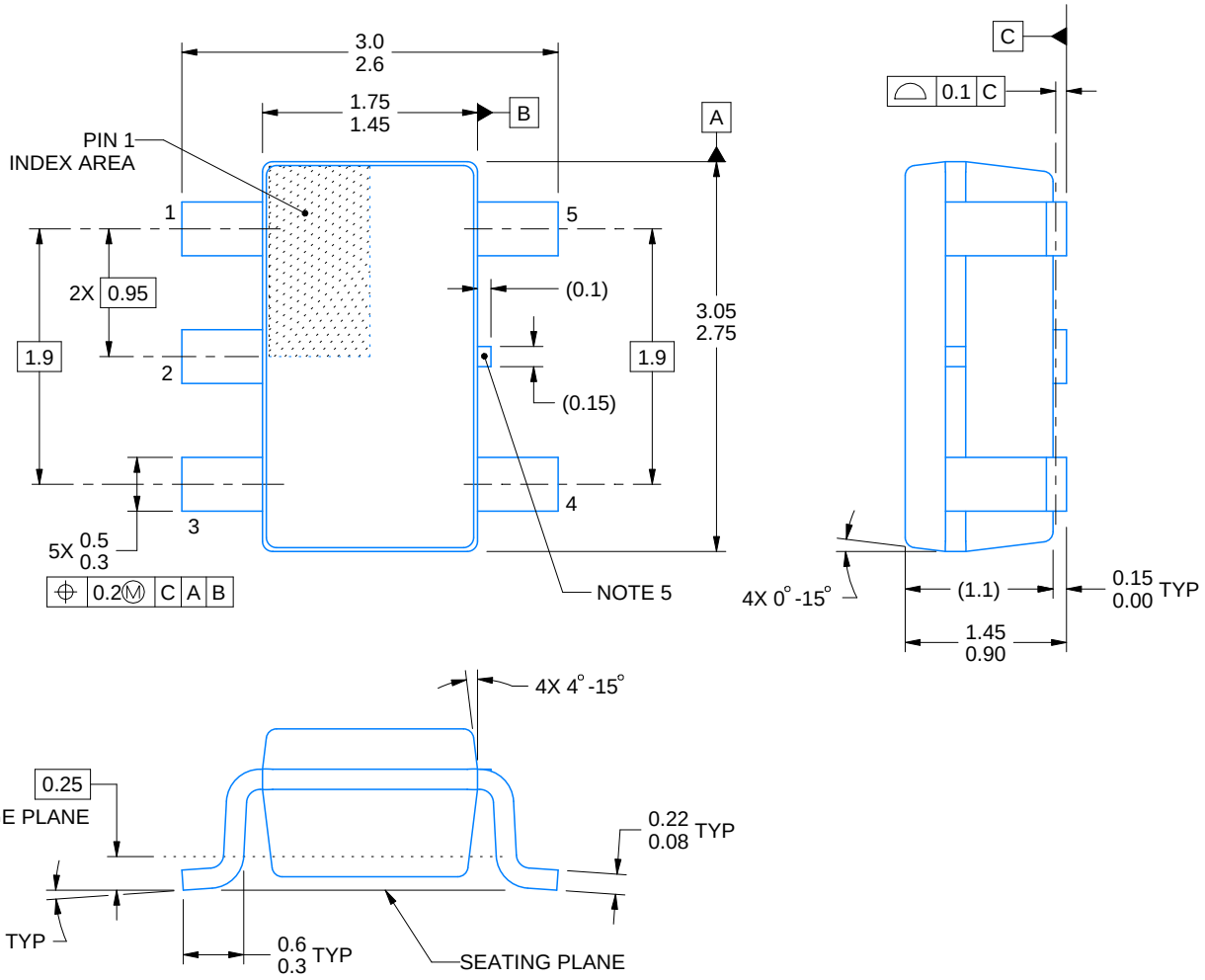
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2001DDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TPS2001DDGK.B	DGK	VSSOP	8	80	330	6.55	500	2.88

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

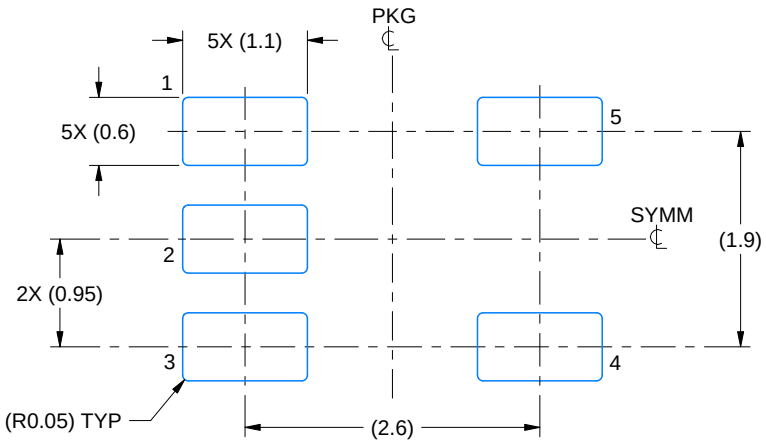
SMALL OUTLINE TRANSISTOR



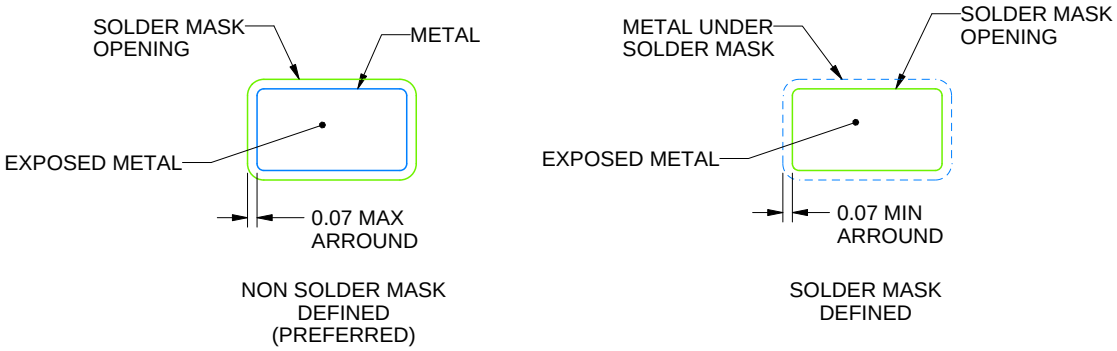
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

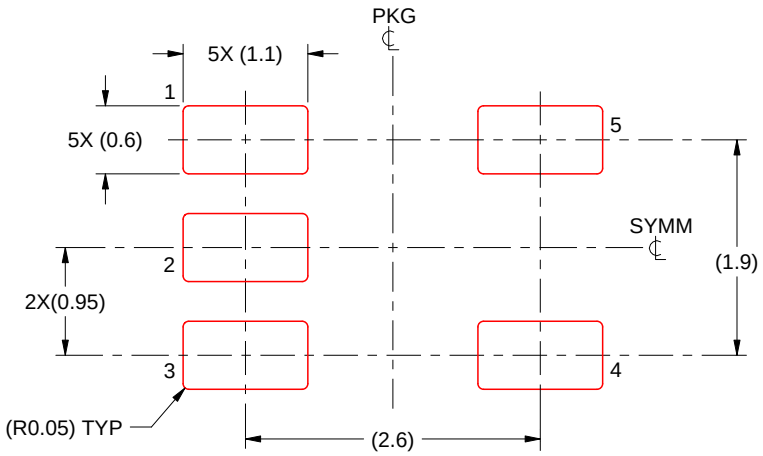


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

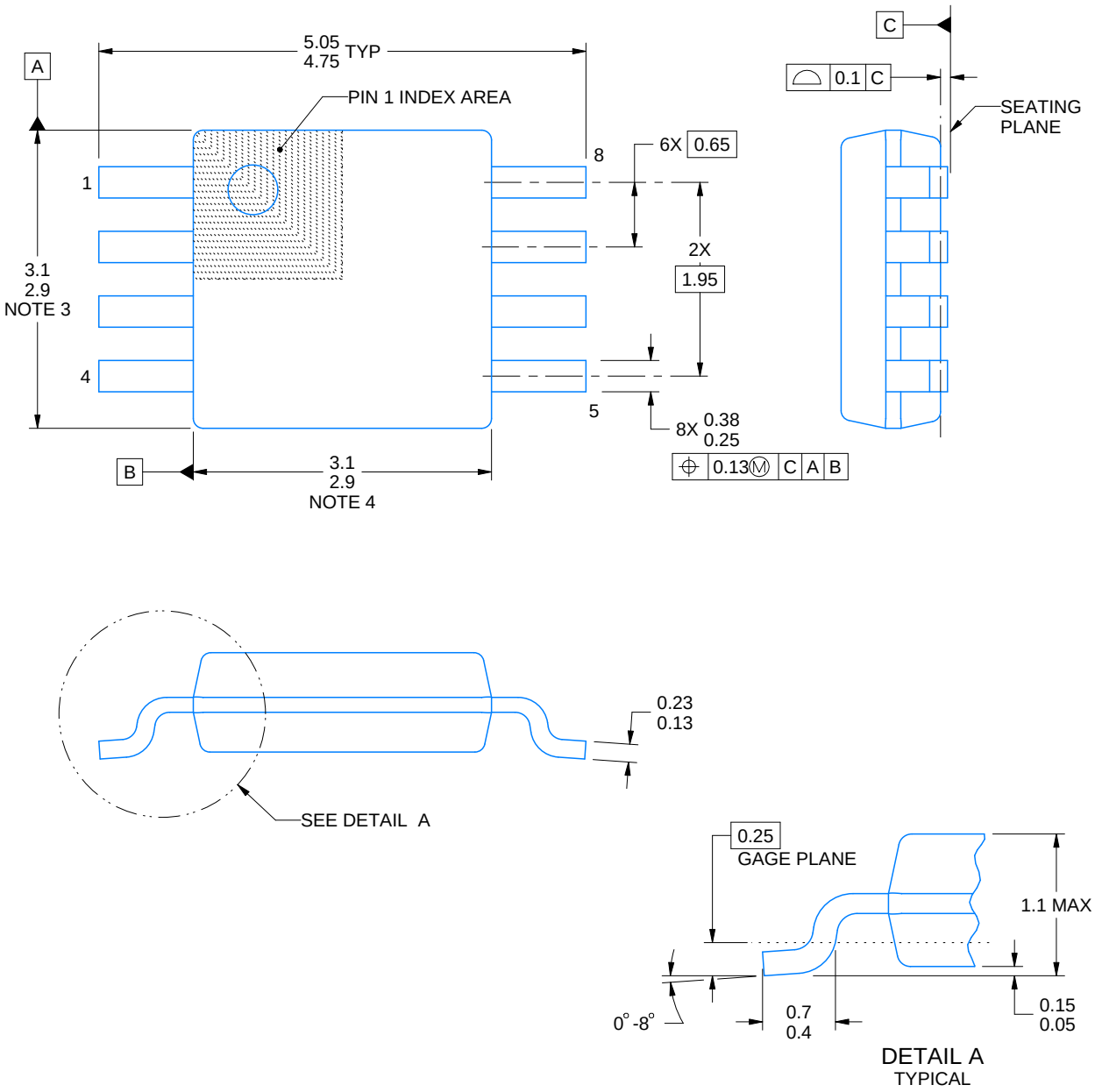
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

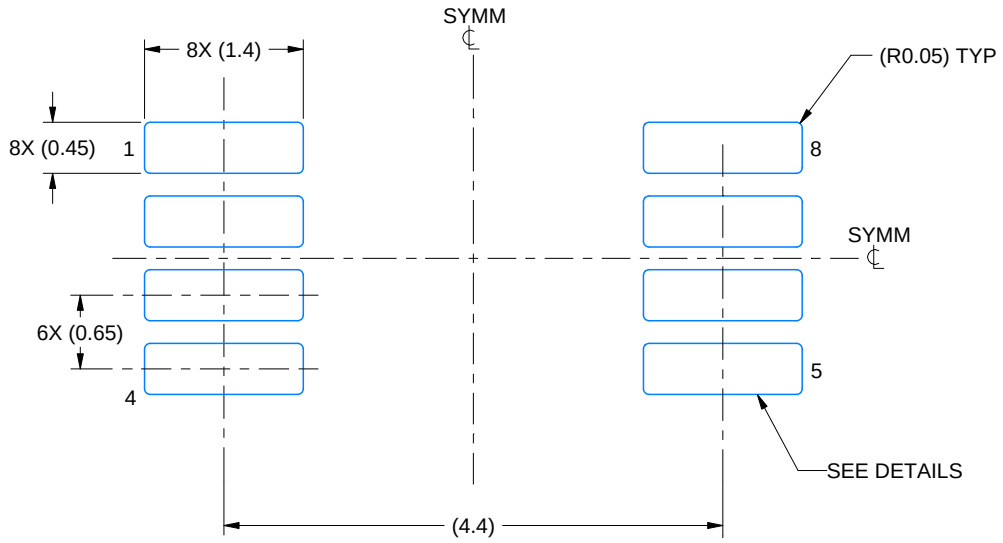
SMALL OUTLINE PACKAGE



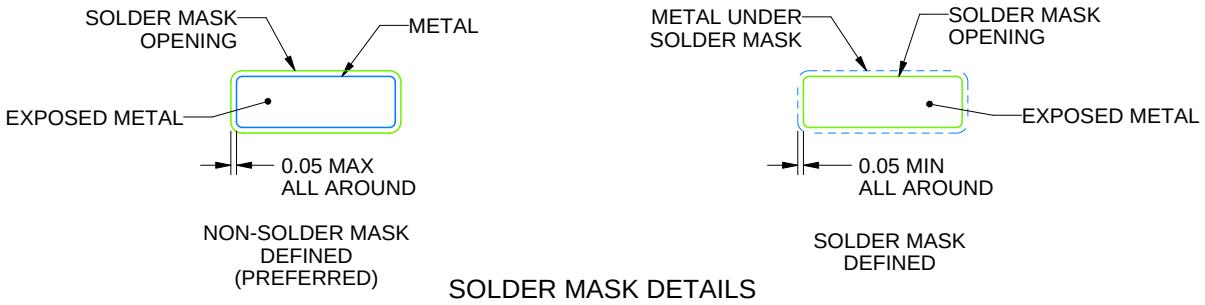
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

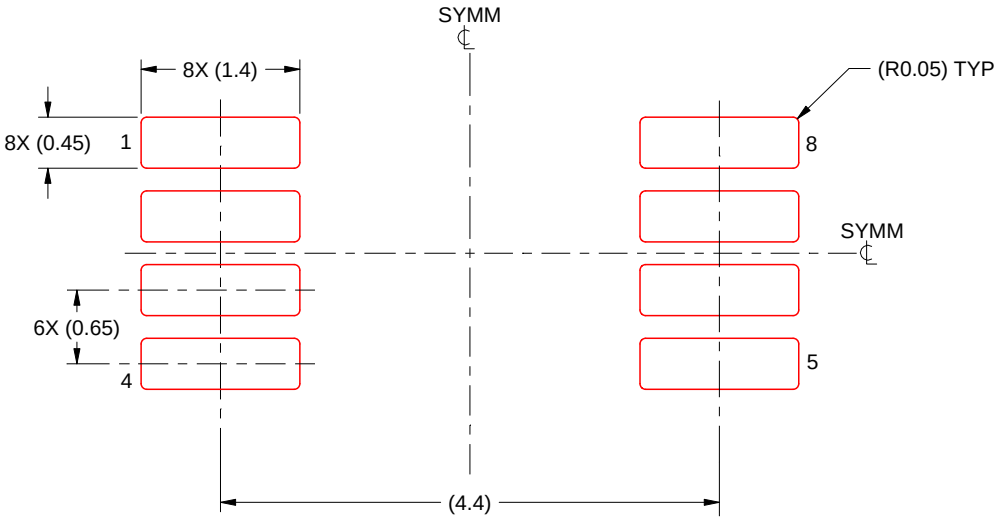


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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