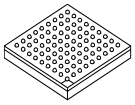
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MIMX8QX*n*AV*x*FZAC
MIMX8DX*n*AV*x*FZAC

i.MX 8QuadXPlus and 8DualXPlus Automotive and Infotainment Applications Processors



Package Information
21 x 21 mm package case outline
17 x 17 mm package case outline

Ordering Information
See Section 1.1Table 2 on page 5

1 Introduction

This data sheet contains specifications for the i.MX 8QuadXPlus and 8DualXPlus processors, which, along with the i.MX 8DualX processor , comprise the i.MX 8X Family (for i.MX 8DualX specifications, see *i.MX 8DualX Automotive and Infotainment Processors* [IMX8DXAEC]). The i.MX 8X processors consist of three to five Arm cores (two to four Arm Cortex®-A35 and one Cortex®-M4F). All devices include separate GPU and VPU subsystems as well as a failover-ready display controller. Advanced multicore audio processing is supported by the Arm cores and a high performance Tensilica® HiFi 4 DSP for pre- and post-audio processing as well as voice recognition. The i.MX 8X Family supports up to three displays with multiple display output options, including parallel, MIPI-DSI, and LVDS. Memory interfaces for this device include:

- LPDDR4 (no error correcting code [ECC])
- DDR3L (optional ECC)
- 2× Quad SPI or 1× Octal SPI (FlexSPI)
- eMMC 5.1, RAW NAND, and SD 3.0

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A wide range of peripheral I/Os such as CAN, parallel or MIPI CSI camera input, Gigabit Ethernet, USB 2.0 OTG, USB 3.0 (8QuadXPlus/8DualXPlus only), ADC, and PCIe 3.0 provide impressive flexibility.

The i.MX 8QuadXPlus/8DualXPlus processors offer numerous advanced features as shown in this table.

Table 1. i.MX 8QuadXPlus/8DualXPlus advanced features

Function	Feature
Multicore architecture provides 2×–4× Cortex-A35 and 1× Cortex-M4F cores	AArch64 for 64-bit support and new architectural features
	AArch32 for full backward compatibility with ARMv7
	Cortex-A35 cores support ARM virtualization extensions.
	Cortex-M4F cores for real-time applications
Graphics Processing Unit (GPU)	4× Vec4 shaders with 16 execution units optimized for higher performance
	Supports OpenGL 3.0, 2.1,; OpenGL ES 3.1, 3.0, 2.0, and 1.1; OpenCL 1.2 Full Profile and 1.1; OpenVG 1.1; and Vulkan
	High-performance 2D Blit Engine
Video Processing Unit (VPU)	H.265 decode (4Kp30)
	H.264 decode (4Kp30)
	WMV9/VC-1 imple decode
	MPEG 1 and 2 decode
	AVS decode
	MPEG4.2 ASP, H.263, Sorenson Spark decode
	Divx 3.11 including GMC decode
	ON2/Google VP6/VP8 decode
	RealVideo 8/9/10 decode
	JPEG and MJPEG decode
	H.264 encode (1080p30)
Tensilica HiFi 4 DSP for pre- and post-processing	640 MHz Fixed-point and vector-floating-point support 32 KB instruction cache, 48 KB data cache, 512 KB SRAM (448 KB of OCRAM and 64 KB of TCM)

Table 1. i.MX 8QuadXPlus/8DualXPlus advanced features (continued)

Function	Feature
Memory	32-bit LPDDR4 @1200 MHz 40-bit DDR3L @933 MHz (ECC option)
	1× Quad SPI which can be used to connect to an FPGA
	2× Quad SPI or 1× Octal SPI (FlexSPI) for fast boot from SPI NOR flash
	2× SD 3.0 card interfaces (note: if eMMC is used, then 1× SD 3.0 available in IOMUX)
	1× eMMC5.1/SD3.0 (note: use of eMMC will restrict SD card availability to 1× SD 3.0 due to IOMUX restrictions)
	RAW NAND (62-bit ECC support via BCH-62 module)
Display Controller	Supports up to 3 independent displays (2× MIPI or LVDS + 1× Parallel)
	Up to 18-layer composition
	Complementary 2D blitting engines and online warping functionality
	Integrated Failover Path (SafeAssure) to ensure display content stays valid even in event of a software failure
Display I/O	Two MIPI-DSI/LVDS Combo PHYs (each up to 1080p60): Each single PHY can either be a 4-lane MIPI-DSI or a 4-lane channel LVDS interface for a total of 2 display interfaces. In combination, the two PHYs can be configured to be a single dual-channel LVDS interface. 1× 24-bit parallel LCD up to 720p60 (DDR bandwidth might limit the available resolution).
Camera I/O and video	1× MIPI-CSI with 4-lanes
	1× 8-bit/10-bit parallel CSI
Security	Advanced High Assurance Boot (AHAB) secure & encrypted boot
	Random Number Generator with a high-quality entropy source generator and Hash_DRBG (based on hash functions)
	RSA up to 4096, Elliptic Curve up to 1023
	AES-128/192/256, DES, 3DES, MD5, SHA-1, SHA-224/256/384/512
	Dedicated Security Controller for Flashless SHE and HSM support, Trustzone, RTIC
	Built-in ECDSA/DSA protocol support
	See the security reference manual for this chip for a full list of security features.
	10× tamper pins (up to 5 active or 10 passive)
	Voltage and Temperature tamper detection
	64 kB Secure RAM (can be erased via tamper detection)

System Control	• 2× I^2C tightly coupled with Cortex-M4 cores (1× per Cortex M4F core)
	  • The tightly coupled M4 I^2C ports cannot be used for general-purpose use
	• System Control Unit (SCU):
	  • Power control, clocks, reset
	  • Boot ROMs
	  • PMIC interface
	  • Resource Domain Controller

Table 1. i.MX 8QuadXPlus/8DualXPlus advanced features (continued)

Function	Feature
I/O	1× PCIe 3.0 (1-lane) with L1 substate support
	1× USBOTG 3.0 with PHY—USB 3.0 can be used as USB 2.0
	1× USBOTG 2.0 (with PHY)
	2× 1Gb Ethernet with AVB (can be used as 10/100 Mbps ENET with AVB)
	3× CAN/CAN-FD
	1× Media Local Bus (MLB25/50)
	6× UARTs: • 4× UARTs (3× with hardware flow control) • 1× UART tightly coupled with Cortex-M4F cores • 1× SCU UART (Note: SCU UART is dedicated to the SCU and not available for general use)
	10× I²C (note that there are two types of I^2C: High-speed I^2C ports with DMA support, and low-speed I^2C ports with no DMA support, which are used in conjunction with a specific PHY interface—for example, for touchscreen): • 4× I2C: High Speed, DMA support • 4× I2C: Low Speed, no DMA support • 1× I2C: PMIC control (dedicated) • 1× I2C: Cortex M4F (dedicated) Note: I2C ports associated with a PHY (e.g. MIPI DSI) can be used generally but require the PHY to be powered on even if the PHY interface itself is not used.
	4× SAI (SAI0 and SAI1 are transmit/receive; SAI2 and SAI3 are receive only)
	1× Enhanced Serial Audio Interface (ESAI)
	2× ASRC (Asynchronous Sample Rate Converter) (note: no I/O signals are directly connected to this module)
	1× SPDIF (Tx and Rx)
	1× 6-channel ADC converter
	3.3 V/1.8 V GPIO
	4× PWM channels
	1× 6×8 KPP (Key Pad Port)
	1× MQS (Medium Quality Sound)
	4× SPI
Packaging	Case FCPBGA 21 x 21 mm, 0.8 mm pitch
	Case FCPBGA 17 x 17 mm, 0.8 mm pitch

1.1 Ordering Information

For ordering information, contact an NXP representative at nxp.com.

Table 2. i.MX 8QuadXPlus Orderable part numbers

Part Number	Options	Cortex-A35 Speed Grade	Cortex-M4F Speed Grade	Temperature Grade	Package
MiMX8QX6AVLFZAC	With GPU, VPU, DSP, 24-bit Parallel LCD	1.2 GHz	264 MHz	Automotive	21 mm X 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MiMX8QX5AVLFZAC	With GPU, VPU, 24-bit Parallel LCD	1.2 GHz	264 MHz	Automotive	21 mm X 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MiMX8QX2AVLFZAC	With DSP. Features not supported: GPU, Display Controller, VPU, 24-bit Parallel LCD	1.2 GHz	264 MHz	Automotive	21 mm X 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MiMX8QX1AVLFZAC	Features not supported: GPU, Display Controller, VPU, 24-bit Parallel LCD, DSP	1.2 GHz	264 MHz	Automotive	21 mm X 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MiMX8QX2AVOFZAC	With DSP, 16-bit DDR. Features not supported: GPU, USB3, Display Controller, VPU, 24-bit Parallel LCD, ECC on DDR3	1.2 GHz	264 MHz	Automotive	17 mm X 17 mm, 0.8 mm pitch, FCPBGA (lidded)
MiMX8QX1AVOFZAC	With 16-bit DDR. Features not supported: GPU, USB3, Display Controller, VPU, 24-bit Parallel LCD, ECC on DDR3, DSP	1.2 GHz	264 MHz	Automotive	17 mm X 17 mm, 0.8 mm pitch, FCPBGA (lidded)

Table 3. i.MX 8DualXPlus Orderable part numbers

Part Number	Options	Cortex-A35 Speed Grade	Cortex-M4F Speed Grade	Temperature Grade	Package
MiMX8DX6AVLFZAC	With GPU, VPU, DSP, 24-bit Parallel LCD	1.2 GHz	264 MHz	Automotive	21 mm X 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MiMX8DX5AVLFZAC	With GPU, VPU, 24-bit Parallel LCD	1.2 GHz	264 MHz	Automotive	21 mm X 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MiMX8DX2AVLFZAC	With DSP. Features not supported: GPU, Display Controller, VPU, 24-bit Parallel LCD	1.2 GHz	264 MHz	Automotive	21 mm X 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MiMX8DX1AVLFZAC	Features not supported: GPU, Display Controller, VPU, 24-bit Parallel LCD, DSP	1.2 GHz	264 MHz	Automotive	21 mm X 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MiMX8DX2AVOFZAC	With DSP, 16-bit DDR. Features not supported: GPU, USB3, Display Controller, VPU, 24-bit Parallel LCD, ECC on DDR3	1.2 GHz	264 MHz	Automotive	17 mm X 17 mm, 0.8 mm pitch, FCPBGA (lidded)
MiMX8DX1AVOFZAC	With 16-bit DDR. Features not supported: GPU, USB3, Display Controller, VPU, 24-bit Parallel LCD, ECC on DDR3, DSP	1.2 GHz	264 MHz	Automotive	17 mm X 17 mm, 0.8 mm pitch, FCPBGA (lidded)

1.2 System Controller Firmware (SCFW) Requirements

The i.MX 8 and 8X families require a minimum SCFW release version for correct operation and to prevent potential reliability issues.

The SCFW is released as part of a Board Support Package (e.g. Linux, Android) which may vary in version number for a specific BSP.

For example, NXP Yocto Linux release 4.14.98_2.3.0 contains SCFW version 1.3.0, NXP Yocto Linux release 4.14.98_2.0.0 GA contains SCFW version 1.2.10, whereas NXP Yocto Linux release 4.14.78_1.0.0GA contains SCFW version 1.1.10.

The released SCFW version associated within each BSP is the minimum version required to correctly support the wider BSP functionality.

Customers should always check that they are using the specific SCFW binary delivered within their chosen BSP release. Customers should not mix newer BSP versions with older revisions of the SCFW.

1.3 Package options

This data sheet lists and describes the superset of features in the i.MX 8X family of parts. The feature lists are subsets and differ between packages. This table describes the differences in feature availability per package.

Table 4. Feature differences per package[1]

Function	21 x 21 mm 0.8 mm FCPBGA	17 x 17 mm 0.8 mm FCPBGA	Comment
DRAM	32-bit LPDDR4, and 40-bit DDR3L with optional ECC	16-bit LPDDR4 and 16-bit DDR3L (no ECC)	Due to the reduced DDR interface on the 17 x 17 package, the maximum DDR density supported is also reduced.
MIPI-CSI	1 (4-lane plus dedicated GPIO)	1 (4-lane interface and MIPI_CSI0_MCLK_OUT only)	MIPI_CSI0_I2C0, MIPI_CSI0_GPIO0_00 and MIPI_CSI0_GPIO0_01 balls removed
MIPI-DSI	2 (4-lane plus dedicated GPIO)	2 (4-lane interface and MIPI_DSIx_I2C0 only)	MIPI_DSIx_GPIO0_00 and MIPI_DSI*x*_GPIO0_01 balls removed (*x* is 0 or 1)
SAI	4	2	SAI0 and SAI1 (RX only) balls removed NOTE: By removing these interfaces the LCDIF is reduced from 24-bit to 18-bit maximum
SPI	4	3	SPI2 balls removed
USB	USB3 (SS3 plus OTG2) and OTG1	OTG1 only	SS3 and OTG2 balls removed
USDHC	2	1	USDHC1 balls removed **Note:** Boot from SD not supported in 17x17 packages

[1] Alternate IOMUX options may exist to replace some of the removed functionality, such as SAI0, SAI1 and SPI2; however, that will place different restrictions on the overall IOMUX capabilities of the smaller package parts.

1.4 Related resources

Table 5. Related resources

Type	Description
Reference manual	The *i.MX 8DualX/8DualXPlus/8QuadXPlus Applications Processor Reference Manual* (IMX8DQXPRM) contains a comprehensive description of the structure and function (operation) of the SoC.
Data sheet	This data sheet includes electrical characteristics and signal connections.
Chip Errata	The chip mask set errata provides additional and/or corrective information for a particular device mask set.
Package drawing	Package dimensions are provided in Section 6, “Package information and contact assignments"."
Hardware guide	Contact an NXP representative for access.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 8QuadXPlus/8DualXPlus processor system.

2.1 Block Diagram

The following figure shows the functional modules in the processor system.

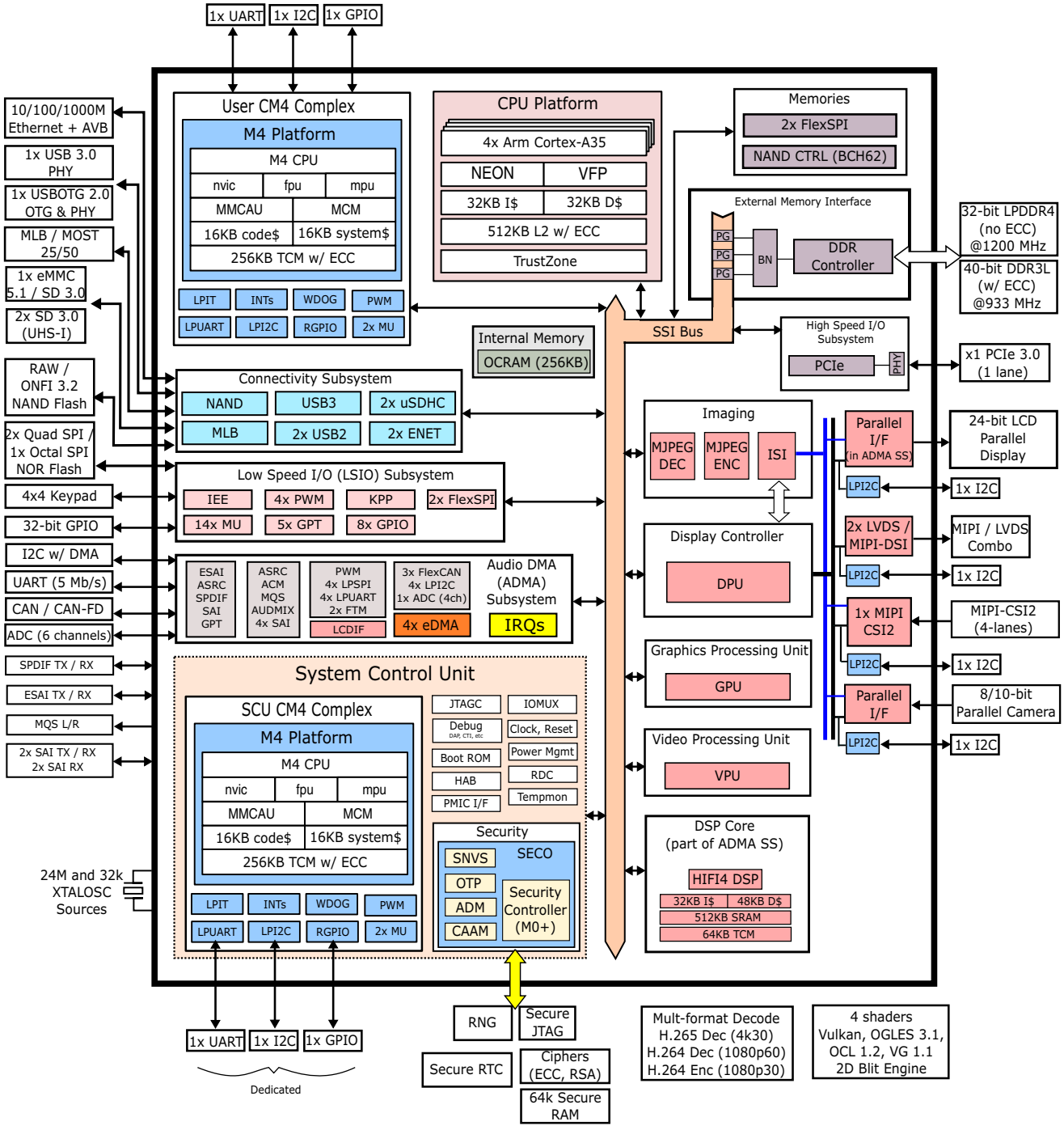


Figure 1. i.MX 8QuadXPlus/8DualXPlus System Block Diagram

3 Modules List

The i.MX 8QuadXPlus/8DualXPlus processors contain a variety of digital and analog modules. This table describes the processor modules in alphabetical order.

Table 6. i.MX 8QuadXPlus/8DualXPlus modules list

Block Mnemonic	Block Name	Brief Description
ADC	Analog-to-Digital Converter	The analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within a SoC.
APBH-DMA	NAND Flash and BCH ECC DMA Controller	The AHB-to-APBH bridge provides the chip with a peripheral attachment bus running on the AHB's HCLK, which includes the AHB-to-APB PIO bridge for a memory-mapped I/O to the APB devices, as well as a central DMA facility for devices on this bus and a vectored interrupt controller for the Arm core.
A35	Arm (CPU1)	2–4x Cortex-A35 CPUs with a 32KB L1 instruction cache and a 32 KB data cache. The CPUs share a 512 KB L2 cache.
ASRC	Asynchronous Sample Rate Converter	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
BCH-62	Binary-BCH ECC Processor	The BCH62 module provides up to 62-bit ECC for NAND Flash controller (GPMI2)
CAAM	Cryptographic Accelerator and Assurance Module	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). CAAM also implements a Secure Memory mechanism. In this device the security memory provided is 64 KB.
CTI	Cross Trigger Interface	CTI sends signals across the chip indicating that debug events have occurred. It is used by features of the Coresight infrastructure.
CTM	Cross Trigger Matrix	Cross Trigger Matrix IP is used to route triggering events between CTIs.
DAP	Debug Access Port	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains.
DC	Display Controller	Dual display controller

DDR Controller	DRAM Controller	• Memory types: LPDDR4 (no ECC) and DDR3L (ECC option)
		• One channel of 32-bit memory:
		  • LPDDR4 up to 1.2 GHz
		  • DDR3L up to 933MHz

DPR	Display/Prefetch/ Resolve	The DPR prefetches data from memory and converts the data to raster format for display output. Raster source buffers can also be prefetched unconverted. The resolve process supports graphics and video formatted tile frame buffers and converts them to raster format. Embedded display memory is used as temporary storage for data which is sourced by the display controller to drive the display.

Table 6. i.MX 8QuadXPlus/8DualXPlus modules list (continued)

Block Mnemonic	Block Name	Brief Description
DTCP	Digital Transport Content Protection	Provides encryption function according to Digital Transmission Content Protection standard for traffic over MLB25/50.

eDMA	Enhanced Direct Memory Access	• 4× eDMA with a total of 96 channels (note: all channels are not assigned; see the product reference manual for more information):
		  • 2× instances with 32 channels each
		  • 2× instances with 16 channels each
		• Programmable source, destination addresses, transfer size, plus support for enhanced addressing modes
		• Internal data buffer, used as temporary storage to support 64-byte burst transfers, one outstanding transaction per DMA controller.
		• Transfer control descriptor organized to support two-deep, nested transfer operations
		• Channel service request via one of three methods:
		  • Explicit software initiation
		  • Initiation via a channel-to-channel linking mechanism for continuous transfers
		  • Peripheral-paced hardware requests (one per channel)
		• Support for fixed-priority and round-robin channel arbitration
		• Channel completion reported via interrupt requests
		• Support for scatter/gather DMA processing
		• Support for complex data structures via transfer descriptors
		• Support to cancel transfers via software or hardware
		• Each eDMA instance can be uniquely assigned to a different resource domain, security (TZ) state, and virtual machine
		• In scatter-gather mode, each transfer descriptor's buffers can be assigned to different SMMU translation

ENET	Ethernet Controller	2× 1 Gbps Ethernet + AVB (Audio Video Bridging, IEEE 802.1Qav)
ESAI	Enhanced Serial Audio Interface	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FTM	FlexTimer	Provides input signal capture and PWM support
FlexCAN	Flexible Controller Area Network	Communication controller implementing the CAN with Flexible Data rate (CAN FD) protocol and the CAN protocol according to the CAN 2.0B protocol specification.

Table 6. i.MX 8QuadXPlus/8DualXPlus modules list (continued)

Block Mnemonic	Block Name	Brief Description
FlexSpi (Quad SPI/Octal SPI)	Flexible Serial Peripheral Interface	• Flexible sequence engine to support various flash vendor devices, including HyperBus™ devices: • Support for FPGA interface • Single, dual, quad, and octal mode of operation. • DDR/DTR mode wherein the data is generated on every edge of the serial flash clock. • Support for flash data strobe signal for data sampling in DDR and SDR mode. • Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.
GIC	Generic Interrupt Controller	The GIC-500 handles all interrupts from the various subsystems and is ready for virtualization.
GPIO	General Purpose I/O Modules	Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Media Interface	The GPMI module supports up to 8× NAND devices. 62-bit ECC (BCH) for NAND Flash controller (GPMI). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU	Graphics Processing	1× GC7000Lite with 4x Vec4 shader cores (16 execution units)
HiFi 4 DSP	Audio Processor	A highly optimized audio processor geared for efficient execution of audio and voice codecs and pre- and post-processing modules to offload the Arm core.
I^2C	I^2C Interface	I^2C provides serial interface for external devices.

IEE		• Supports direct encryption and decryption of FlexSPI memory type
		• Provides decryption services (lower performance) for DRAM traffic
		• Supports I/O direct encrypted storage and retrieval
		• Support for a number of cryptographic standards:
		  • 128/256-bit AES Encryption (AES-CTR, AES-XTS mode options)
		• Multiple keys supported:
		  • Loaded via secure key channel from security block
		  • Key selection is per access and based on source of transaction

IOMUXC	IOMUX Control	This module enables flexible I/O multiplexing. Each I/O pad has default and several alternate functions. The alternate functions are software configurable.
JPEG/dec	MJPEG engine for decode	Provides up to 4-stream decoding in parallel.
JPEG/enc	MJPEG engine for encode	Provides up to 4-stream encoding in parallel.

Table 6. i.MX 8QuadXPlus/8DualXPlus modules list (continued)

Block Mnemonic	Block Name	Brief Description
KPP	Key Pad Port	The Keypad Port (KPP) is a 16-bit peripheral that can be used as a 4 x 4 keypad matrix interface or as general purpose input/output (I/O).
LPIT-1 LPIT-2	Low-Power Periodic Interrupt Timer	Each LPIT is a 32-bit “set and forget” timer that starts counting after the LPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
LPSPI 0–3	Configurable SPI	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
M4F	Arm (CPU3)	• Cortex-M4F core • AHB LMEM (Local Memory Controller) including controllers for TCM and cache memories • 256 KB tightly coupled memory(TCM) (128 KB TCMU, 128 KB TCML) • 16 KB Code Bus Cache • 16 KB System Bus Cache • ECC for TCM memories and parity for code and system caches • Integrated Nested Vector Interrupt Controller (NVIC) • Wakeup Interrupt Controller (WIC) • FPU (Floating Point Unit) • Core MPU (Memory Protection Unit) • Support for exclusive access on the system bus • MMCAU (Crypto Acceleration Unit) • MCM (Miscellaneous Control Module)
MIPI CSI-2	MIPI CSI-2 Interface	The MIPI CSI-2 IP provides MIPI CSI-2 standard camera interface ports. The MIPI CSI-2 interface supports up to 1.5 Gbps for up to 4 data lanes
MIPI-DSI/LVDS	MIPI DSI/LVDS Combo interface	The MIPI DSI IP provides DSI standard display serial interface with 4 data lines. The DSI interface supports 80 Mbps to 1.05 Gbps speed per data lane. The LVDS is a high-performance 2-channel serializer that interfaces with LVDS displays. Note: This is a combination PHY interface. It includes the digital logic and physical interface pins for both MIPI DSI (4 data lanes) and LVDS (4 differential pairs plus one for clock). The interface can be pinned out either as MIPI DSI or as LVDS. However, it does not allow for simultaneous use on one interface
MLB	MediaLB	Media local bus interface module that provides a link to a MOST® data network, using the standardized MediaLB protocol. Supports 3-wire interface (MLB25, MLB50).
MQS	Medium Quality Sound	Medium Quality Sound (MQS) is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
OCOTP_CTRL	OTP Controller	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent nonvolatility.

Table 6. i.MX 8QuadXPlus/8DualXPlus modules list (continued)

Block Mnemonic	Block Name	Brief Description
OCRAM	On-Chip Memory Controller	The On-Chip Memory controller (OCRAM) module is designed as an interface between the system's AXI bus and the internal (on-chip) SRAM memory module. The OCRAM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus.

Parallel CSI	Parallel CSI interface	The Parallel Port Capture Subsystem interfaces to Parallel CSI sensors and includes the following features:
		• Configurable interface logic to support the most commonly used parallel CMOS sensors
		• Configurable master clock output to drive external sensor (24 MHz nominal)
		• Up to 150 MHz input clock from sensor
		• Input data formats supported:
		  • 8-bit/10-bit BT.656
		  • 8-bit/24-bit data port for RGB, YCbCr, and YUV data input
		  • 8-bit/12-bit/10-bit/16-bit data port for Bayer data input
		Note: For some formats a single pixel is sent per clock, for others two or three are sent per clock.

PCIe	PCI Express 3.0	The PCIe IP provides PCI Express Gen 3.0 functionality .
PRG	Prefetch/Resolve Gasket	The PRG is a gasket which translates system memory accesses to local display RTRAM accesses for display refresh. It works with the DPR to complete the prefetch and resolving operations needed to drive the display.
PWM	Pulse Width Modulation	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4×16 data FIFO to generate square waveforms.
RAM 64 KB Secure RAM	Secure/non-secure RAM	Secure/non-secure Internal RAM, interfaced through the CAAM.
RAM 256 KB	Internal RAM	Internal RAM, which is accessed through OCRAM memory controllers.
RNG	Random Number Generator	The purpose of the RNG is to generate cryptographically strong random data. It uses a true random number generator (TRNG) and a pseudo-random number generator (PRNG) to achieve true randomness and cryptographic strength. The RNG generates random numbers for secret keys, per message secrets, random challenges, and other similar quantities used in cryptographic algorithms.
SAI	I2S/SSI/AC97 Interface	The SAI module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.
SECO	Security Controller	Core and associated memory and hardware responsible for key management.
SJC	Secure JTAG Controller	The SJC provides the JTAG interface, which is compatible with JTAG TAP standards, to internal logic. This device uses JTAG port for production, testing, and system debugging. Additionally, the SJC provides BSR (Boundary Scan Register) standard support, which is compatible with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.

Table 6. i.MX 8QuadXPlus/8DualXPlus modules list (continued)

Block Mnemonic	Block Name	Brief Description
SNVS	Secure Non-Volatile Storage	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	The Sony/Philips Digital Interface (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio. The SPDIF transceiver allows the handling of both SPDIF channel status (CS) and User (U) data and includes a frequency measurement block that allows the precise measurement of an incoming sampling frequency.
TEMPMON	Temperature Monitor	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed; therefore, the read-out value may not be the reflection of the temperature value for the entire die.
UART	UART Interface	• High-speed TIA/EIA-232-F compatible, up to 5.0 Mbps • Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s) • 9-bit or Multidrop mode (RS-485) support (automatic slave address detection) • 7, 8, 9, or 10-bit data characters (7-bits only with parity) • 1 or 2 stop bits • Programmable parity (even, odd, and no parity) • Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
USB3/USB2		The USB3/USB2 OTG module has been specified to perform USB 3.0 dual role and USB 2.0 On-The-Go (OTG) compatible with the USB 3.0, and USB 2.0 specification with OTG supplementary specifications. This controller supports twoindependent USB cores (1× USB3.0 dual-role, 1× USB2.0 OTG) and includes the PHY and I/O interfaces to support this operation. The full pinout of the USB 3.0 controller includes the signaling for both USB 3.0 and USB 2.0. This does not mean there is a separate USB 2.0 controller that can be used independently and simultaneously with USB 3.0. This device has an additional separate, independent USB 2.0 OTG controller which can be used simultaneously with this USB 3.0. Specific features requested for this updated module: • Super Speed (5 Gbps), High Speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps) • Fully compatible with the USB 3.0 specification (backward compatible with USB 2.0) • Fully compatible with the USB On-The-Go supplement to the USB 2.0 specification • Hardware support for OTG signaling • Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) implemented in hardware, which can also be controlled by software

Table 6. i.MX 8QuadXPlus/8DualXPlus modules list (continued)

Block Mnemonic	Block Name	Brief Description
USBOH		The USBOH module has been specified which performs USB 2.0 On-The-Go (OTG) and USB 2.0 Host functionality compatible with the USB 2.0 with OTG supplement specification. This controller supports one independent USB core (1× USB2.0 OTG) and includes the PHY and I/O interfaces to support this operation. Key features: • One USB2.0 OTG controller • High Speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps) • Fully compatible with the USB 2.0 specification • Fully compatible with the USB On-The-Go supplement to the USB 2.0 specification • Hardware support for OTG signaling Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) implemented in hardware, which can also be controlled by software
uSDHC	SD/eMMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	The uSDHC is a host controller used to communicate with external low cost data storage and communication media. It supports the previous versions of the MultiMediaCard (MMC) and Secure Digital Card (SD) standards. Specifically, the uSDHC supports: • SD Host Controller Standard Specification v3.0 with the exception that all the registers do not match the standards address mapping. • SD Physical Layer Specification v3.0 UHS-I (SDR104/DDR50) • SDIO specification v3.0 • eMMC System Specification v5.1
VPU	Video Processing Unit	See the device reference manual for the complete list of the VPU's decoding/encoding capabilities.
WDOG	Watchdog	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
XTAL OSC24M		The 24 MHz clock source is an external crystal that acts as one of two main clock sources to the chip. The OSC24M is used as the source clock for subsystem PLLs. OSC24M can be turned off by the System Control Unit (SCU) during sleep mode.
XTAL OSC32K		The 32 KHz clock source is an external crystal that is one of two main clock sources to the chip. The OSC32K is intended to be always on and is distributed by the SCU to modules in the chip.

3.1 Special Signal Considerations

The package contact assignments can be found in Section 6, "Package information and contact assignments"." Signal descriptions are defined in the device reference manual.

3.2 Recommended Connections for Unused Interfaces

The recommended connections for unused analog interfaces can be found in the section, "Unused Input/Output Terminations," in the hardware development guide for this device.

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for these processors.

4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the SoC. See the following table for a quick reference to the individual tables and sections.

Table 7. Chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	on page 17
FCPBGA package thermal resistance data	on page 19
Operating ranges	on page 20
External Input Clock Frequency	on page 22
Maximum supply currents	on page 23
USB 2.0 PHY typical current consumption in Power-Down Mode	on page 26
USB 3.0 PHY typical current consumption in Power-Down Mode	on page 26
Typical current consumption in Power-Down mode for USB 2.0 PHY embedded in USB 3.0 PHY	on page 26

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 8 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating ranges" or other parameter tables is not implied. Exposure to absolute-maximum-rated conditions for extended periods will affect device reliability.

Table 8. Absolute maximum ratings

Parameter Description	Symbol	Min	Max	Units
Core Supplies Input Voltage	VDD_A35	-0.3	1.2	V
	VDD_GPU			
	VDD_MAIN			
DDR PHY supplies	VDD_DDR_VDDQ	-0.3	1.75	V

Table 8. Absolute maximum ratings (continued)

Parameter Description	Symbol	Min	Max	Units
1.0V IO supplies	VDD_MIPI_1P0	-0.3	1.2	V
	VDD_USB_OTG_1P0			
IO Supply for GPIO Type 1.8V IO Single supply	VDD_ADC_1P8	-0.5	2.1	V
	VDD_ADC_DIG_1P8			
	VDD_ANA0_1P8 (IO, analog,OSC SCU)			
	VDD_ANA1_1P8 (IO, analog,OSC SCU)			
	VDD_DDR_PLL_1P8 (memory PLLs)			
	VDD_MIPI_1P8 (PHY, GPIO)			
	VDD_MIPI_CSI_DIG_1P8 (PHY, GPIO)			
	VDD_PCIE_1P8 (PHY)			
	VDD_USB_1P8 (PHY, GPIO)			
IO Supply for GPIO Type 1.8 / 2.5 / 3.3V IO Tri-voltage Supply	VDD_ENET0_VSELECT_1P8_2P5_3P3	-0.3	3.8	V
	VDD_ENET0_1P8_2P5_3P3			
	VDD_ESAI_SPDIF_1P8_2P5_3P3			
IO Supply for GPIO Type 1.8 / 3.3V IO Dual Voltage Supply	VDD_CAN_UART_1P8_3P3	-0.3	3.8	V
	VDD_CSI_1P8_3P3			
	VDD_EMMC0_1P8_3P3			
	VDD_EMMC0_VSELECT_1P8_3P3			
	VDD_ENET_MDIO_1P8_3P3			
	VDD_MIPI_DSI_DIG_1P8_3P3			
	VDD_PCIE_DIG_1P8_3P3			
	VDD_QSPI0A_1P8_3P3			
	VDD_QSPI0B_1P8_3P3			
	VDD_SPI_MCLK_UART_1P8_3P3			
	VDD_SPI_SAI_1P8_3P3			
	VDD_TMPR_CSI_1P8_3P3			
	VDD_USB_3P3 (PHY & GPIO)			
	VDD_USDHC1_1P8_3P3			
	VDD_USDHC1_VSELECT_1P8_3P3			
SNVS Coin Cell	VDD_SNVS_4P2	-0.3	4.3	V
USB VBUS (OTG2)	USB_OTG2_VBUS	-0.3	3.63	V
USB VBUS (OTG1)	USB_OTG1_VBUS	-0.3	5.5	V

Table 8. Absolute maximum ratings (continued)

Parameter Description	Symbol	Min	Max	Units
I/O Voltage for USB Drivers	USB_OTG1_DP/USB_OTG1_DN	-0.3	3.63	V
	USB_OTG2_DP/USB_OTG2_DN			
I/O Voltage for ADC	ADC_IN*x*	-0.1	2.1	V
Vin/Vout input/output voltage range (GPIO Type Pins)	Vin/Vout	-0.3	OVDD+0.3[1]	V
Vin/Vout input/output voltage range (DDR pins)	Vin/Vout	-0.3	OVDD+0.4[1,2]	V
ESD immunity (HBM).	Vesd_HBMX	—	1000	V
ESD immunity (CDM).	Vesd_CDM	—	250	V
Storage temperature range	Tstorage	-55	150	°C

1 OVDD is the I/O supply voltage.

2 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the I/O pins. Per JEDEC standard the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575 V.

4.1.2 Thermal resistance

4.1.2.1 FCPBGA package thermal resistance

This table provides the FCPBGA package thermal resistance data.

Table 9. FCPBGA package thermal resistance data

Rating	Board Type[1]	Symbol	Value, 21x21 mm package	Value, 17x17 mm package	Unit
Junction to Ambient Thermal Resistance[2]	JESD51-9, 2s2p	$R_{\theta JA}$	15.2	15.8	°C/W
Junction to Package Top Thermal Resistance[2]	JESD51-9, 2s2p	Ψ_{JT}	0.1	0.1	°C/W
Junction to Case Thermal Resistance[3]	JESD51-9, 1s	$R_{\theta JC}$	0.7	0.9	°C/W

1 Thermal test board meets JEDEC specification for this package (JESD51-9).

2 Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

3 Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the mold surface temperature at the package top side dead center.

4.1.3 Operating Ranges

The following table provides the operating ranges of these processors.

Table 10. Operating ranges[1]

Symbol	Description	Mode	Min	Typ	Max	Unit	Comments
VDD_A35	Power supply of Cortex-A35 cluster	Overdrive	1.05	1.10	1.15	V	Max frequency: 1.2 GHz
		Nominal	0.95	1.00	1.10	V	Max frequency: 900 MHz
VDD_GPU	Power supply of GPU instance	Overdrive	1.05	1.10	1.15	V	Max frequencies: • Shaders: 850MHz • Core: 700 MHz
		Nominal	0.95	1.00	1.10	V	Max frequencies: shaders: 372 MHz; core: 372 MHz
VDD_MAIN[2]	Power supply of remaining core logic	N/A	0.95	1.00	1.10	V	Max freq.: HiFi4 DSP 640 MHz Max freq.: M4 264 MHz Max freq.: VPU 600 MHz
VDD_DDR_VDDQ	Power supplies of memory IOs	DDR3L	1.30	1.35	1.45	V	Max frequency: 933 MHz to support DDR3L-1866
		LPDDR4	1.06	1.10	1.17	V	Max frequency: 1.2GHz to support LPDDR4-2400
VDD_DDR_PLL_1P8	Power supplies of memory PLLs	N/A	1.65	1.80	1.95	V	PLL supply can be merged with other 1.8V supplies with proper on board decoupling.
VDD_MIPI_1P0	Power supplies of PHYs (1.0V part)	N/A	0.95	1.00	1.10	V	—
VDD_ANA0_1P8 VDD_ANA1_1P8	Power supplies of IOs, analog and oscillator of the SCU	N/A	1.65	1.80	1.95	V	These balls shall be powered by a dedicated supply
VDD_ADC_1P8 VDD_ADC_DIG_1P8 VDD_MIPI_1P8 VDD_MIPI_CSI_DIG_1P8 VDD_USB_1P8	Power supplies of PHYs (1.8V part) and GPIO operating at 1.8V only.	N/A	1.65	1.80	1.95	V	—
VDD_PCIE_1P8	Power supplies of PCIE PHY (1.8 V part)		1.71	1.80	1.89	V	—

Table 10. Operating ranges[1] (continued)

Symbol	Description	Mode	Min	Typ	Max	Unit	Comments
VDD_USB_3P3	Power supplies of PHYs (3.3V part) and GPIO operating at 3.3V only	N/A	3.00	3.30	3.60	V	—
VDD_CAN_UART_1P8_3P3 VDD_CSI_1P8_3P3 VDD_EMMC0_1P8_3P3 VDD_EMMC0_VSELECT_1P8_3P3 VDD_ENET_MDIO_1P8_3P3 VDD_MIPI_DSI_DIG_1P8_3P3 VDD_PCIE_DIG_1P8_3P3 VDD_QSPI0A_1P8_3P3 VDD_QSPI0B_1P8_3P3 VDD_SPI_MCLK_UART_1P8_3P3 VDD_SPI_SAI_1P8_3P3 VDD_TMPR_CSI_1P8_3P3 VDD_USDHC1_1P8_3P3 VDD_USDHC1_VSELECT_1P8_3P3	Power supplies of GPIO supporting both 1.8V or 3.3V	1.8V	1.65	1.80	1.95	V	When VDD_USDHC1_1P8_3P3 is used to support an SD card, then it shall be on a dedicated 1.8V/3.3V regulator. When VDD_SIM0_1P8_3P3 is used to support a SIM card, it shall be on a dedicated 1.8V/3.3V regulator. When VDD_TMPR_CSI_1P8_3P3 is used as a GPIO it can be connected to the 1.8/3.3V supply. VDDs of this list targeting 1.8V can share 1.8V regulator of 1.8V only VDDs VDDs of this list targeting 3.3V can share 3.3V regulator of 3.3V only VDDs
		3.3V	3.00	3.30	3.60	V	—
VDD_ENET0_1P8_2P5_3P3 VDD_ENET0_VSELECT_1P8_2P5_3P3 VDD_ESAI_SPDIF_1P8_2P5_3P3	Power supplies of ethernet IOs	1.8V	1.65	1.80	1.95	V	—
		2.5V	2.40	2.50	2.60	V	—
		3.3V	3.00	3.30	3.60	V	—
VDD_SNVS_4P2	Power supply of SNVS	N/A	2.80	3.30	4.20	V	It can be supplied by a backup battery: a coin cell or a super cap.
Output of embedded LDOs							
VDD_PCIE_LDO_1P0_CAP VDD_USB_SS3_LDO_1P0_CAP	1.0V output of embedded LDOs	N/A	—	1.00	—	V	—
VDD_SNVS_LDO_1P8_CAP	1.8V output of SNVS embedded LDO	N/A	—	1.80	—	V	—

Table 10. Operating ranges[1] (continued)

Symbol	Description	Mode	Min	Typ	Max	Unit	Comments
Power supplies that shall be connected to output of an embedded LDO							
VDD_TMPR_CSI_1P8_3P3	—	N/A	—	1.80	—	V	Shall be connected to VDD_SNVS_LDO_1P8_CAP when used as a tamper pin. In CSI mode use an external 1.8 V supply. In this case, follow the 1.8 V I/O specification above.
VDD_USB_OTG_1P0	—	N/A	—	1.00	—	V	Shall be externally connected to VDD_USB_SS3_LDO_1P0_CAP
Junction temperature							
Junction temperature	—	—	-40	—	125	°C	—

1 Voltage ranges are defined to group as many supplies as possible. Some supplies may have a wider range than listed here.

2 During low power state (see Section 4.1.6, “Low power mode supply currents"), this voltage can be dropped to 0.8 V +/- 3% for retention.

4.1.4 External clock sources

Each processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for real time functions. It supplies the clock for real time clock operation and for slow-system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input requires a crystal using the internal oscillator amplifier.

The PCIe oscillator can be sourced internally or input to the chip. In both cases, it is a 100 MHz nominal clock using HCSL signaling to provide the PCIe reference clock.

The following table shows the interface frequency requirements.

Table 11. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[4,2]	f_{xtal}	—	24	—	MHz
PCIe oscillator[5]	f_{100M}	—	100	—	MHz
Frequency accuracy	—	—	—	±300	ppm

1 External oscillator or a crystal with internal oscillator amplifier.
2 The required frequency stability of this clock source is application dependent. For recommendations, see the hardware development guide for this device.
3 Recommended nominal frequency 32.768 kHz.
4 Fundamental frequency crystal with internal oscillator amplifier.
5 If using an external clock instead of the internal clock source, an HCSL-compatible clock is required.

The typical values shown in Table 11 are required for use with NXP board support packages (BSPs) to ensure precise time keeping and USB operations.

4.1.5 Maximum Supply Currents

NOTE

Some of the numbers shown in this table are based on the companion regulator limits and not actual use cases. Work is in progress to provide use case–based numbers in future data sheet releases.

Table 12. Maximum supply currents

Symbol	Value	Unit	Comments
VDD_A35[1]	2500	mA	
VDD_GPU[1]	2500	mA	
VDD_MAIN	5000	mA	
VDD_DDR_VDDQ	1200	mA	Does not comprehend IO of memory
VDD_DDR_PLL_1P8	20	mA	
VDD_ANA0_1P8	200	mA	
VDD_ANA1_1P8	200	mA	
VDD_MIPI_1P0	100	mA	
VDD_MIPI_1P8	115	mA	
VDD_ADC_DIG_1P8	18	mA	
VDD_CAN_UART_1P8_3P3	30	mA	
VDD_CSI_1P8_3P3	12	mA	
VDD_EMMC0_1P8_3P3	30	mA	
VDD_EMMC0_VSELECT_1P8_3P3	30	mA	
VDD_ENET_MDIO_1P8_3P3	15	mA	
VDD_ENET0_1P8_2P5_3P3	30	mA	
VDD_ENET0_VSELECT_1P8_2P5_3P3	30	mA	
VDD_ESAI_SPDIF_1P8_2P5_3P3	39	mA	
VDD_MIPI_CSI_DIG_1P8	15	mA	

Table 12. Maximum supply currents (continued)

Symbol	Value	Unit	Comments
VDD_MIPI_DSI_DIG_1P8_3P3	24	mA	
VDD_PCIE_DIG_1P8_3P3	9	mA	
VDD_QSPI0A_1P8_3P3	40	mA	
VDD_QSPI0B_1P8_3P3	40	mA	
VDD_SPI_MCLK_UART_1P8_3P3	36	mA	
VDD_SPI_SAI_1P8_3P3	48	mA	
VDD_TMPR_CSI_1P8_3P3	30	mA	
VDD_USDHC1_1P8_3P3	30	mA	
VDD_USDHC1_VSELECT_1P8_3P3	20	mA	
VDD_ADC_1P8	5	mA	
VDD_USB_OTG_1P0	36	mA	Shall be externally connected to VDD_USB_SS3_LDO_1P0_CAP
VDD_USB_1P8	175	mA	
VDD_USB_3P3	40	mA	
VDD_PCIE_1P8	255	mA	
VDD_SNVS_4P2[2]	5	mA	Start-up current

1 VDD_A35 and VDD_GPU can be combined with one power supply.

2 Under normal operating conditions, the maximum current on VDD_SNVS_4P2 is shown Table 11. During initial power on, VDD_SNVS_4P2 can draw up to 5 mA if the supply is capable of sourcing that current. If less than 5 mA is available, the VDD_SNVS_LDO_1P8_CAP charge time will increase.

4.1.6 Low power mode supply currents

The following table shows the current core consumption (not including I/O) in selected low power modes.

Table 13. i.MX 8QuadXPlus/8DualXPlus Key State (KSx) power consumption

Mode	Test conditions	Supply	Max	Unit
KS0	SNVS only, all other supplies OFF. RTC running, tamper not active, external 32K crystal.	VDD_SNVS_4P2 (4.2 V)	50	µA
KS1[1]	RAM and IO state retained. DRAM in self-refresh, associated I/O's OFF. 32K running, 24M, PLLs and ring oscillators OFF. PHYs are in idle state. A35 and GPU supplies OFF. MAIN[2] dropped to 0.8 V.	VDD_ANAx_1P8 (1.8 V) VDD_A35 (OFF) VDD_GPU (OFF) VDD_MAIN (0.8 V) VDD_DDR_VDDQ (1.1 V) Total	0.9 — — 33 0.5 28.6	mA mA mA mA mA mW
KS4[3]	Leakage test, not intended as a customer use case. Overdrive conditions set, memories active, all sub-systems powered ON. Active power minimized.	VDD_ANAx_1P8 (1.8 V) VDD_A35 (1.1 V) VDD_GPU (1.1 V) VDD_MAIN (1.0 V) Total	3.6 660 300 1700 2763	mA mA mA mA mW

1 Maximum values are for 25 °C $T_{ambient}$.

2 0.8 V nominal—voltage specification under this case is ± 3%.

3 Maximum values are for 125 °C $T_{junction}$.

4.1.7 USB 2.0 PHY typical current consumption in Power-Down mode

In power down mode, everything is powered down, including the VBUS valid detectors, typical condition. The following table shows the USB interface typical current consumption in Power-Down mode.

Table 14. USB 2.0 PHY typical current consumption in Power-Down Mode

	VDD_USB_3P3 (3.3 V)	VDD_USB_1P8 (1.8 V)	VDD_USB_OTG_1P0 (1.0 V)
Current	1 µA	0.06 µA	0.5 µA

4.1.8 USB 3.0 PHY typical current consumption in Power-Down mode

In power down mode, everything is powered down, including the VBUS valid detectors, typical condition. The following table shows the USB interface typical current consumption in Power-Down mode.

Table 15. USB 3.0 PHY typical current consumption in Power-Down Mode

	—	VDD_USB_1P8 (1.8 V)	VDD_USB_OTG_1P0 (1.0 V)
Current	—	10 µA	70 µA

The following table shows the current consumption for the USB 2.0 PHY embedded in the USB 3.0 PHY.

Table 16. Typical current consumption in Power-Down mode for USB 2.0 PHY embedded in USB 3.0 PHY

	VDD_USB_3P3 (3.3 V)	VDD_USB_1P8 (1.8 V)	VDD_USB_OTG2_1P0VDD_USB_OTG_1P0 (1.0 V)
Current—Host mode	22.6 µA	12.7 µA	81.5 µA
Current—Device mode	12.6 µA	85.7 µA	78.5 µA

4.1.8.1 USB 3.0 Type-C connector considerations

The device supports USB 3.0 Type-C connection when used in conjunction with the following devices:

- PTN36043
- PTN5150A
- NX5P3090UK

NXP supports many other configurations and implementations for USB 3.0 Type-C connections. See NXP USB Type-C: True Plug’n Play .

4.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to ensure the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor

4.2.1 Power-up sequence

The device has the following power-up sequence requirements:

- Supply group 0 (SNVS) must be powered first. It is expected that group 0 will typically remain always on after the first power-on.
- Supply group 1 (MAIN and SCU) and group 0 must both be powered to their nominal values prior to boot. They must power up after or simultaneously with group 0.
- Supply group 2 (I/O's and DDR interface) consists of those modules required to start the boot process by accessing external storage devices. These must be fully powered prior to POR release if booting from one of these supplies interfaces. They must power up after or simultaneously with group 1.
- Supply group 3 consists of the remaining portions of the SoC. This includes nonboot I/O voltages and supplies for the major computational units. These can be sequenced in any order and as required to perform the desired functions for the intended application. They must power up after or simultaneously with group 2.

NOTE

The definition of "power-up" refers to a stable voltage operating within the range defined in Table 10. This should be taken into consideration, along with the different capacitive loading on each rail, if considering simultaneous switch-on of the different supply groups.

4.2.2 Power-down sequence

The device processor has the following power-down sequence requirements:

- Supply group 0 must be turned off last, after all other supplies.
- Supply group 1 can be turned off just prior to group 0.

All remaining supplies can be turned off prior to group 1.

NOTE

When switching off supply group 0 (SNVS), VDD_SNVS_4P2 must be discharged below 2.4 V before starting the next power-up sequence to ensure correct operation. This will generate a full SNVS reset, allowing correct operation on the next power-up sequence. This would also be a requirement to clear any security related flag as a result of an SNVS voltage drop, when tamper features are enabled.

4.2.3 Power Supplies Usage

The following table shows the power supplies usage by group.

Table 17. Power supplies usage

Supply Groups	Voltage				
Group 0	**2.4 - 4.2v**	**1.8v internal LDO**			
	VDD_SNVS_4P2	VDD_TMPR_CSI_1P8_3P3[1]			
Group 1	**1.0v**	**1.8v**			
	VDD_MAIN	VDD_ANA**x**_1P8			
	VDD_MIPI_1P0				
Group 2	**1.1 - 1.35v**	**1.8v**	**1.8v or 3.3v**	**1.8v or 3.3v switchable**	**3.3v**
	VDD_DDR_VDDQ	VDD_ADC_DIG_1P8	VDD_CAN_UART_1P8_3P3	VDD_EMMC0_1P8_3P3	VDD_USB_3P3
		VDD_ADC_1P8	VDD_CSI_1P8_3P3	VDD_USDHC1_1P8_3P3	
		VDD_DDR_PLL_1P8	VDD_EMMC0_VSELECT_1P8_3P3		
		VDD_MIPI_1P8	VDD_ENET_MDIO_1P8_3P3		
		VDD_MIPI_CSI_DIG_1P8	VDD_MIPI_DSI_DIG_1P8_3P3		
		VDD_PCIE_1P8	VDD_PCIE_DIG_1P8_3P3		
		VDD_USB_1P8	VDD_QSPI0**x**_1P8_3P3		
			VDD_SPI_MCLK_UART_1P8_3P3		
			VDD_SPI_SAI_1P8_3P3		
			VDD_TMPR_CSI_1P8_3P3[1]		
			VDD_USDHC1_VSELECT_1P8_3P3		
Group 3	**1.1 - 1.1v**	**1.0v internal LDO's**	**1.8v or 2.5v or 3.3v**		
	VDD_A35[2]	VDD_USB_OTG_1P0	VDD_ENET0_1P8_2P5_3P3		
	VDD_GPU[2]		VDD_ENET0_VSELECT_1P8_2P5_3P3		
			VDD_ESAI_SPDIF_1P8_2P5_3P3		

1 Supply connection and Supply Group vary depending on use case. For use as tamper pin, it must be tied to the VDD_SNVS_LDO_1P8_CAP. If used as a CSI/SAI, it is tied to I/O supply.

2 VDD_A35 and VDD_GPU can be combined with one power supply.

4.3 PLL electrical characteristics

4.3.1 PLLs of subsystems

i.MX 8QuadXPlus/8DualXPlus embeds a large number of PLLs to address clocking requirements of the various subsystems. These PLLs are controlled through the SCU and not directly by Cortex-A or Cortex-M4F processors. A software API shall be used by those processors to access the PLL settings. Additional PLLs are specific to high-performance interfaces. These are described in the following sections.

This table summarizes the PLLs controlled by the SCU.

Table 18. PLLs controlled by SCU

Subsystem	PLL usage	Source clock	Locking range[1]		Lock freq.	Unit
			Min freq.	Max freq.		
Cortex-A35	Subsystem	24	650	1300	• Overdrive: 1200 • Nominal: 900[2]	
GPU	PLL #0: subsystem	24	648	1344	• Overdrive: 700 • Nominal: 744[3]	MHz
	PLL #1: shaders	24	648	1344	• Overdrive: : 850 • Nominal: 744[4]	MHz
DRC (DRAM Controller)	Subsystem	24	1250	2500	• LPDDR4: 2400 • DDR3L: 1866[5]	MHz
DB (DRAM Block)	Subsystem	24	650	1300	1200	MHz
Display Controller 0	PLL #0: subsystem	24	650	1300	800	MHz
	PLL #1: display clock #0	24	650	1300	User-configurable	MHz
	PLL #2: display clock #1	24	650	1300	User-configurable	MHz
Imaging	Subsystem	24	650	1300	1200	MHz
ADMA	PLL #0: subsystem	24	650	1300	1280	MHz
	PLL #1: audio PLL #0	24	650	1300	User-configurable	MHz
	PLL #2: audio PLL #1	24	650	1300	User-configurable	MHz
	PLL #3: Parallel LCD display	24	650	1300	Pixel freq. $\times N$	MHz
Connectivity	PLL #0: Subsystem	24	650	1300	792	MHz
	PLL #1: PHY	24	650	1300	1000	MHz
HSIO (High-speed I/O)	Subsystem	24	650	1300	800	MHz
LSIO (Low-speed I/O)	Subsystem	24	650	1300	800	MHz

Table 18. PLLs controlled by SCU (continued)

Subsystem	PLL usage	Source clock	Locking range[1]		Lock freq.	Unit
			Min freq.	Max freq.		
Cortex-M4	Subsystem	24	650	1300	792	MHz
VPU	PLL #0: subsystem	24	650	1300	1200	MHz
MIPI-DSI	Subsystem	24	650	1300	864	MHz
MIPI-CSI	Subsystem	24	650	1300	720	MHz
SCU (System Controller Unit)	Subsystem	24	650	1300	1056	MHz

1 Operating frequencies are limited to only those supported by the SCFW.

2 1200 MHz is used to generate the max frequency points, and 1000 MHz for the typical frequency point. See Table 10 to get associated voltages.

3 700 MHz is used to generate the max frequency point, and 744 is used to generate the typical point (372 MHz).

4 850 MHz is used to generate the max frequency point, and 744 is used to generate the typical point (372 MHz)

5 2400 MHz is used to generate 1200 MHz when in LPDDR4 mode. 1866 MHz is used to generate 933 MHz when in DDR3L mode. See Table 10 to get associated voltages.

4.3.2 PLLs dedicated to specific interfaces

The following sections cover PLLs used for specific interfaces. Clock output frequency and clock output range refer to the output of the PLL. Additional clock dividers may be on the output path to divide the output frequency down to the targeted frequency. See the related sections in the reference manual for settings of these clock dividers.

4.3.2.1 Ethernet PLL

This PLL is controlled by the SCU.

Table 19. Ethernet PLL

Parameter	Value	Unit
Reference clock	24	MHz
Clock output frequency	1	GHz

4.3.2.2 USB 3.0 PLLs

USB 3.0 has two PLLs. One is embedded in Super-Speed PHY. The other one is embedded in the USB 2.0 OTG PHY that is part of the USB 3.0 interface.

The table below describes the PLL embedded in the Super-Speed PHY.

Table 20. USB 2.0 PLL embedded in Super Speed PHY

Parameter	Value	Unit
Reference clock	24	MHz
Clock output frequency	5	GHz

The table below describes the PLL embedded in the USBOTG PHY.

Table 21. USB 2.0 PLL embedded in USBOTG PHY

Parameter	Value	Unit
Reference clock	24	MHz
Clock output frequency	480	MHz

4.3.2.3 USB 2.0 OTG PLLs

This PLL is embedded in the USB 2.0 OTG PHY (the one which is not part of the USB 3.0 feature).

Table 22. USB 2.0 OTG PLLs

Parameter	Value	Unit
Reference clock	24	MHz
Clock output frequency	480	MHz

4.3.2.4 PCIe PLLs

The PCIe interface has three PLLs:

- One is used to generate the single, common 100 MHz reference clock to each lane
- One Transmit and one Receive PLL in one lane

The table below shows the characteristics for the reference clock PLL.

Table 23. PCIe reference clock PLLs

Parameter	Value	Unit	Comments
Reference clock	24	MHz	—
Clock output frequency	100	MHz	Used to generate internal 100 MHz reference clock to PCIe lanes

The table below shows characteristics of the TX and RX PLLs used in each lane.

Table 24. PCIe Transmit and Receive PLLs

Parameter	Value	Unit	Comments
Reference clock	100	MHz	From differential input clock pads or from internal PLL
Clock output range	6 ~ 10	GHz	PCIe gen3: 8GHz to get 8GHz baud clock PCIe gen2: 10GHz to get 5GHz baud clock PCIe gen3: 10GHz to get 2.5GHz baud clock

4.3.2.5 MIPI-DSI/LVDS combo PLL

The table below shows characteristics of the PLL embedded in the MIPI-DSI/LVDS combo PHY.

Table 25. MIPI-DSI/LVDS combo PHY PLL

Parameter	Value	Unit	Comments
Reference clock	24	MHz	—
Clock output range	0.75 ~ 1.05	GHz	Dependent on targeted display configuration

4.4 On-chip oscillators

4.4.1 OSC24M

This block integrates trimmable internal loading capacitors and driving circuitry. When combined with a suitable 24 MHz external quartz element, it can generate a low-jitter clock. The oscillator is powered from VDD_ANA1_1P8. The internal loading capacitors are trimmable to provide fine adjustment of the 24 MHz oscillation frequency. It is expected that customers burn appropriate trim values for the selected crystal and board parasitics.

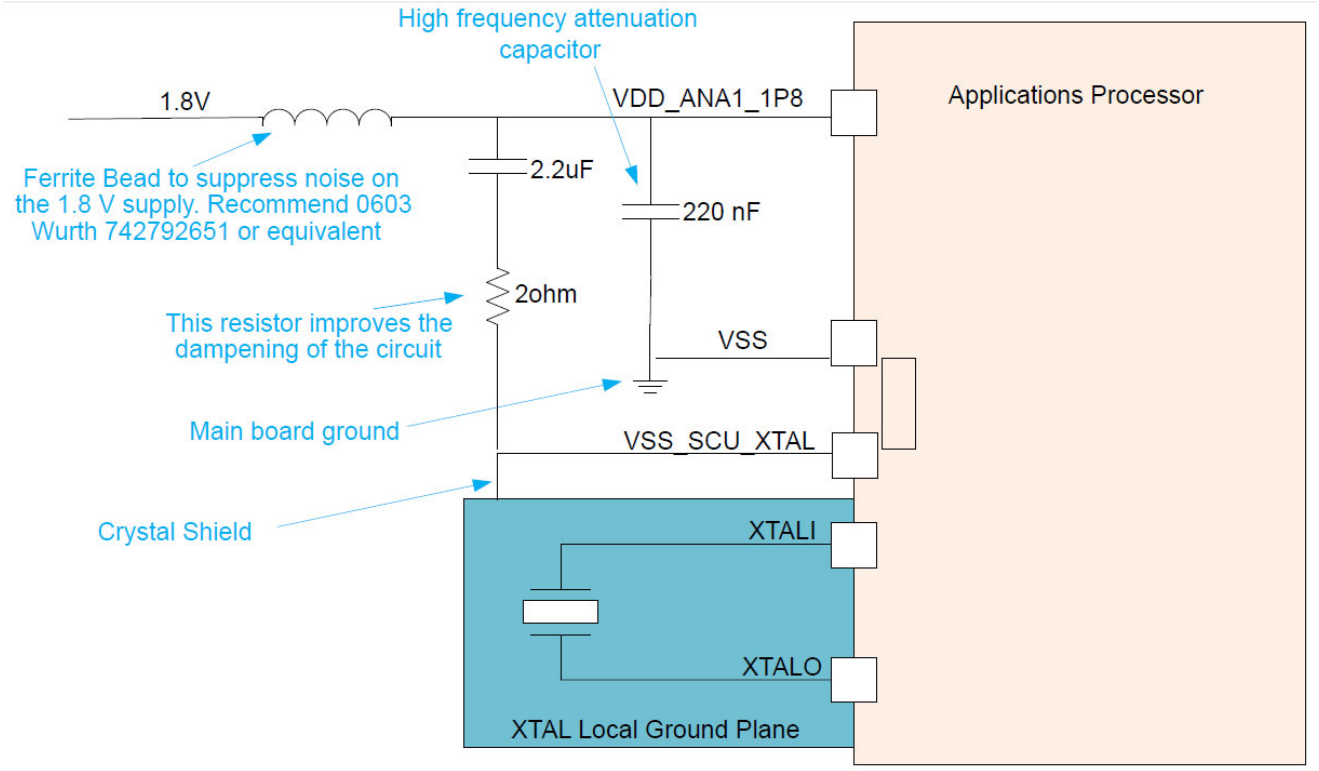


Figure 2. Normal Crystal Oscillation mode

Table 26. Crystal specifications

Parameter description	Min	Typ	Max	Unit
Frequency[1]	—	24	—	MHz
Cload[2]	—	18	—	pF
Maximum drive level	200	—	—	μW
ESR	—	—	60	Ω

1 The required frequency accuracy is set by the serial interfaces utilized for a specific application and is detailed in the respective standard documents.

2 Cload is the specification of the quartz element, not for the capacitors coupled to the quartz element.

4.4.2 OSC32K

This block implements an internal amplifier, trimmable load capacitors and a bias network that when combined with a suitable quartz crystal implements a low power oscillator.

Additionally, if the clock monitor determines that the 32KHz oscillation is not present, then the source of the 32 KHz clock will automatically switch to the internal relaxation oscillator of lesser frequency accuracy.

CAUTION

The internal ring oscillator is not meant to be used in customer applications, due to gross frequency variation over wafer processing, temperature, and supply voltage. These variations will cause timing issues to many different circuits that use the internal ring oscillator for reference; and, if this timing is critical, application issues will occur. To prevent application issues, it is recommended to only use an external crystal or an accurate external clock. If this recommendation is not followed, NXP cannot guarantee full compliance of any circuit using this clock. The OSC32K runs from VDD_SNVS_LDO_1P8_CAP, which is regulated from VDD_SNVS. The target battery/voltage range is 2.8 to 4.2 V for VDD_SNVS, with a regulated output of approximately 1.75 V.

Table 27. OSC32K main characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 KHz is also supported.
Current consumption	—	• xtal oscillator mode: 5 μA • 32K internal oscillator mode: 10 μA	—	These values are for typical process and room temperature. Values will be updated after silicon characterization.
Bias resistor	—	200 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amplifier. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

Table 28. External input clock for OSC32K

	Min	Typ	Max	Unit	Notes
Frequency	—	32.768 or 32	—	kHz	—
V_{PP} RTC_XTALI	700	—	VDD_SNVS_LDO_1P8_CAP	mV	1,2,3
Rise/fall time	—	—	—	ns	4

1 The external clock is fed into the chip from the RTC_XTALI pin; the RTC_XTALO pin should be left floating.
2 The parameter specified here is a peak-to-peak value and VI_H/V_{IL} specifications do not apply.
3 The voltage applied on RTC_XTALI must be within the range of VSS to VDD_SNVS_LDO_1P8_CAP.
4 The rise/fall time of the applied clock are not strictly confined.

4.5 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- XTALI and RTC_XTALI (clock inputs) DC parameters
- General Purpose I/O (GPIO) DC parameters

NOTE

The term 'OVDD' in this section refers to the associated supply rail of an input or output.

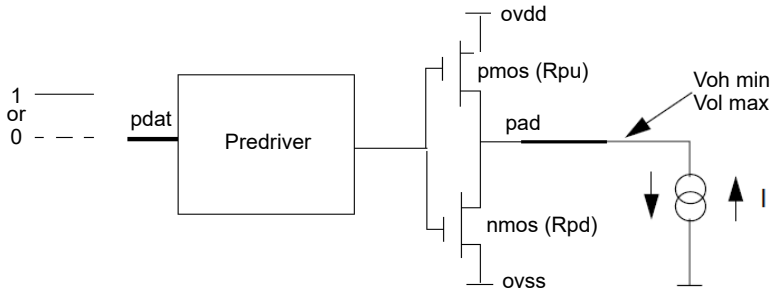


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.5.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

For RTC_XTALI, V_{IH}/V_{IL} specifications do not apply. The high and low levels of the applied clock on this pin are not strictly defined, as long as the input's peak-to-peak amplitude meet the requirements and the input's voltage value does not exceed the limits.

4.5.2 General-purpose I/O (GPIO) DC parameters

4.5.2.1 Tri-voltage GPIO DC parameters

The following tables show tri-voltage 1.8V, 2.5 V, and 3.3 V DC parameters, respectively, for GPIO pads. These parameters are guaranteed per the operating ranges in Table 10, unless otherwise noted.

Table 29. Tri-voltage 1.8 V GPIO DC parameters[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[2,3]	V_{OH}	I_{OH}= -0.1mA DSE=1	0.8 × OVDD	—	V
		I_{OH}= -2mA DSE=0			
Low-level output voltage[2,3]	V_{OL}	I_{OL}= -0.1mA DSE=1	—	0.125 × OVDD	V
		I_{OL}= -2mA DSE=0			
High-Level input voltage[2,4]	V_{IH}	—	0.625 × OVDD	OVDD	V
Low-Level input voltage	V_{IL}	—	0	0.25 × OVDD	V
Pull-up resistance	R_{PU}	V_{IN}=0V (Pullup Resistor) PUN = "L", PDN = "H"	15	50	kΩ
Pull-down resistance	R_{DOWN}	V_{IN}=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	15	50	kΩ
Input current (no PU/PD)	I_{IN}	VI = 0, VI = OVDD PUN = "H", PDN = "H"	-1	1	μA

1 For tri-voltage I/O, the associated IOMUXD compensation control register PSW_OVR and COMP bits must be set correctly. For 1.8 or 3.3 V operation, the SCFW API must be used to set PSW_OVR = 0b0 and COMP=0b000. For 2.5 V operation, PSW_OVR = 0b1 and COMP = 0b010.

2 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.3 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Noncompliance to this specification may affect device reliability or cause permanent damage to the device. (OVDD is the I/O Supply)

3 DSE is the setting of the PDRV register. High Drive mode is recommended for 3v3 and 2v5 modes. Low Drive mode is recommended for 1v8 mode.

4 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{IL} or V_{IH}. Monotonic input transition time is from 0.1 ns to 1 ns.

Table 30. Tri-voltage 2.5 V GPIO DC parameters[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[2,3]	V_{OH}	I_{OH}= -2mA DSE=0	0.8 × OVDD	—	V
Low-level output voltage[2,3]	V_{OL}	I_{OL}= -2mA DSE=0	—	0.125 × OVDD	V
High-Level input voltage[2,4]	V_{IH}	—	0.625 × OVDD	OVDD	V
Low-Level input voltage	V_{IL}	—	0	0.25 × OVDD	V
Pull-up resistance	RPU	V_{IN}=0V (Pullup Resistor) PUN = "L", PDN = "H"	10	100	kΩ

Table 30. Tri-voltage 2.5 V GPIO DC parameters[1] (continued)

Parameter	Symbol	Test Conditions	Min	Max	Units
Pull-down resistance	R_{DOWN}	V_{IN}=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	10	100	kΩ
Input current (no PU/PD)	I_{IN}	VI = 0, VI = OVDD PUN = "H", PDN = "H"	-1	1	μA

1 For tri-voltage I/O, the associated IOMUXD compensation control register PSW_OVR and COMP bits must be set correctly. For 1.8 or 3.3 V operation, the SCFW API must be used to set PSW_OVR = 0b0 and COMP=0b000. For 2.5 V operation, PSW_OVR = 0b1 and COMP = 0b010.

2 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.3 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Noncompliance to this specification may affect device reliability or cause permanent damage to the device. (OVDD is the I/O supply.)

3 DSE is the setting of the PDRV register. High Drive mode is recommended for 3v3 and 2v5 modes. Low Drive mode is recommended for 1v8 mode.

4 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{IL} or V_{IH}. Monotonic input transition time is from 0.1 ns to 1 ns.

Table 31. Tri-voltage 3.3 V GPIO DC parameters[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[2,3]	V_{OH}	I_{OH}= -0.1mA 4DSE=1	0.8 × OVDD		V
		I_{OH}= -2mA 4DSE=0			
Low-level output voltage[2,3]	V_{OL}	I_{OL}= -0.1mA 4DSE[3]=1	—	0.125 × OVDD	V
		I_{OL}= -2mA 4DSE=0			
High-Level input voltage[2,4,3]	V_{IH}	—	0.725 × OVDD	OVDD	V
Low-Level input voltage	V_{IL}	—	0	0.25 × OVDD	V
Pull-up resistance	RPU	V_{IN}=0V (Pullup Resistor) PUN = "L", PDN = "H"	10	100	kΩ
Pull-down resistance	R_{DOWN}	V_{IN}=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	10	100	kΩ
Input current (no PU/PD)	IIN	VI = 0, VI = OVDD PUN = "H", PDN = "H"	-2	2	μA

1 For tri-voltage I/O, the associated IOMUXD compensation control register PSW_OVR and COMP bits must be set correctly. For 1.8 or 3.3 V operation, the SCFW API must be used to set PSW_OVR = 0b0 and COMP=0b000. For 2.5 V operation, PSW_OVR = 0b1 and COMP = 0b010.

2 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.3 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Noncompliance to this specification may affect device reliability or cause permanent damage to the device. (OVDD is the I/O Supply.)

3 DSE is the setting of the PDRV register. High Drive mode recommended for 3v3 and 2v5 modes. Low Drive mode is recommended for 1v8 mode.

4 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{IL} or V_{IH}. Monotonic input transition time is from 0.1 ns to 1 ns.

4.5.2.2 Dual-voltage GPIO DC parameters

The following two tables show dual-voltage 1.8 V and 3.3 V DC parameters, respectively, for GPIO pads. These parameters are guaranteed per the operating ranges in Table 10, unless otherwise noted.

Table 32. Dual-voltage 1.8 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1,2]	V_{OH}	Ioh= -0.1mA DSE=1	0.8 × OVDD	—	V
		Ioh= -2mA DSE=0			
Low-level output voltage[1,2]	V_{OL}	Iol= -0.1mA DSE=1	—	0.125 × OVDD	V
		Iol= -2mA DSE=0			
High-Level input voltage[1,3]	V_{IH}	—	0.625 × OVDD	OVDD	V
Low-Level input voltage	V_{IL}	—	0	0.25 × OVDD	V
Pull-up resistance	R_{PU}	Vin=0 V (Pullup Resistor) PUN = "L", PDN = "H"	15	50	kΩ
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	15	50	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD PUN = "H", PDN = "H"	-1	1	μA

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.3 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Noncompliance to this specification may affect device reliability or cause permanent damage to the device. (OVDD is the IO Supply.)

2 DSE is the setting of the PDRV register. High Drive mode is recommended for SD standard (3v3 mode) and MMC standard (1v8/3v3 modes). Low Drive mode is recommended for SD standard (1v8 mode).

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 ns.

Table 33. Dual-voltage 3.3 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1,2]	V_{OH}	Ioh= -0.1mA DSE=1	0.8 × OVDD	—	V
		Ioh= -2mA DSE=0			
Low-level output voltage[1,2]	V_{OL}	Iol= -0.1mA DSE=1	—	0.125 × OVDD	V
		Iol= -2mA DSE=0			
High-Level input voltage[1,3]	V_{IH}	—	0.725 × OVDD	OVDD	V
Low-Level input voltage	V_{IL}	—	0	0.25 × OVDD	V
Pull-upresistance	R_{PU}	Vin=0V (Pullup Resistor) PUN = "L", PDN = "H"	10	100	kΩ
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	10	100	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD PUN = "H", PDN = "H"	-2	2	µA

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.3 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Noncompliance to this specification may affect device reliability or cause permanent damage to the device. (OVDD is the I/O Supply.)

2 DSE is the setting of the PDRV register. High Drive mode is recommended for SD standard (3v3 mode) and MMC standard (1v8/3v3 modes). Low Drive mode is recommended for SD standard (1v8 mode).

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{IL} or V_{IH}. Monotonic input transition time is from 0.1 ns to 1 ns.

4.5.2.3 Single-voltage GPIO DC parameters

Table 34 and Table 35 show single-voltage 1.8 V and 3.3 V DC parameters, respectively, for GPIO pads. These parameters are guaranteed per the operating ranges in Table 10 unless otherwise noted.

Table 34. Single-voltage 1.8 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1,2]	V_{OH}	I_{OH}= -0.1mA DSE = 000 or 001	OVDD × 0.8	—	V
		I_{OH}= -2mA DSE = 010 or 011			
		I_{OH}= -4mA DSE = 100 to 110			

Table 34. Single-voltage 1.8 V GPIO DC parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Units
Low-level output voltage[1,2]	V_{OL}	I_{OL}= 0.1mA DSE = 000 or 001	—	OVDD × 0.2	V
		I_{OL}= 2mA DSE = 010 or 011			
		I_{OL}= 4mA DSE = 100 to 110			
High-Level input voltage[2,3]	V_{IH}	—	0.65 × OVDD	OVDD	V
Low-Level input voltage[2,3]	V_{IL}	—	0	0.35 × OVDD	V
Pull-up resistance	R_{PU}	Vin=0V (Pullup Resistor) PUN = "L", PDN = "H"	20	90	kΩ
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	20	90	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD PUN = "H", PDN = "H"	-5	5	μA
Keeper Circuit Resistance	R_Keeper	V_I =.3xOVDD, VI = .7x OVDD PUN = "L", PDN = "L"	20	90	kΩ

1 As programmed in the associated IOMUX (DSE field) register.

2 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.3 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Noncompliance to this specification may affect device reliability or cause permanent damage to the device. (OVDD is the IO supply.)

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{IL} or V_{IH}. Monotonic input transition time is from 0.1 ns to 1 ns.

Table 35. Single-voltage 3.3 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1,2]	V_{OH}	I_{OH} = -0.1mA DSE = 00 or 01	0.8 × OVDD	—	V
		I_{OH}= -2mA DSE = 10 or 11			
Low-level output voltage[1,2]	V_{OL}	I_{OL}=0.1mA DSE = 00 or 01	—	0.2 × OVDD	V
		I_{OL} = 2mA DSE = 10 or 11			
High-Level input voltage[2,3]	V_{IH}	—	0.75 × OVDD	OVDD	V
Low-Level input voltage[2,3]	V_{IL}	—	0	0.25 × OVDD	V
Pull-upresistance	R_{PU}	Vin=0 V (Pullup Resistor) PUN = "L", PDN = "H"	20	90	kΩ

Table 35. Single-voltage 3.3 V GPIO DC parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Units
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	20	90	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD PUN = "H", PDN = "H"	-5	5	μA
Keeper Circuit Resistance	R_Keeper	V_I =.3xOVDD, VI = .7x OVDD PUN = "L", PDN = "L"	20	90	kΩ

1 As programmed in the associated IOMUX (DSE field) register.

2 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.3 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Noncompliance to this specification may affect device reliability or cause permanent damage to the device. (OVDD is the IO supply.)

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{IL} or V_{IH}. Monotonic input transition time is from 0.1 ns to 1 ns.

4.5.3 DDR I/O DC parameters

4.5.3.1 LPDDR4 mode I/O DC parameters

These parameters are guaranteed per the operating ranges in Table 10 unless otherwise noted.

Table 36. LPDDR4 DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1]	V_{OH}	Out Drive = All setting (40,48,60,80,120,240) unterminated outputs loaded with 1pF capacitor load	$0.9 \times V_{DDQ}$	—	V
Low-level output voltage[1]	V_{OL}	Out Drive = All setting (40,48,60,80,120,240) unterminated outputs loaded with 1pF capacitor load	—	$0.1 \times V_{DDQ}$	V
Input current (no ODT)	I_{IN}	V_I = VSSQ, V_I = VDDQ	-2	2	μA
DC High-Level input voltage	V_{IH_DC}	—	VREF + 0.1	VDDQ	V
DC Low-Level input voltage	V_{IL_DC}	—	VSSQ	VREF – 0.1	V

1 Maximum peak amplitude allowed for overshoot and undershoot area = 0.35 V. Maximum overshoot area above VDD/VDDQ 0.8 V-ns; maximum undershoot area below VSS/VSSQ 0.8 V-ns.

4.5.3.2 DDR3L mode I/O DC parameters

Table 37. SSTL DDR3L DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
DC High-level output voltage [1]	V_{OH}	Out Drive = All setting (40,60,120) unterminated outputs loaded with 1pF capacitor load	$0.8 \times V_{DDQ}$	—	V
DC Low-level output voltage[1]	V_{OL}	Out Drive = All setting (40,60,120) unterminated outputs loaded with 1pF capacitor load	—	$0.2 \times V_{DDQ}$	V
Input termination resistance (ODT) to VDDQ/2	RTT	40 Ω setting	36	44	Ω
		60 Ω setting	54	66	
		120 Ω setting	100	140	
Input current (no ODT)	I_{IN}	V_I = VSSQ, V_I = VDDQ	-2	2	µA
DC High-Level input voltage	V_{IH_DC}		VREF + 0.09	VDDQ	V
DC Low-Level input voltage	V_{IL_DC}		VSSQ	VREF – 0.09	V

[1] Maximum peak amplitude allowed for overshoot and undershoot area = 0.35 V. Maximum overshoot area above VDD/VDDQ 0.8 V-ns; maximum undershoot area below VSS/VSSQ 0.8 V-ns.

4.6 I/O AC Parameters

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

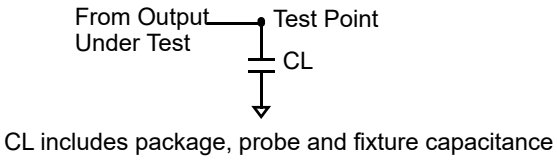


Figure 4. Load Circuit for Output

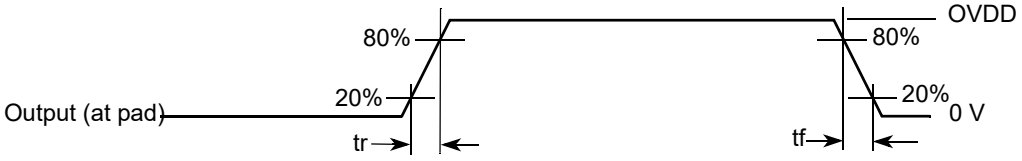


Figure 5. Output Transition Time Waveform

4.6.1 General Purpose I/O (GPIO) AC Parameters

Table 38. General Purpose I/O AC Parameters[1]

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
1.8 V application[2]						
f_{max}	Maximum frequency	Load = 21 pF (PDRV = H, high drive, Type A, 33 Ω	—	—	208	MHz
		Load = 15 pF (PDRV = L, low drive, Type B, 50 Ω				
tr	Rise time	Measured between V_{OL} and V_{OH}	0.4	—	1.32	ns
tf	Fall time	Measured between V_{OH} and V_{OL}	0.4	—	1.32	ns
Driver 3.3 V application[3]						
f_{max}	Maximum frequency	Load = 30 pF	—	—	52	MHz
tr	Rise time	Measured between V_{OL} and V_{OH}	—	—	3	ns
tf	Fall time	Measured between V_{OH} and V_{OL}	—	—	3	ns

1 All output I/O specifications are guaranteed for Accurate mode of the compensation cell operation. This is applicable for both DC and AC specifications.

2 All timing specifications in 1.8 V application are valid for High Drive mode (PDRV = H). In Low Drive mode (PDRV = L), the driver is functional.

3 All timing specifications in 3.3 V application are valid for Type B driver only. In Type A, the driver is functional.

Table 39. Dynamic input characteristics

Symbol	Parameter	Condition[1,2]	Min	Max	Unit
Dynamic Input Characteristics for 3.3 V Application					
f_{op}	Input frequency of operation	—	—	52	MHz
INPSL	Slope of input signal at I/O	Measured between 10% to 90% of the I/O swing	—	3.5	ns
IOMAX	High level input voltage	—	—	3.3 V + 0.3 V	V
IOMIN	Low level input voltage	—	-0.3 V	—	
Dynamic Input Characteristics for 1.8 V Application					
f_{op}	Input frequency of operation	—	—	208	MHz
INPSL	Slope of input signal at I/O	Measured between 10% to 90% of the I/O swing	—	1.5	ns
IOMAX	High level input voltage	—	—	1.8 V + 0.3 V	V
IOMIN	Low level input voltage	—	-0.3 V	—	

1 For all supply ranges of operation.

2 The dynamic input characteristic specifications are applicable for the digital bidirectional cells.

4.7 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters for the following I/O types:

- General Purpose I/O (GPIO) output buffer impedance
- Double Data Rate I/O (DDR) output buffer impedance for LPDDR4 and DDR3L modes

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 6).

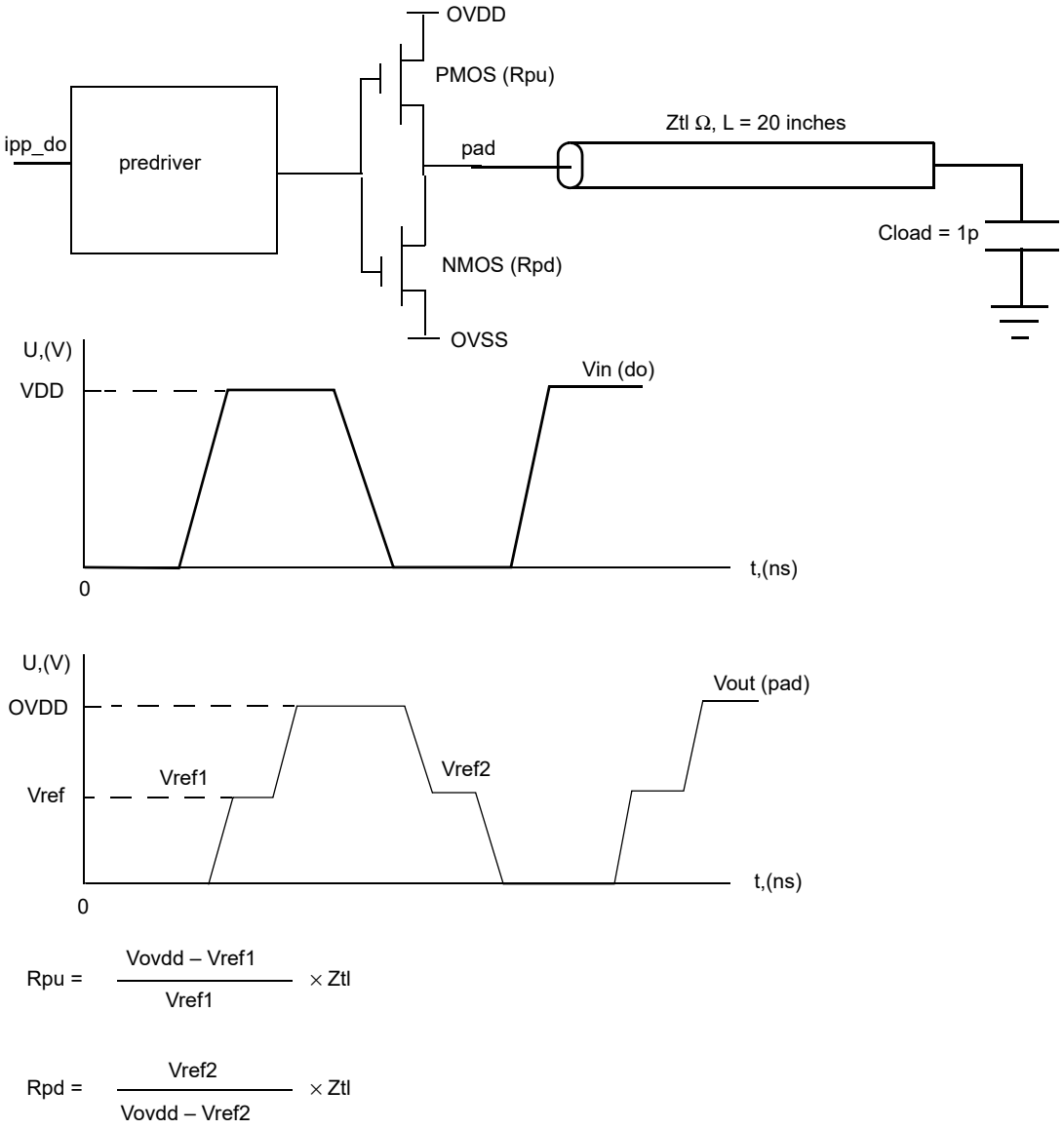


Figure 6. Impedance Matching Load for Measurement

4.7.1 GPIO output buffer impedance

4.7.1.1 Tri-voltage GPIO output buffer impedance

Table 40. Tri-voltage 1.8 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=0	33	Ω
Output impedance	Z_O	[1]DSE=1	50	Ω

[1] As programmed in the associated IOMUX (PDRV field) register.

Table 41. Tri-voltage 2.5 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=0	25	Ω
Output impedance	Z_O	[1]DSE=1	33	Ω

[1] As programmed in the associated IOMUX (PDRV field) register.

Table 42. Tri-voltage 3.3 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=0	25	Ω
Output impedance	Z_O	[1]DSE=1	37	Ω

[1] As programmed in the associated IOMUX (PDRV field) register.

4.7.1.2 Dual-voltage GPIO output buffer impedance

Table 43. Dual-voltage 1.8 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=0	33	Ω
Output impedance	Z_O	[1]DSE=1	50	Ω

[1] ‘As programmed in the associated IOMUX (PDRV field) register.

Table 44. Dual-voltage 3.3 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=0	25	Ω
Output impedance	Z_O	[1]DSE=1	37	Ω

[1] As programmed in the associated IOMUX (PDRV field) register.

4.7.1.3 Single-voltage 1.8 V GPIO output buffer drive strength

The following table shows the GPIO output buffer drive strength (OVDD 1.8 V).

Table 45. Single-voltage GPIO 1.8 V output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=000	200	Ω
		[1]DSE=001	100	
		[1]DSE=010	55	
		[1]DSE=011	40	
		[1]DSE=100	30	
		[1]DSE=101	24	
		[1]DSE=110	20	
		[1]DSE=111	18	

1 As programmed in the associated IOMUX (DSE field) register.

4.7.1.4 Single-voltage 3.3 V GPIO output buffer drive strength

The following table shows the GPIO output buffer drive strength (OVDD 3.3 V).

Table 46. Single-voltage GPIO 3.3 V output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=00	400	Ω
		[1]DSE=01	200	
		[1]DSE=10	100	
		[1]DSE=11	50	

1 As programmed in the associated IOMUX (DSE field) register.

4.7.2 DDR I/O output buffer impedance

The following tables show DDR3L and LPDDR4 I/O output buffer impedance of the device.

The ZQ Calibration cell uses a single register (ZQnPR0) to determine the target output buffer impedances of the pull-up driver and the pull-down driver, as well as the target on-die termination impedance. The resulting calibration setting is then applied to all DDR pads within the PHY complex.

Table 47 and Table 49 show, respectively, the recommended ZQnPR0 field settings for the DDR3L and LPDDR4 I/Os to achieve the desired output buffer impedances. Table 48 and Table 50 show, respectively, the recommended ZQnPR0 field settings for the DDR3L and LPDDR4 I/Os to achieve the desired ODT settings.

Table 47. LPDDR4 I/O output buffer impedance

Parameter	Typical			
	ZQnPR0 ZPROG_ASYM_PU_DRV	Impedance	ZQnPR0 ZPROG_ASYM_PD_DRV	Impedance
Recommended combinations for DQ /CA pins	5	80 Ω	3	120 Ω
	7	60 Ω	5	80 Ω
	9	48 Ω	7	60 Ω
	11	40 Ω	9	48 Ω

Table 48. LPDDR4 I/O on-die termination impedance

Parameter	Typical Impedance	ZQnPR0. ZPROG_HOST_ODT
Recommended combinations for DQ/CA pins	120.0 Ω	3
	80.0 Ω	5
	60.0 Ω	7
	48.0 Ω	9
	40.0 Ω	11

Table 49. DDR3L I/O output buffer impedance

Parameter	Typical Impedance	ZQnPR0. ZPROG_ASYM_PU_DRV	ZQnPR0. ZPROG_ASYM_PD_DRV
Recommended combinations for DQ/CA pins	48.0 Ω	9	9
	40.0 Ω	11	11
	34.3 Ω	13	13

Table 50. DDR3L I/O on-die termination impedance

Parameter	Typical Impedance	ZQnPR0. ZPROG_HOST_ODT
Recommended combinations for DQ/CA pins	120.0 Ω	1
	60.0 Ω	3
	40.0 Ω	5

NOTE

- Output driver impedance is controlled across PVTs using ZQ calibration procedure.
- Calibration is done against 240 Ω external reference resistor.
- Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8 System Modules Timing

This section contains the timing and electrical parameters for the modules in each processor.

4.8.1 Reset Timing Parameters

The following figure shows the reset timing and Table 51 lists the timing parameters.

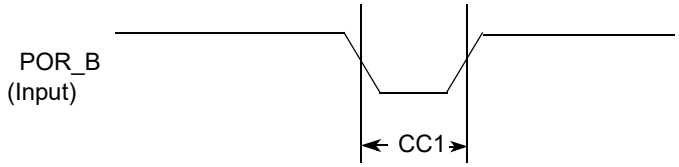


Figure 7. Reset timing diagram

Table 51. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of SRC_POR_B to be qualified as valid	1	—	XTALOSC_RTC_ XTALI cycle

4.8.2 WDOG reset timing parameters

The following figure shows the WDOG reset timing and Table 52 lists the timing parameters.

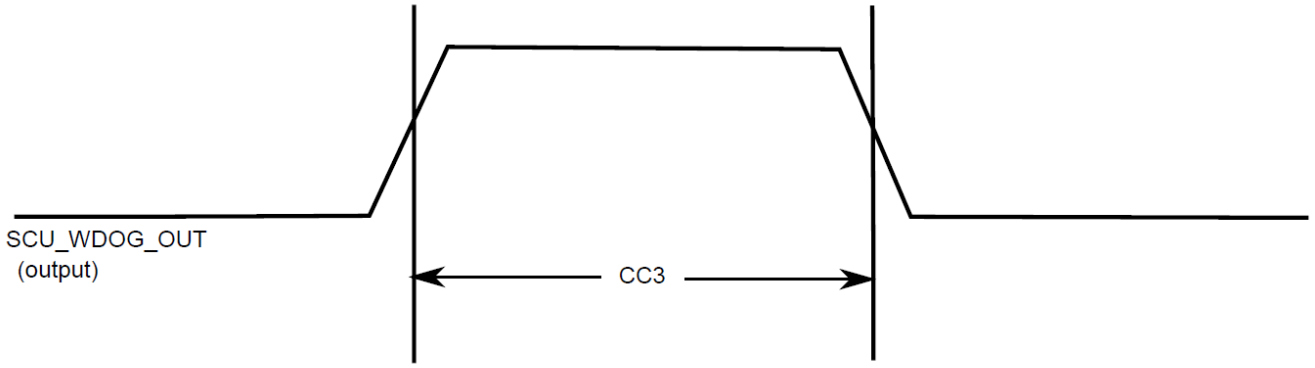


Figure 8. SCU_WDOG_OUT timing diagram

Table 52. WDOG1_B timing parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of SCU_WDOG_OUT assertion	1	—	XTALOSC_RTC_ XTALI cycle

NOTE

XTALOSC_RTC_XTALI is approximately 32 kHz.
XTALOSC_RTC_XTALI cycle is one period or approximately 30 µs.

4.8.3 DDR SDRAM–specific parameters (LPDDR4 and DDR3L)

The i.MX 8x Family of processors have been designed and tested to work with JEDEC JESD209-4A–compliant LPDDR4 memory and with JEDEC JESD79-3-1 DDR3L compliant with DDR3L memory. Timing diagrams and tolerances required to work with these memories are specified in the respective documents and are not reprinted here.

Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. NXP cannot cover in this document all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part variation; PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, VIA placement, GND and Supply planes layout, and DDR controller/PHY register settings all are factors affecting the performance of the memory system. Consult the hardware user guide for this device and NXP validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors and DDR trace routing between the processor and the selected DDR memory. All supporting material is readily available on the device web page on

https://www.nxp.com/products/processors-and-microcontrollers/applications-processors/i.mx-applications-processors/i.mx-8-processors:IMX8-SERIES .

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as closure to a customer's reported DDR issue. Customers bear the responsibility of properly designing the Printed Circuit Board, correctly simulating and modeling the designed DDR system, and validating the system under all expected operating conditions (temperatures, voltages) prior to releasing their product to market.

Table 53. i.MX 8 Family DRAM controller supported SDRAM configurations

Parameter	LPDDR4
Number of Controllers	2
Number of Channels	2 per controller
Number of Chip Selects	2 per channel
Bus Width	16 bit per channel[1]
Maximum Clock Frequency	1600 MHz

1 Only 16-bit external memory configurations are supported.

Table 54. i.MX 8QuadXPlus/8DualXPlus DRAM controller supported SDRAM configurations

Parameter	LPDDR4	DDR3L
Number of Controllers	1	
Number of Channels	2 per controller	N/A
Number of Chip Selects	2 per channel	2 per controller
Bus Width	16-bit per channel	32-bit (optional 40-bit with ECC)
Maximum Clock Frequency	1200 MHz	933 MHz

4.8.3.1 Clock/data/command/address pin allocations

These processors uses generic names for clock, data and command address bus (DCF—DRAM controller functions); the following table provides mapping of clock, data and command address signals for LPDDR4 and DDR3L modes.

Table 55. Clock, data, and command address signals for LPDDR4 and DDR3L modes

Signal name	LPDDR4
DDR_CK0_P	CK_t_A
DDR_CK0_N	CK_c_A

Table 55. Clock, data, and command address signals for LPDDR4 and DDR3L modes (continued)

Signal name	LPDDR4
DDR_CK1_P	CK_t_B
DDR_CK1_N	CK_c_B
DDR_DQ_[15:0]	DQ[15:0]_A
DDR_DQ_[31:16]	DQ[15:0]_B
DDR_DQ_[39:32]	
DDR_DQS_N_[3:0]	DQS_N_[3:0]
DDR_DQS_P_[3:0]	DQS_P_[3:0]
DDR_DQS_N_4	
DDR_DQS_P_4	
DDR_DM_[3:0]	DM_[3:0]
DDR_DM_4	
DDR_DCF00	CA2_A
DDR_DCF01	CA4_A
DDR_DCF03	CA5_A
DDR_DCF04	
DDR_DCF05	
DDR_DCF07	
DDR_DCF08	CA3_A
DDR_DCF09	ODT_CA_A
DDR_DCF10	CS0_A
DDR_DCF11	CA0_A
DDR_DCF12	CS1_A
DDR_DCF14	CKE0_A
DDR_DCF15	CKE1_A
DDR_DCF16	CA1_A
DDR_DCF17	CA4_B
DDR_DCF18	RESET_N
DDR_DCF19	CA5_B
DDR_DCF20	
DDR_DCF21	
DDR_DCF22	
DDR_DCF23	
DDR_DCF24	

Table 55. Clock, data, and command address signals for LPDDR4 and DDR3L modes (continued)

Signal name	LPDDR4
DDR_DCF25	ODT_CA_B
DDR_DCF26	CA3_B
DDR_DCF27	CA0_B
DDR_DCF28	CS0_B
DDR_DCF29	CS1_B
DDR_DCF30	CKE0_B
DDR_DCF31	CKE1_B
DDR_DCF32	CA1_B
DDR_DCF33	CA2_B

4.8.3.2 ECC for DDR3L

i.MX 8QuadXPlus/8DualXPlus supports up to 8-bit ECC when using DDR3L only. This is accomplished through the use of a fifth byte lane (DQS4[P:N],DM4, DQ[32:39]). When using the fifth byte lane, it is not a requirement that all DDR3L devices be identical, but it is required that all devices be able to operate with the same timing parameters. This can be easily accomplished by using memory containing the same die(s), but contained in different packages. Consult the DDR3L device datasheets for timing requirements. The fifth byte lane is for the exclusive use of ECC. If not using ECC, leave the pins as not connected. For LPDDR4 mode, pins DQS4[P:N],DM4, DQ[32:39] are not used and cannot be substituted for one of the other byte lanes. If using LPDDR4 mode, leave these pins as not connected.

4.9 General-Purpose Media Interface (GPMI) Timing

The GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 400 MB/s I/O speed, and individual chip select. It supports Asynchronous Timing mode, Source Synchronous Timing mode, and Toggle Timing mode, as described in the following subsections.

4.9.1 GPMI Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 9 through Figure 12 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 56 describes the timing parameters (NF1–NF17) that are shown in the figures.

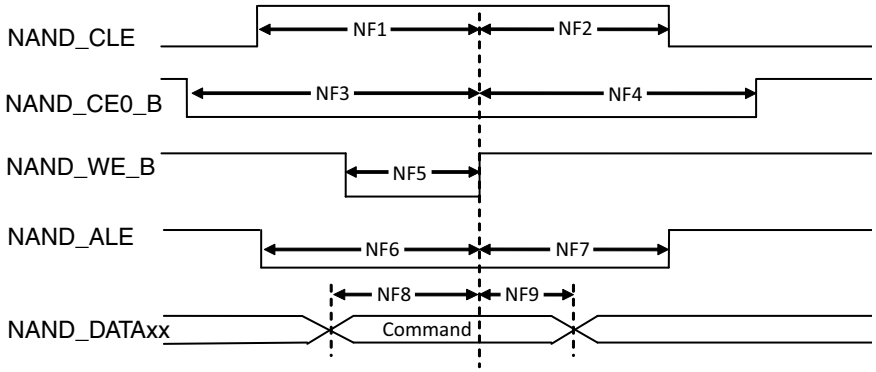


Figure 9. Command Latch Cycle Timing Diagram

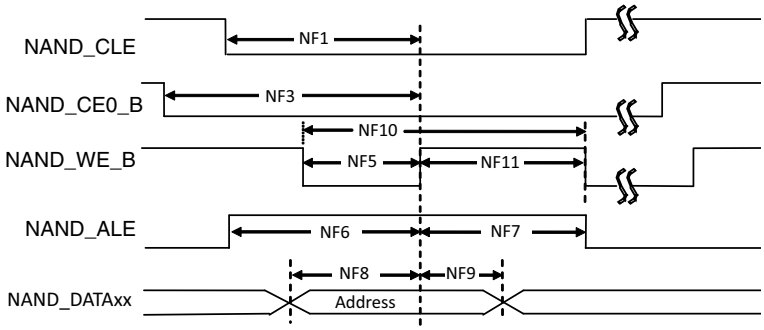


Figure 10. Address Latch Cycle Timing Diagram

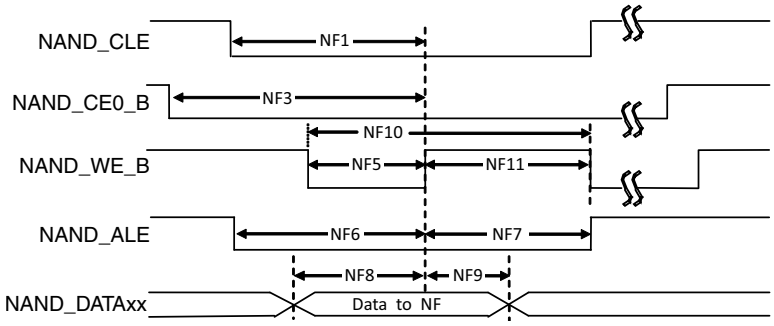


Figure 11. Write Data Latch Cycle Timing Diagram

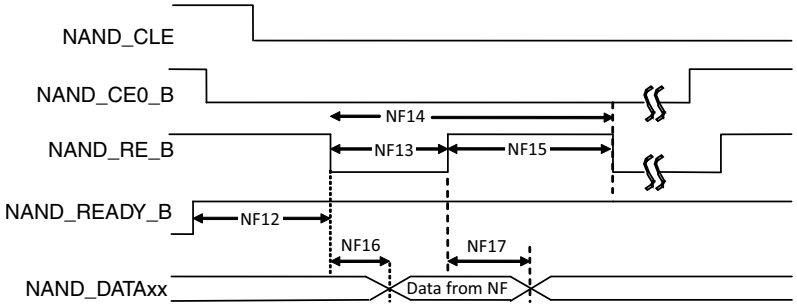


Figure 12. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

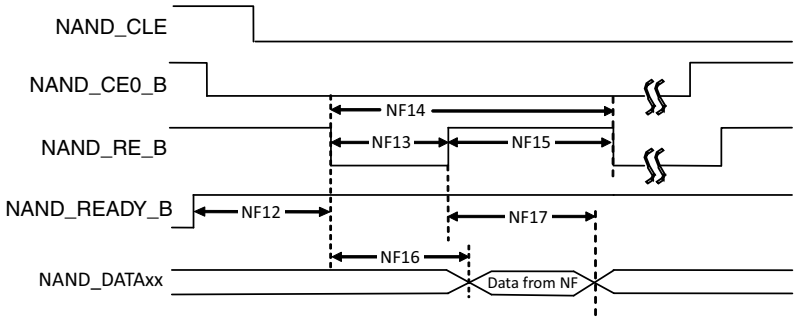


Figure 13. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 56. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		ns
NF3	NAND_CEx_B setup time	tCS	(AS + DS + 1) × T [see 3,2]		ns
NF4	NAND_CEx_B hold time	tCH	(DH+1) × T - 1 [see 2]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see 2]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see 2]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see 2]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see 2]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see 2]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see 3,2]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see 2]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see 2]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see 2]		ns

Table 56. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see [5,6]]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see [5,6]]	—	ns

1 The GPMI asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075ns (half of maximum p-p jitter).

4 NF12 is met automatically by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz
(AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 13), NF16/NF17 are different from the definition in non-EDO mode (Figure 12). They are called tREA/tRHOH (NAND_RE_B access time/NAND_RE_B HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the device reference manual. The typical value of this control register is 0x8 at 50 MT/s EDO mode. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.9.2 GPMI Source Synchronous mode AC timing (ONFI 2.x compatible)

The following figure shows the write and read timing of Source Synchronous mode.

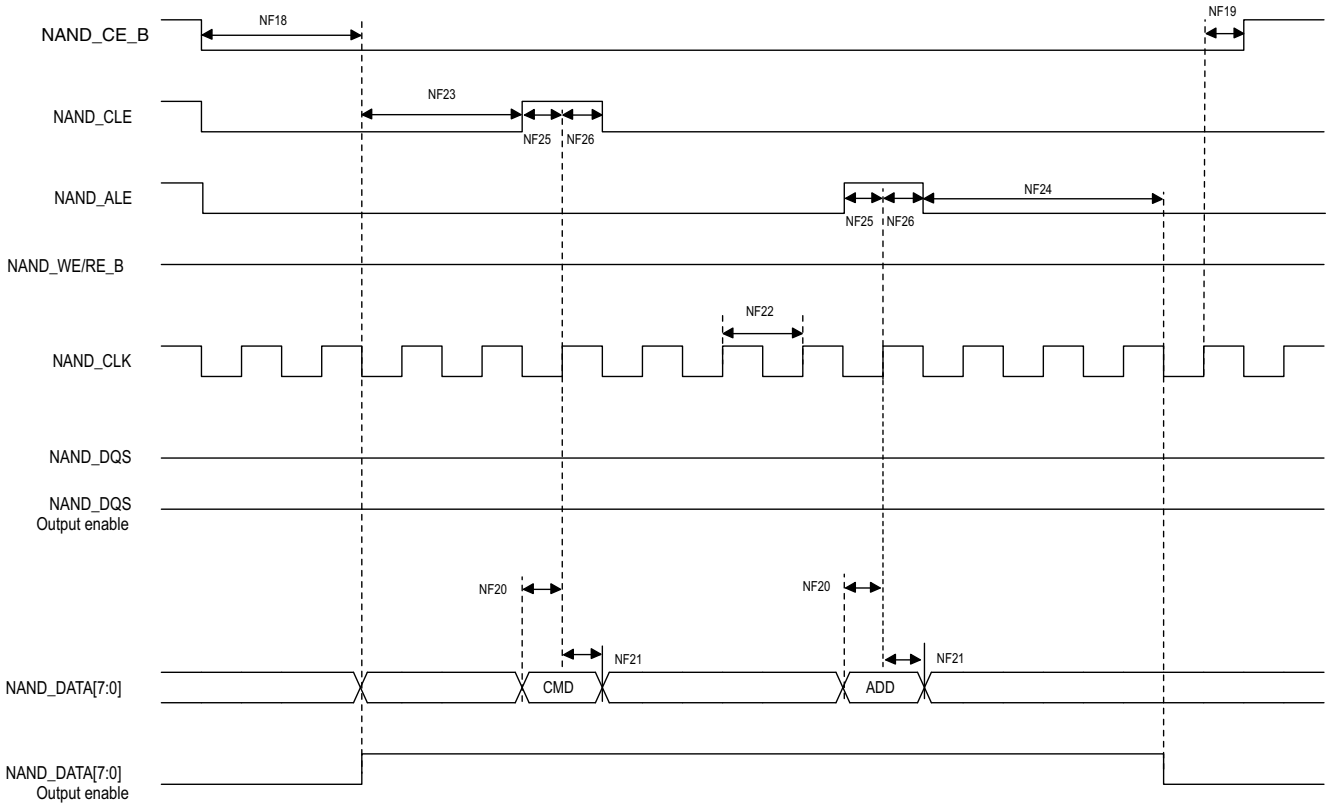


Figure 14. Source Synchronous Mode Command and Address Timing Diagram

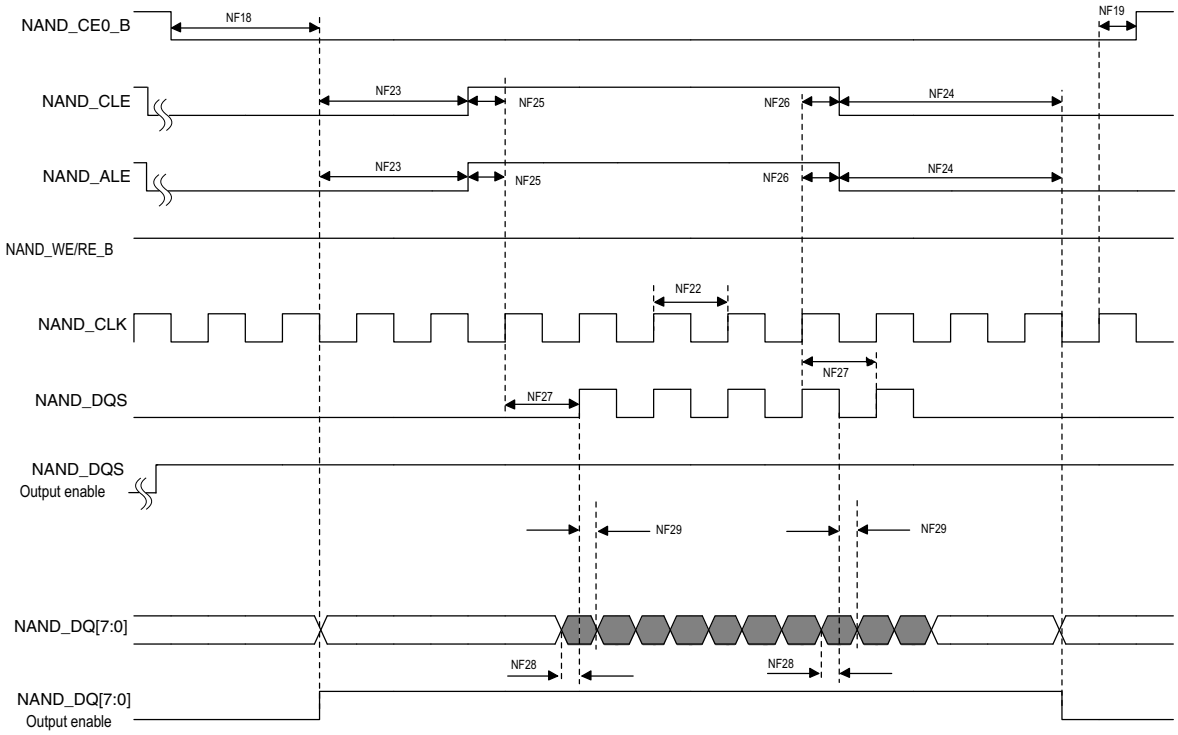


Figure 15. Source Synchronous Mode Data Write Timing Diagram

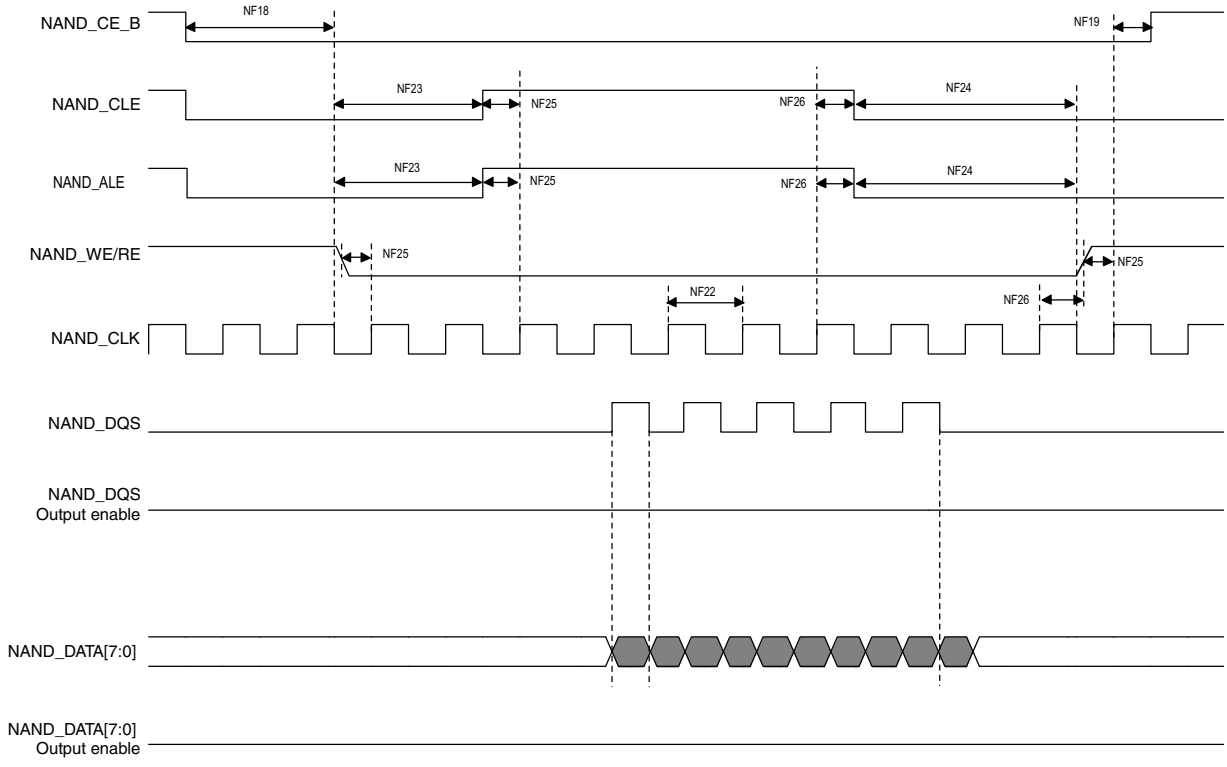


Figure 16. Source Synchronous Mode Data Read Timing Diagram

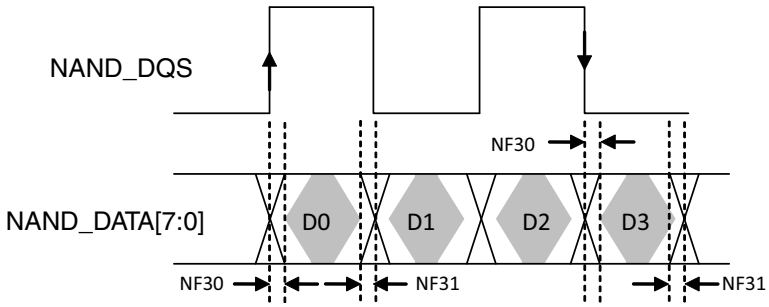


Figure 17. NAND_DQS/NAND_DQ Read Valid Window

Table 57. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T - 0.79 [see 2]		ns
NF19	NAND_CEx_B hold time	tCH	0.5 × tCK - 0.63 [see 2]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see 2]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see 2]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see 2]		ns
NF28	Data write setup	tDS	0.25 × tCK - 0.35		ns
NF29	Data write hold	tDH	0.25 × tCK - 0.85		ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ	—	2.06	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS	—	1.95	—

1 The GPMI source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

Figure 17 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. For Source Synchronous mode, the typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the device reference manual. Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.9.3 ONFI NV-DDR2 mode (ONFI 3.2 compatible)

4.9.3.1 Command and address timing

ONFI 3.2 mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.9.1, “GPMI Asynchronous mode AC timing (ONFI 1.0 compatible)",” for details.

4.9.3.2 Read and write timing

ONFI 3.2 mode read and write timing is the same as Toggle mode AC timing. See Section 4.9.4, “Toggle mode AC Timing",” for details.

4.9.4 Toggle mode AC Timing

4.9.4.1 Command and address timing

NOTE

Toggle mode command and address timing is the same as ONFI 1.0 compatible Asynchronous mode AC timing. See Section 4.9.1, “GPMI Asynchronous mode AC timing (ONFI 1.0 compatible)",” for details.

4.9.4.2 Read and write timing

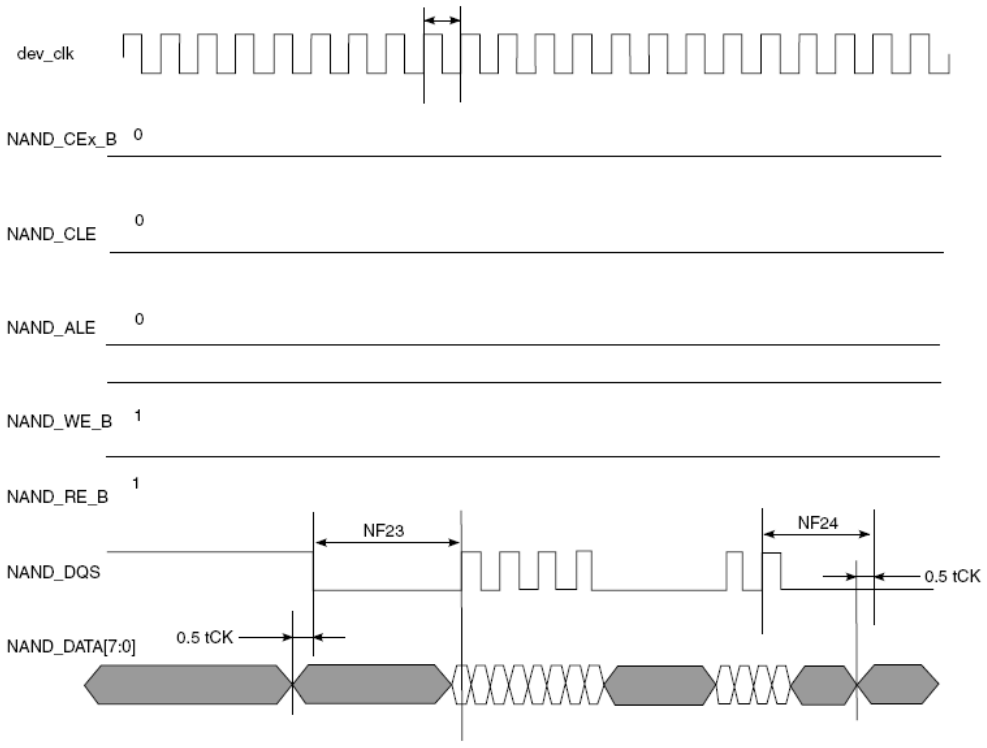


Figure 18. Toggle mode data write timing

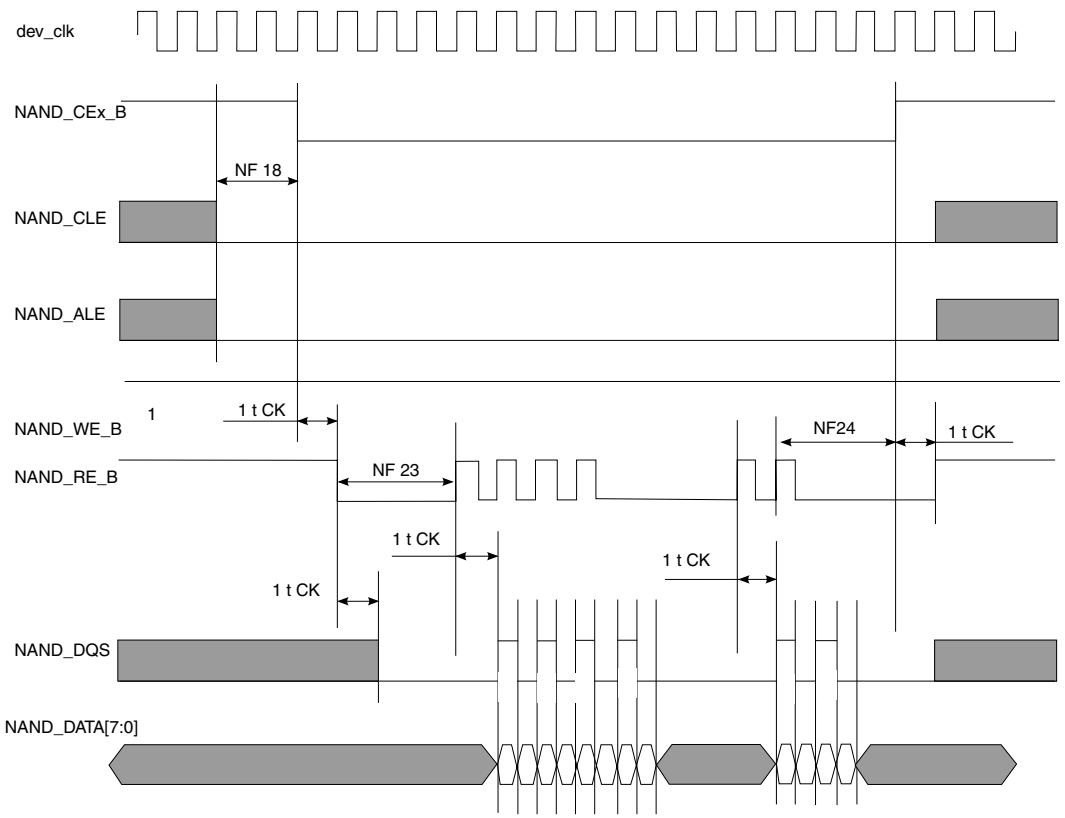


Figure 19. Toggle mode data read timing

Table 58. Toggle mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see note[2]s[,3]]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see notes[,2]]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see note[2]]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes[,2]]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see note[2]]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see note[2]]		
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see notes[4,2]]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see notes[5,2]]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see note[2]]	—	ns

Table 58. Toggle mode timing parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	

1 The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = tCK (GPMI clock period) -0.075 ns (half of maximum p-p jitter).

4 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

5 PRE_DELAY+1) ≥ (AS+DS)

6 Shown in Figure 18.

7 Shown in Figure 19.

For DDR Toggle mode, Figure 19 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the device reference manual. Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.10.1 LPSPI timing parameters

All LPSPI interfaces do not have the same maximum serial clock frequency. There are two groups. LPSPI interfaces which can operate at 60 MHz in Master mode and 40 MHz in Slave mode and the other group where interfaces operate at 40 MHz in Master mode and 20 MHz in Slave mode. The same performance is achieved at 1.8 V and 3.3 V unless otherwise stated.

Below are the LPSPI interfaces and their respective chip selects:

Table 59. LPSPI interfaces and chip selects

LPSPI interface	Chip select	Comment
60 MHz in Master mode and 40 MHz in Slave mode	SPI0, SPI2, SPI2b, SPI3	SPI2 - default SPI2 balls SPI2b - muxed behind audio balls
40 MHz in Master mode and 20 MHz in Slave mode	SPI1, SPI1b, SPI2c	SPI1 - muxed behind SAI balls SPI1b - muxed behind CSI balls SP2c - muxed behind uSDHC1 balls

4.10.1.1 LPSPI Master mode

Waveform is assuming LPSPI is configured in mode 0, i.e. TCR.CPOL=0b0 and TCR.CPHA=0b0. Timing parameters are valid for all modes using appropriate edge of the clock.

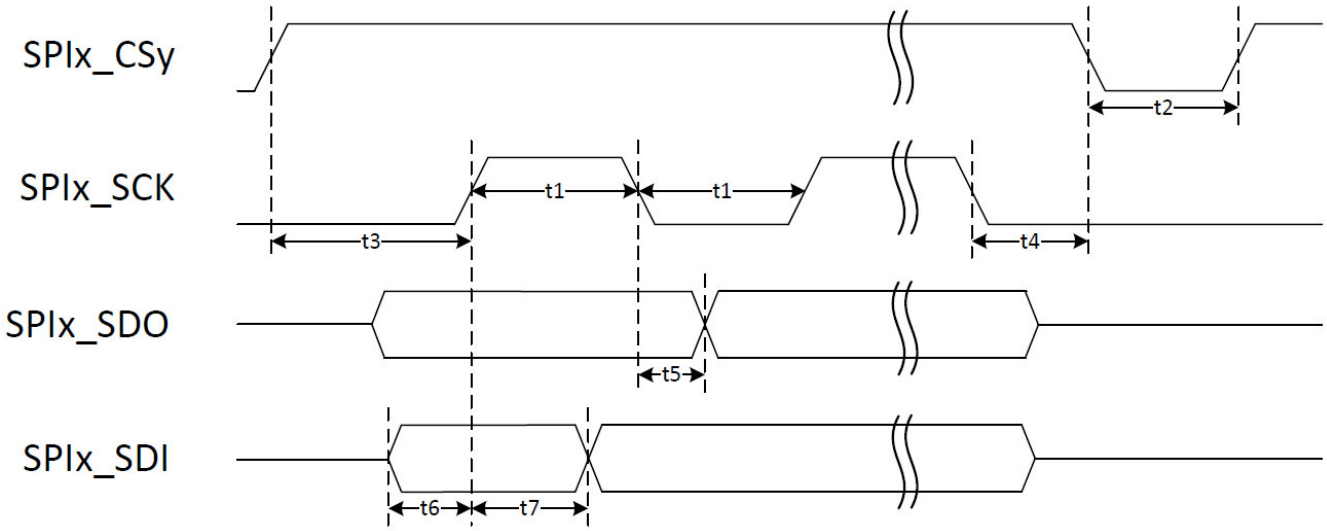


Figure 20. LPSPI Master mode

Table 60. LPSPI timings—Master mode at 60 MHz

ID	Parameter	Min	Max	Unit
—	SPIx_SCLK Cycle frequency	—	60	MHz
t1	SPIx_SCLK High or Low Time–Read SPIx_SCLK High or Low Time–Write	7.5	—	ns
t2	SPIx_CSy pulse width	7.5	—	ns
t3	SPIx_CSy Lead Time(1)	FCLK_PERIOD(2) x (PCSSCK + 1) / $2^{PRESCALE}$ - 3	—	ns

Table 60. LPSPI timings—Master mode at 60 MHz (continued)

ID	Parameter	Min	Max	Unit
t4	SPIx_CSy Lag Time[3]	FCLK_PERIOD[2] x (SCKPCS + 1) / $2^{PRESCALE}$ + 3	—	ns
t5	SPIx_SDO output Delay (CLOAD = 20 pF)	—	3	ns
t6	SPIx_SDI Setup Time	2	—	ns
t7	SPIx_SDI Hold Time	2	—	ns

1 This timing is controllable through CCR.PCSSCK and TCR.PRESCALE registers.

2 FCLK_PERIOD is the period of the functional clock provided to LPSPI module. Maximum allowed frequency is 240 MHz.

3 This timing is controllable through CCR.SCKPCS and TCR.PRESCALE registers.

Table 61. LPSPI timings—Master mode at 40 MHz

ID	Parameter	Min	Max	Unit
—	SPIx_SCLK Cycle frequency	—	40	MHz
t1	SPIx_SCLK High or Low Time–Read SPIx_SCLK High or Low Time–Write	11	—	ns
t2	SPIx_CSy pulse width	11	—	ns
t3	SPIx_CSy Lead Time[1]	FCLK_PERIOD[2] x (PCSSCK + 1) / $2^{PRESCALE}$ + 3	—	ns
t4	SPIx_CSy Lag Time[3]	FCLK_PERIOD[2] x (SCKPCS + 1) / $2^{PRESCALE}$ + 3	—	ns
t5	SPIx_SDO output Delay (CLOAD = 20 pF)	—	5	ns
t6	SPIx_SDI Setup Time	5	—	ns
t7	SPIx_SDI Hold Time	4	—	ns

1 This timing is controllable through CCR.PCSSCK and TCR.PRESCALE registers.

2 FCLK_PERIOD is the period of the functional clock provided to LPSPI module. Maximum allowed frequency is 240 MHz.

3 This timing is controllable through CCR.SCKPCS and TCR.PRESCALE registers.

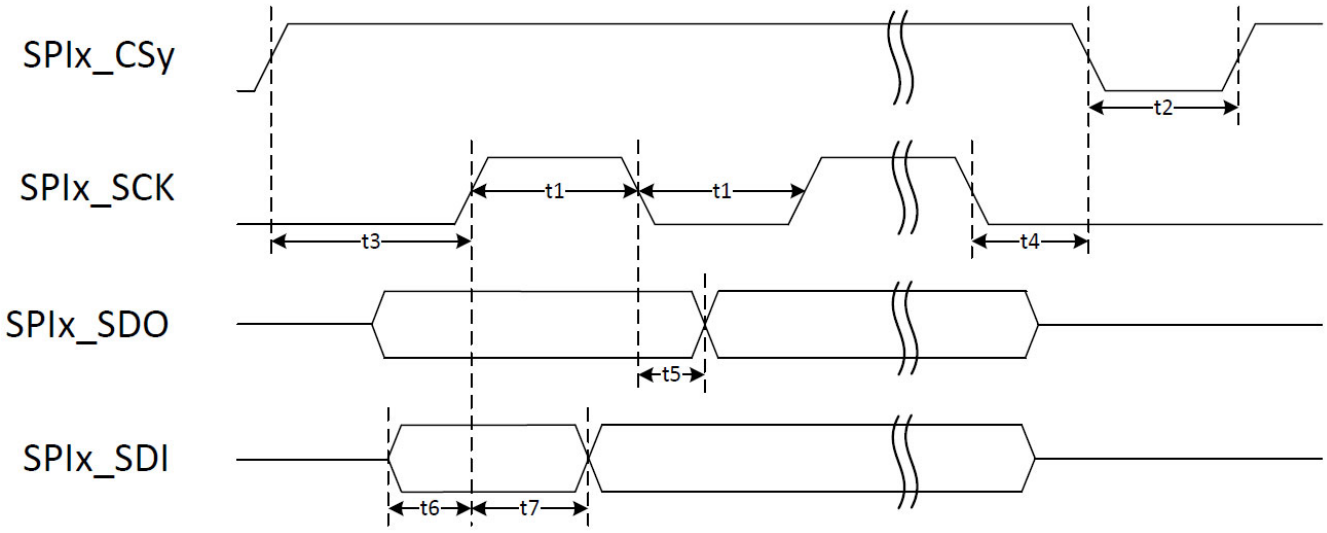


Figure 21. LPSPI Slave mode

Table 62. LPSPI timings—Slave mode at 40 MHz

ID	Parameter	Min	Max	Unit
—	SPI*x*_SCLK Cycle frequency	—	40	MHz
t1	SPI*x*_SCLK High or Low Time–Read SPI*x*_SCLK High or Low Time–Write	11	—	ns
t2	SPI*x*_CSy pulse width	11	—	ns
t3	SPI*x*_CSy Lead Time (CS setup time)	4	—	ns
t4	SPI*x*_CSy Lag Time (CS hold time)	2	—	ns
t5	SPI*x*_SDO output Delay (CLOAD = 20 pF)	—	5	ns
t6	SPI*x*_SDI Setup Time	2	—	ns
t7	SPI*x*_SDI Hold Time	2	—	ns

Table 63. LPSPI timings—Slave mode at 20 MHz

ID	Parameter	Min	Max	Unit
—	SPI*x*_SCLK Cycle frequency	—	20	MHz
t1	SPI*x*_SCLK High or Low Time–Read SPI*x*_SCLK High or Low Time–Write	22	—	ns
t2	SPI*x*_CSy pulse width	22	—	ns
t3	SPI*x*_CSy Lead Time (CS setup time)	4	—	ns

Table 63. LPSPI timings—Slave mode at 20 MHz (continued)

ID	Parameter	Min	Max	Unit
t4	SPI*x*_CSy Lag Time (CS hold time)	2	—	ns
t5	SPI*x*_SDO output Delay (CLOAD = 20 pF)	—	18	ns
t6	SPI*x*_SDI Setup Time	2	—	ns
t7	SPI*x*_SDI Hold Time	2	—	ns

4.10.2 Serial audio interface (SAI) timing parameters

The timings and figures in this section are valid for noninverted clock polarity (I2S_TCR2.BCP = 0b0, I2S_RCR2.BCP = 0b0) and non-inverted frame sync polarity (I2S_TCR4.FSP = 0b0, I2S_RCR4.FSP = 0b0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_TXC / SAI_RXC) and/or the frame sync (SAI_TXFS / SAI_RXFS) shown in the figures below.

The same performance is achieved at both 1.8 V and 3.3 V unless otherwise stated.

NOTE

SAI0 and SAI1 are transmit/receive capable. SAI2 and SAI3 are receive only.

4.10.2.1 SAI Master Synchronous mode

In this mode, transmitter clock and frame sync are used by both transmitter and receiver (I2S_TCR2.SYNC=0b00, I2S_RCR2.SYNC=0b01). In that case, SAI interface requires only 4 signals to be routed: SAI_TXC, SAI_TXFS, SAI_TXD and SAI_RXD. SAI_RXC and SAI_RXFS can be left unconnected. I2S_RCR2.BCI shall be set to 0b1 to get setup and hold times provided in Table 64.

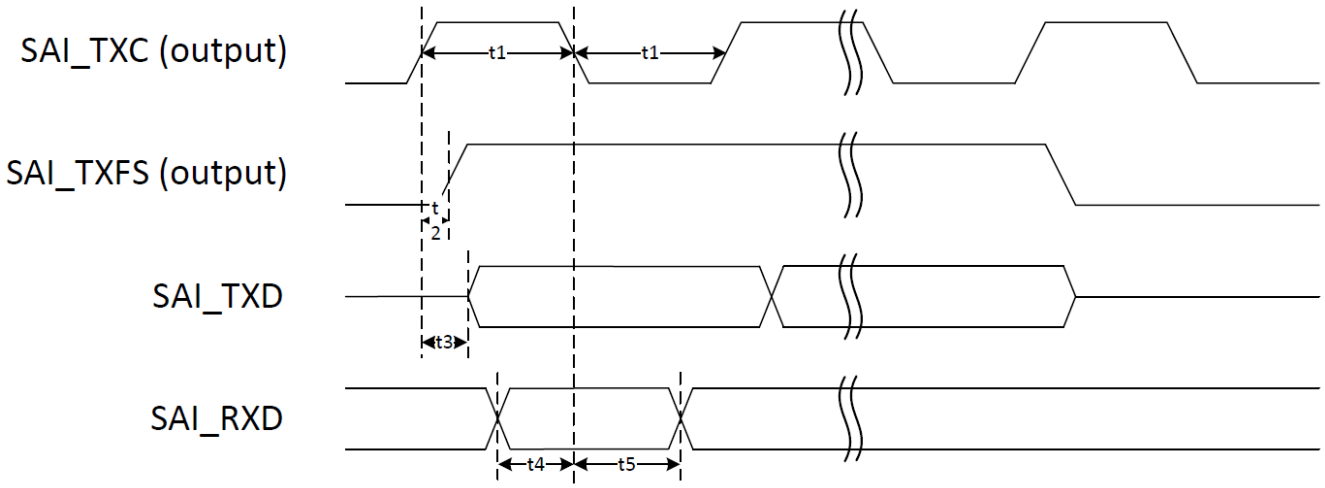


Figure 22. SAI Master Synchronous mode

Table 64. SAI timings—Master Synchronous mode

ID	Parameters	Min	Max	Unit
—	SAI TXC clock frequency	—	49.152	MHz
t1	SAI TXC pulse width low / high	45%	55%	SAI_TXC period
t2	SAI TXFS output valid	—	2	ns
t3	SAI TXD output valid	—	2	ns
t4	SAI RXD input setup	1	—	ns
t5	SAI RXD input hold	4	—	ns

4.10.2.2 SAI Master mode

In this mode, transmitter and/or receiver part are set to bring out transmit and/or receive clock. Frame sync can be either input or output.

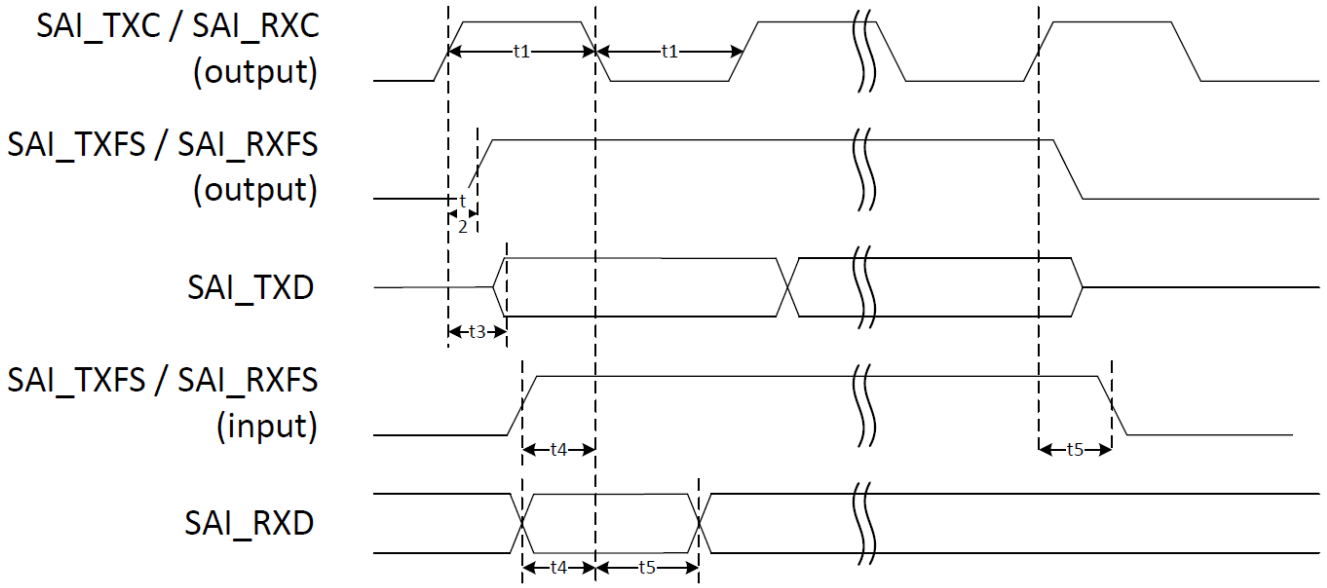


Figure 23. SAI Master mode

Table 65. SAI timings—Master mode

ID	Parameters	Min	Max	Unit
—	SAI TXC / RXC clock frequency[1]	—	49.152	MHz
t1	SAI TXC / RXC pulse width low / high	45%	55%	TXC/RXC period
t2	SAI TXFS / RXFS output valid	—	2	ns

Table 65. SAI timings—Master mode (continued)

ID	Parameters	Min	Max	Unit
t3	SAI TXD output valid	—	2	ns
t4	SAI RXD/RXFS/TXFS input setup	6	—	ns
t5	SAI RXD/RXFS/TXFS input hold	0	—	ns

1 Given the high setup time requirement on inputs, receiver and transmitter, when using frame sync in input, are likely to run at a lower frequency. This frequency will be driven by characteristics of the external component connected to the interface.

4.10.2.3 SAI Slave mode

In this mode, transmitter and/or receiver parts are set to receive transmit and/or receive clock from external world. Frame sync can be either input or output.

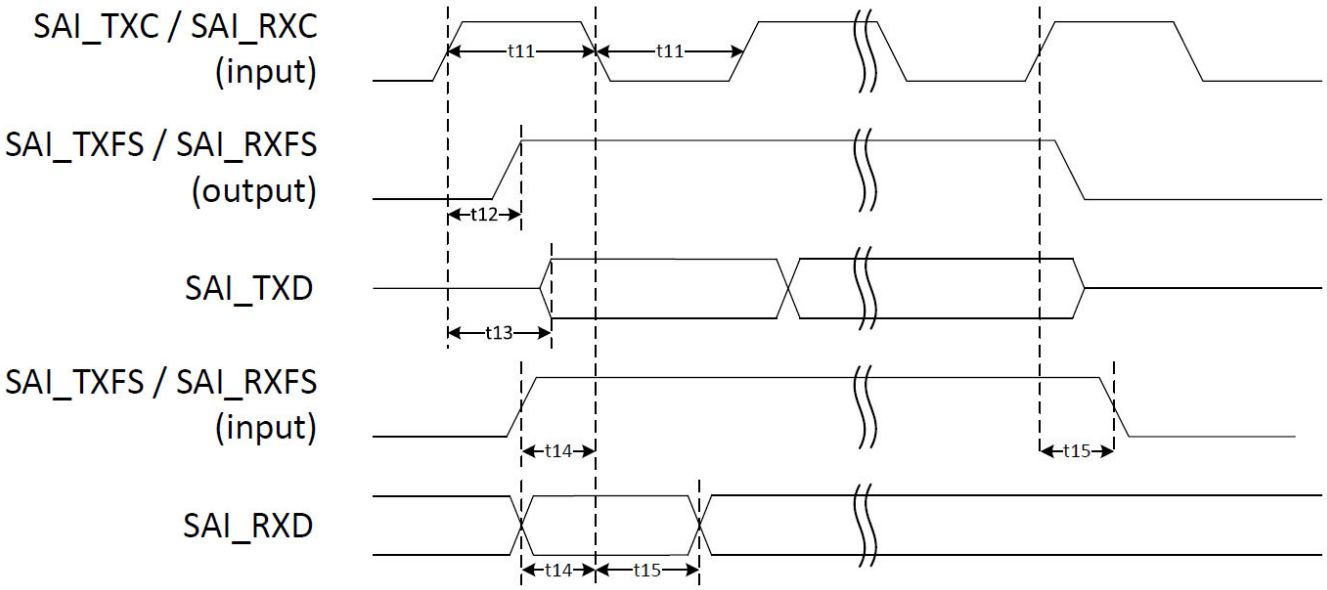


Figure 24. SAI Slave mode

Table 66. SAI timings—Slave mode

ID	Parameters	Min	Max	Unit
—	SAI TXC/RXC clock frequency	—	24.576	MHz
t11	SAI TXC/RXC pulse width low/high	45%	55%	TXC/RXC period
t12	SAI TXFS/RXFS output valid	—	13	ns
t13	SAI TXD output valid	—	13	ns
t14	SAI RXD/RXFS/TXFS input setup	1	—	ns
t15	SAI RXD/RXFS/TXFS input hold	4	—	ns

4.10.3 Enhanced serial audio interface (ESAI)

The same performance is achieved at both 1.8 V and 3.3 V unless otherwise stated.

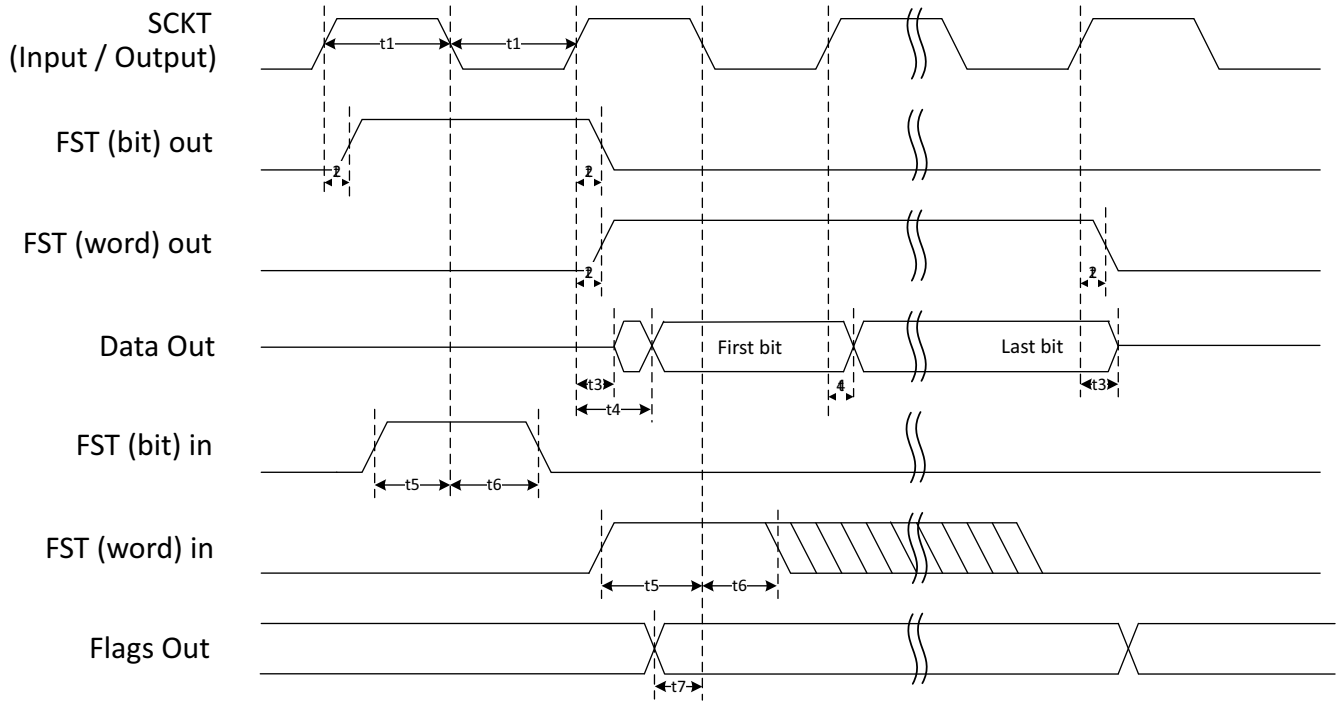


Figure 25. ESAI Transmit timing

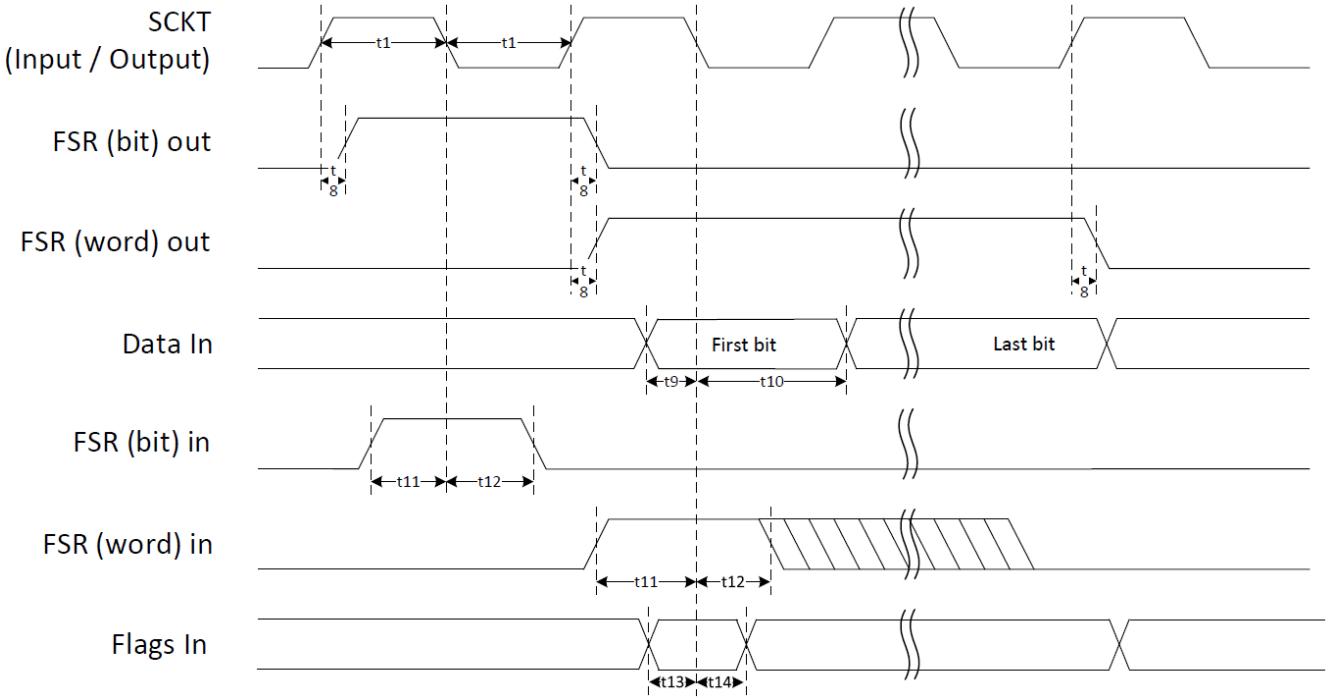


Figure 26. ESAI Receive timing

The following table shows the interface timing values. The ID field in the table refers to timing signals found in Figure 25 and Figure 26.

Table 67. Enhanced Serial Audio Interface (ESAI) Timing

ID	Parameters	Min	Max	Condition[1]	Unit
—	Clock frequency	—	24.576	—	MHz
t1	SCKT / SCKT pulse width high / low	45%	55%	—	SCKT / SCKR period
t2	FST output delay	—	10 2	x ck i ck	ns
t3	TX data - high impedance / valid data	—	9 1	x ck i ck	ns
t4	TX data output delay	—	10 2	x ck i ck	ns
t5	FST - setup requirement	—	2 10	x ck i ck	ns
t6	FST - hold requirement	—	2 0	x ck i ck	ns
t7	Flag output delay		10 2	x ck i ck	ns

Table 67. Enhanced Serial Audio Interface (ESAI) Timing (continued)

ID	Parameters	Min	Max	Condition[1]	Unit
t8	FSR output delay		7 4	x ck i ck a	ns
t9	RX data pins - setup requirement	2 10	—	x ck i ck	ns
t10	RX data pins - hold requirement	2 0	—	x ck i ck	ns
t11	FSR - setup requirement	2 10	—	x ck i ck a	ns
t12	FSR - hold requirement	2 0	—	x ck i ck a	ns
t13	Flags - setup requirement	2 10	—	x ck i ck s	ns
t14	Flags - hold requirement	2 0	—	x ck i ck s	ns
—	RX_HF_CLK / TX_HX_CLK clock cycle	20	—	—	ns
—	TX_HF_CLK input to SCKT		10	—	ns
—	RX_HF_CLK input to SCKR		10	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode (SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode (SCKT and SCKR are the same clock)

4.10.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, including:

- SD3.1/eMMC5.1 High-Speed mode AC Timing
- eMMC5.1 DDR 52 mode/SD3.1 DDR 50 mode timing
- HS400 AC timing—eMMC 5.1 only
- HS200 Mode Timing
- SDR50/SDR104 AC Timing

4.10.4.1 SD3.1/eMMC5.1 High-Speed mode AC Timing

The following figure depicts the timing of SD3.1/eMMC5.1 High-Speed mode, and Table 68 lists the timing characteristics.

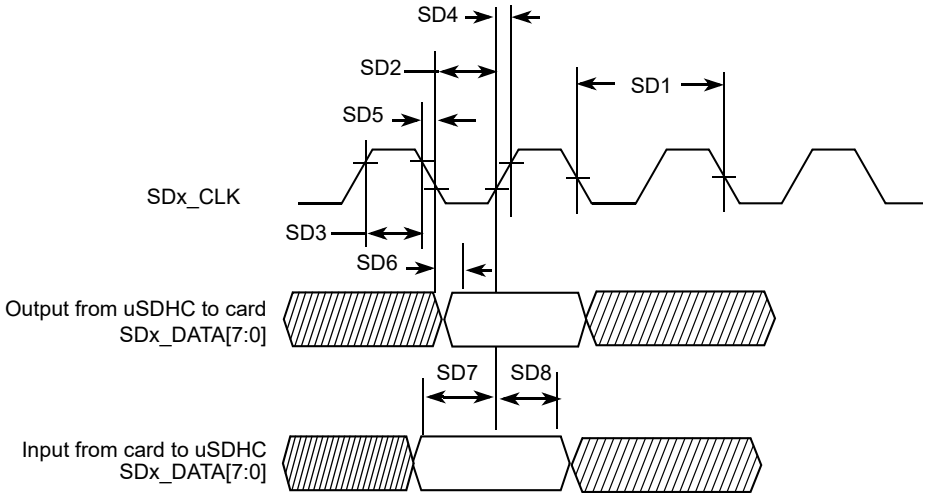


Figure 27. SD3.1/eMMC5.1 High-Speed mode Timing

Table 68. SD3.1/eMMC5.1 High-Speed mode interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SD_CMD, SD_DATA (Reference to SD_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns
eSDHC Input/Card Outputs SD_CMD, SD_DATA (Reference to SD_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.10.4.2 eMMC5.1 DDR 52 mode/SD3.1 DDR 50 mode timing

The following figure depicts the timing of eMMC5.1 DDR 52 mode/SD3.1 DDR 50 mode, and Table 69 lists the timing characteristics. Be aware that only SD*x*_DATA is sampled on both edges of the clock (not applicable to SD_CMD).

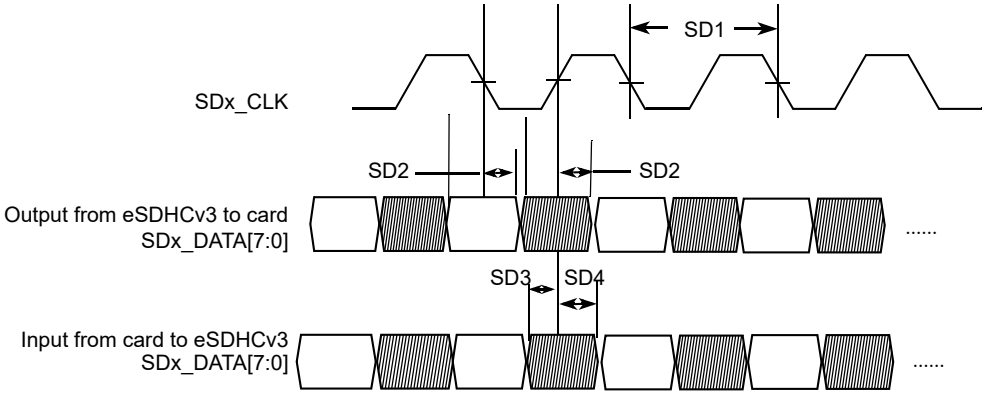


Figure 28. eMMC 5.1 timing

Figure 29. eMMC5.1 DDR 52 mode/SD3.1 DDR 50 mode interface timing

Table 69. eMMC5.1 DDR 52 mode/SD3.150 mode interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock[1]					
SD1	Clock Frequency (eMMC5.1 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.1 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SD*x*_DATA*x* (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.8	6.8	ns
uSDHC Input / Card Outputs SD_CMD, SD*x*_DATA*x* (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

1 Clock duty cycle will be in the range of 47% to 53%.

4.10.4.3 HS400 AC timing—eMMC 5.1 only

Figure 30 depicts the timing of HS400. Table 70 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for

HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6 and SD7 parameters in Table 72 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

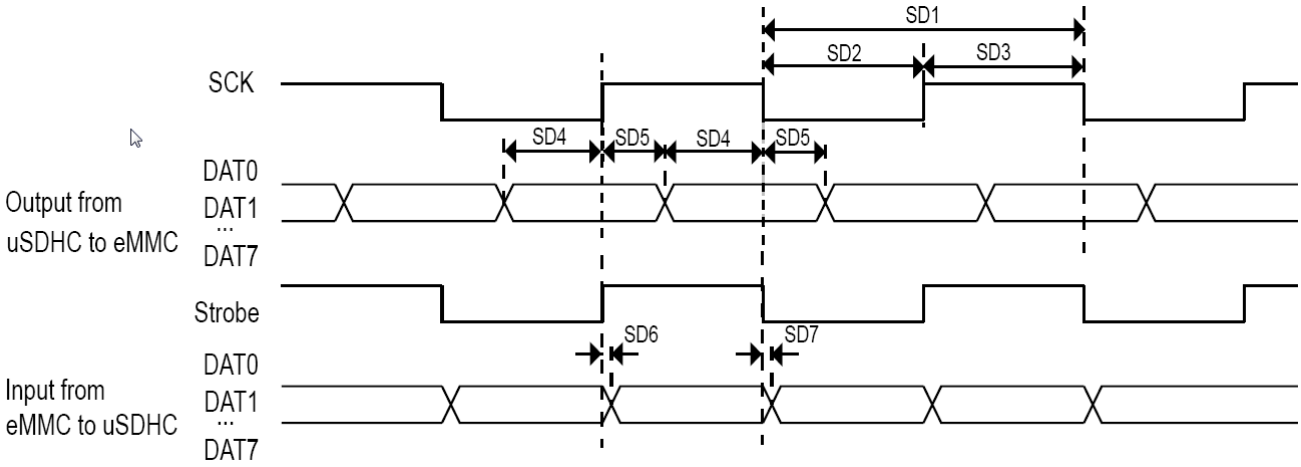


Figure 30. HS400 timing

Table 70. HS400 interface timing specifications

ID	Parameter	Symbols	Min	Max	Unit
Card Input clock					
SD1	Clock Frequency	fPP	0	200	Mhz
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card inputs DAT (Reference to SCK)					
SD4	Output Skew from Data of Edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output Skew from Edge of SCK to Data	t_{OSkew2}	0.45	—	ns
uSDHC input/Card Outputs DAT (Reference to Strobe)					
SD6	uSDHC input skew	t_{RQ}	—	0.45	ns
SD7	uSDHC hold skew	t_{RQH}	—	0.45	ns

4.10.4.4 HS200 Mode Timing

The following figure depicts the timing of HS200 mode, and Table 71 lists the HS200 timing characteristics.

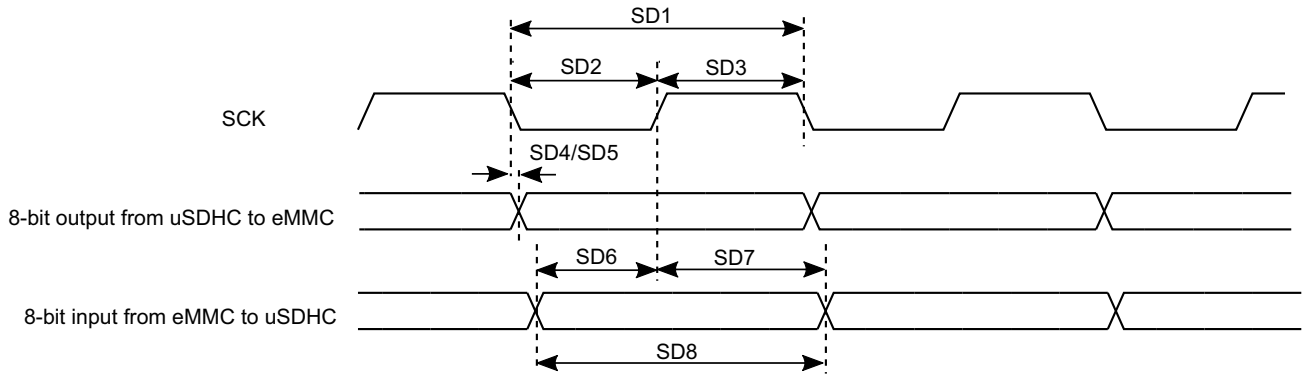


Figure 31. HS200 Mode Timing

Table 71. HS200 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD2	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5*t_{CLK}$	—	ns

[1]HS200 is for 8 bits while SDR104 is for 4 bits.

4.10.4.5 SDR50/SDR104 AC Timing

The following figure depicts the timing of SDR50/SDR104, and Table 72 lists the SDR50/SDR104 timing characteristics.

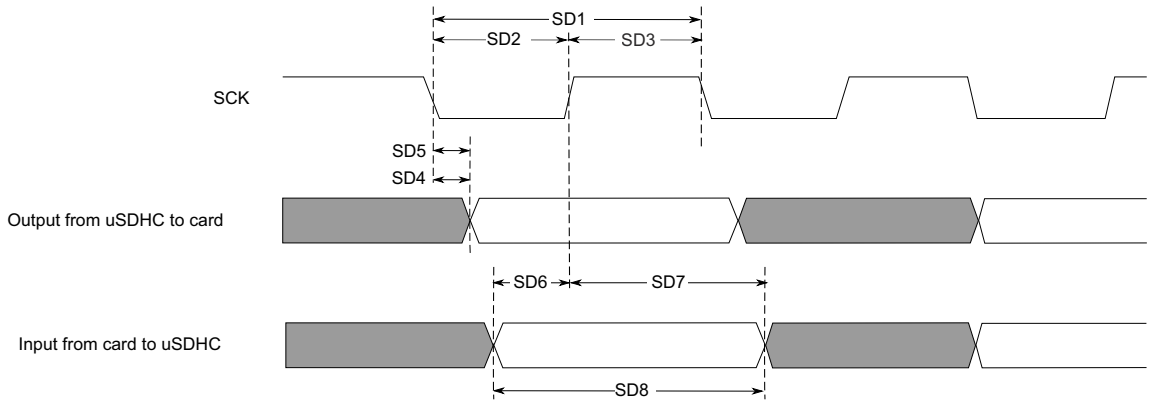


Figure 32. SDR50/SDR104 timing

Table 72. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

4.10.4.6 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC 5.1 and eMMC 5.1 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2, and NVCC_SD3 supplies are identical to those shown in "," and Table 32, "Dual-voltage 1.8 V GPIO DC parameters," on page 39Table 33, "Dual-voltage 3.3 V GPIO DC parameters," on page 40.

4.10.5 Ethernet Controller (ENET) AC Electrical Specifications

ENET interface supporting RGMII protocol in delay and non-delay mode. RGMII is used to support up to 1000 Mbps Ethernet as well as RMII protocol. RMII is used to support up to 100 Mbps Ethernet.

NOTE

Both ENET0 and ENET1 support RGMII at 1.8 V and 2.5 V, and RMII at 3.3 V.

Table 73. RGMII/RMII pin mapping

Pin name[1]	RGMII	RMII	Comment[2]
ENET*x*_RGMII_TXC	RGMII_TXC	RCLK50M	RCLK50M can be an input or an output. It's using different Alternate pin muxing modes. Refer to pin muxing for details.
ENET*x*_RGMII_TX_CTL	RGMII_TX_CTL	RMII_TXEN	—
ENET*x*_RGMII_TXD0	RGMII_TXD0	RMII_TXD0	—
ENET*x*_RGMII_TXD1	RGMII_TXD1	RMII_TXD1	—
ENET*x*_RGMII_TXD2	RGMII_TXD2	N/A	—
ENET*x*_RGMII_TXD3	RGMII_TXD3	N/A	—
ENET*x*_RGMII_RXC	RGMII_RXC	N/A	—
ENET*x*_RGMII_RX_CTL	RGMII_RX_CTL	RMII_CRS_DV	—
ENET*x*_RGMII_RXD0	RGMII_RXD0	RMII_RXD0	—
ENET*x*_RGMII_RXD1	RGMII_RXD1	RMII_RXD1	—
ENET*x*_RGMII_RXD2	RGMII_RXD2	RMII_RXER	RMII_RXER is mapped on ALT1 mode of pin muxing.
ENET*x*_RGMII_RXD3	RGMII_RXD3	N/A	—
ENET*x*_REFCLK_125M_25M	RGMII_REF_CLK	N/A	RGMII_REF_CLK is optional for RGMII operation and dependent on the intended clock configuration.
ENET*x*_MDIO	RGMII_MDIO	RMII_MDIO	—
ENET*x*_MDC	RGMII_MDC	RMII_MDC	—

1 *x* can be 0 or 1.

2 Except for RCLK50M and RMII_RXER, all other RMII functions are using the same pin muxing mode as RGMII.

4.10.5.1 RGMII

4.10.5.1.1 No-Internal-Delay mode

This mode corresponds to the RGMIIv1.3 specification.

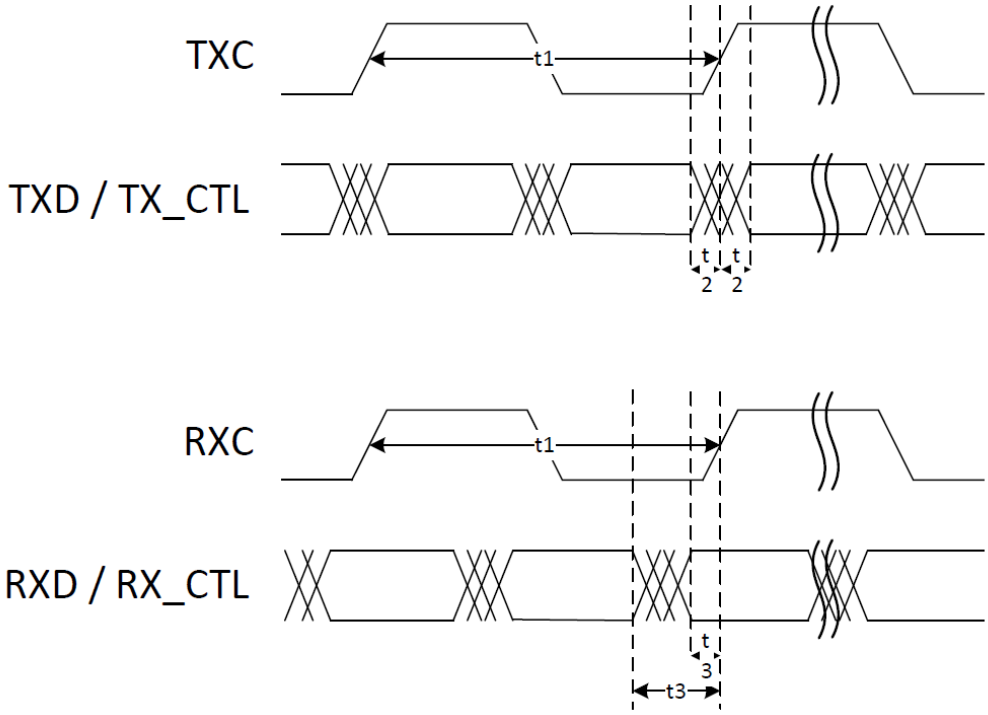


Figure 33. RGMII timing diagram—No-Internal-Delay mode

Table 74. RGMII timings—No-Internal-Delay mode

ID	Parameter	Min	Typ	Max	Unit
	TXC / RXC frequency	—	125	—	MHz
t1	Clock cycle	7.2	8	8.8	ns
t2	Data to clock output skew	-500	—	500	ps
t3	Data to clock input skew[1(1)]	1	—	2.6	ns

1 This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.

4.10.5.1.2 Internal-delay mode

This mode corresponds to RGMIIv2.0 specification. The interface is still operating at 2.5 V. 1.5 V is not supported.

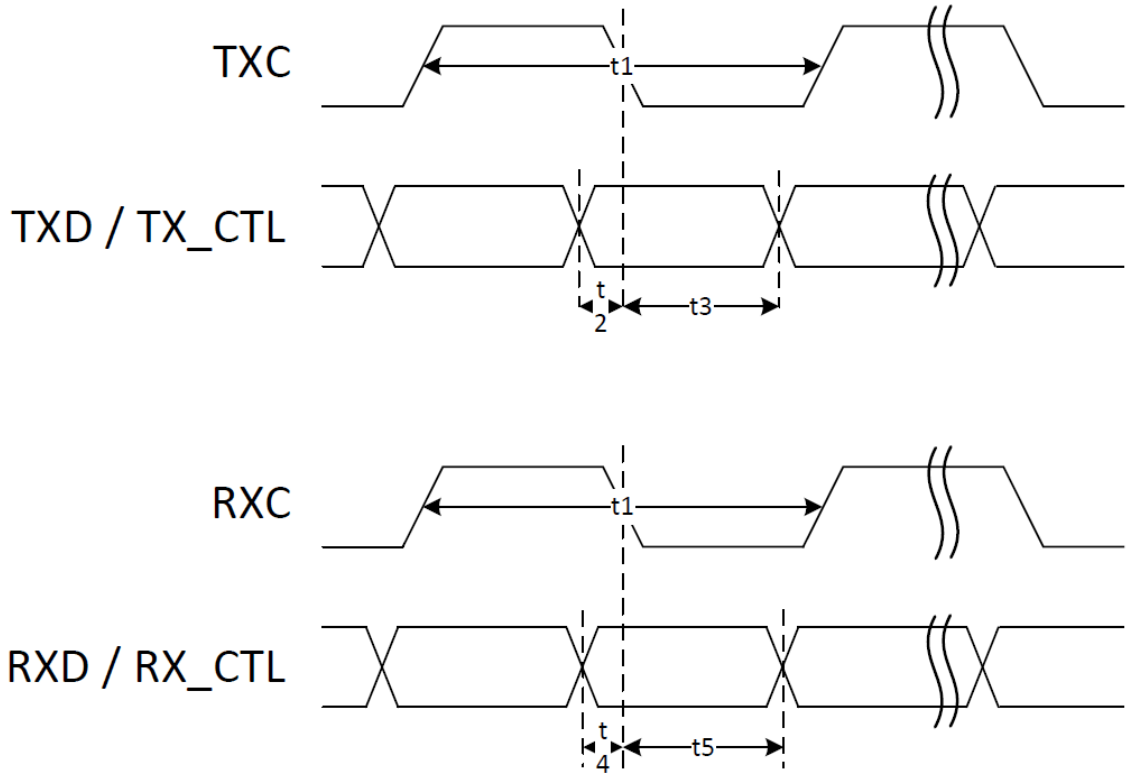


Figure 34. RGMII timing diagram—Internal-Delay mode

Table 75. RGMII timing—Internal-Delay mode

ID	Parameter	Min	Typ	Max	Unit
	TXC / RXC frequency	—	125	—	MHz
t1	Clock cycle	7.2	8	8.8	ns
t2	TXD setup time	1.2	—	—	ns
t3	TXD hold time	1.2	—	—	ns
t4	RXD setup time	0	—	—	ns
t5	RXD hold time	2.5	—	—	ns

4.10.5.2 RMII

RMII interface is matching RMII v1.2 specification. In RMII mode, the reference clock can be generated internally and provided to the PHY through RCLK50M_OUT. Or, it come from and external 50MHz clock generator which is connected to the PHY and to i.MX8 through RCLK50M_IN pin.

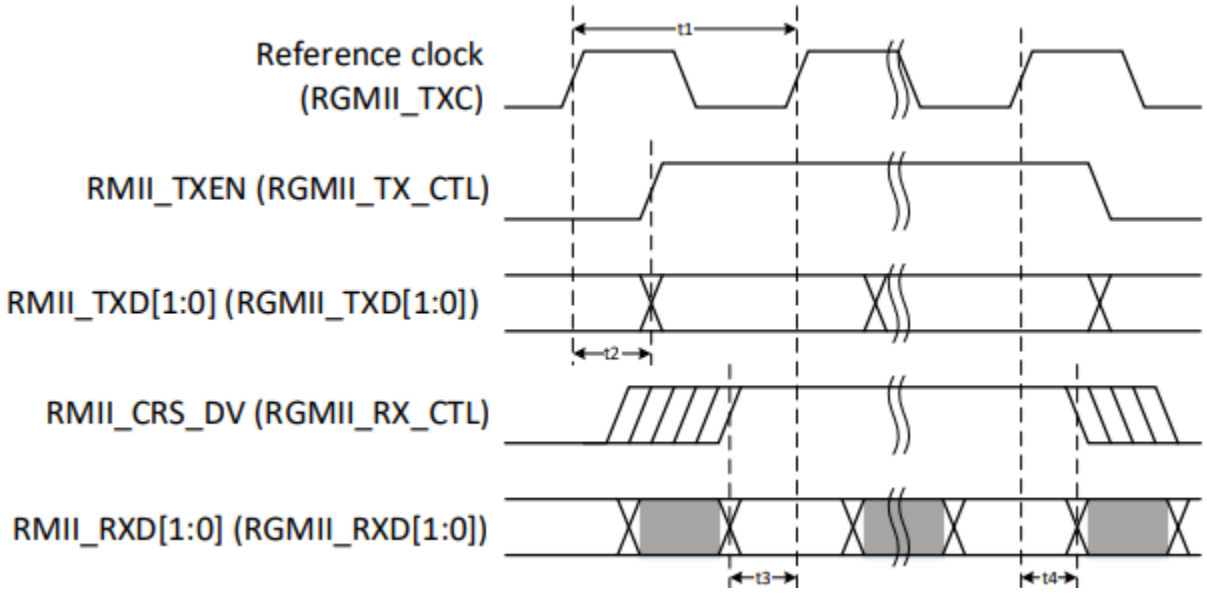


Figure 35. RMII timing diagram

Timings in table below are covering both cases: reference clock generated internally or externally.

Table 76. RMII timing

ID	Parameter	Min	Typ	Max	Unit
t1	Reference clock	—	50	—	MHz
	Reference clock accuracy	—	—	50	ppm
	Reference clock duty-cycle	35	—	65	%
t2	RMII_TXEN, RMII_TXD output delay	2	—	12	ns
t3	RMII_CRS_DV, RMII_RXD setup time	4	—	—	ns
t4	RMII_CRS_DV, RMII_RXD hold time	2	—	—	ns

4.10.5.3 MDIO

MDIO is the control link used to configure Ethernet PHY connected to i.MX8 device.

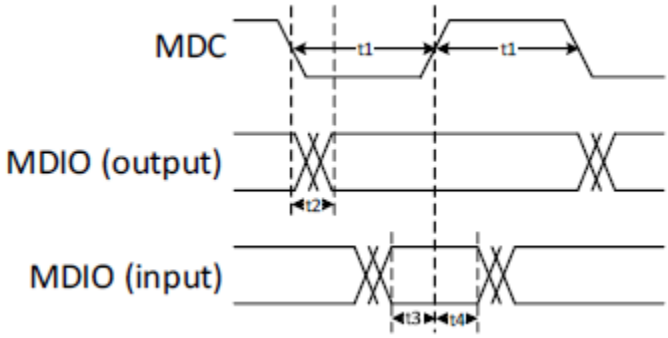


Figure 36. MDIO timing diagram

Table 77. MDIO timing

ID	Parameter	Min	Typ	Max	Unit
	MDC frequency	—	2.5	—	MHz
t1	MDC high / low pulse width	180	—	—	%
t2	MDIO output delay	0	—	20	ns
t3	MDIO setup time	10	—	—	ns
t4	MDIO hold time	10	—	—	ns

4.10.6 CAN network AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification. The processor has three CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the device reference manual to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.10.7 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. The following figure depicts the timing of the I²C module, and Table 78 lists the I²C module timing characteristics.

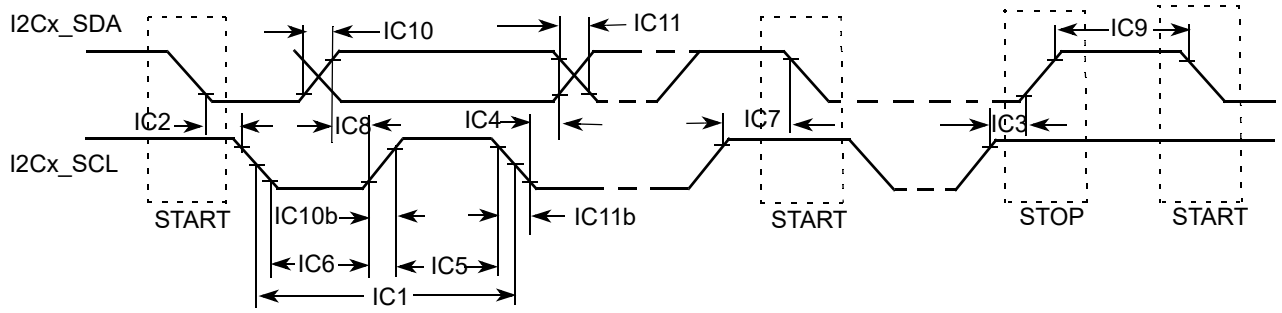


Figure 37. I²C bus timing

Table 78. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10/IC10b	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11/IC11b	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal in order to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

Table 79. I2C timing

		Fast Mode Plus		High Speed[1]		Unit
ID	Parameter	Min	Max	Min	Max	
IC1	SCL clock frequency	—	1	—	3.4	MHz
IC2	Hold time (repeated) START condition	260	—	160	—	ns
IC3	Set-up time for STOP condition	260	—	160	—	ns
IC4	Data hold time	0	—	0	70	ns
IC5	HIGH Period of I2Cx_SCL Clock	260	—	60	—	ns
IC6	LOW Period of the I2Cx_SCL Clock	500	—	160	—	ns
IC7	Set-up time for a repeated START condition	260	—	160	—	ns
IC8	Data set-up time	50	—	10	—	ns
IC9	Bus free time between a STOP and START condition	500	—	150	—	ns
IC10	Rise time of I2Cx_SDA signals	—	120	10	80	ns
IC11	Fall time of I2Cx_SDA signals	12 (@3.3 V) 6.5 (@1.8 V)	120	10	80	ns
IC10b	Rise time of I2Cx_SCL signals	—	120	10	40	ns
IC11b	Fall time of I2Cx_SCL signals	12 (@3.3 V) 6.5 (@1.8 V)	120	10	40	ns
IC12	Capacitive load for each bus line (Cb)	—	550	—	100	pF

1 High-speed mode is only available for I2C modules in DMA, SCU and Cortex-M4 subsystems.

4.10.8 MIPI-DSI/LVDS combo display output specifications

The physical pins of the combo display output controller can be used in LVDS mode or in DSI display mode.

4.10.8.1 MIPI-DSI/LVDS display bridge module parameters

Maximum frequency support for combination MIPI-DSI/LVDS modules:

Table 80. MIPI-DSI/LVDS combo pins

Function[1,2]	Channel A	Channel B
DSI	DSI up to 1.05 Gb/per lane	DSI up to 1.05 Gb/per lane
Mix	4 pairs LVDS up to 1.05 Gb per pair	DSI up to 1.05 Gb/per lane
Mix	DSI up to 1.05 Gb/per lane	4 pairs LVDS up to 1.05 Gb per pair

Table 80. MIPI-DSI/LVDS combo pins (continued)

Function[1,2]	Channel A	Channel B
LVDS (single channel)	4 pairs LVDS up to 1.05 Gb per pair	4 pairs LVDS up to 1.05 Gb per pair
LVDS (dual channel)	8 pairs LVDS up to 595 Mb per pair	

1 For DSI the maximum clock speed is 1.05 GHz.

2 For LVDS in single-channel operation the maximum clock speed is 150 MHz; in dual-channel operation with a single synchronized clock the maximum clock speed is 85 MHz.

4.10.8.2 LVDS display bridge (LDB) module electrical specifications

The MIPI DSI/LVDS interface is compatible with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits."

Table 81. LVDS Display Bridge (LDB) Electrical Specifications

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V_{OD}	100 Ω Differential load	0.25	0.4	V
Output Voltage High	Voh	100 Ω differential load (0 V Diff—Output High Voltage static)	—	1.475	V
Output Voltage Low	Vol	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.925	—	V
Offset Static Voltage	V_{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.125	1.275	V
VOS Differential	V_{OSDIFF}	Difference in V_{OS} between a One and a Zero state	—	—	mV
Output short-circuited to GND	ISA ISB	With the output common shorted to GND	—	40	mA
Output short current	ISAB		—	12	mA

4.10.8.3 MIPI-DSI HS-TX specifications

Table 82. MIPI high-speed transmitter DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{CMTX}[1]	High Speed Transmit Static Common Mode Voltage	150	200	250	mV
$\lvert\Delta V_{CMTX}\rvert_{(1,0)}$	V_{CMTX} mismatch when Output is Differential-1 or Differential-0	—	—	5	mV
$\lvert V_{OD}\rvert$[1]	High Speed Transmit Differential Voltage	140	200	270	mV

Table 82. MIPI high-speed transmitter DC specifications (continued)

Symbol	Parameter	Min	Typ	Max	Unit
$\|\Delta V_{OD}\|$	V_{OD} mismatch when Output is Differential-1 or Differential-0	—	—	10	mV
V_{OHHS}[1]	High Speed Output High Voltage	—	—	360	mV
Z_{OS}	Single Ended Output Impedance	40	50	62.5	Ω
ΔZ_{OS}	Single Ended Output Impedance Mismatch	—	—	10	%

1 Value when driving into load impedance anywhere in the Z_{ID} range.

Table 83. MIPI high-speed transmitter AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
$\Delta V_{CMTX(HF)}$	Common-level variations above 450 MHz	—	—	15	mVRMS
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450 MHz	—	—	25	mVPEAK
t_R and t_F[1]	Rise Time and Fall Time (20% to 80%)	100	—	0.35 UI	ps

1 UI is the long-term average unit interval.

4.10.8.4 MIPI-DSI LP-TX specifications

Table 84. MIPI low-power transmitter DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}[1]	Thevenin Output High Level	1.1	1.2	1.3	V
V_{OL}	Thevenin Output Low Level	–50	—	50	mV
Z_{OLP}[2]	Output Impedance of Low Power Transmitter	110	—	—	Ω

1 This specification can only be met when limiting the core supply variation from 1.1 V till 1.3 V.

2 Although there is no specified maximum for ZOLP, the LP transmitter output impedance ensures the TRLP/TFLP specification is met.

Table 85. MIPI low-power transmitter AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
T_{RLP}/T_{FLP}[1]	15% to 85% Rise Time and Fall Time	—	—	25	ns
T_{REOT}[1,2,3]	30% to 85% Rise Time and Fall Time	—	—	35	ns
$T_{LP\text{-}PULSE\text{-}TX}$[4]	Pulse width of the LP exclusive-OR clock: First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	—	—	ns
	Pulse width of the LP exclusive-OR clock: All other pulses	20	—	—	ns
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock	90	—	—	ns

Table 85. MIPI low-power transmitter AC specifications (continued)

Symbol	Parameter	Min	Typ	Max	Unit
$\delta V/\delta t_{SR}$ [1,5,6,7]	Slew Rate @ C_{LOAD}= 0 pF	30	—	500	mV/ns
	Slew Rate @ C_{LOAD}= 5 pF	30	—	200	mV/ns
	Slew Rate @ C_{LOAD}= 20 pF	30	—	150	mV/ns
	Slew Rate @ C_{LOAD}= 70 pF	30	—	100	mV/ns
C_{LOAD}	Load Capacitance	0	—	70	pF

1 C_{LOAD} includes the low equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be < 10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2 ns delay.

2 The rise-time of TREOT starts from the HS common-level at the moment of the differential amplitude drops below 70 mV, due to stopping the differential drive.

3 With an additional load capacitance CCM between 0 to 60 pF on the termination center tap at RX side of the lane.

4 This parameter value can be lower then TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in Low-Power Receiver section.

5 When the output voltage is between 15% and below 85% of the fully settled LP signal levels.

6 Measured as average across any 50 mV segment of the output signal transition.

7 This value represents a corner point in a piecewise linear curve.

4.10.8.5 MIPI-DSI LP-RX specifications

Table 86. MIPI low power receiver DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage	880	—	1.3	mV
V_{IL}	Logic 0 input voltage, not in ULP state	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULP state	—	—	300	mV
V_{HYST}	Input hysteresis	25	—	—	mV

Table 87. MIPI low power receiver AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
e_{SPIKE} [1,2]	Input pulse rejection	—	—	300	V.ps
T_{MIN-RX} [3]	Minimum pulse width response	20	—	—	ns
V_{INT}	Peak Interference amplitude	—	—	200	mV
f_{INT}	Interference frequency	450	—	—	MHz

1 Time-voltage integration of a spike above V_{IL} when in LP-0 state or below VIH when in LP-1 state.

2 An impulse below this value will not change the receiver state.

3 An input pulse greater than this value shall toggle the output.

4.10.8.6 MIPI-DSI LP-CD specifications

Table 88. MIPI contention detector DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IHCD}	Logic 1 contention threshold	450	—	—	mV
V_{ILCD}	Logic 0 contention threshold	—	—	200	mV

4.10.8.7 MIPI-DSI DC specifications

Table 89. MIPI input characteristics DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{PIN}	Pad signal voltage range	–50	—	1350	mV
I_{LEAK}[1]	Pin leakage current	–10	—	10	µA
V_{GNDSH}	Ground shift	–50	—	50	mV
$V_{PIN(absmax)}$[2]	Maximum pin voltage level	–0.15	—	1.45	V
$T_{VPIN(absmax)}$[3]	Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$	—	—	20	ns

1 When the pad voltage is within the signal voltage range between $V_{GNDSH(min)}$ to VOH + $V_{GNDSH(max)}$ and the Lane Module is in LP receive mode.

2 This value includes ground shift.

3 The voltage overshoot and undershoot beyond the V_{PIN} is only allowed during a single 20 ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.

4.10.9 PCIe 3.0 PHY Parameters

The TX and RX eye diagrams specifications are per the template shown in the following figure. The summary of specifications is shown in Table 90 and Table 91. Note that the time closure (1–A OPENING) in the eye templates needs not match jitter specifications in the Standards Specifications, as there are such discrepancies in some Standards Specifications. The design meets the tightest of specifications in case of discrepancy.

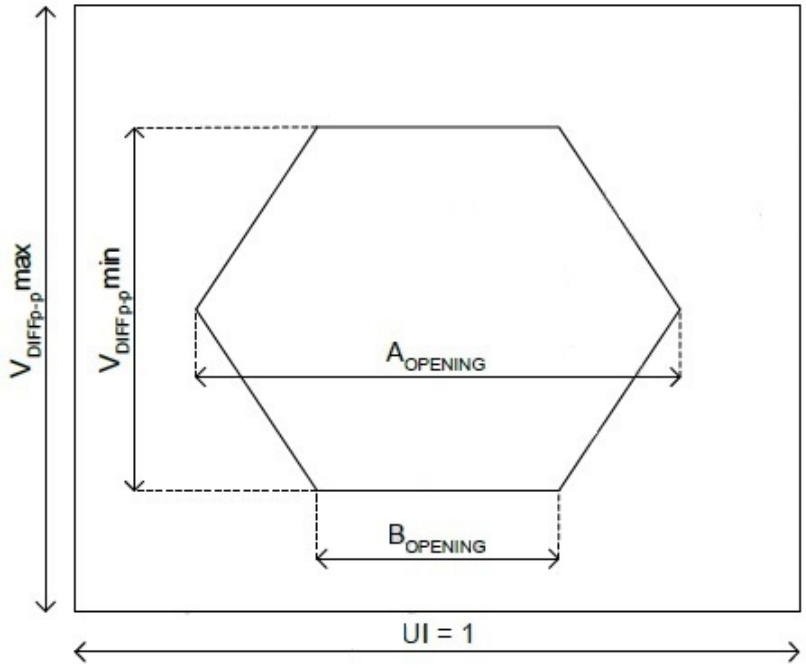


Figure 38. TX and RX eye diagram template

Table 90. PCIe transmitter eye specifications for example standards

	UI	$A_{OPENING}$	$B_{OPENING}$	$A_{OPENING}$	$B_{OPENING}$	$V_{DIFFp-p}$min	$V_{DIFFp-p}$max
	ps	UI		ps		mV	
PCI Express Gen 1 Transition Bit	400	0.75	0	300	0	800	1200[1]
PCI ExpressGen 1 De-emphasized Bit	400	0.75	0	300	0	505	757
PCI Express Gen 2 Transition Bit	200	0.75	0	150	0	800	1200[1]
PCI Express Gen 2 De-emphasized Bit	200	0.75	0	150	0	379	850

1 $V_{DIFFp-p}$ eye opening is limited to VDDIO under matched termination conditions.

Table 91. PCIe receiver eye specifications for example standards

	UI	$A_{OPENING}$	$B_{OPENING}$	$A_{OPENING}$	$B_{OPENING}$	$V_{DIFFp-p}$min	$V_{DIFFp-p}$max
	ps	UI		ps		mV	
PCI Express Gen 1 Transition Bit	400	0.4	0	160	0	175	1200
PCI Express Gen 2 Transition Bit	200	0	0	0	0	100	1200
PCI Express Gen 3 Virtual EYE[1]	125	0.3	0	38	0	25	1300

1 PCIE 3.0 8 GT/s measured using PCIE reference equalizer + CDR per PCIE specification.

Table 92. PCIe differential output driver characteristics (including board and load)

Parameter	Min	Typ	Max	Units	Notes
Output Rise and fall time T_R, T_F	175	—	350	ps	1
Output Rise/Fall matching	—	—	20	%	1, 2
Output skewT_{OSKEW}	—	—	50	ps	—
Initialization time from assertion of TXOE	100	—	—	ns	—
Initialization time from assertion of TXENA	—	10	—	µs	—
Transmission line characteristic impedance (Z_O)	—	50	—	Ω	—
Driver output impedance, single ended (small signal @ Vout=Vcm)	—	1000	—	Ω	—
Output single ended voltage (RS= 33, RT= 50 Ω) V_{OH} I_{OH}@ 6 * I_R V_{OL}	 0.65 -13 -0.20	 0.71 -14.2 0.00	 0.85 -17 0.05	 V mA V	3, 4 3
Output common mode voltage (RS = 33, RT= 50 Ω) $\|V_{OCM}\|$ $\Delta V_{OCM\ (DC)}$ $\Delta V_{OCM\ (AC)}$	 0.25 -0.015 -0.050	 0.375	 0.55 0.015 0.050	 V	 5 6
Buffer induced deterministic jitter (absolute, pk-pk)	—	—	4	ps	7,8
Reference Buffer Dynamic Power (Digital)	—	0.015	0.66	µA	9
Reference Buffer Dynamic Power (Analog)	—	2.8	3.14	mA	9
Output Buffer Dynamic Power (Digital)	—	0.035	1.8	µA	9
Output Buffer Dynamic Power (Analog)	—	18.9	22.11	mA	9

1 When the output is transitioning between logic 0 and logic 1, or logic 1 and logic 0, and driving a terminated transmission line, the outputs monotonically transition between VOL and VOH, VOH, and VOL respectively. Target rise and fall times observed at the receiver and are primarily set by board trace impedance and Load capacitance. Rise and fall times are defined by 25% and 75% crossing points.

2 Calculated as: 2 × (TR–TF) / (TR+ TF)

3 I_R is proportional to the reference current. Measured across RT. The primary contributor to output voltage spread is VDD spread, and so a VDD tighter than ±10% may be required to achieve this spread.

4 Higher output voltages may occur depending on load, power supply, and selected output drive. Higher output voltages may transiently occur during initialization period following TXENA assertion.

5 Peak change in output differential voltage when driving a logic 0 and when driving a logic 1 under DC conditions.

6 Peak change in output differential voltage when driving a logic 0 and when driving a logic 1 under AC conditions.

7 Measured under “clean power supply and ground” conditions, and after de-embedding the jitter of the input, measured over a time span of 1000 cycles

8 Power supply induced jitter is included under this category, and the power supply variation is to be less than 8mVpp. Note that customer has to be uncommonly careful with power supply fidelity due to the small jitter numbers.

9 Power consumption is simulated under the following conditions:
Typ: TT, VDD=1.0 V, VD18=1.8 V, 25 °C
Max: FF, VDD=1.1 V, VD18=1.98 V, 125 °C
Dynamic: TXENA=1, TXOE=1
Static: TXENA=0, TXOE=1

4.10.9.1 PCIE_REXT reference resistor connection

The following figure shows the PCIE_REXT reference resistor connection.

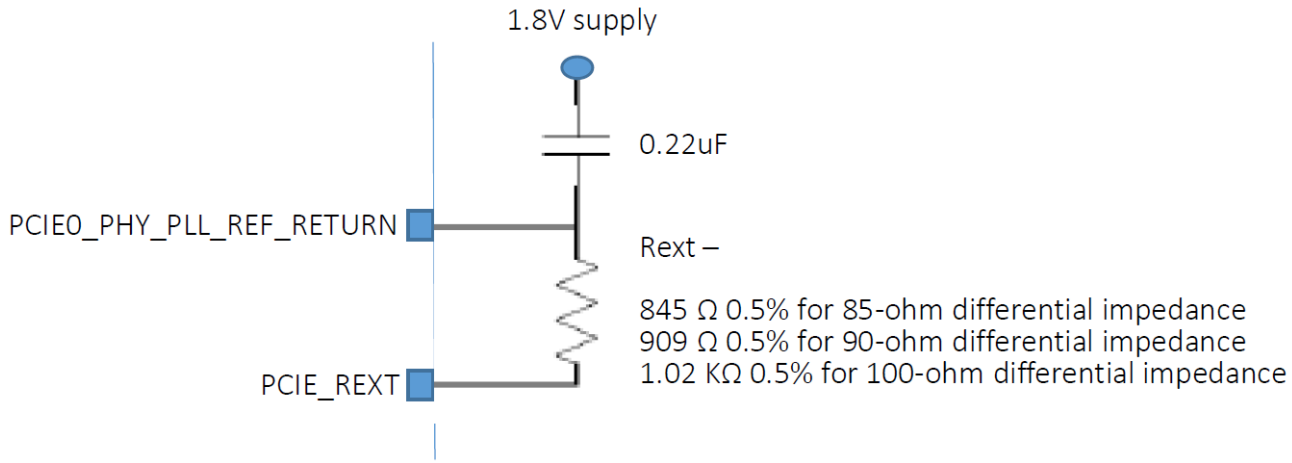


Figure 39. PCIE_REXT reference resistor connection

4.10.9.2 PCIE_REF_CLK

Contact an NXP representative to obtain the hardware development guide for this device, which contains details on the PCIe reference clock requirements.

4.10.10 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

The following figure depicts the timing of the PWM, and Table 93 lists the PWM timing parameters.

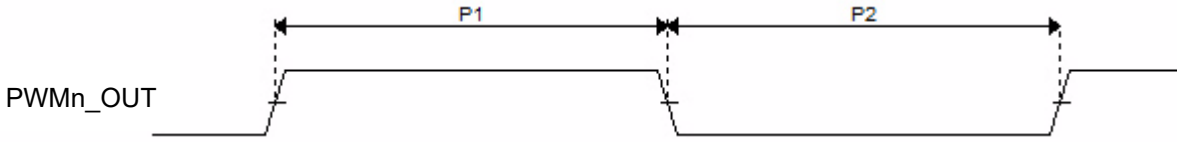


Figure 40. PWM Timing

Table 93. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
—	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

4.10.11 LCD controller (LCDIF) parameters

Figure 41 shows the LCDIF timing, and the table below lists the timing parameters.

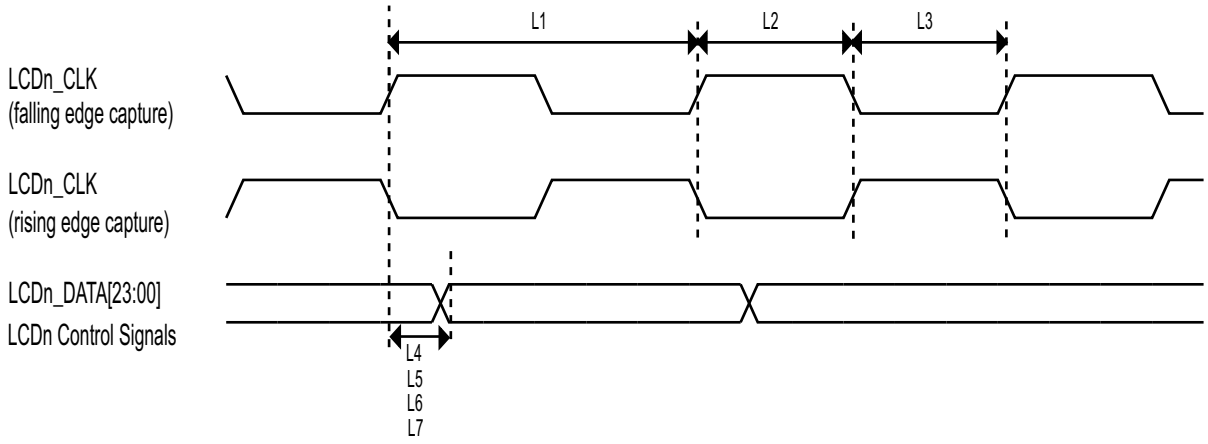


Figure 41. LCD Timing

Table 94. LCD Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency	tCLK(LCD)	—	80	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	6	—	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	6	—	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1	1	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1	1	ns
L6	LCD pixel clock high to control signal valid (falling edge capture)	td(CLKH-CTRLV)	-1	1	ns
L7	LCD pixel clock low to control signal valid (rising edge capture)	td(CLKL-CTRLV)	-1	1	ns

4.10.11.1 LCDIF signal mapping

The table below lists the details about the mapping signals.

Table 95. LCD Signal Parameters

Pin name	8-bit DOTCLK LCD IF	16-bit DOTCLK LCD IF	18-bit DOTCLK LCD IF	24-bit DOTCLK LCD IF	8-bit DVI LCD IF
LCD_RS	—	—	—	—	CCIR_CLK
LCD_VSYNC* (Two options)	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	—
LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	—

Table 95. LCD Signal Parameters (continued)

LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	—
LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	—
LCD_D23	—	—	—	R[7]	—
LCD_D22	—	—	—	R[6]	—
LCD_D21	—	—	—	R[5]	—
LCD_D20	—	—	—	R[4]	—
LCD_D19	—	—	—	R[3]	—
LCD_D18	—	—	—	R[2]	—
LCD_D17	—	—	R[5]	R[1]	—
LCD_D16	—	—	R[4]	R[0]	—
LCD_D15 / VSYNC*	—	R[4]	R[3]	G[7]	—
LCD_D14 / HSYNC**	—	R[3]	R[2]	G[6]	—
LCD_D13 / LCD_DOTCLK **	—	R21]	R[1]	G[5]	—
LCD_D12 / ENABLE**	—	R[1]	R[0]	G[4]	—
LCD_D11	—	R[0]	G[5]	G[3]	—
LCD_D10	—	G[5]	G[4]	G[2]	—
LCD_D9	—	G[4]	G[3]	G[1]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D7	R[2]	G[2]	G[1]	B[7]	Y/C[7]
LCD_D6	R[1]	G[1]	G[0]	B[6]	Y/C[6]
LCD_D5	R[0]	G[0]	B[5]	B[5]	Y/C[5]
LCD_D4	G[2]	B[4]	B[4]	B[4]	Y/C[4]
LCD_D3	G[1]	B[3]	B[3]	B[3]	Y/C[3]
LCD_D2	G[0]	B[2]	B[2]	B[2]	Y/C[2]
LCD_D1	B[1]	B[1]	B[1]	B[1]	Y/C[1]
LCD_D0	B[0]	B[0]	B[0]	B[0]	Y/C[0]
LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	—
LCD_BUSY / LCD_VSYNC	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	—

4.10.12 FlexSPI (Quad SPI/Octal SPI) timing parameters

The FlexSPI interface can work in SDR or DDR modes. It can operate up to 60 MHz at 3.3 V, 166 MHz at 1.8 V SDR mode or 200 MHz at 1.8 V DDR mode. It supports single-ended and differential DQS signaling.

FlexSPI supports the following clocking scheme for a read data path:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPIn_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPIn_MCR0[RXCLKSRC] = 0x1). It means the I/O cannot be used for another feature.
- Read strobe provided by memory device and input from DQS pad (FlexSPIn_MCR0[RXCLKSRC] = 0x3)

4.10.12.1 SDR mode

4.10.12.1.1 SDR mode timing diagrams

The following write timing diagram is valid for any FlexSPI*n*_MCR0[RXCLKSRC] value.

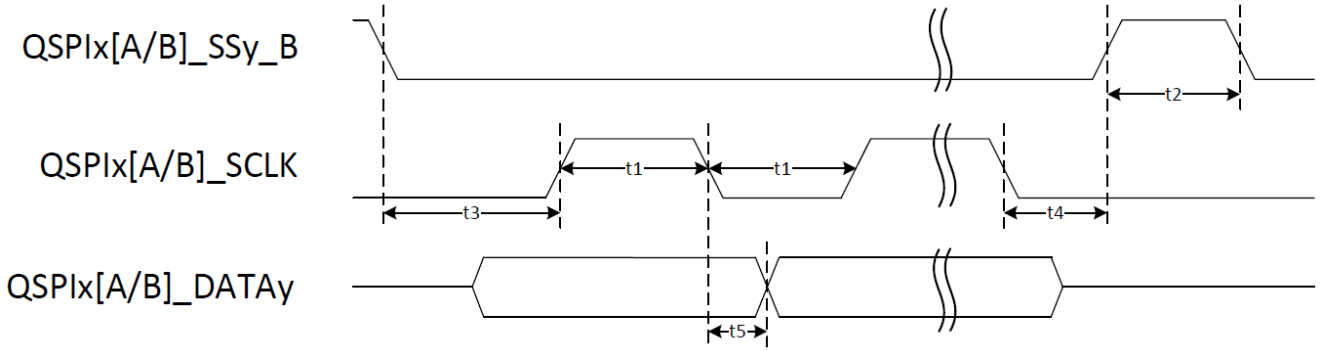


Figure 42. FlexSPI write timing diagram (SDR mode)

The following read timing diagram is valid for FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 or 0x1.

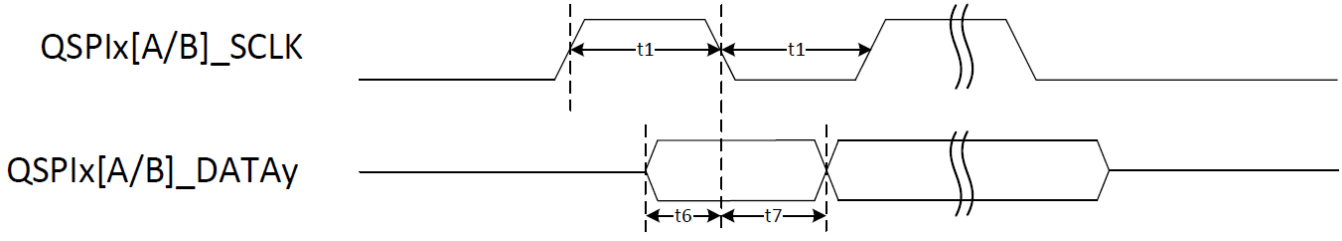


Figure 43. FlexSPI read timing diagram (SDR mode)

The following read timing diagram is valid for FlexSPI*n*_MCR0[RXCLKSRC] = 0x3.

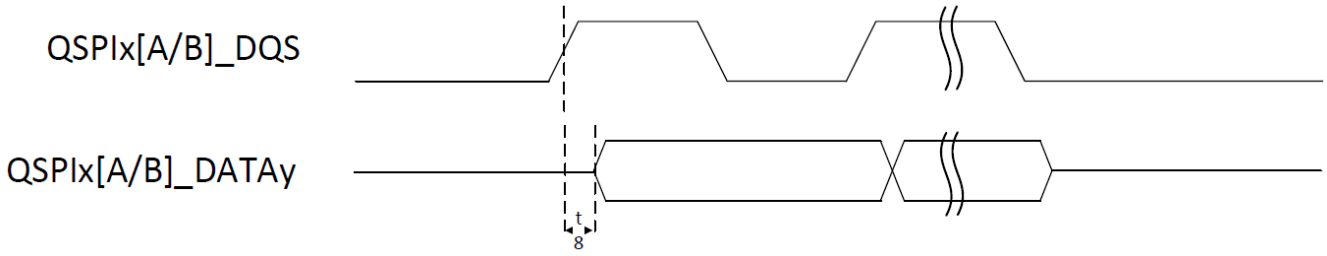


Figure 44. FlexSPI read with DQS timing diagram (SDR mode)

4.10.12.1.2 SDR mode timing parameter tables

Table 96. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 (SDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	60	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	7.5	—	ns
t2	QSPI*x*[A/B]_SS*y*_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SS*y*_B Lead Time[1]	TCSS+0.5	—	SCLK
t4	QSPI*x*[A/B]_SS*y*_B Lag Time[1]	TCSH	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output Delay	—	1	ns
t6	QSPI*x*[A/B]_DATA*y* Setup Time	6	—	ns
t7	QSPI*x*[A/B]_DATA*y* Hold Time	0	—	ns

[1] Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

Table 97. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x1 (SDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	166	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	2.7	—	ns
t2	QSPI*x*[A/B]_SSy_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SSy_B Lead Time[1]	TCSS+0.5	—	SCLK
t4	QSPI*x*[A/B]_SSy_B Lag Time[1]	TCSH	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output Delay	—	1	ns
t6	QSPI*x*[A/B]_DATA*y* Setup Time	1	—	ns
t7	QSPI*x*[A/B]_DATA*y* Hold Time	2	—	ns

1 Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

Table 98. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (SDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_DQS Cycle frequency	—	200	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	2.25	—	ns
t2	QSPI*x*[A/B]_SS*y*_B pulse width[1]	CSINTERVAL	—	SCLK
t3	QSPI*x*[A/B]_SS*y*_B Lead Time[2]	TCSS+0.5	—	SCLK
t4	QSPI*x*[A/B]_SS*y*_B Lag Time[2]	TCSH	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output Delay	—	1	ns
t8	QSPI*x*[A/B]_DQS / QSPI*x*[A/B]_DATA*y* delta	-0.65	0.65	ns

1 Minimum is 2 SCLK cycles even if CSINTERVAL value is less than 2.

2 Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

4.10.12.2 DDR mode

4.10.12.2.1 DDR mode timing diagrams

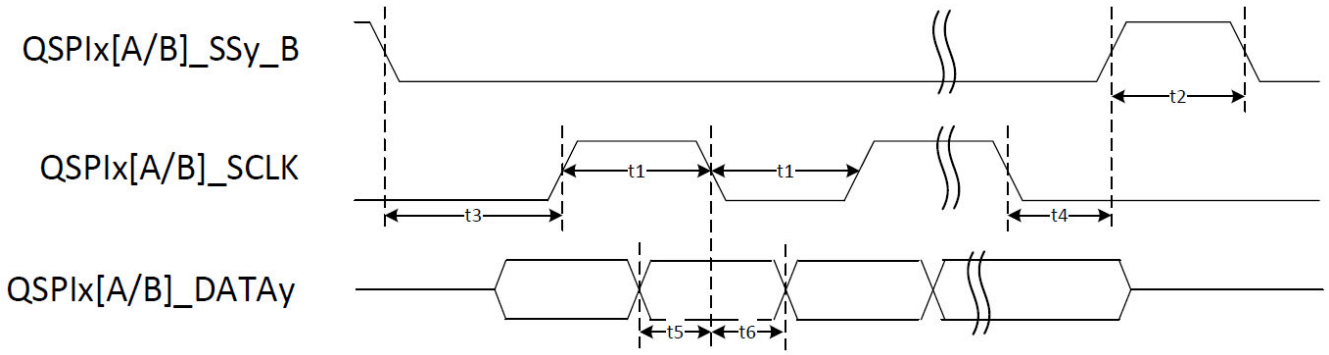


Figure 45. FlexSPI write timing diagram (DDR mode)

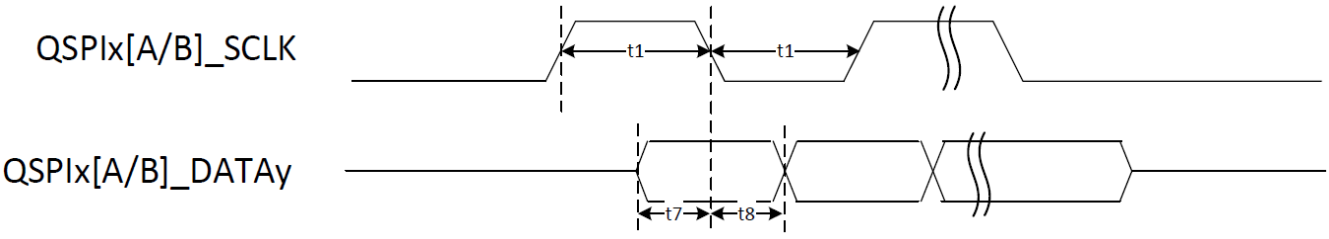


Figure 46. FlexSPI read timing diagram (DDR mode)

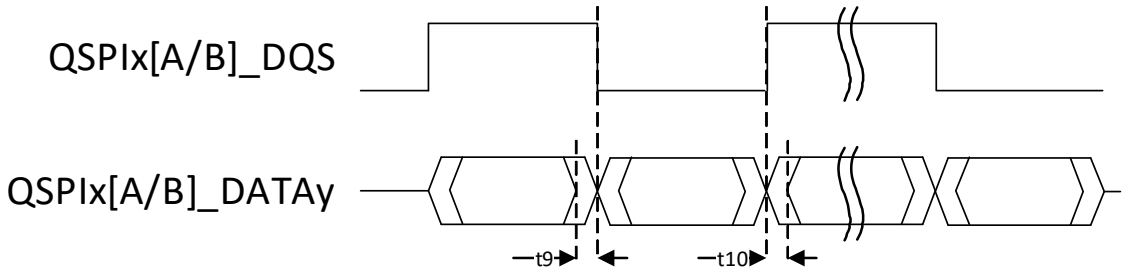


Figure 47. FlexSPI read with DQS timing diagram (DDR mode)

Table 99. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 (DDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	30	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	15	—	ns
t2	QSPI*x*[A/B]_SS*y*_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SS*y*_B Lead Time[1]	(TCSS+0.5)/2	—	SCLK
t4	QSPI*x*[A/B]_SS*y*_B Lag Time[1]	TCSH/2	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output valid time	6.5	—	ns
t6	QSPI*x*[A/B]_DATA*y* output hold time	6.5	—	ns
t7	QSPI*x*[A/B]_DATA*y* Setup Time	6	—	ns
t8	QSPI*x*[A/B]_DATA*y* Hold Time	0	—	ns

1 Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

Table 100. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x1 (DDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	83	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	5.4	—	ns
t2	QSPI*x*[A/B]_SSy_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SSy_B Lead Time[1]	(TCSS+0.5)/2	—	SCLK
t4	QSPI*x*[A/B]_SSy_B Lag Time[1]	TCSH/2	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output valid time	2	—	ns
t6	QSPI*x*[A/B]_DATA*y* output hold time	2	—	ns
t7	QSPI*x*[A/B]_DATA*y* Setup Time	1	—	ns
t8	QSPI*x*[A/B]_DATA*y* Hold Time	1	—	ns

1 Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

Table 101. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (DDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	200	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	2.25	—	ns
t2	QSPI*x*[A/B]_SS*y*_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SS*y*_B Lead Time[1]	(TCSS+0.5)/2	—	SCLK
t4	QSPI*x*[A/B]_SS*y*_B Lag Time[1]	TCSH/2	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output valid time	0.65	—	ns
t6	QSPI*x*[A/B]_DATA*y* output hold time	0.65	—	ns
t9	QSPI*x*[A/B]_DATA*y* Setup Skew	—	0.65	ns
t10	QSPI*x*[A/B]_DATA*y* Hold Skew	—	0.65	ns

1 Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

4.10.13 Secure JTAG controller (SJC)

4.10.13.1 Internal pull-up/pull-down configuration

The following table describes the default configuration of internal pull-ups and pull-downs of the JTAG interface. External pull-ups and pull-downs are needed when this interface is routed to a connector.

Table 102. JTAG default configuration for internal pull-up/pull-down

Ball name	Internal pull setting[1]	Typical pull value	Unit
JTAG_TMS	PU	50	KΩ
JTAG_TCK	PD		
JTAG_TDI	PU		
TEST_MODE_SELECT	PD		

1 PU = pull-up; PD = pull-down

4.10.13.2 JTAG timing parameters

Figure 48 depicts the SJC test clock input timing. Figure 49 depicts the SJC boundary scan timing. Figure 50 depicts the SJC test access port. Signal parameters are listed in Table 103.

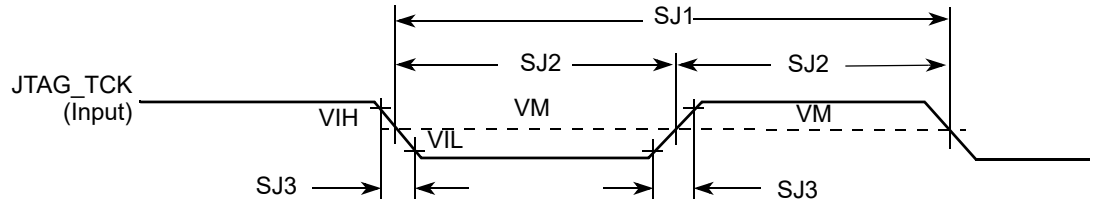


Figure 48. Test Clock Input Timing Diagram

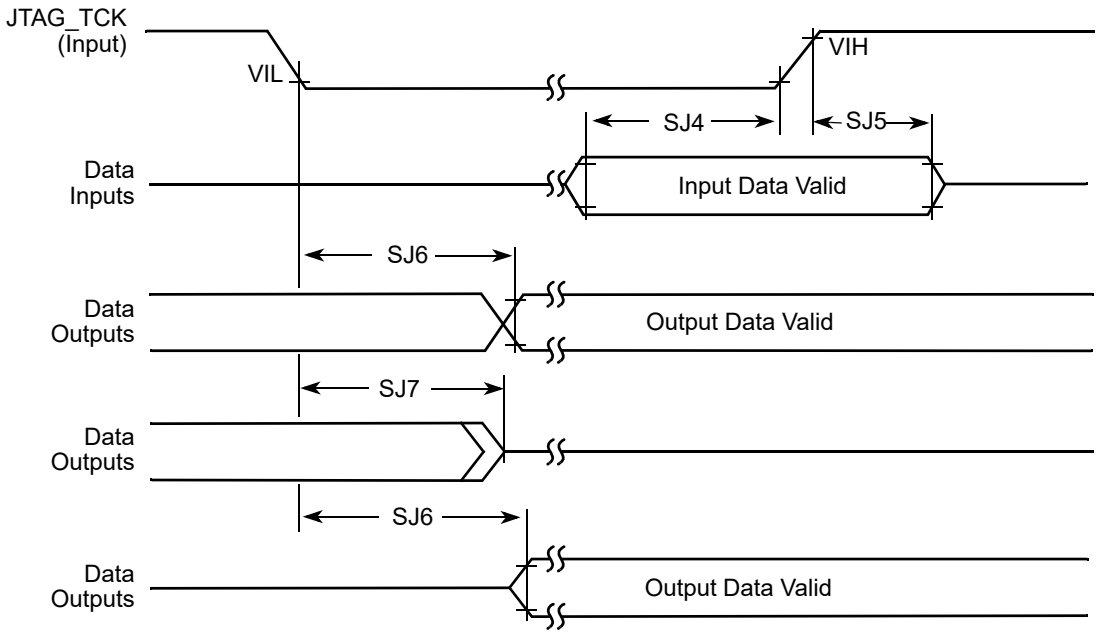


Figure 49. Boundary system (JTAG) timing diagram

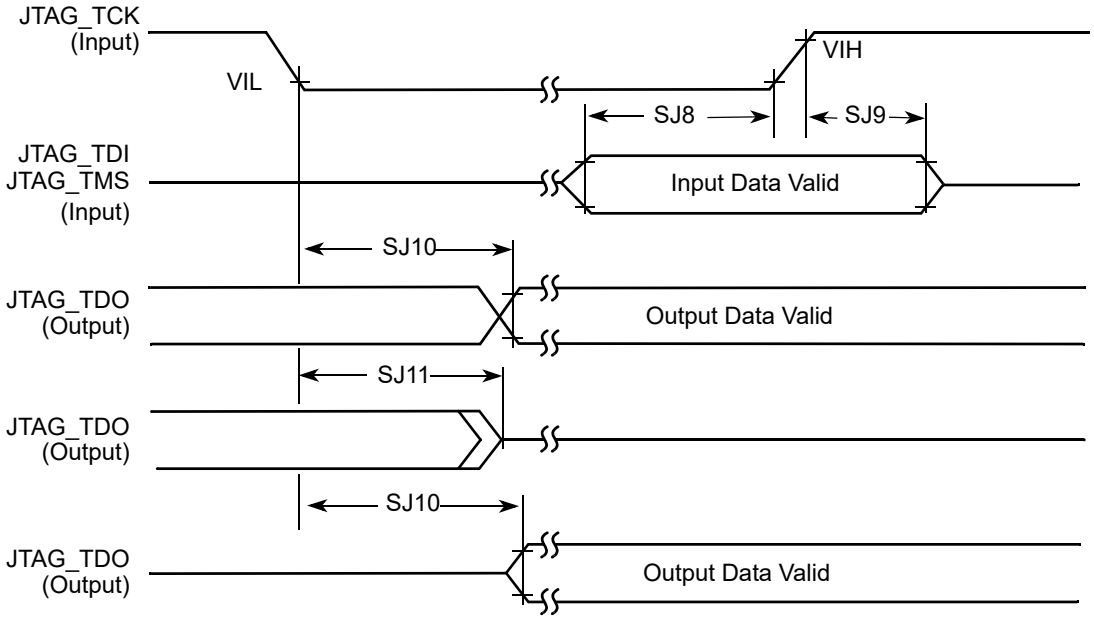


Figure 50. Test Access Port Timing Diagram

Table 103. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3xT_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.10.14 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 104, Figure 51, and Figure 52 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 104. SPDIF Timing Parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

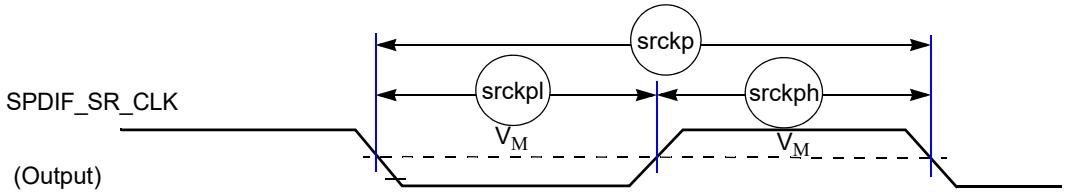


Figure 51. SPDIF_SR_CLK Timing Diagram

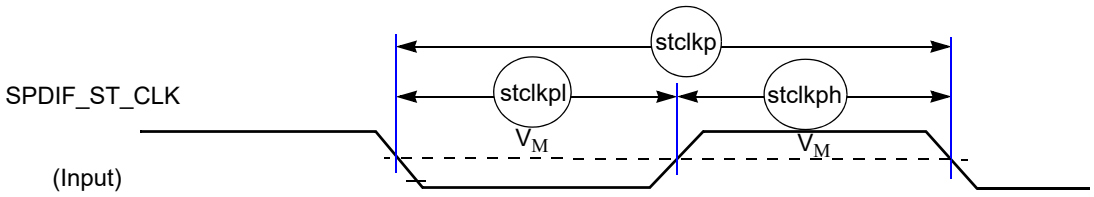


Figure 52. SPDIF_ST_CLK Timing Diagram

4.10.15 UART I/O configuration and timing parameters

4.10.15.0.1 UART Transmitter

The following figure depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 105 lists the UART RS-232 serial mode transmit timing characteristics.

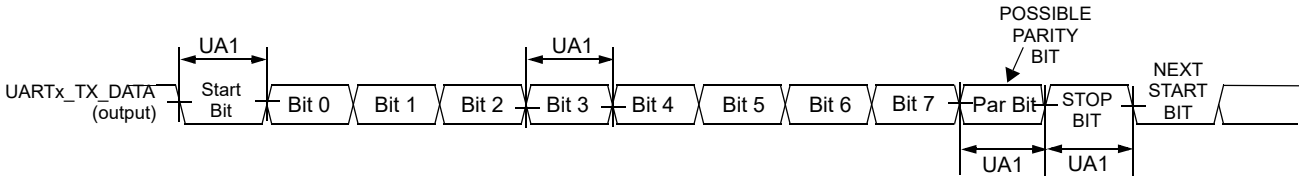


Figure 53. UART RS-232 Serial Mode Transmit Timing Diagram

Table 105. UART RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud_rate} + T_{ref_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).

2 T_{ref_clk}: The period of UART reference clock ref_clk (LPUART_clk after SBR divider).

4.10.15.0.2 UART Receiver

The following figure depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 106 lists serial mode receive timing characteristics.

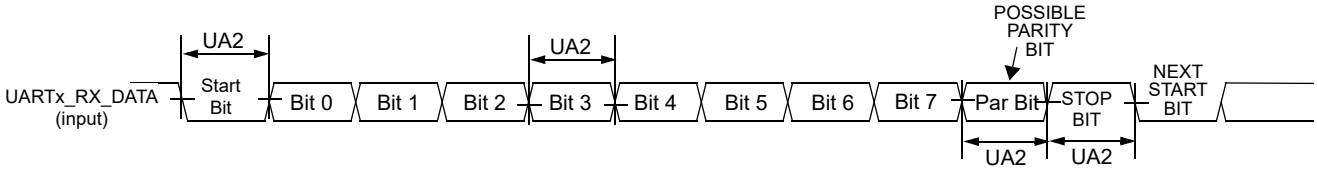


Figure 54. UART RS-232 Serial Mode Receive Timing Diagram

Table 106. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud_rate}$[2] – $1/(16 \times F_{baud_rate})$	$1/F_{baud_rate}$ + $1/(16 \times F_{baud_rate})$	—

1 The UART receiver can tolerate 1/((OSR+1) × Fbaud_rate) tolerance in each bit, but accumulation tolerance in one frame must not exceed 3/((OSR+1) × Fbaud_rate).

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).

4.10.15.0.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

The following figure depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 107 lists the transmit timing characteristics.

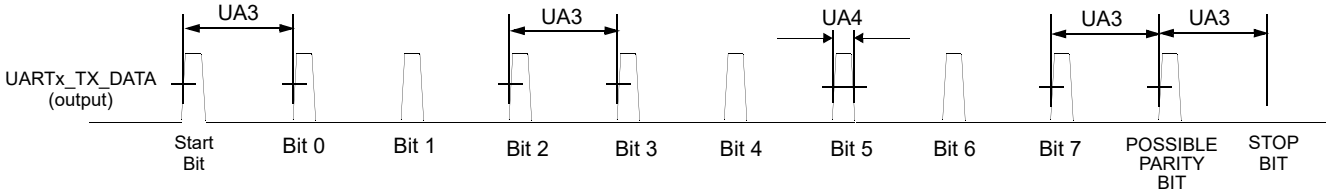


Figure 55. UART IrDA Mode Transmit Timing Diagram

Table 107. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud_rate} + T_{ref_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(TNP+1)/(OSR+1) \times (1/F_{baud_rate}) - T_{ref_clk}$	$(TNP+1)/(OSR+1) \times (1/F_{baud_rate}) + T_{ref_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).

2 T_{ref_clk}: The period of UART reference clock ref_clk (LPUART_clk after SBR divider).

UART IrDA Mode Receiver

The following figure depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 108 lists the receive timing characteristics.

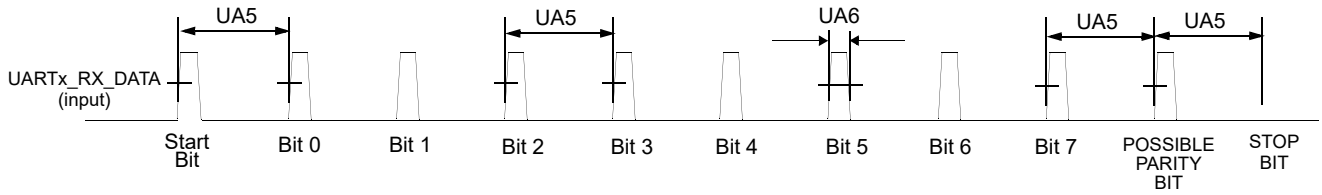


Figure 56. UART IrDA Mode Receive Timing Diagram

Table 108. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud_rate}$ [2] – $1/(16 \times F_{baud_rate})$	$1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud_rate})$	—

1 The UART receiver can tolerate 1/((OSR+1) × Fbaud_rate) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/((OSR+1) × Fbaud_rate).

[2] Fbaud_rate: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).

4.10.16 USB 2.0 PHY Parameters

4.10.16.1 USB 2.0 PHY Transmitter specifications

This section describes the transmitter specifications for USB2.0 PHY.

4.10.16.1.1 USB 2.0 PHY full-speed/low-speed transmitter specifications

The following table lists the full-speed/low-speed (FS/LS) transmitter specifications for USB2.0 PHY.

Table 109. USB 2.0 PHY FS/LS transmitter specifications

Symbol	Description	Min	Typ	Max	Units
VOL	Output Voltage Low	0	—	0.3	V
VOH	Output Voltage High (Driven)	2.8	—	3.6	V
VOSE1	Single Ended One (SE1)	0.8	—	—	V
VCRS	Output Signal Cross Over Voltage	1.3	—	2.0	V
TFR	Driver Rise Time - FS	4	—	20	ns
TLR	Driver Rise Time - LS	75	—	300	ns
TFF	Driver Fall Time - FS	4	—	20	ns
TLF	Driver Fall Time - LS	75	—	300	ns
TFRFM	Differential Rise and Fall Time Matching - FS	90	—	111.11	%
TLRFM	Differential Rise and Fall Time Matching - LS	80	—	125	%
ZHSDRV	Driver Output Resistance (Also serves as HS Termination)	40.5	—	49.5	Ω
TDJ1	Source Jitter (Next Transition) - FS	-3.5	—	3.5	ns
TDJ2	Source Jitter (Paired Transition) - FS	-4	—	4	ns
TFDEOP	Source Jitter (Differential to SE0 transition) - FS	-2	—	5	ns
TFEOPT	Source SE0 interval of EOP - FS	160	—	175	ns
TDDJ1	Source Jitter in downstream direction (Next Transition) - LS	-25	—	25	ns
TDDJ2	Source Jitter in downstream direction (Paired Transition) - LS	-14	—	14	ns
TUDJ1	Source Jitter in upstream direction (Next Transition) - LS	-95	—	95	ns
TUDJ2	Source Jitter in upstream direction (Paired Transition) - LS	-150	—	150	ns
TLDEOP	Source Jitter in upstream direction (Differential to SE0 transition) - LS	-40	—	100	ns
TLEOPT	Source SE0 interval of EOP - LS	1.25	—	1.5	µs

4.10.16.2 USB 2.0 PHY high-speed transmitter specifications

The following table lists the high-speed (HS) transmitter specifications for USB 2.0 PHY.

Table 110. USB 2.0 PHY HS transmitter specifications

Symbol/Parameter	Description	Min	Typ	Max	Units
HSOI	High Speed Idle Level	-10	—	10	mV
VHSTERM	Termination Voltage in High Speed	-10	—	10	mV
VHSOL	High Speed Data Signaling Low	-10	—	10	mV
VCHIRPJ	Chirp J (Differential Voltage)	700	—	1100	mV
VCHIRPK	Chirp K (Differential Voltage)	-900	—	-500	mV
ZHSDRV	Driver Output Resistance	40.5	—	49.5	Ω
THSR	Rise Time (10% to 90%)	100	—	—	ps
THSF	Fall Time (10% to 90%)	100	—	—	ps
HS Eye Opening: Template 1	Differential eye opening at 37.5% US and 62.5% UI for a hub measured at TP2 and for a device without a captive cable measured at TP3.	-300	—	300	mV
HS Eye Opening: Template 2	Differential eye opening at 37.5% US and 62.5% UI for a device with a captive cable measured at TP2.	-175	—	175	mV
HS Jitter: Template 1	Peak-Peak Jitter at Zero crossing for a hub measured at TP2 and for a device without captive cable measured at TP3.	—	—	15	%UI
		—	—	312.5	ps
HS Jitter: Template 2	Peak-Peak Jitter at Zero crossing for a device with captive cable measured at TP2.	—	—	25	%UI
		—	—	520.83	ps

4.10.16.3 USB 2.0 PHY receiver specifications

This section describes the receiver specifications implemented in USB 2.0 PHY.

4.10.16.3.1 USB 2.0 PHY full-speed/low-speed (FS/LS) receiver specifications

Table 111. USB 2.0 PHY FS/LS receiver specifications

Symbol	Description	Min	Typ	Max	Units
VIH	Input Voltage Level - High (Driven)	2	—	—	V
VIHZ	Input Voltage Level - High (Floating)	2.7	—	3.6	V
VIL	Input Voltage Level - Low	—	—	0.8	V
VTH	Switching Threshold	0.8	—	2.0	V
VCM	Common Mode Range	0.8	—	2.5	V
TJR1	Receiver Jitter Budget (Next Transition) - FS	-18.5	—	18.5	ns

Table 111. USB 2.0 PHY FS/LS receiver specifications (continued)

Symbol	Description	Min	Typ	Max	Units
TJR2	Receiver Jitter Budget (Paired Transition) - FS	-9	—	9	ns
TFEOPR	Receiver EOP Interval of EOP - FS	82	—	—	ns
TUJR1	US Port Differential Receiver Jitter (Next Transition) - LS	-152	—	152	ns
TUJR2	US Port Differential Receiver Jitter (Paired Transition) - LS	-200	—	200	ns
TDJR1	DS Port Differential Receiver Jitter (Next Transition) - LS	-75	—	75	ns
TDJR2	DS Port Differential Receiver Jitter (Paired Transition) - LS	-45	—	45	ns
TLEOPR	Receiver EOP Interval of EOP - LS	670	—	—	ns

4.10.16.3.2 USB 2.0 PHY high-speed receiver specifications

The following table lists the high-speed (HS) receiver specifications for USB 2.0 PHY.

Table 112. USB 2.0 PHY HS receiver specifications

Symbol/Parameter	Description	Min	Typ	Max	Units
VHSCM	HS RX input common mode voltage range.	-50	—	500	mV
ZHSDRV	HS RX input termination (Same as Driver output resistance).	40.5	—	49.5	Ω
HSRX Jitter: Template 3	HS RX Peak-Peak Jitter specification at differential zero crossing for a device with captive cable when signal applied at TP2.	—	—	20	%UI
		—	—	416.66	ps
HSRX Jitter: Template 4	HS RX Peak-Peak Jitter specification at differential zero crossing for a device without captive cable at TP3 and for a hub at TP2.	—	—	30	%UI
		—	—	625	ps
HSRX Input Eye Opening: Template 3	HS RX differential sensitivity specification at 40% and 60% UI for a device with captive cable when signal is applied at TP2.	-275	—	275	mV
HSRX Input Eye Opening: Template 4	HS RX differential sensitivity specification at 35% and 65% UI for a device without captive cable when signal is applied at TP3 and for a hub when a signal is applied at TP2.	-150	—	150	mV

4.10.16.3.3 USB 2.0 PHY high-speed envelope detector specifications

The following table lists the high-speed (HS) Envelope Detector Specifications of USB 2.0 PHY.

Table 113. USB 2.0 PHY HS envelope detector specifications

Symbol	Description	Min	Typ	Max	Units
VHSSQ	HS Squelch Detection threshold (differential signal amplitude)	100	—	150	mV
VHSDSC	HS Disconnect Detection threshold (differential signal amplitude)	525	—	625	mV

4.10.16.4 USB 2.0 PHY full-speed/high-speed terminations specification

The following table lists the full-speed/low-speed (FS/LS) Terminations Specification of USB 2.0 PHY.

Table 114. USB 2.0 PHY FS/LS terminations specification

Symbol	Description	Min	Typ	Max	Units
RPU	Bus Pull-Up resistor on US Port in IDLE State	900	—	1575	Ω
	Bus Pull-Up resistor on US Port in ACTIVE State	1425	—	3090	Ω
RPD	Bus Pull-Down resistor on DS Port	14.25	—	24.8	KΩ
VTERM	Termination Voltage for US Port Pull-Up (RPU)	3.0	—	3.6	V

4.10.16.5 Voltage threshold specification

The following table lists the OTG Comparator Specifications of USB2.0 PHY.

Table 115. USB 2.0 PHY OTG comparator specifications

Symbol	Description	Min	Typ	Max	Units
sessvld	B-Device Session Valid threshold	0.8	—	4.0	V
vbusvalid	VBUS Valid threshold	4.4	—	4.75	V

4.10.17 USB 3.0 PHY parameters

The following content is from the USB 3.0 PHY specifications.

4.10.17.1 USB 3.0 PHY external component

Table 116. USB 3.0 PHY external component specifications

Name	Min	Typ	Max	Units	Descriptions
rext	497.5	500	502.5	Ω	There needs to be an external resistor component connected at rext ball while the internal resistor or current is getting calibrated. Package routing from rext ball to its respective bump should not contribute more than 0.05 Ω.

4.10.17.2 USB 3.0 PHY transmitter module

Table 117. USB 3.0 PHY transmitter module electrical specifications

Symbol	Description	Min	Typ	Max	Unit
Voltage/current parameters					
$V_{TX-DIFFp}$	Programmable output voltage swing (single-ended)	50	—	500	mV
$V_{TX-DIFFp-p}$	Programmable differential peak-to-peak output voltage	100	—	1000	mV
$V_{TX-DIFFp-p-LOW}$[1]	Low power differential p-p TX voltage swing	400	—	1200	mV
$I_{TX-SHORT}$	Transmit lane short-circuit current	—	—	100	mA
$RL_{TX-DIFF}$	Transmitter differential return loss	—	—	0 < -20dB < 100Mhz 100Mhz < -18dB < 300Mhz 300Mhz < -16dB < 600Mhz 600Mhz < -10dB < 2500Mhz 2500Mhz < -9dB < 4875Mhz 4875Mhz < -8dB < 11200Mhz 11200Mhz < -5dB < 16800Mhz and -3dB beyond that	Db
RL_{TX-CM}	Transmitter common mode return loss	—	—	50Hz < -8dB < 15000Mhz	dB
$Z_{TX-DIFF-DC}$	DC differential TX impedance	80	100	120	Ω
UI	Unit Interval	199.94	—	200.06	ps
$T_{TX-MAX-JITTER}$	Transmitter total jitter (peak-to-peak) (T_j)	—	—	0.4	UI
$T_{TX-RJ-PLL-sigma}$	After application of TX jitter transfer function	—	—	2.42	ps
LTLAT-10	Transmitter data latency	—	—	210	UI
Voltage parameters					
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle.	0	—	100	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Peak Output Voltage	0	—	20	mV
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	—	25	mV
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	0	—	600	mV
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an EIOS	—	—	8	ns

Table 117. USB 3.0 PHY transmitter module electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid diff signaling after leaving Electrical Idle	—	—	8	ns
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage (5.0 GT/s)	20	—	150	mVpp
T_{EIExit}	Time to exit Electrical Idle (L0s) state and to enter L0	—	—	5	Txsysclk
Tx signal characteristics					
f_{tol}	TX Frequency Long Term Accuracy	-300	—	300	ppm of Fbaud
f_{SSC}	Spread-Spectrum Modulation Frequency	30	—	33	kHz
$t_{20-80TX}$	TX Rise/Fall Time	0.2	—	0.41	UI
t_{skewTX}	TX Differential Skew	—	—	20	ps

[1] For USB 3.0, no EQ is required

4.10.17.3 USB 3.0 PHY receiver module

Table 118. USB 3.0 PHY receiver module electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Comments
Voltage Parameters						
$V_{RX-DIFF(p-p)}$	Differential input voltage (peak-to-peak) (that is, receiver eye voltage opening)	100	—	1200	mV	—
$V_{RX-IDLE-DET-DIFF(p-p)}$	Differential input threshold voltage (peak-to-peak) to detect idle (LFPS)	100	—	300	mV	USB3 LFPS
$V_{cm, acRX}$	RX AC Common Mode Voltage	—	—	100	mVp-p	Simulated at 250 MHz
$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling	—	0	150	mV	—
$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	W	100 Ω ± 10%
$RL_{RX-DIFF}$	Receiver differential return loss	Same as TX RL	—	—	dB	—
Jitter Parameters						
$T_{RX-MAX-JITTER}$	Receiver total jitter tolerance	0	—	0.66	UI	Incoming Jitter: USB3 = 0.43UI DJ + 0.23UI RJ USB3 numbers are with REFC-TLE

Table 119. PLL module electrical specifications

Parameter	Symbol	Description	Min	Typ	Max	Units
Input Reference Clock						
REF CLK Frequency	REF CLK	—	19.2	19.2/24/25/26/38.4	38.4	MHz
REF CLK Duty Cycle	—	—	47	—	53	MHz
REF CLK Frequency	REF CLK	—	40	40/48/50/52/100	100	MHz
REF CLK RJ Tolerance	—	Integrated jitter from 10 kHz to 16 MHz after applying appropriate PLL ref clock transfer function and the protocol JTF	—	—	0.5	ps
REF CLK Duty Cycle	—	—	37	—	63	%
Divided Reference Frequency	—	—	19.2	—	38.4	MHz
Dividers						
Input division	IPDIV<7:0>	—	1	—	255	Counts
Feedback division	pll_fbdiv_high<9:0>	—	2	—	1025	Counts
	pll_fbdiv_low<9:0>	—	2	—	1025	Counts
Feedback fractional division range	—	—	>-2	—	<2	Counts
Number of fractional bits	—	This includes one bit for sign	—	27	—	Bits
VCO						
Clock frequency	—	Output full rate clocks	—	5000	—	MHz
VCO frequency	—	VCO oscillation frequency	—	5000	—	MHz
Output clock frequency tolerance	—	This includes SSC deviation	-5300	—	300	ppm
SSC modulation rate	—	As applicable for USB3.0	30	—	33	kHz
Output clock RJ sigma for TX	—	After application of TX jitter transfer function	—	—	2.42	ps
Output clock RJ sigma for RX	—	After application of RX jitter transfer function	—	—	1.40	ps

4.11 Analog-to-digital converter (ADC)

The following table shows the ADC electrical specifications for VREFH=VDD_ADC_1P8.

Table 120. ADC electrical specifications (VREFH=VDD_ADC_1P8)

Symbol	Description	Min	Typ[1]	Max	Unit	Notes
V_{ADIN}	Input Voltage	VREFL	—	VREFH	V	—
C_{ADIN}	Input capacitance	—	4.5	—	pF	—
R_{ADIN}	Input Resistance	—	500	—	Ω	—
R_{AS}	Analog Source Resistance	—	—	5	kΩ	2
f_{ADCK}	ADC Conversion Clock Frequency	—	24	—	MHz	—
C_{sample}	Sample cycles	3.5	—	131.5	—	3
$C_{compare}$	Fixed compare cycles	—	17.5	—	cycles	—
$C_{conversion}$	Conversion cycles	$C_{conversion} = C_{sample} + C_{compare}$			cycles	—
DNL	Differential Non-Linearity	—	± 0.6	-0.5 to +1.1	LSB	4
INL	Integral Non-Linearity	—	± 0.9	±1.1	LSB	4
ENOB	Effective Number of Bits	—	—	—	—	5,6,7
	Avg = 1	10.1	10.4	—	Bits	
	Avg = 2	10.5	10.7	—	Bits	
	Avg = 16	11.1	11.3	—	Bits	
SINAD	Signal to Noise plus Distortion	SINAD=6.02 x ENOB + 1.76			dB	—
E_G	Gain error	—	-0.29	—	%FSV	8
E_O	Offset error	—	0.01	—	%FSV	9
I_{VDDA18}	Supply Current	—	480	—	µA	10
$I_{in,ext,leak}$	External Channel Leakage Current	—	30	500	nA	—
E_{IL}	Input leakage error	RAS * I_{in}			mV	—

1 Typical values assume VDD_ADC_1P8 = 1.8 V, Temp = 25 °C, fACLK = Max, unless otherwise stated. Typical values are for reference only. All values, including Min and Max, are derived from lab characterization and are not tested in production.

2 This resistance is external to the input pad. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance. The RAS/CAS (analog source capacitance) time constant should be kept to < 1 ns.

3 See Figure 57.

4 ADC conversion clock at max frequency and using linear histogram.

5 Input data used for test was 1 kHz sine wave.

6 Measured at VREFH = 1.8 V and pwrsel = 2.

7 ENOB can be lower than shown, if an ADC channel corrupts other ADC channels through capacitive coupling. This coupling may be dominated by board parasitics. Care must be taken not to corrupt the desired channel being measured. This coupling becomes worse at higher analog frequencies and with switching waveforms due to the harmonic content.

8 Error measured at fullscale at 1.8 V.

9 Error measured at zero scale at 0 V.

[10] Power Configuration Select, PWRSEL, is set to 10 binary.

The following table shows the ADC electrical specifications for 1V≤VREFH<VDD_ADC_1P8.

Table 121. ADC electrical specifications (1V≤VREFH<VDD_ADC_1P8)

Symbol	Description	Min	Typ[1]	Max	Unit	Notes
V_{ADIN}	Input Voltage	VREFL	—	VREFH	V	—
C_{ADIN}	Input capacitance	—	4.5	—	pF	—
R_{ADIN}	Input Resistance	—	500	—	Ω	—
R_{AS}	Analog Source Resistance	—	—	5	kΩ	2
f_{ADCK}	ADC Conversion Clock Frequency	—	24	—	MHz	—
C_{sample}	Sample cycles	3.5	—	131.5	—	3
$C_{compare}$	Fixed compare cycles	—	17.5	—	cycles	—
$C_{conversion}$	Conversion cycles	$C_{conversion} = C_{sample} + C_{compare}$			cycles	—
DNL	Differential Non-Linearity	—	± 0.6	-0.5 to +1.1	LSB	4
INL	Integral Non-Linearity	—	± 0.9	±1.1	LSB	4
ENOB	Effective Number of Bits	—	—	—	—	5,6,7
	Avg = 1	9.5	9.7	—	Bits	
	Avg = 2	9.9	10.1	—	Bits	
	Avg = 16	10.8	11	—	Bits	
SINAD	Signal to Noise plus Distortion	SINAD=6.02 x ENOB + 1.76			dB	—
E_G	Gain error	—	0.29	—	%FSV	8
E_O	Offset error	—	0.01	—	%FSV	9
I_{VDDA18}	Supply Current	—	480	—	μA	10
$I_{in,ext,leak}$	External Channel Leakage Current	—	30	500	nA	—
E_{IL}	Input leakage error	RAS * I_{in}			mV	—

1 Typical values assume VDD_ANA_1P8 = 1.8 V, Temp = 25 °C, fACLK = Max, unless otherwise stated. Typical values are for reference only. All values, including Min and Max, are derived from lab characterization and are not tested in production.

2 This resistance is external to the input pad. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance. The RAS/CAS (analog source capacitance) time constant should be kept to < 1 ns.

3 See Figure 57.

4 ADC conversion clock at max frequency and using linear histogram.

5 Input data used for test was 1 kHz sine wave.

6 Measured at VREFH = 1 V and pwrsel = 2.

7 ENOB can be lower than shown, if an ADC channel corrupts other ADC channels through capacitive coupling. This coupling may be dominated by board parasitics. Care must be taken not to corrupt the desired channel being measured. This coupling becomes worse at higher analog frequencies and with switching waveforms due to the harmonic content.

8 Error measured at fullscale at 1.0 V.

[9] Error measured at zero scale at 0 V.
[10] Power Configuration Select, PWRSEL, is set to 10 binary.

The following figure shows a plot of the ADC sample time versus R_{AS}.

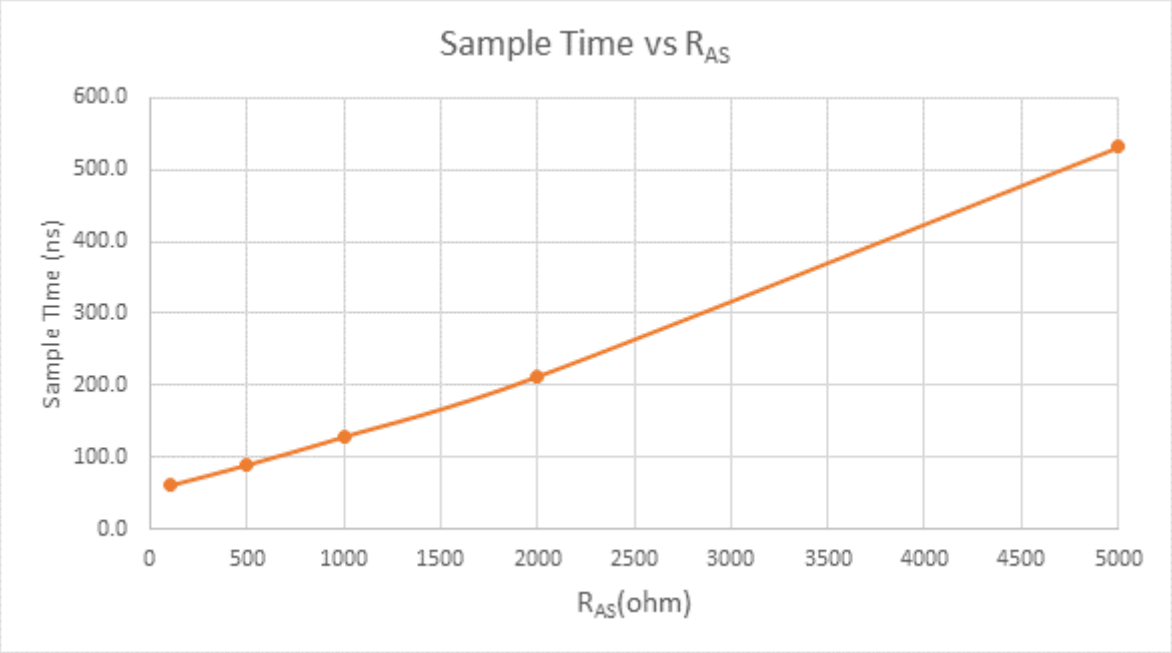


Figure 57. Sample time vs. R_{AS}

5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot mode configuration pins

The following table provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of FORCE_BOOT_FROM_FUSE. After it is blown, the Boot mode pin is ignored by ROM; ROM receives 'boot mode' from the BT_MODE_FUSES fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is ‘0’ (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the Boot mode pins, see the “System Boot, Fusemap, and eFuse” chapter of the device reference manual for more details.

Table 122. Fuse and associated pins used for Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
BOOT_MODE[0]	Input	SCU_BOOT_MODE0	Boot mode selection
BOOT_MODE[1]	Input	SCU_BOOT_MODE1	
BOOT_MODE[2]	Input	SCU_BOOT_MODE2	
BOOT_MODE[3]	Input	SCU_BOOT_MODE3	

5.2 Boot devices interfaces allocation

The following table lists the interfaces that can be used by the boot process in accordance with the specific Boot mode configuration. The table also describes the interface’s specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 123. Interface allocation during boot

Interface	IP Instance	Allocated Pads During Boot	Comment
eMMC	USDHC0	EMMC0_CLK, EMMC0_CMD, EMMC0_DATA0, EMMC0_DATA1, EMMC0_DATA2, EMMC0_DATA3, EMMC0_DATA4, EMMC0_DATA5, EMMC0_DATA6, EMMC0_DATA7, EMMC0_RESET_B	
SD	USDHC1	USDHC1_CD_B, USDHC1_CLK, USDHC1_CMD, USDHC1_DATA0, USDHC1_DATA1, USDHC1_DATA2, USDHC1_DATA3, USDHC1_RESET_B, USDHC1_VSELECT	USDHC1_CD_B is used by first (A0) silicon only. Second (B0) silicon uses USDHC1_DATA3 for CD (Card Detect).

Table 123. Interface allocation during boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
NAND	GPMI	EMMC0_CLK, EMMC0_CMD, EMMC0_DATA0, EMMC0_DATA1, EMMC0_DATA2, EMMC0_DATA3, EMMC0_DATA4, EMMC0_DATA5, EMMC0_DATA6, EMMC0_DATA7, EMMC0_STROBE, EMMC0_RESET_B, USDHC1_CD_B, USDHC1_CMD, USDHC1_DATA0, USDHC1_DATA1, USDHC1_DATA2, USDHC1_DATA3, USDHC1_RESET_B, USDHC1_VSELECT, USDHC1_WP	8 bit boot from CS0 only, but will drive CS1 to high when booting if specified in fuse. Single-ended DQS: • USDHC1_CD_B Single-ended RE: • USDHC1_VSELECT Differential DQS: • _N use USDHC1_WP • _P use USDHC1_CD_B Differential RE: • _N use USDHC1_RESET_B • _P use USDHC1_VSELECT
Quad SPI	QSPI0	QSPI0A_DATA0, QSPI0A_DATA1, QSPI0A_DATA2, QSPI0A_DATA3, QSPI0A_DQS, QSPI0A_SCLK, QSPI0A_SS0_B, QSPI0A_SS1_B, QSPI0B_DATA0, QSPI0B_DATA1, QSPI0B_DATA2, QSPI0B_DATA3, QSPI0B_DQS, QSPI0B_SCLK, QSPI0B_SS0_B, QSPI0B_SS1_B	4, dual-4, or 8 bit
USB	USB-OTG1	USB_OTG1_DN, USB_OTG2_DN, USB_OTG1_DP, USB_OTG2_DP, USB_OTG1_ID, USB_OTG2_ID, USB_OTG1_VBUS, USB_OTG2_VBUS	

6 Package information and contact assignments

This section contains package information and contact assignments for the following package(s):

- FCPBGA, 21 x 21 mm, 0.8 mm pitch
- FCPBGA, 17 x 17 mm, 0.8 mm pitch

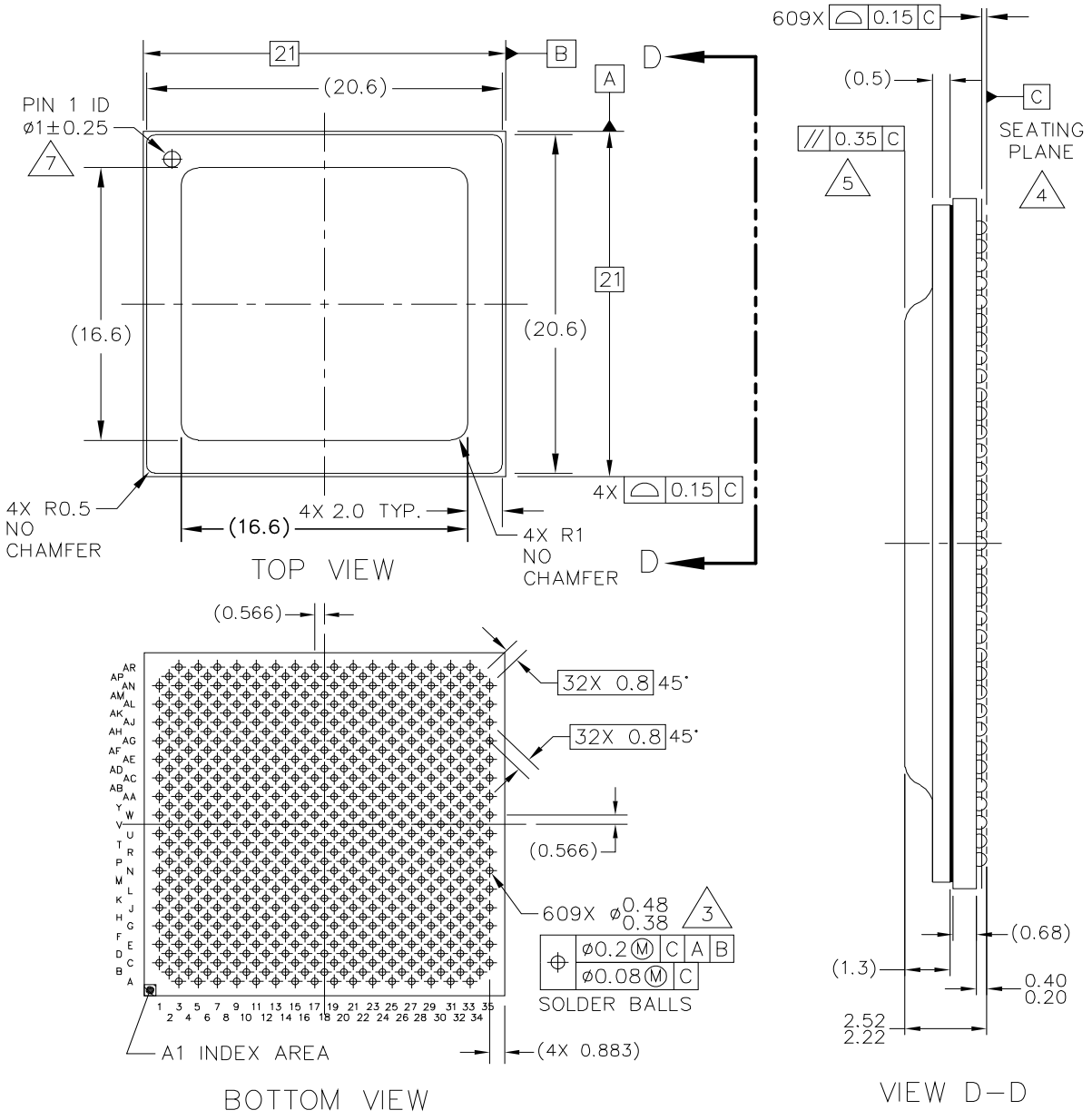
6.1 FCPBGA, 21 x 21 mm, 0.8 mm pitch

This section includes the following information for the 21 x 21 mm, 0.8 mm pitch package:

- Mechanical package drawing
- Ball map
- Contact assignments

6.1.1 21 x 21 mm package case outline

The following figure shows the top, bottom, and side views of the 21 x 21 mm package.



RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES.
MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

TITLE: FCPBGA, WITH LID, 21 X 21 X 2.37 PKG, 0.8 MM PITCH, 609 I/O INTERSTITIAL	DOCUMENT NO: 98ASA01051D REV: C
	STANDARD: NON–JEDEC
	SOT1916–1 SHEET: 1 OF 3

Figure 58. 21 x 21 mm Package Top, Bottom, and Side Views

The following notes pertain to the preceding figure, “21 x 21 mm Package Top, Bottom, and Side Views.”

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
4. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
7. PIN 1 THRU HOLE SHALL BE CENTERED WITHIN FOOT AREA.
8. LID OVERHANG ON SUBSTRATE NOT ALLOWED.

Figure 59. Notes on 21 x 21 mm Package Top, Bottom, and Side Views

6.1.2 21 x 21 mm, 0.8 mm pitch ball map

The following page shows the 21 x 21 mm, 0.8 mm pitch ball map.

Package information and functional contact assignments for FCPBGA, 21 x 21 mm, 0.8 mm pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
A			VSS_MAIN		DDR_DQ31		DDR_DQ28		PCIE0_TX0_N		PCIE_CTRL0_WAKE_B		PCIE0_RX0_P		USB_SS3_TX_N		VSS_MAIN		USB_SS3_RX_P		EMMC0_DATA1		EMMC0_DATA6		USDHC1_VSELECT		USDHC1_DATA0		ENET0_RGMII_TX_CTL		ENET0_RGMII_RXD0		VSS_MAIN		
B		DDR_DQ30		DDR_DQ29		DDR_DQ16		VSS_MAIN		PCIE0_TX0_P		PCIE0_RX0_N		VSS_MAIN		USB_SS3_TX_P		USB_SS3_RX_N		VSS_MAIN		EMMC0_DATA4		USDHC1_RESET_B		USDHC1_DATA1		ENET0_RGMII_TXD1		ENET0_RGMII_RX_CTL		ENET0_MDIO		ESAI0_TX1	
C	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		USB_SS3_TC3		VSS_MAIN		VSS_MAIN		EMMC0_DATA0		VSS_MAIN		USDHC1_CMD		VSS_MAIN		ENET0_RGMII_RXD1		VSS_MAIN		ESAI0_TX3_RX2		VSS_MAIN
D		DDR_DQS3_P		DDR_DM2		DDR_DQS2_P		DDR_DQ19		PCIE_CTRL0_CLKREQ_B		PCIE_REFCLK100M_N		USB_OTG2_REXT		USB_OTG2_DN		USB_OTG1_DP		EMMC0_CMD		EMMC0_DATA7		USDHC1_WP		USDHC1_DATA2		ENET0_RGMII_RXC		ENET0_MDC		ESAI0_TX0		SPDIF0_TX	
E	DDR_DM3		DDR_DQS3_N		DDR_DQS2_N		DDR_DQ18		DDR_DQ17		PCIE_REFCLK100M_P		USB_SS3_REXT		VSS_MAIN		USB_OTG2_DP		USB_OTG1_DN		EMMC0_DATA2		USDHC1_CD_B		USDHC1_DATA3		ENET0_RGMII_TXD2		VSS_MAIN		ESAI0_SCKT		VSS_MAIN		SPDIF0_EXT_CLK
F		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		PCIE_REF_QR		USB_SS3_TC0		USB_OTG2_ID		VSS_MAIN		VSS_MAIN		EMMC0_STROBE		VSS_MAIN		ENET0_RGMII_TXD3		ENET0_REFCLK_125M_25M		ESAI0_FSR		ESAI0_TX4_RX1		SPI3_SDO	
G	DDR_DQ27		DDR_DQ26		DDR_DQ23		DDR_DQ20		DDR_ZQ		PCIE0_PHY_PLL_REF_RETURN		VDD_PCIE_1P8		USB_SS3_TC2		USB_OTG1_ID		EMMC0_CLK		EMMC0_DATA5		USDHC1_CLK		ENET0_RGMII_TXD0		ENET0_RGMII_RXD2		ESAI0_FST		SPDIF0_RX		SPI3_SDI		MCLK_IN0
H		DDR_DQ24		DDR_DQ25		DDR_DQ22		DDR_DQ21		PCIE_CTRL0_PERST_B		PCIE_REXT		USB_SS3_TC1		USB_OTG2_VBUS		USB_OTG1_VBUS		EMMC0_DATA3		EMMC0_RESET_B		ENET0_RGMII_TXC		ENET0_RGMII_RXD3		ESAI0_SCKR		VSS_MAIN		SPI3_SCK		UART1_TX	
J	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		ESAI0_TX5_RX0		SPI3_CS0		VSS_MAIN		SAI0_TXC
K		DDR_DCF29		DDR_DCF27		DDR_DCF28		DDR_DCF25		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		ESAI0_TX2_RX3		SPI3_CS1		UART1_CTS_B		SAI0_TXD	
L	DDR_DCF18		DDR_DCF32		DDR_DCF31		DDR_DCF26		VSS_MAIN		VDD_PCIE_DIG_1P8_3P3		VDD_PCIE_LDO_1P0_CAP		VDD_USB_3P3		VDD_USB_OTG_1P0		VDD_EMMC0_1P8_3P3		VDD_USDHC1_VSELECT_1P8_3P3		VDD_ENET0_VSELECT_1P8_2P5_3P3		VDD_ENET_MDIO_1P8_3P3		VSS_MAIN		MCLK_OUT0		UART1_RX		SAI0_TXFS		SAI1_RXC	
M		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_DDR_VDDQ		VDD_AN A0_1P8		VDD_USB_SS3_LDO_1P0_CAP		VDD_USB_1P8		VDD_EMMC0_VSELECT_1P8_3P3		VDD_USDHC1_1P8_3P3		VDD_ENET0_1P8_2P5_3P3		VSS_MAIN		MCLK_IN1		VSS_MAIN		SAI1_RXD		SAI0_RXD	
N	DDR_DCF19		DDR_DCF17		DDR_CK1_N		DDR_DCF30		VDD_DDR_VDDQ		VDD_DDR_VDDQ		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VDD_ESAI_SPDIF_1P8_2P5_3P3		VSS_MAIN		UART1_RTS_B		SPI2_SDI		VSS_MAIN		SAI1_RXFS
P		DDR_DCF22		DDR_DCF20		DDR_CK1_P		DDR_DCF33		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VDD_GPU		VDD_MAIN		VSS_MAIN		SPI2_CS0		SPI0_SCK		SPI2_SDO		SPI0_SDI	
R	VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_DDR_VDDQ		VSS_MAIN		VDD_DDR_VDDQ		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VSS_MAIN		VDD_SPI_MCLK_UART_1P8_3P3		VSS_MAIN		SPI2_SCK		SPI0_SDO		SPI0_CS0		SPI0_CS1
T		DDR_DCF07		DDR_DCF23		DDR_DCF24		DDR_DCF21		VSS_MAIN		VDD_DDR_VDDQ		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN	
U	DDR_DCF03		DDR_DCF01		DDR_DCF05		DDR_DCF04		VSS_MAIN		VDD_DDR_VDDQ		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VDD_SPI_SAI_1P8_3P3		VSS_MAIN		ADC_VREFH		ADC_VREFL		ADC_IN1		ADC_IN0	
V		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_ADC_1P8		ADC_IN3		ADC_IN2		ADC_IN5	
W	DDR_DCF00		DDR_DCF11		DDR_CK0_P		DDR_DCF16		VSS_MAIN		VDD_DDR_VDDQ		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VSS_MAIN		VSS_MAIN		VDD_ADC_DIG_1P8		VSS_MAIN		ADC_IN4		VSS_MAIN		VSS_MAIN		VSS_MAIN
Y		DDR_DCF14		DDR_DCF15		DDR_CK0_N		DDR_DCF12		VSS_MAIN		VDD_DDR_VDDQ		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VDD_CAN_UART_1P8_3P3		VSS_MAIN		VSS_MAIN		VSS_MAIN		FLEXCAN0_TX		FLEXCAN0_RX	
AA	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_DDR_VDDQ		VDD_DDR_VDDQ		VSS_MAIN		VDD_A35		VDD_A35		VDD_A35		VSS_MAIN		VDD_MAIN		VDD_MIPI_DSI_DIG_1P8_3P3		VSS_MAIN		UART0_TX		FLEXCAN2_TX		FLEXCAN1_RX		FLEXCAN1_TX	
AB		DDR_DQ14		DDR_DCF08		DDR_DCF09		DDR_ATO		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_A35		VDD_A35		VDD_A35		VSS_MAIN		VDD_ANA1_1P8		VSS_MAIN		MIPI_DSI0_I2C0_SDA		VSS_MAIN		UART0_RX		FLEXCAN2_RX	
AC	DDR_DQ15		DDR_DQ12		DDR_DCF10		DDR_DTO0		VDD_DDR_PLL_1P8		VDD_DDR_VDDQ		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_SNVS_4P2		VSS_MAIN		MIPI_DSI1_I2C0_SDA		MIPI_DSI0_I2C0_SCL		VSS_MAIN		UART2_TX	
AD		VSS_MAIN		VSS_MAIN		VSS_MAIN		DDR_VREF		VSS_MAIN		VDD_DDR_VDDQ		VDD_MAIN		VDD_MIPI_1P8		VDD_MIPI_1P0		VSS_MAIN		VDD_MAIN		VDD_TMPR_CSI_1P8_3P3		VSS_MAIN		SCU_WDOG_OUT		MIPI_DSI1_GPIO0_00		MIPI_DSI0_GPIO0_00		UART2_RX	
AE	DDR_DQS1_N		DDR_DQ13		DDR_DQ01		DDR_DTO1		VSS_MAIN		VDD_DDR_VDDQ		VDD_QSPI0B_1P8_3P3		VDD_QSPI0A_1P8_3P3		VDD_MIPI_1P8		VDD_MIPI_1P0		VDD_MIPI_CSI_DIG_1P8		VDD_CSI_1P8_3P3		VDD_SNVS_LDO_1P8_CAP		VSS_MAIN		TEST_MODE_SELECT		JTAG_TCK		MIPI_DSI1_I2C0_SCL		MIPI_DSI0_GPIO0_01	
AF		DDR_DQS1_P		DDR_DM1		DDR_DQ00		DDR_DQ03		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		SCU_GPIO0_00		VSS_MAIN		JTAG_TDO		MIPI_DSI1_GPIO0_01	
AG	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		SCU_PMIC_STANDBY		POR_B		VSS_MAIN		JTAG_TMS	
AH		DDR_DQ10		DDR_DQ11		DDR_DQS0_N		DDR_DQ02		QSPI0B_SS0_B		QSPI0A_DATA3		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		ON_OFF_BUTTON		SCU_GPIO0_01		PMIC_I2C_SDA		JTAG_TDI	
AJ	DDR_DQ08		DDR_DQ09		DDR_DQS0_P		DDR_DM0		QSPI0B_SS1_B		QSPI0B_DATA2		QSPI0A_DATA2		MIPI_DSI0_DATA3_N		MIPI_DSI0_DATA1_N		MIPI_DSI0_CLK_N		MIPI_DSI0_DATA0_N		MIPI_DSI0_DATA2_N		CSI_D06		CSI_D03		SCU_BOOT_MODE3		SCU_BOOT_MODE0		PMIC_INT_B		PMIC_I2C_SCL	
AK		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		QSPI0B_DQS		QSPI0A_SS1_B		QSPI0A_DATA0		MIPI_DSI0_DATA3_P		MIPI_DSI0_DATA1_P		MIPI_DSI0_CLK_P		MIPI_DSI0_DATA0_P		MIPI_DSI0_DATA2_P		CSI_PCLK		CSI_D00		VSS_MAIN		SCU_BOOT_MODE1		ANA_TEST_OUT_N	
AL	DDR_DQ32		DDR_DQ34		DDR_DQ06		DDR_DQ07		QSPI0B_DATA1		QSPI0A_DQS		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		CSI_VSYNC		CSI_D01		SCU_BOOT_MODE2		VSS_MAIN		ANA_TEST_OUT_P	
AM		DDR_DQ33		DDR_DQ04		DDR_DQ05		QSPI0B_DATA3		QSPI0B_DATA0		QSPI0A_SS0_B		MIPI_DSI1_DATA2_N		MIPI_DSI1_CLK_N		MIPI_DSI1_DATA3_N		MIPI_CSI0_DATA1_N		MIPI_CSI0_DATA0_N		MIPI_CSI0_I2C0_SDA		CSI_MCLK		CSI_D07		CSI_D05		RTC_XTALO		XTALO	
AN	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		MIPI_DSI1_DATA0_N		MIPI_DSI1_DATA1_N		MIPI_CSI0_DATA3_N		MIPI_CSI0_CLK_N		MIPI_CSI0_DATA2_N		MIPI_CSI0_MCLK_OUT		VSS_MAIN		CSI_D04		VSS_MAIN		VSS_SCU_XTAL		VSS_SCU_XTAL
AP		DDR_DQ35		DDR_DQS4_P		DDR_DM4		DDR_DQ36		DDR_DQ37		QSPI0A_SCLK		MIPI_DSI1_DATA2_P		MIPI_DSI1_CLK_P		MIPI_DSI1_DATA3_P		MIPI_CSI0_DATA1_P		MIPI_CSI0_DATA0_P		MIPI_CSI0_GPIO0_01		MIPI_CSI0_I2C0_SCL		CSI_EN		CSI_D02		RTC_XTALI		XTALI	
AR			VSS_MAIN		DDR_DQS4_N		DDR_DQ39		DDR_DQ38		QSPI0B_SCLK		QSPI0A_DATA1		MIPI_DSI1_DATA0_P		MIPI_DSI1_DATA1_P		MIPI_CSI0_DATA3_P		MIPI_CSI0_CLK_P		MIPI_CSI0_DATA2_P		MIPI_CSI0_GPIO0_00		CSI_RESET		CSI_HSYNC		PMIC_ON_REQ		VSS_SCU_XTAL			

6.1.3 21 x 21 mm power supplies and functional contact assignments

The following table shows the power supplies contact assignments for the 21 × 21 mm package

Table 124. 21 x 21 mm power supplies contact assignments

Power rail	Ball reference
VDD_A35[1]	AA15,AA17,AA19,AB16,AB18,AB20
VDD_ADC_1P8	V28
VDD_ADC_DIG_1P8	W25
VDD_ANA0_1P8	M14
VDD_ANA1_1P8	AB24
VDD_CAN_UART_1P8_3P3	Y24
VDD_CSI_1P8_3P3	AE23
VDD_DDR_PLL_1P8	AC9
VDD_DDR_VDDQ	AA11,AA9,M12,N9,N11,R7,R11,T12,U11,W11,Y12,AC11,AD12,AE11
VDD_EMMC0_1P8_3P3	L19
VDD_EMMC0_VSELECT_1P8_3P3	M20
VDD_ENET_MDIO_1P8_3P3	L25
VDD_ENET0_1P8_2P5_3P3	M24
VDD_ENET0_VSELECT_1P8_2P5_3P3	L23
VDD_ESAI_SPDIF_1P8_2P5_3P3	N25
VDD_GPU[1]	N23,P20,P22,R21,T22,U23,V20,W21
VDD_MAIN	AA23,AB12,AC13,AC17,AC21,AD14,AD22,N15,N19,P12,P16,P24,R13,R17,T14,T18,U15,U19,V12,V16,V24,W13,W17,Y14,Y18,Y22
VDD_MIPI_1P0	AD18,AE19
VDD_MIPI_1P8	AD16,AE17
VDD_MIPI_CSI_DIG_1P8	AE21
VDD_MIPI_DSI_DIG_1P8_3P3	AA25
VDD_PCIE_1P8	G13
VDD_PCIE_DIG_1P8_3P3	L11
VDD_PCIE_LDO_1P0_CAP	L13
VDD_QSPI0A_1P8_3P3	AE15
VDD_QSPI0B_1P8_3P3	AE13
VDD_SNVS_4P2	AC25
VDD_SNVS_LDO_1P8_CAP	AE25
VDD_SPI_MCLK_UART_1P8_3P3	R25

Table 124. 21 x 21 mm power supplies contact assignments (continued)

Power rail	Ball reference
VDD_SPI_SAI_1P8_3P3	U25
VDD_TMPR_CSI_1P8_3P3	AD24
VDD_USB_1P8	M18
VDD_USB_3P3	L15
VDD_USB_OTG_1P0	L17
VDD_USB_SS3_LDO_1P0_CAP	M16
VDD_USDHC1_1P8_3P3	M22
VDD_USDHC1_VSELECT_1P8_3P3	L21
VSS_MAIN	A17, A3, A33, AA1, AA13, AA21, AA27, AA3, AA5,AA7,AB10,AB14,AB22,AB26,AB30,AC15,AC19,AC23,AC27,AC33,AD10,AD2, AD20,AD26,AD4,AD6,AE27,AE9,AF10,AF12,AF14,AF16,AF18,AF20,AF22,AF24,AF26,AF30,AG1,AG11,AG13,AG15,AG17,AG19,AG21,AG23, AG25,AG27,AG3,AG33,AG5,AG7,AG9,AH14,AH16,AH18,AH20,AH22,AH24,AH26,AK2,AK30,AK4,AK6,AK8,AL13,AL15,AL17,AL19,AL21,AL23,AL25,AL33, AN1,AN11,AN13,AN27,AN3,AN31,AN5,AN7,AN9,AR3,B14,B20,B8,C1,C11,C13,C17,C19,C23,C27,C3,C31,C35,C5,C7,C9,E15,E29,E33, F10,F18,F2,F20,F24,F4,F6,F8,H30,J1,J11,J13,J15,J17,J19,J21,J23,J25,J27,J3,J33,J5,J7,J9,K10,K12,K14,K16,K18,K20,K22,K24,K26,L27,L9,M10,M2,M26, M30,M4,M6,M8,N13,N17,N21,N27,N33,P10,P14,P18,P26,R1,R15,R19,R23,R27,R3,R5,R9,T10,T16,T20,T24,T26,T28,T30,T32,T34,U13,U17,U21,U27,U9, V10, V14,V18,V2,V22,V26,V4,V6,V8,W15,W19,W23,W27,W31,W33,W35,W9,Y10,Y16, Y20,Y26,Y28,Y30
VSS_SCU_XTAL	AN33,AN35,AR33

[1] VDD_A35 and VDD_GPU can be combined with one power supply.

The following table shows functional contact assignments for the 21 × 21 mm package.

Table 125. 21 x 21 mm functional contact assignments

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
U35	ADC_IN0	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN0	INPUT	PD(50K)
U33	ADC_IN1	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN1	INPUT	PD(50K)
V32	ADC_IN2	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN2	INPUT	PD(50K)
V30	ADC_IN3	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN3	INPUT	PD(50K)
W29	ADC_IN4	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN4	INPUT	PD(50K)
V34	ADC_IN5	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN5	INPUT	PD(50K)
U29	ADC_VREFH	VDD_ADC_1P8	ANA		ADC_VREFH		
U31	ADC_VREFL	VDD_ADC_1P8	ANA		ADC_VREFL		
AK34	ANA_TEST_OUT_N	VDD_SCU_ANA_1P8	ANA		SCU.DSC.TEST_OUT_N		
AL35	ANA_TEST_OUT_P	VDD_SCU_ANA_1P8	ANA		SCU.DSC.TEST_OUT_P		
AK28	CSI_D00	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D02	INPUT	PD(50K)
AL29	CSI_D01	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D03	INPUT	PD(50K)
AP30	CSI_D02	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D04	INPUT	PD(50K)
AJ27	CSI_D03	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D05	INPUT	PD(50K)
AN29	CSI_D04	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D06	INPUT	PD(50K)
AM30	CSI_D05	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D07	INPUT	PD(50K)
AJ25	CSI_D06	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D08	INPUT	PD(50K)
AM28	CSI_D07	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D09	INPUT	PD(50K)
AR29	CSI_HSYNC	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_HSYNC	INPUT	PD(50K)
AL27	CSI_VSYNC	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_VSYNC	INPUT	PD(50K)
AP28	CSI_EN	VDD_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_EN	INPUT	PD(50K)
AM26	CSI_MCLK	VDD_CSI_1P8_3P3	GPIO	ALT4	LSIO.GPIO3.IO01	INPUT	PD(50K)
AK26	CSI_PCLK	VDD_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_PCLK	INPUT	PD(50K)
AR27	CSI_RESET	VDD_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_RESET	INPUT	PD(50K)
G19	EMMC0_CLK	VDD_EMMC0_1P8_3P3	FASTD	ALT4	LSIO.GPIO4.IO07	INPUT	PD(50K)
D20	EMMC0_CMD	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.CMD	INPUT	PD(50K)
C21	EMMC0_DATA0	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA0	INPUT	PD(50K)
A21	EMMC0_DATA1	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA1	INPUT	PD(50K)
E21	EMMC0_DATA2	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA2	INPUT	PD(50K)
H20	EMMC0_DATA3	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA3	INPUT	PD(50K)
B22	EMMC0_DATA4	VDD_EMMC0_VSELECT_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA4	INPUT	PD(50K)
G21	EMMC0_DATA5	VDD_EMMC0_VSELECT_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA5	INPUT	PD(50K)
A23	EMMC0_DATA6	VDD_EMMC0_VSELECT_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA6	INPUT	PD(50K)

Table 125. 21 x 21 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type [1]	Reset Condition [2]			
				Default Mode	Default Function	Default Direction	Default Pull
D22	EMMC0_DATA7	VDD_EMMC0_VSELECT_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA7	INPUT	PD(50K)
H22	EMMC0_RESET_B	VDD_EMMC0_VSELECT_1P8_3P3	GPIO	ALT4	LSIO.GPIO4.IO18	INPUT	PU(50K)
F22	EMMC0_STROBE	VDD_EMMC0_VSELECT_1P8_3P3	FASTD	ALT0	CONN.EMMC0.STROBE	INPUT	PD(50K)
D30	ENET0_MDC	VDD_ENET_MDIO_1P8_3P3	GPIO	ALT4	LSIO.GPIO5.IO11	INPUT	PD(50K)
B32	ENET0_MDIO	VDD_ENET_MDIO_1P8_3P3	GPIO	ALT0	CONN.ENET0.MDIO	INPUT	PU(50K)
F28	ENET0_REFCLK_125M_25M	VDD_ENET_MDIO_1P8_3P3	GPIO	ALT4	LSIO.GPIO5.IO09	INPUT	PD(50K)
B30	ENET0_RGMII_RX_CTL	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RX_CTL	INPUT	PD(50K)
D28	ENET0_RGMII_RXC	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXC	INPUT	PD(50K)
A31	ENET0_RGMII_RXD0	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD0	INPUT	PD(50K)
C29	ENET0_RGMII_RXD1	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD1	INPUT	PD(50K)
G27	ENET0_RGMII_RXD2	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD2	INPUT	PD(50K)
H26	ENET0_RGMII_RXD3	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD3	INPUT	PD(50K)
A29	ENET0_RGMII_TX_CTL	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO4.IO30	INPUT	PD(50K)
H24	ENET0_RGMII_TXC	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO4.IO29	INPUT	PD(50K)
G25	ENET0_RGMII_TXD0	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO4.IO31	INPUT	PD(50K)
B28	ENET0_RGMII_TXD1	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO5.IO00	INPUT	PD(50K)
E27	ENET0_RGMII_TXD2	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO5.IO01	INPUT	PD(50K)
F26	ENET0_RGMII_TXD3	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO5.IO02	INPUT	PD(50K)
F30	ESAI0_FSR	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.FSR	INPUT	PD(50K)
G29	ESAI0_FST	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.FST	INPUT	PD(50K)
H28	ESAI0_SCKR	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.SCKR	INPUT	PD(50K)
E31	ESAI0_SCKT	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.SCKT	INPUT	PD(50K)
D32	ESAI0_TX0	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX0	INPUT	PD(50K)
B34	ESAI0_TX1	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX1	INPUT	PD(50K)
K28	ESAI0_TX2_RX3	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX2_RX3	INPUT	PD(50K)
C33	ESAI0_TX3_RX2	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX3_RX2	INPUT	PD(50K)
F32	ESAI0_TX4_RX1	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX4_RX1	INPUT	PD(50K)
J29	ESAI0_TX5_RX0	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX5_RX0	INPUT	PD(50K)
Y34	FLEXCAN0_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.FLEXCAN0.RX	INPUT	PD(50K)
Y32	FLEXCAN0_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO16	INPUT	PD(50K)
AA33	FLEXCAN1_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.FLEXCAN1.RX	INPUT	PD(50K)
AA35	FLEXCAN1_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO18	INPUT	PD(50K)
AB34	FLEXCAN2_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.FLEXCAN2.RX	INPUT	PD(50K)
AA31	FLEXCAN2_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO20	INPUT	PD(50K)
AE31	JTAG_TCK	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TCK	INPUT	PD(50K)

Table 125. 21 x 21 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
AH34	JTAG_TDI	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TDI	INPUT	PU(50K)
AF32	JTAG_TDO	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TDO	OUTPUT	HiZ
AG35	JTAG_TMS	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TMS	INPUT	PU(50K)
G35	MCLK_IN0	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.ACM.MCLK_IN0	INPUT	PD(50K)
M28	MCLK_IN1	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.ACM.MCLK_IN1	INPUT	PD(50K)
L29	MCLK_OUT0	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO0.IO20	INPUT	PD(50K)
AN21	MIPI_CSI0_CLK_N	VDD_MIPI_1P8	CSI		MIPI_CSI0.CKN		Hi-Z
AR21	MIPI_CSI0_CLK_P	VDD_MIPI_1P8	CSI		MIPI_CSI0.CKP		Hi-Z
AM22	MIPI_CSI0_DATA0_N	VDD_MIPI_1P8	CSI		MIPI_CSI0.DN0		Hi-Z
AP22	MIPI_CSI0_DATA0_P	VDD_MIPI_1P8	CSI		MIPI_CSI0.DP0		Hi-Z
AM20	MIPI_CSI0_DATA1_N	VDD_MIPI_1P8	CSI		MIPI_CSI0.DN1		Hi-Z
AP20	MIPI_CSI0_DATA1_P	VDD_MIPI_1P8	CSI		MIPI_CSI0.DP1		Hi-Z
AN23	MIPI_CSI0_DATA2_N	VDD_MIPI_1P8	CSI		MIPI_CSI0.DN2		Hi-Z
AR23	MIPI_CSI0_DATA2_P	VDD_MIPI_1P8	CSI		MIPI_CSI0.DP2		Hi-Z
AN19	MIPI_CSI0_DATA3_N	VDD_MIPI_1P8	CSI		MIPI_CSI0.DN3		Hi-Z
AR19	MIPI_CSI0_DATA3_P	VDD_MIPI_1P8	CSI		MIPI_CSI0.DP3		Hi-Z
AR25	MIPI_CSI0_GPIO0_00	VDD_MIPI_CSI_DIG_1P8	GPIO	ALT0	MIPI_CSI0.GPIO0.IO00	INPUT	PD(50K)
AP24	MIPI_CSI0_GPIO0_01	VDD_MIPI_CSI_DIG_1P8	GPIO	ALT0	MIPI_CSI0.GPIO0.IO01	INPUT	PD(50K)
AP26	MIPI_CSI0_I2C0_SCL	VDD_MIPI_CSI_DIG_1P8	GPIO	ALT0	MIPI_CSI0.I2C0.SCL	INPUT	PU(50K)
AM24	MIPI_CSI0_I2C0_SDA	VDD_MIPI_CSI_DIG_1P8	GPIO	ALT0	MIPI_CSI0.I2C0.SDA	INPUT	PU(50K)
AN25	MIPI_CSI0_MCLK_OUT	VDD_MIPI_CSI_DIG_1P8	GPIO	ALT4	LSIO.GPIO3.IO04	INPUT	PD(50K)
AJ19	MIPI_DSI0_CLK_N	VDD_MIPI_1P8	DSI		MIPI_DSI0.CKN		Hi-Z
AK20	MIPI_DSI0_CLK_P	VDD_MIPI_1P8	DSI		MIPI_DSI0.CKP		Hi-Z
AJ21	MIPI_DSI0_DATA0_N	VDD_MIPI_1P8	DSI		MIPI_DSI0.DN0		Hi-Z
AK22	MIPI_DSI0_DATA0_P	VDD_MIPI_1P8	DSI		MIPI_DSI0.DP0		Hi-Z
AJ17	MIPI_DSI0_DATA1_N	VDD_MIPI_1P8	DSI		MIPI_DSI0.DN1		Hi-Z
AK18	MIPI_DSI0_DATA1_P	VDD_MIPI_1P8	DSI		MIPI_DSI0.DP1		Hi-Z
AJ23	MIPI_DSI0_DATA2_N	VDD_MIPI_1P8	DSI		MIPI_DSI0.DN2		Hi-Z
AK24	MIPI_DSI0_DATA2_P	VDD_MIPI_1P8	DSI		MIPI_DSI0.DP2		Hi-Z
AJ15	MIPI_DSI0_DATA3_N	VDD_MIPI_1P8	DSI		MIPI_DSI0.DN3		Hi-Z
AK16	MIPI_DSI0_DATA3_P	VDD_MIPI_1P8	DSI		MIPI_DSI0.DP3		Hi-Z
AD32	MIPI_DSI0_GPIO0_00	VDD_MIPI_DSI_DIG_1P8_3P3	GPIO	ALT0	MIPI_DSI0.GPIO0.IO00	INPUT	PD(50K)
AE35	MIPI_DSI0_GPIO0_01	VDD_MIPI_DSI_DIG_1P8_3P3	GPIO	ALT0	MIPI_DSI0.GPIO0.IO01	INPUT	PD(50K)
AC31	MIPI_DSI0_I2C0_SCL	VDD_MIPI_DSI_DIG_1P8_3P3	GPIO	ALT0	MIPI_DSI0.I2C0.SCL	INPUT	PU(50K)
AB28	MIPI_DSI0_I2C0_SDA	VDD_MIPI_DSI_DIG_1P8_3P3	GPIO	ALT0	MIPI_DSI0.I2C0.SDA	INPUT	PU(50K)

Table 125. 21 x 21 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
AM16	MIPI_DSI1_CLK_N	VDD_MIPI_1P8	DSI		MIPI_DSI1.CKN		Hi-Z
AP16	MIPI_DSI1_CLK_P	VDD_MIPI_1P8	DSI		MIPI_DSI1.CKP		Hi-Z
AN15	MIPI_DSI1_DATA0_N	VDD_MIPI_1P8	DSI		MIPI_DSI1.DN0		Hi-Z
AR15	MIPI_DSI1_DATA0_P	VDD_MIPI_1P8	DSI		MIPI_DSI1.DP0		Hi-Z
AN17	MIPI_DSI1_DATA1_N	VDD_MIPI_1P8	DSI		MIPI_DSI1.DN1		Hi-Z
AR17	MIPI_DSI1_DATA1_P	VDD_MIPI_1P8	DSI		MIPI_DSI1.DP1		Hi-Z
AM14	MIPI_DSI1_DATA2_N	VDD_MIPI_1P8	DSI		MIPI_DSI1.DN2		Hi-Z
AP14	MIPI_DSI1_DATA2_P	VDD_MIPI_1P8	DSI		MIPI_DSI1.DP2		Hi-Z
AM18	MIPI_DSI1_DATA3_N	VDD_MIPI_1P8	DSI		MIPI_DSI1.DN3		Hi-Z
AP18	MIPI_DSI1_DATA3_P	VDD_MIPI_1P8	DSI		MIPI_DSI1.DP3		Hi-Z
AD30	MIPI_DSI1_GPIO0_00	VDD_MIPI_DSI_DIG_1P8_3P3	GPIO	ALT0	MIPI_DSI1.GPIO0.IO00	INPUT	PD(50K)
AF34	MIPI_DSI1_GPIO0_01	VDD_MIPI_DSI_DIG_1P8_3P3	GPIO	ALT0	MIPI_DSI1.GPIO0.IO01	INPUT	PD(50K)
AE33	MIPI_DSI1_I2C0_SCL	VDD_MIPI_DSI_DIG_1P8_3P3	GPIO	ALT0	MIPI_DSI1.I2C0.SCL	INPUT	PU(50K)
AC29	MIPI_DSI1_I2C0_SDA	VDD_MIPI_DSI_DIG_1P8_3P3	GPIO	ALT0	MIPI_DSI1.I2C0.SDA	INPUT	PU(50K)
AH28	ON_OFF_BUTTON	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.ON_OFF_BUTTON		
D10	PCIE_CTRL0_CLKREQ_B	VDD_PCIE_DIG_1P8_3P3	GPIO	ALT0	HSIO.PCIE0.CLKREQ_B	INPUT	PD(50K)
H10	PCIE_CTRL0_PERST_B	VDD_PCIE_DIG_1P8_3P3	GPIO	ALT0	HSIO.PCIE0.PERST_B	INPUT	PD(50K)
A11	PCIE_CTRL0_WAKE_B	VDD_PCIE_DIG_1P8_3P3	GPIO	ALT0	HSIO.PCIE0.WAKE_B	INPUT	PU(50K)
F12	PCIE_REF_QR	VDD_PCIE_1P8	PCIE		HSIO.PCIE_IOB.REF_QR		
D12	PCIE_REFCLK100M_N	VDD_PCIE_1P8	PCIE		HSIO.PCIE_IOB.EXT_REFCLK100M_N		
E11	PCIE_REFCLK100M_P	VDD_PCIE_1P8	PCIE		HSIO.PCIE_IOB.EXT_REFCLK100M_P		
H12	PCIE_REXT	VDD_PCIE0_1P0	PCIE		HSIO.PCIE.REXT		
G11	PCIE0_PHY_PLL_REF_RETURN	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.PLL_REF_RETURN		
B12	PCIE0_RX0_N	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.RX0_N		
A13	PCIE0_RX0_P	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.RX0_P		
A9	PCIE0_TX0_N	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.TX0_N		
B10	PCIE0_TX0_P	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.TX0_P		
AJ35	PMIC_I2C_SCL	VDD_ANA1_1P8	SCU	ALT0	SCU.PMIC_I2C.SCL	INPUT	PU(50K)
AH32	PMIC_I2C_SDA	VDD_ANA1_1P8	SCU	ALT0	SCU.PMIC_I2C.SDA	INPUT	PU(50K)
AJ33	PMIC_INT_B	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.PMIC_INT_B	INPUT	PU(50K)
AR31	PMIC_ON_REQ	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.PMIC_ON_REQ		
AG31	POR_B	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.POR_B	INPUT	PU(50K)
AK14	QSPI0A_DATA0	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA0	INPUT	PD(50K)
AR13	QSPI0A_DATA1	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA1	INPUT	PD(50K)
AJ13	QSPI0A_DATA2	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA2	INPUT	PD(50K)

Table 125. 21 x 21 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
AH12	QSPI0A_DATA3	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA3	INPUT	PD(50K)
AL11	QSPI0A_DQS	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DQS	INPUT	PD(50K)
AP12	QSPI0A_SCLK	VDD_QSPI0A_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO16	INPUT	PD(50K)
AM12	QSPI0A_SS0_B	VDD_QSPI0A_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO14	INPUT	PU(50K)
AK12	QSPI0A_SS1_B	VDD_QSPI0A_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO15	INPUT	PU(50K)
AM10	QSPI0B_DATA0	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA0	INPUT	PD(50K)
AL9	QSPI0B_DATA1	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA1	INPUT	PD(50K)
AJ11	QSPI0B_DATA2	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA2	INPUT	PD(50K)
AM8	QSPI0B_DATA3	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA3	INPUT	PD(50K)
AK10	QSPI0B_DQS	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DQS	INPUT	PD(50K)
AR11	QSPI0B_SCLK	VDD_QSPI0B_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO17	INPUT	PD(50K)
AH10	QSPI0B_SS0_B	VDD_QSPI0B_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO23	INPUT	PU(50K)
AJ9	QSPI0B_SS1_B	VDD_QSPI0B_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO24	INPUT	PU(50K)
AP32	RTC_XTALI	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.RTC_XTALI		
AM32	RTC_XTALO	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.RTC_XTALO		
M34	SAI0_RXD	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SAI0.RXD	INPUT	PD(50K)
J35	SAI0_TXC	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SAI0.TXC	INPUT	PD(50K)
K34	SAI0_TXD	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SAI0.TXD	INPUT	PD(50K)
L33	SAI0_TXFS	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SAI0.TXFS	INPUT	PD(50K)
L35	SAI1_RXC	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SAI1.RXC	INPUT	PD(50K)
M32	SAI1_RXD	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SAI1.RXD	INPUT	PD(50K)
N35	SAI1_RXFS	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SAI1.RXFS	INPUT	PD(50K)
AJ31	SCU_BOOT_MODE0	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.BOOT_MODE0	INPUT	PD(50K)
AK32	SCU_BOOT_MODE1	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.BOOT_MODE1	INPUT	PD(50K)
AL31	SCU_BOOT_MODE2	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.BOOT_MODE2	INPUT	PD(50K)
AJ29	SCU_BOOT_MODE3	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.BOOT_MODE3	INPUT	PD(50K)
AF28	SCU_GPIO0_00	VDD_ANA1_1P8	GPIO	ALT0	SCU.GPIO0.IO00	INPUT	PD(50K)
AH30	SCU_GPIO0_01	VDD_ANA1_1P8	GPIO	ALT0	SCU.GPIO0.IO01	INPUT	PU(50K)
AG29	SCU_PMIC_STANDBY	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.PMIC_STANDBY	OUTPUT	HiZ
AD28	SCU_WDOG_OUT[3]	VDD_ANA1_1P8	SCU	ALT1	SCU.WDOG0.WDOG_OUT	OUTPUT	PD(50K)
E35	SPDIF0_EXT_CLK	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.SPDIF0.EXT_CLK	INPUT	PD(50K)
G31	SPDIF0_RX	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.SPDIF0.RX	INPUT	PD(50K)
D34	SPDIF0_TX	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT4	LSIO.GPIO0.IO11	INPUT	PD(50K)
R33	SPI0_CS0	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SPI0.CS0	INPUT	PD(50K)
R35	SPI0_CS1	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SPI0.CS1	INPUT	PD(50K)

Table 125. 21 x 21 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
P30	SPI0_SCK	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SPI0.SCK	INPUT	PD(50K)
P34	SPI0_SDI	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SPI0.SDI	INPUT	PD(50K)
R31	SPI0_SDO	VDD_SPI_SAI_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO06	INPUT	PD(50K)
P28	SPI2_CS0	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SPI2.CS0	INPUT	PD(50K)
R29	SPI2_SCK	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SPI2.SCK	INPUT	PD(50K)
N31	SPI2_SDI	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	ADMA.SPI2.SDI	INPUT	PD(50K)
P32	SPI2_SDO	VDD_SPI_SAI_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO01	INPUT	PD(50K)
J31	SPI3_CS0	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.CS0	INPUT	PD(50K)
K30	SPI3_CS1	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.CS1	INPUT	PD(50K)
H32	SPI3_SCK	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.SCK	INPUT	PD(50K)
G33	SPI3_SDI	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.SDI	INPUT	PD(50K)
F34	SPI3_SDO	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO0.IO14	INPUT	PD(50K)
AE29	TEST_MODE_SELECT	VDD_ANA1_1P8	SCU	ALT0	SCU.TCU.TEST_MODE_SELECT	INPUT	PD(50K)
AB32	UART0_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.UART0.RX	INPUT	PD(50K)
AA29	UART0_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO22	INPUT	PD(50K)
K32	UART1_CTS_B	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.UART1.CTS_B	INPUT	PD(50K)
N29	UART1_RTS_B	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPT0.CLK	INPUT	PD(50K)
L31	UART1_RX	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.UART1.RX	INPUT	PD(50K)
H34	UART1_TX	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO0.IO21	INPUT	PD(50K)
AD34	UART2_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.UART2.RX	INPUT	PD(50K)
AC35	UART2_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO23	INPUT	PD(50K)
E19	USB_OTG1_DN	VDD_USB_3P3	OTG		CONN.USB_OTG1.DN		
D18	USB_OTG1_DP	VDD_USB_3P3	OTG		CONN.USB_OTG1.DP		
G17	USB_OTG1_ID	VDD_USB_3P3	OTG		CONN.USB_OTG1.ID		
H18	USB_OTG1_VBUS		OTG		CONN.USB_OTG1.VBUS		
D16	USB_OTG2_DN	VDD_USB_3P3	OTG		CONN.USB_OTG2.DM		
E17	USB_OTG2_DP	VDD_USB_3P3	OTG		CONN.USB_OTG2.DP		
F16	USB_OTG2_ID	VDD_USB_3P3	OTG		CONN.USB_OTG2.ID		
D14	USB_OTG2_REXT	VDD_USB_3P3	OTG		CONN.USB_OTG2.RTRIM		
H16	USB_OTG2_VBUS		OTG		CONN.USB_OTG2.VBUS		
E13	USB_SS3_REXT	VDD_USB_1P8	USB3		CONN.USB_SS3.REXT		
B18	USB_SS3_RX_N	VDD_USB_SS3_LDO_1P0_CAP	USB3		CONN.USB_SS3.RX_M_LN_0		Hi-Z
A19	USB_SS3_RX_P	VDD_USB_SS3_LDO_1P0_CAP	USB3		CONN.USB_SS3.RX_P_LN_0		Hi-Z
F14	USB_SS3_TC0	VDD_USB_3P3	GPIO	ALT0	ADMA.I2C1.SCL	INPUT	PD(50K)
H14	USB_SS3_TC1	VDD_USB_3P3	GPIO	ALT0	ADMA.I2C1.SCL	INPUT	PD(50K)

Table 125. 21 x 21 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type [1]	Reset Condition [2]			
				Default Mode	Default Function	Default Direction	Default Pull
G15	USB_SS3_TC2	VDD_USB_3P3	GPIO	ALT0	ADMA.I2C1.SDA	INPUT	PD(50K)
C15	USB_SS3_TC3	VDD_USB_3P3	GPIO	ALT0	ADMA.I2C1.SDA	INPUT	PD(50K)
A15	USB_SS3_TX_N	VDD_USB_SS3_LDO_1P0_CAP	USB3		CONN.USB_SS3.TX_M_LN_0		
B16	USB_SS3_TX_P	VDD_USB_SS3_LDO_1P0_CAP	USB3		CONN.USB_SS3.TX_P_LN_0		
E23	USDHC1_CD_B	VDD_USDHC1_VSELECT_1P8_3P3	FASTD	ALT0	CONN.USDHC1.CD_B	INPUT	PU(50K)
G23	USDHC1_CLK	VDD_USDHC1_1P8_3P3	FASTD	ALT4	LSIO.GPIO4.IO23	INPUT	PD(50K)
C25	USDHC1_CMD	VDD_USDHC1_1P8_3P3	FASTD	ALT0	CONN.USDHC1.CMD	INPUT	PU(50K)
A27	USDHC1_DATA0	VDD_USDHC1_1P8_3P3	FASTD	ALT0	CONN.USDHC1.DATA0	INPUT	PU(50K)
B26	USDHC1_DATA1	VDD_USDHC1_1P8_3P3	FASTD	ALT0	CONN.USDHC1.DATA1	INPUT	PU(50K)
D26	USDHC1_DATA2	VDD_USDHC1_1P8_3P3	FASTD	ALT0	CONN.USDHC1.DATA2	INPUT	PU(50K)
E25	USDHC1_DATA3	VDD_USDHC1_1P8_3P3	FASTD	ALT0	CONN.USDHC1.DATA3	INPUT	PU(50K)
B24	USDHC1_RESET_B	VDD_USDHC1_VSELECT_1P8_3P3	FASTD	ALT4	LSIO.GPIO4.IO19	INPUT	PU(50K)
A25	USDHC1_VSELECT	VDD_USDHC1_VSELECT_1P8_3P3	FASTD	ALT4	LSIO.GPIO4.IO20	INPUT	PD(50K)
D24	USDHC1_WP	VDD_USDHC1_VSELECT_1P8_3P3	FASTD	ALT0	CONN.USDHC1.WP	INPUT	PD(50K)
AP34	XTALI	VDD_ANA1_1P8	ANA		SCU.DSC.XTALI		
AM34	XTALO	VDD_ANA1_1P8	ANA		SCU.DSC.XTALO		

1 FASTD are GPIO balls configured for high speed operation using the FASTRZ control.

2 Reset condition shown is before boot code execution. For pad changes after boot code execution, see the System Boot chapter of the device reference manual.

3 SCU_WDOG_OUT was previously named JTAG_TRST_B; it has been renamed because its functionality has changed.

The following table shows DDR pin function.

Table 126. DRAM pin function

Ball Name	Ball	LPDDR4 function	DDR3L function
DDR_ATO	AB8	—	—
DDR_CK0_N	Y6	DDR_CK0_N	DDR_CK0_N
DDR_CK0_P	W5	DDR_CK0_P	DDR_CK0_P
DDR_CK1_N	N5	DDR_CK1_N	DDR_CK1_N
DDR_CK1_P	P6	DDR_CK1_P	DDR_CK1_P
DDR_DCF00	W1	CA2_A	A5
DDR_DCF01	U3	CA4_A	A6
DDR_DCF03	U1	CA5_A	A7
DDR_DCF04	U7	—	A8
DDR_DCF05	U5	—	A9
DDR_DCF07	T2	—	RAS#
DDR_DCF08	AB4	CA3_A	A3
DDR_DCF09	AB6	ODT_CA_A	ODT
DDR_DCF10	AC5	CS0_A	A1
DDR_DCF11	W3	CA0_A	A0
DDR_DCF12	Y8	CS1_A	A2
DDR_DCF14	Y2	CKE0_A	—
DDR_DCF15	Y4	CKE1_A	—
DDR_DCF16	W7	CA1_A	A4
DDR_DCF17	N3	CA4_B	A12
DDR_DCF18	L1	RESET_N	RESET_N
DDR_DCF19	N1	CA5_B	A14
DDR_DCF20	P4	—	A15
DDR_DCF21	T8	—	BA0
DDR_DCF22	P2	—	BA1
DDR_DCF23	T4	—	BA2
DDR_DCF24	T6	—	CAS#
DDR_DCF25	K8	ODT_CA_B	ODT1
DDR_DCF26	L7	CA3_B	A13
DDR_DCF27	K4	CA0_B	A10
DDR_DCF28	K6	CS0_B	CS_N[0]

Table 126. DRAM pin function (continued)

Ball Name	Ball	LPDDR4 function	DDR3L function
DDR_DCF29	K2	CS1_B	CS_N[1]
DDR_DCF30	N7	CKE0_B	CKE0
DDR_DCF31	L5	CKE1_B	CKE1
DDR_DCF32	L3	CA1_B	A11
DDR_DCF33	P8	CA2_B	WE#
DDR_DM0	AJ7	DDR_DMI0	DDR_DMI0
DDR_DM1	AF4	DDR_DMI1	DDR_DMI1
DDR_DM2	D4	DDR_DMI2	DDR_DMI2
DDR_DM3	E1	DDR_DMI3	DDR_DMI3
DDR_DM4	AP6	—	DDR_DMI4
DDR_DQ00	AF6	DDR_DQ00	DDR_DQ00
DDR_DQ01	AE5	DDR_DQ01	DDR_DQ01
DDR_DQ02	AH8	DDR_DQ02	DDR_DQ02
DDR_DQ03	AF8	DDR_DQ03	DDR_DQ03
DDR_DQ04	AM4	DDR_DQ04	DDR_DQ04
DDR_DQ05	AM6	DDR_DQ05	DDR_DQ05
DDR_DQ06	AL5	DDR_DQ06	DDR_DQ06
DDR_DQ07	AL7	DDR_DQ07	DDR_DQ07
DDR_DQ08	AJ1	DDR_DQ08	DDR_DQ08
DDR_DQ09	AJ3	DDR_DQ09	DDR_DQ09
DDR_DQ10	AH2	DDR_DQ10	DDR_DQ10
DDR_DQ11	AH4	DDR_DQ11	DDR_DQ11
DDR_DQ12	AC3	DDR_DQ12	DDR_DQ12
DDR_DQ13	AE3	DDR_DQ13	DDR_DQ13
DDR_DQ14	AB2	DDR_DQ14	DDR_DQ14
DDR_DQ15	AC1	DDR_DQ15	DDR_DQ15
DDR_DQ16	B6	DDR_DQ16	DDR_DQ16
DDR_DQ17	E9	DDR_DQ17	DDR_DQ17
DDR_DQ18	E7	DDR_DQ18	DDR_DQ18
DDR_DQ19	D8	DDR_DQ19	DDR_DQ19
DDR_DQ20	G7	DDR_DQ20	DDR_DQ20
DDR_DQ21	H8	DDR_DQ21	DDR_DQ21
DDR_DQ22	H6	DDR_DQ22	DDR_DQ22

Table 126. DRAM pin function (continued)

Ball Name	Ball	LPDDR4 function	DDR3L function
DDR_DQ23	G5	DDR_DQ23	DDR_DQ23
DDR_DQ24	H2	DDR_DQ24	DDR_DQ24
DDR_DQ25	H4	DDR_DQ25	DDR_DQ25
DDR_DQ26	G3	DDR_DQ26	DDR_DQ26
DDR_DQ27	G1	DDR_DQ27	DDR_DQ27
DDR_DQ28	A7	DDR_DQ28	DDR_DQ28
DDR_DQ29	B4	DDR_DQ29	DDR_DQ29
DDR_DQ30	B2	DDR_DQ30	DDR_DQ30
DDR_DQ31	A5	DDR_DQ31	DDR_DQ31
DDR_DQ32	AL1	—	DDR_DQ32
DDR_DQ33	AM2	—	DDR_DQ33
DDR_DQ34	AL3	—	DDR_DQ34
DDR_DQ35	AP2	—	DDR_DQ35
DDR_DQ36	AP8	—	DDR_DQ36
DDR_DQ37	AP10	—	DDR_DQ37
DDR_DQ38	AR9	—	DDR_DQ38
DDR_DQ39	AR7	—	DDR_DQ39
DDR_DQS0_N	AH6	DDR_DQS0_N	DDR_DQS0_N
DDR_DQS0_P	AJ5	DDR_DQS0_P	DDR_DQS0_P
DDR_DQS1_N	AE1	DDR_DQS1_N	DDR_DQS1_N
DDR_DQS1_P	AF2	DDR_DQS1_P	DDR_DQS1_P
DDR_DQS2_N	E5	DDR_DQS2_N	DDR_DQS2_N
DDR_DQS2_P	D6	DDR_DQS2_P	DDR_DQS2_P
DDR_DQS3_N	E3	DDR_DQS3_N	DDR_DQS3_N
DDR_DQS3_P	D2	DDR_DQS3_P	DDR_DQS3_P
DDR_DQS4_N	AR5	—	DDR_DQS4_N
DDR_DQS4_P	AP4	—	DDR_DQS4_P
DDR_DTO0	AC7	—	—
DDR_DTO1	AE7	—	—
DDR_VREF	AD8	—	—
DDR_ZQ	G9	—	—

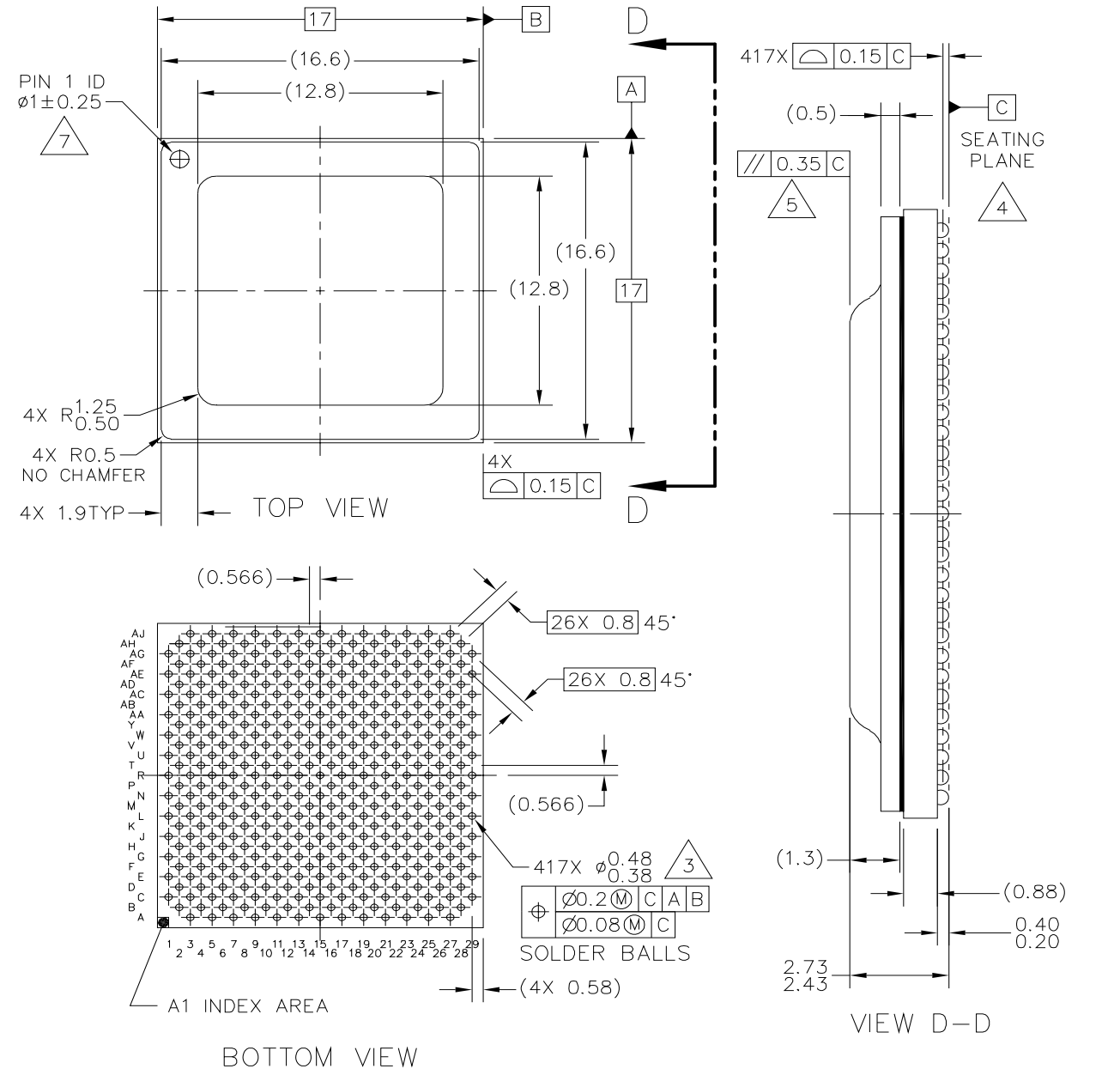
6.2 FCPBGA, 17 x 17 mm, 0.8 mm pitch

This section includes the following:

- Mechanical package drawing
- Ball map for case FCPBGA, 17 x 17 mm, 0.8 mm pitch
- Contact assignments

6.2.1 17 x 17 mm package case outline

The following figure shows the top, bottom, and side views of the 17 x 17 mm package.



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TITLE: FCPBGA, WITH LID, 17 X 17 X 2.58 PKG, 0.8 MM PITCH, 417 I/O INTERSTITIAL	DOCUMENT NO: 98ASA01087D REV: A
	STANDARD: NON–JEDEC
	SOT1932–1 SHEET: 1 OF 3

Figure 60. 17 x 17 mm Package Top, Bottom, and Side Views

The following notes pertain to the preceding figure, “17 x 17 mm Package Top, Bottom, and Side Views.”

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
4. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
7. PIN 1 THRU HOLE SHALL BE CENTERED WITHIN FOOT AREA.
8. LID OVERHANG ON SUBSTRATE NOT ALLOWED.

Figure 61. Notes on 17 x 17 mm Package Top, Bottom, and Side Views

6.2.2 17 x 17 mm, 0.8 mm pitch, ball map

The following page shows the 17 x 17 mm, 0.8 mm pitch, ball map.

Package information and functional contact assignments for FCPBGA, 17 x 17 mm, 0.8 mm pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A			VSS_MAIN		DDR_DCF18		DDR_CK1_P		DDR_DCF26		PCIE_CTRL0_PERST_B		PCIE0_TX0_P		PCIE0_RX0_P		USB_OTG1_ID		USB_OTG1_DP		EMMC0_DATA0		ENET0_RGMII_RXC		ENET0_MDC		VSS_MAIN		
B		DDR_DCF01		DDR_DCF07		DDR_DCF17		DDR_CK1_N		DDR_DCF21		PCIE0_TX0_N		PCIE_CTRL0_WAKE_B		PCIE0_RX0_N		USB_OTG1_DN		EMMC0_RESET_B		ENET0_RGMII_TXD3		ENET0_RGMII_RXD3		ESAI0_FSR		ESAI0_TX4_RX1	
C	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		PCIE_REFCLK100M_N		VSS_MAIN		VSS_MAIN		VDD_EMMC0_VSELECT_1P8_3P3		ENET0_RGMII_TXD1		ENET0_RGMII_RXD0		ESAI0_SCKT		ESAI0_TX2_RX3		VSS_MAIN
D		DDR_DCF12		DDR_DCF05		DDR_DCF20		DDR_DCF29		DDR_DCF28		VDD_USB_3P3		PCIE_REFCLK100M_P		VDD_USB_SS3_LDO_1P0_CAP		VDD_EMMC0_1P8_3P3		VDD_ENET0_VSELECT_1P8_2P5_3P3		ENET0_RGMII_RXD1		ESAI0_TX3_RX2		SPI3_CS0		SPI3_SCK	
E	DDR_DCF15		DDR_DCF03		DDR_DCF22		DDR_DCF32		DDR_DCF27		PCIE_CTRL0_CLKREQ_B		EMMC0_CMD		EMMC0_DATA6		VSS_MAIN		EMMC0_DATA3		VDD_ENET0_1P8_2P5_3P3		ESAI0_FST		ESAI0_TX1		SPDIF0_EXT_CLK		UART1_RX
F		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		DDR_ZQ		PCIE_REF_QR		EMMC0_CLK		EMMC0_DATA5		EMMC0_DATA1		ENET0_RGMII_TXD0		ENET0_REFCLK_125M_25M		SPDIF0_RX		VDD_ENET_MDIO_1P8_33		SPI3_CS1	
G	DDR_DCF10		DDR_CK0_N		DDR_DCF00		DDR_DCF33		DDR_DCF31		PCIE0_PHY_PLL_REF_RETURN		USB_SS3_TC1		EMMC0_DATA2		EMMC0_DATA4		ENET0_RGMII_TXC		ENET0_RGMII_RXD2		ESAI0_TX0		SPI3_SDO		UART1_CTS_B		UART1_RTS_B
H		DDR_CK0_P		DDR_DCF24		DDR_DCF19		DDR_DCF30		DDR_DCF25		PCIE_REXT		USB_SS3_TC3		EMMC0_DATA7		ENET0_RGMII_TX_CTL		ENET0_RGMII_RX_CTL		ESAI0_SCKR		SPI3_SDI		VSS_MAIN		SPI0_CS0	
J	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_PCIE_DIG_1P8_3P3		VDD_PCIE_1P8		VSS_MAIN		USB_OTG1_VBUS		EMMC0_STROBE		ENET0_RGMII_TXD2		ENET0_MDIO		SPDIF0_TX		UART1_TX		SPI0_SDO		SPI0_SDI
K		DDR_DCF08		DDR_DCF14		DDR_DCF04		VDD_DDR_VDDQ		VDD_ANA0_1P8		VDD_PCIE_LDO_1P0_CAP		VDD_USB_1P8		VDD_MAIN		VSS_MAIN		VDD_GPU		ESAI0_TX5_RX0		MCLK_OUT0		VDD_ESAI_SPDIF_1P8_2P5_3P3		SPI0_CS1	
L	DDR_DCF11		DDR_DCF09		DDR_DCF23		DDR_DCF16		VSS_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VDD_GPU		VDD_MAIN		MCLK_IN0		SPI0_SCK		VDD_SPI_MCLK_UART_1P8_3P3		VSS_MAIN
M		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_DDR_VDDQ		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VSS_MAIN		MCLK_IN1		VSS_MAIN		VSS_MAIN		ADC_VREFH	
N	DDR_DQ02		DDR_DQ00		DDR_DQ13		DDR_DQ15		VDD_DDR_VDDQ		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VSS_MAIN		ADC_IN1		ADC_IN3		ADC_IN2		ADC_VREFL
P		DDR_DQ01		DDR_DQ12		DDR_DQ14		VDD_DDR_VDDQ		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VDD_ADC_1P8		ADC_IN0		ADC_IN5		ADC_IN4	
R	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VSS_MAIN		VDD_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
T		DDR_DQ03		DDR_DQS1_N		DDR_DM1		VDD_DDR_VDDQ		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU		VSS_MAIN		FLEXCAN0_RX		FLEXCAN1_RX		VDD_ADC_DIG_1P8		FLEXCAN2_RX	
U	DDR_DQS0_N		DDR_DQS0_P		DDR_DQS1_P		DDR_DTO0		VDD_DDR_VDDQ		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VDD_CAN_UART_1P8_3P3		UART0_TX		FLEXCAN0_TX		FLEXCAN2_TX		FLEXCAN1_TX
V		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_DDR_VDDQ		VSS_MAIN		VDD_A35		VDD_A35		VDD_A35		VSS_MAIN		VDD_MAIN		MIPI_DSI0_I2C0_SDA		VSS_MAIN		UART2_TX		UART0_RX	
W	DDR_DM0		DDR_DQ10		DDR_ATO		VDD_DDR_PLL_1P8		VSS_MAIN		VSS_MAIN		VDD_A35		VDD_A35		VDD_A35		VSS_MAIN		VDD_ANA1_1P8		JTAG_TMS		MIPI_DSI1_I2C0_SDA		MIPI_DSI0_I2C0_SCL		UART2_RX
Y		DDR_DQ04		DDR_DQ08		DDR_VREF		VDD_DDR_VDDQ		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		SCU_GPIO0_00		JTAG_TDO		VDD_SNVS_4P2		MIPI_DSI1_I2C0_SCL	
AA	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_DDR_VDDQ		VDD_MAIN		VDD_MIPI_1P8		VDD_MIPI_1P0		VSS_MAIN		VDD_MAIN		VDD_TMPR_CSI_1P8_3P3		PMIC_INT_B		TEST_MODE_SELECT		VSS_MAIN		JTAG_TCK
AB		DDR_DQ05		DDR_DQ11		DDR_DTO1		VDD_DDR_VDDQ		QSPI0A_DQS		QSPI0A_SS0_B		VDD_MIPI_1P8		VDD_MIPI_1P0		VDD_MIPI_CSI_DIG_1P8		PMIC_ON_REQ		SCU_BOOT_MODE3		SCU_PMIC_STANDBY		VDD_SNVS_LDO_1P8_CAP		SCU_WDOG_OUT	
AC	DDR_DQ06		DDR_DQ07		DDR_DQ09		QSPI0B_DATA0		QSPI0A_DATA2		MIPI_CSI0_DATA3_N		MIPI_CSI0_DATA1_N		MIPI_CSI0_CLK_N		MIPI_CSI0_DATA0_N		MIPI_CSI0_DATA2_N		CSI_D00		SCU_BOOT_MODE1		SCU_GPIO0_01		PMIC_I2C_SCL		JTAG_TDI
AD		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_QSPI0A_1P8_3P3		QSPI0A_SS1_B		MIPI_CSI0_DATA3_P		MIPI_CSI0_DATA1_P		MIPI_CSI0_CLK_P		MIPI_CSI0_DATA0_P		MIPI_CSI0_DATA2_P		CSI_D02		VSS_MAIN		SCU_BOOT_MODE0		POR_B	
AE	QSPI0B_DATA1		QSPI0B_DATA3		VDD_QSPI0B_1P8_3P3		QSPI0B_SS0_B		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		ANA_TEST_OUT_P		SCU_BOOT_MODE2		VSS_MAIN		PMIC_I2C_SDA
AF		QSPI0B_DATA2		QSPI0B_DQS		QSPI0B_SS1_B		MIPI_DSI1_DATA0_N		MIPI_DSI1_DATA1_N		MIPI_DSI0_DATA3_N		MIPI_DSI0_CLK_N		MIPI_DSI0_DATA2_N		MIPI_CSI0_MCLK_OUT		CSI_VSYNC		VDD_CSI_1P8_3P3		ANA_TEST_OUT_N		RTC_XTALO		XTALO	
AG	VSS_MAIN		QSPI0A_SCLK		QSPI0A_DATA3		MIPI_DSI1_DATA2_N		MIPI_DSI1_CLK_N		MIPI_DSI1_DATA3_N		MIPI_DSI0_DATA1_N		MIPI_DSI0_DATA0_N		VSS_MAIN		CSI_PCLK		CSI_D04		CSI_D03		VSS_MAIN		VSS_SCU_XTAL		VSS_SCU_XTAL
AH		QSPI0B_SCLK		QSPI0A_DATA1		VSS_MAIN		MIPI_DSI1_DATA0_P		MIPI_DSI1_DATA1_P		MIPI_DSI0_DATA3_P		MIPI_DSI0_CLK_P		MIPI_DSI0_DATA2_P		CSI_RESET		CSI_HSYNC		CSI_D07		CSI_D01		RTC_XTALI		XTALI	
AJ			VSS_MAIN		QSPI0A_DATA0		MIPI_DSI1_DATA2_P		MIPI_DSI1_CLK_P		MIPI_DSI1_DATA3_P		MIPI_DSI0_DATA1_P		MIPI_DSI0_DATA0_P		CSI_EN		CSI_MCLK		CSI_D06		CSI_D05		ON_OFF_BUTTON		VSS_SCU_XTAL		

6.2.3 17 x 17 mm power supplies and functional contact assignments

The following table shows the power supplies contact assignments for the 17 x 17 mm package.

Table 127. 17 x 17 mm power supplies contact assignments

Power rail	Ball reference
VDD_A35	V12,V14,V16,W13,W15,W17
VDD_ADC_1P8	P22
VDD_ADC_DIG_1P8	T26
VDD_ANA0_1P8	K10
VDD_ANA1_1P8	W21
VDD_CAN_UART_1P8_3P3	U21
VDD_CSI_1P8_3P3	AF22
VDD_DDR_PLL_1P8	W7
VDD_DDR_VDDQ	AA9,AB8,K8,M8,N9,P8,T8,U9,V8,Y8
VDD_EMMC0_1P8_3P3	D18
VDD_EMMC0_VSELECT_1P8_3P3	C19
VDD_ENET_MDIO_1P8_3P3	F26
VDD_ENET0_1P8_2P5_3P3	E21
VDD_ENET0_VSELECT_1P8_2P5_3P3	D20
VDD_ESAI_SPDIF_1P8_2P5_3P3	K26
VDD_GPU	K20,L17,L19,M18,N19,P20,R17,T18
VDD_MAIN	AA11,AA19,K16,L13,L21,M10,M14,N11,N15,P12,P16,R13,R21,T10,T14,U11,U15, U19,V20,Y10,Y14,Y18
VDD_MIPI_1P0	AA15,AB16
VDD_MIPI_1P8	AA13,AB14
VDD_MIPI_CSI_DIG_1P8	AB18
VDD_PCIE_1P8	J11
VDD_PCIE_DIG_1P8_3P3	J9
VDD_PCIE_LDO_1P0_CAP	K12
VDD_QSPI0A_1P8_3P3	AD8
VDD_QSPI0B_1P8_3P3	AE5
VDD_SNVS_4P2	Y26
VDD_SNVS_LDO_1P8_CAP	AB26
VDD_SPI_MCLK_UART_1P8_3P3	L27
VDD_TMPR_CSI_1P8_3P3	AA21

Table 127. 17 x 17 mm power supplies contact assignments (continued)

Power rail	Ball reference
VDD_USB_1P8	K14
VDD_USB_3P3	D12
VDD_USB_SS3_LDO_1P0_CAP	D16
VSS_MAIN	A3,A27,C1,C3,C5,C7,C9,C11,C15,C17,C29,E17,F2,F4,F6,F8,H26,J1,J3,J5,J7,J13,K18,L9,L11,L15,L29,M2,M4,M6,M12,M16,M20,M24,M26,N13,N17,N21,P10,P14,P18,R1,R3,R5,R7,R9,R11,R15,R19,R23,R25,R27,R29,T12,T16,T20,U13,U17,V2,V4,V6,V10,V18,V24,W9,W11,W19,Y12,Y16,Y20,AA1,AA3,AA5,AA7,AA17,AA27,AD2,AD4,AD6,AD24,AE9,AE11,AE13,AE15,AE17,AE19,AE21,AE27,AG1,AG17,AG25,AH6,AJ3
VSS_SCU_XTAL	AG27,AG29,AJ27

The following table shows functional contact assignments for the 17 x 17 mm package.

Table 128. 17 x 17 mm functional contact assignments

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
P24	ADC_IN0	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN0	INPUT	PD(50K)
N23	ADC_IN1	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN1	INPUT	PD(50K)
N27	ADC_IN2	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN2	INPUT	PD(50K)
N25	ADC_IN3	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN3	INPUT	PD(50K)
P28	ADC_IN4	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN4	INPUT	PD(50K)
P26	ADC_IN5	VDD_ADC_DIG_1P8	GPIO	ALT0	ADMA.ADC.IN5	INPUT	PD(50K)
M28	ADC_VREFH	VDD_ADC_1P8	ANA		ADC_VREFH		
N29	ADC_VREFL	VDD_ADC_1P8	ANA		ADC_VREFL		
AF24	ANA_TEST_OUT_N	VDD_SCU_ANA_1P8	ANA		SCU.DSC.TEST_OUT_N		
AE23	ANA_TEST_OUT_P	VDD_SCU_ANA_1P8	ANA		SCU.DSC.TEST_OUT_P		
AC21	CSI_D00	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D02	INPUT	PD(50K)
AH24	CSI_D01	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D03	INPUT	PD(50K)
AD22	CSI_D02	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D04	INPUT	PD(50K)
AG23	CSI_D03	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D05	INPUT	PD(50K)
AG21	CSI_D04	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D06	INPUT	PD(50K)
AJ23	CSI_D05	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D07	INPUT	PD(50K)
AJ21	CSI_D06	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D08	INPUT	PD(50K)
AH22	CSI_D07	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_D09	INPUT	PD(50K)
AH20	CSI_HSYNC	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_HSYNC	INPUT	PD(50K)
AF20	CSI_VSYNC	VDD_TMPR_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_VSYNC	INPUT	PD(50K)
AJ17	CSI_EN	VDD_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_EN	INPUT	PD(50K)
AJ19	CSI_MCLK	VDD_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_MCLK	INPUT	PD(50K)
AG19	CSI_PCLK	VDD_CSI_1P8_3P3	GPIO	ALT4	LSIO.GPIO3.IO00	INPUT	PD(50K)
AH18	CSI_RESET	VDD_CSI_1P8_3P3	GPIO	ALT0	CI_PI.CSI_RESET	INPUT	PD(50K)
W5	DDR_ATO	VDD_DDR_VDDQ	DDR		DRC.ATO		
G3	DDR_CK0_N	VDD_DDR_VDDQ	DDR		DRC.CK0_N		
H2	DDR_CK0_P	VDD_DDR_VDDQ	DDR		DRC.CK0_P		
B8	DDR_CK1_N	VDD_DDR_VDDQ	DDR		DRC.CK1_N		
A7	DDR_CK1_P	VDD_DDR_VDDQ	DDR		DRC.CK1_P		
G5	DDR_DCF00	VDD_DDR_VDDQ	DDR		DRC.DCF00		
B2	DDR_DCF01	VDD_DDR_VDDQ	DDR		DRC.DCF01		

Table 128. 17 x 17 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
E3	DDR_DCF03	VDD_DDR_VDDQ	DDR		DRC.DCF03		
K6	DDR_DCF04	VDD_DDR_VDDQ	DDR		DRC.DCF04		
D4	DDR_DCF05	VDD_DDR_VDDQ	DDR		DRC.DCF05		
B4	DDR_DCF07	VDD_DDR_VDDQ	DDR		DRC.DCF07		
K2	DDR_DCF08	VDD_DDR_VDDQ	DDR		DRC.DCF08		
L3	DDR_DCF09	VDD_DDR_VDDQ	DDR		DRC.DCF09		
G1	DDR_DCF10	VDD_DDR_VDDQ	DDR		DRC.DCF10		
L1	DDR_DCF11	VDD_DDR_VDDQ	DDR		DRC.DCF11		
D2	DDR_DCF12	VDD_DDR_VDDQ	DDR		DRC.DCF12		
K4	DDR_DCF14	VDD_DDR_VDDQ	DDR		DRC.DCF14		
E1	DDR_DCF15	VDD_DDR_VDDQ	DDR		DRC.DCF15		
L7	DDR_DCF16	VDD_DDR_VDDQ	DDR		DRC.DCF16		
B6	DDR_DCF17	VDD_DDR_VDDQ	DDR		DRC.DCF17		
A5	DDR_DCF18	VDD_DDR_VDDQ	DDR		DRC.DCF18		
H6	DDR_DCF19	VDD_DDR_VDDQ	DDR		DRC.DCF19		
D6	DDR_DCF20	VDD_DDR_VDDQ	DDR		DRC.DCF20		
B10	DDR_DCF21	VDD_DDR_VDDQ	DDR		DRC.DCF21		
E5	DDR_DCF22	VDD_DDR_VDDQ	DDR		DRC.DCF22		
L5	DDR_DCF23	VDD_DDR_VDDQ	DDR		DRC.DCF23		
H4	DDR_DCF24	VDD_DDR_VDDQ	DDR		DRC.DCF24		
H10	DDR_DCF25	VDD_DDR_VDDQ	DDR		DRC.DCF25		
A9	DDR_DCF26	VDD_DDR_VDDQ	DDR		DRC.DCF26		
E9	DDR_DCF27	VDD_DDR_VDDQ	DDR		DRC.DCF27		
D10	DDR_DCF28	VDD_DDR_VDDQ	DDR		DRC.DCF28		
D8	DDR_DCF29	VDD_DDR_VDDQ	DDR		DRC.DCF29		
H8	DDR_DCF30	VDD_DDR_VDDQ	DDR		DRC.DCF30		
G9	DDR_DCF31	VDD_DDR_VDDQ	DDR		DRC.DCF31		
E7	DDR_DCF32	VDD_DDR_VDDQ	DDR		DRC.DCF32		
G7	DDR_DCF33	VDD_DDR_VDDQ	DDR		DRC.DCF33		
W1	DDR_DM0	VDD_DDR_VDDQ	DDR		DRC.DM0		
T6	DDR_DM1	VDD_DDR_VDDQ	DDR		DRC.DM1		
N3	DDR_DQ00	VDD_DDR_VDDQ	DDR		DRC.DQ00		
P2	DDR_DQ01	VDD_DDR_VDDQ	DDR		DRC.DQ01		

Table 128. 17 x 17 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
N1	DDR_DQ02	VDD_DDR_VDDQ	DDR		DRC.DQ02		
T2	DDR_DQ03	VDD_DDR_VDDQ	DDR		DRC.DQ03		
Y2	DDR_DQ04	VDD_DDR_VDDQ	DDR		DRC.DQ04		
AB2	DDR_DQ05	VDD_DDR_VDDQ	DDR		DRC.DQ05		
AC1	DDR_DQ06	VDD_DDR_VDDQ	DDR		DRC.DQ06		
AC3	DDR_DQ07	VDD_DDR_VDDQ	DDR		DRC.DQ07		
Y4	DDR_DQ08	VDD_DDR_VDDQ	DDR		DRC.DQ08		
AC5	DDR_DQ09	VDD_DDR_VDDQ	DDR		DRC.DQ09		
W3	DDR_DQ10	VDD_DDR_VDDQ	DDR		DRC.DQ10		
AB4	DDR_DQ11	VDD_DDR_VDDQ	DDR		DRC.DQ11		
P4	DDR_DQ12	VDD_DDR_VDDQ	DDR		DRC.DQ12		
N5	DDR_DQ13	VDD_DDR_VDDQ	DDR		DRC.DQ13		
P6	DDR_DQ14	VDD_DDR_VDDQ	DDR		DRC.DQ14		
N7	DDR_DQ15	VDD_DDR_VDDQ	DDR		DRC.DQ15		
U1	DDR_DQS0_N	VDD_DDR_VDDQ	DDR		DRC.DQS0_N		
U3	DDR_DQS0_P	VDD_DDR_VDDQ	DDR		DRC.DQS0_P		
T4	DDR_DQS1_N	VDD_DDR_VDDQ	DDR		DRC.DQS1_N		
U5	DDR_DQS1_P	VDD_DDR_VDDQ	DDR		DRC.DQS1_P		
U7	DDR_DTO0	VDD_DDR_VDDQ	DDR		DRC.DTO0		
AB6	DDR_DTO1	VDD_DDR_VDDQ	DDR		DRC.DTO1		
Y6	DDR_VREF	VDD_DDR_VDDQ	DDR		DRC.VREF0		
F10	DDR_ZQ	VDD_DDR_VDDQ	DDR		DRC.ZQ		
F14	EMMC0_CLK	VDD_EMMC0_1P8_3P3	FASTD	ALT4	LSIO.GPIO4.IO07	INPUT	PD(50K)
E13	EMMC0_CMD	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.CMD	INPUT	PD(50K)
A21	EMMC0_DATA0	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA0	INPUT	PD(50K)
F18	EMMC0_DATA1	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA1	INPUT	PD(50K)
G15	EMMC0_DATA2	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA2	INPUT	PD(50K)
E19	EMMC0_DATA3	VDD_EMMC0_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA3	INPUT	PD(50K)
G17	EMMC0_DATA4	VDD_EMMC0_VSELECT_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA4	INPUT	PD(50K)
F16	EMMC0_DATA5	VDD_EMMC0_VSELECT_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA5	INPUT	PD(50K)
E15	EMMC0_DATA6	VDD_EMMC0_VSELECT_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA6	INPUT	PD(50K)
H16	EMMC0_DATA7	VDD_EMMC0_VSELECT_1P8_3P3	FASTD	ALT0	CONN.EMMC0.DATA7	INPUT	PD(50K)
B20	EMMC0_RESET_B	VDD_EMMC0_VSELECT_1P8_3P3	GPIO	ALT4	LSIO.GPIO4.IO18	INPUT	PU(50K)

Table 128. 17 x 17 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
J17	EMMC0_STROBE	VDD_EMMC0_VSELECT_1P8_3P3	FASTD	ALT0	CONN.EMMC0.STROBE	INPUT	PD(50K)
A25	ENET0_MDC	VDD_ENET_MDIO_1P8_3P3	GPIO	ALT4	LSIO.GPIO5.IO11	INPUT	PD(50K)
J21	ENET0_MDIO	VDD_ENET_MDIO_1P8_3P3	GPIO	ALT0	CONN.ENET0.MDIO	INPUT	PU(50K)
F22	ENET0_REFCLK_125M_25M	VDD_ENET_MDIO_1P8_3P3	GPIO	ALT4	LSIO.GPIO5.IO09	INPUT	PD(50K)
H20	ENET0_RGMII_RX_CTL	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RX_CTL	INPUT	PD(50K)
A23	ENET0_RGMII_RXC	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXC	INPUT	PD(50K)
C23	ENET0_RGMII_RXD0	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD0	INPUT	PD(50K)
D22	ENET0_RGMII_RXD1	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD1	INPUT	PD(50K)
G21	ENET0_RGMII_RXD2	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD2	INPUT	PD(50K)
B24	ENET0_RGMII_RXD3	VDD_ENET0_1P8_2P5_3P3	FASTD	ALT0	CONN.ENET0.RGMII_RXD3	INPUT	PD(50K)
H18	ENET0_RGMII_TX_CTL	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO4.IO30	INPUT	PD(50K)
G19	ENET0_RGMII_TXC	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO4.IO29	INPUT	PD(50K)
F20	ENET0_RGMII_TXD0	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO4.IO31	INPUT	PD(50K)
C21	ENET0_RGMII_TXD1	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO5.IO00	INPUT	PD(50K)
J19	ENET0_RGMII_TXD2	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO5.IO01	INPUT	PD(50K)
B22	ENET0_RGMII_TXD3	VDD_ENET0_VSELECT_1P8_2P5_3P3	FASTD	ALT4	LSIO.GPIO5.IO02	INPUT	PD(50K)
B26	ESAI0_FSR	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.FSR	INPUT	PD(50K)
E23	ESAI0_FST	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.FST	INPUT	PD(50K)
H22	ESAI0_SCKR	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.SCKR	INPUT	PD(50K)
C25	ESAI0_SCKT	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.SCKT	INPUT	PD(50K)
G23	ESAI0_TX0	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX0	INPUT	PD(50K)
E25	ESAI0_TX1	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX1	INPUT	PD(50K)
C27	ESAI0_TX2_RX3	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX2_RX3	INPUT	PD(50K)
D24	ESAI0_TX3_RX2	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX3_RX2	INPUT	PD(50K)
B28	ESAI0_TX4_RX1	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX4_RX1	INPUT	PD(50K)
K22	ESAI0_TX5_RX0	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.ESAI0.TX5_RX0	INPUT	PD(50K)
T22	FLEXCAN0_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.FLEXCAN0.RX	INPUT	PD(50K)
U25	FLEXCAN0_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO16	INPUT	PD(50K)
T24	FLEXCAN1_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.FLEXCAN1.RX	INPUT	PD(50K)

Table 128. 17 x 17 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
U29	FLEXCAN1_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO18	INPUT	PD(50K)
T28	FLEXCAN2_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.FLEXCAN2.RX	INPUT	PD(50K)
U27	FLEXCAN2_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO20	INPUT	PD(50K)
AA29	JTAG_TCK	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TCK	INPUT	PD(50K)
AC29	JTAG_TDI	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TDI	INPUT	PU(50K)
Y24	JTAG_TDO	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TDO	OUTPUT	HiZ
W23	JTAG_TMS	VDD_ANA1_1P8	TEST	ALT0	SCU.JTAG.TMS	INPUT	PU(50K)
L23	MCLK_IN0	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.ACM.MCLK_IN0	INPUT	PD(50K)
M22	MCLK_IN1	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.ACM.MCLK_IN1	INPUT	PD(50K)
K24	MCLK_OUT0	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO0.IO20	INPUT	PD(50K)
AC15	MIPI_CSI0_CLK_N	VDD_MIPI_CSI0_1P8	CSI		MIPI_CSI0.CKN		
AD16	MIPI_CSI0_CLK_P	VDD_MIPI_CSI0_1P8	CSI		MIPI_CSI0.CKP		
AC17	MIPI_CSI0_DATA0_N	VDD_MIPI_CSI0_1P8	CSI		MIPI_CSI0.DN0		
AD18	MIPI_CSI0_DATA0_P	VDD_MIPI_CSI0_1P8	CSI		MIPI_CSI0.DP0		
AC13	MIPI_CSI0_DATA1_N	VDD_MIPI_CSI0_1P8	CSI		MIPI_CSI0.DN1		
AD14	MIPI_CSI0_DATA1_P	VDD_MIPI_CSI0_1P8	CSI		MIPI_CSI0.DP1		
AC19	MIPI_CSI0_DATA2_N	VDD_MIPI_CSI0_1P8	CSI		MIPI_CSI0.DN2		
AD20	MIPI_CSI0_DATA2_P	VDD_MIPI_CSI0_1P8	CSI		MIPI_CSI0.DP2		
AC11	MIPI_CSI0_DATA3_N	VDD_MIPI_CSI0_1P8	CSI		MIPI_CSI0.DN3		
AD12	MIPI_CSI0_DATA3_P	VDD_MIPI_CSI0_1P8	CSI		MIPI_CSI0.DP3		
AF18	MIPI_CSI0_MCLK_OUT	VDD_MIPI_CSI_DIG_1P8	GPIO	ALT4	LSIO.GPIO3.IO04	INPUT	PD(50K)
AF14	MIPI_DSI0_CLK_N	VDD_MIPI_DSI0_1P8	DSI		MIPI_DSI0.CKN		
AH14	MIPI_DSI0_CLK_P	VDD_MIPI_DSI0_1P8	DSI		MIPI_DSI0.CKP		
AG15	MIPI_DSI0_DATA0_N	VDD_MIPI_DSI0_1P8	DSI		MIPI_DSI0.DN0		
AJ15	MIPI_DSI0_DATA0_P	VDD_MIPI_DSI0_1P8	DSI		MIPI_DSI0.DP0		
AG13	MIPI_DSI0_DATA1_N	VDD_MIPI_DSI0_1P8	DSI		MIPI_DSI0.DN1		
AJ13	MIPI_DSI0_DATA1_P	VDD_MIPI_DSI0_1P8	DSI		MIPI_DSI0.DP1		
AF16	MIPI_DSI0_DATA2_N	VDD_MIPI_DSI0_1P8	DSI		MIPI_DSI0.DN2		
AH16	MIPI_DSI0_DATA2_P	VDD_MIPI_DSI0_1P8	DSI		MIPI_DSI0.DP2		
AF12	MIPI_DSI0_DATA3_N	VDD_MIPI_DSI0_1P8	DSI		MIPI_DSI0.DN3		
AH12	MIPI_DSI0_DATA3_P	VDD_MIPI_DSI0_1P8	DSI		MIPI_DSI0.DP3		
W27	MIPI_DSI0_I2C0_SCL	VDD_CAN_UART_1P8_3P3[3]	GPIO	ALT0	MIPI_DSI0.I2C0.SCL	INPUT	PU(50K)
V22	MIPI_DSI0_I2C0_SDA	VDD_CAN_UART_1P8_3P3[3]	GPIO	ALT0	MIPI_DSI0.I2C0.SDA	INPUT	PU(50K)

Table 128. 17 x 17 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
AG9	MIPI_DSI1_CLK_N	VDD_MIPI_DSI1_1P8	DSI		MIPI_DSI1.CKN		
AJ9	MIPI_DSI1_CLK_P	VDD_MIPI_DSI1_1P8	DSI		MIPI_DSI1.CKP		
AF8	MIPI_DSI1_DATA0_N	VDD_MIPI_DSI1_1P8	DSI		MIPI_DSI1.DN0		
AH8	MIPI_DSI1_DATA0_P	VDD_MIPI_DSI1_1P8	DSI		MIPI_DSI1.DP0		
AF10	MIPI_DSI1_DATA1_N	VDD_MIPI_DSI1_1P8	DSI		MIPI_DSI1.DN1		
AH10	MIPI_DSI1_DATA1_P	VDD_MIPI_DSI1_1P8	DSI		MIPI_DSI1.DP1		
AG7	MIPI_DSI1_DATA2_N	VDD_MIPI_DSI1_1P8	DSI		MIPI_DSI1.DN2		
AJ7	MIPI_DSI1_DATA2_P	VDD_MIPI_DSI1_1P8	DSI		MIPI_DSI1.DP2		
AG11	MIPI_DSI1_DATA3_N	VDD_MIPI_DSI1_1P8	DSI		MIPI_DSI1.DN3		
AJ11	MIPI_DSI1_DATA3_P	VDD_MIPI_DSI1_1P8	DSI		MIPI_DSI1.DP3		
Y28	MIPI_DSI1_I2C0_SCL	VDD_CAN_UART_1P8_3P3[3]	GPIO	ALT0	MIPI_DSI1.I2C0.SCL	INPUT	PU(50K)
W25	MIPI_DSI1_I2C0_SDA	VDD_CAN_UART_1P8_3P3[3]	GPIO	ALT0	MIPI_DSI1.I2C0.SDA	INPUT	PU(50K)
AJ25	ON_OFF_BUTTON	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.ON_OFF_BUTTON		
E11	PCIE_CTRL0_CLKREQ_B	VDD_PCIE_DIG_1P8_3P3	GPIO	ALT0	HSIO.PCIE0.CLKREQ_B	INPUT	PD(50K)
A11	PCIE_CTRL0_PERST_B	VDD_PCIE_DIG_1P8_3P3	GPIO	ALT0	HSIO.PCIE0.PERST_B	INPUT	PD(50K)
B14	PCIE_CTRL0_WAKE_B	VDD_PCIE_DIG_1P8_3P3	GPIO	ALT0	HSIO.PCIE0.WAKE_B	INPUT	PU(50K)
F12	PCIE_REF_QR	VDD_PCIE_1P8	PCIE		HSIO.PCIE_IOB.REF_QR		
C13	PCIE_REFCLK100M_N	VDD_PCIE_1P8	PCIE		HSIO.PCIE_IOB.EXT_REFCLK100M_N		
D14	PCIE_REFCLK100M_P	VDD_PCIE_1P8	PCIE		HSIO.PCIE_IOB.EXT_REFCLK100M_P		
H12	PCIE_REXT	VDD_PCIE0_1P0	PCIE		HSIO.PCIE.REXT		
G11	PCIE0_PHY_PLL_REF_RETURN	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.PLL_REF_RETURN		
B16	PCIE0_RX0_N	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.RX0_N		
A15	PCIE0_RX0_P	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.RX0_P		
B12	PCIE0_TX0_N	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.TX0_N		
A13	PCIE0_TX0_P	VDD_PCIE_LDO_1P0_CAP	PCIE		HSIO.PCIE0.TX0_P		
AC27	PMIC_I2C_SCL	VDD_ANA1_1P8	SCU	ALT0	SCU.PMIC_I2C.SCL	INPUT	PU(50K)
AE29	PMIC_I2C_SDA	VDD_ANA1_1P8	SCU	ALT0	SCU.PMIC_I2C.SDA	INPUT	PU(50K)
AA23	PMIC_INT_B	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.PMIC_INT_B	INPUT	PU(50K)
AB20	PMIC_ON_REQ	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.PMIC_ON_REQ		
AD28	POR_B	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.POR_B	INPUT	PU(50K)
AJ5	QSPI0A_DATA0	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA0	INPUT	PD(50K)

Table 128. 17 x 17 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
AH4	QSPI0A_DATA1	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA1	INPUT	PD(50K)
AC9	QSPI0A_DATA2	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA2	INPUT	PD(50K)
AG5	QSPI0A_DATA3	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DATA3	INPUT	PD(50K)
AB10	QSPI0A_DQS	VDD_QSPI0A_1P8_3P3	FASTD	ALT0	LSIO.QSPI0A.DQS	INPUT	PD(50K)
AG3	QSPI0A_SCLK	VDD_QSPI0A_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO16	INPUT	PD(50K)
AB12	QSPI0A_SS0_B	VDD_QSPI0A_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO14	INPUT	PU(50K)
AD10	QSPI0A_SS1_B	VDD_QSPI0A_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO15	INPUT	PU(50K)
AC7	QSPI0B_DATA0	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA0	INPUT	PD(50K)
AE1	QSPI0B_DATA1	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA1	INPUT	PD(50K)
AF2	QSPI0B_DATA2	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA2	INPUT	PD(50K)
AE3	QSPI0B_DATA3	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DATA3	INPUT	PD(50K)
AF4	QSPI0B_DQS	VDD_QSPI0B_1P8_3P3	FASTD	ALT0	LSIO.QSPI0B.DQS	INPUT	PD(50K)
AH2	QSPI0B_SCLK	VDD_QSPI0B_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO17	INPUT	PD(50K)
AE7	QSPI0B_SS0_B	VDD_QSPI0B_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO23	INPUT	PU(50K)
AF6	QSPI0B_SS1_B	VDD_QSPI0B_1P8_3P3	FASTD	ALT4	LSIO.GPIO3.IO24	INPUT	PU(50K)
AH26	RTC_XTALI	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.RTC_XTALI		
AF26	RTC_XTALO	VDD_SNVS_LDO_1P8_CAP	ANA		SNVS.RTC_XTALO		
AD26	SCU_BOOT_MODE0	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.BOOT_MODE0	INPUT	PD(50K)
AC23	SCU_BOOT_MODE1	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.BOOT_MODE1	INPUT	PD(50K)
AE25	SCU_BOOT_MODE2	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.BOOT_MODE2	INPUT	PD(50K)
AB22	SCU_BOOT_MODE3	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.BOOT_MODE3	INPUT	PD(50K)
Y22	SCU_GPIO0_00	VDD_ANA1_1P8	GPIO	ALT0	SCU.GPIO0.IO00	INPUT	PD(50K)
AC25	SCU_GPIO0_01	VDD_ANA1_1P8	GPIO	ALT0	SCU.GPIO0.IO01	INPUT	PU(50K)
AB24	SCU_PMIC_STANDBY	VDD_ANA1_1P8	SCU	ALT0	SCU.DSC.PMIC_STANDBY	OUTPUT	Drive 0
AB28	SCU_WDOG_OUT[4]	VDD_ANA1_1P8	SCU	ALT1	SCU.WDOG0.WDOG_OUT	OUTPUT	PD(50K)
E27	SPDIF0_EXT_CLK	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.SPDIF0.EXT_CLK	INPUT	PD(50K)
F24	SPDIF0_RX	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT0	ADMA.SPDIF0.RX	INPUT	PD(50K)
J23	SPDIF0_TX	VDD_ESAI_SPDIF_1P8_2P5_3P3	GPIO	ALT4	LSIO.GPIO0.IO11	INPUT	PD(50K)
H28	SPI0_CS0	VDD_SPI_MCLK_UART_1P8_3P3[3]	GPIO	ALT0	ADMA.SPI0.CS0	INPUT	PD(50K)
K28	SPI0_CS1	VDD_SPI_MCLK_UART_1P8_3P3[3]	GPIO	ALT0	ADMA.SPI0.CS1	INPUT	PD(50K)
L25	SPI0_SCK	VDD_SPI_MCLK_UART_1P8_3P3[3]	GPIO	ALT0	ADMA.SPI0.SCK	INPUT	PD(50K)
J29	SPI0_SDI	VDD_SPI_MCLK_UART_1P8_3P3[3]	GPIO	ALT0	ADMA.SPI0.SDI	INPUT	PD(50K)
J27	SPI0_SDO	VDD_SPI_MCLK_UART_1P8_3P3[3]	GPIO	ALT4	LSIO.GPIO1.IO06	INPUT	PD(50K)

Table 128. 17 x 17 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition[2]			
				Default Mode	Default Function	Default Direction	Default Pull
D26	SPI3_CS0	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.CS0	INPUT	PD(50K)
F28	SPI3_CS1	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.CS1	INPUT	PD(50K)
D28	SPI3_SCK	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.SCK	INPUT	PD(50K)
H24	SPI3_SDI	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.SPI3.SDI	INPUT	PD(50K)
G25	SPI3_SDO	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO0.IO14	INPUT	PD(50K)
AA25	TEST_MODE_SELECT	VDD_ANA1_1P8	SCU	ALT0	SCU.TCU.TEST_MODE_SELECT	INPUT	PD(50K)
V28	UART0_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.UART0.RX	INPUT	PD(50K)
U23	UART0_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO22	INPUT	PD(50K)
G27	UART1_CTS_B	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.UART1.CTS_B	INPUT	PD(50K)
G29	UART1_RTS_B	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPT0.CLK	INPUT	PD(50K)
E29	UART1_RX	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT0	ADMA.UART1.RX	INPUT	PD(50K)
J25	UART1_TX	VDD_SPI_MCLK_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO0.IO21	INPUT	PD(50K)
W29	UART2_RX	VDD_CAN_UART_1P8_3P3	GPIO	ALT0	ADMA.UART2.RX	INPUT	PD(50K)
V26	UART2_TX	VDD_CAN_UART_1P8_3P3	GPIO	ALT4	LSIO.GPIO1.IO23	INPUT	PD(50K)
B18	USB_OTG1_DN	VDD_USB_3P3	OTG		CONN.USB_OTG1.DN		
A19	USB_OTG1_DP	VDD_USB_3P3	OTG		CONN.USB_OTG1.DP		
A17	USB_OTG1_ID	VDD_USB_3P3	OTG		CONN.USB_OTG1.ID		
J15	USB_OTG1_VBUS	OTG		CONN.USB_OTG1.VBUS			
G13	USB_SS3_TC1	VDD_USB_3P3	GPIO	ALT0	ADMA.I2C1.SCL	INPUT	PD(50K)
H14	USB_SS3_TC3	VDD_USB_3P3	GPIO	ALT0	ADMA.I2C1.SDA	INPUT	PU(50K)
AH28	XTALI	VDD_ANA1_1P8	ANA		SCU.DSC.XTALI		
AF28	XTALO	VDD_ANA1_1P8	ANA		SCU.DSC.XTALO		

1 FASTD are GPIO balls configured for high speed operation using the FASTRZ control.

2 Reset condition shown is before boot code execution. For pad changes after boot code execution, see the System Boot chapter of the device reference manual.

3 Power domain and associated IO grouping differs from 21 x 21 package.

4 SCU_WDOG_OUT was previously named JTAG_TRST_B; it has been renamed because its functionality has changed.

The following table shows the DDR 17 x 17 mm pin function.

Table 129. i.MX 8QXP 17 x 17 mm DRAM pin function

Ball Name	Ball	LPDDR4 function	DDR3L function
DDR_ATO	W5	DDR_ATO	DDR_ATO
DDR_CK0_N	G3	DDR_CK0_N	DDR_CK0_N
DDR_CK0_P	H2	DDR_CK0_P	DDR_CK0_P
DDR_CK1_N	B8	DDR_CK1_N	DDR_CK1_N
DDR_CK1_P	A7	DDR_CK1_P	DDR_CK1_P
DDR_DCF00	G5	CA2_A	A5
DDR_DCF01	B2	CA4_A	A6
DDR_DCF03	E3	CA5_A	A7
DDR_DCF04	K6	/	A8
DDR_DCF05	D4	/	A9
DDR_DCF07	B4	/	RAS#
DDR_DCF08	K2	CA3_A	A3
DDR_DCF09	L3	ODT_CA_A	ODT
DDR_DCF10	G1	CS0_A	A1
DDR_DCF11	L1	CA0_A	A0
DDR_DCF12	D2	CS1_A	A2
DDR_DCF14	K4	CKE0_A	/
DDR_DCF15	E1	CKE1_A	/
DDR_DCF16	L7	CA1_A	A4
DDR_DCF17	B6	CA4_B	A12
DDR_DCF18	A5	RESET_N	RESET_N
DDR_DCF19	H6	CA5_B	A14
DDR_DCF20	D6	/	A15
DDR_DCF21	B10	/	BA0
DDR_DCF22	E5	/	BA1
DDR_DCF23	L5	/	BA2
DDR_DCF24	H4	/	CAS#
DDR_DCF25	H10	ODT_CA_B	ODT1
DDR_DCF26	A9	CA3_B	A13
DDR_DCF27	E9	CA0_B	A10
DDR_DCF28	D10	CS0_B	CS_N[0]

Table 129. i.MX 8QXP 17 x 17 mm DRAM pin function (continued)

Ball Name	Ball	LPDDR4 function	DDR3L function
DDR_DCF29	D8	CS1_B	CS_N[1]
DDR_DCF30	H8	CKE0_B	CKE0
DDR_DCF31	G9	CKE1_B	CKE1
DDR_DCF32	E7	CA1_B	A11
DDR_DCF33	G7	CA2_B	WE#
DDR_DM0	W1	DDR_DMI0	DDR_DMI0
DDR_DM1	T6	DDR_DMI1	DDR_DMI1
DDR_DQ00	N3	DDR_DQ00	DDR_DQ00
DDR_DQ01	P2	DDR_DQ01	DDR_DQ01
DDR_DQ02	N1	DDR_DQ02	DDR_DQ02
DDR_DQ03	T2	DDR_DQ03	DDR_DQ03
DDR_DQ04	Y2	DDR_DQ04	DDR_DQ04
DDR_DQ05	AB2	DDR_DQ05	DDR_DQ05
DDR_DQ06	AC1	DDR_DQ06	DDR_DQ06
DDR_DQ07	AC3	DDR_DQ07	DDR_DQ07
DDR_DQ08	Y4	DDR_DQ08	DDR_DQ08
DDR_DQ09	AC5	DDR_DQ09	DDR_DQ09
DDR_DQ10	W3	DDR_DQ10	DDR_DQ10
DDR_DQ11	AB4	DDR_DQ11	DDR_DQ11
DDR_DQ12	P4	DDR_DQ12	DDR_DQ12
DDR_DQ13	N5	DDR_DQ13	DDR_DQ13
DDR_DQ14	P6	DDR_DQ14	DDR_DQ14
DDR_DQ15	N7	DDR_DQ15	DDR_DQ15
DDR_DQS0_N	U1	DDR_DQS0_N	DDR_DQS0_N
DDR_DQS0_P	U3	DDR_DQS0_P	DDR_DQS0_P
DDR_DQS1_N	T4	DDR_DQS1_N	DDR_DQS1_N
DDR_DQS1_P	U5	DDR_DQS1_P	DDR_DQS1_P
DDR_DTO0	U7	DDR_DTO0	DDR_DTO0
DDR_DTO1	AB6	DDR_DTO1	DDR_DTO1

7 Release Notes

This table provides release notes for the data sheet.

Table 130. Data sheet release notes

Rev. Number	Date	Substantive Change(s)
2	02/2020	• Updated Table 1, "i.MX 8QuadXPlus/8DualXPlus advanced features" • Updated Table 2, "i.MX 8QuadXPlus Orderable part numbers" and Table 3, "i.MX 8DualXPlus Orderable part numbers" • Updated Section 1.2, “System Controller Firmware (SCFW) Requirements" • Added note to Table 4, "Feature differences per package" • Updated Table 6, "i.MX 8QuadXPlus/8DualXPlus modules list" • In Table 8, "Absolute maximum ratings" updated storage temperature range • In Table 10, "Operating ranges" updated VDD_TMPR_CSI_1P8_3P3 information • Updated Table 13, "i.MX 8QuadXPlus/8DualXPlus Key State (KSx) power consumption" • Updated note in Section 4.2.2, “Power-down sequence" • Updated footnote and Group 2 in Table 17, "Power supplies usage" • Updated pull-up and pull-down resistance numbers in Table 40, "Tri-voltage 1.8 V GPIO output impedance DC parameters" • Updated pull-up and pull-down resistance numbers in Table 43, "Dual-voltage 1.8 V GPIO output impedance DC parameters" • Updated Section 4.7.2, “DDR I/O output buffer impedance" • Added footnote to Table 120, "ADC electrical specifications (VREFH=VDD_ADC_1P8)" • Updated Table 99, "FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x0 (DDR mode)" • Updated Table 100, "FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x1 (DDR mode)" • Updated Figure 58, "21 x 21 mm Package Top, Bottom, and Side Views," and Table 59, "Notes on 21 x 21 mm Package Top, Bottom, and Side Views" • Updated and added footnotes to Table 125, "21 x 21 mm functional contact assignments" • Updated Figure 60, "17 x 17 mm Package Top, Bottom, and Side Views," and Figure 61, "Notes on 17 x 17 mm Package Top, Bottom, and Side Views," • Added footnotes to Table 128, "17 x 17 mm functional contact assignments"

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