Integrated Class D Amplifier

Features


7x7mm PQFN42L

- 2 channel integrated analog input Class D audio amplifier in a small package
- No mechanical heatsink required
- High peak music power output
- Split or single power supply
- Differential or single-ended input
- Over-current, over-temperature and under voltage protections with self-reset feature
- Start/stop click noise reduction
- Clip and Fault reporting outputs
- High noise immunity

RoHS

Potential applications

- Home theatre systems
- Docking station audio systems
- PC audio systems
- Musical instruments
- Karaoke amplifiers
- Game consoles
- Powered speaker systems
- General purpose audio power amplifiers

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Product type	Package
MA5332	7x7mm PQFN42

Description

The MA5332M integrates 2 channel PWM controller and digital audio MOSFETs forming a high performance Class D audio amplifier. As a result of fully optimized MOSFETs co-packed with a dedicated controller IC, the MA5332M operates without mechanical heatsink attached in a typical music playback use case. High voltage ratings and noise immunity in the controller IC ensures reliable operation over various environmental conditions. A small 7x7 mm PQFN package enhances the benefit of smaller size of Class D topology. The MA5332M series is lead-free, and ROHS compliant.

Topology	Half bridge / Full bridge
MA5332 Output power (Typical, THD+N=10%)	150 W/ 2 Ω 200 W/ 4 Ω 160 W/ 6 Ω
*Residual noise (AES-17, IHF-A, typical)	250 µVrms
*THD+N (1kHz, 1W, 4 Ω, typical)	0.03 %

* In a typical application

Table of contents

Features 1
Potential applications 1
Product validation 1
Description 1
Table of contents 2
1 Typical connection diagrams 3
2 Qualification information 4
3 Absolute maximum ratings 5
4 Recommended operating conditions 7
5 Electrical characteristics 8
6 Functional block diagram 11
7 Input / Output pin equivalent circuit diagrams 12
8 Lead definitions 13
9 Lead assignments 14
10 Package details 15
11 Board mounting, part marking, and ordering information 18
Revision history 19

1 Typical connection diagrams

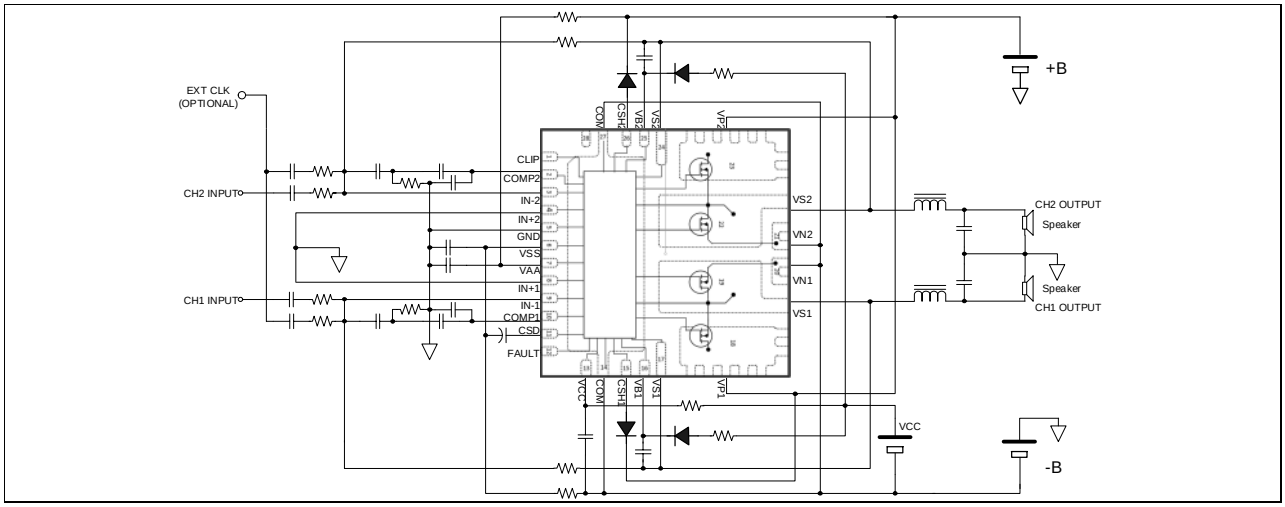


Figure 1 Inverting amplifier

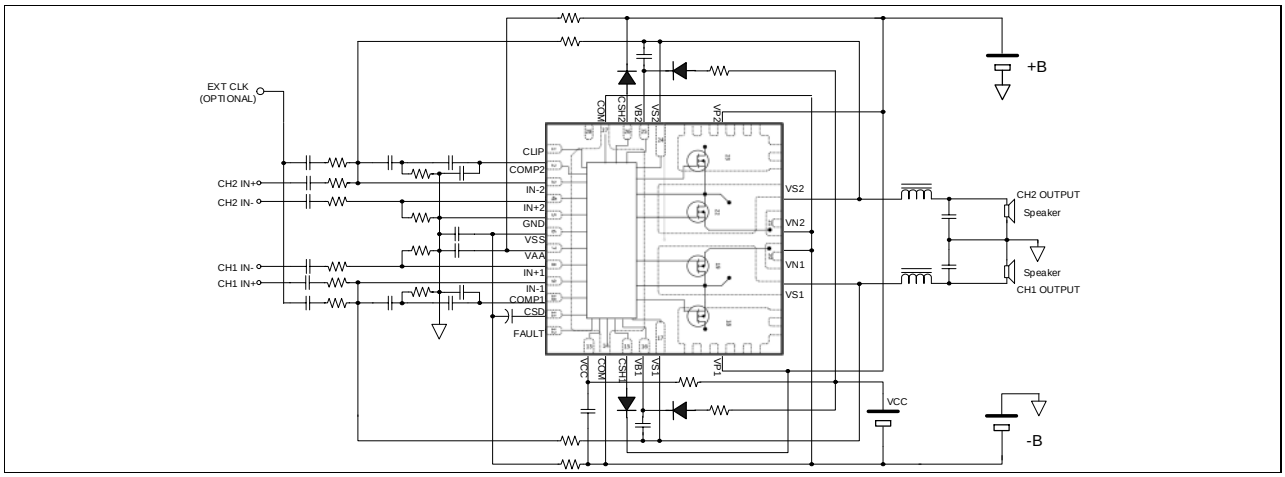


Figure 2 Differential amplifier

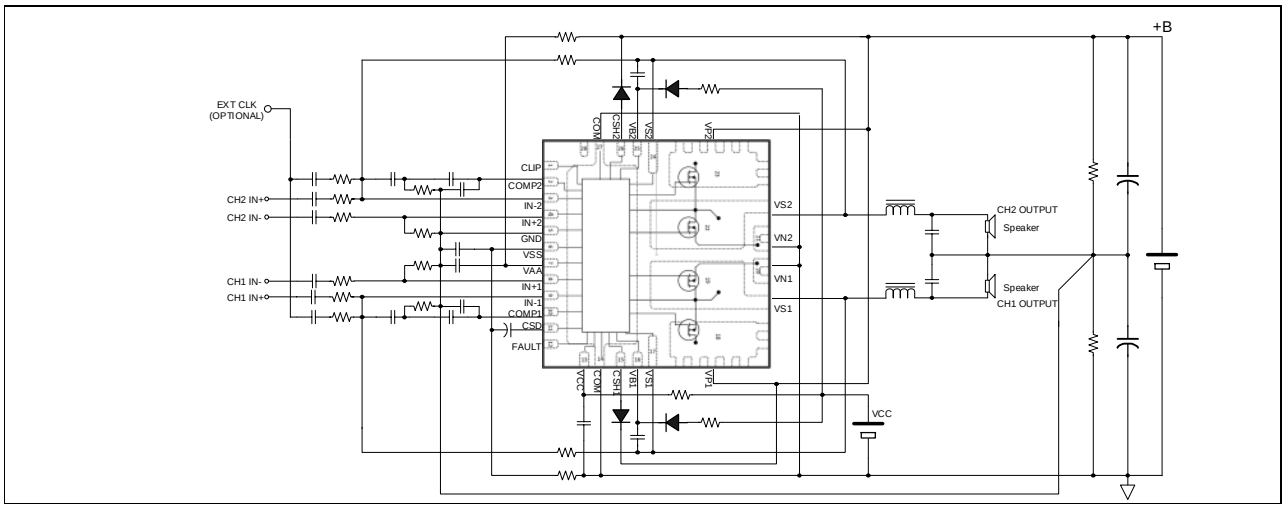


Figure 3 Single power supply (differential amplifier)

2 Qualification information

Qualification Level (1)		Industrial (**2**) Qualified for industrial applications according to the relevant tests of JEDEC47/20/22
Moisture Sensitivity Level (MSL) (3)		MSL3 (per IPC/JEDEC J-STD-020C)
ESD	**Charge Device Model**	Class 2 (per JEDEC standard JESD22-C101)
	Human Body Model	Class 1C (per EIA/JEDEC standard JESD22-A114)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

Note:

1. *Qualification standards can be found at Infineon's web site http://www.infineon.com/*
2. *Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.*
3. *Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.*

3 Absolute maximum ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM=VN1=VN2; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V_{Pn}	Positive power supply rail voltage, n=1-2	-	100	
V_{Bn}	High side floating supply voltage	-0.3	115	
V_{Sn}	High side floating supply voltage(2), n=1-2	V_{Bn} -15	V_{Bn} +0.3	
V_{CSHn}	CSH pin input voltage, n=1-2	V_{Sn} -0.3	V_{Bn} +0.3	
V_{CC}	Low side supply voltage(2)	-0.3	15	
V_{AA}	Floating input positive supply voltage(2)	-0.3	110	
V_{SS}	Floating input negative supply voltage(2)	-1 (See I_{SSZ})	GND +0.3	
V_{IN+n}	Floating input supply ground voltage , n=1-2	V_{SS} -0.3	V_{AA} +0.3	
I_{INn}	Input current between IN- and IN+ pins(1), n=1-2	-	±3	mA
V_{CSD}	CSD pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{COMPn}	COMP pin input voltage, n=1-2	V_{SS} -0.3	V_{AA} +0.3	
V_{CLIP}	CLIP pin input voltage	GND -0.3	V_{AA} +0.3	
I_{CLIP}	CLIP pin sinking current	-	5	mA
V_{FAULT}	FAULT pin input voltage	GND -0.3	V_{AA} +0.3	V
I_{FAULT}	FAULT pin sinking current	-	5	mA
I_{AAZ}	Floating input supply zener clamp current(2)	-	20	
I_{SSZ}	Floating input negative supply zener clamp current(2)	-	20	
I_{CCZ}	Low side supply zener clamp current(3)	-	20	
I_{BSZn}	Floating supply zener clamp current(3), n=1-2	-	20	
dV_{Sn}/dt	Allowable Vs voltage slew rate, n=1-2	-	50	V/ns
dV_{SS}/dt	Allowable Vss voltage slew rate(3)	-	50	V/ms
$Id_{@\ 25°C}$	Continuous output current, from VPn to VSn, VSn to VNn, V_{CC}=10V, V_{Bn}-V_{Sn}=10V	-	16	A
$Id_{@\ 100°C}$	Continuous output current, from VPn to VSn, VSn to VNn, V_{CC}=10V, V_{Bn}-V_{Sn}=10V	-	10	
I_{DM}	Pulsed output current, from VPn to VSn, VSn to VNn, V_{CC}=10V, V_{Bn}-V_{Sn}=10V(5)	-	64	
Pd	Power dissipation(4)@ T_C = 25°C	-	25	
Rth_{JC}	Thermal resistance, junction to case(4)	-	5	
T_{JIC}	Control IC junction temperature	-	150	°C
T_{JFET}	FET junction temperature	-	150	
T_S	Storage Temperature	-55	150	
T_L	Lead temperature (Soldering, 10 seconds)	-	300	

Absolute maximum ratings

Note:

1. *IN- and IN+ contain clamping diodes between the two pins.*
2. *V_{AA} -V_{SS}, Vcc-COM and VBn-VSn contain internal shunt zener diodes. Note that the voltage ratings of these can be limited by the clamping current.*
3. *For the rising and falling edges of step signal of 10V. Vss=15V to 200V.*
4. *Per MOSFET.*
5. *Repetitive rating, pulse width limited by maximum junction temperature.*

4 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions below. The Vss and Vsn offset ratings are tested with supplies biased at COM=VN1=VN2, V_{AA}-V_{SS}=9.6V, V_{CC}=12V and V_{Bn}-V_{Sn}=12V. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

Symbol	Definition		Min	Max	Units
V_{Pn}	Positive power supply voltage, n=1-2, without heatsink	MA5332M	-	60	
	Positive power supply voltage, n=1-2, with heatsink	MA5332M	-	80	V
V_{Bn}	High side floating supply absolute voltage, n=1-2		V_{Sn} +10	V_{Sn} +14	
V_{Sn}	High side floating supply offset voltage, n=1-2	MA5332M	(1)	100	
V_{AA}	Floating input positive supply voltage(2)		V_{SS} +9.0	V_{SS} + 9.8	
V_{SS}	Floating input negative supply voltage(2)	MA5332M	0	100	
I_{AAZ}	Floating input supply zener clamp current(2)		1	15	mA
I_{SSZ}	Floating input negative supply zener clamp current(2)		1	15	
V_{CC}	Low side fixed supply voltage		10	15	V
V_{IC}	IN- and IN+ pins common mode input voltage		V_{SS} + 2	V_{AA} - 2	
V_{IN-n}	Inverting input voltage, n=1-2		V_{IN+} -0.5	V_{IN+} +0.5	
V_{CSD}	CSD pin input voltage		V_{SS}	V_{AA}	
V_{COMPn}	COMP pin input voltage, n=1-2		V_{SS}	V_{AA}	
C_{COMPn}	COMP pin phase compensation capacitor to GND , n=1-2		1	-	nF
V_{CSHn}	CSH pin input voltage, n=1-2		V_{Sn}	V_{Bn}	V
dVss/dt	Allowable Vss voltage slew rate upon power-up(3)		-	50	V/ms
f_{SW}	Switching frequency		-	500	kHz
T_{J_IC}	Juction temperature of controller IC		-40	100	°C

Note:

1. *Logic operational for Vs equal to –5V to +100V. Logic state held for Vs equal to –5V to –V_{BS}.*
2. *GND input voltage is limited by I_{AAZ} and I_{SSZ}.*
3. *Vss ramps up from 0V to 90V.*

5 Electrical characteristics

Unless otherwise specified, the following apply:

- V_{CC},V_{BS}= 12 V
- V_{SS}=V_{S1}=V_{S2}=V_{N1}=V_{N2}=COM=0V
- V_{AA}=9.6V
- T_A=25°C

Table 1 Electrical characteristics

Symbol	Definition	Min	Typ	Max	Units	Test conditions
Low-side supply						
UV_{CC+}	Vcc supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	Vcc supply UVLO negative threshold	8.2	8.7	9.2	V	
UV_{CCHYS}	UV_{CC} hysteresis	-	0.2	-	V	
I_{QCC}	Low side quiescent current	-	-	3	mA	
I_{CC}	Low side supply current	-	10	-	mA	f=400kHz
V_{CLAMPL}n	Low side zener diode clamp voltage, n=1-2	14.7	15.3	16.2	V	I_{CC}=5mA
High-side floating supply						
UV_{BS+n}	High side well UVLO positive threshold, n=1-2	8.0	8.5	9.0	V	
UV_{BS-n}	High side well UVLO negative threshold, n=1-2	7.8	8.3	8.8	V	
UV_{BSHYSn}	UV_{BS} hysteresis, n=1-2	-	0.2	-	V	
I_{QBSn}	High side quiescent current, n=1-2	-	-	2.4	mA	
$I_{QBSn_OFF-CSH}$	High side quiescent current, with CSH pin open n=1-2	350	500	650	uA	
$V_{CLAMPHn}$	High side zener diode clamp voltage, n=1-2	14.7	15.3	16.2	V	I_{BS}=5mA
Floating input supply						
UV_{AA+}	VA+, VA- floating supply UVLO positive threshold from V_{SS}	8.2	8.7	9.2	V	V_{SS} =0V, GND pin floating
UV_{AA-}	VA+, VA- floating supply UVLO negative threshold from V_{SS}	7.7	8.2	8.7	V	V_{SS} =0V, GND pin floating
UV_{AAHYS}	UV_{AA} hysteresis	-	0.5	-	V	V_{SS} =0V, GND pin floating
I_{QAA0}	Floating Input positive quiescent supply current	-	1.5	3	mA	V_{AA}=9.6V, V_{SS} =0V, V_{CSD} =VSS
I_{QAA1}	Floating Input positive quiescent supply current	-	4	6	mA	V_{AA}=9.6V, V_{SS} =0V, V_{CSD} =VAA

Electrical characteristics

I_{QAA2}	Floating Input positive quiescent supply current	-	5	7.5	mA	V_{AA}=9.6V, V_{SS} =0V, V_{CSD} =GND
I_{LKM}	Floating input side to Low side leakage current	-	-	50	µA	V_{AA}=V_{SS}=V_{GND}= 100V
$V_{CLAMPM+}$	V_{AA} floating supply zener diode clamp voltage, positive, with respect to GND	4.9	5.1	5.4	V	I_{AA}=5mA, I_{SS}=5mA, V_{GND}=0V, V_{CSD} =VSS
$V_{CLAMPM-}$	V_{SS} floating supply zener diode clamp voltage, negative, with respect to GND	-5.4	-5.1	-4.9	V	I_{AA}=5mA, I_{SS}=5mA, V_{GND}=0V, V_{CSD} =VSS
Audio input (V_{GND}=0, V_{AA}=4.8V, V_{SS}=-4.8V)						
V_{OSn}	Input offset voltage, n=1-2	-18	0	18	mV	
I_{BINn}	Input bias current, n=1-2	-	-	40	nA	
GBWn	Small signal bandwidth in OTA, n=1-2	-	9	-	MHz	C_{COMP}=1nF, Rf=0
g_{mn}	OTA transconductance, n=1-2	-	10	-	mS	V_{IN+}=0V, V_{IN-} =10mV
G_{Vn}	OTA gain, n=1-2	50	-	-	dB	
V_{Nrmsn}	CHn OTA input noise voltage, n=1-2	-	200	330	mVrms	
PWM						
Vth_{PWM}	PWM comparator threshold in COMP	-	(V_{AA} - V_{SS})/2	-	V	
f_{OTAn}	COMP pin star-up local oscillation frequency, n=1-2	0.7	1.0	1.5	MHz	V_{CSD} =GND
Ton_n	COMP to VS rising edge propagation delay, n=1-2	-	370	-	ns	
Toff_n	COMP to VS trailing edge propagation delay, n=1-2	-	320	-	ns	
DTn	Deadtime: Low-side turn-off to High-side turn-on (DT_{LO-HO}) & High-side turn-off to Low-side turn-on (DT_{HO-LO}) , n=1-2	-	50	-	ns	VP=30V, VN=-30V,
Power MOSFET (FET1, FET2, FET3, FET4) (MA5332)						
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	100	-	-	V	V_{GS}=0V, I_D=250uA
$R_{DS(ON)}$	FET on resistance	-	24.4	30.5	mΩ	I_D=3.3A
Qg	Total gate charge	-	9.8	12.3	nC	V_{GS}=10V
I_{LK0}	VP leakage current, VS=VN	-	-	20	µA	V_P=100V, V_{CSD} =VSS
Protection						
I_{OCPn}	Over current detection Positive threshold, n=1-2	-	40	-	A	
I_{OCNn}	Over current detection Negative threshold, n=1-2	-	-40	-	A	

Electrical characteristics

Vth1	CSD pin shutdown release threshold	0.62xV_{AA}	0.70xV_{AA}	0.78xV_{AA}	V	
Vth2	CSD pin self-reset threshold	0.26xV_{AA}	0.30xV_{AA}	0.34xV_{AA}	V	
I_{CSD+}	CSD pin discharge current	70	100	130	µA	$V_{CSD} = V_{SS}$ +4.8V
I_{CSD-}	CSD pin charge current	70	100	130	µA	$V_{CSD} = V_{SS}$ +4.8V
t_{SDn}	Shutdown propagation delay from V_S < Vth1 to Shutdown, n=1-2	-	-	250	ns	COMP = V_{SS}
t_{OCPn}	CHn propagation delay time from $I_{On} > I_{OCPn}$ to Shutdown, n=1-2	-	-	500	ns	COMP = V_{SS}
t_{OCNn}	CHn propagation delay time from $I_{On} < I_{OCNn}$ to Shutdown, n=1-2	-	-	500	ns	COMP = V_{SS}
$Vth+_{CLIP}$	Clip detection positive threshold in COMP	0.85xV_{AA}	0.90xV_{AA}	0.95xV_{AA}	V	
$Vth-_{CLIP}$	Clip detection negative threshold in COMP	0.05xV_{AA}	0.10xV_{AA}	0.15xV_{AA}	V	
t_{CLIP}	Clipping detection propagation delay	-	40	-	ns	
$t_{CLIPmin}$	Clipping detection minimum output duration	-	3	-	us	
T_{SD}	Over temperature shutdown threshold in controller IC	100	-	-	°C	
T_{SDHYS}	Over temperature shutdown threshold hysteresis	-	7	-	°C	

6 Functional block diagram

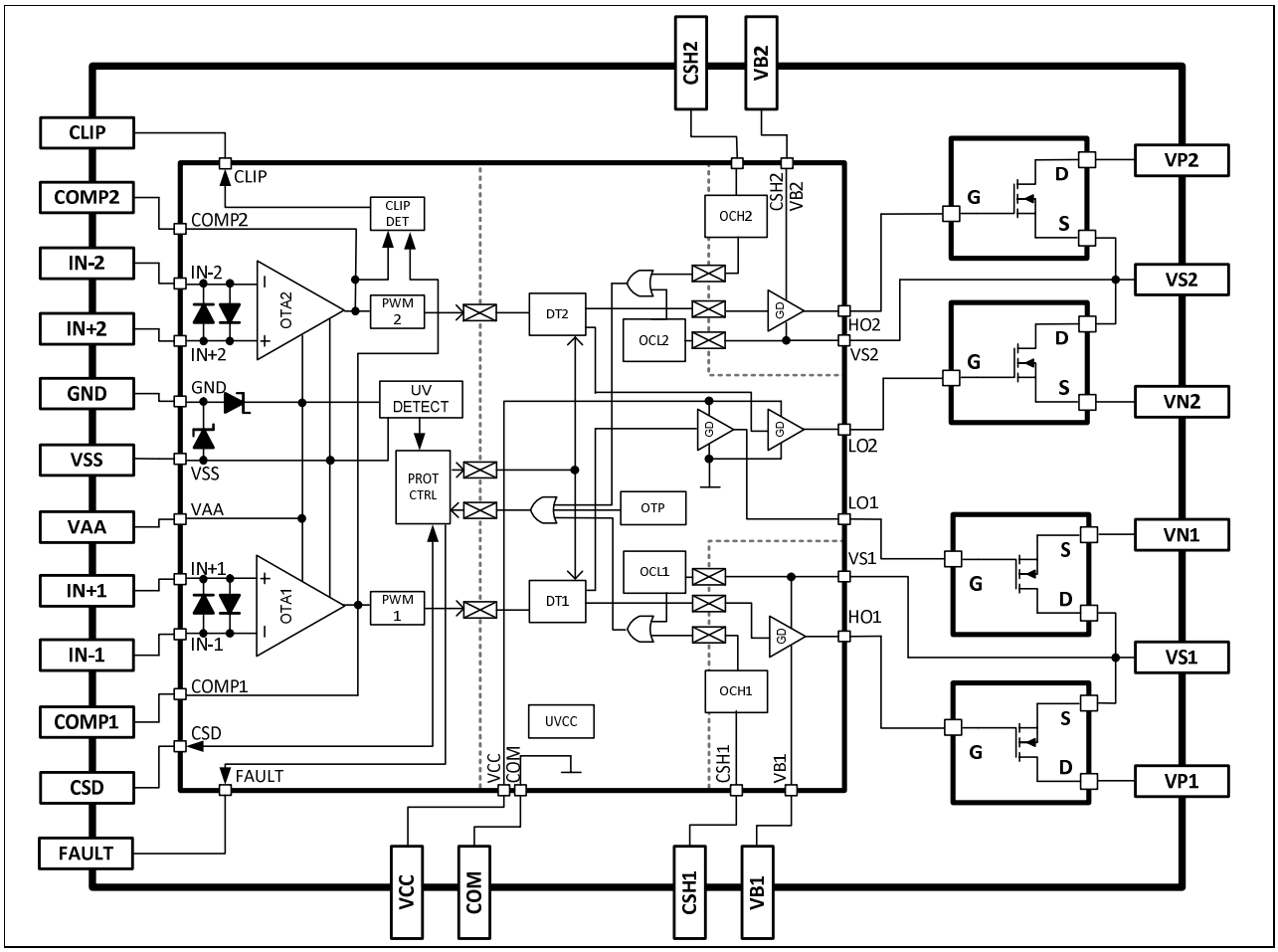


Figure 4 Block diagram

7 Input / Output pin equivalent circuit diagrams

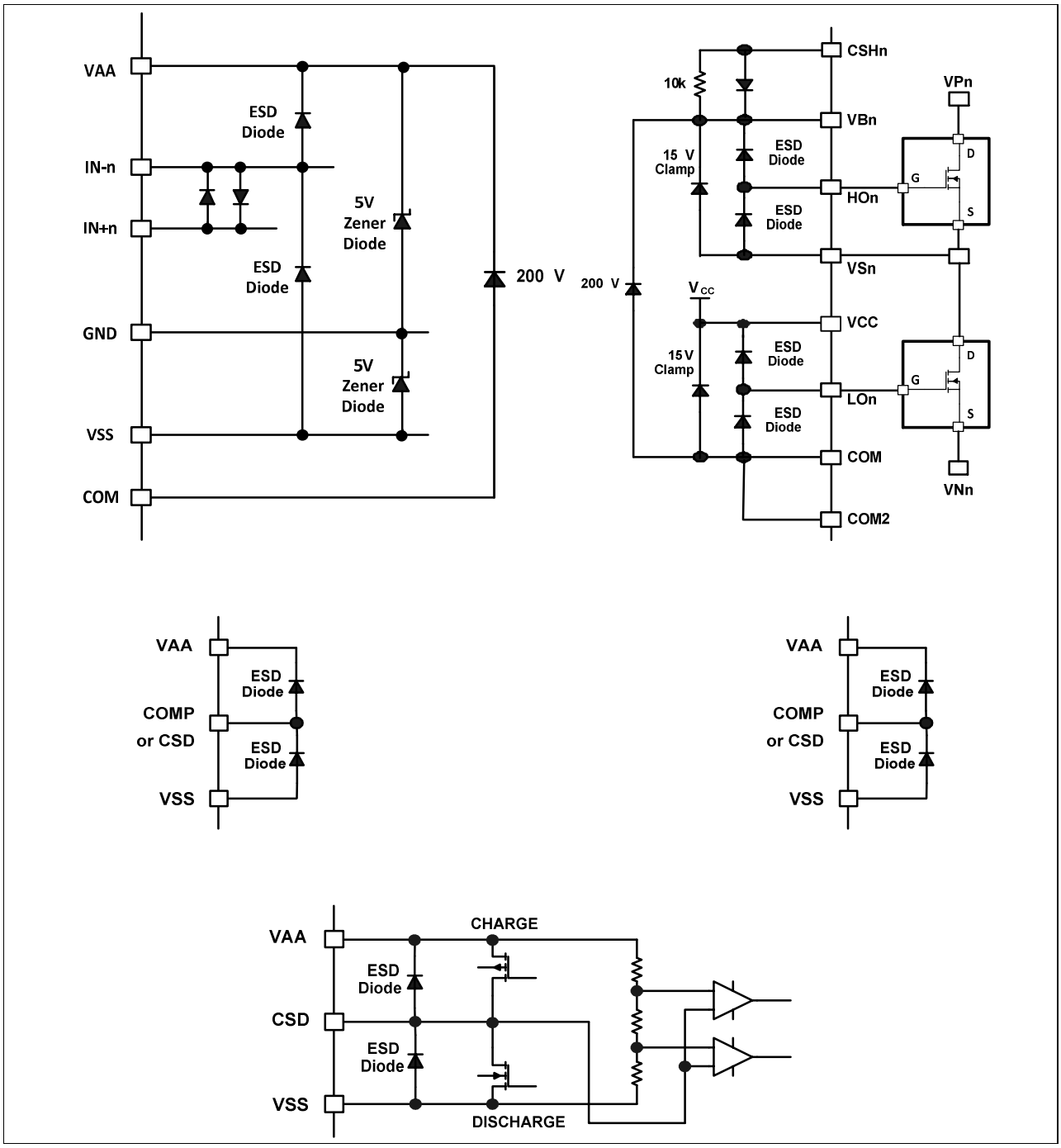


Figure 5 Input/output pin equivalent circuit diagrams

8 Lead definitions

Pin #	Symbol	Description
1	CLIP	Clipping detection output, open drain, referenced to GND
2	COMP2	CH2 PWM comparator input
3	IN-2	CH2 Analog inverting input
4	IN+2	CH2 Analog non-inverting input
5	GND	GND for internal shunt zener diodes to VAA and VSS
6	VSS	Floating input negative supply
7	VAA	Floating input positive supply
8	IN+1	CH1 Analog non-inverting input
9	IN-1	CH1 Analog inverting input
10	COMP1	CH1 PWM comparator input
11	CSD	Shutdown timing capacitor / shutdown input
12	FAULT	Fault reporting output, open drain, referenced to GND
13	VCC	Low side supply
14	COM	Low side supply return, internally connected to pin 27
15	CSH1	CH1 High side over current sensing input, referenced to VS1
16	VB1	CH1 High side floating supply
17	VS1	CH1 PWM output, internally connected to pin 19
18	VP1	CH1 Positive power supply
19	VS1	CH1 PWM output
20	VN1	CH1 Negative power supply, connect to COM externally
21	VN2	CH2 Negative power supply, connect to COM externally
22	VS2	CH2 PWM output, internally connected to pin 24
23	VP2	CH2 Positive power supply
24	VS2	CH2 PWM output
25	VB2	CH2 High side floating supply
26	CSH2	CH2 High side over current sensing input, referenced to VS2
27	COM	Low side supply return, internally connected to pin 14
28	NC	

9 Lead assignments

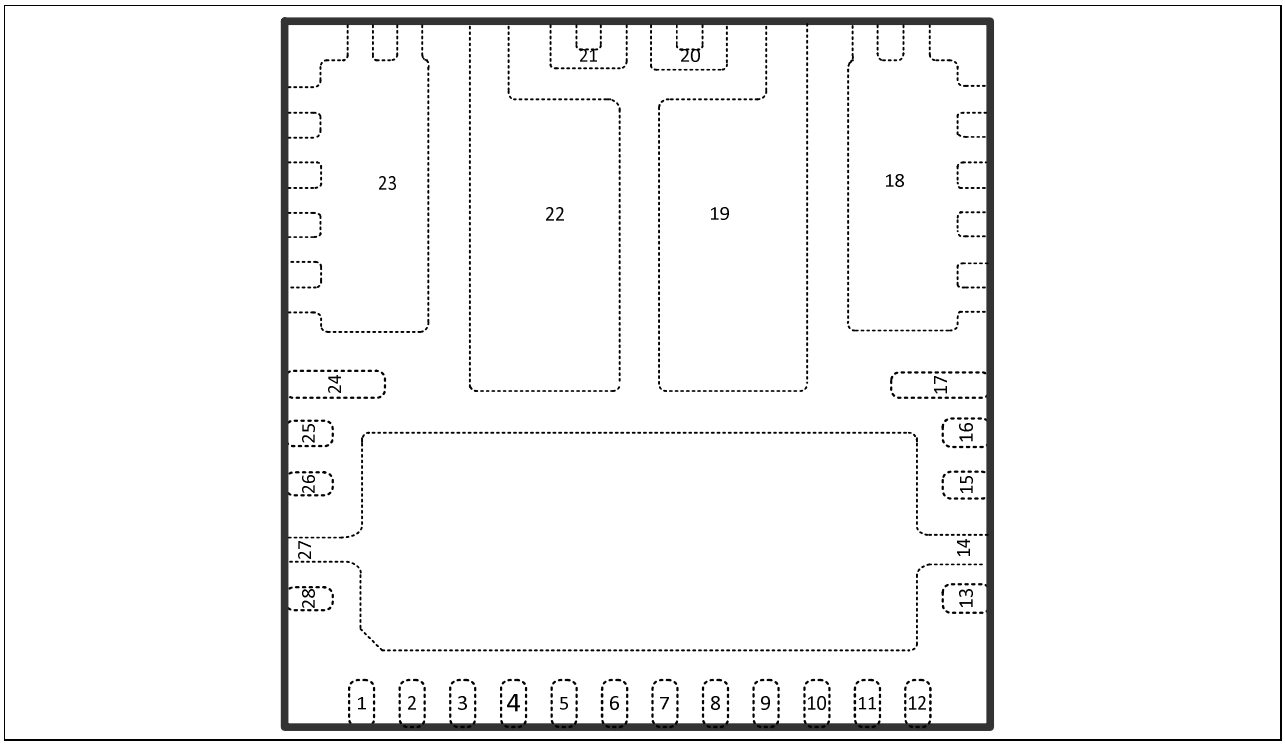


Figure 6 Lead assignments

10 Package details

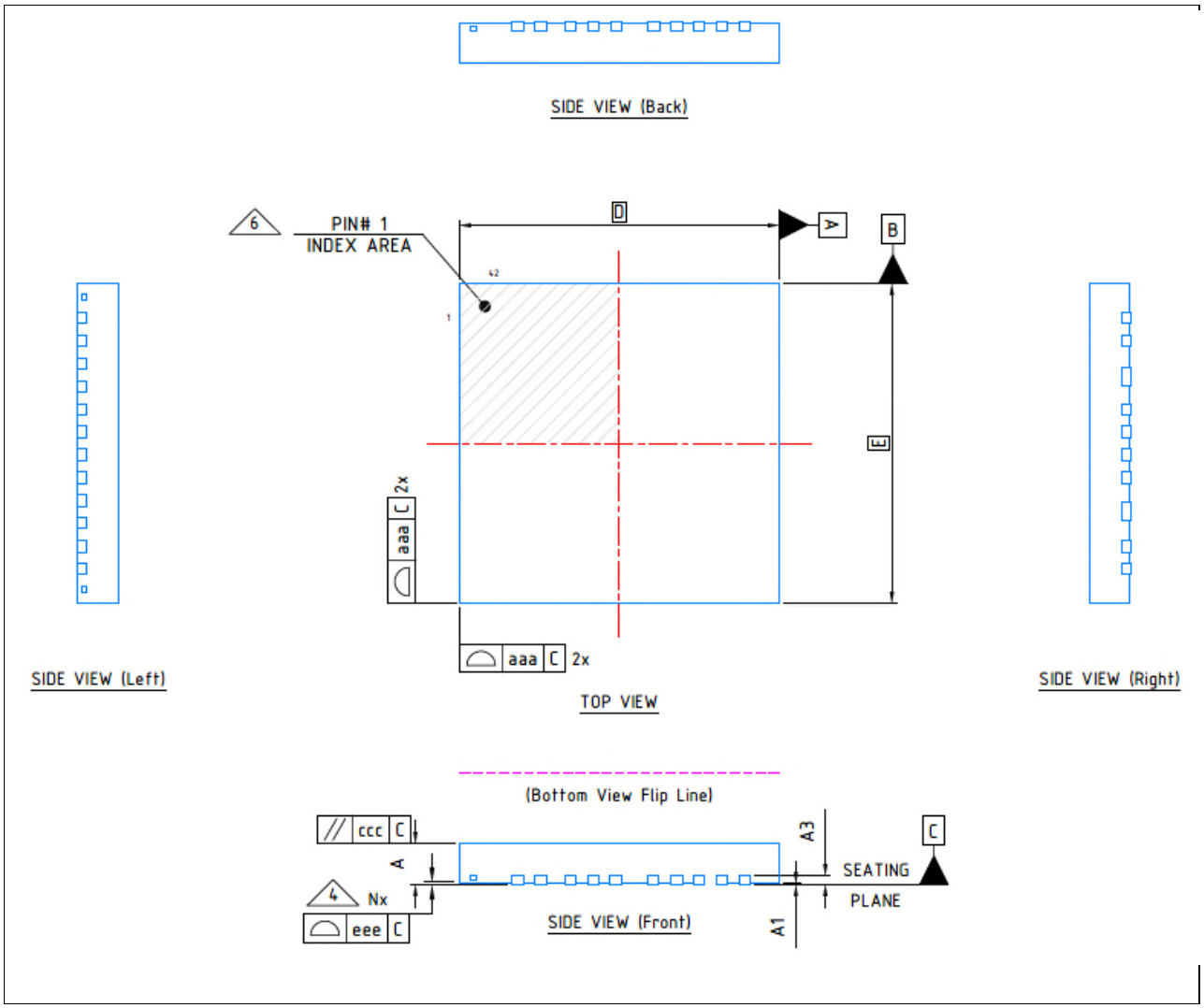


Figure 7 Package details

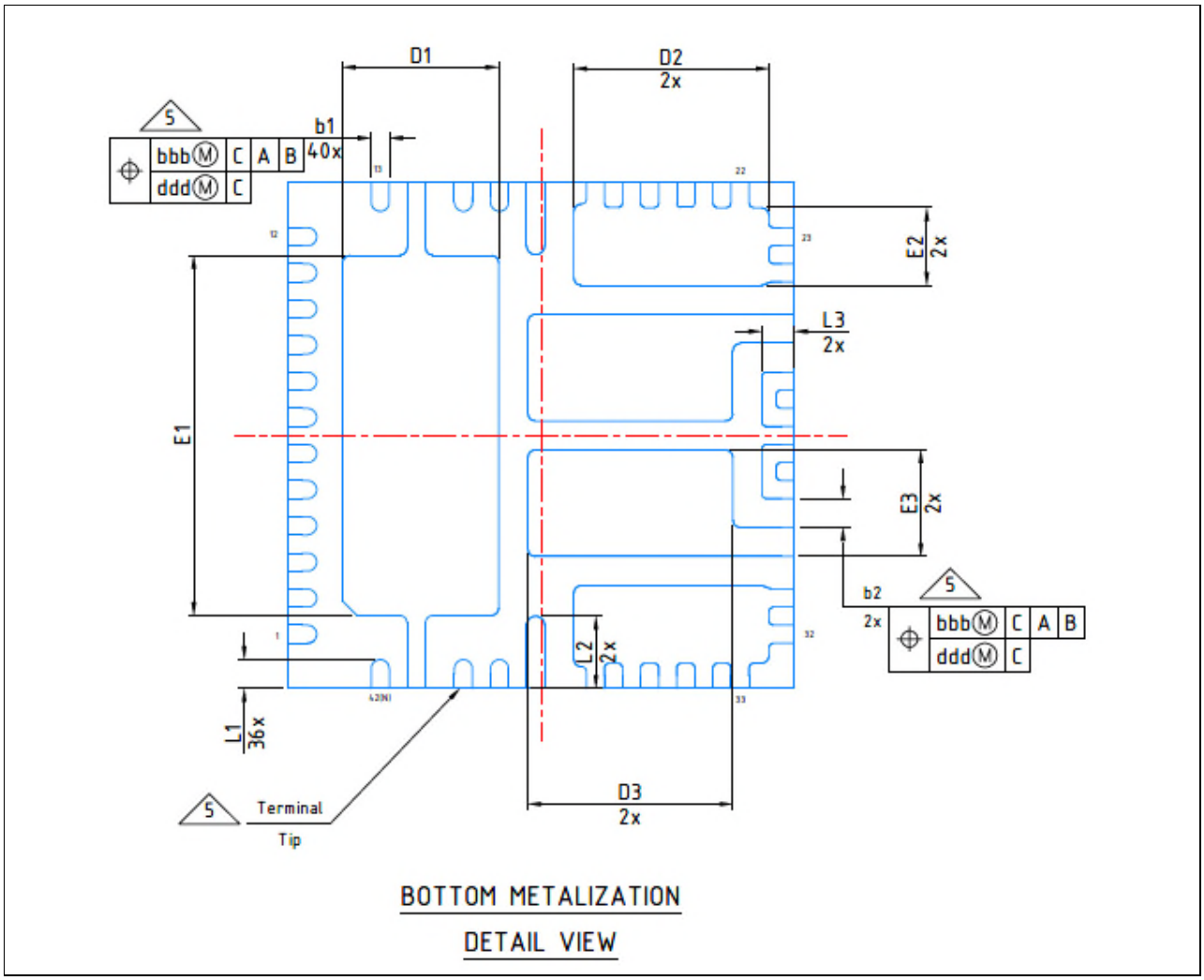


Figure 8 Package details; Bottom metallization detail view

Dimension Table				
Thickness / Symbol	V			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref	---	
b1	0.20	0.25	0.30	5
b2	0.35	0.40	0.45	5
D	7.00 BSC			
E	7.00 BSC			
D1	2.013	2.163	2.263	
E1	4.832	4.982	5.082	
D2	2.550	2.700	2.800	
E2	0.925	1.075	1.175	
D3	2.684	2.834	2.934	
E3	1.325	1.475	1.575	
L1	0.30	0.40	0.50	
L2	0.90	1.00	1.10	
L3	0.35	0.45	0.55	
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	42			3
NOTES	1, 2			
LF PART NO.	TBA			
LF DWG. NO.	TBA			

Figure 9 Dimension table

11 Board mounting, part marking, and ordering information

Board mounting

Refer to Application Note AN-1170 Audio Power Quad Flat No-Lead (PQFN) Board Mounting Application

Part marking

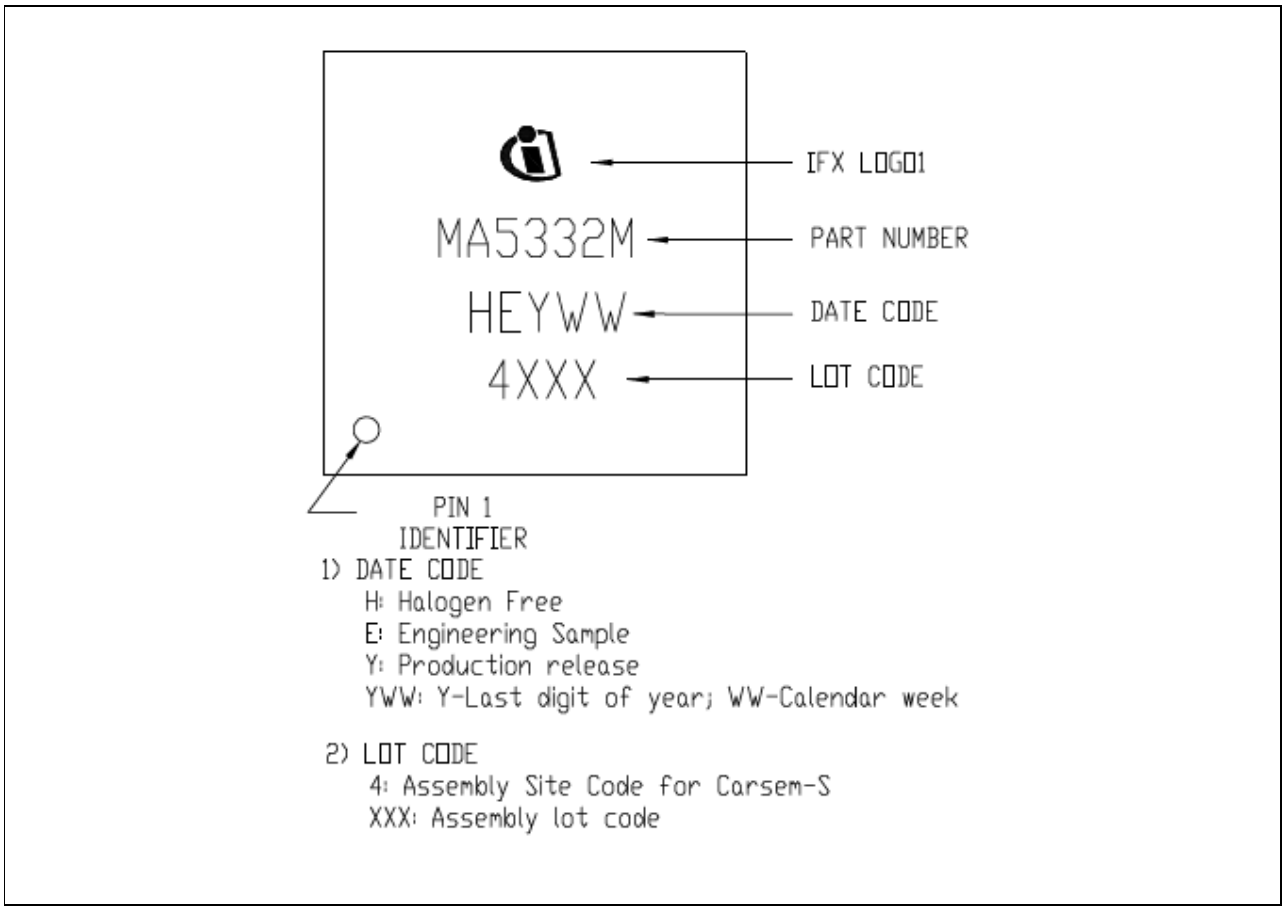


Figure 10 Part marking

Ordering information

Base part number	Package type	Standard pack		Complete part number
		Form	Quantity	
MA5332M	PQFN42 7x7mm	Tape and Reel	3000	MA5332MTRPBF

Revision history

Document version	Date of release	Description of changes
V1.0	Oct 10, 2016	First draft
V2.0	Feb 21, 2017	Updated package dimensions
V3.0	May 30, 2017	Updated Lead Definitions and Assignments
V3.5	Aug 22, 2017	MOSFET leakage current test conditions: I_{LK0} VP leakage current, VS=VN - - 20 µA V_P=100V, V_{CSD} =VSS I_{LK1} VP leakage current, VS=VP - - 50 µA I_{LK0} VP leakage current, VS=VN - - 20 µA V_P=150V, V_{CSD} =VSS I_{LK1} VP leakage current, VS=VP - - 50 µA
V3.6	Feb 14, 2018	Change Rds(on) max for MA5332 = 64m ohms. **Power MOSFET (FET1, FET2, FET3, FET4) (MA5342)** $R_{DS(ON)}$ FET on resistance - 46 64 mΩ I_D=3.6A
V3.7	Sep 10, 2018	1, Update MA5342 Maximum Power 2, Correct V_{AA} minimum supply voltage from Vss+4.5V→Vss+10V V_{AA} Floating input positive supply voltage†† V_{SS} +9.2 3, Append IQBS_OFF_CSH MIN=350uA, TYP=500uA, MAX=650uA 4, Append Noise limit V_{Nrmsn} CHn OTA input noise voltage, n=1-2 - 200 330 mVrms
V3.9	Apr 2, 2019	Update part marking information
V4.0	Aug 14, 2019	MA5332 only

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2019-08-19

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2020 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie") .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.