UMW FDD4243

-40V P-Channel MOSFET

1.Description

This P-Channel MOSFET has been produced technology to deliver low $R_{DS(ON)}$ and optimized Bvdss capability to offer superior performance benefit in the applications.

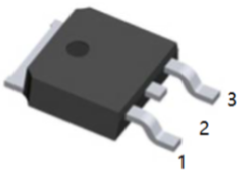
2.Features

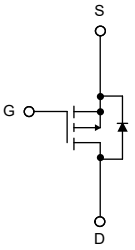
- $V_{DS\ (V)}$=-40V
- $R_{DS(ON)}$<20mΩ(V_{GS}=-10V)
- $R_{DS(ON)}$<30mΩ(V_{GS}=-4.5V)
- RoHS Compliant
- High performance trench technology for extremely low $R_{DS(ON)}$

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK) top view





4.Absolute Maximum Ratings T_C= 25°C

Parameter		Symbol	Rating	Units
Drain to Source Voltage		V_{DS}	-40	V
Gate to Source Voltage		V_{GS}	±20	
Drain Current -Continuous (Package limited)	T_C=25°C	I_D	-14	A
-Continuous (Silicon limited)	T_C=25°C (Note 1)		-24	
-Continuous	T_A=25°C (Note 1a)		-6.7	
-Pulsed			-60	
Single Pulse Avalanche Energy	(Note 3)	E_{AS}	84	mJ
Power Dissipation	T_C=25°C	P_D	42	W
Power Dissipation	(Note 1a)		3	
Operating and Storage Junction Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction to Case		$R_{\theta JC}$	3	°C/W
Thermal Resistance, Junction to Ambient	(Note 1a)	$R_{\theta JA}$	40	°C/W

6.Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=-250μA, V_{GS}=0V	-40			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D=-250μA Referenced to 25°C		-32		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-32V, V_{GS}=0V			-1	μA
		V_{DS}=-32V, V_{GS}=0V, T_J=125°C			-100	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
On Characteristics						
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1.4	-1.6	-3	V
Gate to Source Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D=-250μA Referenced to 25°C		4.7		mV/°C
Drain to Source On Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-6.7A		13	20	mΩ
		V_{GS}=-4.5V, I_D=-5.5A		25	30	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-6.7A		16		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS}=-20V, V_{GS}=0V, f=1MHz		1165	1550	pF
Output Capacitance	C_{oss}			165	220	pF
Reverse Transfer Capacitance	C_{rss}			90	135	pF
Gate Resistance	R_g	f=1MHz		4		Ω
SWITCHING PARAMETERS (Note 2)						
Turn-On DelayTime	$t_{D(on)}$	V_{DD}=-20V, I_D=-6.7A, V_{GS}=-10V, R_{GEN}=6Ω		6	12	ns
Rise Time	t_r			15	26	ns
Turn-Off DelayTime	$t_{D(off)}$			22	35	ns
Fall Time	t_f			7	14	ns
Total Gate Charge at 10V	$Q_{g(TOT)}$	V_{DD}=-20V, I_D=-6.7A, V_{GS}=-10V		21	29	nC
Gate to Source Gate Charge	Q_{gs}			3.4		nC
Gate to Drain “Miller” Charge	Q_{gd}			4		nC

Drain–Source Diode Characteristics						
Source to Drain Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=-6.7A (Note 2)		0.86	1.2	V
Reverse Recovery Time	t_{rr}	I_F=-6.7A, di/dt=100A/μs		29	43	ns
Reverse Recovery Charge	Q_{rr}			30	44	nC

Notes:

1: $R_{\theta JA}$ is sum of junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JC}$ is determined by the user's board design.

a. 40°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 96°C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3: Starting T_J=25°C, L=3mH, I_{AS}=7.5A, V_{DD}=40V, V_{GS}=10V.

7.1Typical characteristic

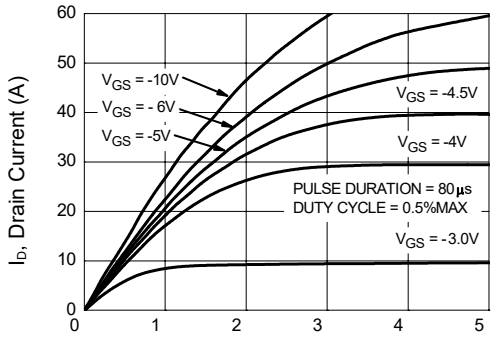


Figure 1: On-Region Characteristics

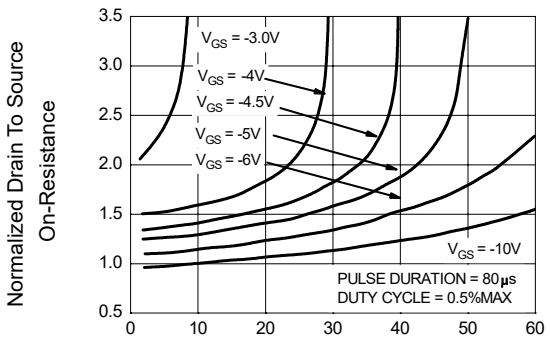


Figure 2: Normalized On-Resistance vs Drain Current and Gate Voltage

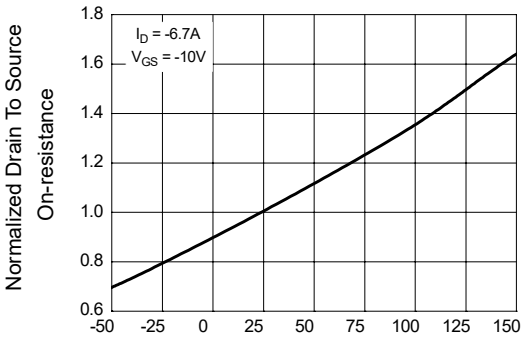


Figure 3: Normalized On Resistance vs Junction Temperature

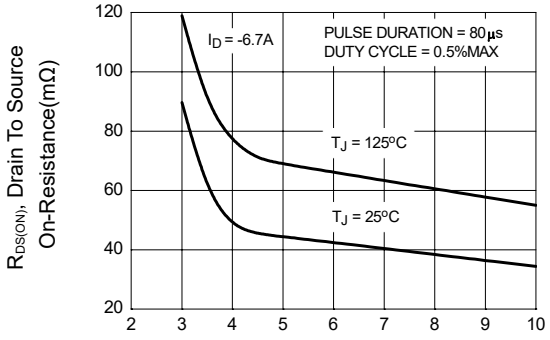


Figure 4: On-Resistance Variation with Gate-to-Source Voltage

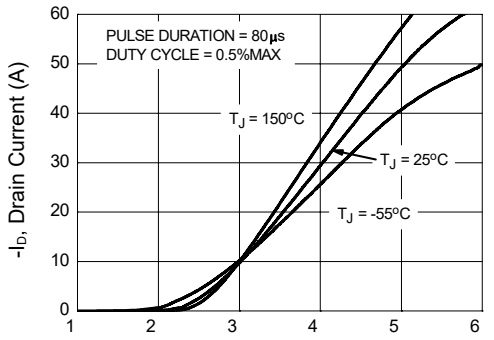


Figure 5: Transfer Characteristics

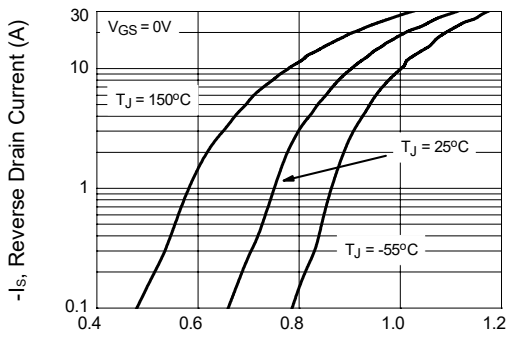


Figure 6: Source to Drain Diode Forward Voltage vs Source Current

7.2Typical characteristic

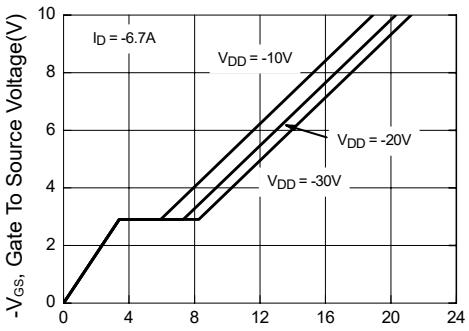


Figure 7: Gate Charge Characteristics

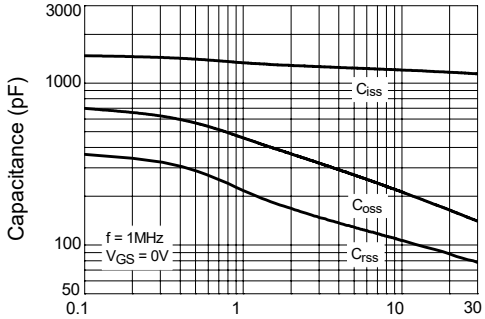


Figure 8: Capacitance vs Drain to Source Voltage

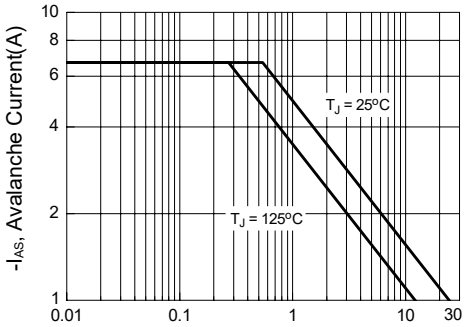


Figure 9: Unclamped Inductive Switching Capability

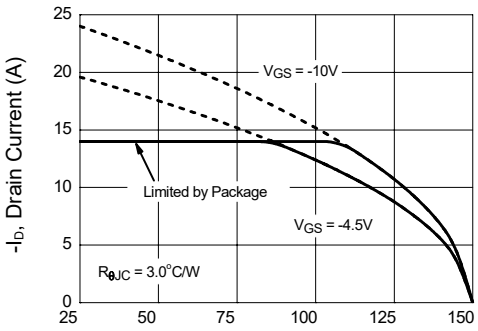


Figure 10: Maximum Continuous Drain Current vs Case Temperature

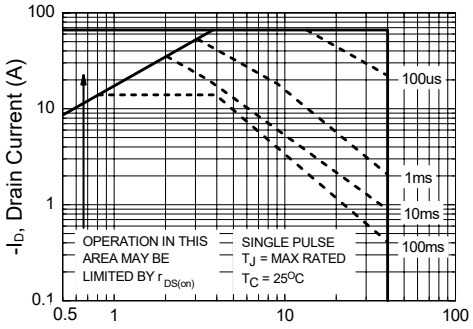


Figure 11: Forward Bias Safe Operating Area

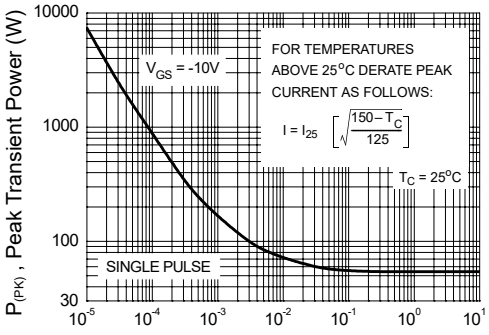


Figure 12: Single Pulse Maximum Power Dissipation

7.3Typical characteristic

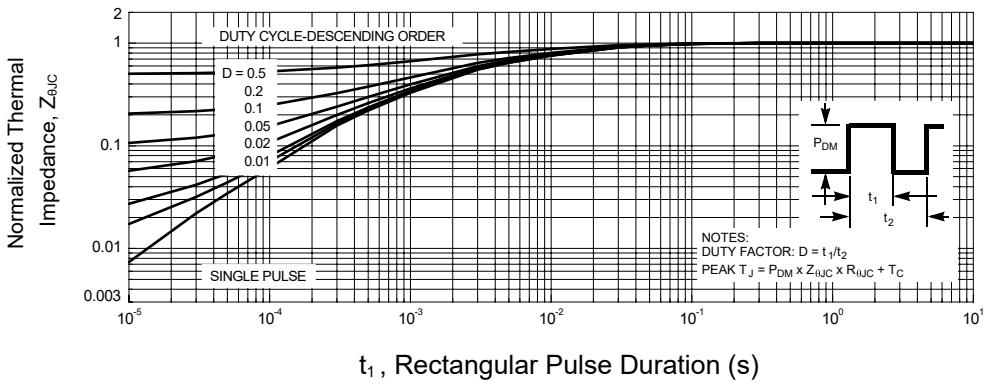
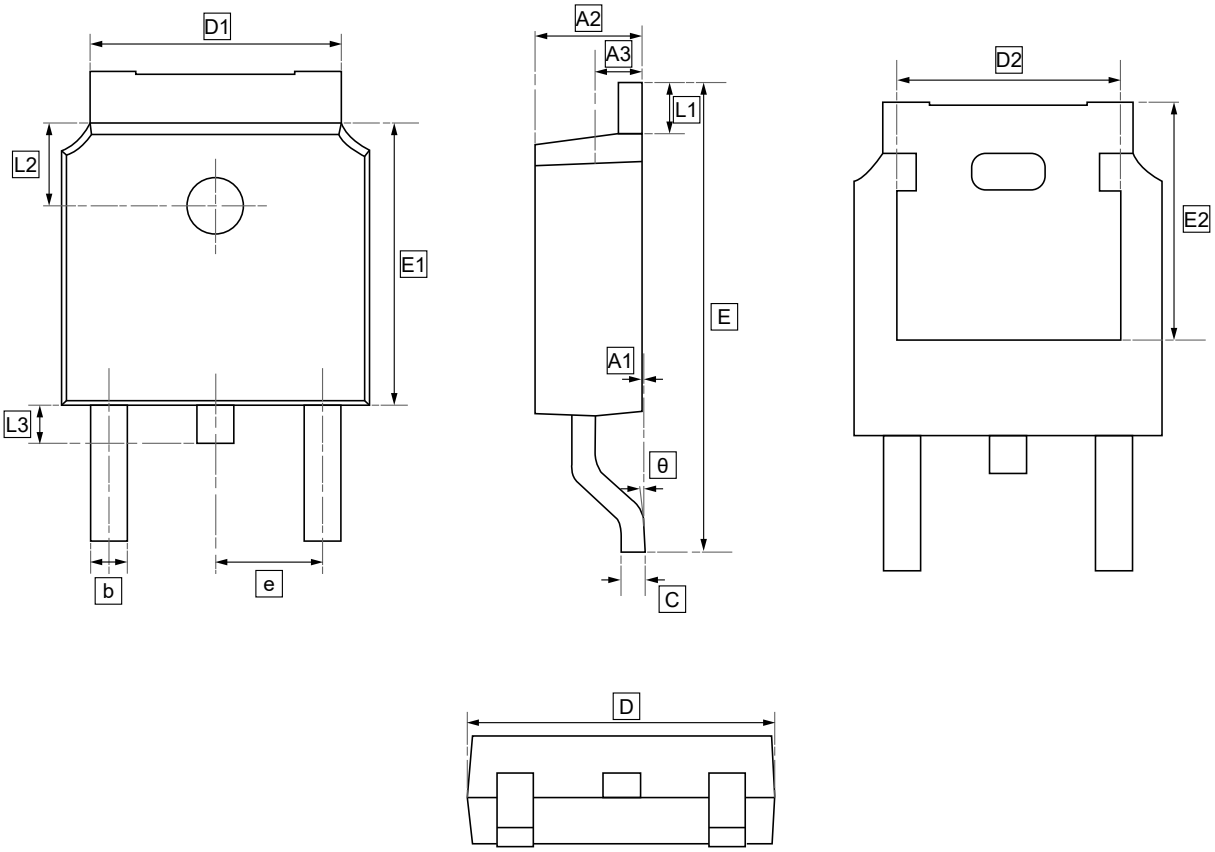


Figure 13: Transient Thermal Response Curve

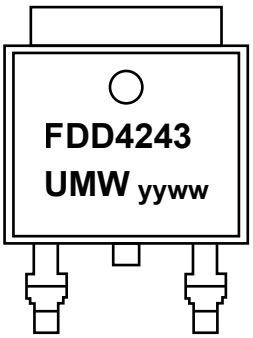
8.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDD4243	TO-252	2500	Tape and reel

10.Disclaimer

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