SNx4ACT74 双路正边沿触发式 D 型触发器

1 特性

- 4.5V 至 5.5V V_{CC} 运行
- 输入电压高达 5.5V
- t_{pd} 最大值为 10.5ns（5V 时）
- 输入兼容 TTL 电压

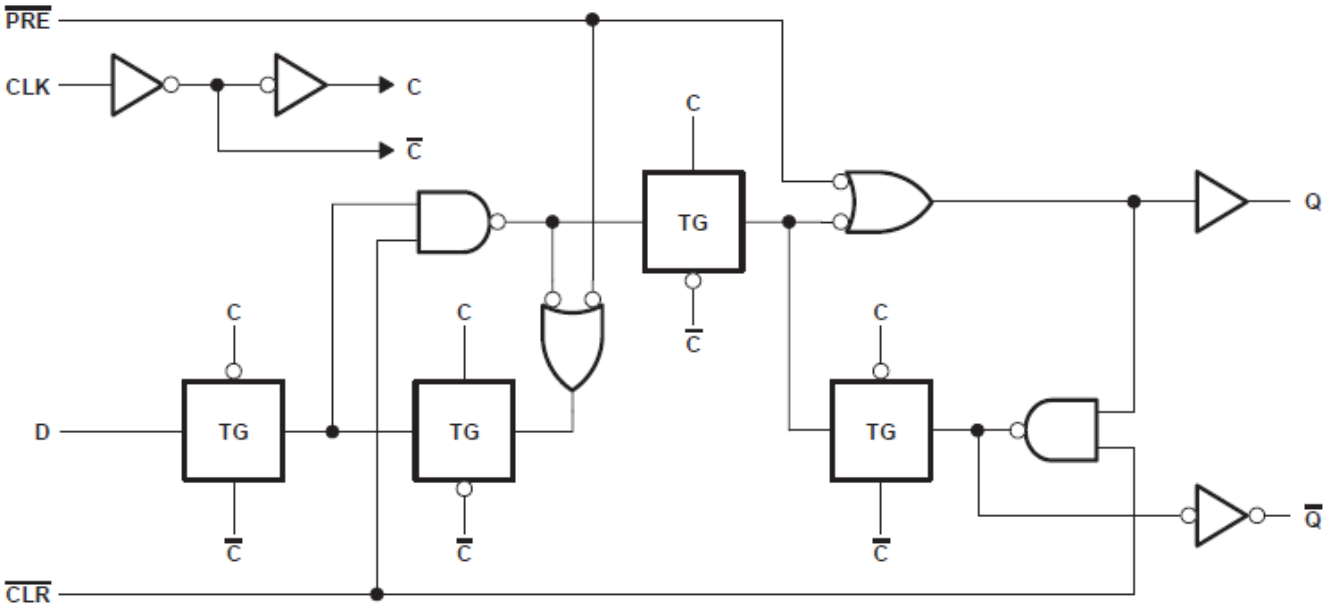
2 说明

'ACT74 双路正边沿触发器件是 D 型触发器。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SNx4ACT74	PW（TSSOP，14）	5mm × 6.4mm	5mm × 4.40mm
	D（SOIC，14）	8.65mm × 6mm	8.65mm × 3.9mm
	DB（SSOP，14）	6.2mm × 7.8mm	6.2mm × 5.3mm
	N（PDIP，14）	19.3mm × 9.4mm	19.3mm × 6.35mm
	NS（SOP，14）	10.2mm × 7.8mm	10.3mm × 5.3mm
	BQA (WQFN)	3mm × 2.5mm	3mm × 2.5mm

(1) 如需了解更多信息，请参阅机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



逻辑图（正逻辑）

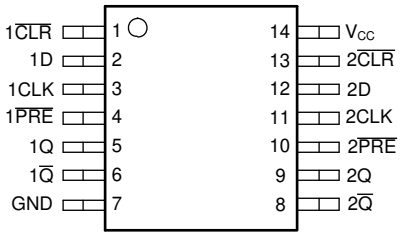
本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

内容

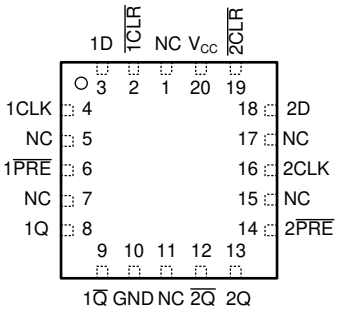
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3 引脚配置和功能



SN54ACT74 J 或 W 封装；SN74ACT74 D、DB、N、NS、PW（顶视图）



SN54ACT74 FK 封装（顶视图）

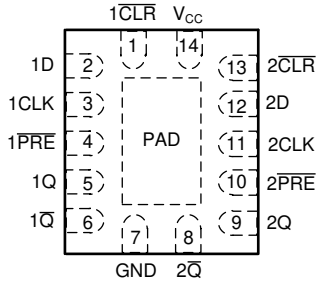


图 3-1. SN54ACT74 BQA 封装（顶视图）

引脚		类型(1)	说明
名称	编号		
1 $\overline{CLR}$	1	输入	通道 1，清零输入，低电平有效
1D	2	输入	通道 1，数据输入
1CLK	3	输入	通道 1，正边沿触发时钟输入
1 $\overline{PRE}$	4	输入	通道 1，预设输入，低电平有效
1Q	5	输出	通道 1，输出
1 $\overline{Q}$	6	输出	通道 1，反相输出
GND	7	—	接地
2 $\overline{Q}$	8	输出	通道 2，反相输出
2Q	9	输出	通道 2，输出
2 $\overline{PRE}$	10	输入	通道 2，预设输入，低电平有效
2CLK	11	输入	通道 2，正边沿触发时钟输入
2D	12	输入	通道 2，数据输入
2 $\overline{CLR}$	13	输入	通道 2，清零输入，低电平有效
V_{CC}	14	—	正电源

(1) 信号类型：I = 输入，O = 输出，I/O = 输入或输出

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4 规格

4.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	7	V
V_I	输入电压(2)		-0.5	V_{CC} + 0.5	V
V_O	在高阻抗或断电状态对任一输出施加的电压范围(2)		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	（V_I < 0 或 V_I > V_{CC}）		±20	mA
I_{OK}	输出钳位电流	（V_O < 0 或 V_O > V_{CC}）		±20	mA
I_O	持续输出电流	（V_O = 0 至 V_{CC}）		±50	mA
	通过 V_{CC} 或 GND 的持续电流			±200	mA
T_{stg}	贮存温度范围		-65	150	°C

4.2 建议的运行条件

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

		SN54ACT74		SN74ACT74		单位
		最小值	最大值	最小值	最大值	
V_{CC}	电源电压	4.5	5.5	4.5	5.5	V
V_{IH}	高电平输入电压	2		2		V
V_{IL}	低电平输入电压		0.8		0.8	V
V_I	输入电压	0	V_{CC}	0	V_{CC}	V
V_O	输出电压	0	V_{CC}	0	V_{CC}	V
I_{OH}	高电平输出电流		-24		-24	mA
I_{OL}	低电平输出电流		24		24	mA
$\Delta t/\Delta v$	输入转换上升或下降速率		8		8	ns/V
T_A	自然通风条件下的工作温度范围	-55	125	-40	85	°C

4.3 热性能信息

热指标(1)		SN74ACT74						
		BQA (WQFN)	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	单位
		14 引脚						
$R_{\theta JA}$	结温至环境温度热阻	91.3	119.9	96	80	76	145.7	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	99.4	—	—	—	—	—	°C/W
$R_{\theta JB}$	结至电路板热阻	60.1	—	—	—	—	—	°C/W
Ψ_{JT}	结至顶部特征参数	14.5	—	—	—	—	—	°C/W
Ψ_{JB}	结至电路板特征参数	60.8	—	—	—	—	—	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	37.0	—	—	—	—	—	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

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4.4 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	T_A = 25°C			SN54ACT74		SN74ACT74		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	I_{OH} = -50μA	4.5V	4.4	4.49		4.4		4.4		V
		5.5V	5.4	5.49		5.4		5.4		
	I_{OH} = -24mA	4.5V	3.86			3.7		3.76		
		5.5V	4.86			4.7		4.76		
	I_{OH} = – 50mA†(1)	5.5V				3.86				
	I_{OH} = – 75mA†(1)	5.5V						3.85		
V_{OL}	I_{OL} = 50μA	4.5V		0.001	0.1		0.1		0.1	V
		5.5V		0.001	0.1		0.1		0.1	
	I_{OL} = 24mA	4.5V			0.36		0.5		0.44	
		5.5V			0.36		0.5		0.44	
	I_{OL} = 50mA†(1)	5.5V					1.65			
	I_{OL} = 75mA†(1)	5.5V							1.65	
I_I	V_I = V_{CC} 或 GND	5.5V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} 或 GND，I_O = 0	5.5V			2		40		20	μA
ΔI_{CC}‡ (2)	一个输入电压为 3.4V，其他输入电压为 GND 或 V_{CC}	5.5V		0.6			1.6		1.5	mA
C_i	V_I = V_{CC} 或 GND	5V		3						pF

(1) 一次不应测试超过一个输出，且测试持续时间不应超过 2ms。
(2) 这是每个输入在指定 TTL 电压电平之一而不是 0V 或 V_{CC} 时电源电流的增加情况。

4.5 时序要求

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

			T_A = 25°C		SN54ACT74		SN74ACT74		单位
			最小值	最大值	最小值	最大值	最小值	最大值	
f_{clock}	时钟频率			145		85		125	MHz
t_w	脉冲持续时间	$\overline{PRE}$ 或 $\overline{CLR}$ 为低电平	5		7		6		ns
		CLK	5		7		6		
t_{su}	建立时间，CLK↑ 前的数据	数据	3		4		3.5		ns
			0		0.5		0		
t_h	保持时间，CLK↑ 后的数据	$\overline{PRE}$ 或 $\overline{CLR}$ 处于非活动状态	1		1		1		ns

4.6 开关特性

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	SN54ACT74					SN74ACT74					单位
			T_A = 25°C			最小值	最大值	T_A = 25°C			最小值	最大值	
			最小值	典型值	最大值			最小值	典型值	最大值			
f_{max}			145	210		85		145	210		125		MHz
t_{PLH}	$\overline{PRE}$ 或 $\overline{CLR}$	Q 或 $\overline{Q}$	1	5.5	9.5	1	11.5	3	5.5	9.5	2.5	10.5	ns
t_{PHL}			1	6	10	1	12.5	3	6	10	3	11.5	

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在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	SN54ACT74					SN74ACT74					单位
			T_A = 25°C					T_A = 25°C					
			最小值	典型值	最大值	最小值	最大值	最小值	典型值	最大值	最小值	最大值	
t_{PLH}	CLK	Q 或 $\overline{Q}$	1	7.5	11	1	14	4	7.5	11	4	13	ns
t_{PHL}			1	6	10	1	12	3.5	6	10	3	11.5	

4.7 工作特性

V_{CC} = 5V，T_A = 25°C

参数		测试条件		典型值	单位
C_{pd}	功率耗散电容	C_L = 50pF，	f = 1MHz	45	pF

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5 参数测量信息

C_L 包括探头和夹具电容。所有输入脉冲均由具有以下特性的发生器提供：PRR ≤ 1MHz、ZO = 50Ω、tr ≤ 2.5ns、tf ≤ 2.5ns。一次测量一个输出，每次测量一个输入转换。

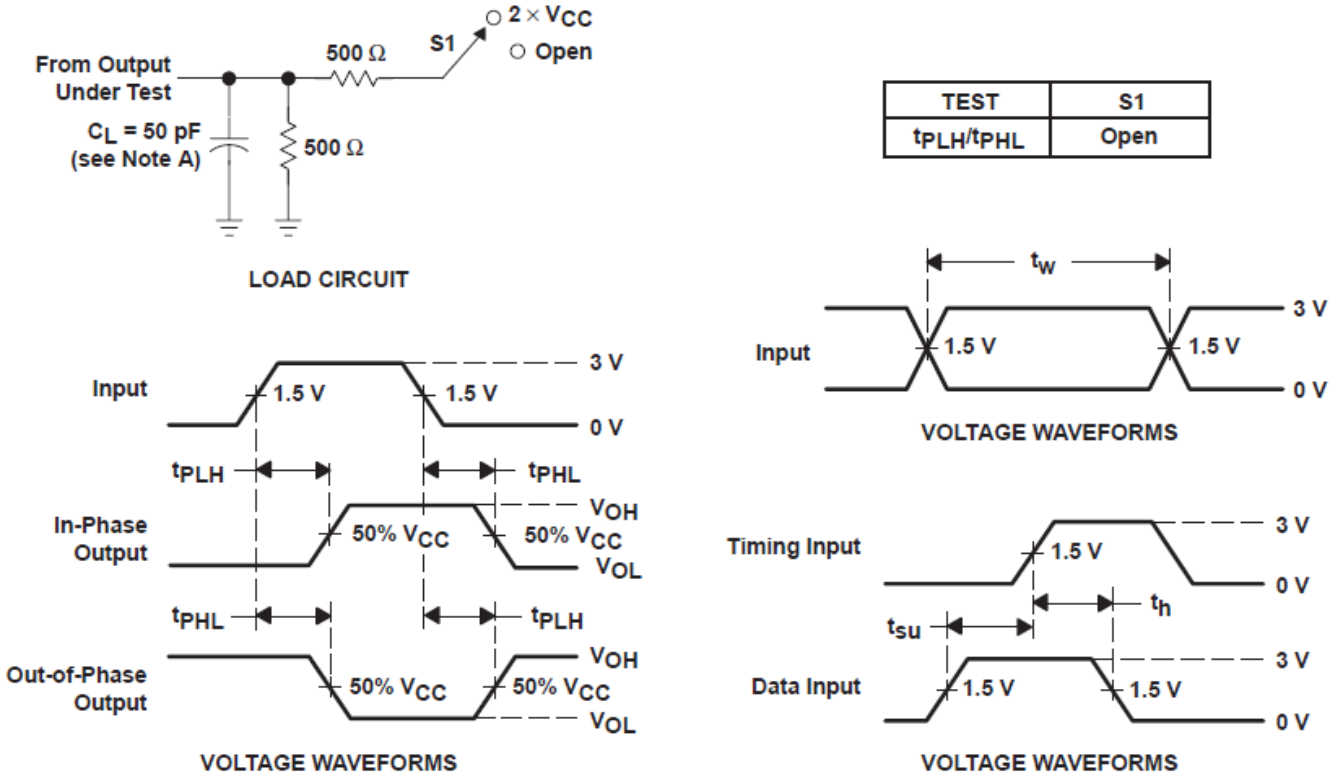


图 5-1. 负载电路和电压波形

备注

A. C_L 包括探针和夹具电容。

B. 所有输入脉冲均由具有以下特性的发生器提供：PRR ≤ 1MHz、ZO = 50Ω、tr ≤ 2.5ns、tf ≤ 2.5ns。

C. 一次测量一个输出，每次测量进行一次输入转换。

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6 详细说明

6.1 概述

预设 ($\overline{PRE}$) 或清零 ($\overline{CLR}$) 输入端的低电平将会设置或重置输出，而不受其他输入端的电平的影响。当 $\overline{PRE}$ 和 $\overline{CLR}$ 处于非活动状态（高电平）时，数据 (D) 输入处满足设置时间要求的数据将传输到时钟脉冲正向边沿上的输出处。时钟触发出现在一个特定电压电平上，并且不与时钟脉冲的上升时间直接相关。经过保持时间间隔后，如果更改 D 处的数据，不会影响输出端的电平。

6.2 功能方框图

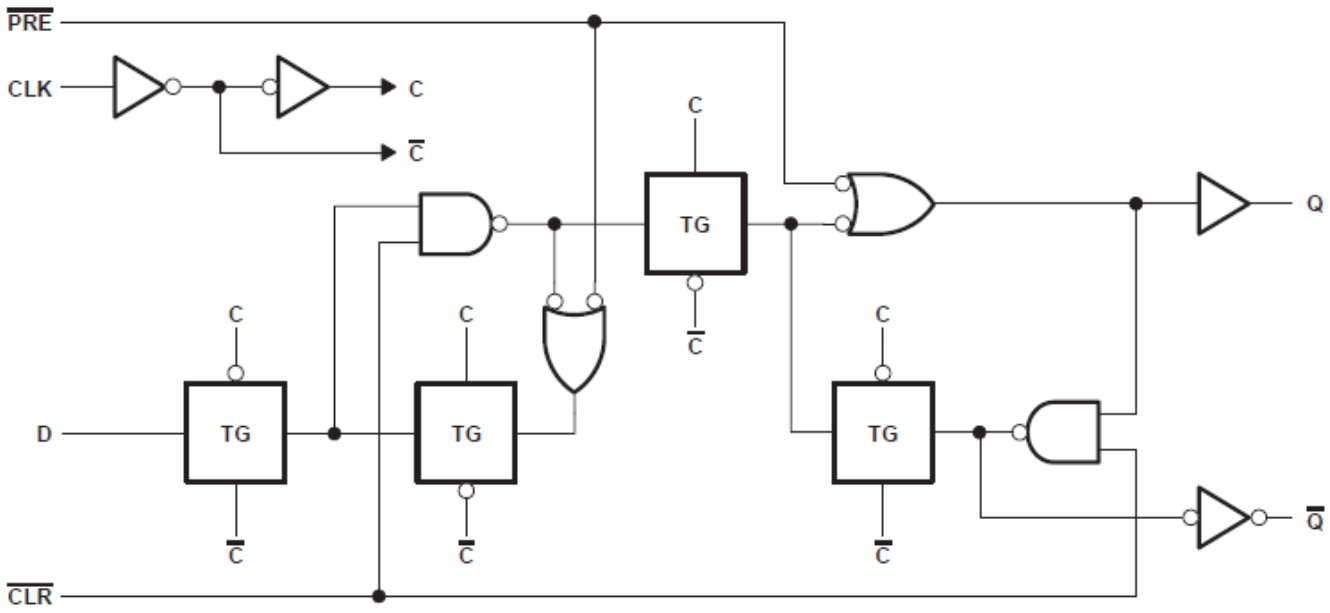


图 6-1. 逻辑图（正逻辑）

6.3 器件功能模式

表 6-1. 功能表（每个触发器）

输入				输出	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H1	H1
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

1. 该配置不稳定；也就是说，当 PRE 或 CLR 恢复到其非活动（高）电平时，该配置不会持续存在。

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7 应用和实施

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

7.1 电源相关建议

电源可以是*建议运行条件*中最小和最大电源电压额定值之间的任何电压。每个 V_{CC} 端子均应具有一个良好的旁路电容器，以防止功率干扰。建议为该器件使用 0.1 µF 电容器。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 µF 和 1 µF 电容器通常并联使用。旁路电容器应安装在尽可能靠近电源端子的位置，以获得更佳效果，如图 7-1 所示。

7.2 布局

7.2.1 布局指南

当使用多位逻辑器件时，输入决不能悬空。

在许多情况下，是未使用数字逻辑器件的全部或部分功能（例如，仅使用三输入与门的两个输入，或仅使用四个缓冲门中的三个）。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的运行状态。以下指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。应根据器件的功能为任何特定未使用的输入施加逻辑电平。通常，它们将连接到 GND 或 V_{CC}，具体取决于哪种更合理或更方便。悬空输出通常是可行的，除非该器件是收发器。如果该收发器有一个输出使能引脚，它会在置为有效时禁用该器件的输出部分。这不会禁用 I/O 的输入部分，因此输入在禁用后也无法悬空。

7.2.2 布局示例

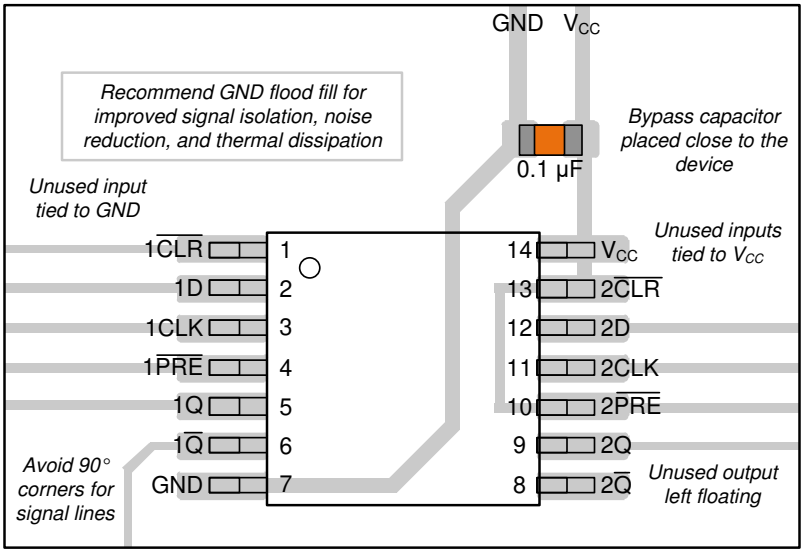


图 7-1. SNx4ACT74 封装的示例布局

8 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

8.1 文档支持（模拟）

8.1.1 相关文档

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 8-1. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
SN54ACT74	点击此处	点击此处	点击此处	点击此处	点击此处
SN74ACT74	点击此处	点击此处	点击此处	点击此处	点击此处

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (July 2024) to Revision J (April 2025) **Page**

- 添加了 BQA 封装 3
- 添加了 BQA 热性能信息 4

Changes from Revision H (October 2003) to Revision I (July 2024) **Page**

- 添加了*器件信息*表、*引脚功能*表、*热性能信息*表、*器件功能模式*、*应用和实施*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1
- 更新了整个文档中的表格、图和交叉参考的编号格式 1

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• 更新了 R θ JA 值：D = 86 至 119.9，PW = 113 至 145.7，所有值均以 °C/W 为单位..... 4

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

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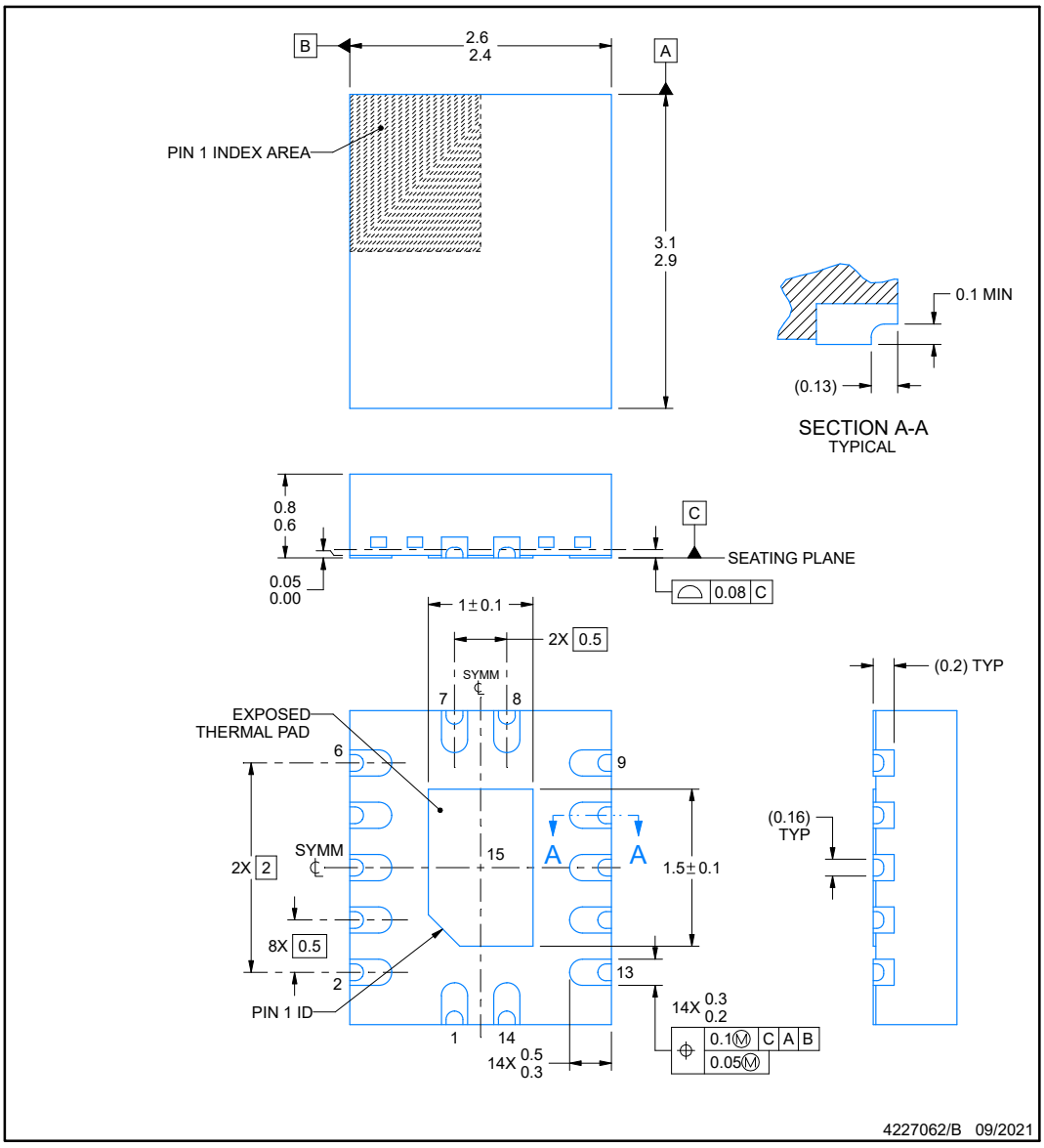
PACKAGE OUTLINE



BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

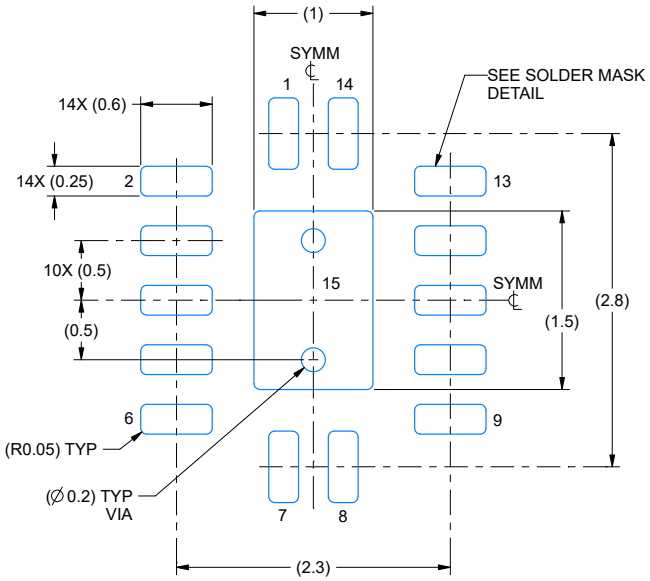
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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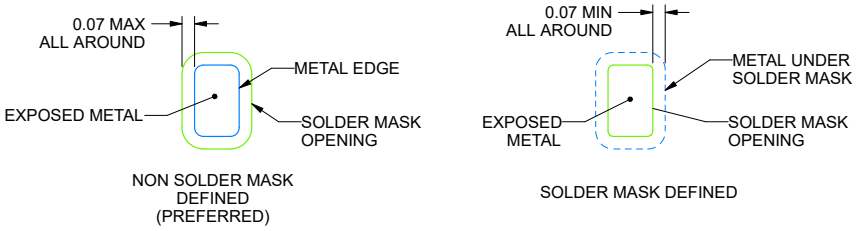
EXAMPLE BOARD LAYOUT

BQA0014B — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4227062/B 09/2021

NOTES: (continued)

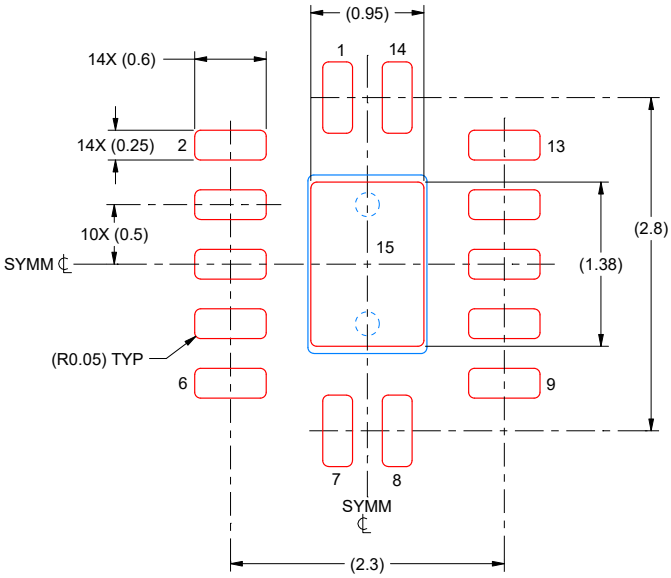
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

BQA0014B — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8752501M2A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8752501M2A SNJ54ACT 74FK
5962-8752501MCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8752501MCA SNJ54ACT74J
5962-8752501MDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8752501MDA SNJ54ACT74W
SN74ACT74BQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD74
SN74ACT74D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	ACT74
SN74ACT74DBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD74
SN74ACT74DBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD74
SN74ACT74DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74
SN74ACT74DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74
SN74ACT74DR1G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74
SN74ACT74DR1G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74
SN74ACT74N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT74N
SN74ACT74N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT74N
SN74ACT74NE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT74N
SN74ACT74NSR	NRND	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74
SN74ACT74NSR.A	NRND	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74
SN74ACT74PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	AD74
SN74ACT74PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	AD74
SN74ACT74PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD74
SN74ACT74PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD74
SN74ACT74PWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD74
SNJ54ACT74FK	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8752501M2A SNJ54ACT 74FK

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54ACT74FK.A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8752501M2A SNJ54ACT 74FK
SNJ54ACT74J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8752501MCA SNJ54ACT74J
SNJ54ACT74J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8752501MCA SNJ54ACT74J
SNJ54ACT74W	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8752501MDA SNJ54ACT74W
SNJ54ACT74W.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8752501MDA SNJ54ACT74W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ACT74, SN74ACT74 :

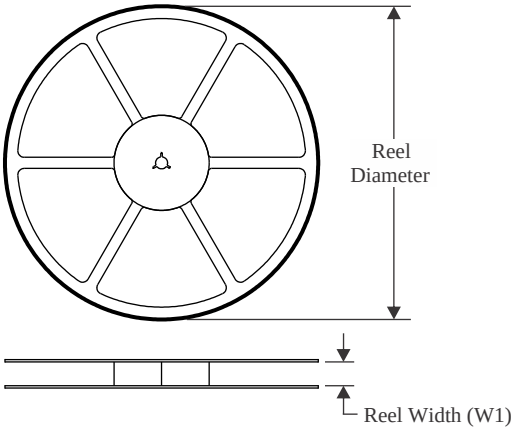
- Catalog : SN74ACT74
- Automotive : SN74ACT74-Q1, SN74ACT74-Q1
- Enhanced Product : SN74ACT74-EP, SN74ACT74-EP
- Military : SN54ACT74

NOTE: Qualified Version Definitions:

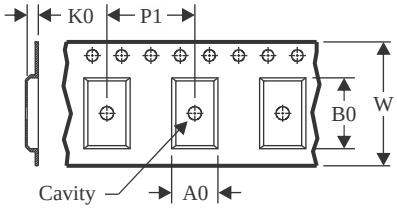
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

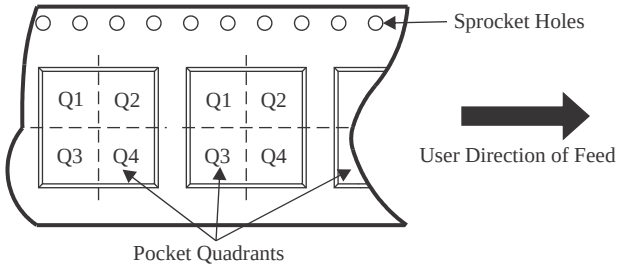


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

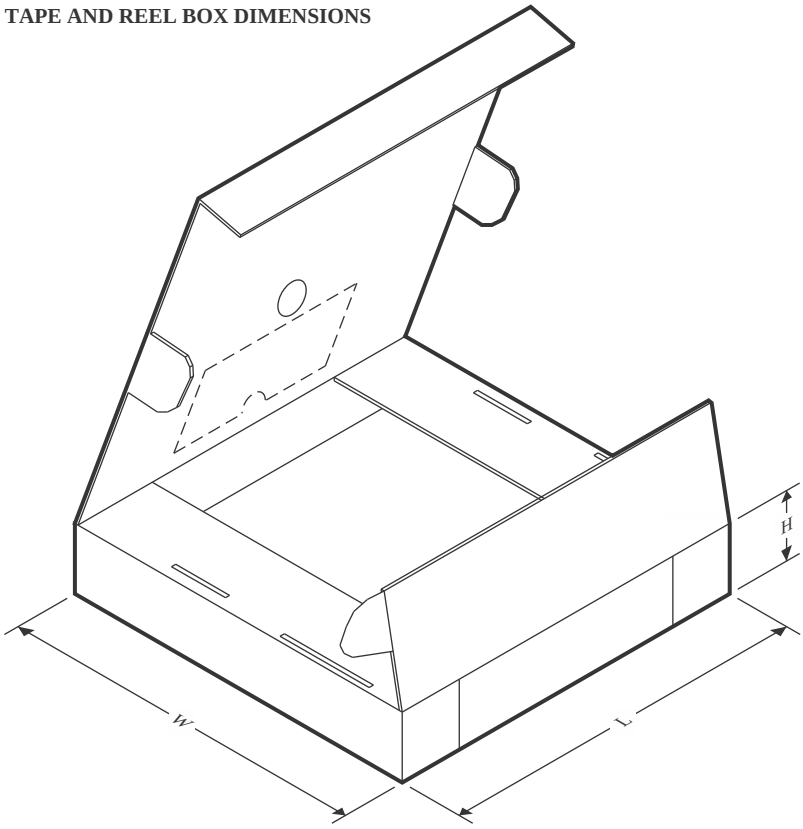
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT74BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74ACT74DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ACT74NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74ACT74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT74PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

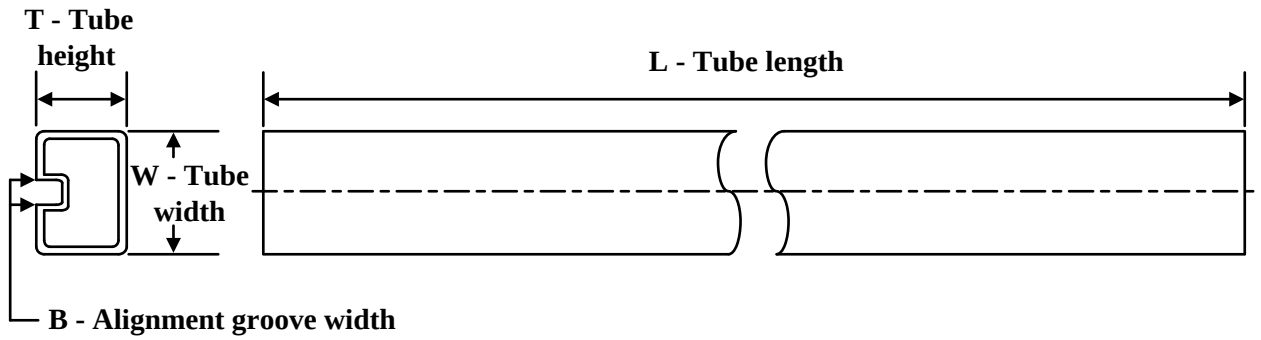
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

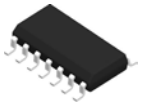
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT74BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74ACT74DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74ACT74NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74ACT74PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74ACT74PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8752501M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8752501MDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74ACT74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT74N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT74N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54ACT74FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT74FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT74W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54ACT74W.A	W	CFP	14	25	506.98	26.16	6220	NA

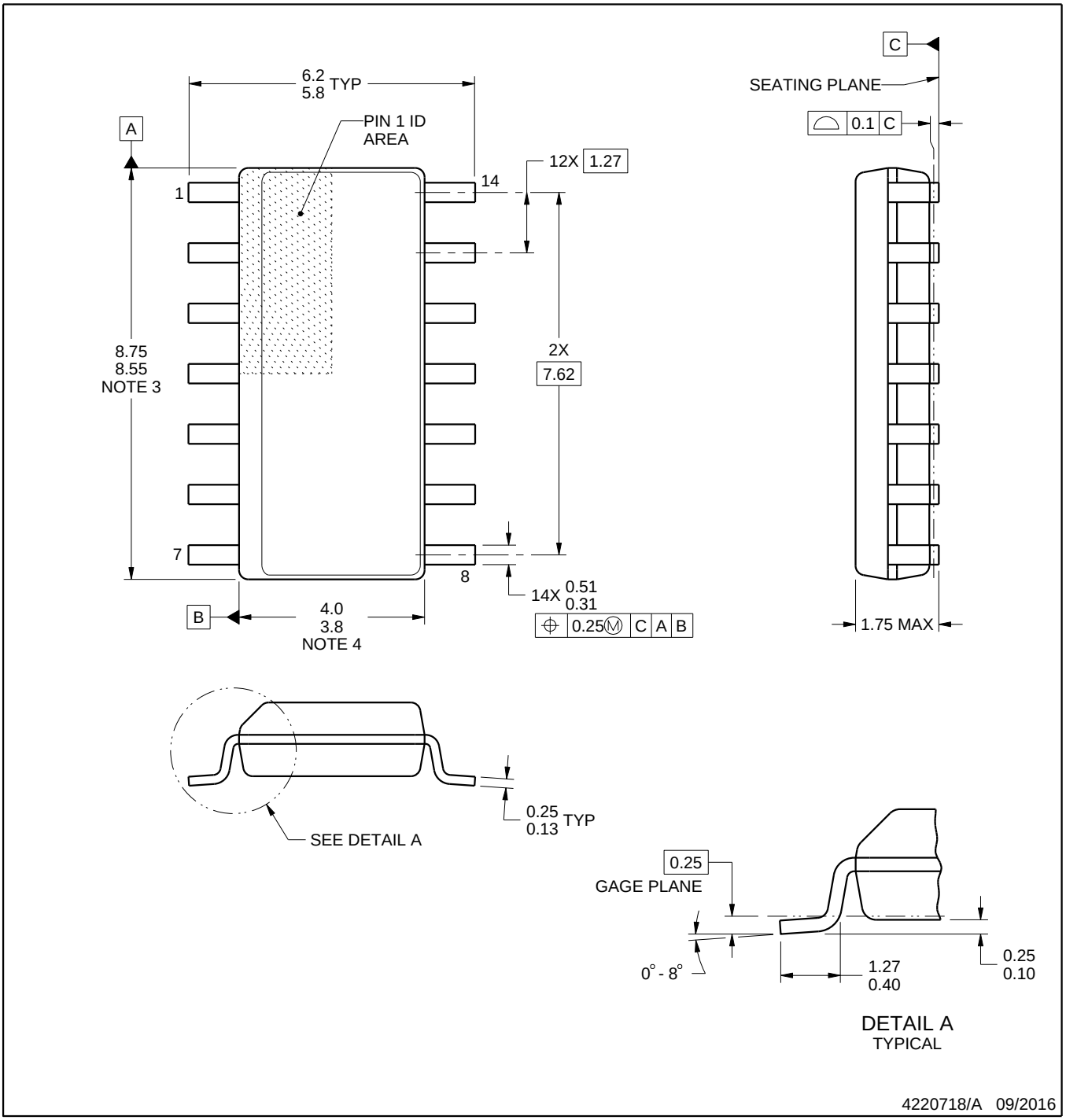


PACKAGE OUTLINE

D0014A

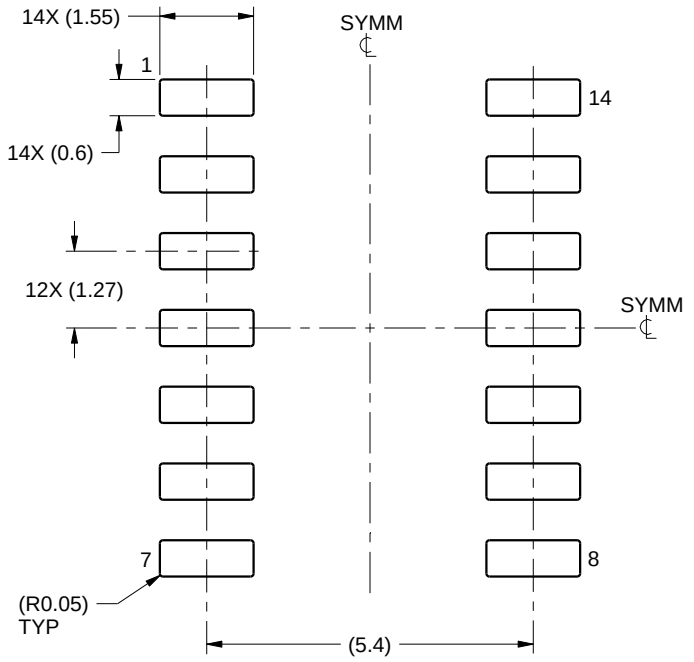
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

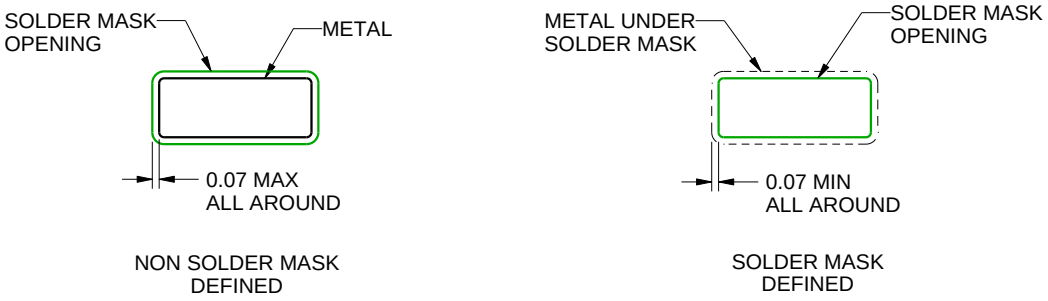


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

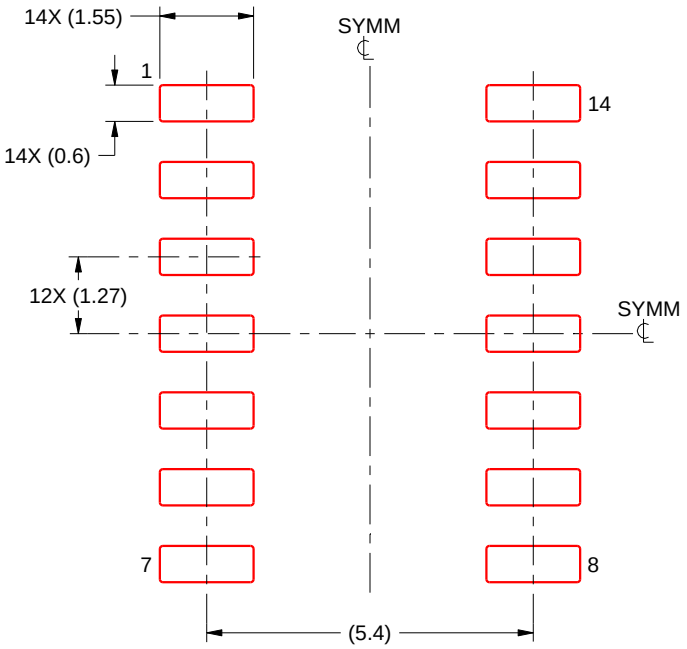
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

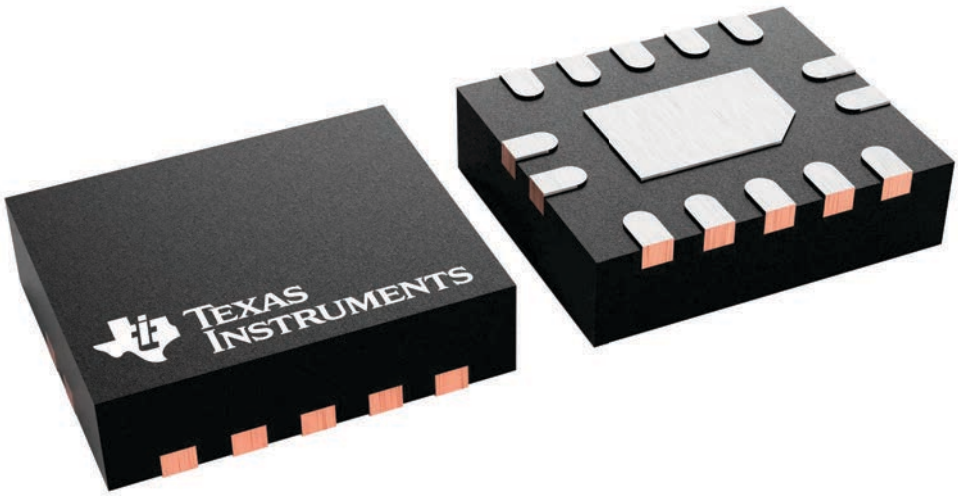
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

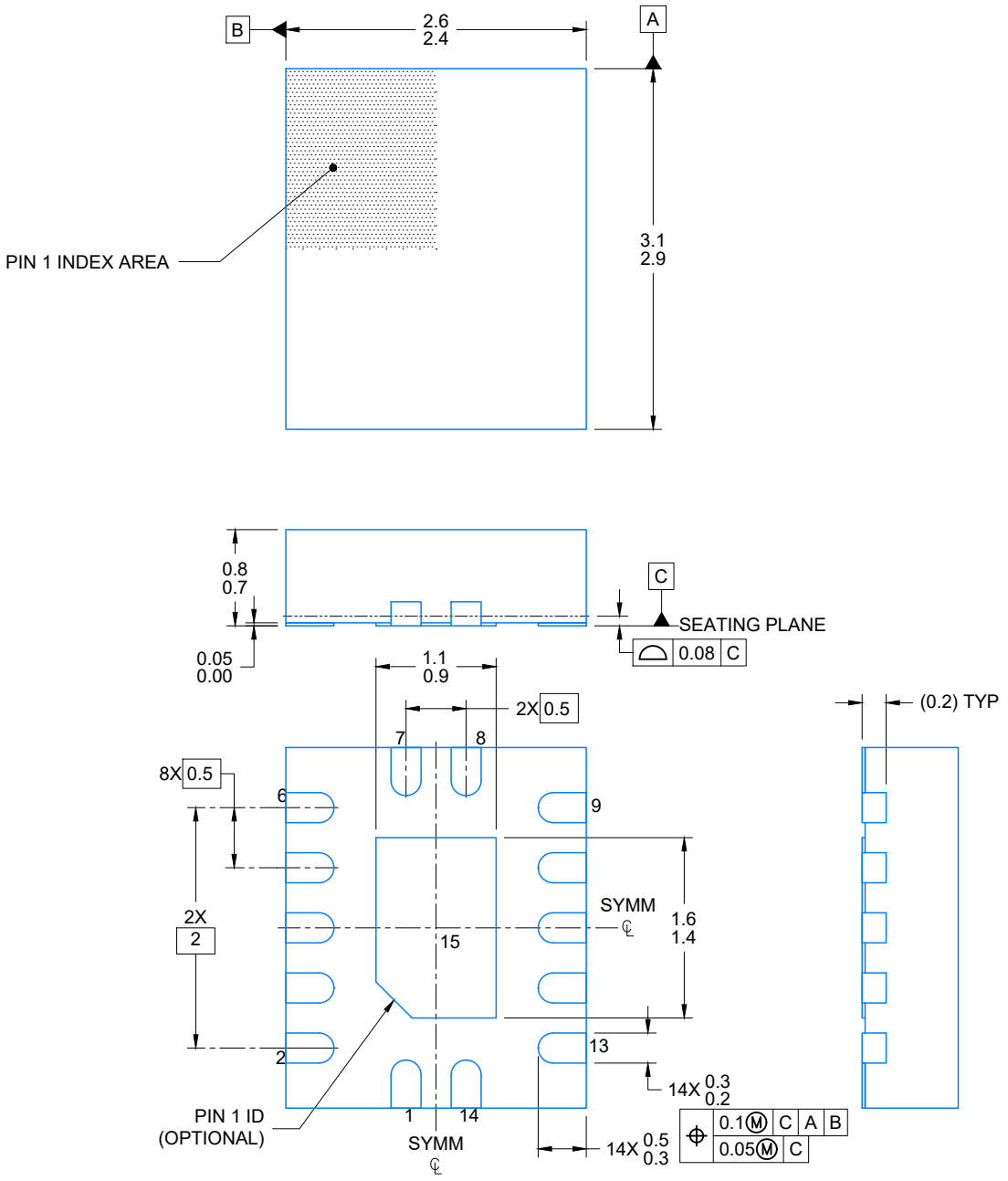


PACKAGE OUTLINE

BQA0014A

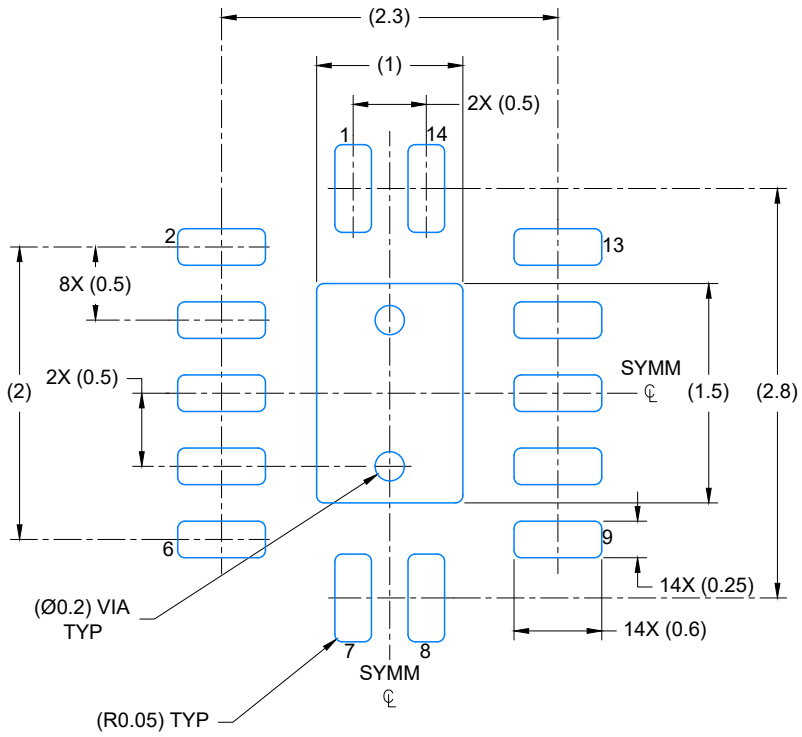
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

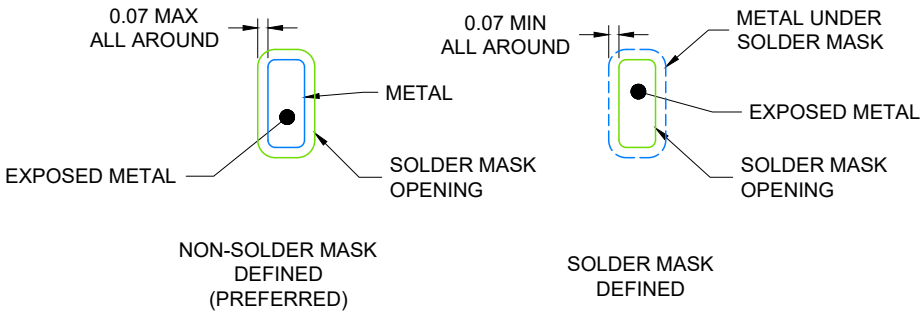


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



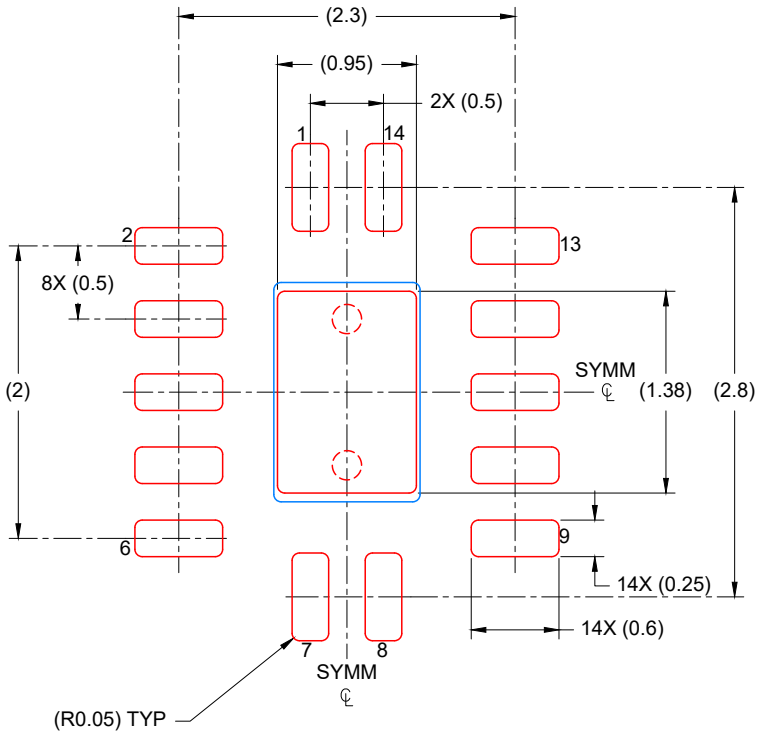
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

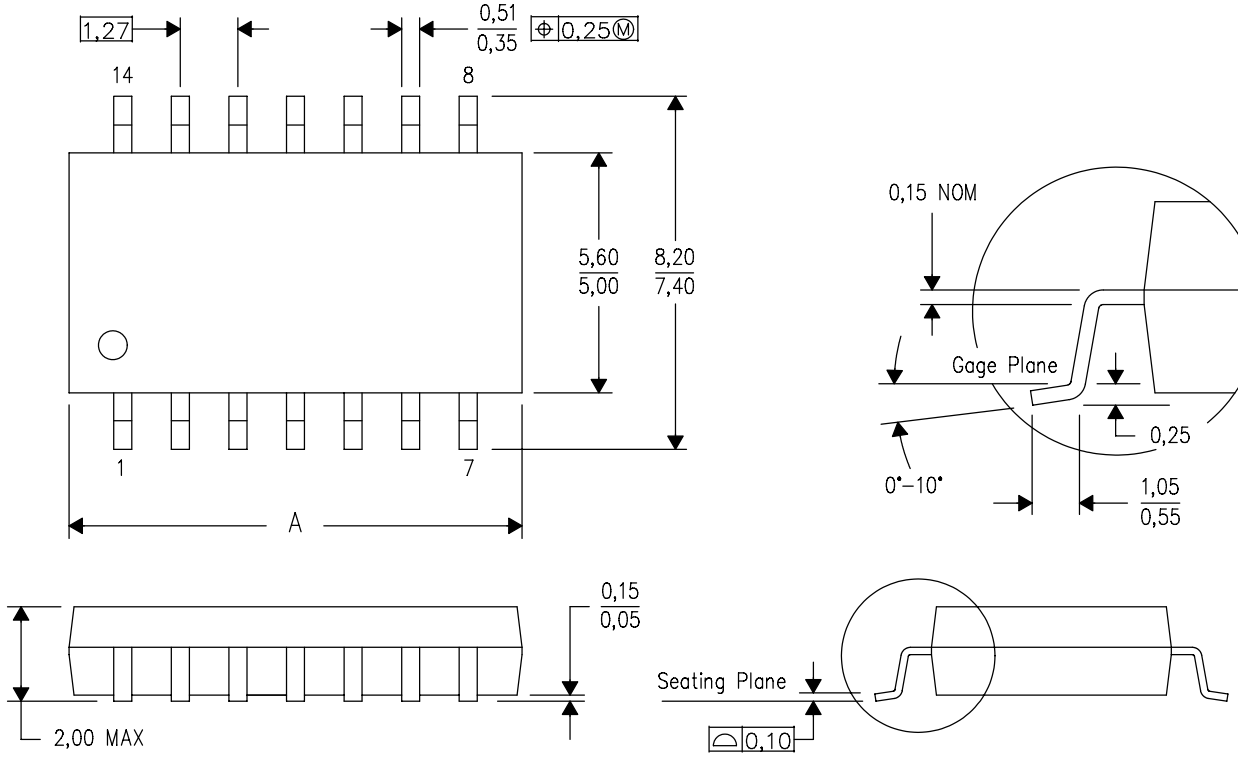
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

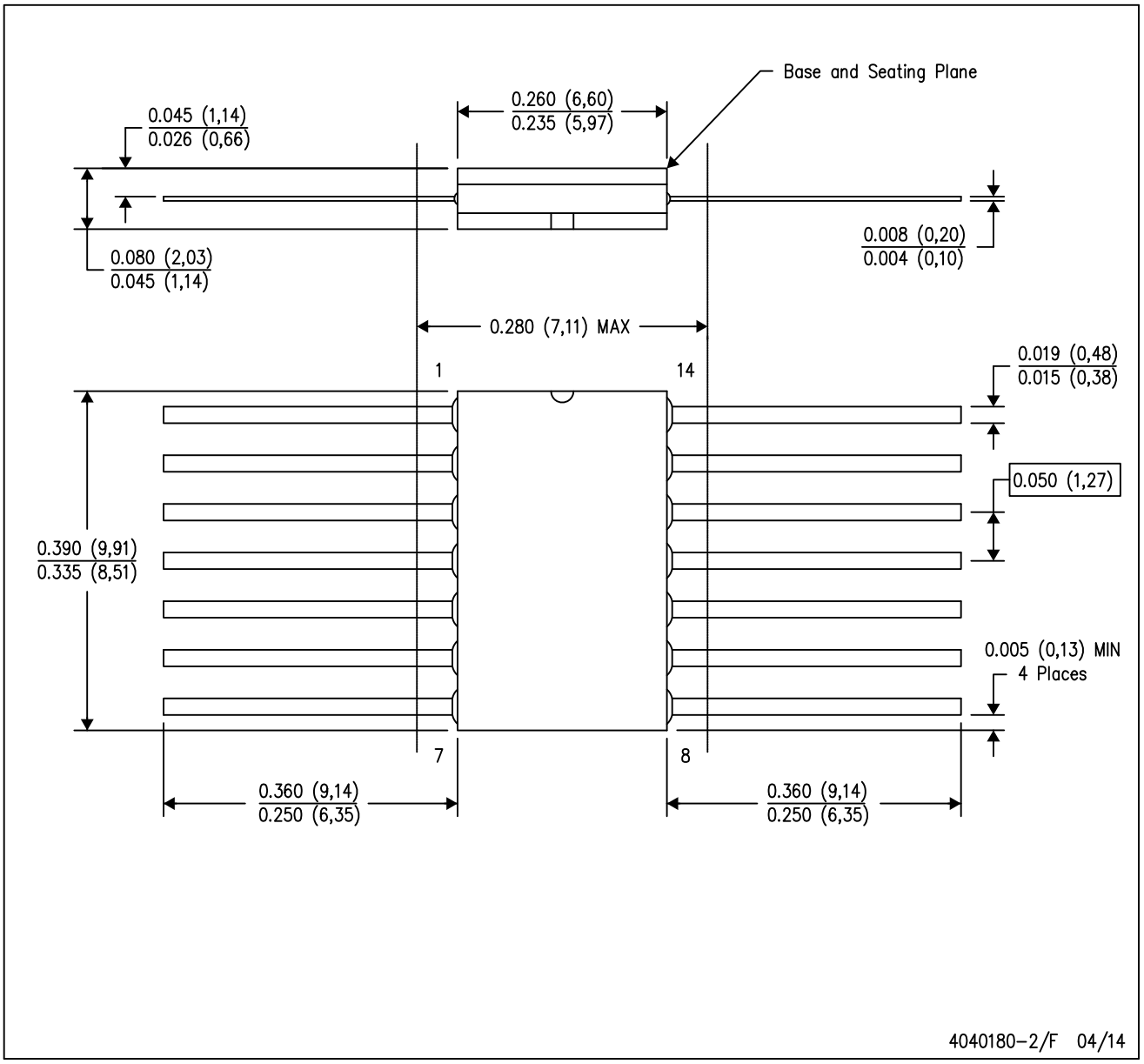


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



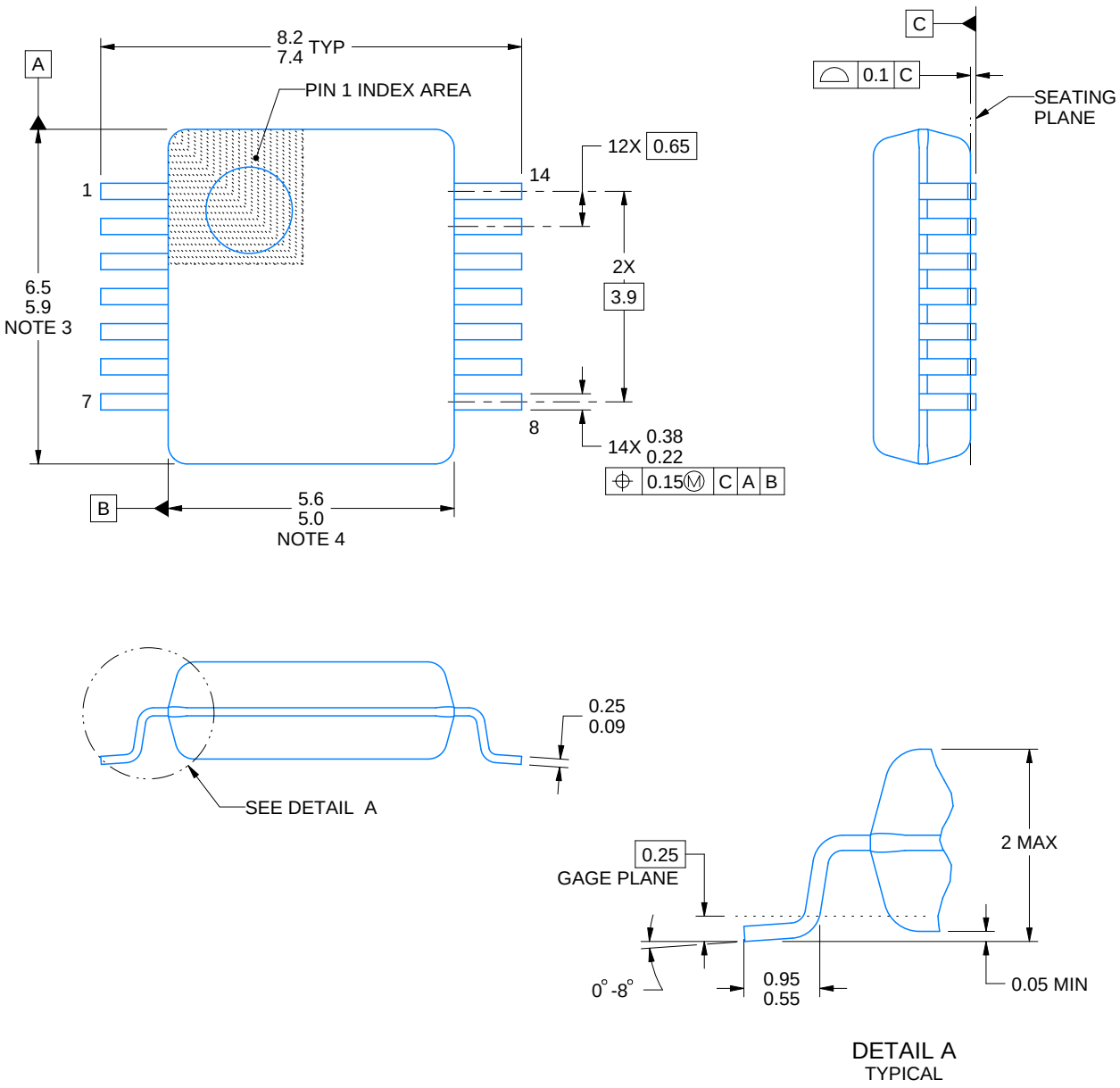
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

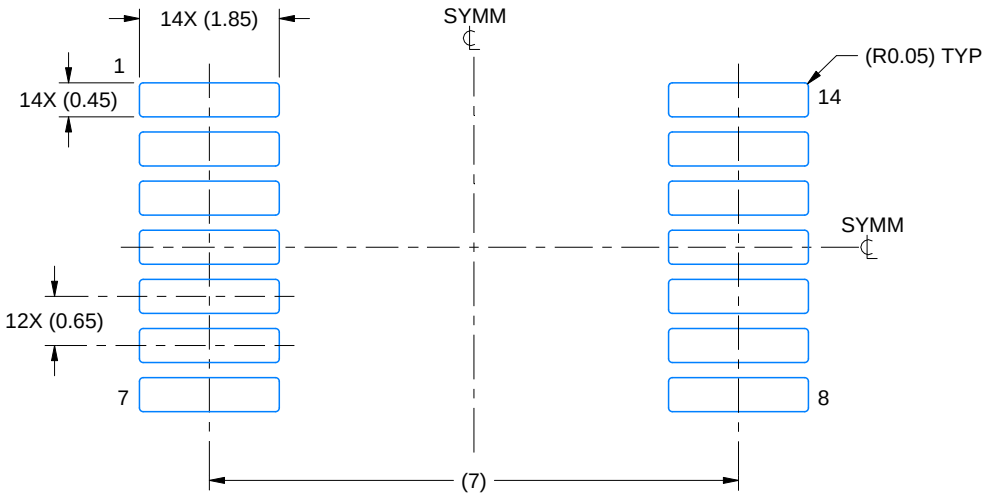
SMALL OUTLINE PACKAGE



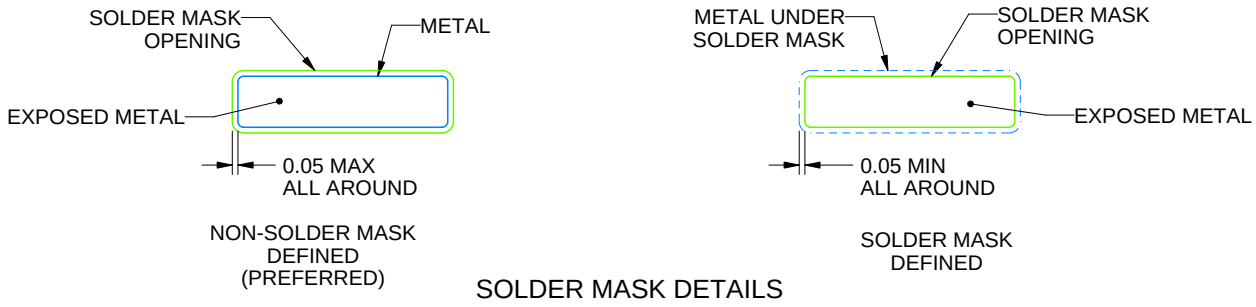
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

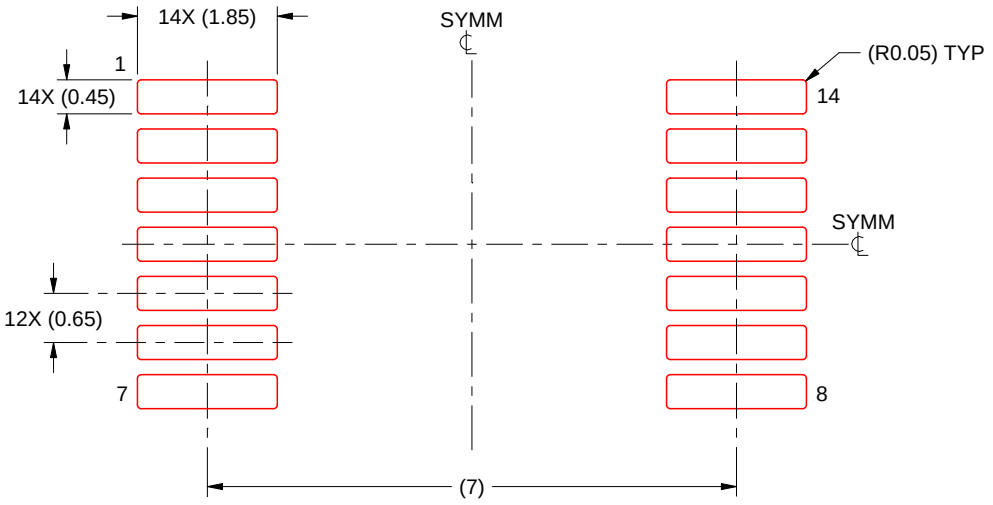


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

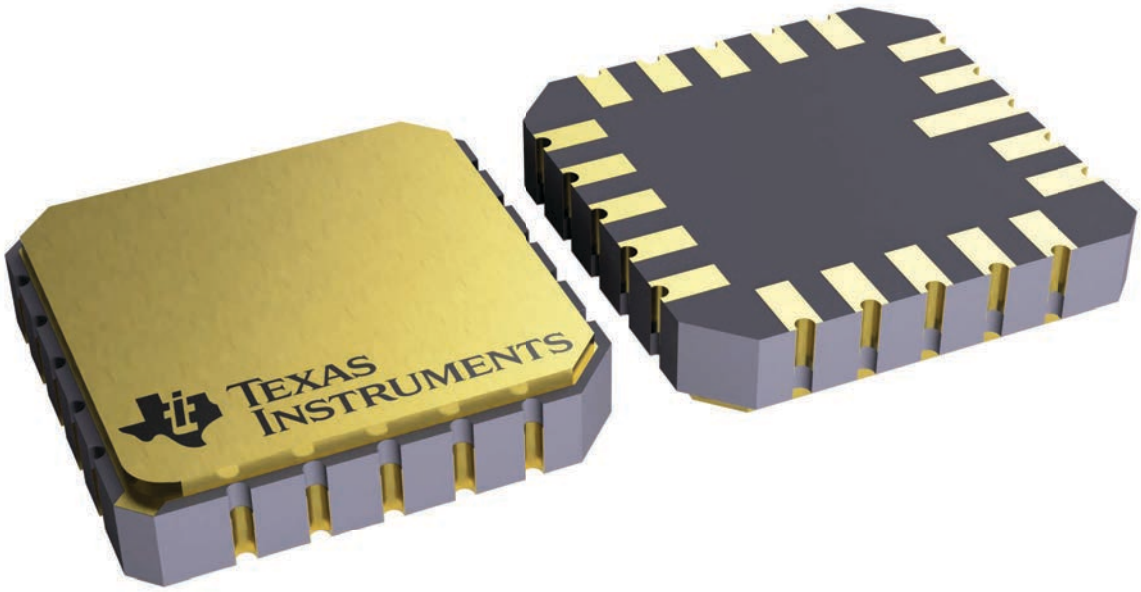
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

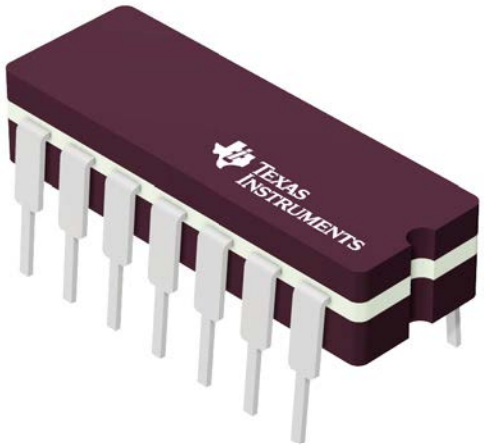


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

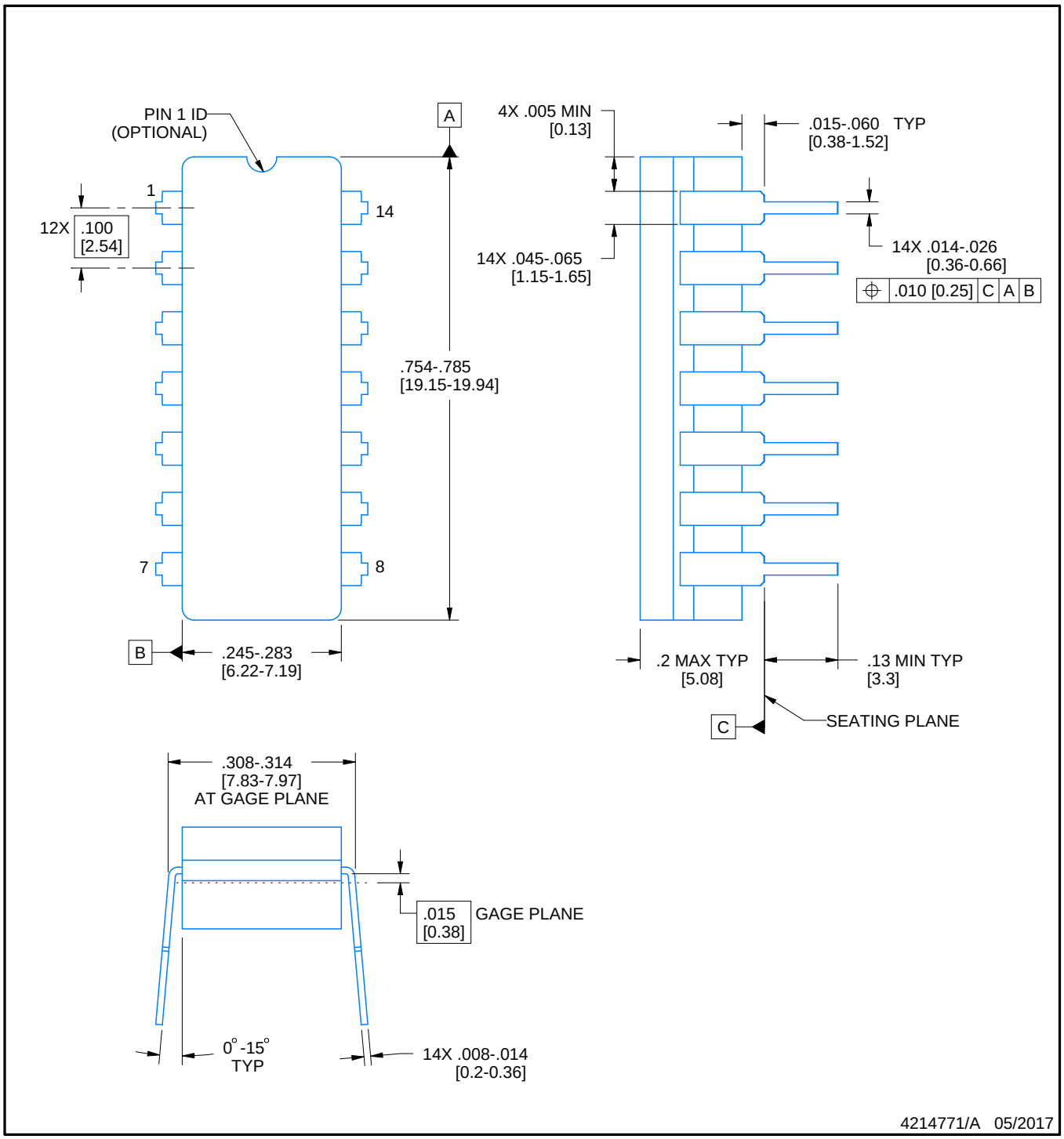


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

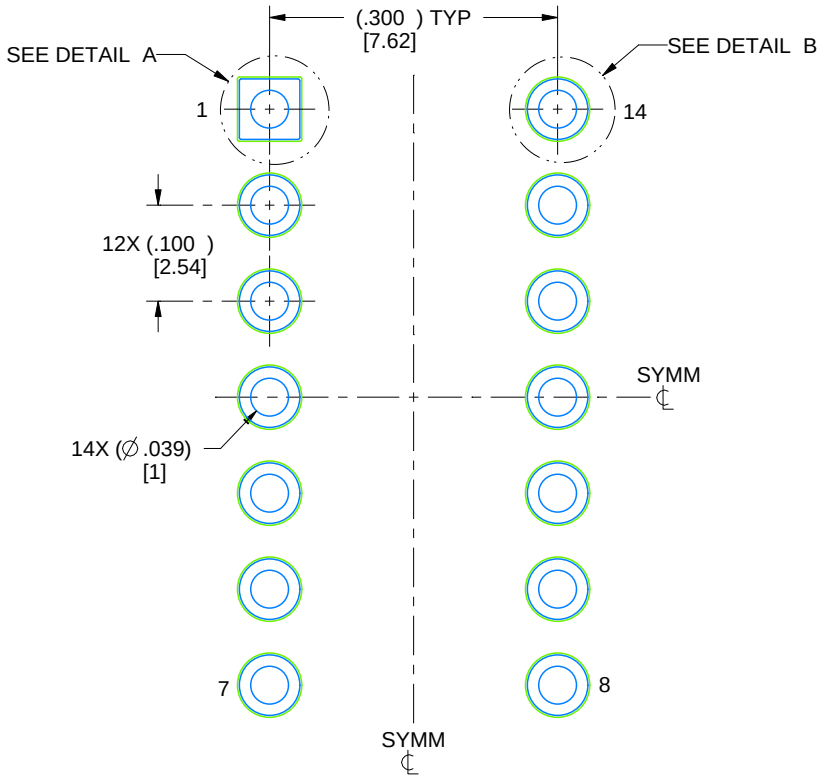
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

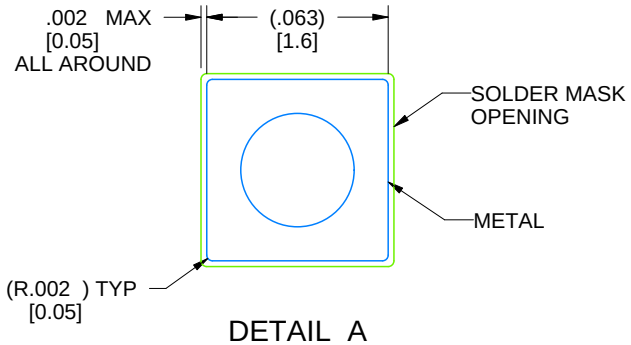
J0014A

CDIP - 5.08 mm max height

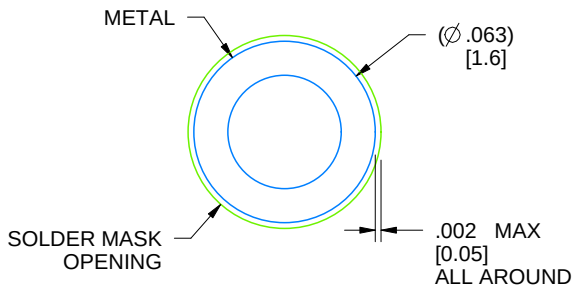
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



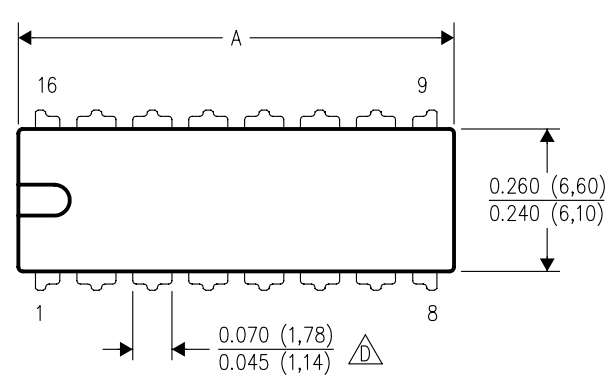
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

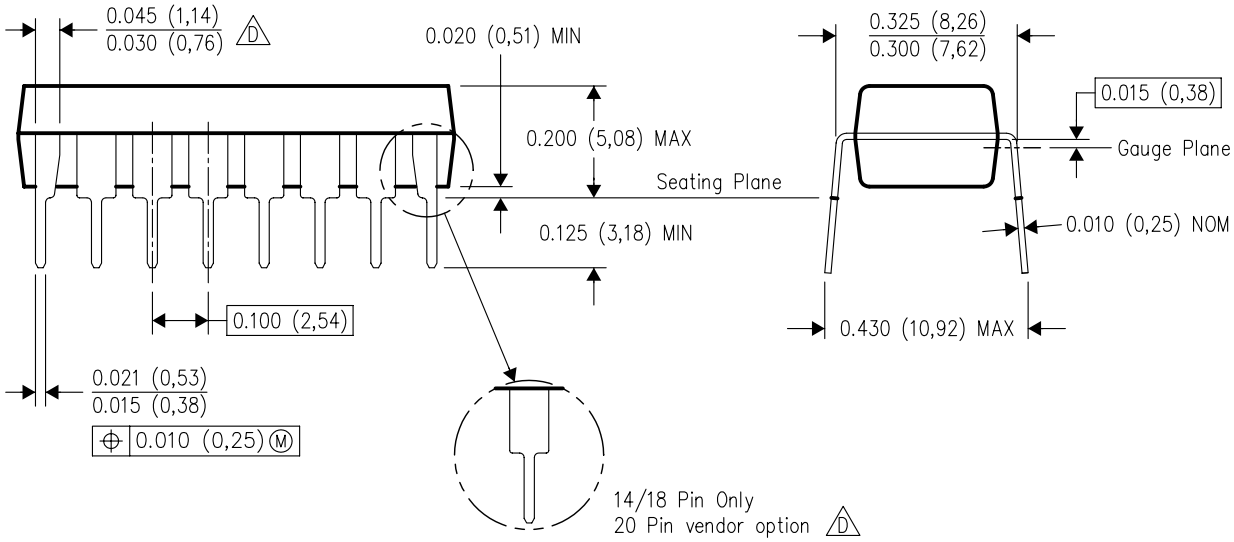
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

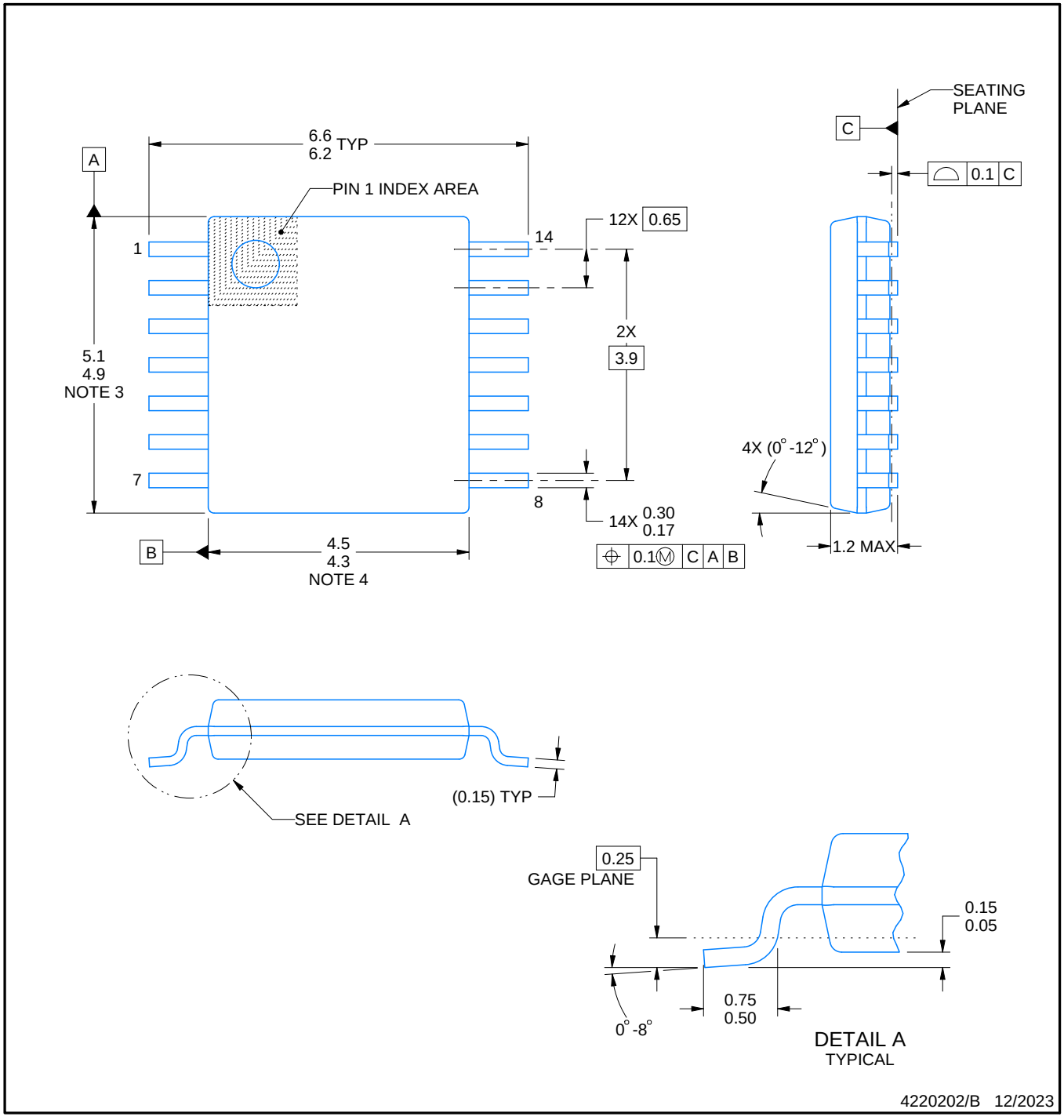
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

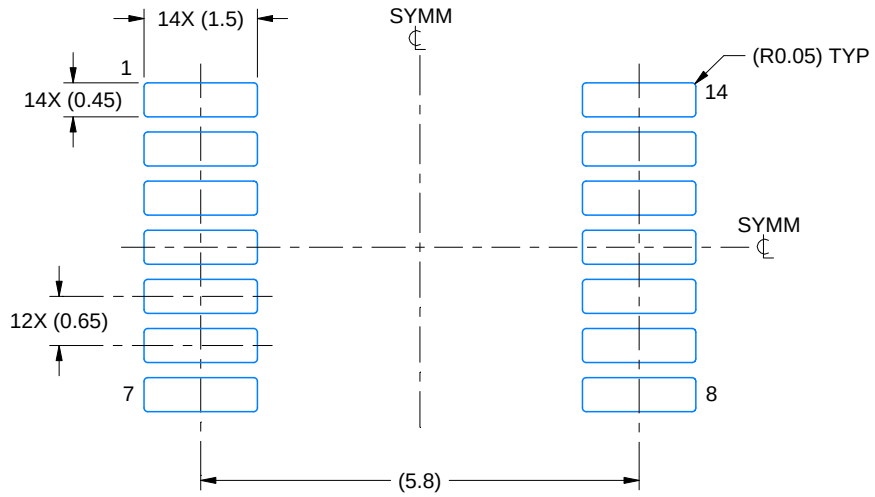
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

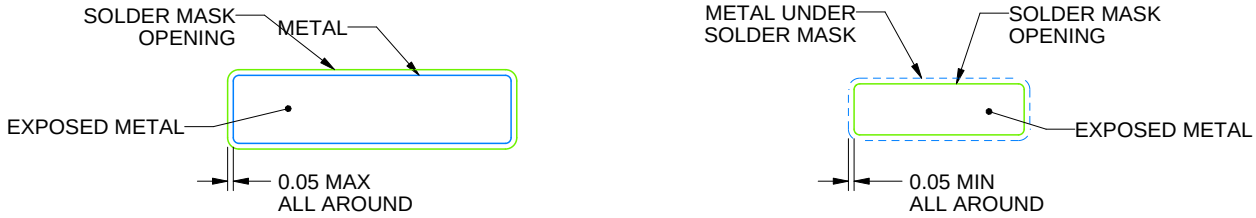


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

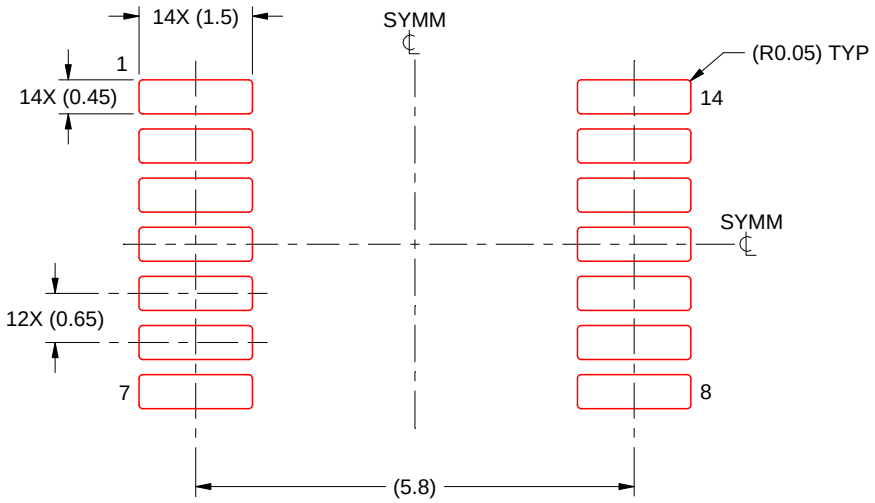


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月