LED Drivers for LCD Backlights

1ch Boost up Type White LED Driver for large LCD

BD9411F

General Description

BD9411F is a high efficiency driver for white LEDs and is designed for large LCDs. BD9411F has a boost DCDC converter that employs an array of LEDs as the light source.

BD9411F has some protect functions against fault conditions, such as over-voltage protection (OVP), over current limit protection of DCDC (OCP), LED OCP protection, and over-boost protection (FBMAX).

Therefore it is available for the fail-safe design over a wide range output voltage.

Key Specifications

- Operating power supply voltage range: 9.0V to 35.0V
- Oscillator frequency of DCDC: 150kHz (RT=100kΩ)
- Operating Current: 3.3 mA(Typ)
- Operating temperature range: -40°C to +105°C

Package(s) W(Typ) x D(Typ) x H(Max)

SOP18 11.20mm x 7.80mm x 2.01mm

Pin pitch 1.27mm

Features

- DCDC converter with current mode
- LED protection circuit (Over boost protection, LED OCP protection)
- Over-voltage protection (OVP) for the output voltage V_{OUT}
- Adjustable soft start
- Adjustable oscillation frequency of DCDC
- Wide range of analog dimming 0.2V to 3.0V
- UVLO detection for the input voltage of the power stage
- LED Dimming PWM Over Duty Protection(ODP)



Figure 1. SOP18

Applications

- TV, Computer Display, LCD Backlighting

Typical Application Circuit

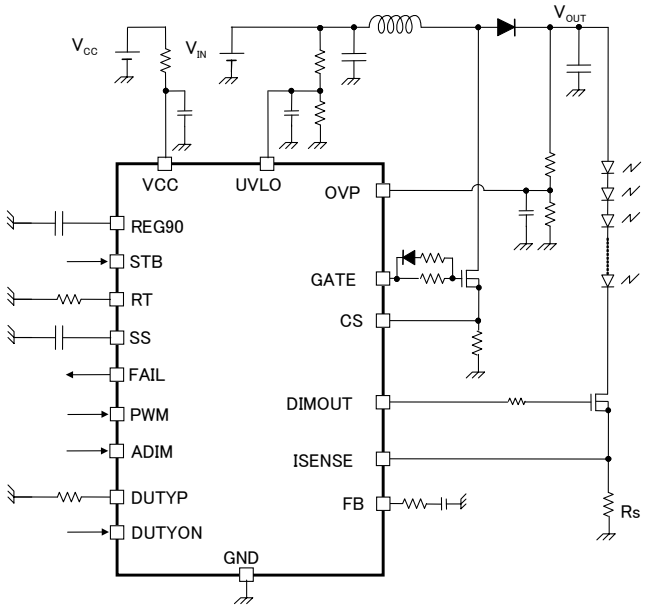


Figure 2. Typical Application Circuit

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Pin Configuration(s)

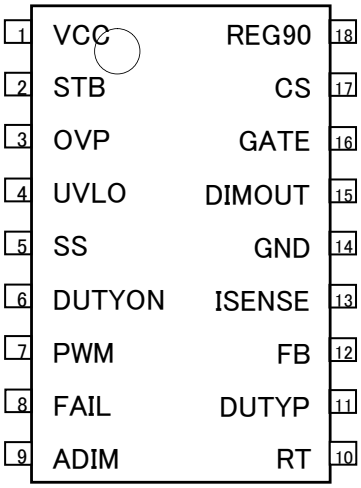


Figure 3. Pin Configuration

Pin Description(s)

No.	Terminal Name	Function
1	VCC	Power supply pin
2	STB	IC ON/OFF pin
3	OVP	Over voltage protection detection pin
4	UVLO	Under voltage lock out detection pin
5	SS	Soft start setting pin
6	DUTYON	Over Duty Protection ON/OFF pin
7	PWM	External PWM dimming signal input pin
8	FAIL	Error detection output pin
9	ADIM	ADIM signal input pin
10	RT	DC/DC switching frequency setting pin
11	DUTYP	Over Duty Protection setting pin
12	FB	Error amplifier output pin
13	ISENSE	LED current detection input pin
14	GND	-
15	DIMOUT	Dimming signal output for NMOS
16	GATE	DC/DC switching output pin
17	CS	DC/DC output current detect pin, OCP input pin
18	REG90	9.0V output voltage pin

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Block Diagram(s)

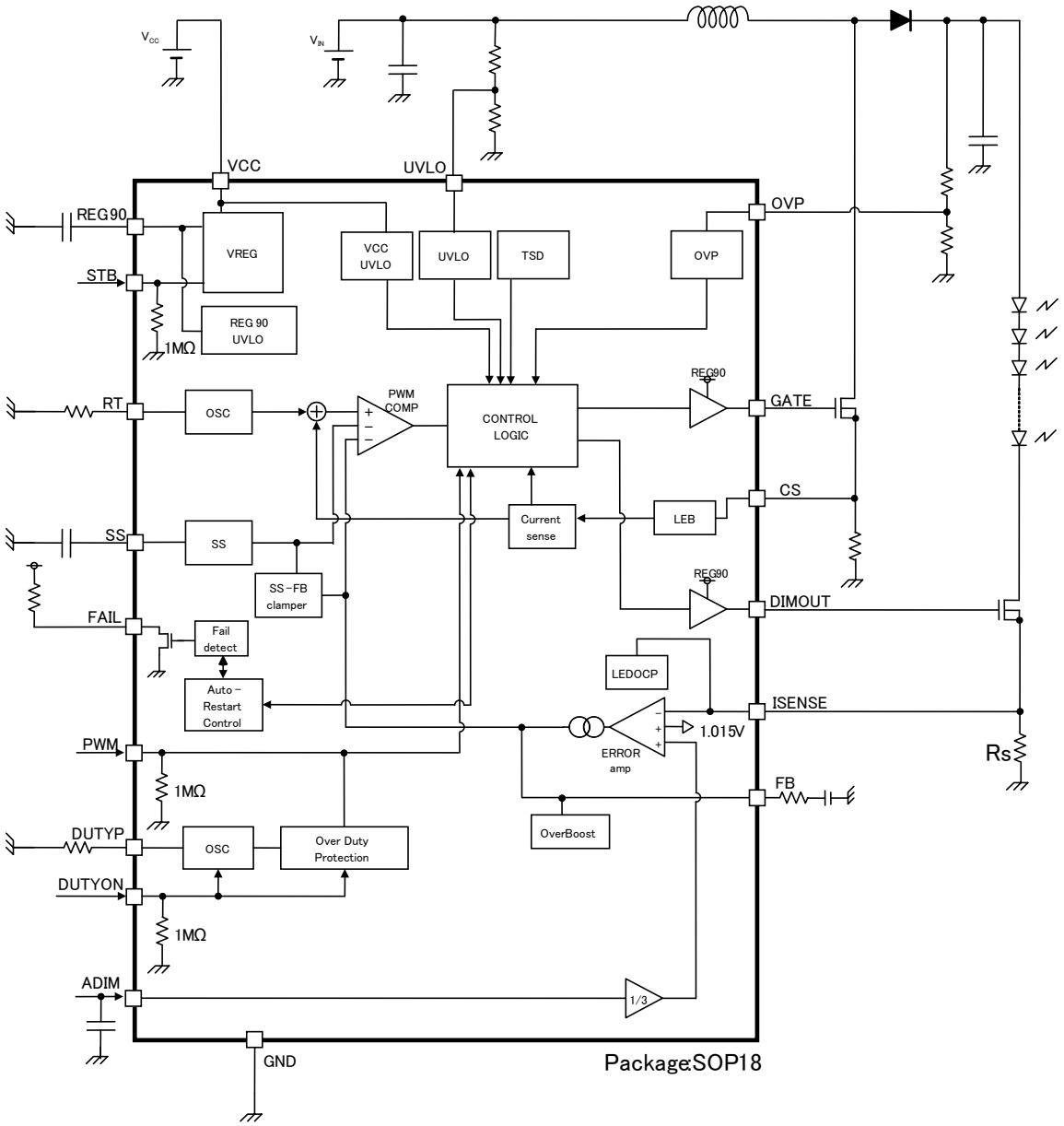


Figure 4. Block Diagram

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Absolute Maximum Ratings (Tj=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VCC	-0.3 to +36	V
SS, RT, ISENSE, FB, CS, DUTYP Pin Voltage	SS, RT, ISENSE, FB, CS, DUTYP	-0.3 to +7	V
REG90, DIMOUT, GATE Pin Voltage	REG90, DIMOUT, GATE	-0.3 to +13	V
OVP, UVLO, PWM, ADIM, STB, FAIL, DUTYON Pin Voltage	OVP, UVLO, PWM, ADIM, STB, FAIL, DUTYON	-0.3 to +20	V
Operating Temperature Range	Topr	-40 to +105	°C
Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Thermal Resistance[*(Note 1)*]

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s[*(Note 3)*]	2s2p[*(Note 4)*]	
SOP18				
Junction to Ambient	θ_{JA}	179.3	119.9	°C/W
Junction to Top Characterization Parameter[*(Note 2)*]	Ψ_{JT}	20.0	17.0	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air)
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 3)*Using a PCB board based on JESD51-3.
*(Note 4)*Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Recommended Operating Ranges

Parameter	**Symbol**	**Range**	**Unit**
Power Supply Voltage	VCC	9.0 to 35.0	V
DC/DC Oscillation Frequency	fsw	50 to 1000	kHz
Effective Range of ADIM Signal	VADIM	0.2 to 3.0	V
PWM Input Frequency	FPWM	90 to 2000	Hz

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Electrical Characteristics (Unless otherwise specified V_{CC}=24V Tj=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
【Total Current Consumption】						
Circuit Current	I_{CC}	−	3.3	6.6	mA	V_{STB}=3.0V, PWM=3.0V
Circuit Current (standby)	I_{ST}	−	40	80	μA	V_{STB}=0V
【UVLO Block】						
Operation Voltage（V_{CC}）	V_{UVLO_VCC}	6.5	7.5	8.5	V	V_{CC}=SWEEP UP
Hysteresis Voltage（V_{CC}）	V_{UHYS_VCC}	150	300	600	mV	V_{CC}=SWEEP DOWN
UVLO Release Voltage	V_{UVLO}	2.88	3.00	3.12	V	V_{UVLO}=SWEEP UP
UVLO Hysteresis Voltage	V_{UHYS}	250	300	350	mV	V_{UVLO}=SWEEP DOWN
UVLO Pin Leak Current	I_{VUVLO_LK}	-2	0	2	μA	V_{UVLO}=4.0V
【DC/DC Block】						
ISENSE Threshold Voltage 1	V_{LED1}	0.225	0.233	0.242	V	V_{ADIM}=0.7V
ISENSE Threshold Voltage 2	V_{LED2}	0.656	0.667	0.677	V	V_{ADIM}=2.0V
ISENSE Threshold Voltage 3	V_{LED3}	0.988	1.000	1.012	V	V_{ADIM}=3.0V
ISENSE Clamp Voltage	V_{LED4}	0.990	1.015	1.040	V	V_{ADIM}=3.3V (as masking analog dimming)
Oscillation Frequency	F_{CT}	142.5	150	157.5	kHz	RT=100kΩ
RT Short Protection Range	V_{RT_DET}	-0.3	-	V_{RT} ×90%	V	RT=SWEEP DOWN
RT Terminal Voltage	V_{RT}	1.6	2.0	2.4	V	RT=100kΩ
GATE Pin MAX DUTY Output	D_{MAX_DUTY}	90	95	99	%	RT=100kΩ
GATE Pin ON Resistance (as source)	R_{ON_GSO}	2.5	5.0	10.0	Ω	
GATE Pin ON Resistance (as sink)	R_{ON_GSI}	2.0	4.0	8.0	Ω	
SS Pin Source Current	I_{SSSO}	-3.75	-3.0	-2.25	μA	V_{SS}=2.0V
SS Pin ON Resistance at OFF	R_{SS_L}	-	3.0	5.0	kΩ	
Soft Start Ended Voltage	V_{SS_END}	3.52	3.70	3.88	V	SS=SWEEP UP
【DC/DC Block】						
FB Source Current	I_{FBSO}	-115	-100	-85	μA	V_{ISENSE}=0.2V, V_{ADIM}=3.0V, V_{FB}=1.0V
FB Sink Current	I_{FBSI}	85	100	115	μA	V_{ISENSE}=2.0V, V_{ADIM}=3.0V, V_{FB}=1.0V
【DC/DC Protection Block】						
OCP Detect Voltage1	V_{CS1}	360	400	440	mV	CS=SWEEP UP, Pulse by pulse
OCP Detect Voltage2	V_{CS2}	0.85	1.00	1.15	V	CS=SWEEP UP
OVP Detect Voltage	V_{OVP}	2.88	3.00	3.12	V	V_{OVP} SWEEP UP
OVP Detect Hysteresis	V_{OVP_HYS}	150	200	250	mV	V_{OVP} SWEEP DOWN
OVP Pin Leak Current	I_{OVP_LK}	-2	0	2	μA	V_{OVP}=4.0V, V_{STB}=3.0V
【LED Protection Block】						
LED OCP Detect Voltage	V_{LEDOCP}	2.88	3.00	3.12	V	V_{ISENSE}=SWEEP UP
Over Boost Detection Voltage	V_{FBH}	3.84	4.00	4.16	V	V_{FB}=SWEEP UP
【Dimming Block】						
ADIM Pin Leak Current	I_{LADIM}	-2	0	2	μA	V_{ADIM}=2.0V
ISENSE Pin Leak Current	I_{L_ISENSE}	-2	0	2	μA	V_{ISENSE}=4.0V
DIMOUT Source ON Resistance	R_{ON_DIMSO}	5.0	10.0	20.0	Ω	
DIMOUT Sink ON Resistance	R_{ON_DIMSI}	4.0	8.0	16.0	Ω	
【REG90 Block】						
REG90 Output Voltage 1	V_{REG90_1}	8.91	9.00	9.09	V	I_O=0mA
REG90 Output Voltage 2	V_{REG90_2}	8.865	9.00	9.135	V	I_O=-15mA
REG90 Available Current	$\lvert I_{REG90} \rvert$	15	-	-	mA	
REG90_UVLO Detect Voltage	V_{REG90_TH}	5.22	6.00	6.78	V	V_{REG90}=SWEEP DOWN, V_{STB}=0V
REG90 Discharge Resistance	V_{REG90_DIS}	13.2	22.0	30.8	kΩ	STB=ON->OFF, V_{REG90}=8.0V, PWM=L

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Electrical Characteristics (Unless otherwise specified V_{CC}=24V Tj=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
【STB Block】						
STB Pin HIGH Voltage	V_{STBH}	2.0	-	18	V	
STB Pin LOW Voltage	V_{STBL}	-0.3	-	0.8	V	
STB Pull Down Resistance	R_{STB}	600	1000	1400	kΩ	V_{STB}=3.0V
【PWM Block】						
PWM Pin HIGH Voltage	V_{PWM_H}	1.5	-	18	V	
PWM Pin LOW Voltage	V_{PWM_L}	-0.3	-	0.8	V	
PWM Pin Pull Down Resistance	R_{PWM}	600	1000	1400	kΩ	V_{PWM}=3.0V
【DUTYON Block】						
DUTYON Pin HIGH Voltage	V_{DTYON_H}	1.5	-	18	V	
DUTYON Pin LOW Voltage	V_{DTYON_L}	-0.3	-	0.8	V	
DUTYON Pin Pull Down Resistance	R_{DTYON}	600	1000	1400	kΩ	V_{DUTYON}=3.0V
【Over Duty Protection Block】						
PWM ODP Protection Detect Duty	D_{ODP}	-	35	-	%	F_{PWM}=120Hz, DUTYP=341kΩ
DUTYP Short Protection Range	V_{DTYP_DET}	-0.3	-	V_{DUTYP} ×90%	V	DUTYP=SWEEP DOWN
DUTYP Terminal Voltage	V_{DTYP}	1.6	2.0	2.4	V	DUTYP=100kΩ
【Filter Block】						
Abnormal Detection Timer	t_{CP}	-	20	-	ms	F_{CT}=800kHz
AUTO Timer	t_{AUTO}	-	163	-	ms	F_{CT}=800kHz
【FAIL Block 】						
FAIL Pin LOW Voltage	V_{FAILL}	0.25	0.5	1.0	V	I_{FAIL}=1mA

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Typical Performance Curves (Reference data)

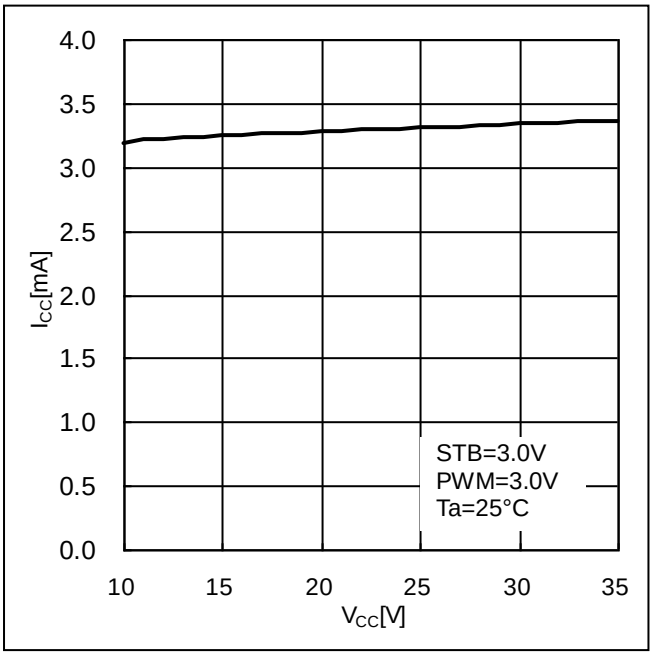


Figure 5. Operating circuit current

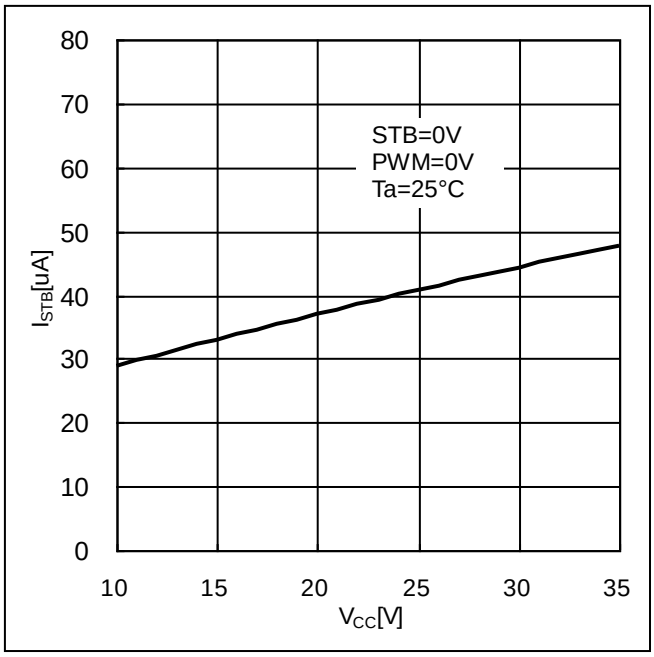


Figure 6. Standby circuit current

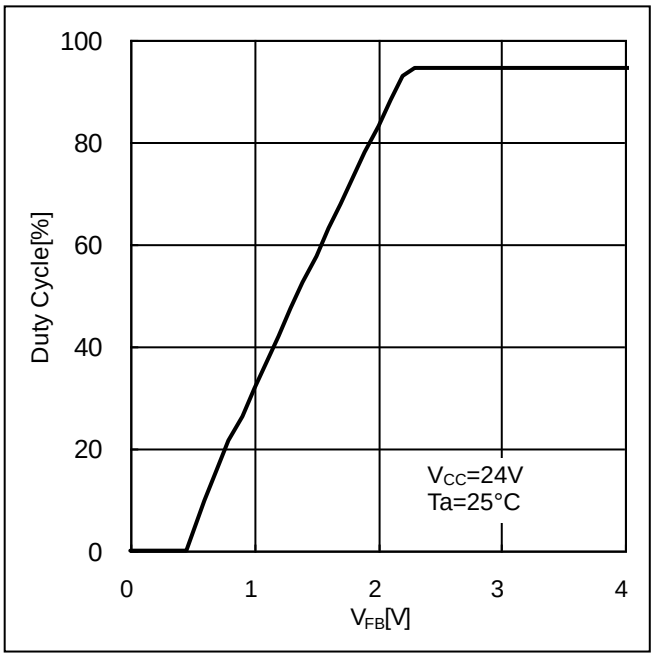


Figure 7. Duty cycle vs FB character

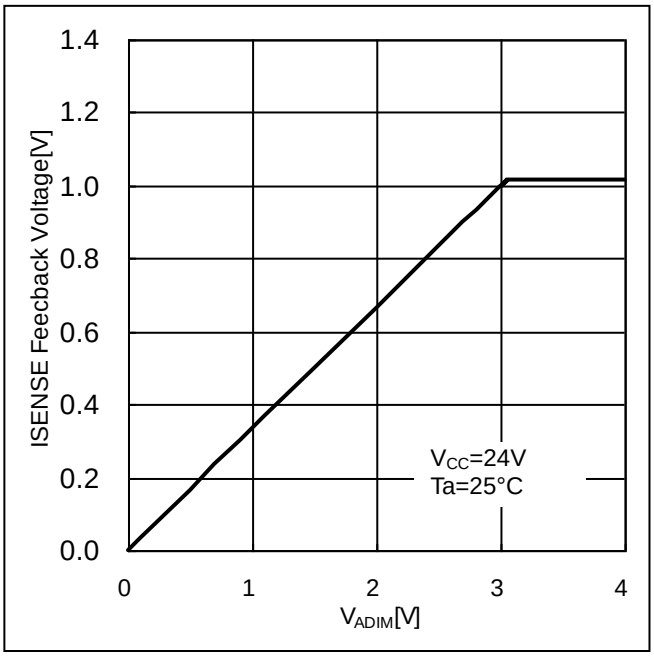


Figure 8. ISENSE feedback voltage vs ADIM character

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Pin Descriptions

○Pin 1: VCC

This is the power supply pin of the IC. Input range is from 9V to 35V.
The operation starts at more than 7.5V(Typ) and shuts down at less than 7.2V(Typ).

○Pin 2: STB

This is the ON/OFF setting terminal of the IC.
At startup, internal bias starts at high level, and then PWM DCDC boost starts after PWM rise edge inputs.
Note: IC status (IC ON/OFF) transits depending on the voltage inputted to STB terminal. Avoid the use of intermediate level (from 0.8V to 2.0V).

○Pin 3: OVP

The OVP terminal is the input for over-voltage protection. If OVP is more than 3.0V(Typ), the over-voltage protection (OVP) will work. At the moment of these detections, it sets GATE=L, DIMOUT=L and starts to count up the abnormal interval. If OVP detection continued to count four GATE clocks, IC's operation will be stop. (Please refer to "OVP Detection" Timing Chart on Page26)
The OVP pin is high impedance, because the internal resistance is not connected to a certain bias.
Even if OVP function is not used, pin bias is still required because the open connection of this pin is not a fixed potential.
The setting example is separately described in the ”OVP Setting" section on Page16.

○Pin 4: UVLO

Under Voltage Lock Out pin is the input voltage of the power stage. , IC starts the boost operation if UVLO is more than 3.0V(Typ) and stops if lower than 2.7V(Typ).
The UVLO pin is high impedance, because the internal resistance is not connected to a certain bias.
Even if UVLO function is not used, pin bias is still required because the open connection of this pin is not a fixed potential.
The setting example is separately described in the ”UVLO Setting" section on Page15

○Pin 5: SS

This is the pin which sets the soft start interval of DC/DC converter. It performs the constant current charge of 3.0 μA(Typ) to external capacitance Css. The switching duty of GATE output will be limited during 0V to 3.7V(Typ) of the SS voltage.
So the soft start interval Tss can be expressed as follows

$$T_{SS} = 1.23 \times 10^{6} \times C_{SS}[\mathrm{sec}]$$ **C_{SS}: the external capacitance of the SS pin**.

The logic of SS pin asserts low is defined as the DC/DC operation stop state after protection function or PWM is not input high level after STB reset release. When SS capacitance is under 1nF, take note if the in-rush current during startup is too large, or if over boost detection (FBMAX) mask timing is too short.
Please refer to soft start behavior in the “Timing Chart" section on Page13.

○Pin 6: DUTYON

This is the ON/OFF setting terminal of the LED PWM Over Duty Protection (ODP). By adjusting DUTYON input voltage, it is ON/OFF of the ODP adjusted.

State	DUTYON input voltage
ODP=ON	DUTYON= −0.3V to +0.8V
ODP=OFF	DUTYON= 1.5V to 18.0V

○Pin 7: PWM

This is the PWM dimming signal input terminal. The high / low level of PWM pins are the following.

State	PWM input voltage
PWM=H	PWM= 1.5V to 18.0V
PWM=L	PWM= -0.3V to +0.8V

○Pin 8: FAIL

This is FAIL signal output (OPEN DRAIN) pin. At normal operation, NMOS will be in ON (500 ohm Typ) state, during abnormality detection NMOS will be in OPEN state (OFF).

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○Pin 9: ADIM

This is the input pin for analog dimming signal. The ISENSE feedback point is set as 1/3 of this pin bias. If more than 3.0V(Typ) is input, ISENSE feedback voltage is clamped to limit to flow LED large current. In this condition, the input current is caused. Please refer to <ISENSE> terminal explanation.

○Pin 10: RT

This is the DC/DC switching frequency setting pin. DCDC frequency is decided by connected resistor.

○The relationship between the frequency and RT resistance value **(ideal)**

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

The oscillation setting ranges from 50kHz to 1000kHz.
The setting example is separately described in the ”DCDC Oscillation Frequency Setting” section on Page15

○Pin 11: DUTYP

This is the ODP setting pin. The ODP (Over Duty Protection) is the function to limit DUTY of LED PWM frequency f_{PWM} by ODP detection Duty (ODP_{duty}) set by resistance (R_{DUTY}) connected to DUTYP pin.

○Relationship between LED PWM frequency f_{PWM}, ODP Detection Duty and DUTYP resistance (ideal)

$$R_{DUTYP} = \frac{1172 \times ODP_{duty}[\%]}{f_{PWM}[Hz]} \quad [k\Omega]$$

The R_{DUTYP} setting ranges from 15kΩ to 1MΩ.
The setting example is separately described in the ”ODP Setting” section on Page16.

○Pin 12: FB

This is the output terminal of error amplifier.
FB pin rises with the same slope as the SS pin during the soft-start period.
After soft -start completion (SS>3.7V(Typ)), it operates as follows.

When PWM=H, it detects ISENSE terminal voltage and outputs error signal compared to analog dimming signal (ADIM).
When PWM=L, IC holds the OVP voltage at the edge of PWM=H to L, and operates to hold the adjacent voltage. Please refer to “Timing Chart” section

It detects over boost (FBMAX) over FB=4.0V(Typ). After the SS completion, if FB>4.0V and PWM=H continues 4clk GATE, the CP counter starts. After that, only the FB>4.0V is monitored, When CP counter reaches 16384clk (2^{14}clk), IC's operation will be stop. (Please refer to “Timing Chart” section on Page27.)

The loop compensation setting is described in section "Loop Compensation" on Page21.

○Pin 13: ISENSE

This is the input terminal for the current detection. Error amplifier compares ISENSE voltage and the lower voltage between 1/3 of the ADIM (analog dimming terminal) voltage and 1.015V(Typ) for FB voltage control.
And this terminal detects abnormal LED's over-current when ISENSE voltage continues over 3.0V(Typ) during 4CLKs (equivalent to 40us at f_{osc} = 100kHz), DC/DC operation becomes stop. (Please refer to “Timing Chart” section on Page 28.)

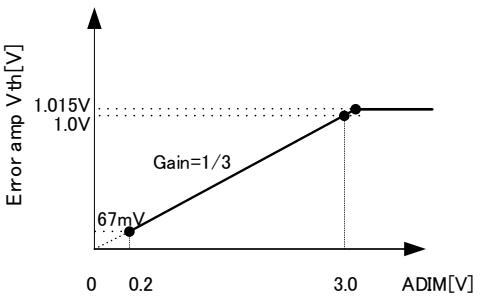


Figure 9. Relationship of the feedback voltage and ADIM

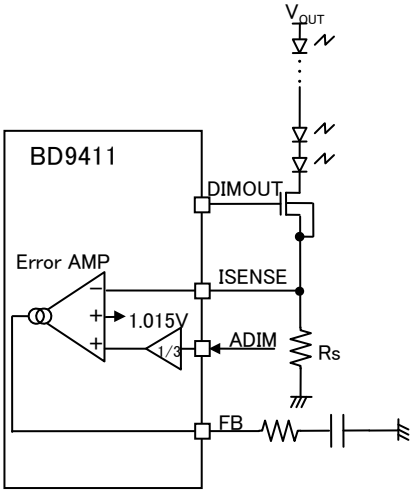


Figure 10. ISENSE terminal circuit example

○Pin 14: GND

This is the GND pin of the IC.

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○Pin 15: DIMOUT

This is the output pin for external dimming NMOS. The table below shows the rough output logic of each operation state, and the output H level is REG90. Please refer to “Timing Chart” section for detailed explanations, because DIMOUT logic has an exceptional behavior. Please insert the resistor R_{DIM} between the dimming MOS gate to improve the over shoot of LED current, as PWM turns from low to high.

Status	DIMOUT output
Normal	Same logic to PWM
Abnormal	GND Level

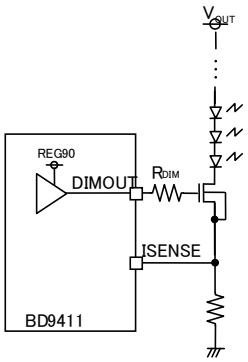


Figure 11. DIMOUT terminal circuit example

○Pin 16: GATE

This is the output terminal for driving the gate of the boost MOSFET. The high level is REG90. Frequency can be set by the resistor connected to RT. Refer to <RT> pin description for the frequency setting.

○Pin 17: CS

The CS pin has two functions.

1. DC / DC current mode Feedback terminal

The inductor current is converted to the CS pin voltage by the sense resistor R_{CS}. This voltage compared to the voltage set by error amplifier controls the output pulse.

2. Inductor current limit (OCP) terminal

The CS terminal also has an over current protection (OCP). If the voltage is more than 0.4V(Typ), the switching operation will be stopped compulsorily. And the next boost pulse will be restarted to normal frequency.
In addition, the CS voltage is more than 1.0V(Typ) during 4CLKs GATE operation, IC operation will be stop. As above OCP operation, if the current continues to flow nevertheless GATE=L because of the destruction of the boost MOS, IC will stops the operation completely.

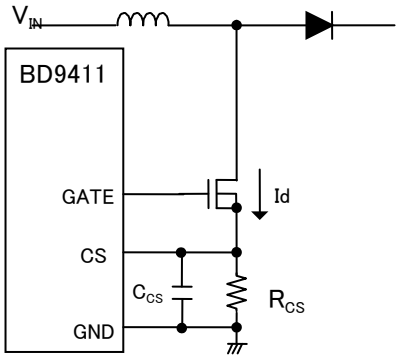


Figure 12. CS terminal circuit example

Both of the above functions are enabled after 300ns (Typ) when GATE pin asserts high, because the Leading Edge Blanking function (LEB) is included into this IC to prevent the effect of noise.
Please refer to “OCP Setting / Calculation Method for the Current Rating of DCDC Parts” section on Page18, for detailed explanation.
If the capacitance C_{CS} in the right figure is increased to a micro order, please be careful that the limited value of NMOS drain current Id is more than the simple calculation. Because the current Id flows not only through R_{CS} but also through C_{CS}, as the CS pin voltage moves according to Id.

○Pin 18: REG90

This is the 9.0V(Typ) output pin. Available current is 15mA (min).
The characteristic of V_{CC} line regulation at REG90 is shown as figure. V_{CC} must be used in more than 10.5V for stable 9V output.
Please place the ceramic capacitor connected to REG90 pin (1.0μF to 10μF) closest to REG90-GND pin.

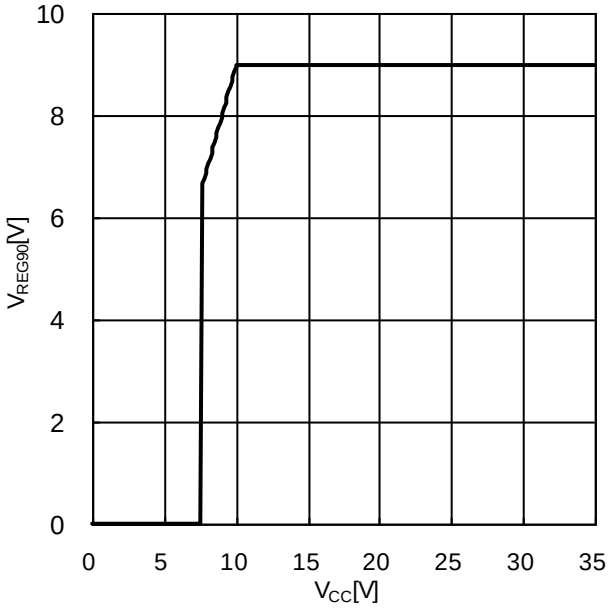


Figure 13. REG90 line regulation

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List of The Protection Function Detection Condition (Typ Condition)

Protect function	Detection pin	Detect condition			Release condition	Timer operation	Protection Type
		Detection condition	PWM	SS			
FBMAX	FB	FB > 4.0V	H(4clk)	SS>3.7V	FB < 4.0V	2^{14}clk	Immediately auto-restart after detection (Judge periodically whether normal or not)
LED OCP	ISENSE	ISENSE > 3.0V	-	-	ISENSE < 3.0V	4clk	Immediately auto-restart after detection (Judge periodically whether normal or not)
RT GND SHORT	RT	RT<VRT×90%	-	-	Release RT=GND	NO	Restart by release
RT HIGH SHORT	RT	RT>5V	-	-	Release RT=HIGH	NO	Restart by release
UVLO	UVLO	UVLO<2.7V	-	-	UVLO>3.0V	NO	Restart by release
REG90UVLO	REG90	REG90<6.0V	-	-	REG90>6.5V	NO	Restart by release
VCCUVLO	VCC	VCC<7.2V	-	-	VCC>7.5V	NO	Restart by release
OVP	OVP	OVP>3.0V	-	-	OVP<2.8V	4clk	Immediately auto-restart after detection (Judge periodically whether normal or not)
OCP	CS	CS>0.4V	-	-	-	NO	Pulse by pulse
OCP detection2	CS	CS>1.0V	-	-	CS<1.0V	4clk	Immediately auto-restart after detection (Judge periodically whether normal or not)
DUTYP GND SHORT	DUTYP	DUTYP <VDUTYP×90%	-	-	Release DUTYP=GND	NO	Restart by release
DUTYP HIGH SHORT	DUTYP	DUTYP >5V	-	-	Release DUTYP=HIGH	NO	Restart by release
ODP(*1)	PWM	DUTYON=H and PWM on duty > setting duty by DUTYP resistor	H	-	-	NO	Cycle by cycle

To reset the FBMAX, LED OCP, OVP and OCP detection2 protection, please set STB logic to 'L' once. Otherwise the detection of VCCUVLO, REG90UVLO is required.
The clock number of timer operation corresponds to the boost pulse clock.
(*1) When PWM Duty count start, PWM=H → L is input, when PWM=L → H is input, the ODP is reset.
The GATE output, the DIMOUT output maintain L until PWM=H → L is input in PWM = 100% again when ODP works once.

List of The Protection Function Operation

Protect function	Operation of the protect function			
	DC/DC gate output	Dimming transistor (DIMOUT) logic	SS pin	FAIL pin
FBMAX	Stop after timer operation	Low after timer operation	Discharge after timer operation	High after timer operation
LED OCP	Stop immediately	Immediately high, Low after timer operation	Discharge after timer operation	High after timer operation
RT GND SHORT	Stop immediately	Immediately low	Not discharge	Low
RT HIGH SHORT	Stop immediately	Immediately low	Not discharge	Low
STB	Stop immediately	Low after REG90UVLO detects	Discharge immediately	Low
UVLO	Stop immediately	Immediately low	Discharge immediately	Low
REG90UVLO	Stop immediately	Immediately low	Discharge immediately	Low
VCC UVLO	Stop immediately	Immediately low	Discharge immediately	Low
OVP	Stop immediately	Immediately low	Discharge after timer operation	Low
OCP	Stop immediately	Normal operation	Not discharge	Low
OCP detection2	Stop after timer operation	Low after timer operation	Discharge after timer operation	High after timer operation
DUTYP GND SHORT	Stop immediately	Immediately low	Not discharge	Low
DUTYP HIGH SHORT	Stop immediately	Immediately low	Not discharge	Low
ODP	Immediately low	Immediately low	Not discharge	Low

Please refer to "Timing Chart" section for details.

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Application Circuit Example

Introduce an example application using the BD9411F.

- **Basic Application Example**

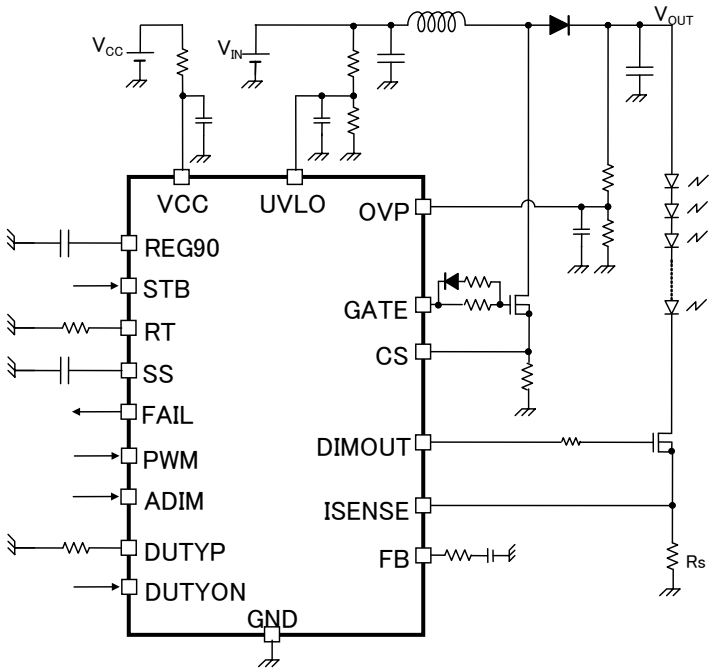


Figure 14. Basic application example

- **Analog Dimming or PWM Dimming Examples**

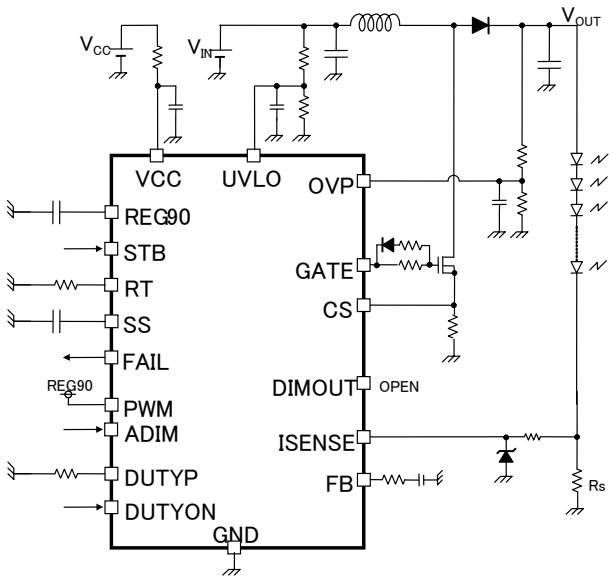


Figure 15. Example circuit for analog dimming

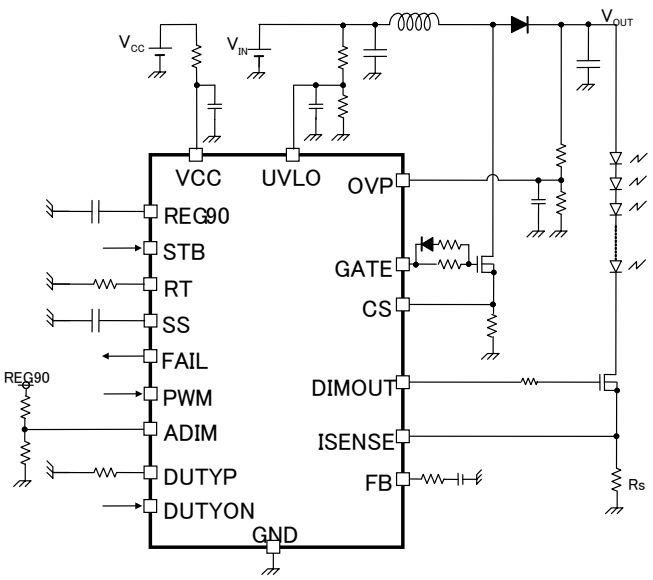


Figure 16. Example circuit for PWM dimming

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External Components Selection

1. Start Up Operation and Soft Start External Capacitance Setting

The below explanation is the start up sequence of this IC

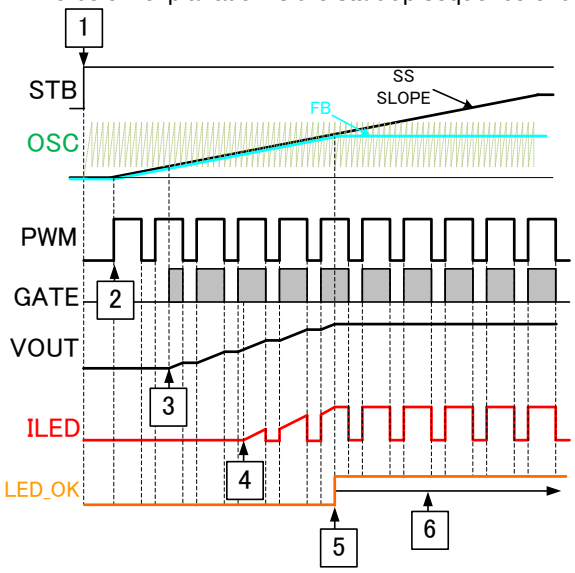


Figure 17. Startup waveform

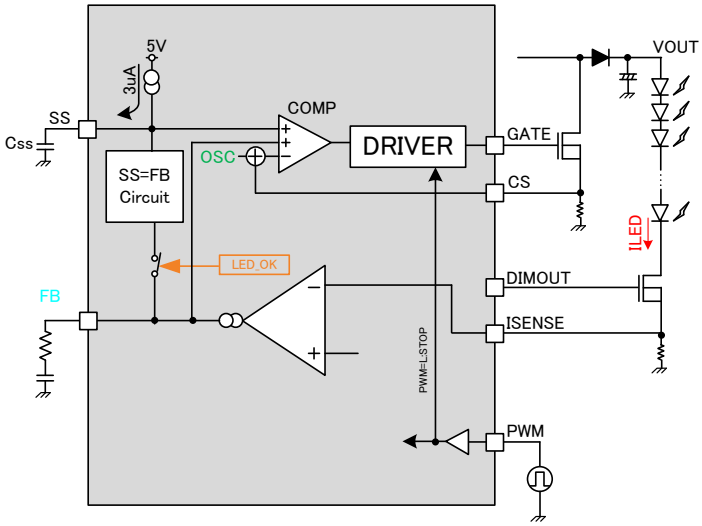


Figure 18. Circuit behavior at startup

○Explanation of start up sequence

1. Reference voltage REG90 starts by STB=H.
2. SS starts to charge at the time of first PWM=H. At this moment, the SS voltage of slow-start starts to equal FB voltage,and the circuit becomes FB=SS regardless of PWM logic.
3. When FB=SS reaches the lower point of internal sawtooth waveform, GATE terminal outputs pulse and starts to boost VOUT.
4. It boosts VOUT and VOUT reaches the voltage to be able to flow LED current.
5. If LED current flows over decided level, FB=SS circuit disconnects and startup behavior completes.
6. Then it works normal operation by feedback of ISENSE terminal. If LED current doesn't flow when SS becomes over 3.7V(Typ), SS=FF circuit completes forcibly and FBMAX protection starts.

○Method of setting SS external capacitance

According to the sequence described above, start time Tss that startup completes with FB=SS condition is the time that FB voltage reaches the feedback point.
The capacitance of SS terminal is defined as Css and the feedback voltage of FB terminal is defined as VFB. The equality on T_{FB} is as follows.

$$T_{SS} = \frac{C_{SS}[\mu F] \times VFB[V]}{3[\mu A]} \quad [sec]$$

If Css is set to a very small value, rush current flows into the inductor at startup.
On the contrary, if Css is enlarged too much, LED will light up gradually.
Since Css differs in the constant set up with the characteristic searched for and differs also by factors, such as a voltage rise ratio, an output capacitance, DCDC frequency, and LED current, please confirm with the system.

【Setting example】

When Css=0.1uF,Iss=3μA,and startup completes at VFB=3.7V, SS setting time is as follows.

$$T_{SS} = \frac{0.1 \times 10^{-6}[F] \times 3.7[V]}{3 \times 10^{-6}[A]} = 0.123 \quad [sec]$$

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2. VCC Series Resistance Setting

Here are the following effects of inserting series resistor Rvcc into V_{CC} line.
(i) In order to drop the voltage V_{CC}, it is possible to suppress the heat generation of the IC.
(ii) It can limit the inflow current to V_{CC} line.
However, if resistance R_{VCC} is set bigger, V_{CC} voltage becomes under minimum operation voltage (V_{CC}<9V). RVCC must be set to an appropriate series resistance.

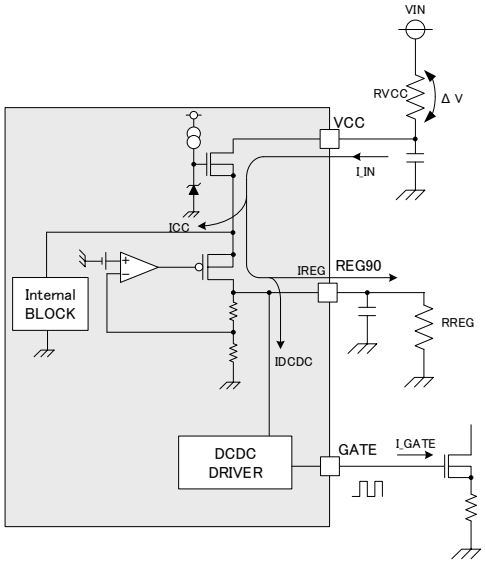


Figure 19. VCC series resistance circuit example

IC's inflow current line I_IN has the following inflow lines.
・IC's circuit current…I_{CC}
・Current of R_{REG} connected to REG90…I_{REG}
・Current to drive FET's Gate…$I_{_GATE}$
These decide the voltage ΔV at R_{VCC}.
VCC terminal voltage at that time can be expressed as follows.

$$V_{CC}[V] = VIN[V] - \left(I_{CC}[A] + I_{DCDC}[A] + I_{REG}[A]\right) \times R_{VCC} > 9[V]$$

Here, judgement is the 9V minimum operation voltage.
Please consider a sufficient margin when setting the series resistor of V_{CC}.

【setting example】
Above equation is translated as follows.

$$R_{VCC}[\Omega] < \frac{VIN[V] - 9[V]}{I_{CC}[A] + I_{DCDC}[A] + I_{REG}[A]}$$

When V_{IN}=24V, I_{CC}=2.0mA, R_{REG}=10kΩ and I_{DCDC}=2mA, R_{VCC}'s value is calculated as follows.

$$R_{VCC}[\Omega] < \frac{24[V] - 9[V]}{0.002[A] + 0.002[A] + 5.8[V]/10000[\Omega]} = 3.26[k\Omega]$$

(I_{CC} is 3.3mA(Typ)) . Please set each values with tolerance and margin.

3. LED current setting

LED current can be adjusted by setting the resistance R_S [Ω] which connects to ISENSE pin and ADIM[V].

Relationship between R_S and I_{LED} current

With DC dimming (ADIM<3.0V)

$$R_S = \frac{1}{3} \cdot \frac{ADIM[V]}{I_{LED}[A]}[\Omega]$$

Without DC dimming (ADIM>3.0V)

$$R_S = \frac{1.015[V]}{I_{LED}[A]}[\Omega]$$

【setting example】
If I_{LED} current is 200mA and ADIM is 2.0V, we can calculate R_S as below.

$$R_S = \frac{1}{3} \cdot \frac{ADIM[V]}{I_{LED}[A]} = \frac{1}{3} \cdot \frac{2.0[V]}{0.2[A]} = 3.33[\Omega]$$

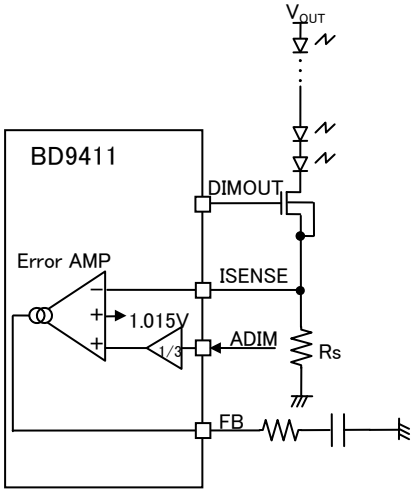


Figure 20. LED current setting example

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4. DCDC Oscillation Frequency Setting

R_{RT} which connects to RT pin sets the oscillation frequency f_{SW} of DCDC.

○Relationship between frequency f_{SW} and RT resistance (ideal)

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

【setting example】

When DCDC frequency fsw is set to 200kHz, R_{RT} is as follows.

$$R_{RT} = \frac{15000}{f_{sw}[kHz]} = \frac{15000}{200[kHz]} = 75 \quad [k\Omega]$$

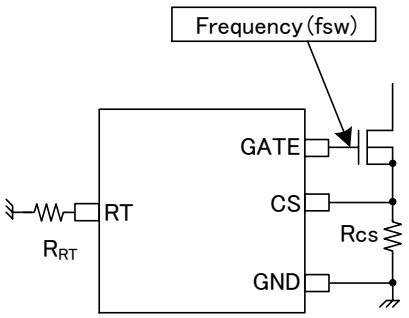


Figure 21. RT terminal setting example

5. UVLO Setting

Under Voltage Lock Out pin is the input voltage of the power stage. IC starts boost operation if UVLO is more than 3.0V(Typ) and stops if lower than 2.7V(Typ).
The UVLO pin is high impedance, because the internal resistance is not connected to a certain bias.
So, the bias by the external components is required, because the open connection of this pin is not a fixed potential.

Detection voltage is set by dividing resistors R1 and R2. The resistor values can be calculated by the formula below.

○UVLO detection equation

As V_{IN} decreases, R1 and R2 values are set in the following formula by the VIN_{DET} that UVLO detects.

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.7[V])}{2.7[V]} \quad [k\Omega]$$

○UVLO release equation

R1 and R2 setting is decided by the equation above. The equation of UVLO release voltage is as follows.

$$VIN_{CAN} = 3.0V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

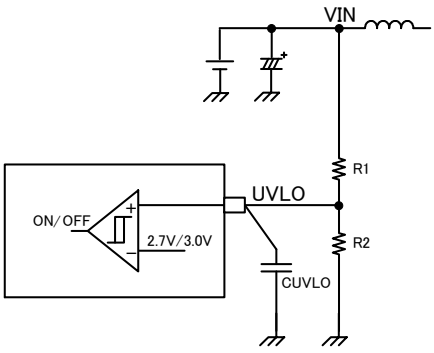


Figure 22. UVLO setting example

【setting example】

If the normal input voltage, V_{IN} is 24V, the detect voltage of UVLO is 18V, R2 is 30kΩ, R1 is calculated as follows.

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.7[V])}{2.7[V]} = 30[k\Omega] \times \frac{(18[V] - 2.7[V])}{2.7[V]} = 170.0 \quad [k\Omega]$$

By using these R1 and R2, the release voltage of UVLO, VIN_{CAN}, can be calculated too as follows.

$$VIN_{CAN} = 3.0[V] \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 3.0[V] \times \frac{170[k\Omega] + 30[k\Omega]}{30[k\Omega]}[V] = 20.0 \quad [V]$$

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6. ODP Setting

R_{DUTYP} which connects to ODP pin sets the ODP detection duty.

○Relationship between LED PWM frequency f_{PWM}, ODP Detection Duty and DUTYP resistance (ideal)

$$R_{DUTYP} = \frac{1172 \times ODP_{duty}[\%]}{f_{PWM}[Hz]} \quad [k\Omega]$$

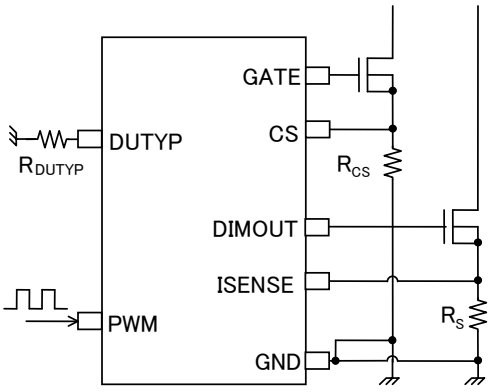


Figure 23. ODP setting example

【setting example】

When LED PWM frequency f_{PWM}, is set to 120Hz and ODP Detection Duty (ODP_{duty}) is set to 35%, R_{DUTYP} is as follows.

$$R_{DUTYP} = \frac{1172 \times 35[\%]}{120[Hz]} = 341.8[k\Omega]$$

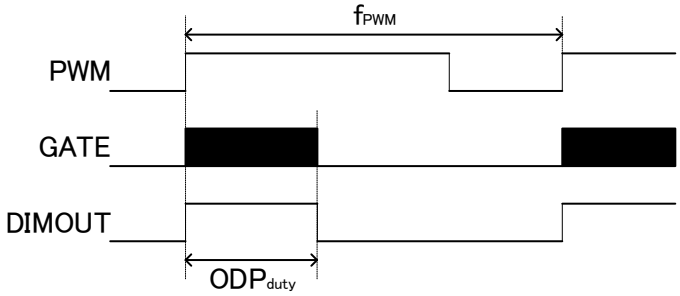


Figure 24. The GATE and the DIMOUT waveform as PWM dimming (ODP)

7. OVP Setting

The OVP terminal is the input for over-voltage protection of output voltage.
The OVP pin is high impedance, because the internal resistance is not connected to a certain bias.

Detection voltage of V_{OUT} is set by dividing resistors R1 and R2. The resistor values can be calculated by the formula below.

○OVP detection equation

If V_{OUT} is boosted abnormally, $VOVP_{DET}$, the detect voltage of OVP, R1, R2 can be expressed by the following formula.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]} \quad [k\Omega]$$

○OVP release equation

By using R1 and R2 in the above equation, the release voltage of OVP, $VOVP_{CAN}$ can be expressed as follows.

$$VOVP_{CAN} = 2.8V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

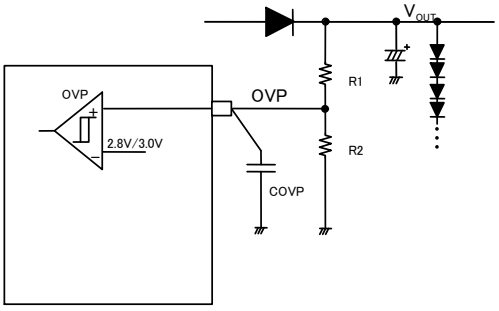


Figure 25. OVP setting example

【setting example】

If the normal output voltage, V_{OUT} is 40V, the detect voltage of OVP is 48V, R2 is 10kΩ, R1 is calculated as follows.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]} = 10[k\Omega] \times \frac{(48[V] - 3[V])}{3[V]} = 150[k\Omega]$$

By using these R1 and R2, the release voltage of OVP, $VOVP_{CAN}$ can be calculated as follows.

$$VOVP_{CAN} = 2.8[V] \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 2.8[V] \times \frac{10[k\Omega] + 150[k\Omega]}{10[k\Omega]}[V] = 44.8[V]$$

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8. Protection Timer (CP Counter) Setting, Auto-Restart Timer Setting

About over boost protection (FBMAX), protection timer (CP Counter) is set by counting the clock frequency which is set at the RT pin. About the behavior from abnormal detection for use timer, please refer to the “Timing Chart” section.

The condition FB>4.0V(Typ) and PWM=H continues more than four GATE clocks, counting starts from the timing. After that, FBMAX protection monitor only the FB voltage and DCDC operation will be stop after below time has passed.

$$TIMER_{TIME} = 2^{14} \times \frac{R_{RT}}{1.5 \times 10^{10}} = 16384 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^{7}}[s]$$

$$AUTO_{TIME} = 2^{17} \times \frac{R_{RT}}{1.5 \times 10^{10}} = 131072 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^{7}}[s]$$

Here, $TIMER_{TIME}$ = time until IC's operation stop, $AUTO_{TIME}$ = auto restart timer’s time
R_{RT} = Resistor value connected to RT pin

【setting example】

Protection Timer time when RT=100kohm

$$TIMER_{TIME} = 16384 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^{7}} = 16384 \times \frac{100[k\Omega]}{1.5 \times 10^{7}} = 109.2\,[ms]$$

$$AUTO_{TIME} = 131072 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^{7}} = 131072 \times \frac{100[k\Omega]}{1.5 \times 10^{7}} = 873.8\,[ms]$$

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DCDC Parts Selection

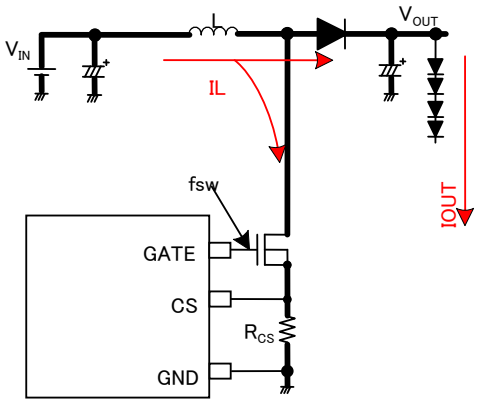
1. OCP Setting / Calculation Method for the Current Rating of DCDC Parts

OCP detection stops the switching when the CS pin voltage is more than 0.4V(Typ). The resistor value of CS pin, R_{CS} needs to be considered by the coil L current. And the current rating of DCDC external parts is required more than the peak current of the coil.
Shown below are the calculation method of the coil peak current, the selection method of R_{CS} (the resistor value of CS pin) and the current rating of the external DCDC parts at Continuous Current Mode.

(the calculation method of the coil peak current, I_{peak} at Continuous Current Mode)

At first, since the ripple voltage at CS pin depends on the application condition of DCDC, the following variables are used.
Vout voltage=V_{OUT}[V]
LED total current=I_{OUT}[A]
DCDC input voltage of the power stage =V_{IN}[V]
Efficiency of DCDC =η[%]
And then, the average input current IIN is calculated by the following equation.

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$



And the ripple current of the inductor L (ΔI_L[A]) can be calculated by using DCDC the switching frequency, f_{SW}, as follows.

$$\Delta I_L = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$

On the other hand, the peak current of the inductor I_{peak} can be expressed as follows.

$$I_{peak} = I_{IN}[A] + \frac{\Delta I_L[A]}{2} \quad [A] \qquad \cdots (1)$$

Therefore, the bottom of the ripple current I_{min} is

$$I_{\min} = I_{IN}[A] - \frac{\Delta I_L[A]}{2} \quad \text{or } 0$$

If Imin>0, the operation mode is CCM (Continuous Current Mode), otherwise the mode is DCM (Discontinuous Current Mode).

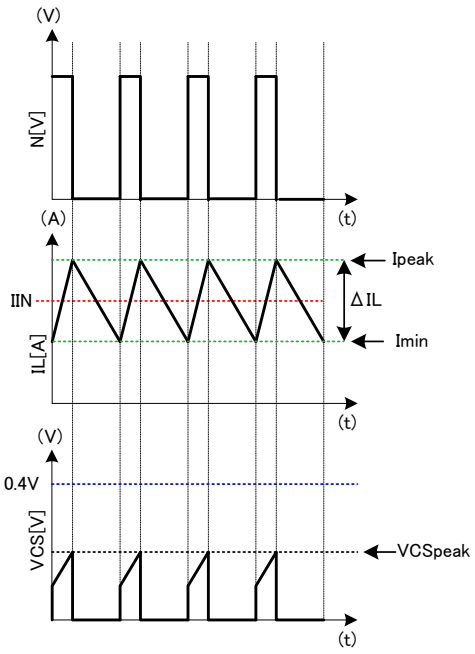


Figure 26. Coil current waveform

(the selection method of Rcs at Continuous Current Mode)

Ipeak flows into R_{CS} and that causes the voltage signal to CS pin. (Please refer to the timing chart at the right)
Peak voltage VCS_{peak} is as follows.

$$VCS_{peak} = R_{CS} \times I_{peak} \quad [V]$$

As this VCSpeak reaches 0.4V(Typ), the DCDC output stops the switching. Therefore, R_{CS} value is necessary to meet the condition below.

$$R_{CS} \times I_{peak}[V] << 0.4[V]$$

(the current rating of the external DCDC parts)

The peak current as the CS voltage reaches OCP level (0.4V (Typ)) is defined as I_{peak_det}.

$$I_{peak_det} = \frac{0.4[V]}{R_{CS}[\Omega]} \quad [A] \qquad \cdots (2)$$

The relationship among I_{peak} (equation (1)), I_{peak_det} (equation (2)) and the current rating of parts is required to meet the following

$$I_{peak} << I_{peak_det} << \text{The current rating of parts}$$

Please make the selection of the external parts such as FET, Inductor, diode meet the above condition.

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[setting example]
Output voltage = V_{OUT} [V] = 40V
LED total current = I_{OUT} [A] = 0.48V
DCDC input voltage of the power stage = V_{IN} [V] = 24V
Efficiency of DCDC =η[%] = 90%
Averaged input current IIN is calculated as follows.

$$I_{IN}[A] = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} = \frac{40[V] \times 0.48[A]}{24[V] \times 90[\%]} = 0.89\,[A]$$

If the switching frequency, f_{SW} = 200kHz, and the inductor, L=100μH, the ripple current of the inductor L (ΔIL[A]) can be calculated as follows.

$$\Delta I_L = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} = \frac{(40[V] - 24[V]) \times 24[V]}{100 \times 10^{-6}[H] \times 40[V] \times 200 \times 10^{3}[Hz]} = 0.48\,[A]$$

Therefore the inductor peak current, I_{peak} is

$$I_{peak} = I_{IN}[A] + \frac{\Delta IL[A]}{2}[A] = 0.89[A] + \frac{0.48[A]}{2} = 1.13\,[A]$$ …calculation result of the peak current

If Rcs is assumed to be 0.3Ω

$$VCS_{peak} = Rcs \times Ipeak = 0.3[\Omega] \times 1.13[A] = 0.339 \quad [V] << 0.4V$$ …R_{CS} value confirmation

The above condition is met.
And I_{peak_det}, the current OCP works, is

$$I_{peak_det} = \frac{0.4[V]}{0.3[\Omega]} = 1.33\,[A]$$

If the current rating of the used parts is 2A,

$$I_{peak} << I_{peak_det} << \text{The current rating} \quad = 1.13[A] << 1.33[A] << 2.0[A]$$ …current rating confirmation of DCDC parts

This inequality meets the above relationship. The parts selection is proper.
And I_{MIN}, the bottom of the IL ripple current, can be calculated as follows.

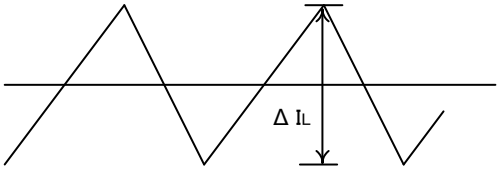
$$I_{MIN} = I_{IN}[A] - \frac{\Delta I_L[A]}{2}[A] = 1.13[A] - 0.48[A] = 0.65[A] >> 0$$

This inequality implies that the operation is continuous current mode.

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2. Inductor Selection

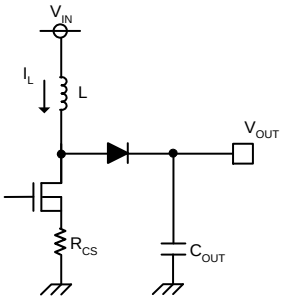
The inductor value affects the input ripple current, as shown the "OCP setting" on Page18.



$$\Delta I_L = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$

$$Ipeak = I_{IN}[A] + \frac{\Delta I_L[A]}{2} \quad [A]$$



Where
L: coil inductance [H] V_{OUT}: DCDC output voltage [V]
V_{IN}: input voltage [V]
I_{OUT}: output load current (the summation of LED current) [A]
I_{IN}: input current [A] f_{SW}: oscillation frequency [Hz]

Figure 27. Inductor current waveform and diagram

In continuous current mode, ⊿I_L is set to 30% to 50% of the output load current in many cases.
In using smaller inductor, the boost is operated by the discontinuous current mode in which the coil current returns to zero at every period.

*The current exceeding the rated current value of inductor flown through the coil causes magnetic saturation, results in decreasing in efficiency. Inductor needs to be selected to have such adequate margin that peak current does not exceed the rated current value of the inductor.
*To reduce inductor loss and improve efficiency, inductor with low resistance components (DCR, ACR) needs to be selected

3. Output Capacitance Cout Selection

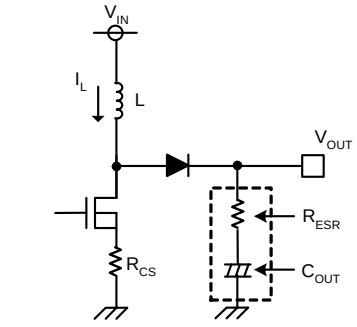


Figure 28. Output capacitor diagram

Output capacitor needs to be selected in consideration of equivalent series resistance required to even the stable area of output voltage or ripple voltage. Be aware that set LED current may not be flown due to decrease in LED terminal voltage if output ripple component is high.
Output ripple voltage ⊿V_{OUT} is determined by Equation (4):

$$\Delta V_{OUT} = \Delta I_L \times R_{ESR}[V] \quad \cdots\cdots \quad (4)$$

When the coil current is charged to the output capacitor as MOS turns off, much output ripple is caused. Much ripple voltage of the output capacitor may cause the LED current ripple.

* Rating of capacitor needs to be selected to have adequate margin against output voltage.
*To use an electrolytic capacitor, adequate margin against allowable current is also necessary. Be aware that the LED current is larger than the set value transitionally in case that LED is provided with PWM dimming especially.

4. MOSFET Selection

There is no problem if the absolute maximum rating is larger than the rated current of the inductor L, or is larger than the sum of the tolerance voltage of C_{OUT} and the rectifying diode V_F. The product with small gate capacitance (injected charge) needs to be selected to achieve high-speed switching.

* One with over current protection setting or higher is recommended.
* The selection of one with small on resistance results in high efficiency.

5. Rectifying Diode Selection

A schottky barrier diode which has current ability higher than the rated current of L, reverse voltage larger than the tolerance voltage of C_{OUT}, and low forward voltage VF especially needs to be selected.

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Loop Compensation

A current mode DCDC converter has each one pole (phase lag) f_p due to CR filter composed of the output capacitor and the output resistance (= LED current) and zero (phase lead) f_Z by the output capacitor and the ESR of the capacitor.
Moreover, a step-up DCDC converter has RHP zero (right-half plane zero point) f_{ZRHP} which is unique with the boost converter. This zero may cause the unstable feedback. To avoid this by RHP zero, the loop compensation that the cross-over frequency f_c, set as follows, is suggested.

fc = f_{ZRHP} /5 (f_{ZRHP}: RHP zero frequency)

Considering the response speed, the calculated constant below is not always optimized completely. It needs to be adequately verified with an actual device.

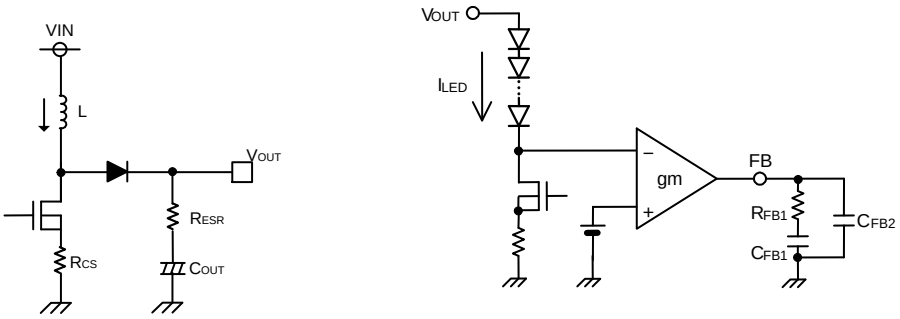


Figure 29. Output stage and error amplifier diagram

i. Calculate the pole frequency fp and the RHP zero frequency f_{ZRHP} of DC/DC converter

$$f_p = \frac{I_{LED}}{2\pi \times V_{OUT} \times C_{OUT}}[Hz] \qquad f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi \times L \times I_{LED}}[Hz]$$

Where I_{LED} = the summation of LED current, $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$ (Continuous Current Mode)

ii. Calculate the phase compensation of the error amp output (f_c = f_{ZRHP}/5)

$$R_{FB1} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED}}{5 \times f_p \times gm \times V_{OUT} \times (1-D)}[\Omega]$$

$$C_{FB1} = \frac{1}{2\pi \times R_{FB1} \times f_C} = \frac{5}{2\pi \times R_{FB1} \times f_{ZRHP}}[F]$$

$$gm = 4.0 \times 10^{-4}[S]$$

Above equation is described for lighting LED without the oscillation. The value may cause much error if the quick response for the abrupt change of dimming signal is required.
To improve the transient response, R_{FB1} needs to be increased, and C_{FB1} needs to be decreased. It needs to be adequately verified with an actual device in consideration of variation from parts to parts since phase margin is decreased.

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Timing Chart

1. PWM Start up 1 (Input PWM Signal After Input STB Signal)

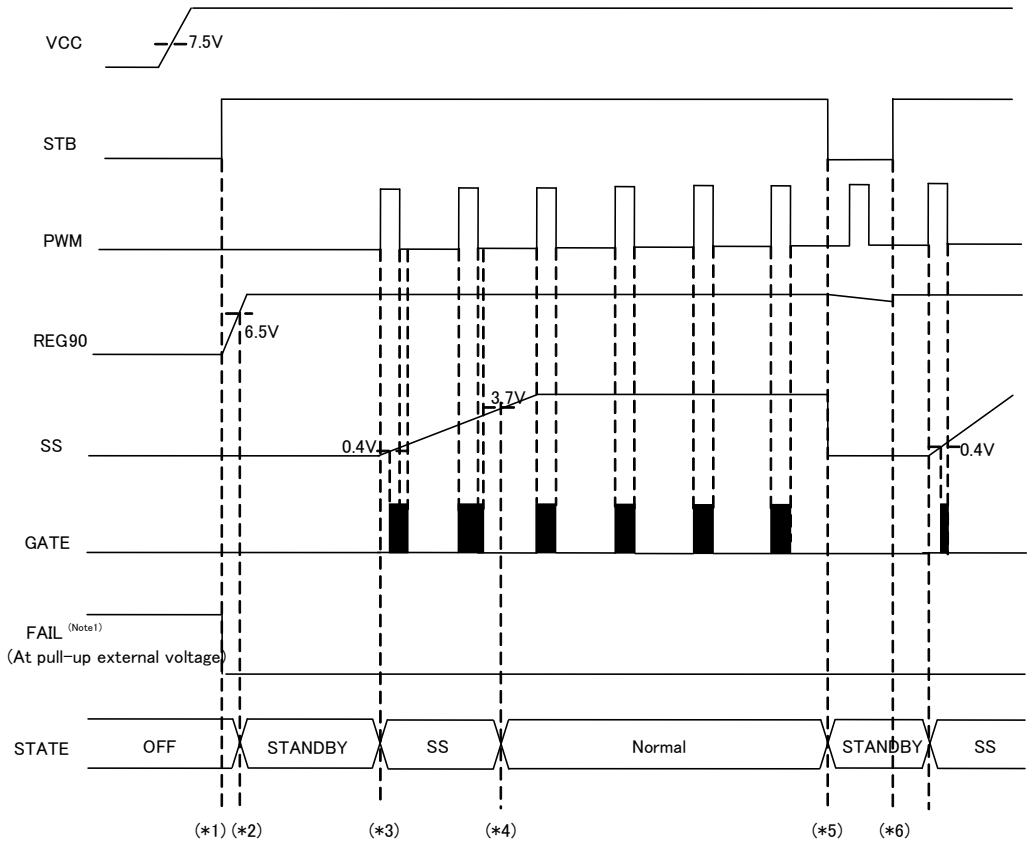


Figure 30. PWM Start up 1 (Input PWM Signal After Input STB Signal)

(*1)…REG90 starts up when STB is changed from Low to High. In the state where the PWM signal is not inputted, SS terminal is not charged and DCDC doesn't start to boost, either.
(*2)…When REG90 is more than 6.5V(Typ), the reset signal is released.
(*3)…The charge of the pin SS starts at the positive edge of PWM=L to H, and the soft start starts. And while the SS is less than 0.4V, the pulse does not output. The pin SS continues charging in spite of the assertion of PWM or OVP level.
(*4)…The soft start interval will end if the voltage of the pin SS, V_{SS} reaches 3.7V(Typ). By this time, it boosts V_{OUT} to the voltage where the set LED current flows. The abnormal detection of FBMAX starts to be monitored.
(*5)…As STB=L, the boost operation is stopped instantaneously. (Discharge operation continues in the state of STB=L and REGUVLO=L. Please refer to the "Turn Off" section on Page24)
(*6)…In this diagram, before the charge period is completed, STB is changed to High again. As STB=H again, the boost operation restarts the next PWM=H. It is the same operation as the timing of (*2). (For capacitance setting of SS terminal, please refer to the "Method of setting SS external capacitance" section on Page13.

(Note1) At FAIL terminal pull-up to external voltage, FAIL voltage is "H" until REG90 over 6.5V. (Initial FAIL's NMOS is "OFF" before IC's circuit will operate).

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2. **PWM Start Up 2 (Input STB Signal after Inputted PWM Signal)**

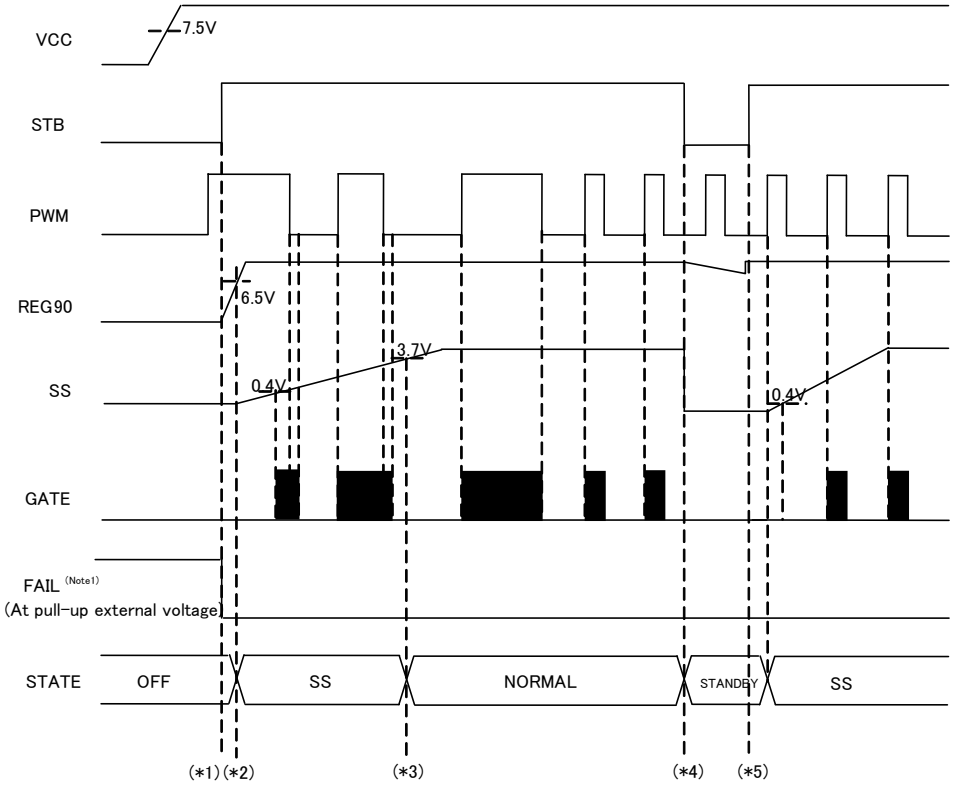


Figure 31. PWM Start Up 2 (Input STB Signal after Inputted PWM Signal)

(*1)…REG90 starts up when STB=H.
(*2)…When REG90UVLO releases or PWM is inputted to the edge of PWM=L→H, SS charge starts and soft start period is started. And while the SS is less than 0.4V, the pulse does not output. The pin SS continues charging in spite of the assertion of PWM or OVP level.
(*3)…The soft start interval will end if the voltage of the pin SS, V_{SS} reaches 3.7V(Typ). By this time, it boosts V_{OUT} to the point where the set LED current flows. The abnormal detection of FBMAX starts to be monitored.
(*4)…As STB=L, the boost operation is stopped instantaneously (GATE=L, SS=L). (Discharge operation works in the state of STB=L and REG90UVLO=H. Please refer to the "Turn Off" section on Page24)
(*5)…In this diagram, before the discharge period is completed, STB is changed to High again. As STB=H again, operation will be the same as the timing of (*1).

(Note1) At FAIL terminal pull-up to external voltage, FAIL voltage is "H" until STB change from "L" to "H". (Initial FAIL's NMOS is "OFF" before IC's circuit will operate).

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3. Turn Off

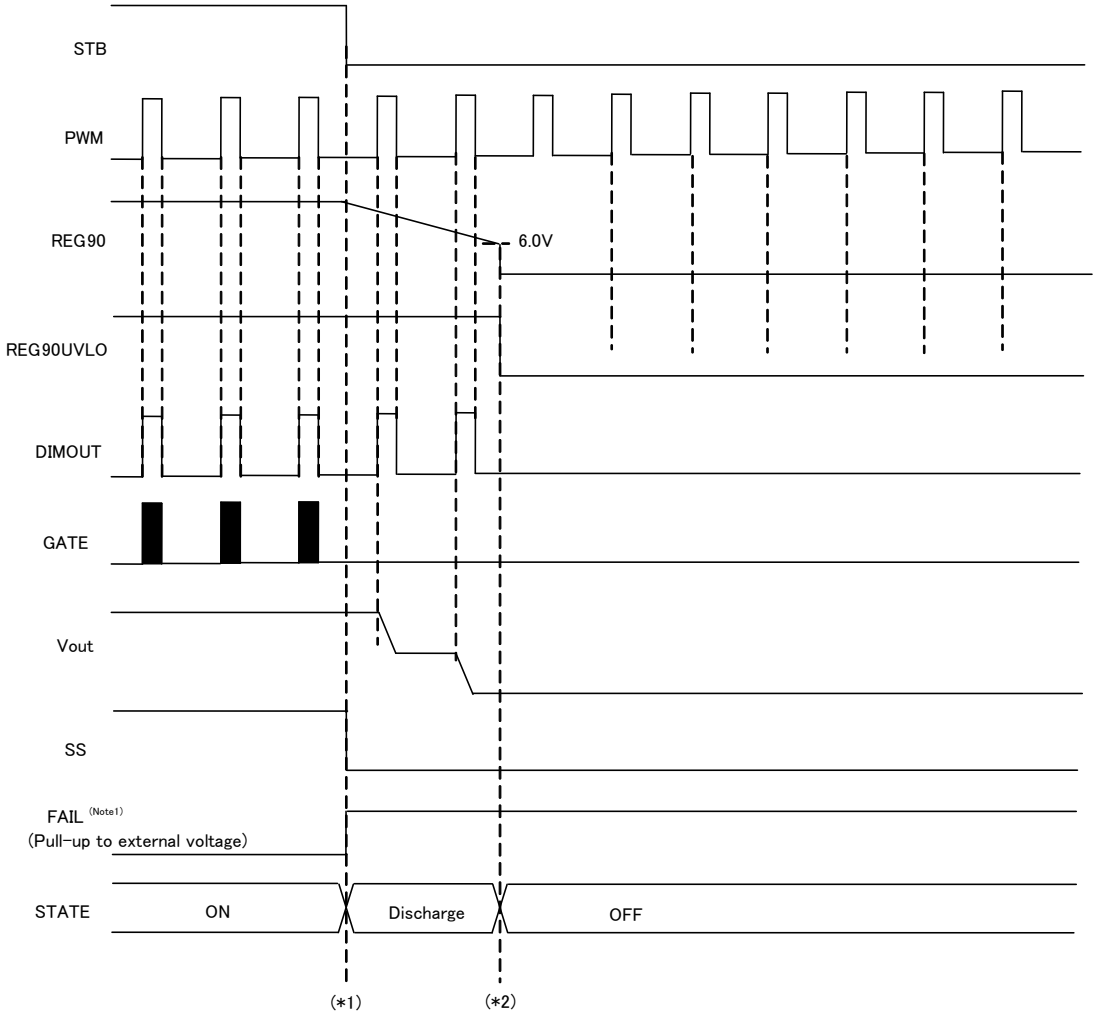


Figure 32. Turn Off

(*1)…As STB=H→L, boost operation stops and REG90 starts to discharge. The discharge curve is decided by REG90 discharge resistance and the capacitor of the REG90 terminal.
(*2)…While STB=L, REG90UVLO=H, DIMOUT becomes same as PWM. When REG90=9.0V is less than 6.0V(Typ), IC becomes OFF state. V_{OUT} is discharged completely until this time. It should be set to avoid a sudden brightness.

(Note1) At FAIL terminal pull-up to external voltage, FAIL voltage is "H" until STB change from "L" to "H". (Initial FAIL's NMOS is "OFF" before IC's circuit will operate).

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4. Soft Start Function

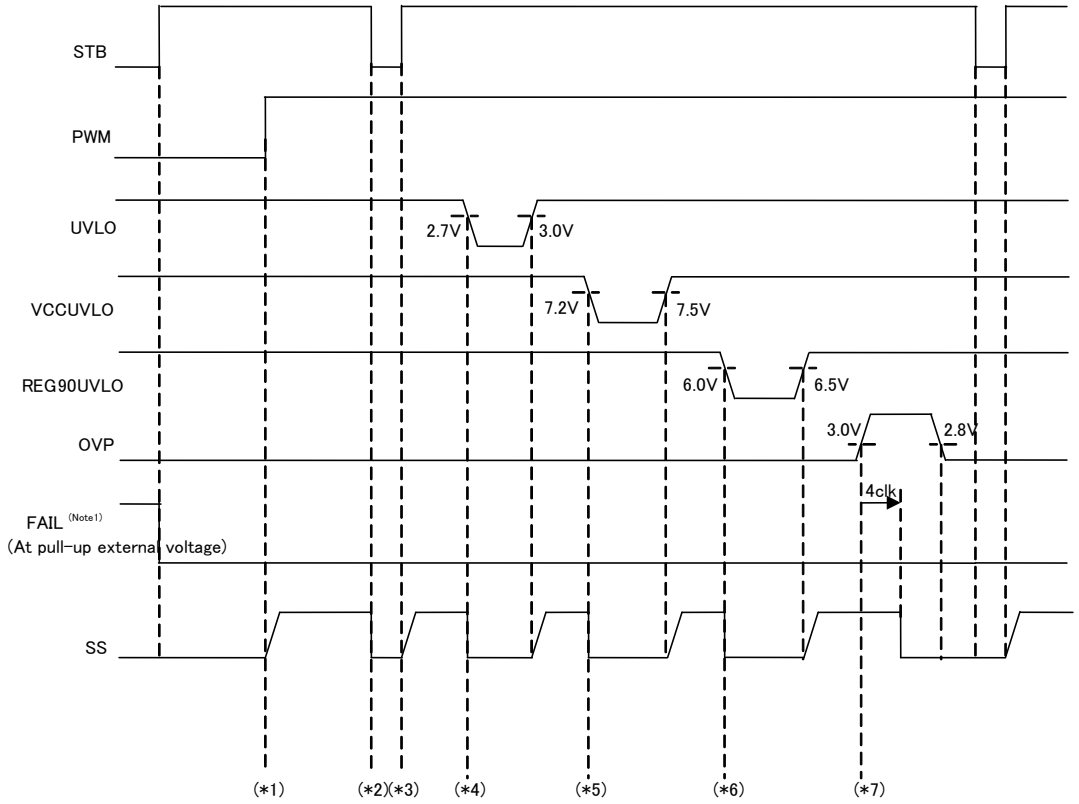


Figure 33. Soft Start Function

(*1)…The SS pin charge does not start by just STB=H. PWM=H is required to start the soft start. In the low SS voltage, the GATE pin duty depends on the SS voltage. And while the SS is less than 0.4V, the pulse does not output.
(*2)…By the time STB=L, the SS pin is discharged immediately.
(*3)…As the STB recovered to STB=H, The SS charge starts immediately by the logic PWM=H in this chart.
(*4)…The SS pin is discharged immediately by the UVLO=L.
(*5)…The SS pin is discharged immediately by the VCCUVLO=L.
(*6)…The SS pin is discharged immediately by the REG90UVLO=L.
(*7)…The SS pin is not discharged by the abnormal detection for use timer Type protection such as OVP until the timer finish.

(Note1) At FAIL terminal pull-up to external voltage, FAIL voltage is "H" until STB change from "L" to "H". (Initial FAIL's NMOS is "OFF" before IC's circuit will operate).

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5. OVP Detection

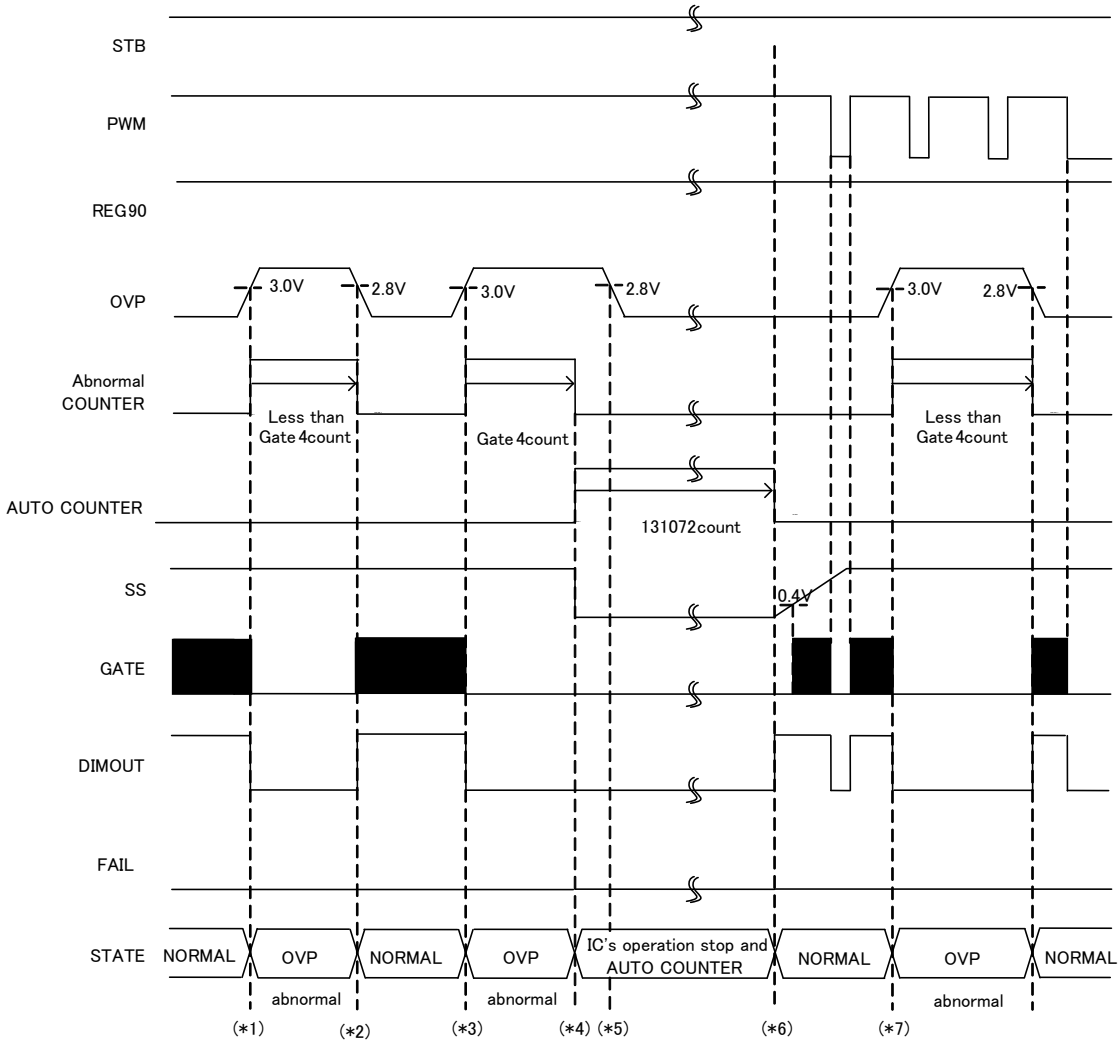


Figure 34. OVP Detection

(*1)…As OVP is detected, the output GATE=L, DIMOUT=L, and the abnormal counter starts.
(*2)…If OVP is released within 4 clocks of abnormal counter of the GATE pin frequency, the boost operation restarts.
(*3)…As the OVP is detected again, the boost operation is stopped.
(*4)…As the OVP detection continues up to 4 count by the abnormal counter, IC's operation will be stop. After IC operation stop, auto counter starts counting.
(*5)… Once IC operation stop, the boost operation doesn't restart even if OVP is released.
(*6)…When auto counter reaches 131072clk (2^{17}clk), IC will be auto-restarted. The auto restart interval can be calculated by the external resistor of RT pin. (Please refer to the "Timer Latch Time setting, Auto-Restart Timer setting" section on Page17.)
(*7)…The operation of the OVP detection is not related to the logic of PWM.

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6. FBMAX Detection

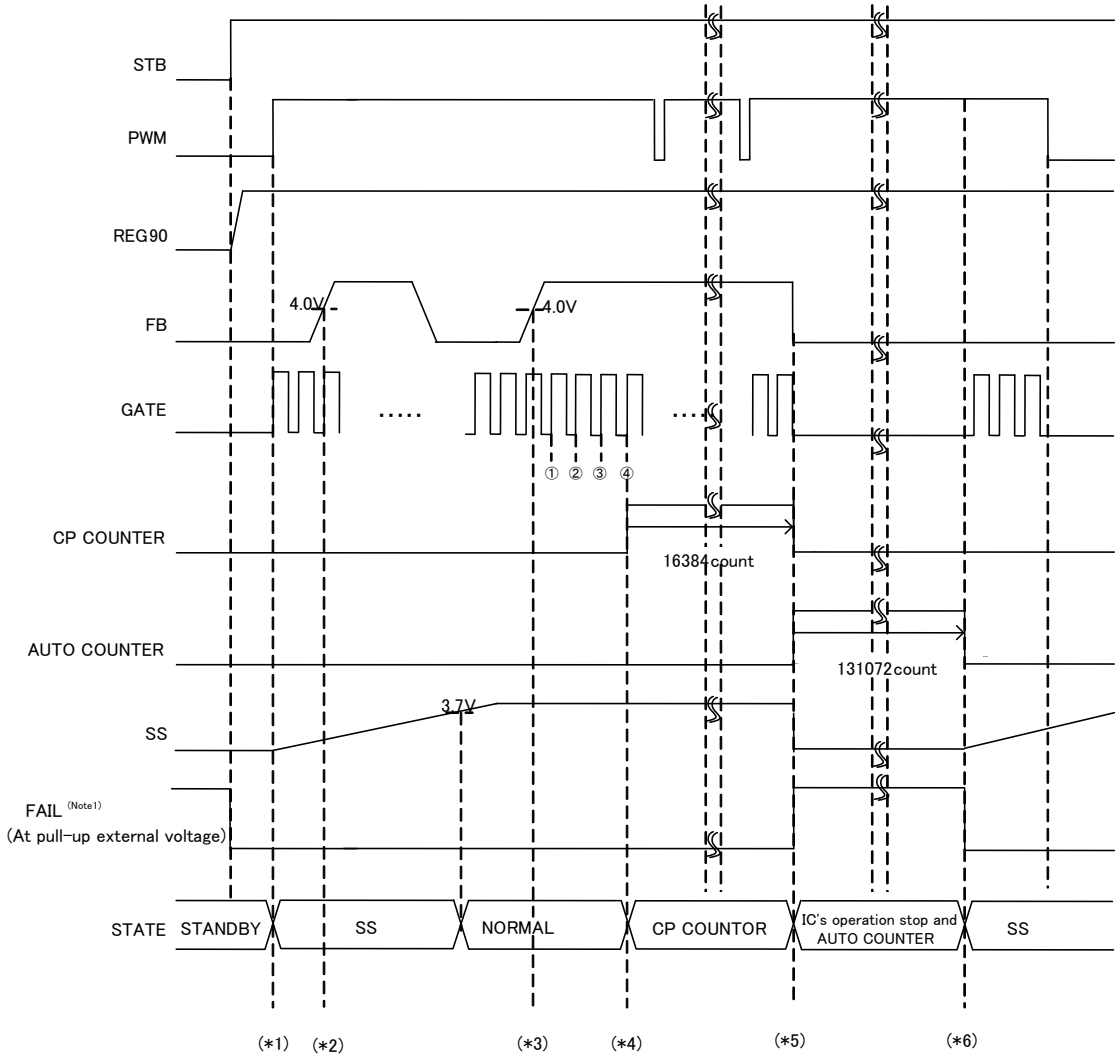


Figure 35. FBMAX Detection

(*2)…During the soft start, it is not judged to the abnormal state even if the FB=H(FB>4.0V(Typ)).
(*3)…When the PWM=H and FB=H, the abnormal counter doesn't start immediately.
(*4)…The CP counter will start if the PWM=H and the FB=H detection continues up to 4 clocks of the GATE frequency. Once the count starts, only FB level is monitored.
(*5)…When the FBMAX detection continues till the CP counter reaches 16384clk (2^{14}clk), IC's operation will be stop. The operation stop interval can be calculated by the external resistor of RT pin. (Please refer to the "Timer Latch Time setting, Auto-Restart Timer setting" section on Page17.)
(*6)…When auto counter reaches 131072clk (2^{17}clk), IC will be auto-restarted. The auto restart interval can be calculated by the external resistor of RT pin. (Please refer to the "Timer Latch Time setting, Auto-Restart Timer setting" section on Page17.)

(Note1) At FAIL terminal pull-up to external voltage, FAIL voltage is "H" until STB change from "L" to "H". (Initial FAIL's NMOS is "OFF" before IC's circuit will operate).

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7. LED OCP Detection

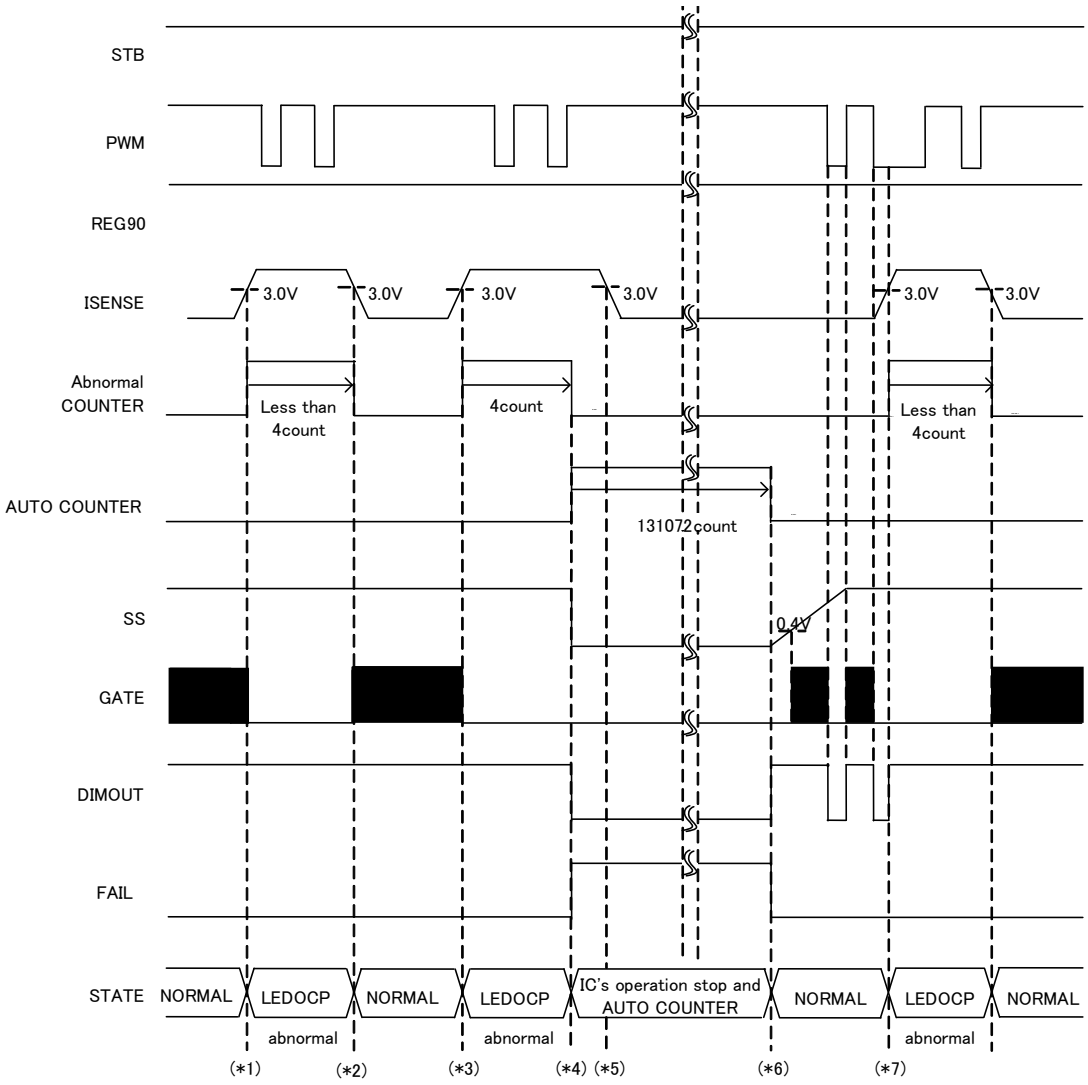
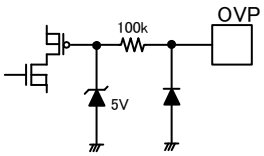
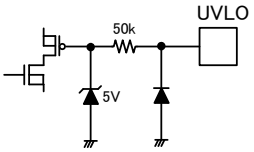
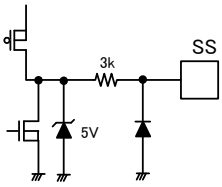
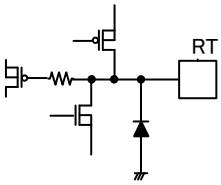
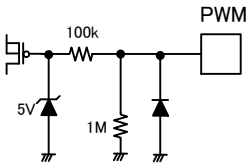
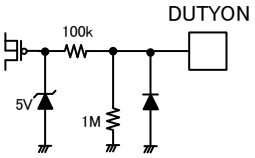
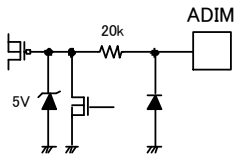
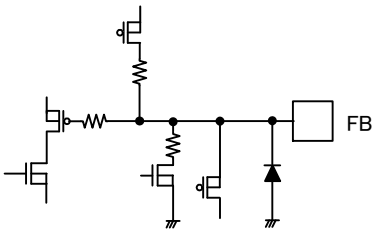
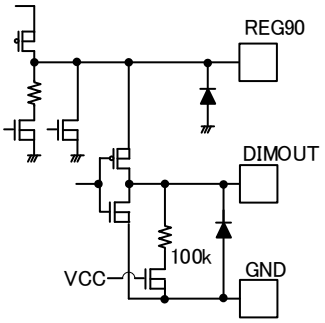
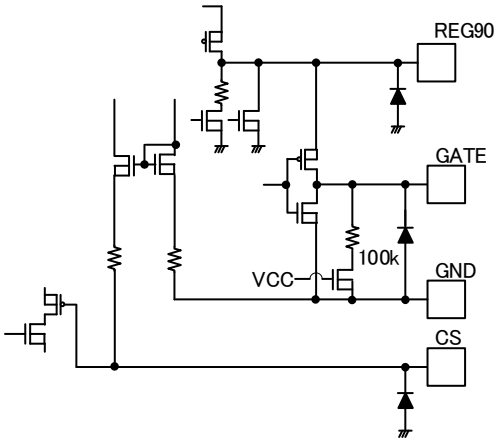
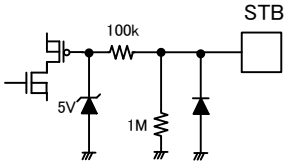
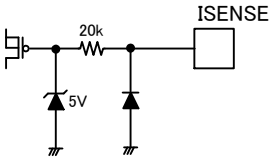
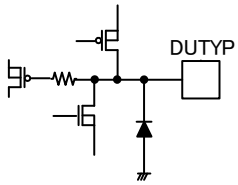
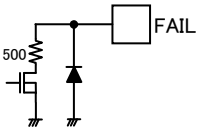


Figure 36. LED OCP Detection

(*1)…If ISENSE>3.0V(Typ), LEDOCP is detected, and GATE becomes L. To detect LEDOCP continuously, The DIMOUT is compulsorily high, regardless of the PWM dimming signal.
(*2)…When the LEDOCP releases within 4 counts of the GATE frequency, the boost operation restarts.
(*3) …As the LEDOCP is detected again, the boost operation is stopped.
(*4)…If the LEDOCP detection continues up to 4 counts of GATE frequency. IC's operation will be stop. After IC operation stop, auto counter starts counting.
(*5)…Once IC's operation stop, the boost operation doesn't restart even if the LEDOCP releases.
(*6)…When auto counter reaches 131072clk (2^{17}clk), IC will be auto-restarted. The auto restart interval can be calculated by the external resistor of RT pin. (Please refer to the "Timer Latch Time setting, Auto-Restart Timer setting" section on Page17.)
(*7)…The operation of the LEDOCP detection is not related to the logic of the PWM.

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I/O Equivalent Circuits

OVP	UVLO	SS
		
RT	**PWM**	**DUTYON**
		
ADIM	**FB**	**DIMOUT / REG90**
		
GATE / REG90 / CS	**STB**	**ISENSE**
		
DUTYP	**FAIL**	
		

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

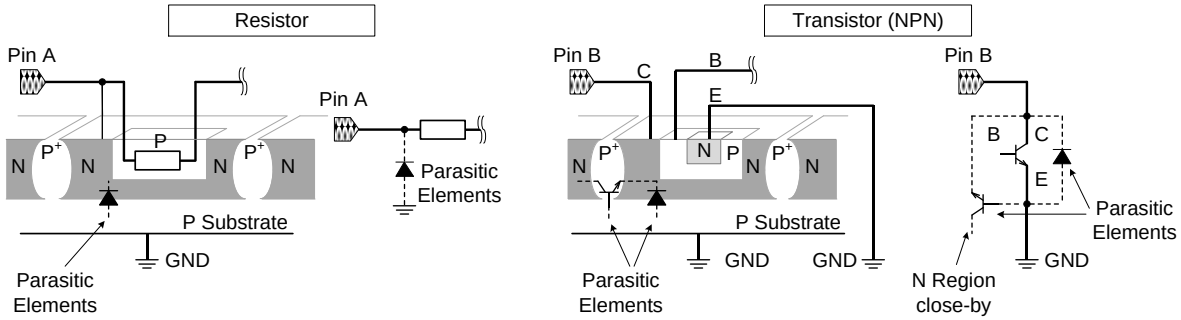


Figure 37. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

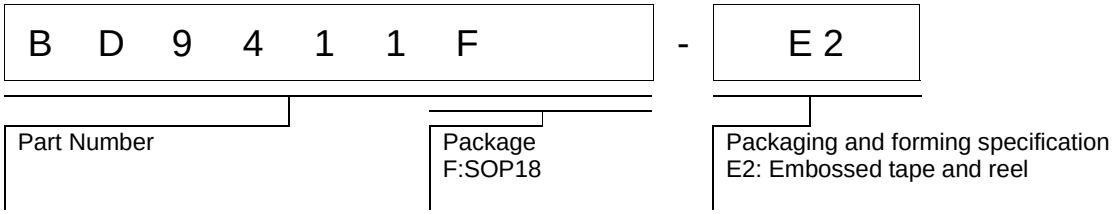
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

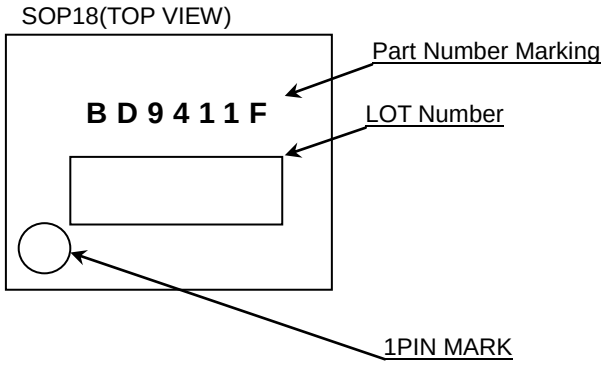
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information



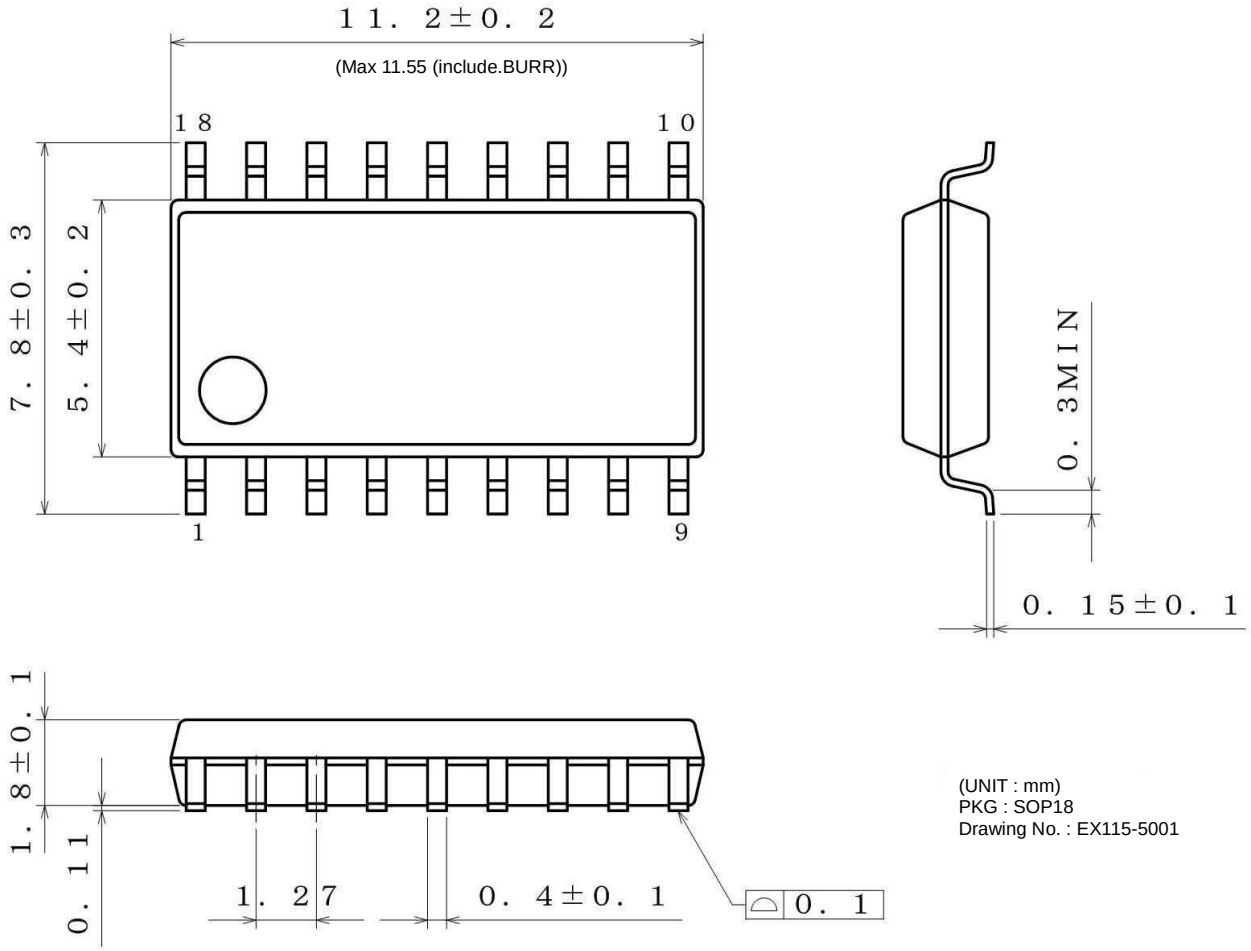
Marking Diagrams



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Physical Dimension, Tape and Reel Information

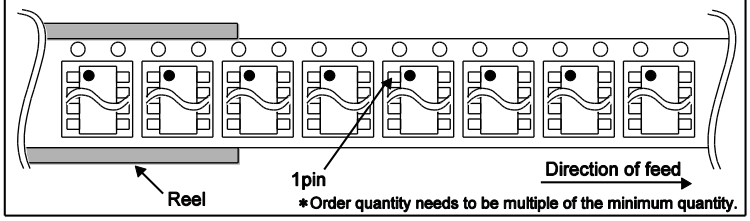
Package Name	SOP18



(UNIT : mm)
PKG : SOP18
Drawing No. : EX115-5001

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
20.Feb. 2017	001	New Release

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Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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