TEXAS INSTRUMENTS
UC1823A, UC2823A, UC2823B, UC3823A, UC3823B
UC1825A, UC2825A, UC2825B, UC3825A, UC3825B
ZHCSQX4F – AUGUST 1995 – REVISED AUGUST 2022

高速 PWM 控制器

1 特性

- UC3823/UC3825 PWM 控制器的改进版本
- 与电压模式或电流模式控制方法兼容
- 实际工作开关频率高达 1MHz
- 50ns 传播延迟到输出
- 大电流双图腾柱输出（2A 峰值）
- 修整的振荡器放电电流
- 低 100μA 启动电流
- 逐脉冲电流限制比较器
- 可在整个周期内重启的锁存过流比较器

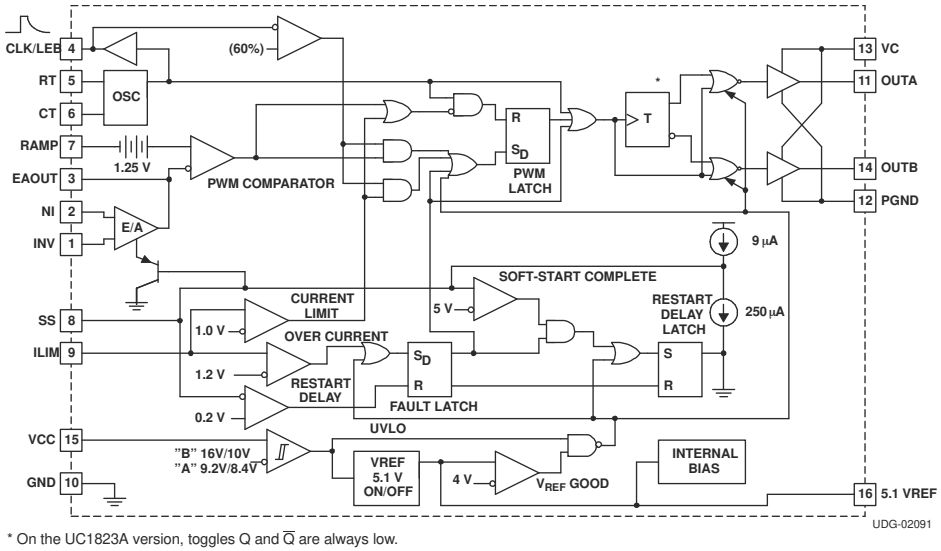
2 说明

UC3823A 和 UC3823B 以及 UC3825A 和 UC3825B 系列 PWM 控制器是标准 UC3823 和 UC3825 系列的改进版本，其中几个电路块的性能得到了提升。误差放大器增益带宽积为 12MHz，而输入失调电压为 2mV。电流限制阈值经验证为耐受的 5%。为实现精准死区时间控制，振荡器放电电流额定值为 10mA。频率精度被提升至 6%。典型值为 100μA 的启动电源电流非常适合于脱机应用。在不对启动电流技术规格产生影响的情况下，重新设计了输出驱动器，以便在 UVLO 期间主动灌电流。此外，每个输出在转换期间能够输出 2A 的峰值电流。

该系列还实施了功能改进。UC3825 关断比较器现在是一款阈值为 1.2V 的高速过流比较器。该过流比较器通过使锁存器置位，可确保软启动电容器在允许重新启动之前完全放电。当故障锁存器被置位时，输出处于低电平状态。如果发生持续故障，软启动电容器会在放电前充满电，以确保故障频率不超过设计的软启动周期。UC3825 时钟引脚已变成 CLK/LEB。该引脚结合了时钟输出和前沿消隐调节功能，可提供缓冲输出以便于连接。

UC3825A 和 UC3825B 具有双路交替输出以及与 UC3825 相同的引脚配置。UC3823A 和 UC3823B 输出同相运行，占空比从 0 到小于 100%。UC3823A 和 UC3823B 的引脚配置与 UC3823 相同（引脚 11 除外，它现在是输出引脚，而不是电流限制比较器的基准引脚）。*A* 版本器件具有与原始 UC3823 和 UC3825 相同的 UVLO 阈值。*B* 版本的 UVLO 阈值为 16V 和 10V，方便在离线应用中使用。

要了解详细的技术和应用信息，请参阅 *UC3823A/B 和 UC3825A/B 增强型 PWM 控制器* (SLUA125) 应用手册。



* On the UC1823A version, toggles Q and $\overline{Q}$ are always low.

图 2-1. 方框图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (September 2010) to Revision F (August 2022)	Page
• Added SOIC package	3
• Added Thermal Information	5

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4 Ordering Information

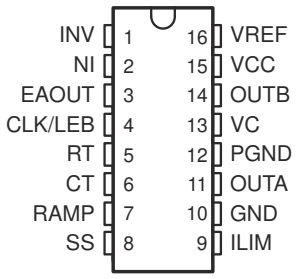
T_A	MAXIMUM DUTY CYCLE	UVLO					
		9.2 V / 8.4 V			16 V / 10 V		
		SOIC-16 (1) (DW)	PDIP-16 (N)	PLCC-20(1) (Q)	SOIC-16 (DW)	PDIP-16 (N)	PLCC-20 (1) (Q)
40°C to 85°C	< 100%	UC2823ADW	UC2823AN	UC2823AQ	UC2823BDW	UC2823BN	
	< 50%	UC2825ADW	UC2825AN	UC2825AQ	UC2825BDW	UC2825BN	
0°C to 70°C	< 100%	UC3823ADW	UC3823AN	UC3823AQ	UC3823BDW	UC3823BN	
	< 50%	UC3825ADW	UC3825AN	UC3825AQ	UC3825BDW	UC3825BN	UC3825BQ

(1) The DW and Q packages are also available taped and reeled. Add TR suffix to the device type (i.e., UC2823ADWR). To order quantities of 1000 devices per reel for the Q package and 2000 devices per reel for the DW package.

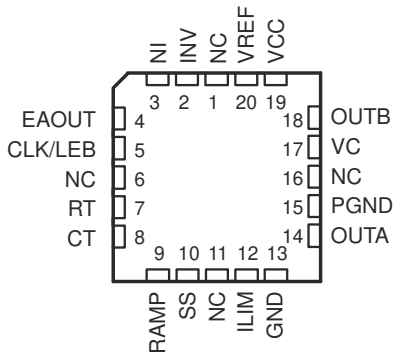
5 Pin Configuration and Functions

T_A	MAXIMUM DUTY CYCLE	UVLO (9.2 V/8.4 V)	
		CDIP-16 (J)	LCCC-20 (L)
55°C to 125°C	< 100%	UC1823AJ, UC1823AJ883B, UC1823AJQMLV	UC1823AL, UC1823AL883B
	< 50%	UC1825AJ, UC1825AJ883B, UC1825AJQMLV	UC1825AL, UC1825AL883B, UC1825ALQMLV

DW, J, OR N PACKAGES
(TOP VIEW)



Q OR L PACKAGES
(TOP VIEW)



NC = no connection

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	J, N, or DW	Q or L		
CLK/LEB	4	5	O	Output of the internal oscillator
CT	6	8	I	Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length.
EAOUT	3	4	O	Output of the error amplifier for compensation
GND	10	13		Analog ground return pin
ILIM	9	12	I	Input to the current limit comparator
INV	1	2	I	Inverting input to the error amplifier
NI	2	3	I	Non-inverting input to the error amplifier
OUTA	11	14	O	High current totem pole output A of the on-chip drive stage.
OUTB	14	18	O	High current totem pole output B of the on-chip drive stage.
PGND	12	15		Ground return pin for the output driver stage
RAMP	7	9	I	Non-inverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation, this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input.
RT	5	7	I	Timing resistor connection pin for oscillator frequency programming
SS	8	10	I	Soft-start input pin which also doubles as the maximum duty cycle clamp.
VC	13	17		Power supply pin for the output stage. This pin should be bypassed with a 0.1- μF monolithic ceramic low ESL capacitor with minimal trace lengths.
VCC	15	19		Power supply pin for the device. This pin should be bypassed with a 0.1- μF monolithic ceramic low ESL capacitor with minimal trace lengths
VREF	16	20	O	5.1-V reference. For stability, the reference should be bypassed with a 0.1- μF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.

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6 Specifications

6.1 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			VALUE	UNIT
V_{IN}	Supply voltage,	VC, VCC	22	V
I_O	Source or sink current,DC	OUTA, OUTB	0.5	A
I_O	Source or sink current, pulse (0.5 μs)	OUTA, OUTB	2.2	A
	Analog inputs	INV, NI, RAMP	–0.3 to 7	V
		ILIM, SS	–0.3 to 6	V
	Power ground	PGND	±0.2	V
I_{CLK}	Clock output current	CLK/LEB	–5	mA
$I_{O(EA)}$	Error amplifier output current	EAOUT	5	mA
I_{SS}	Soft-start sink current	SS	20	mA
I_{OSC}	Oscillator charging current	RT	–5	mA
T_J	Operating virtual junction temperature range		–55 to 150	°C
T_{stg}	Storage temperature		–65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		–55 to 150	°C
t_{STG}	Storage temperature		–65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from cases for 10 seconds		300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Thermal Information

PACKAGE	θ_{JA}	θ_{JC}
J-16	80-120	28(2)
N-16	90(1)	45
DW-16	45-90(1)	25
PLCC-20 (Q package)	43-75(1)	34
LCC-20 (L package)	70-80	20(2)

(1) Specified θ_{JA} (junction to ambient) is for devices mounted to 5 in2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 in2 aluminum PC board. Test PWB was 0.062" thick and typically used 0.635 mm trace widths for power packages and 1.3 mm trace widths for non-power packages with 100 x 100 mil probe land area at the end of each trace.

(2) θ JC data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states, "The baseline values shown are worst case (mean + 2s) for a 60 x 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die size greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W".

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6.3 ELECTRICAL CHARACTERISTICS

T_A = –55°C to 125°C for the UC1823A/UC1825A, T_A = –40°C to 85°C for the UC2823x/UC2825x, T_A = 0°C to 70°C for the UC3823x/UC3825x, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 12 V, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE, V_{REF}						
V_O	Ouput voltage range	T_J = 25°C, I_O = 1 mA	5.05	5.1	5.15	V
	Line regulation	12 V ≤ VCC ≤ 20 V		2	15	mV
	Load regulation	1 mA ≤ I_O ≤ 10 mA		5	20	
	Total output variation	Line, load, temperature	5.03		5.17	V
	Temperature stability[1]	$T_{(min)}$ < T_A < $T_{(max)}$		0.2	0.4	mV/°C
	Output noise voltage[1]	10 Hz < f < 10 kHz		50		μ V_{RMS}
	Long term stability[1]	T_J = 125°C, 1000 hours		5	25	mV
	Short circuit current	VREF = 0 V	30	60	90	mA
OSCILLATOR						
f_{OSC}	Initial accuracy[1]	T_J = 25°C	375	400	425	kHz
		R_T = 6.6 kΩ, C_T = 220 pF, T_A = 25°C	0.9	1	1.1	MHz
	Total variation[1]	Line, temperature	350		450	kHz
		R_T = 6.6 kΩ, C_T = 220 pF	0.85		1.15	MHz
	Voltage stability	12 V < VCC < 20 V			1%	
	Temperature stability[1]	$T_{(min)}$ < T_A < $T_{(max)}$		±5%		
	High-level output voltage, clock		3.7	4		V
	Low-level output voltage, clock			0	0.2	
	Ramp peak		2.6	2.8	3	
	Ramp valley		0.7	1	1.25	
	Ramp valley-to-peak		1.6	1.8	2	
I_{OSC}	Oscillator discharge current	R_T = OPEN, V_{CT} = 2 V	9	10	11	mA
ERROR AMPLIFIER						
	Input offset voltage			2	10	mV
	Input bias current			0.6	3	μ A
	Input offset current			0.1	1	
	Open loop gain	1 V < V_O < 4 V	60	95		dB
CMRR	Common mode rejection ratio	1.5 V < V_{CM} < 5.5 V	75	95		
PSRR	Power supply rejection ratio	12 V < V_{CC} < 20 V	85	110		
$I_{O(sink)}$	Output sink current	V_{EAOUT} = 1 V	1	2.5		mA
$I_{O(src)}$	Output source current	V_{EAOUT} = 4 V		–1.3	–0.5	
	High-level output voltage	I_{EAOUT} = –0.5 mA	4.5	4.7	5	V
	Low-level output voltage	I_{EAOUT} = –1 mA	0	0.5	1	
	Gain bandwidth product	f = 200 kHz	6	12		Mhz
	Slew rate[1]		6	9		V/μ s

(1) Ensured by design. Not production tested.

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6.4 ELECTRICAL CHARACTERISTICS

T_A = –55°C to 125°C for the UC1823A/UC1825A, T_A = –40°C to 85°C for the UC2823x/UC2825x, T_A = 0°C to 70°C for the UC3823x/UC3825x, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 12 V, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIIONS	MIN	TYP	MAX	UNIT
PWM COMPARATOR						
I_{BIAS}	Bias current, RAMP	V_{RAMP} = 0 V		–1	–8	µA
	Minimum duty cycle				0%	
	Maximum duty cycle		85%			
t_{LEB}	Leading edge blanking time	R_{LEB} = 2 kΩ, C_{LEB} = 470 pF	300	375	450	ns
R_{LEB}	Leading edge blanking resistance	$V_{CLK/LEB}$ = 3 V	8.5	10.0	11.5	kΩ
V_{ZDC}	Zero dc threshold voltage, EAOUT	V_{RAMP} = 0 V	1.10	1.25	1.4	V
t_{DELAY}	Delay-to-output time(1)	V_{EAOUT} = 2.1 V, V_{ILIM} = 0 V to 2 V step		50	80	ns
CURRENT LIMIT / START SEQUENCE / FAULT						
I_{SS}	Soft-start charge current	V_{SS}= 2.5 V	8	14	20	µA
V_{SS}	Full soft-start threshold voltage		4.3	5		V
I_{DSCH}	Restart discharge current	V_{SS}= 2.5 V	100	250	350	µA
I_{SS}	Restart threshold voltage			0.3	0.5	V
I_{BIAS}	ILIM bias current	V_{ILIM} = 0 V to 2 V step			15	µA
I_{CL}	Current limit threshold voltage		0.95	1	1.05	V
	Overcurrent threshold voltage		1.14	1.2	1.26	
t_d	Delay-to-output time, ILIM(1)	V_{ILIM} = 0 V to 2 V step		50	80	ns
OUTPUT						
	Low-level output saturation voltage	I_{OUT} = 20 mA		0.25	0.4	V
		I_{OUT} = 200 mA		1.2	2.2	
	High-level output saturation voltage	I_{OUT} = -20 mA		1.9	2.9	
		I_{OUT} = -200 mA		2	3	
t_r, t_f	Rise/fall time(1)	C_L = 1 nF		20	45	ns
UNDERVOLTAGE LOCKOUT (UVLO)						
	Start threshold voltage	UC2823B, UC2825B, UC3825B, UC3825B		16	17	V
		UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A	8.4	9.2	9.6	
	Stop threshold voltage	UC2823B, UC2825B, UC3825B, UC3825B	9	10		
	OVLO hysteresis	UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A	0.4	0.8	1.2	
		UC2823B, UC2825B, UC3825B, UC3825B	5	6	7	
SUPPLY CURRENT						
I_{su}	Startup current	VC = VCC = V_{TH}(start) – 0.5 V		100	300	µA
I_{CC}	Input current			28	36	mA

(1) Ensured by design. Not production tested.

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7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 LEADING EDGE BLANKING

The UC3823A, UC2823B, UC3825A, and UC3825B perform fixed frequency pulse width modulation control. The UC3823A, and UC3823B outputs operate together at the switching frequency and can vary from zero to some value less than 100%. The UC3825A and UC3825B outputs are alternately controlled. During every other cycle, one output is off. Each output then switches at one-half the oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output(s) is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

Normally the PWM comparator senses a ramp crossing a control voltage (error amplifier output) and terminates the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking.

To program a leading edge blanking (LEB) period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10-kΩ resistor determines the blanked interval. The 10-kΩ resistor has a 10% tolerance. For more accuracy, an external 2-kΩ 1% resistor (R) can be added, resulting in an equivalent resistance of 1.66 kΩ with a tolerance of 2.4%. The design equation is:

$$t_{LEB} = 0.5 \times (R \parallel 10\ k\Omega) \times C \quad (1)$$

Values of R less than 2 kΩ should not be used.

Leading edge blanking is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the 1-V threshold, the pulse is terminated. The overcurrent comparator, however, is not blanked. It catches catastrophic overcurrent faults without a blanking delay. Any time the ILIM pin exceeds 1.2 V, the fault latch is set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.

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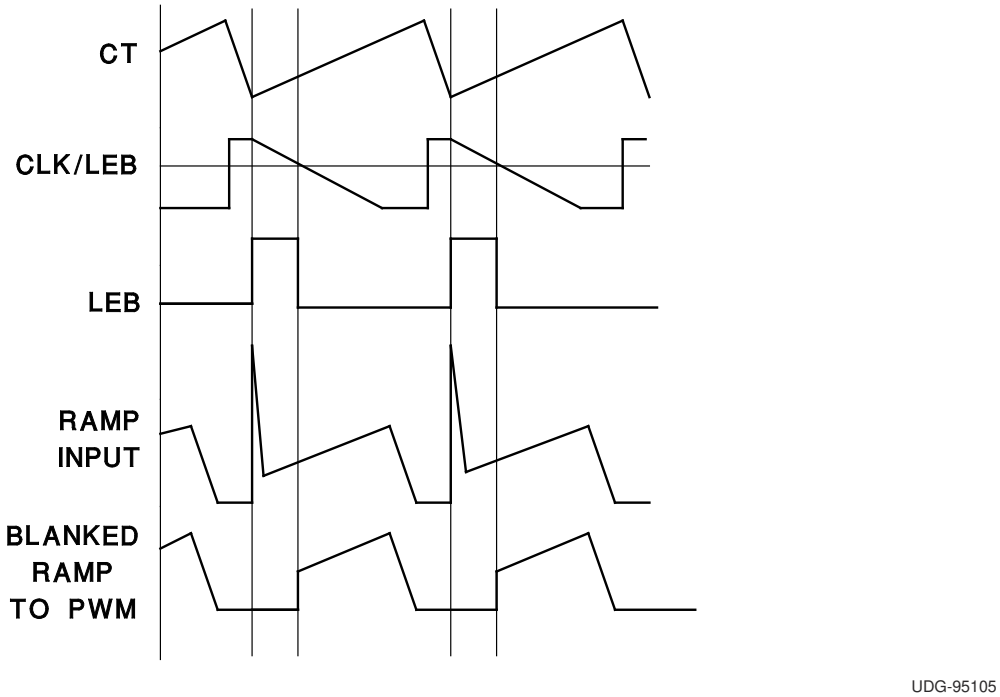


图 7-1. Leading Edge Blanking Operational Waveforms

7.2 UVLO、软启动和故障管理

软启动是通过 SS 引脚上的电容器编程的。上电时，SS 放电。当 SS 处于低电平状态时，误差放大器输出也被强制为低电平。当内部 9 µA 电源为 SS 引脚充电时，误差放大器输出会随之升高，直到闭环稳压状态。

无论何时 ILIM 超过 1.2V，故障锁存器会被置位，输出引脚会被驱动为低电平。软启动电容器然后会以 250 µA 的灌电流放电。在软启动完全放电且 ILIM 低于 1.2V 之前，不允许再出现输出脉冲。此时，故障锁存器复位，芯片执行软启动。

如果在软启动期间故障锁存被置位，则会立即终止输出，但软启动电容器在首次充满电之前不会放电。这会在连续故障情况下产生受控断续间隔。

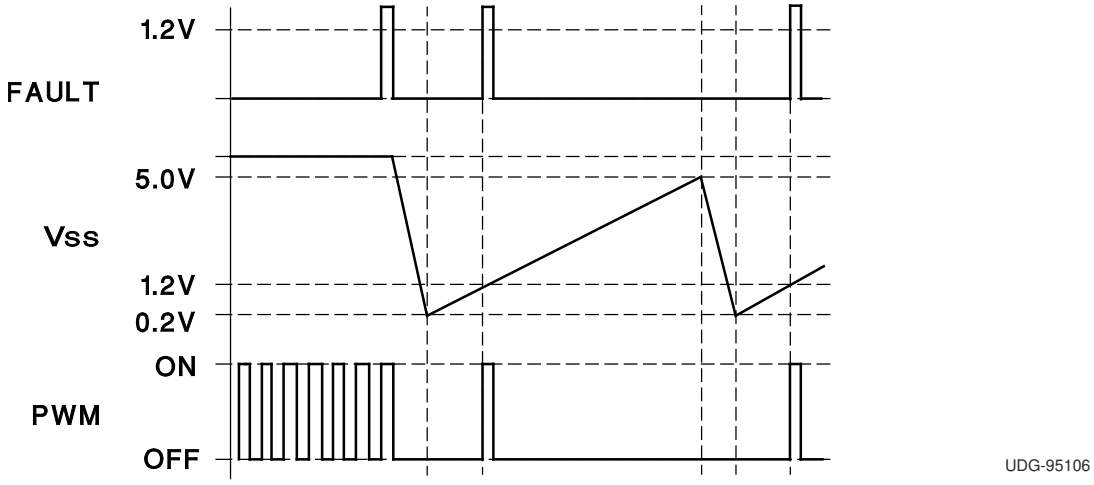


图 7-2. 软启动和故障波形

7.3 ACTIVE LOW OUTPUTS DURING UVLO

The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate.

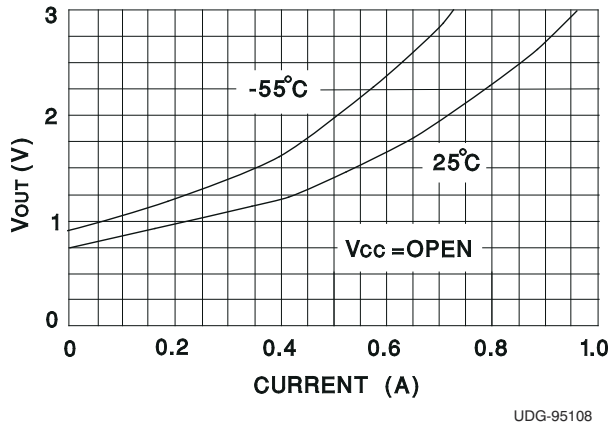


图 7-3. Output Voltage vs Output Current

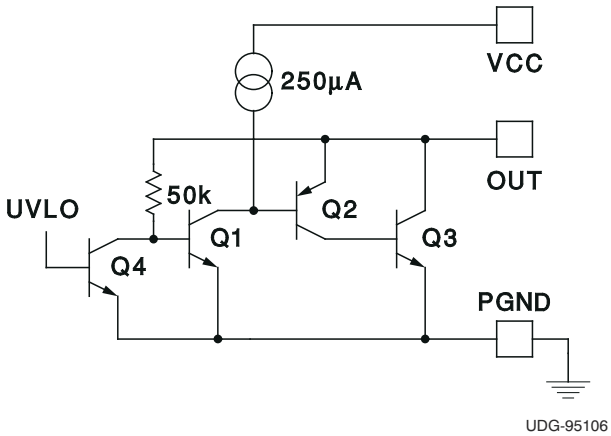


图 7-4. Output V and I During UVLO

7.4 CONTROL METHODS

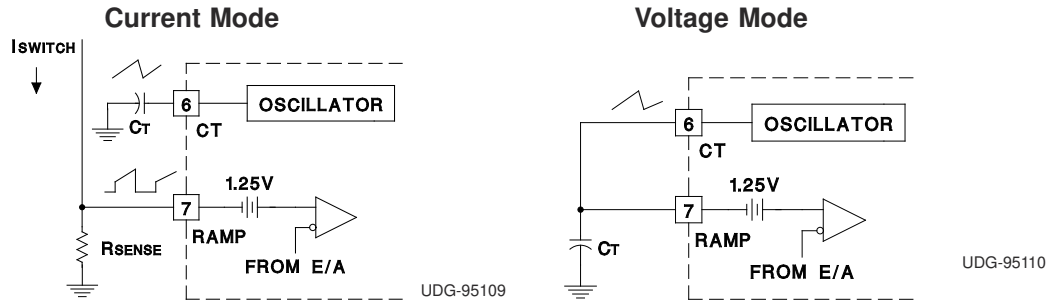


图 7-5. Control Methods

7.5 SYNCHRONIZATION

The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free running frequency of the oscillator to be 10% to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10 ns and less than half the discharge time of the oscillator. The rising edge of the CLK/LEB pin can be used to generate a synchronizing pulse for other chips. Note that the CLK/LEB pin no longer accepts an incoming synchronizing signal.

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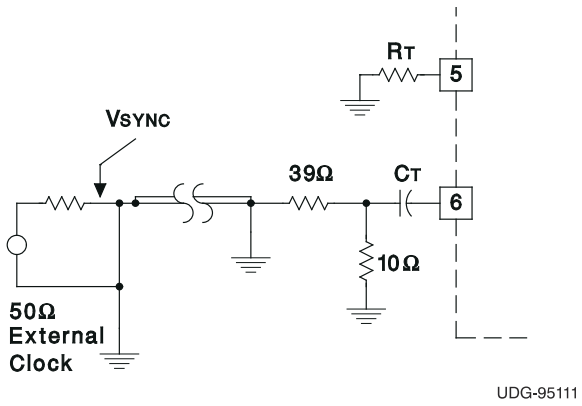


图 7-6. General Oscillator Synchronization

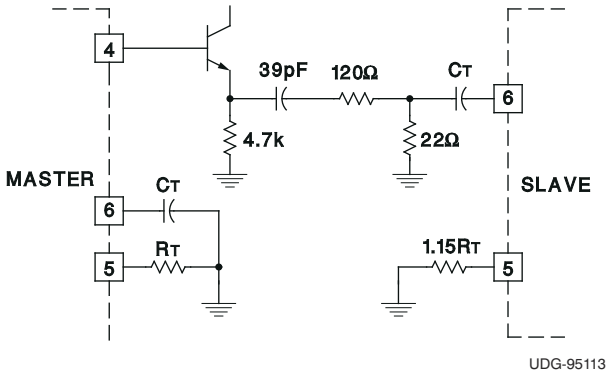


图 7-7. Two Unit Interface

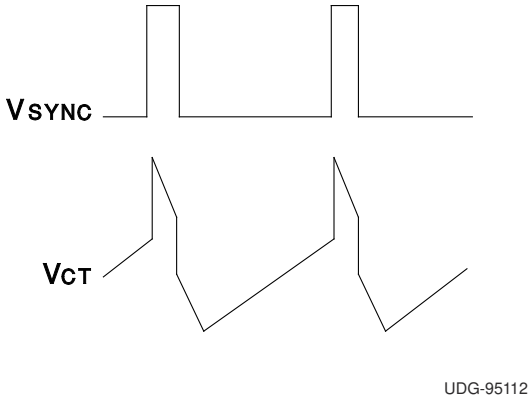


图 7-8. Operational Waveforms

7.6 HIGH CURRENT OUTPUTS

Each totem pole output of the UC3823A and UC3823AB, UC3825A, and UC3825B can deliver a 2-A peak current into a capacitive load. The output can slew a 1000-pF capacitor by 15 V in approximately 20 ns. Separate collector supply (VC) and power ground (PGND) pins help decouple the device's analog circuitry from the high-power gate drive noise. The use of 3-A Schottky diodes (1N5120, USD245, or equivalent) as shown in the 图 7-10 from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive/capacitive load, typical of a MOSFET gate. Schottky diodes must be used because a low forward voltage drop is required. DO NOT USE standard silicon diodes.

Although they are *single-ended* devices, two output drivers are available on the UC3823A and UC3823B devices. These can be *paralleled* by the use of a 0.5 Ω (noninductive) resistor connected in series with each output for a combined peak current of 4 A.

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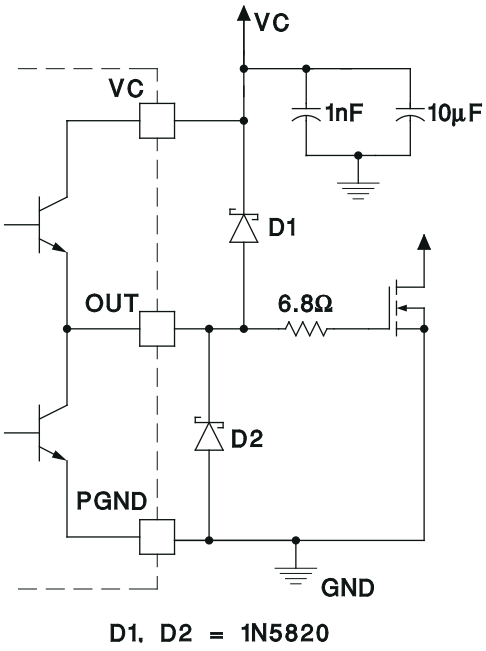


图 7-9. Power MOSFET Drive Circuit

7.7 GROUND PLANES

Each output driver of these devices is capable of 2-A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1-mF capacitors are recommended for both VCC and VREF. All analog circuitry should likewise be bypassed to the signal ground plane.

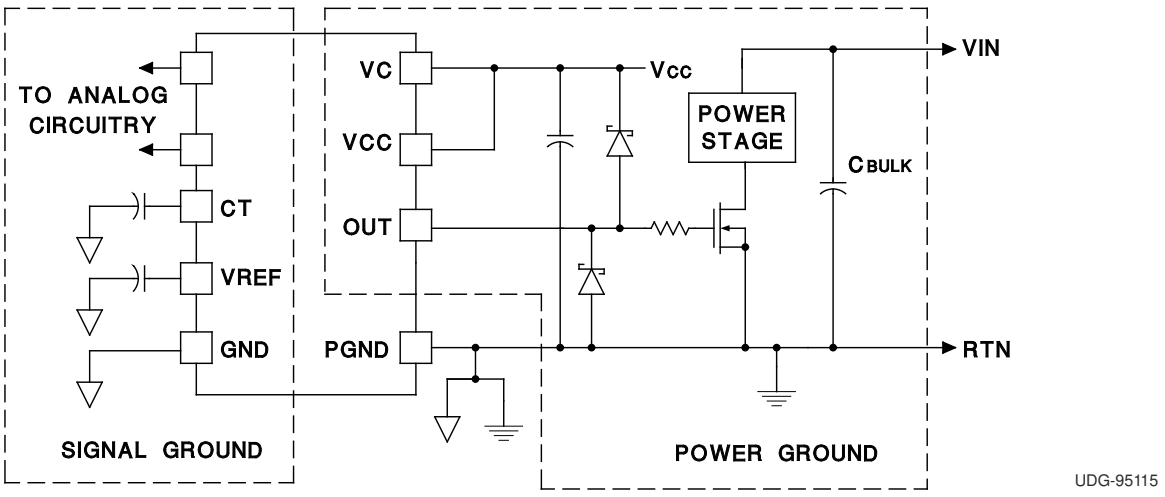


图 7-10. Ground Planes Diagram

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7.8 OPEN LOOP TEST CIRCUIT

This test fixture is useful for exercising many functions of this device family and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

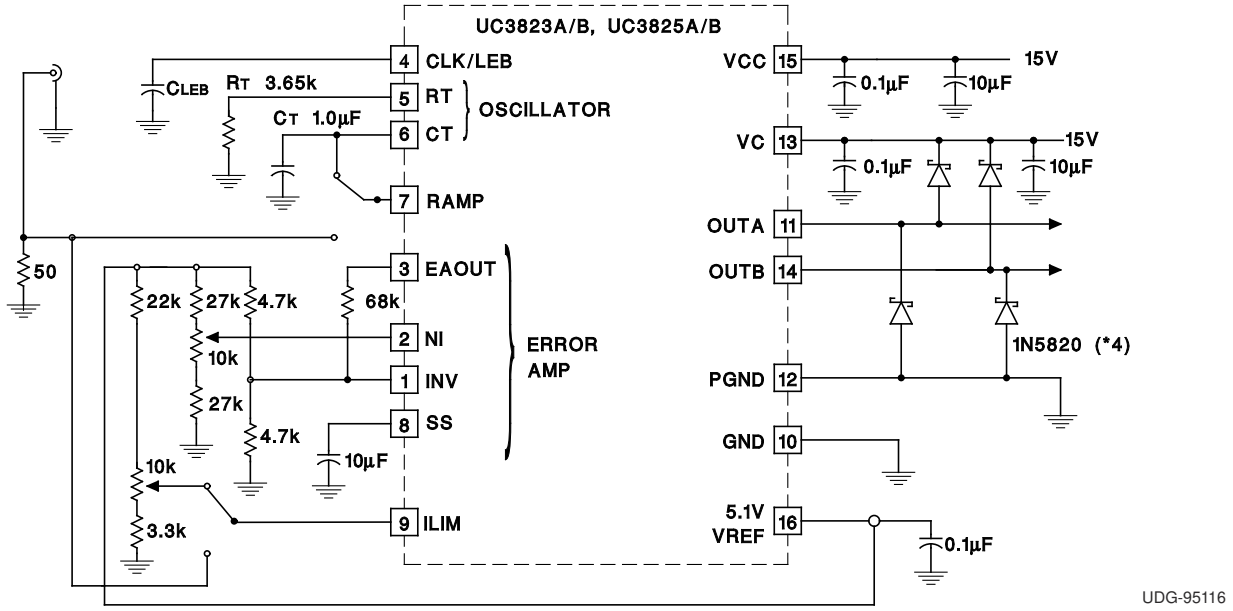


图 7-11. Open Loop Test Circuit Schematic

8 Device and Documentation Support

8.1 Documentation Support

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

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9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-87681022A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87681022A UC1825AL/883B
5962-8768102EA	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8768102EA UC1825AJ/883B
5962-89905022A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89905022A UC1823AL/883B
5962-8990502EA	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8990502EA UC1823AJ/883B
5962-8990502VEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8990502VEA UC1823AJQMLV
5962-8990502VEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8990502VEA UC1823AJQMLV
UC1823AJ	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1823AJ
UC1823AJ.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1823AJ
UC1823AJ883B	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8990502EA UC1823AJ/883B
UC1823AJ883B.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8990502EA UC1823AJ/883B
UC1823AL	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1823AL
UC1823AL.A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1823AL
UC1823AL883B	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89905022A UC1823AL/883B
UC1823AL883B.A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89905022A UC1823AL/883B

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC1825AJ	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1825AJ
UC1825AJ.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1825AJ
UC1825AJ883B	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8768102EA UC1825AJ/883B
UC1825AJ883B.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8768102EA UC1825AJ/883B
UC1825AL	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1825AL
UC1825AL.A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1825AL
UC1825AL883B	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87681022A UC1825AL/883B
UC1825AL883B.A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87681022A UC1825AL/883B
UC2823ADW	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2823ADW
UC2823ADW.A	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2823ADW
UC2823ADWTR	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2823ADW
UC2823ADWTR.A	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2823ADW
UC2823AN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2823AN
UC2823AN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2823AN
UC2823BDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2823BDW
UC2823BDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2823BDW
UC2825ADW	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2825ADW
UC2825ADW.A	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2825ADW
UC2825ADWG4	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2825ADW
UC2825ADWTR	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2825ADW
UC2825ADWTR.A	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2825ADW
UC2825ADWTRG4	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2825ADW
UC2825AN	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2825AN
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UC2825ANG4	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2825AN

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
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UC2825BDW.A	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2825BDW
UC2825BDWG4	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2825BDW
UC2825BN	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2825BN
UC2825BN.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2825BN
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UC3823ADWTR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3823ADW
UC3823ADWTR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3823ADW
UC3823AN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3823AN
UC3823AN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3823AN
UC3823BDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3823BDW
UC3823BDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3823BDW
UC3823BDWTR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3823BDW
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UC3825ADW.A	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3825ADW
UC3825ADWG4	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3825ADW
UC3825ADWTR	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3825ADW
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UC3825ADWTRG4	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3825ADW
UC3825AN	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3825AN
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UC3825ANG4	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3825AN
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UC3825BDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3825BDW
UC3825BDWTR	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	0 to 70	UC3825BDW
UC3825BN	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3825BN
UC3825BN.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3825BN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC1823A, UC1823A-SP, UC1825A, UC2825A, UC3823A, UC3825A :

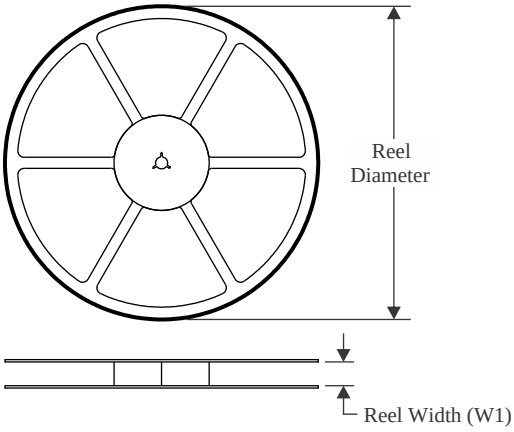
- Catalog : UC3823A, UC1823A, UC3825A
- Automotive : UC2825A-Q1
- Enhanced Product : UC2825A-EP
- Military : UC1823A, UC1825A
- Space : UC1823A-SP, UC1825A-SP

NOTE: Qualified Version Definitions:

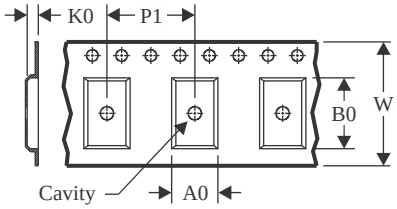
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

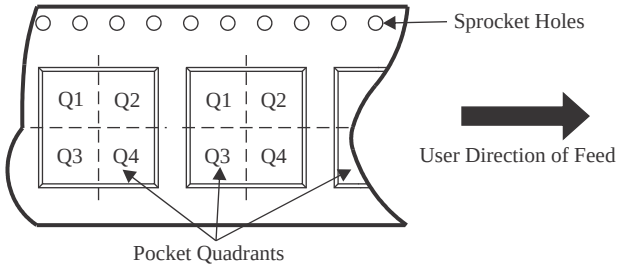


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

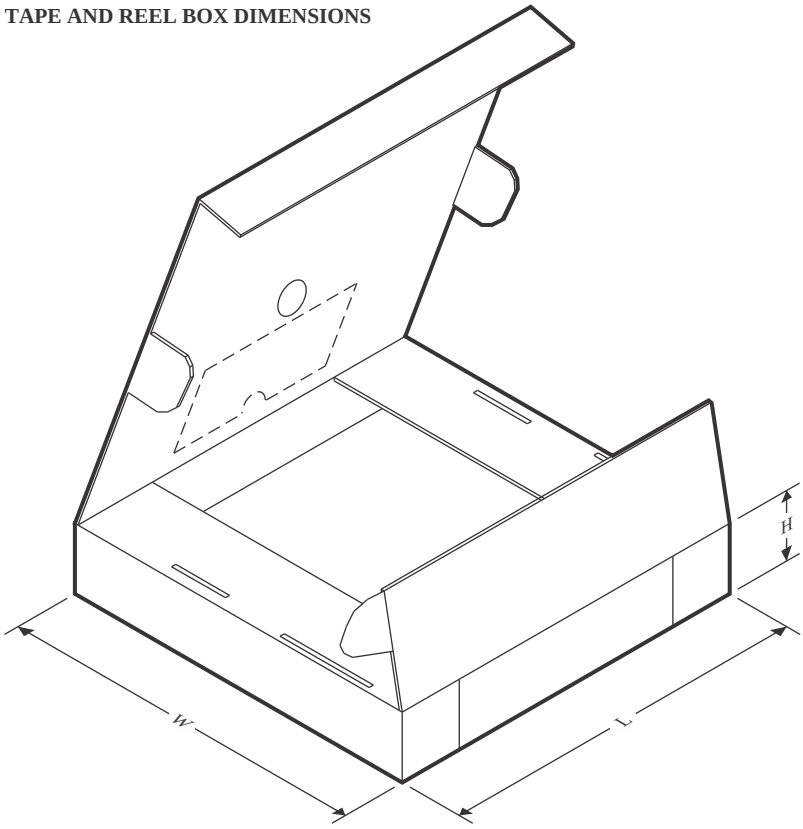
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2823ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC2825ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3823ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3823BDWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3825ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

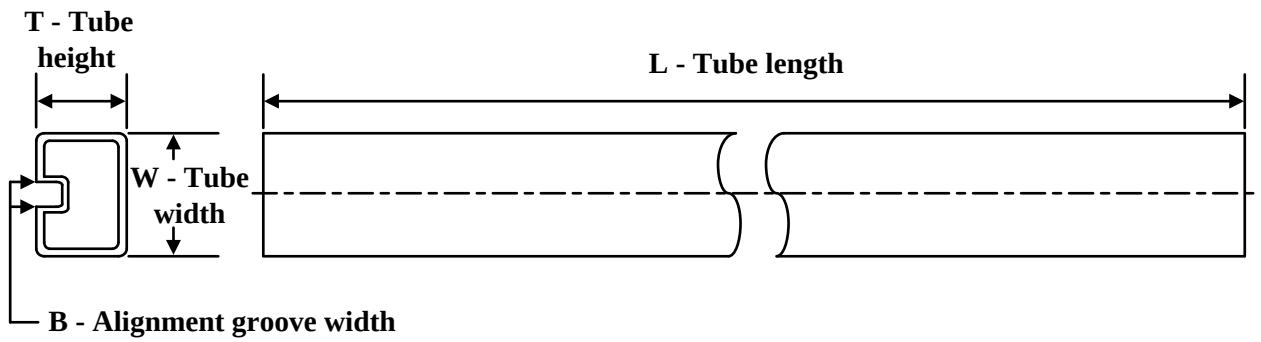
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2823ADWTR	SOIC	DW	16	2000	353.0	353.0	32.0
UC2825ADWTR	SOIC	DW	16	2000	353.0	353.0	32.0
UC3823ADWTR	SOIC	DW	16	2000	353.0	353.0	32.0
UC3823BDWTR	SOIC	DW	16	2000	353.0	353.0	32.0
UC3825ADWTR	SOIC	DW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-87681022A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-89905022A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1823AL	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1823AL.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1823AL883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1823AL883B.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1825AJ	J	CDIP	16	25	506.98	15.24	13440	NA
UC1825AJ.A	J	CDIP	16	25	506.98	15.24	13440	NA
UC1825AL	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1825AL.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1825AL883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1825AL883B.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC2823ADW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2823ADW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC2823AN	N	PDIP	16	25	506	13.97	11230	4.32
UC2823AN.A	N	PDIP	16	25	506	13.97	11230	4.32
UC2823BDW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2823BDW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC2825ADW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2825ADW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC2825ADWG4	DW	SOIC	16	40	507	12.83	5080	6.6
UC2825AN	N	PDIP	16	25	506	13.97	11230	4.32
UC2825AN.A	N	PDIP	16	25	506	13.97	11230	4.32
UC2825ANG4	N	PDIP	16	25	506	13.97	11230	4.32
UC2825BDW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2825BDW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC2825BDWG4	DW	SOIC	16	40	507	12.83	5080	6.6
UC2825BN	N	PDIP	16	25	506	13.97	11230	4.32
UC2825BN.A	N	PDIP	16	25	506	13.97	11230	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC3823ADW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3823ADW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC3823AN	N	PDIP	16	25	506	13.97	11230	4.32
UC3823AN.A	N	PDIP	16	25	506	13.97	11230	4.32
UC3823BDW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3823BDW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC3825ADW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3825ADW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC3825ADWG4	DW	SOIC	16	40	507	12.83	5080	6.6
UC3825AN	N	PDIP	16	25	506	13.97	11230	4.32
UC3825AN.A	N	PDIP	16	25	506	13.97	11230	4.32
UC3825ANG4	N	PDIP	16	25	506	13.97	11230	4.32
UC3825BDW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3825BDW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC3825BN	N	PDIP	16	25	506	13.97	11230	4.32
UC3825BN.A	N	PDIP	16	25	506	13.97	11230	4.32

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