DRV8812 Dual-Bridge Motor Controller IC

1 Features

- 8.2-V to 45-V Operating Supply Voltage Range
- 1.6-A Maximum Drive Current at 24 V and T_A = 25°C
- Dual H-Bridge Current Control Motor Driver
  - Drive a Bipolar Stepper or Two DC Motors
  - Four Level Winding Current Control
- Multiple Decay Modes
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Industry Standard Parallel Digital Control Interface
- Low Current Sleep Mode
- Built In 3.3-V Reference Output Small Package and Footprint
- Protection Features
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - VM Undervoltage Lockout (UVLO)
  - Fault Condition Indication Pin (nFAULT)

2 Applications

- Automatic Teller Machines
- Money Handling Machines
- Video Security Cameras
- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

3 Description

The DRV8812 provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has two H-bridge drivers, and can drive a bipolar stepper motor or two DC motors. The output driver block for each consists of N-channel power MOSFET's configured as full H-bridges to drive the motor windings. The DRV8812 is capable of driving up to 1.6-A of output current (with proper heatsinking, at 24 V and 25°C).

A simple parallel digital control interface is compatible with industry-standard devices. Decay mode is programmable.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature.

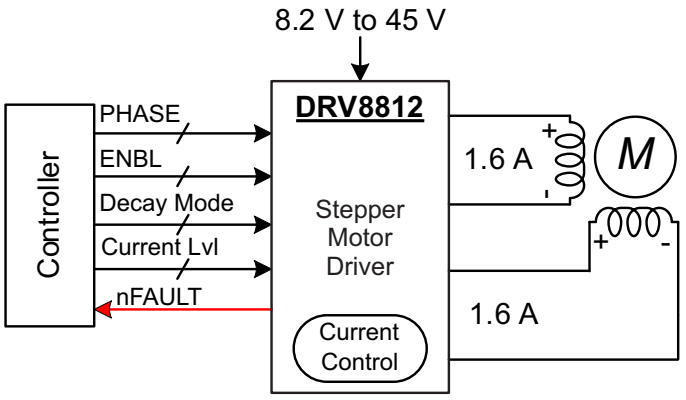
The DRV8812 is available in a 28-pin HTSSOP package with PowerPAD™ and in a 28-pin QFN package PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8812	HTSSOP (28)	9.70 mm x 4.40 mm
	VQFN (28)	5.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

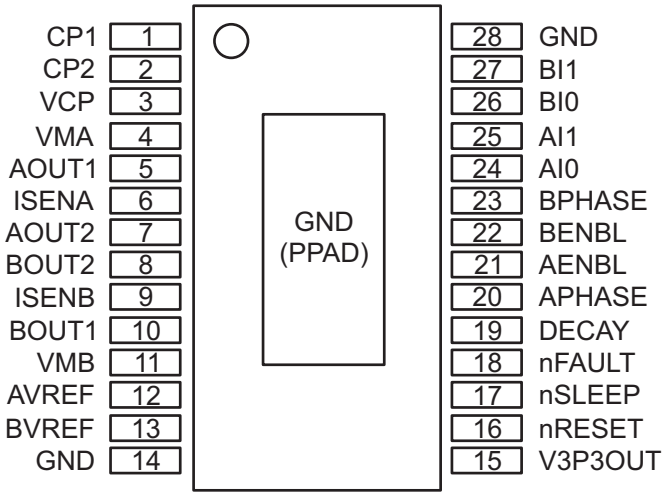
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2013) to Revision G	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	5

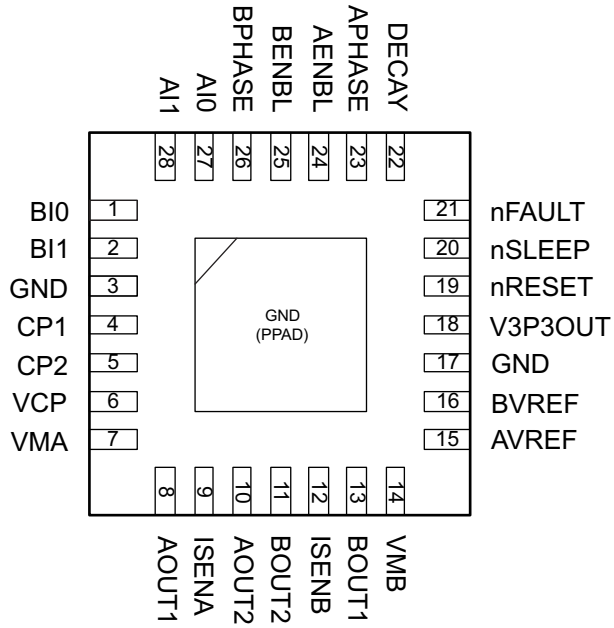
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5 Pin Configuration and Functions

PWP Package
28 Pin HTSSOP
Top View



RHD Package
28-Pin VQFN
Top View



Pin Functions

PIN			I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	PWP	RHD			
POWER AND GROUND					
GND	14, 28	3, 17	-	Device ground	
VMA	4	7	-	Bridge A power supply	Connect to motor supply (8.2-V to 45-V). Both pins must be connected to the same supply, bypassed with a 0.1uF capacitor to GND, and connected to appropriate bulk capacitance.
VMB	11	14	-	Bridge B power supply	
V3P3OUT	15	18	O	3.3-V regulator output	Bypass to GND with a 0.47-µF 6.3-V ceramic capacitor. Can be used to supply VREF.
CP1	1	4	IO	Charge pump flying capacitor	Connect a 0.01-µF 50-V capacitor between CP1 and CP2.
CP2	2	5	IO	Charge pump flying capacitor	
VCP	3	6	IO	High-side gate drive voltage	Connect a 0.1-µF 16-V ceramic capacitor and a 1-MΩ resistor to VM.
CONTROL					
AENBL	21	24	I	Bridge A enable	Logic high to enable bridge A
APHASE	20	23	I	Bridge A phase (direction)	Logic high sets AOUT1 high, AOUT2 low
AI0	24	27	I	Bridge A current set	Sets bridge A current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0
AI1	25	28	I		
BENBL	22	25	I	Bridge B enable	Logic high to enable bridge B
BPHASE	23	26	I	Bridge B phase (direction)	Logic high sets BOUT1 high, BOUT2 low
BI0	26	1	I	Bridge B current set	Sets bridge B current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0
BI1	27	2	I		
DECAY	19	22	I	Decay mode	Low = slow decay, open = mixed decay, high = fast decay
nRESET	16	19	I	Reset input	Active-low reset input initializes internal logic and disables the H-bridge outputs
nSLEEP	17	20	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode
AVREF	12	15	I	Bridge A current set reference input	Reference voltage for winding current set. Can be driven individually with an external DAC for microstepping, or tied to a reference (e.g., V3P3OUT). A 0.01-µF bypass capacitor to GND is recommended.
BVREF	13	16	I	Bridge B current set reference input	
STATUS					
nFAULT	18	21	OD	Fault	Logic low when in fault condition (overtemp, overcurrent)
OUTPUT					
ISENA	6	9	IO	Bridge A ground / Isense	Connect to current sense resistor for bridge A
ISENB	9	12	IO	Bridge B ground / Isense	Connect to current sense resistor for bridge B
AOUT1	5	8	O	Bridge A output 1	Connect to motor winding A
AOUT2	7	10	O	Bridge A output 2	
BOUT1	10	13	O	Bridge B output 1	Connect to motor winding B
BOUT2	8	11	O	Bridge B output 2	

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
VMx	Power supply voltage	–0.3	47	V
VMx	Power supply ramp rate		1	V/µs
	Digital pin voltage	–0.5	7	V
VREF	Input voltage	–0.3	4	V
	ISENSEx pin voltage (3)	–0.8	0.8	V
	Peak motor drive output current, t < 1 µS	Internally limited		A
	Continuous motor drive output current (4)	0	1.6	A
	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating virtual junction temperature	–40	150	°C
T_A	Operating ambient temperature	–40	85	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Transients of ±1 V for less than 25 ns are acceptable
(4) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range (1)	8.2		45	V
V_{REF}	VREF input voltage (2)	1		3.5	V
I_{V3P3}	V3P3OUT load current			1	mA

(1) All V_M pins must be connected to the same supply voltage.
(2) Operational at VREF between 0 V and 1 V, but accuracy is degraded.

6.4 Thermal Information

THERMAL METRIC (1)		DRV8812 PWP (HTSSOP) 28 PINS	DRV8812 RHD (VQFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.9	35.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.3	25.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.2	8.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.9	8.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		5	8	mA
I_{VMQ}	VM sleep mode supply current	V_M = 24 V		10	20	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		7.8	8.2	V
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA, V_M = 24 V, T_J = 25°C	3.18	3.30	3.42	V
		IOUT = 0 to 1 mA	3.10	3.30	3.50	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2		5.25	V
V_{HYS}	Input hysteresis			0.45		V
I_{IL}	Input low current	VIN = 0	–20		20	µA
I_{IH}	Input high current	VIN = 3.3 V			100	µA
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
DECAY INPUT						
V_{IL}	Input low threshold voltage	For slow decay mode	0		0.8	V
V_{IH}	Input high threshold voltage	For fast decay mode	2			V
I_{IN}	Input current				±40	µA
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.63		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.76	0.90	Ω
$R_{DS(ON)}$	LS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.65		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.78	0.90	Ω
I_{OFF}	Off-state leakage current		–20		20	µA
MOTOR DRIVER						
f_{PWM}	Internal PWM frequency			50		kHz
t_{BLANK}	Current sense blanking time			3.75		µs
t_R	Rise time	V_M = 24 V	100		360	ns
t_F	Fall time	V_M = 24 V	80		250	ns
t_{DEAD}	Dead time			400		ns
t_{DEG}	Input deglitch time		1.3		2.9	µs
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.8		5	A
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
CURRENT CONTROL						
I_{REF}	xVREF input current	xVREF = 3.3 V	–3		3	µA
V_{TRIP}	xISENSE trip voltage	xVREF = 3.3 V, 100% current setting	635	660	685	mV
		xVREF = 3.3 V, 71% current setting	445	469	492	mV
		xVREF = 3.3 V, 38% current setting	225	251	276	mV
A_{ISENSE}	Current sense amplifier gain	Reference only		5		V/V

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6.6 Typical Characteristics

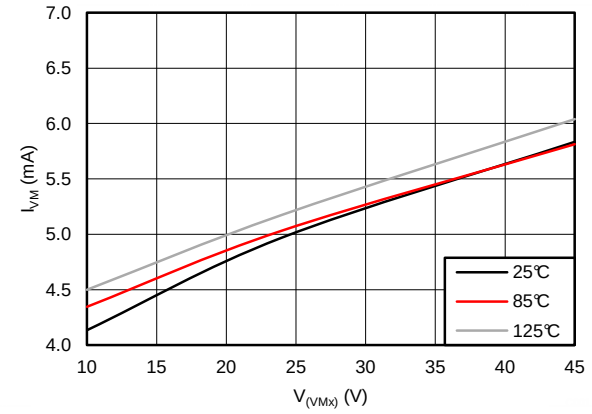


Figure 1. I_{VMx} vs $V_{(VMx)}$

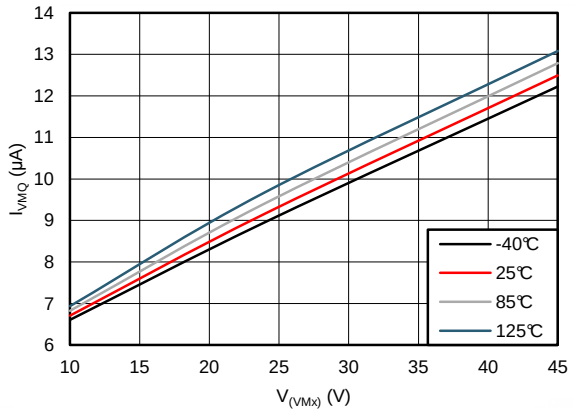


Figure 2. I_{VMxQ} vs $V_{(VMx)}$

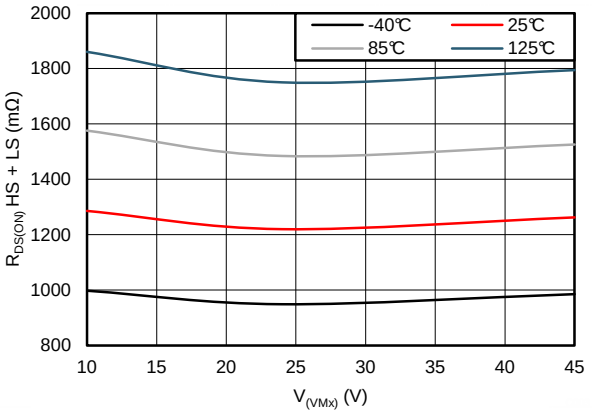


Figure 3. $R_{DS(ON)}$ vs $V_{(VMx)}$

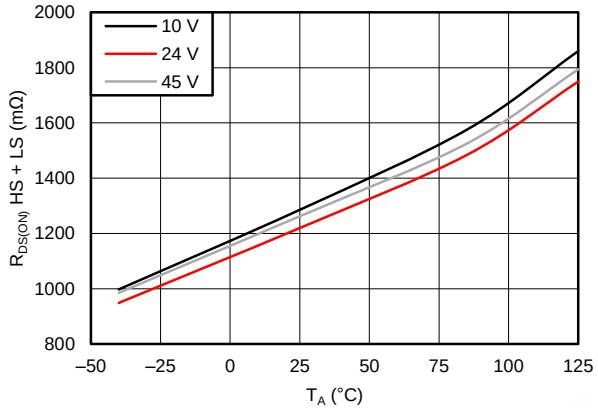


Figure 4. $R_{DS(ON)}$ vs Temperature

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7 Detailed Description

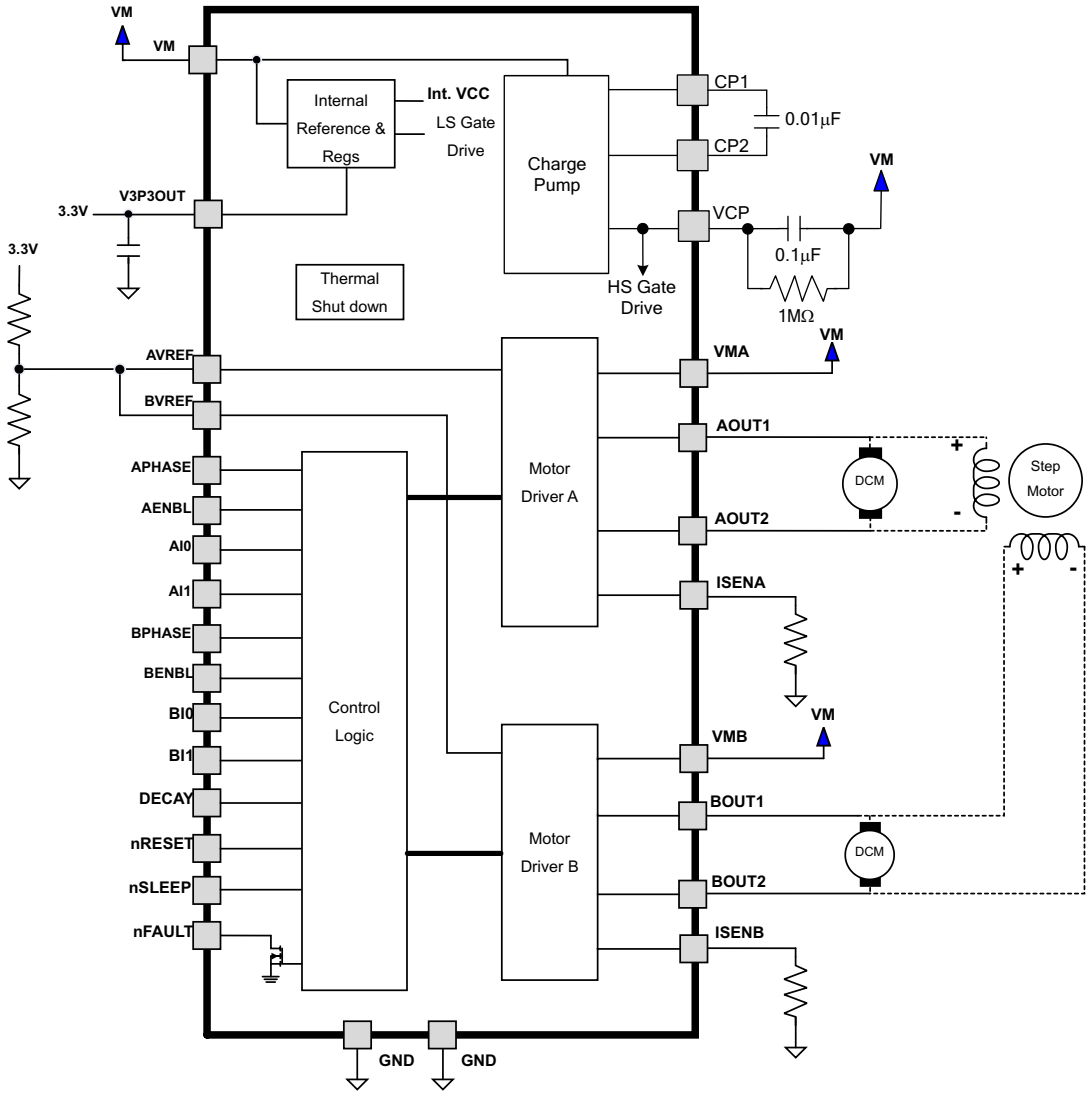
7.1 Overview

The DRV8812 is an integrated motor driver solution for a bipolar stepper motor or two brushed DC motors. The device integrates two NMOS H-bridges, current sense, regulation circuitry, and detailed fault detection. The DRV8813 can be powered with a supply voltage between 8.2 V and 45 V and is capable of providing an output current up to 1.6 A full-scale.

A PHASE/ENBL interface allows for simple interfacing to the controller circuit. The winding current control allows the external controller to adjust the regulated current that is provided to the motor. The current regulation is highly configurable, with three decay modes of operation. Fast, slow, and mixed decay can be selected depending on the application requirements.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8812 contains two H-bridge motor drivers with current-control PWM circuitry. A block diagram of the motor control circuitry is shown in Figure 5. A bipolar stepper motor is shown, but the drivers can also drive two separate DC motors.

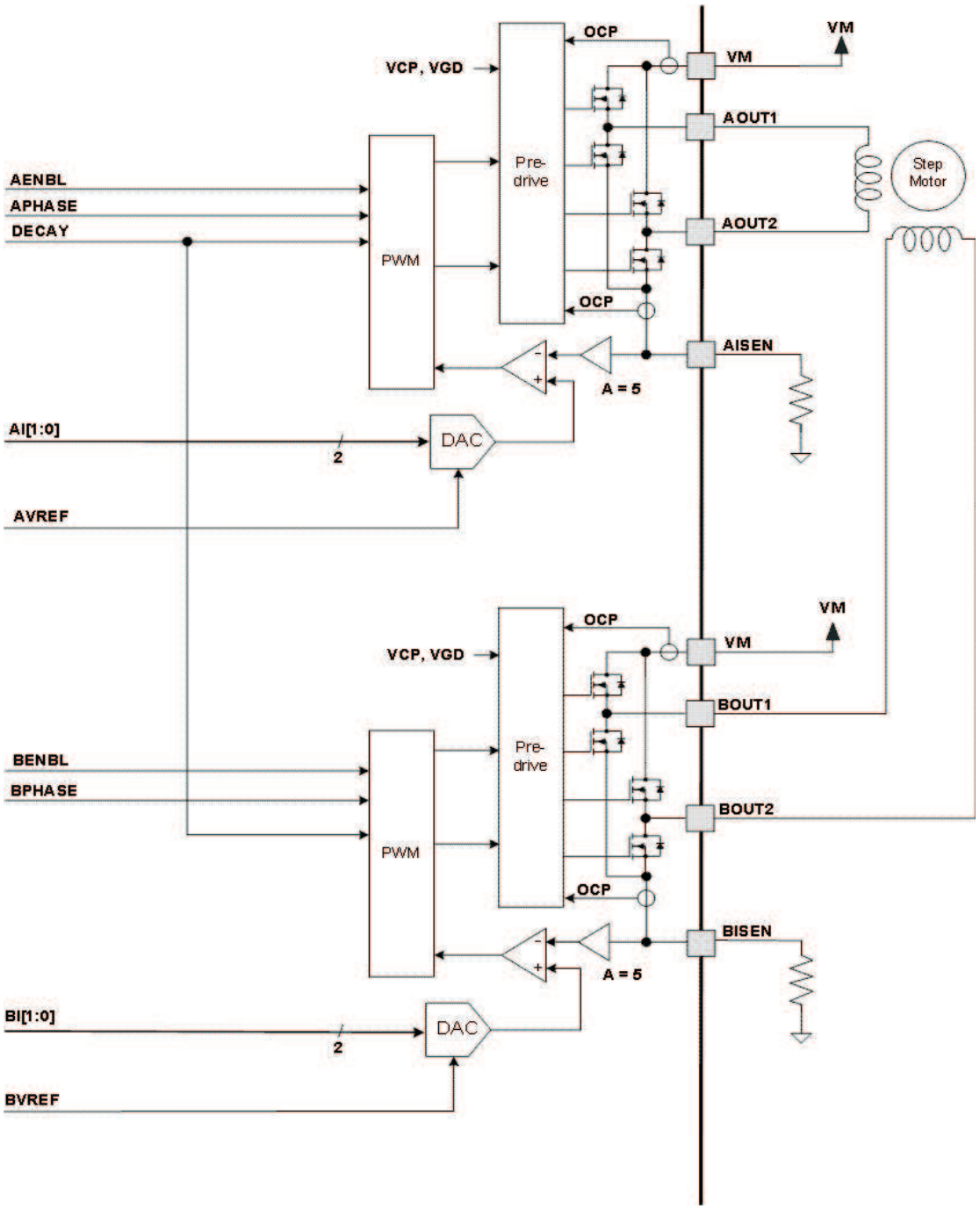


Figure 5. Motor Control Circuitry

Note that there are multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

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7.4 Device Functional Modes

7.4.1 Bridge Control

The xPHASE input pins control the direction of current flow through each H-bridge. The xENBL input pins enable the H-bridge outputs when active high. Table 1 shows the logic.

Table 1. H-Bridge Logic

xENBL	xPHASE	xOUT1	xOUT2
0	X	Z	Z
1	1	H	L
1	0	L	H

7.4.2 Current Regulation

The current through the motor windings is regulated by a fixed-frequency PWM current regulation, or current chopping. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For stepping motors, current regulation is normally used at all times, and can changing the current can be used to microstep the motor. For DC motors, current regulation is used to limit the start-up and stall current of the motor.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins, and is scaled by a 2-bit DAC that allows current settings of 100%, 71%, 38% of full-scale, plus zero.

The full-scale (100%) chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{V_{REFX}}{5 \times R_{ISENSE}} \quad (1)$$

Example:

If a 0.5-Ω sense resistor is used and the VREFx pin is 3.3 V, the full-scale (100%) chopping current will be 3.3 V / (5 x 0.5 Ω) = 1.32 A.

Two input pins per H-bridge (xI1 and xI0) are used to scale the current in each bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The function of the pins is shown in

Table 2.

Table 2. H-Bridge Pin Functions

xI1	xI0	RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)
1	1	0% (Bridge disabled)
1	0	38%
0	1	71%
0	0	100%

Note that when both xI bits are 1, the H-bridge is disabled and no current flows.

Example:

If a 0.5-Ω sense resistor is used and the VREF pin is 3.3 V, the chopping current will be 1.32 A at the 100% setting (xI1, xI0 = 00). At the 71% setting (xI1, xI0 = 01) the current will be 1.32 A x 0.71 = 0.937 A, and at the 38% setting (xI1, xI0 = 10) the current will be 1.32 A x 0.38 = 0.502 A. If (xI1, xI0 = 11) the bridge will be disabled and no current will flow.

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7.4.3 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 6 as case 1. The current flow direction shown indicates the state when the xENBL pin is high.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 6 as case 2.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 6 as case 3.

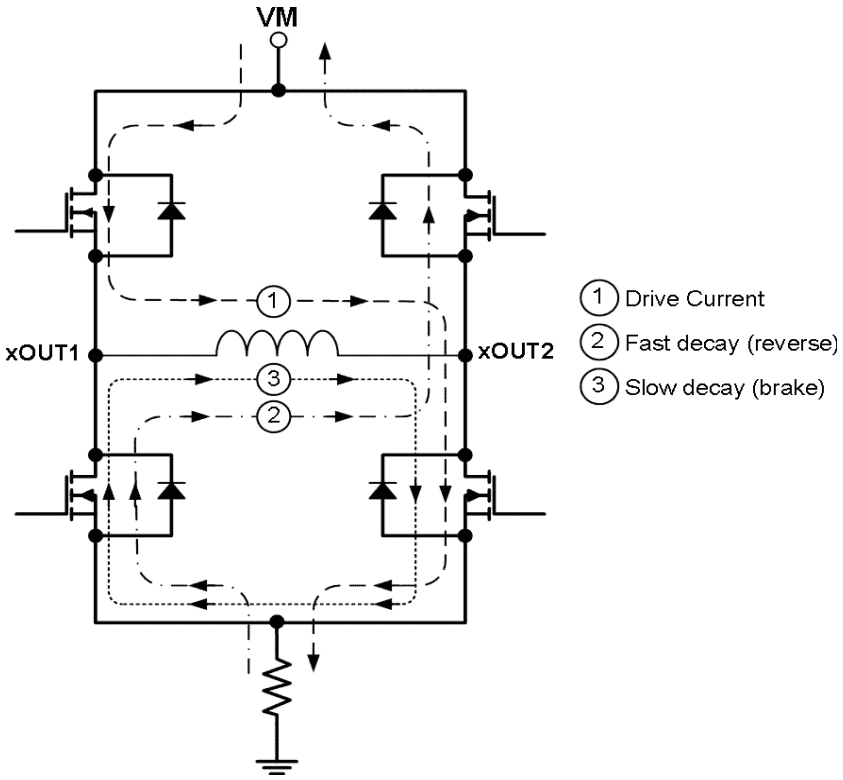


Figure 6. Decay Mode

The DRV8812 supports fast decay, slow decay and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY pin - logic low selects slow decay, open selects mixed decay operation, and logic high sets fast decay mode. Note that the DECAY pin sets the decay mode for both H-bridges.

Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period.

7.4.4 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. Note that the blanking time also sets the minimum on time of the PWM.

7.4.5 nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge drivers. All inputs are ignored while nRESET is active.

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Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational.

7.4.6 Protection Circuits

The DRV8812 is fully protected against undervoltage, overcurrent and overtemperature events.

7.4.6.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device will remain disabled until either nRESET pin is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or VREF voltage.

7.4.6.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

7.4.6.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when V_M rises above the UVLO threshold.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8812 can be used to control a bipolar stepper motor. The PHASE/ENBL interface controls the outputs and current control can be implemented with the internal current regulation circuitry. Detailed fault reporting is provided with the internal protection circuits and nFAULT pin.

8.2 Typical Application

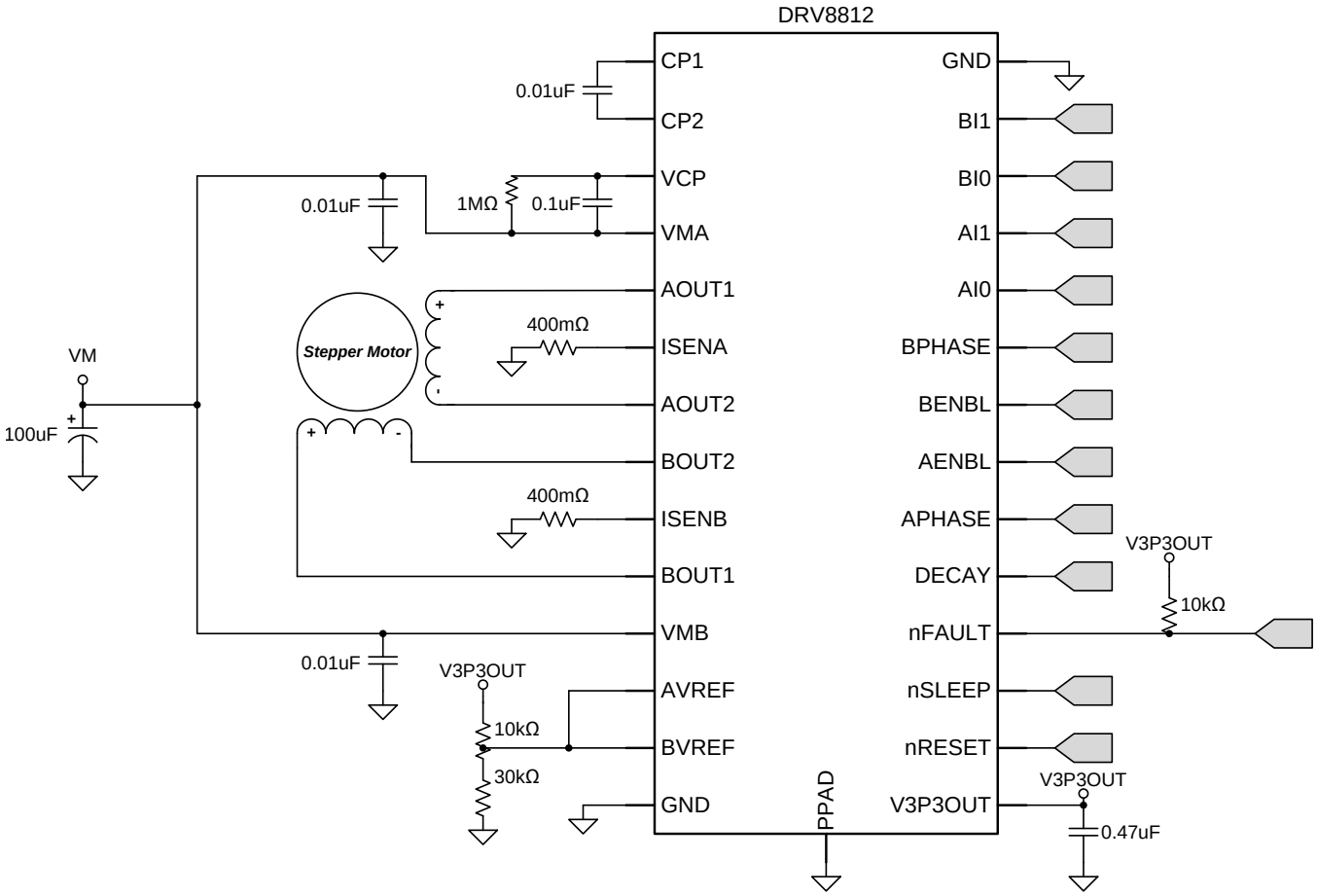


Figure 7. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 3. Design Parameters

PARAMETER	REFERENCE	VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	3.9 Ω
Motor winding inductance	I_L	2.9 mH
Sense resistor value	R_{SENSE}	400 mΩ
Target full-scale current	I_{FS}	1.25 A

8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

In a stepper motor, the set full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the xVREF analog voltage and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step. The gain of DRV8812 is set for 5 V/V.

$$I_{FS}(A) = \frac{xVREF(V)}{A_V \times R_{SENSE}(\Omega)} = \frac{xVREF(V)}{5 \times R_{SENSE}(\Omega)} \quad (2)$$

To achieve I_{FS} = 1.25 A with R_{SENSE} of 0.2 Ω, xVREF should be 1.25 V.

8.2.2.2 Decay Modes

The DRV8812 supports three different decay modes: slow decay, fast decay, and mixed decay. The current through the motor windings is regulated using a fixed-frequency PWM scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8812 will place the winding in one of the three decay modes until the PWM cycle has expired. Afterward, a new drive phase starts.

The blanking time, t_{BLANK}, defines the minimum drive time for the current chopping. I_{TRIP} is ignored during t_{BLANK}, so the winding current may overshoot the trip level.

8.2.2.3 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $Irms^2$ x R. For example, if the rms motor current is 2-A and a 100-m Ω sense resistor is used, the resistor will dissipate 2 A^2 × 0.1 Ω = 0.4 W. The power quickly increases with greater current levels.

Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

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8.2.3 Application Curves

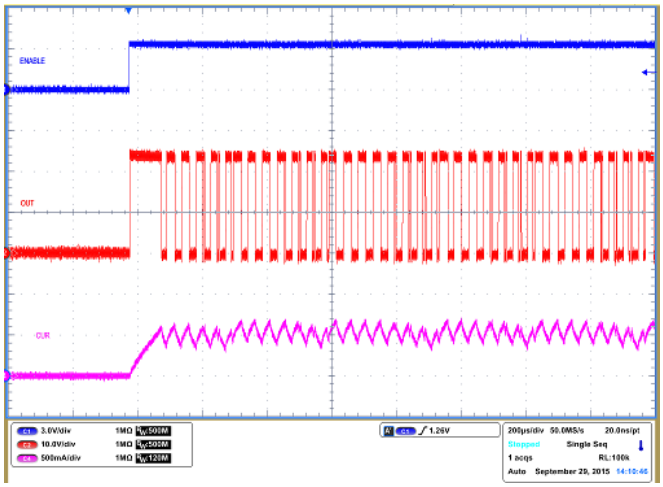


Figure 8. DRV8828 Current Limiting

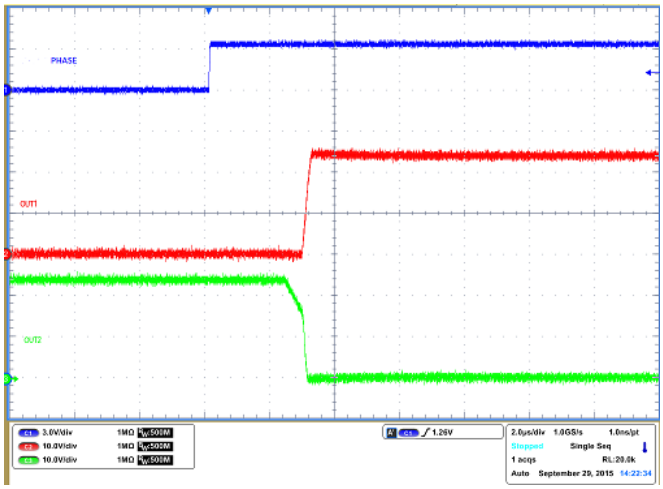


Figure 9. DRV8828 Direction Change

9 Power Supply Recommendations

The DRV8812 is designed to operate from an input voltage supply (VMx) range between 8.2 and 45 V. Two 0.1-µF ceramic capacitors rated for VMx must be placed as close as possible to the VMA and VMB pins respectively (one on each pin). In addition to the local decoupling caps, additional bulk capacitance is required and must be sized accordingly to the application requirements.

9.1 Bulk Capacitance

Bulk capacitance sizing is an important factor in motor drive system design. It is dependent on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. You should size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet generally provides a recommended value but system level testing is required to determine the appropriate sized bulk capacitor.

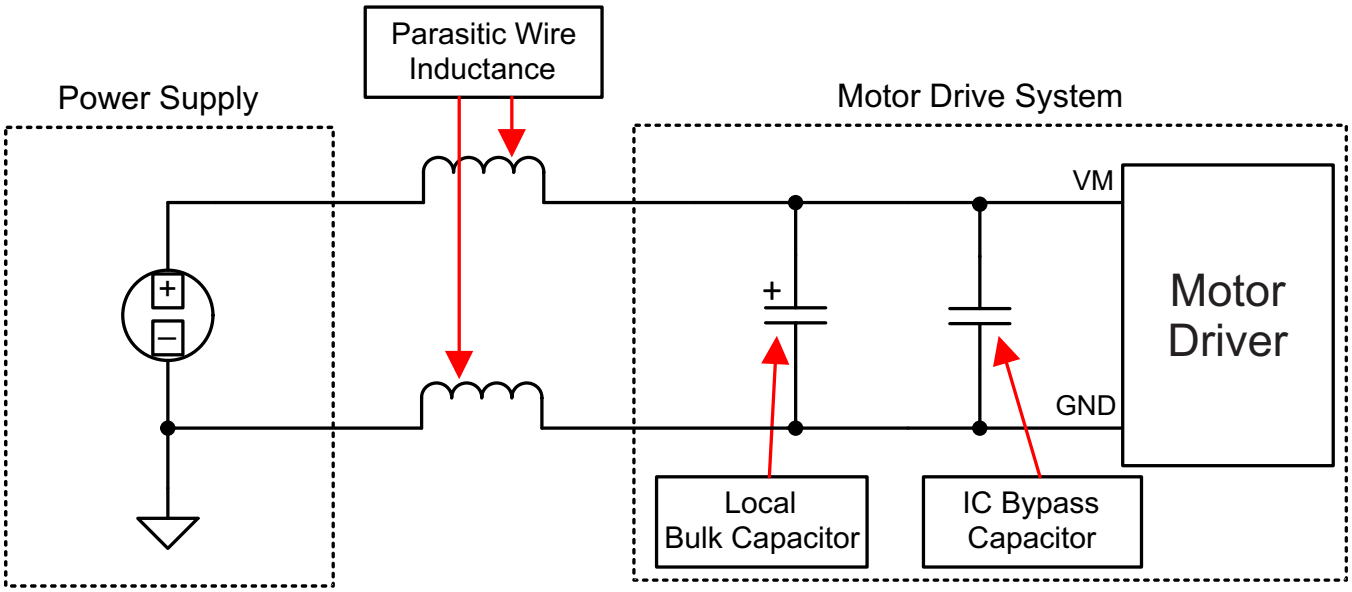


Figure 10. Setup of Motor Drive System With External Power Supply

9.2 Power Supply and Logic Sequencing

There is no specific sequence for powering-up the DRV8812. It is okay for digital input signals to be present before VMx is applied. After VMx is applied to the DRV8812, it begins operation based on the status of the control pins.

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10 Layout

10.1 Layout Guidelines

The VMA and VMB pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1-µF rated for VMx. This capacitor should be placed as close to the VMA and VMB pins as possible with a thick trace or ground plane connection to the device GND pin.

The VMA and VMB pins must be bypassed to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8812.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. TI recommends a value of 0.01-µF rated for VMx. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VMA and VCP pins. TI recommends a value of 0.1-µF rated for 16 V. Place this component as close to the pins as possible. Also, place a 1-MΩ resistor between VCP and VMA.

Bypass V3P3 to ground with a ceramic capacitor rated 6.3 V. Place this bypass capacitor as close to the pin as possible

10.2 Layout Example

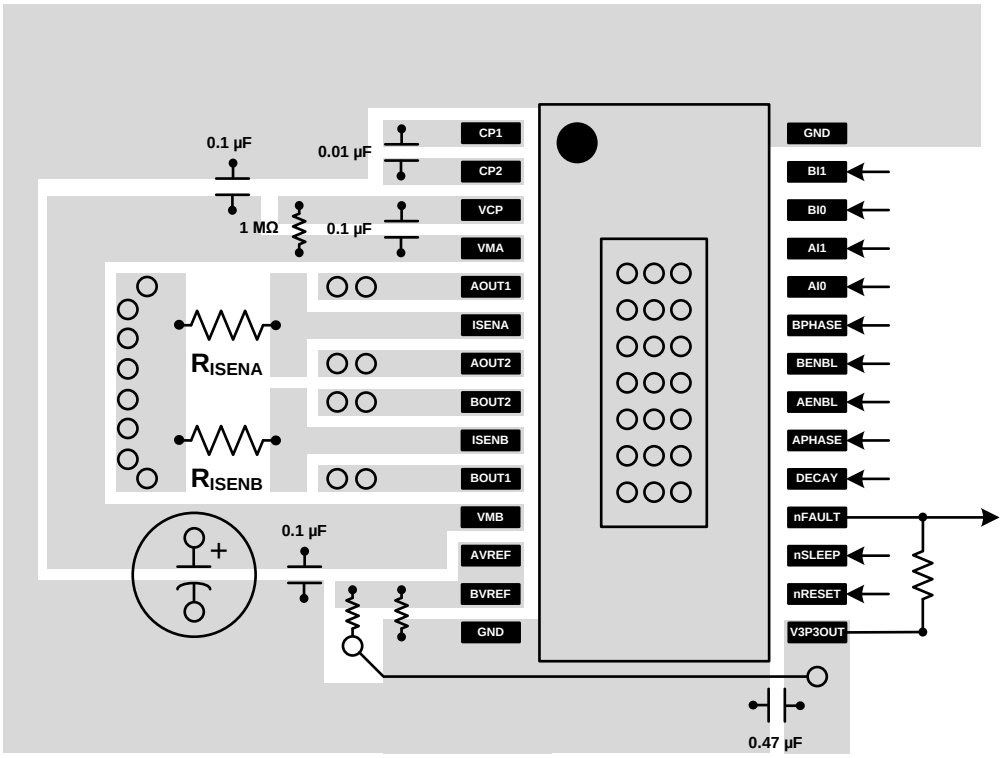


Figure 11. DRV8812 Layout Example

10.3 Thermal Consideration

10.3.1 Thermal Protection

The DRV8812 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.2 Power Dissipation

Power dissipation in the DRV8812 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 3.

$$P_{TOT} = 4 \times R_{DS(ON)} \times \left(I_{OUT(RMS)}\right)^2 \quad (3)$$

where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.3.3 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, "PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, "PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

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11 Device and Documentation Support

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8812PWP	Obsolete	Production	HTSSOP (PWP) | 28	-	-	Call TI	Call TI	-40 to 85	DRV8812
DRV8812PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8812
DRV8812PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8812
DRV8812PWPR.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8812
DRV8812RHDR	Active	Production	VQFN (RHD) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8812
DRV8812RHDR.A	Active	Production	VQFN (RHD) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8812
DRV8812RHDR.B	Active	Production	VQFN (RHD) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8812

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

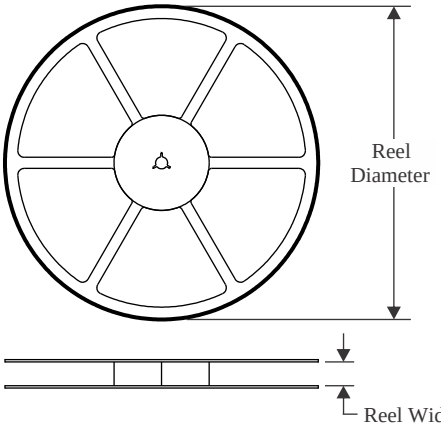
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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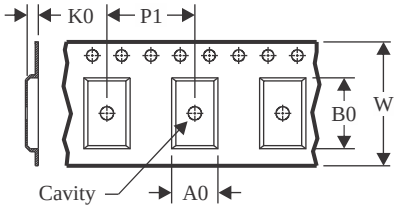
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

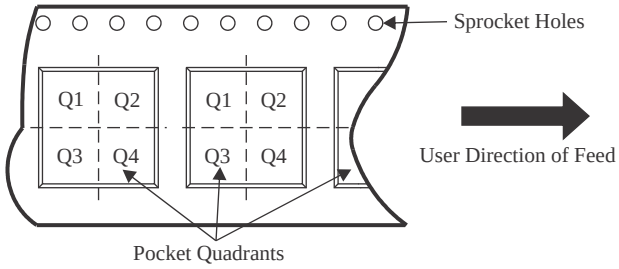


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

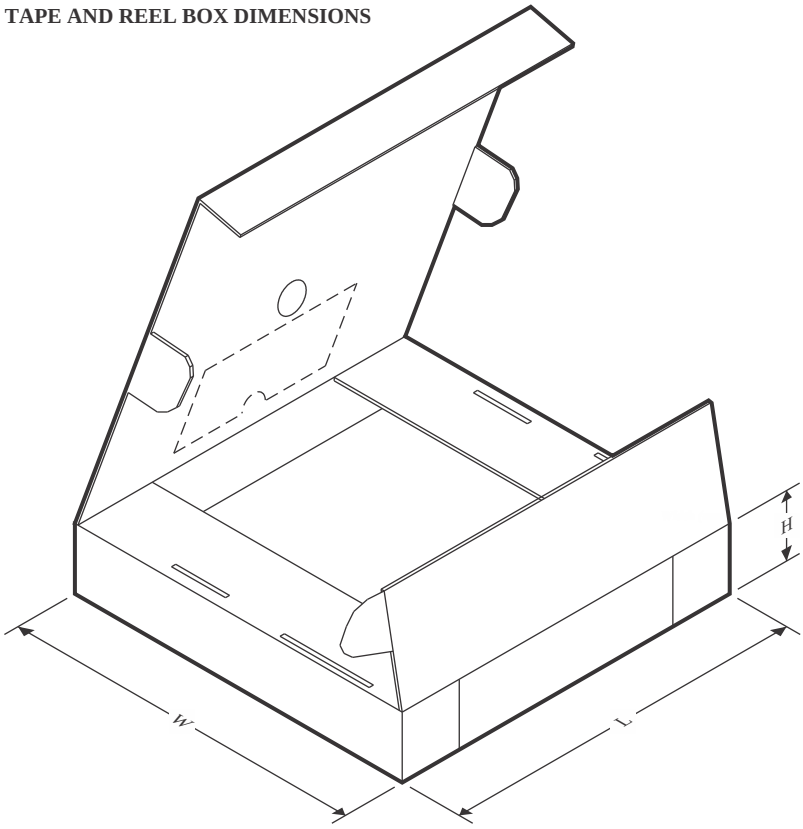
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8812PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
DRV8812PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8812RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8812RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8812PWPR	HTSSOP	PWP	28	2000	353.0	353.0	32.0
DRV8812PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
DRV8812RHDR	VQFN	RHD	28	3000	346.0	346.0	33.0
DRV8812RHDR	VQFN	RHD	28	3000	360.0	360.0	36.0

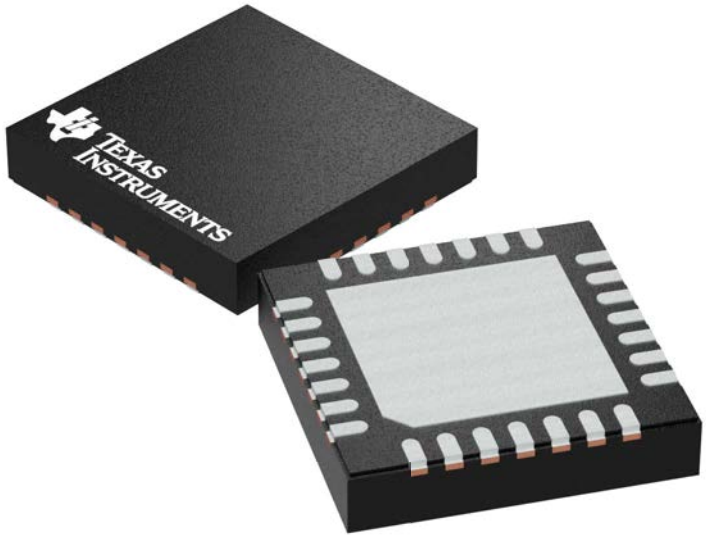
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

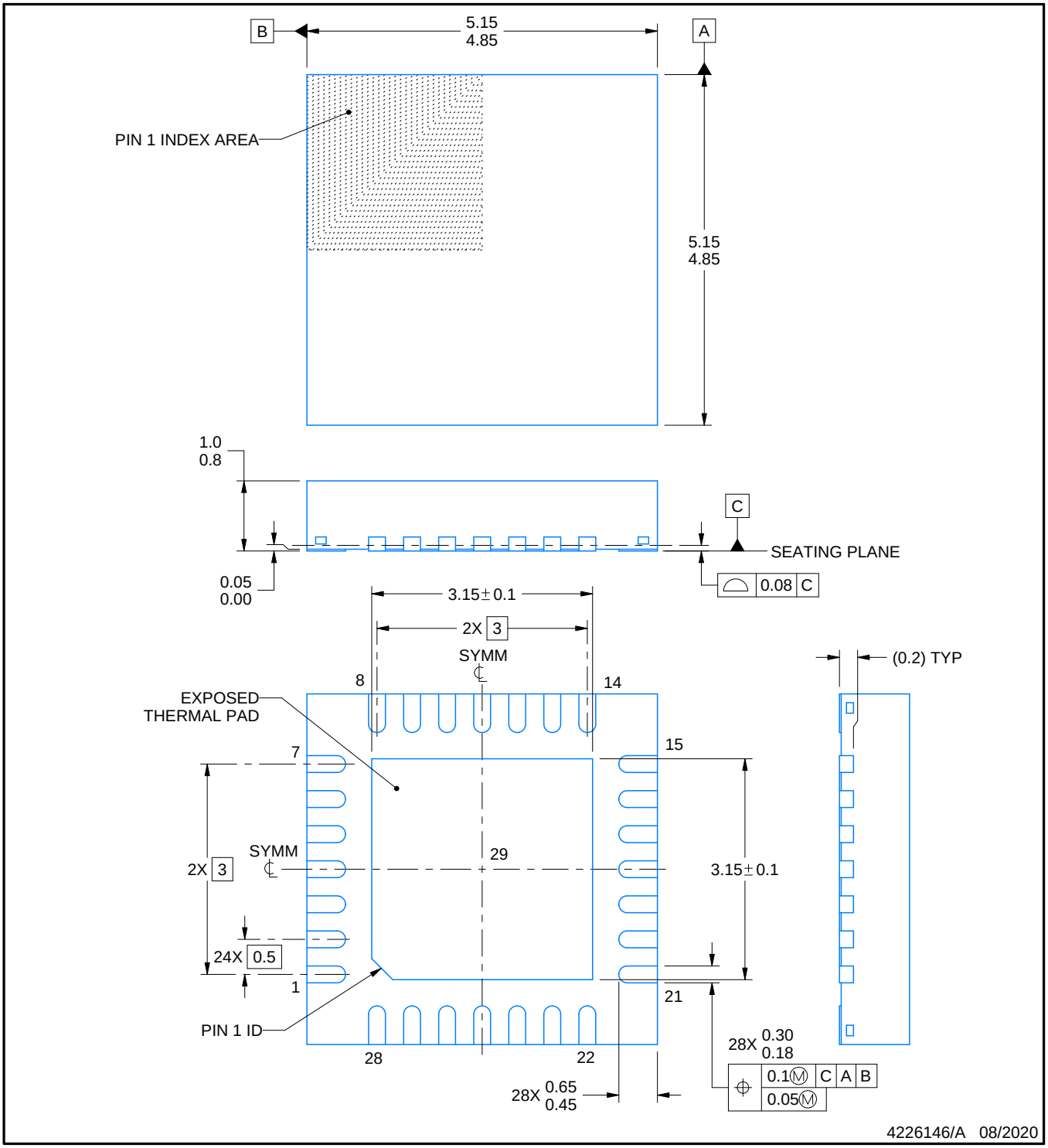
4204400/G

RHD0028B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

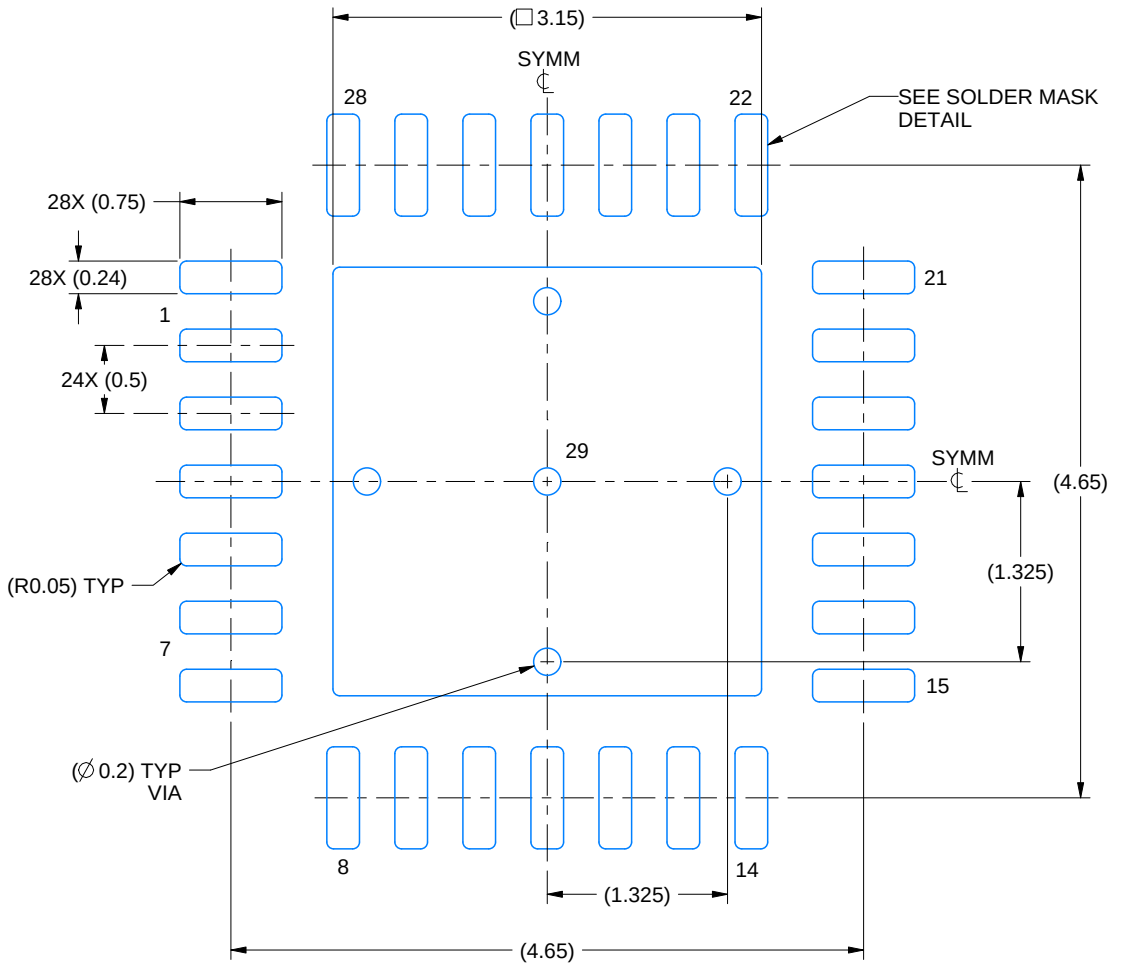
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

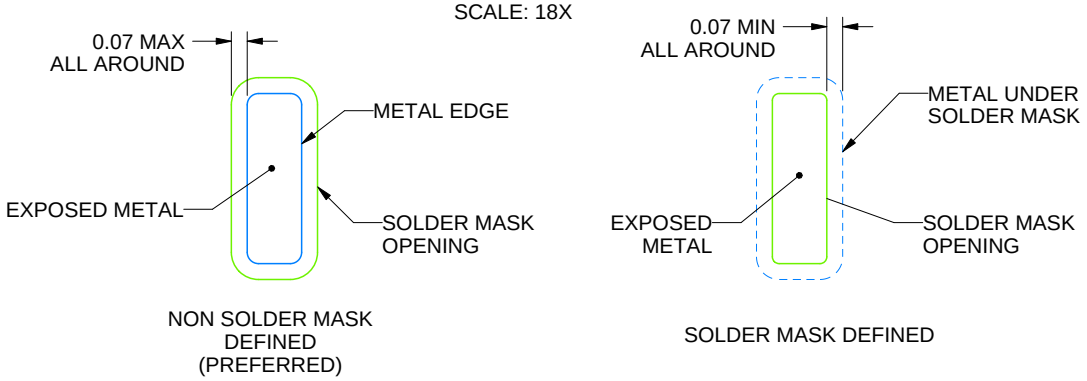
RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

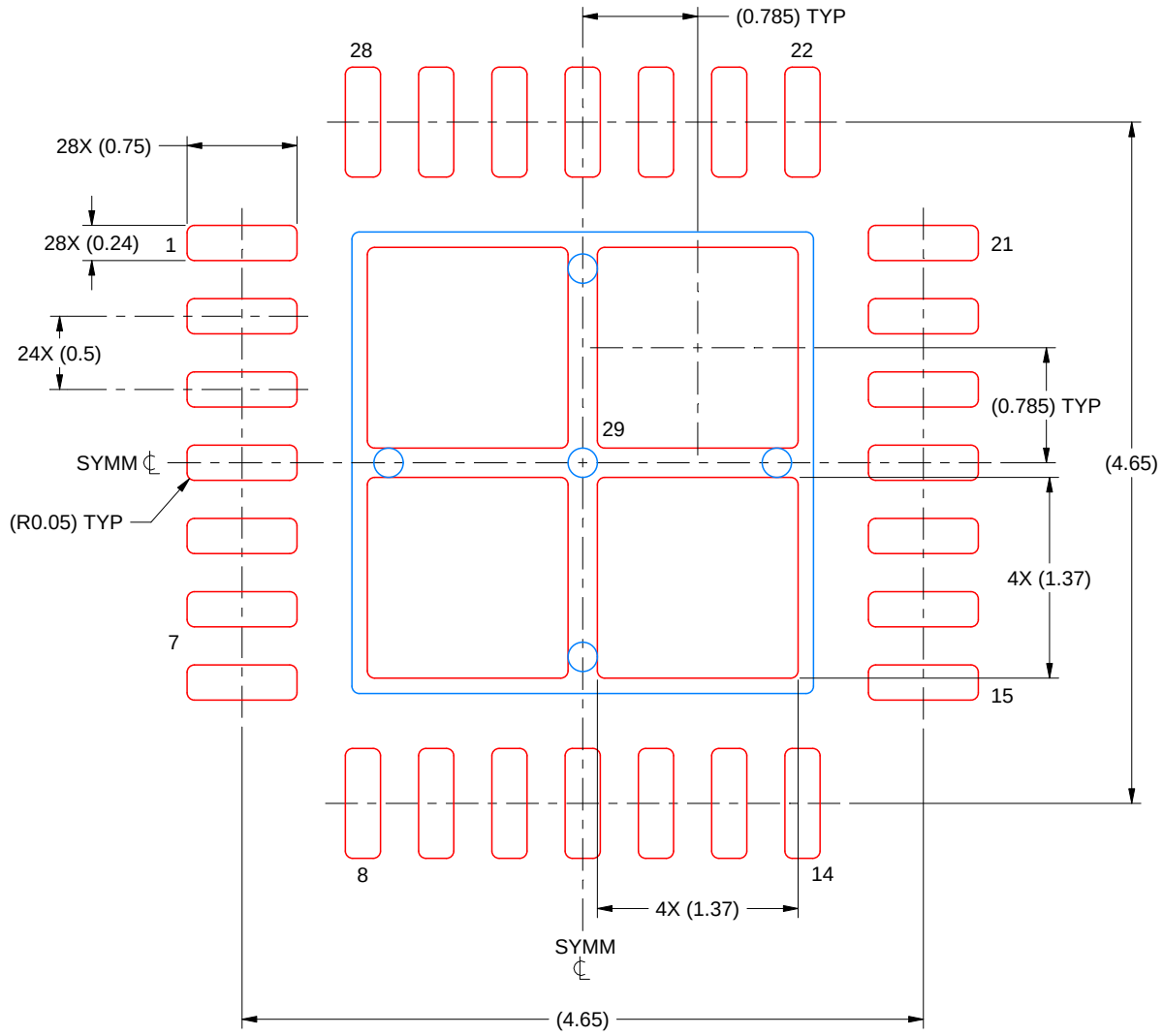


SOLDER MASK DETAILS

4226146/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4226146/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

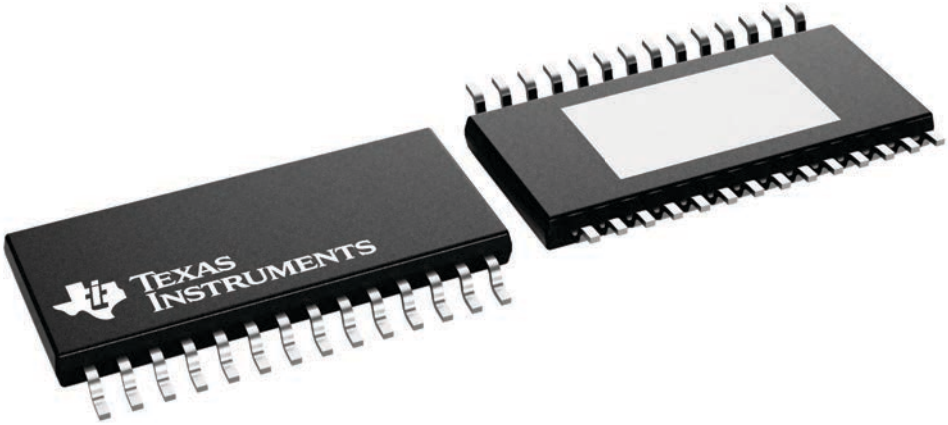
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

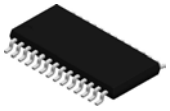
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

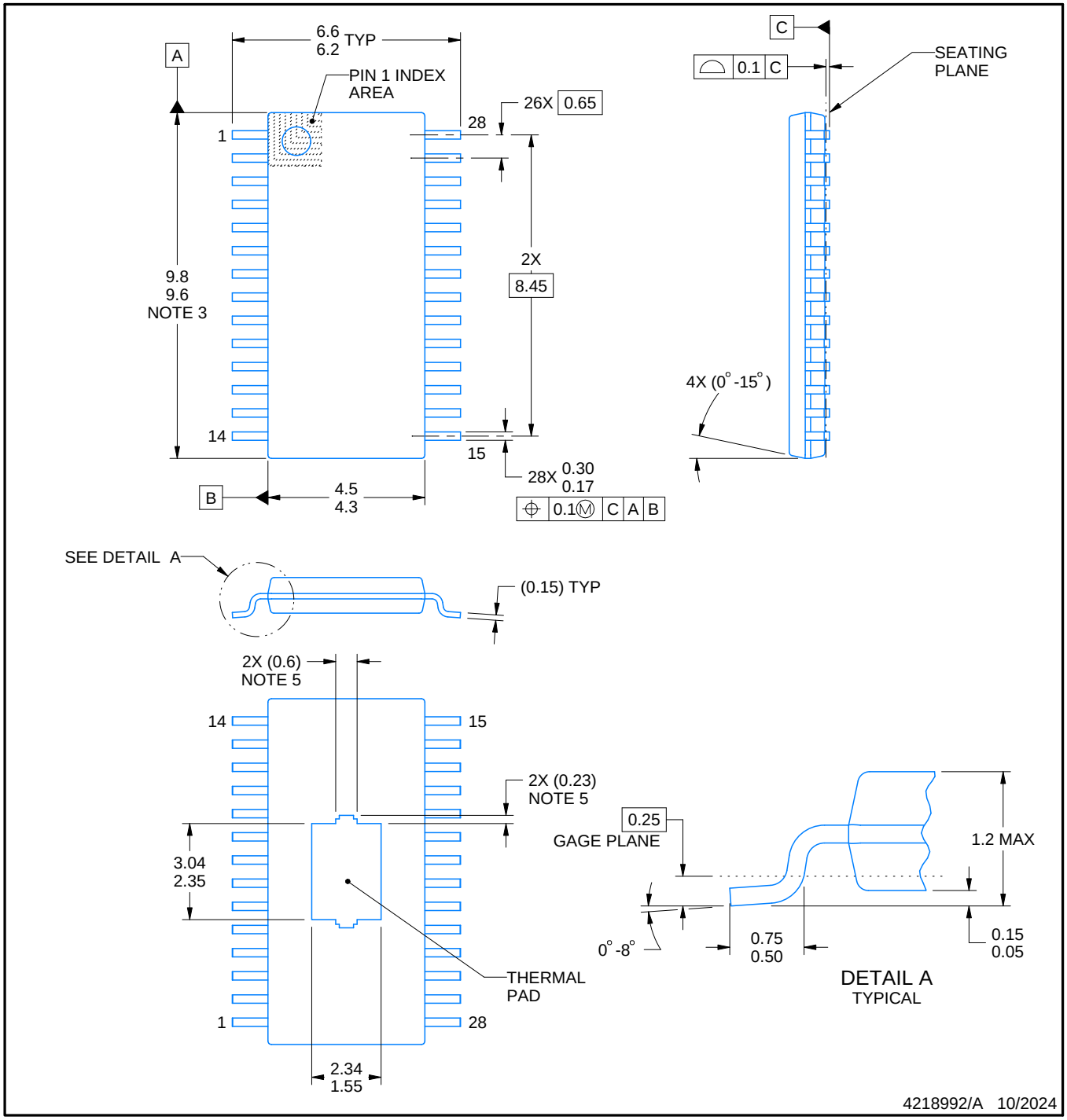
PACKAGE OUTLINE

PWP0028H



PowerPAD™ TSSOP - 1.2 mm max height

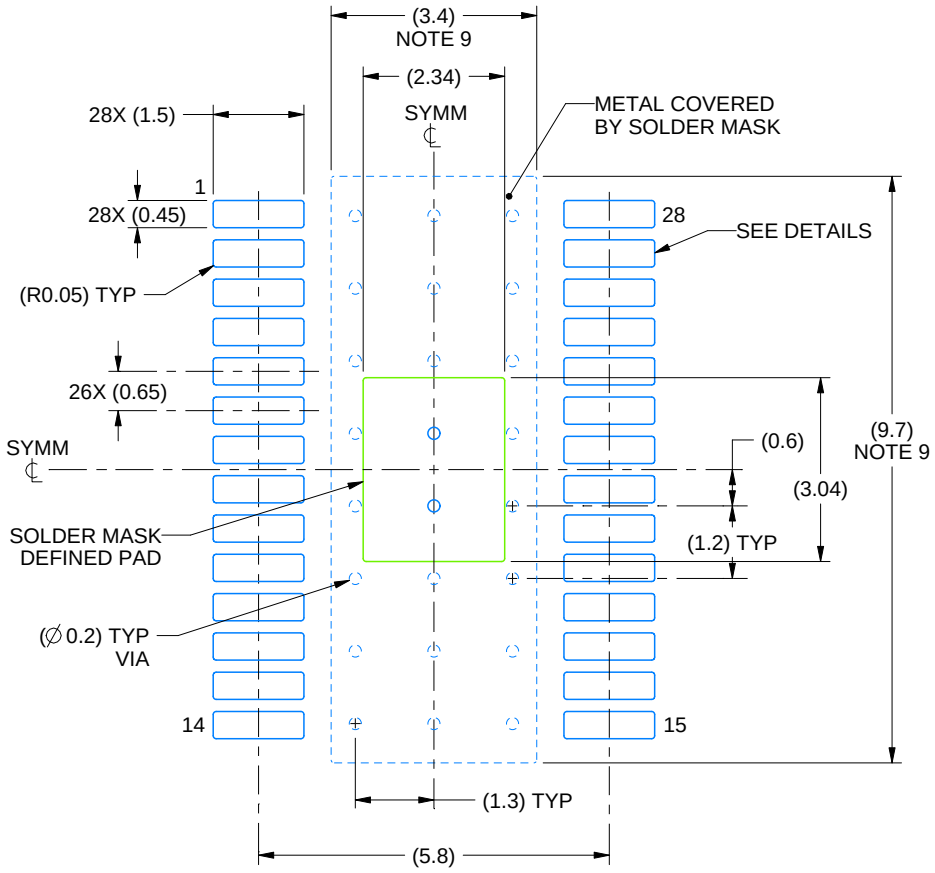
SMALL OUTLINE PACKAGE



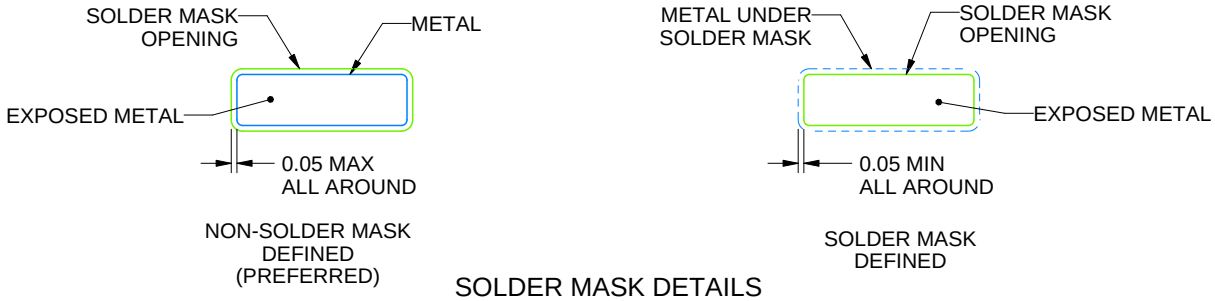
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

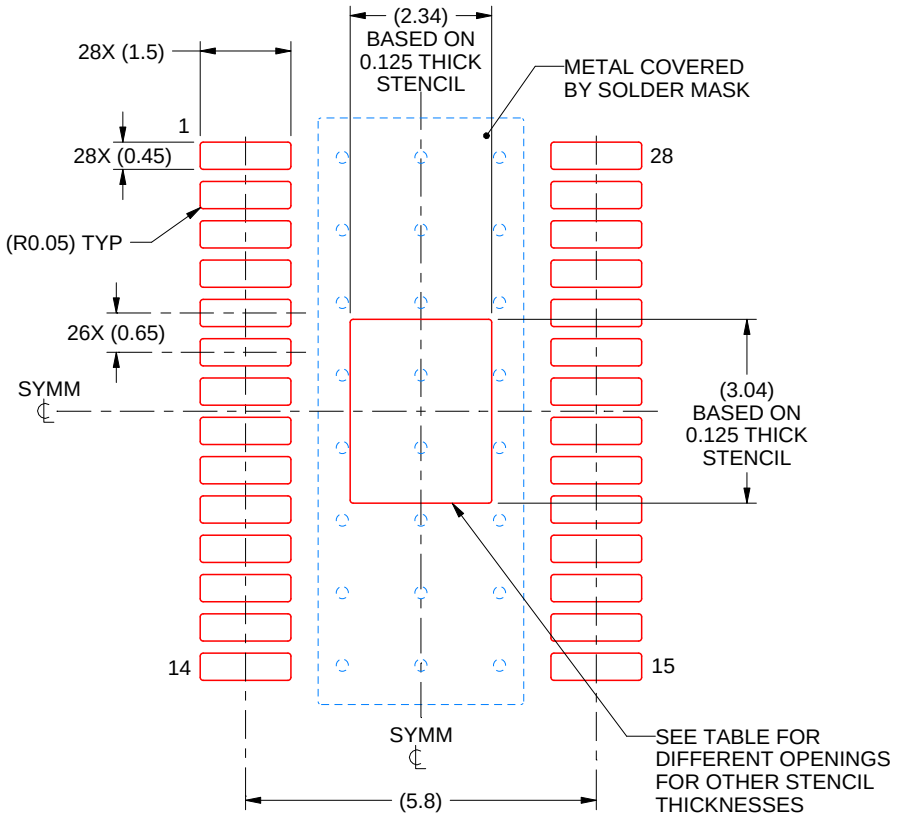


SOLDER MASK DETAILS

4218992/A 10/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 3.40
0.125	2.34 X 3.04 (SHOWN)
0.15	2.14 X 2.78
0.175	1.98 X 2.57

4218992/A 10/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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