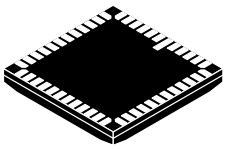
1/3-Inch CMOS Digital Image Sensor

MT9M034



ILCC48 10x10
CASE 847AD

Table 1. KEY PARAMETERS

Parameter		Value
Optical Format		1/3−inch (6 mm)
Active Pixels		1280 × 960 = 1.2 Mp
Pixel Size		3.75 μm
Color Filter Array		RGB Bayer or Monochrome
Shutter Type		Electronic Rolling Shutter
Input Clock Range		6−50 MHz
Output Clock Maximum		74.25 MHz
Output	Parallel	12−bit
Frame Rate	Full Resolution	45 fps
	720p	60 fps
Responsivity		5.48 V/lux−sec
SNR_{MAX}		43.9 dB
Maximum Dynamic Range		>115 dB
Supply Voltage	I/O	1.8 V* or 2.8 V
	Digital	1.8 V
	Analog	2.8 V
Power Consumption		270 mW (1280 × 720 60 fps Parallel Output Linear Mode) 460 mW (1280 × 720 60 fps Parallel Output HDR Mode)
Operating Temperature (ambient) $-T_A$		−30°C to + 70°C (Surveillance)
Package Options		10×10 mm 48−pin iLCC
		Bare Die

*1.8 V VDD_IO is recommended due to better row noise performance

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Features

- Superior Low−light performance
- HD Video (720p60)
- Linear or High Dynamic Range Capture
- Video/Single Frame Modes
- On−chip AE and Statistics Engine
- Parallel and Serial Output
- Auto Black Level Calibration
- Context Switching
- Temperature Sensor

Applications

- Video Surveillance
- 720p60 Video Applications
- High Dynamic Range Imaging

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Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
MT9M034I12STC−DPBR1	1.2 MP 1/3” CIS	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M034I12STC−DRBR1	1.2 MP 1/3” CIS	Dry Pack without Protective Film, Double Side BBAR Glass
MT9M034I12STM−DPBR1	1.2 MP 1/3” CIS	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M034I12STM−DRBR	1.2 MP 1/3” CIS	Dry Pack without Protective Film, Double Side BBAR Glass

GENERAL DESCRIPTION

The **onsemi** MT9M034 is a 1/3−inch CMOS digital image sensor with an active−pixel array of 1280 (H) × 960 (V). It captures images in either linear or high dynamic range modes, with a rolling−shutter readout. It includes sophisticated camera functions such as auto exposure control, windowing, and both video and single frame modes. It is designed for both low light and high dynamic range scene performance. It is programmable through a simple two−wire serial interface. The MT9M034 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including surveillance and HD video.

The **onsemi** MT9M034 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 960p−resolution image at 45 frames per second (fps). In linear mode, it outputs 12−bit raw data. In high dynamic range mode, it outputs 12−bit compressed data using parallel output. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

The MT9M034 includes additional features to allow application−specific tuning; windowing and offset, adjustable auto−exposure control, auto black level correction, and on−board temperature sensor. Optional register information and histogram statistic information can be embedded in first and last two lines of the image frame.

The sensor is designed to operate in a wide temperature range (−30°C to +70°C).

FUNCTIONAL OVERVIEW

The MT9M034 is a progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase−locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 50 MHz The maximum output pixel rate is 74.25 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor.

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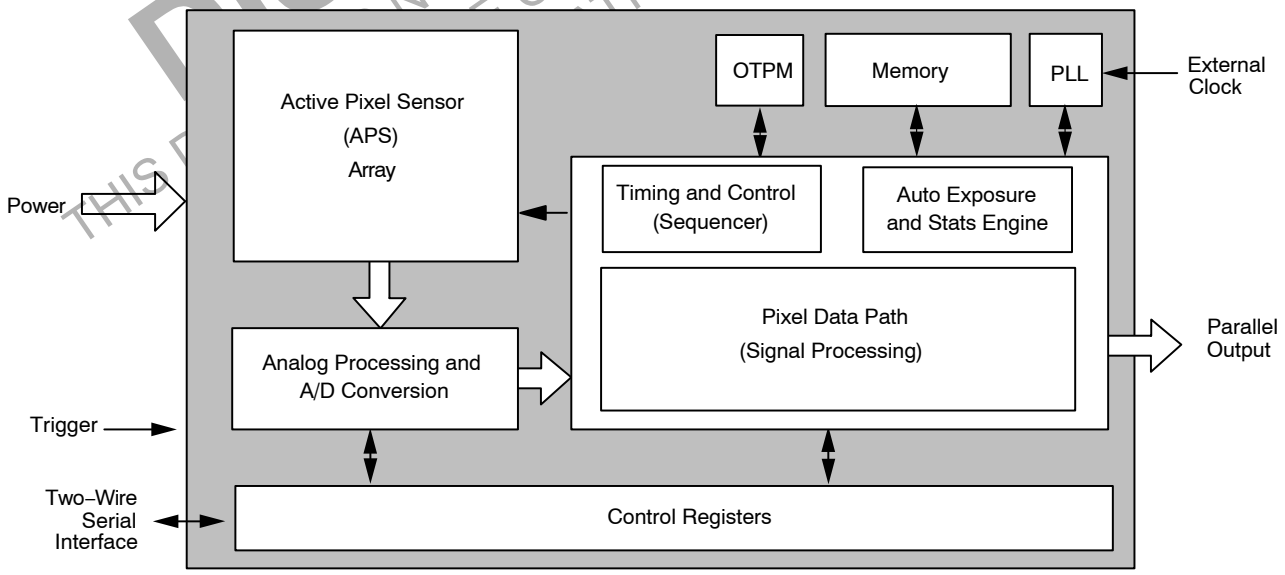
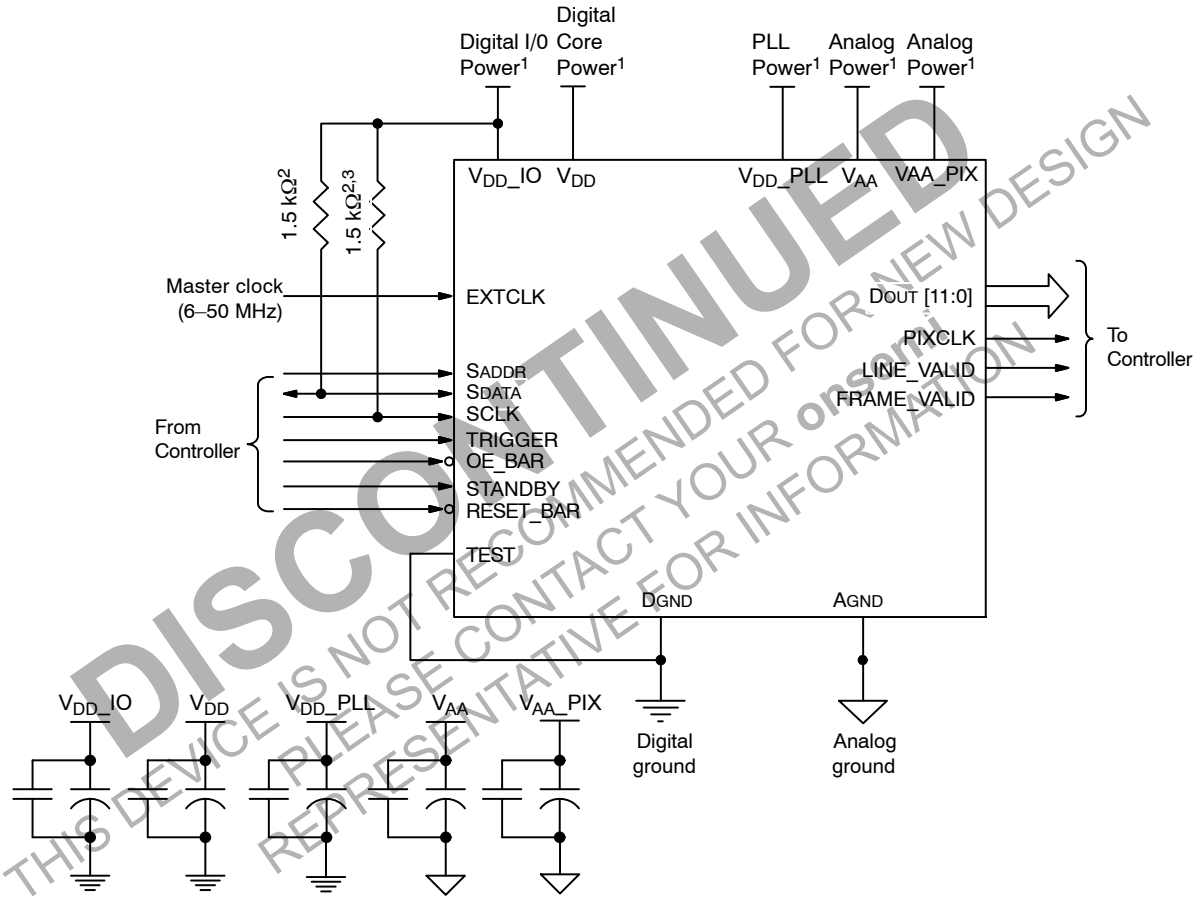


Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.2 Mp Active− Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog−to−digital converter (ADC). The output from the ADC is a 12−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where multiple images are combined on−chip to produce a single image at 20−bit per pixel value. A compressing mode is further offered to allow this 20−bit pixel value to be transmitted to the host system as a 12−bit value with close to zero loss in image quality. The pixel data are output at a rate of up to 74.25 Mp/s, in parallel to frame and line synchronization signals.



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1. All power supplies should be adequately decoupled.
2. **onsemi** recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. The serial interface output pads and VDDSLVS can be left unconnected if the parallel output interface is used.
4. **onsemi** recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Check the demo headboard schematics for circuit recommendations.
5. **onsemi** recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.
7. The serial interface output pads and VDDSLVS can be left unconnected if the parallel output interface is used.

Figure 2. Typical Configuration: Parallel Pixel Data Interface

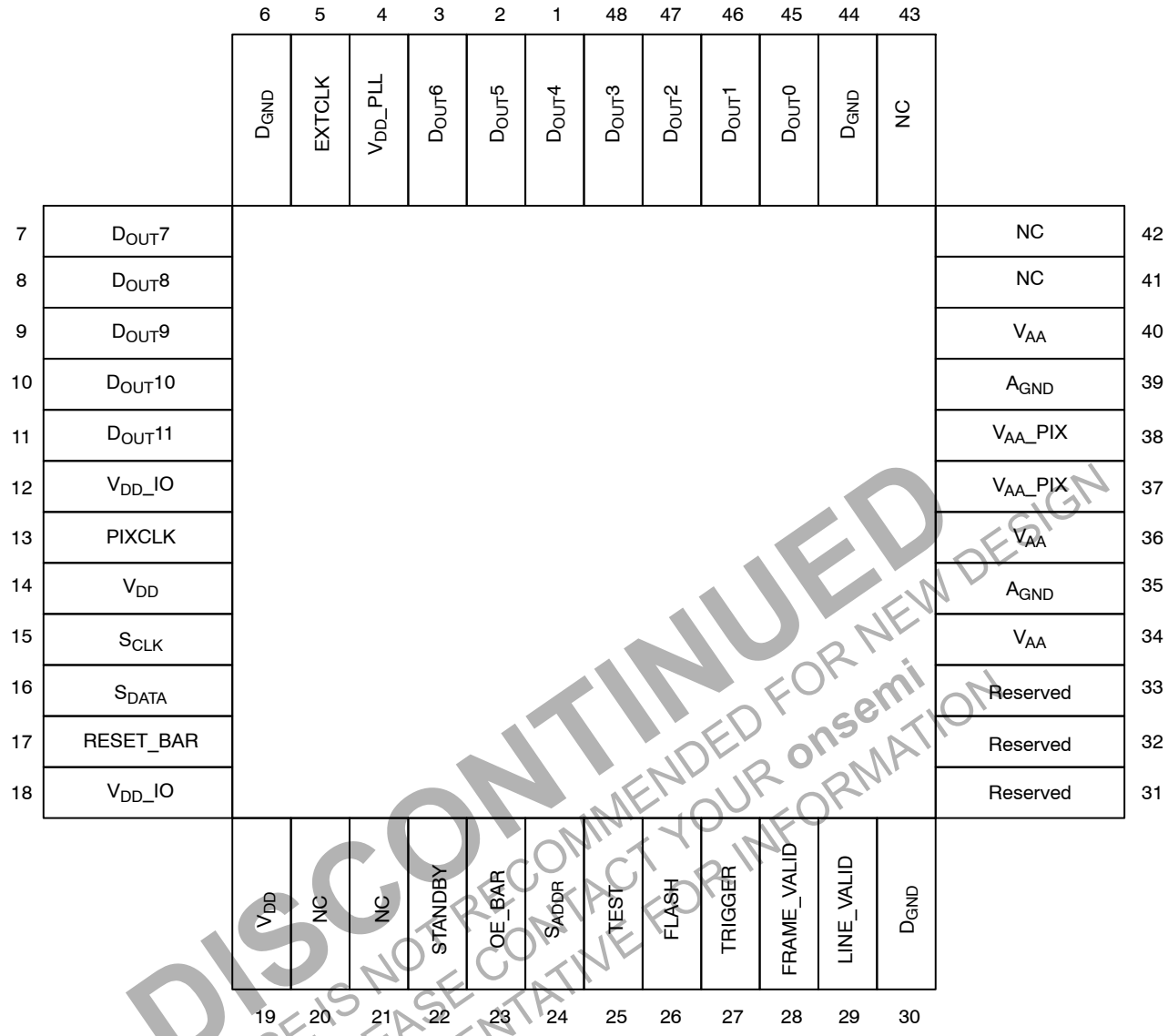


Figure 3. 48 iLCC Package, Parallel Output

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Table 3. PIN DESCRIPTION

Pin Number	Name	Type	Description
1	DOUT4	Output	Parallel pixel data output
2	DOUT5	Output	Parallel pixel data output
3	DOUT6	Output	Parallel pixel data output
4	VDD_PLL	Power	PLL power
5	EXTCLK	Input	External input clock
6	DGND	Power	Digital ground
7	DOUT7	Output	Parallel pixel data output
8	DOUT8	Output	Parallel pixel data output
9	DOUT9	Output	Parallel pixel data output
10	DOUT10	Output	Parallel pixel data output
11	DOUT11	Output	Parallel pixel data output (MSB)
12	VDD_IO	Power	I/O supply power
13	PIXCLK	Output	Pixel clock out. DOUT is valid on rising edge of this clock
14	VDD	Power	Digital power
15	SCLK	Input	Two−Wire Serial clock input
16	SDATA	I/O	Two−Wire Serial data I/O
17	RESET_BAR	Input	Asynchronous reset (active LOW). All settings are restored to factory default
18	VDD_IO	Power	I/O supply power
19	VDD	Power	Digital power
20	NC		
21	NC		
22	STANDBY	Input	Standby−mode enable pin (active HIGH)
23	OE_BAR	Input	Output enable (active LOW)
24	SADDR	Input	Two−Wire Serial address select
25	TEST	Input	Manufacturing test enable pin (connect to DGND)
26	FLASH	Output	Flash output control
27	TRIGGER	Input	Exposure synchronization input
28	FRAME_VALID	Output	Asserted when DOUT frame data is valid
29	LINE_VALID	Output	Asserted when DOUT line data is valid
30	DGND	Power	Digital ground
31	Reserved		NC
32	Reserved		NC
33	Reserved		NC
34	VAA	Power	Analog power
35	AGND	Power	Analog ground
36	VAA	Power	Analog power
37	VAA_PIX	Power	Pixel power
38	VAA_PIX	Power	Pixel power
39	AGND	Power	Analog ground
40	VAA	Power	Analog power
41	NC		

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Table 3. PIN DESCRIPTION (continued)

Pin Number	Name	Type	Description
42	NC		
43	NC		
44	DGND	Power	Digital ground
45	DOUT0	Output	Parallel pixel data output (LSB)
46	DOUT1	Output	Parallel pixel data output
47	DOUT2	Output	Parallel pixel data output
48	DOUT3	Output	Parallel pixel data output

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PIXEL DATA FORMAT

Pixel Array Structure

The MT9M034 pixel array is configured as 1412 columns by 1028 rows, (see Figure 4). The dark pixels are optically black and are used internally to monitor black level. Of the right 100 columns, 64 are dark pixels used for row noise correction. Of the top 24 rows of pixels, 12 of the dark rows are used for black level correction. There are 1296 columns by 976 rows of optically active pixels. While the sensor's format is 1280 × 960, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

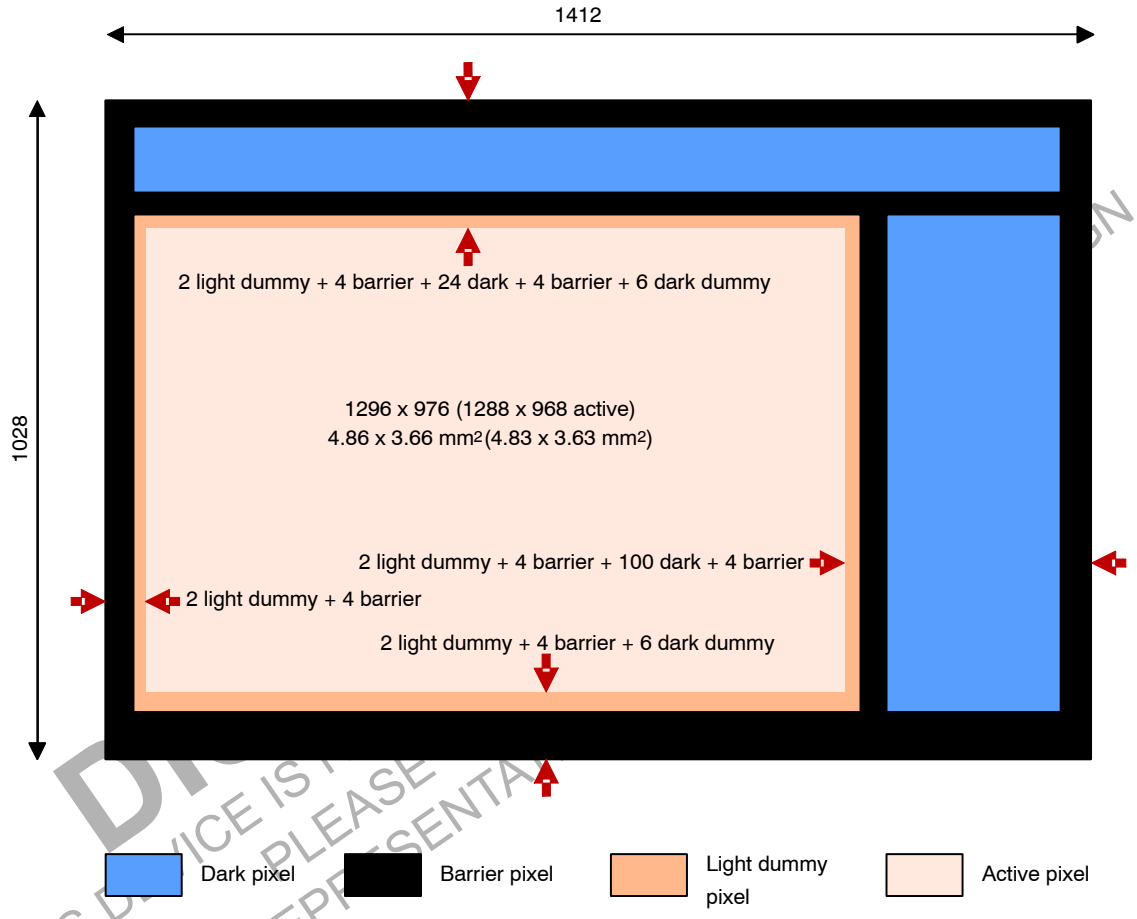


Figure 4. Pixel Array Description

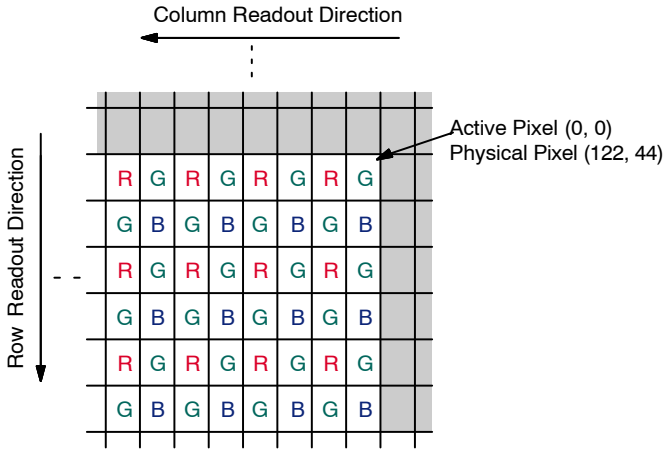


Figure 5. Pixel Color Pattern Detail (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 5). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (112, 44).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 6. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 6.

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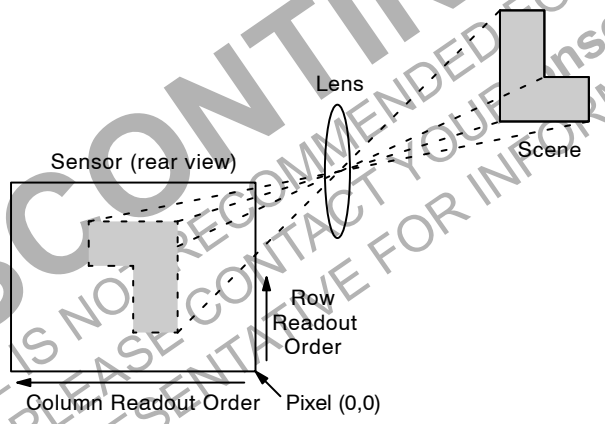


Figure 6. Imaging a Scene

Digital Gain Control

MT9M034 supports four digital gains for the color channels: Red, Green1 (green pixels on the red rows), Green2 (green pixels on the blue rows), and Blue. Digital gain control of the MT9M034 is dependent on the configuration of the x_addr_start register. Table 4 illustrates how the digital gains are applied when x_addr_start is even or odd number.

Table 4. DIGITAL GAIN CONTROL FOR ODD AND EVEN X_ADDR_START (R0X3004)

Pixels	x_addr_start	Gain	Register
Red	Even	red_gain	R0x305A
	Odd	green1_gain	R0x3056
Green1 (on Red rows)	Even	green1_gain	R0x3056
	Odd	red_gain	R0x305A
Green2 (on Blue rows)	Even	green2_gain	R0x305C
	Odd	blue_gain	R0x3058

Table 4. DIGITAL GAIN CONTROL FOR ODD AND EVEN X_ADDR_START (R0X3004)

Pixels	x_addr_start	Gain	Register
Blue	Even	blue_gain	R0x3058
	Odd	green2_gain	R0x305C

OUTPUT DATA FORMAT

The MT9M034 image data is read out in a progressive scan. Valid image data is surrounded by horizontal and vertical blanking (see Figure 7). The amount of horizontal row time (in clocks) is programmable through R0x300C. The amount of vertical frame time (in rows) is programmable through R0x300A. Line_Valid (LV) is HIGH during the shaded region of Figure 7. Optional Embedded Register setup information and Histogram statistic information are available in first two and last row of image data.

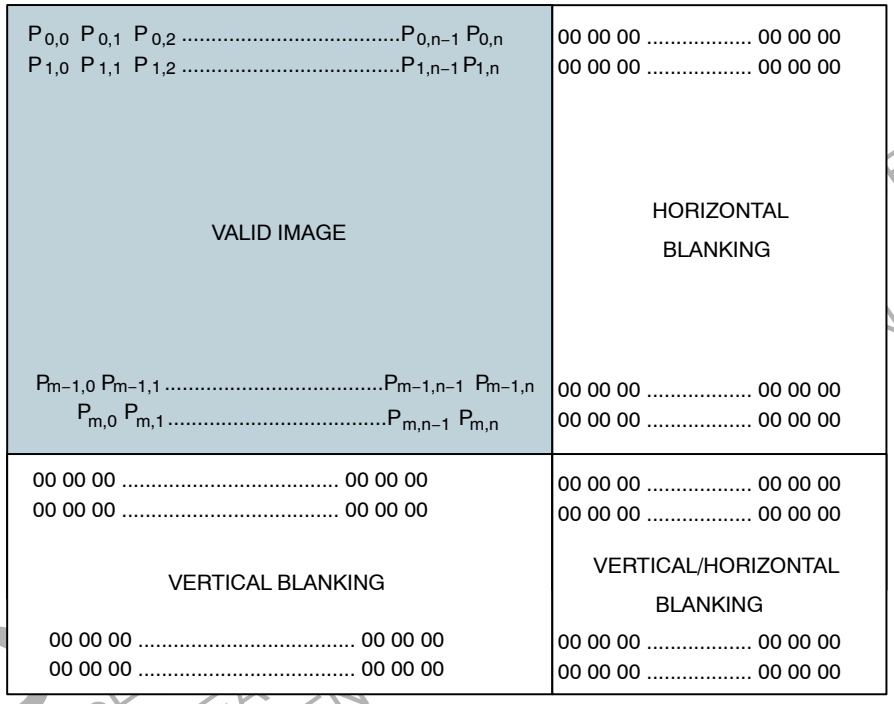


Figure 7. Spatial Illustration of Image Readout

Readout Sequence

Typically, the readout window is set to a region including only active pixels. The user has the option of reading out dark regions of the array, but if this is done, consideration must be given to how the sensor reads the dark regions for its own purposes.

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Parallel Output Data Timing

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 968 rows of 1284 columns each. The FV and LV signals indicate the boundaries between frames and lines, respectively. PIXCLK can be used as a clock to latch the data. For each PIXCLK cycle, with respect to the falling edge, one 12−bit pixel datum outputs on the DOUT pins. When both FV and LV are asserted, the pixel is valid. PIXCLK cycles that occur when FV is de−asserted are called vertical blanking. PIXCLK cycles that occur when only LV is de−asserted are called horizontal blanking.

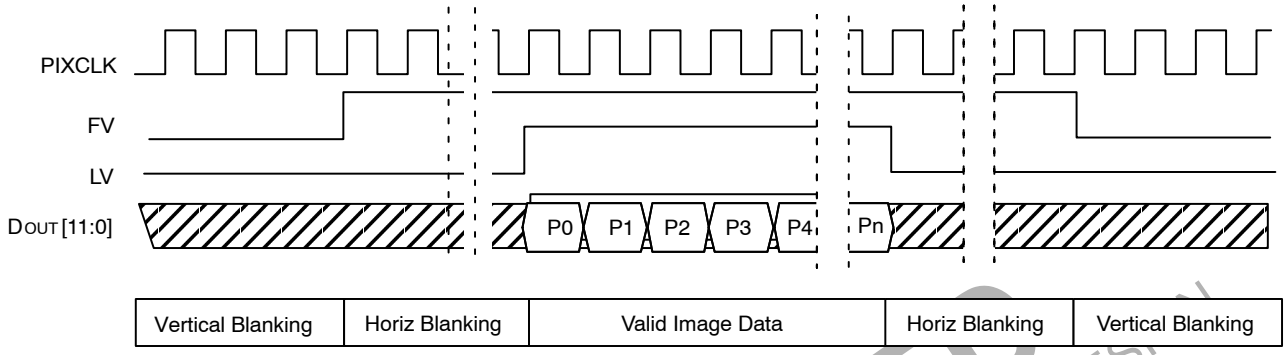


Figure 8. Default Pixel Output Timing

LV and FV

The timing of the FV and LV outputs is closely related to the row time and the frame time.

FV will be asserted for an integral number of row times, which will normally be equal to the height of the output image.

LV will be asserted during the valid pixels of each row. The leading edge of LV will be offset from the leading edge of FV by 6 PIXCLKs. Normally, LV will only be asserted if FV is asserted; this is configurable as described below.

LV Format Options

The default situation is for LV to be de−asserted when FV is de−asserted. By configuring R0x306E[1:0], the LV signal can take two different output formats. The formats for reading out four lines and two vertical blanking lines are shown in Figure 9.

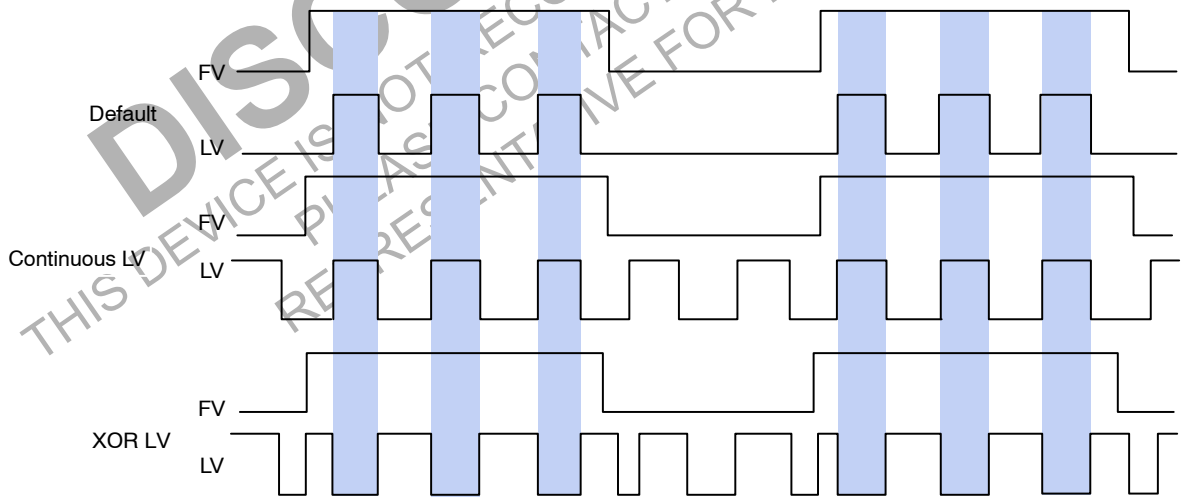


Figure 9. LV Format Options

The timing of an entire frame is shown in Figure 10.

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Frame Time

The pixel clock (PIXCLK) represents the time needed to sample 1 pixel from the array. The sensor outputs data at the maximum rate of 1 pixel per PIXCLK. One row time (^{t}ROW) is the period from the first pixel output in a row to the first pixel output in the next row. The row time and frame time are defined by equations in Table 5.

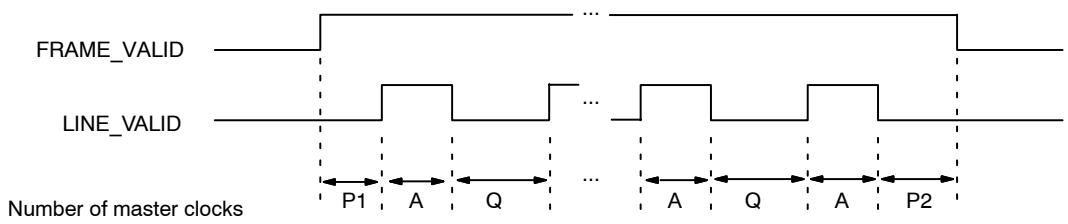


Figure 10. Line Timing and FRAME_VALID/LINE_VALID Signals

Table 5. FRAME TIME (EXAMPLE BASED ON 1280 X 960, 45 FRAMES PER SECOND)

Parameters	Name	Equation	Default Timing at 74.25 MHz
A	Active Data Time	Context A: R0x3008 − R0x3004 + 1 Context B: R0x308E − R0x308A + 1	1280 pixel clocks = 17.23 μs
P1	Frame Start Blanking	6 (fixed)	6 pixel clocks = 0.08 μs
P2	Frame End Blanking	6 (fixed)	6 pixel clocks = 0.08 μs
Q	Horizontal Blanking	R0x300C − A	370 pixel clocks = 4.98 μs
A + Q (tROW)	Line (Row) Time	R0x300C	1650 pixel clocks = 22.22 μs
V	Vertical Blanking	Context A: (R0x300A−(R0x3006−R0x3002+1)) x (A + Q) Context B: ((R0x30AA−(R0x3090−R0x308C+1)) x (A + Q)	49,500 pixel clocks = 666.66 μs
Nrows × (A + Q)	Frame Valid Time	Context A: ((R0x3006−R0x3002+1) × (A+Q))−Q+P1+P2 Context B: ((R0x3090−R0x308C+1) × (A+Q))−Q+P1+P2	1,584,000 pixel clocks = 21.33 ms
F	Total Frame Time	V + (Nrows × (A + Q))	1,633,500 pixel clocks = 22.22 ms

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Sensor timing is shown in terms of pixel clock cycles (see Figure 7). The recommended pixel clock frequency is 74.25 MHz. The vertical blanking and the total frame time equations assume that the integration time (coarse integration time plus fine integration time) is less than the number of active lines plus the blanking lines:

Window Height + Vertical Blanking (eq. 1)

If this is not the case, the number of integration lines must be used instead to determine the frame time, (see Table 6). In this example, it is assumed that the coarse integration time control is programmed with 2000 rows and the fine shutter width total is zero.

For Master mode, if the integration time registers exceed the total readout time, then the vertical blanking time is internally extended automatically to adjust for the additional integration time required. This extended value is not written back to the frame_length_lines register. The frame_length_lines register can be used to adjust frame−to−frame readout time. This register does not affect the exposure time but it may extend the readout time.

Table 6. FRAME TIME: LONG INTEGRATION TIME

Parameters	Name	Equation (Number of Pixel Clock Cycles)	Default Timing at 74.25 MHz
F'	Total Frame Time (Long Integration Time)	Context A: (R0x3012 x (A + Q)) + R0x3014 + P1 + P2 Context B: (R0x3016 x (A + Q)) + V R0x3018 + P1 + P2	3,300,012 pixel clocks = 44.44 ms

1. The MT9M034 uses column parallel analog−digital converters; thus short line timing is not possible. The minimum total line time is 1650 columns (horizontal width + horizontal blanking) for HDR mode and 1400 for linear mode. The minimum horizontal blanking is 370.

Exposure

Total integration time is the result of Coarse_Integration_Time and Fine_Integration_Time registers, and depends also on whether manual or automatic exposure is selected.

The actual total integration time, t_{INT} is defined as:

$$t_{INT} = t_{INTCoarse} - 410 - t_{INTFine} \quad \text{(eq. 2)}$$

= (number of lines of integration x line time) − (410 pixel clocks of conversion time overhead) − (number of pixels of integration x pixel time)

where:

- Number of Lines of Integration (Auto Exposure Control: Enabled)
  When automatic exposure control (AEC) is enabled, the number of lines of integration may vary from frame to frame, with the limits controlled by R0x311E (minimum auto exposure time) and R0x311C (maximum auto exposure time)
- Number of Lines of Integration (Auto Exposure Control: Disabled)
  If AEC is disabled, the number of lines of integration equals the value in R0x3012 (context A) or R0x3016 (context B)
- Number of Pixels of Integration
  The number of fine shutter width pixels is independent of AEC mode (enabled or disabled):
  - Context A: the number of pixels of integration equals the value in R0x3014
  - Context B: the number of pixels of integration equals the value in R0x3018. Maximum value for $t_{INTFINE}$ is line length pixel clocks − 611

Typically, the value of the Coarse_Integration_Time register is limited to the number of lines per frame (which includes vertical blanking lines), such that the frame rate is not affected by the integration time. For more information on coarse and fine integration time settings limits, please refer to the Register Reference document.

NOTE: In HDR mode, there are specific limitations on coarse_integration_time due to the number of line buffers available. Please refer to the section called "HDR Specific Exposure Settings".

For best image quality, it is recommended that the integration time be set to two rows or greater for the shortest exposure, particularly for monochrome sensors. For linear mode, this would be the coarse integration time (R0x3012). For HDR mode, the integration time should be set such that the T3 exposure is two rows or greater. Setting the exposure time to 1 row may result in non−uniformity between rows.

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HIGH DYNAMIC RANGE MODE

By default, the sensor powers up in Linear Mode, however, the MT9M034 can be configured to run in HDR mode. The HDR scheme used is multi−exposure HDR. This allows the sensor to handle 120 dB of dynamic range. The sensor also features a linear mode. In HDR mode, the sensor sequentially captures three exposures by maintaining 3 separate read and reset pointers that are interleaved within the rolling shutter readout. The intermediate pixel values are stored in line buffers while waiting for the 3 exposures values to be present. As soon as a pixel's 3 exposure values are available, they are combined to create a linearized 20−bit value for each pixel's response. This 20−bit value is then optionally compressed back to a 12− or 14−bit value for output. For 14−bit mode, the compressing is lossless. In 12−bit mode, there is minimal data loss. Figure 11 shows the HDR data compression:

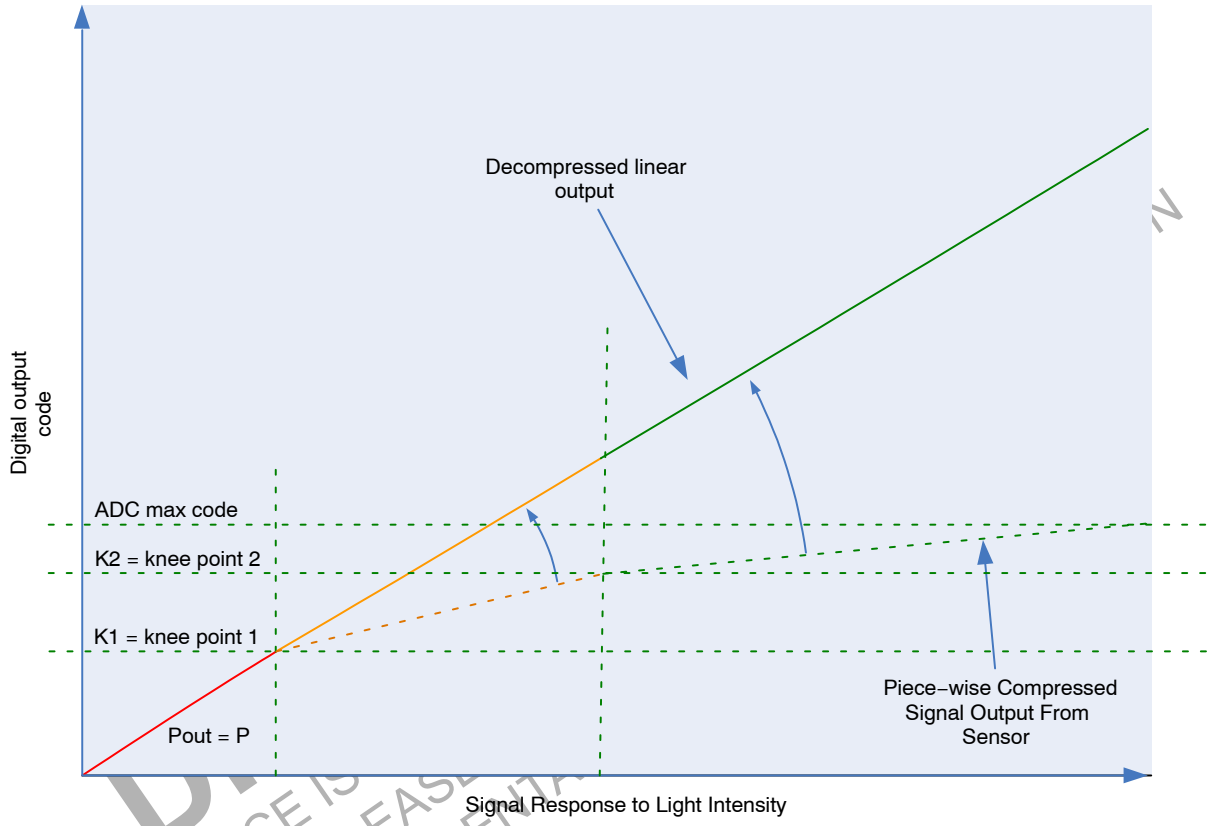


Figure 11. HDR Data Compression

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The HDR mode is selected when Operation_Mode_Ctrl, R0x3082[1:0] = 0. Further controls on exposure time limits and compressing are controlled by R0x3082[5:2], and R0x31D0. More details can be found in the MT9M034 Register Reference.

In HDR mode, when compression is used, there are two types of knee−points: (i) T1/T2 and T2/T3 capture knee−points and (ii) P_{OUT} and Pout2 compression knee−points (Figure 11). Aligning the capture knee−points on top of the compression knee−points, can avoid code losses (SNR loss) in the compression. Tables 7 and 8 below show the knee points for the different modes. Alternatively, the sensor automatically reports the knee points and can be read directly from registers R0x319A and R0x319C.

Table 7. KNEE POINTS FOR COMPRESSION TO 14 BITS

T1/T2 Exposure Ratio (R1) R0x3082[3:2]	P1	P_{OUT1} = P1	P2	P_{OUT2} = (P2 − P1) / R1 + P_{OUT1}	T2/T3 Exposure Ratio (R2) R0x3082[5:4]	P_{MAX}	$P_{OUT_{MAX}}$ = (P_{MAX} − P2) / (R1 × R2) + P_{OUT2}
4x	2^{12}	4096	2^{14}	7168	4x	2^{16}	10240
					8x	2^{17}	10752
					16x	2^{18}	11008
8x	2^{12}	4096	2^{15}	7680	4x	2^{17}	10752
					8x	2^{18}	11264
					16x	2^{19}	11520
16x	2^{12}	4096	2^{16}	7936	4x	2^{18}	11008
					8x	2^{19}	11520
					16x	2^{20}	11776

Table 8. KNEE POINTS FOR COMPRESSION TO 12 BITS

T1/T2 Exposure Ratio (R1) R0x3082[3:2]	P1	P_{OUT1} = P1	P2	P_{OUT2} = (P2 − P1) / R1 + P_{OUT1}	T2/T3 Exposure Ratio (R2) R0x3082[5:4]	P_{MAX}	$P_{OUT_{MAX}}$ = (P_{MAX} − P2) / (R1 × R2) + P_{OUT2}
4x	2^{11}	2048	2^{14}	2944	8x	2^{17}	3840
					16x	2^{18}	3904
8x	2^{11}	2048	2^{15}	3008	4x	2^{17}	3776
					8x	2^{18}	3904
					16x	2^{19}	3968
16x	2^{11}	2048	2^{16}	3040	4x	2^{18}	3808
					8x	2^{19}	3936
					16x	2^{20}	4000

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HDR Specific Exposure Settings

In HDR mode, pixel values are stored in line buffers while waiting for all 3 exposures to be available for final pixel data combination. There are 42 line buffers used to store intermediate T1 data. Due to this limitation, the maximum coarse integration time possible is equal to 42 × T1 / T2 lines.

For example, if R0x3082[3:2] = 2, the sensor is set to have T1/T2 ratio = 16x. Therefore the maximum number of integration lines is 42 × 16 = 672 lines.

If coarse integration time is greater than this, the T2 integration time will stay at 42. The sensor will calculate the ratio internally,enabling the linearization to be performed. If companding is being than relinearization would still follow the programmed ratio. For example if the T1 / T2 ratio was programmed to 16x but coarse integration was increased beyond 672 than one would still use the 16x relinearization formulas.

An additional limitation is the maximum number of exposure lines in relation to the frame_length_lines register. In Linear mode, maximum coarse_integration_time = frame_length_lines − 1. However in HDR mode, since the coarse integration time register controls T1, the max coarse_integration time is frame_length_lines − 45.

Putting the two criteria listed above together, it can be summarized as follows:

$$\text{maximum coarse_integration_time} = \text{minimum}(42 \times T1/T2, \text{frame_length_lines} - 45) \quad \text{(eq. 3)}$$

In HDR mode, subline integration is not utilized. As such, fine integration time register changes will have no effect on the image.

There is also a limitation of the minimum number of exposure lines that can be used. This is summarized in the following formula:

$$\text{minimumcoarse_integration_time} = (0.5) \times (T1/T2) \times (T2/T3) \quad \text{(eq. 4)}$$

Due to limitation on the internal floating point calculation, the exact ratio specified by the RATIO_T2_T3 (R0x3082[5:4]) may not be achievable.

When using companded output in combination with certain exposure ratios (other than T1 / T2 = 16x and T2 / T3 = 16x), digital gain needs to be set to a fixed value. Table 9 provides the proper digital gain settings for each T1 / T2 and T2 / T3 ratio.

Table 9. DIGITAL GAIN SETTING FOR EACH T1 / T2 AND T2 / T3 RATIO

T1 / T2 Ratio	T2 / T3 Ratio	Setting for Digital Gain Register (0x305E Context A or 0x30C4 Context B)
4	4	0x02h
4	8	0x04h
4	16	0x08h
8	4	0x04h
8	8	0x08h
8	16	0x10h
16	4	0x08h
16	8	0x10h
16	16	Any Legal Value

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Motion Compensation

In typical multi−exposure HDR systems, motion artifacts can be created when objects move during the T1, T2 or T3 integration time. When this happens, edge artifacts can potentially be visible and might look like a ghosting effect.

To correct this feature, the MT9M034 has special 2D motion compensation circuitry that detects motion artifacts and corrects the image accordingly.

There are two motion compensation options available. One using the default HDR motion compensation by setting R0x318C[14] = 1. Additional parameters are available to control the extent of motion detection and correction as per the requirements of the specific application. These can be set in R0x318C−R0x3190. The other is using the DLO method of HDR combination. When using DLO, R0x318C[14] is ignored. DLO is enabled by setting R0x3190[13] = 1. Noise filtering is enabled by setting R0x3190[14] = 1. For more information, please refer to the MT9M034 Register Reference document.

REAL−TIME CONTEXT SWITCHING

In the MT9M034, the user may switch between two full register sets (listed in Table 10) by writing to a context switch change bit in R0x30B0[13]. This context switch will change all registers (no shadowing) at the frame start time and have the new values apply to the immediate next exposure and readout time.

Table 10. REAL−TIME CONTEXT−SWITCH REGISTERS

Register Description	Register Number	
	Context A	Context B
Y_Addr_Start	R0x3002	R0x308C
X_Addr_Start	R0x3004	R0x308A
Y_Addr_End	R0x3006	R0x3090
X_Addr_End	R0x3008	R0x308E
Coarse_Integration_Time	R0x3012	R0x3016
Fine_Integration_Time	R0x3014	R0x3018
Y_Odd_Inc	R0x30A6	R0x30A8
Column Gain	R0x30B0[5:4]	R0x30B0[9:8]
Green1_Gain (GreenR)	R0x3056	R0x30BC
Blue_Gain	R0x3058	R0x30BE
Red_Gain	R0x305A	R0x30C0
Green2_Gain (GreenB)	R0x305C	R0x30C2
Global_Gain	R0x305E	R0x30C4
Frame_Length_Lines	R0x300A	R0x30AA
Digital_Binning	R0x3032[1:0]	R0x3032[5:4]
Operation_Mode_Ctrl	0x3082	0x3084

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FEATURES

See the MT9M034 Register Reference for additional details.

Reset

The MT9M034 may be reset by using RESET_BAR (active LOW) or the reset register.

Hard Reset of Logic

The RESET_BAR pin can be connected to an external RC circuit for simplicity. The recommended RC circuit uses a 10 kΩ resistor and a 0.1 μF capacitor. The rise time for the RC circuit is 1 μs maximum.

Soft Reset of Logic

Soft reset of logic is controlled by the R0x301A Reset register. Bit 0 is used to reset the digital logic of the sensor while preserving the existing two−wire serial interface configuration. Furthermore, by asserting the soft reset, the sensor aborts the current frame it is processing and starts a new frame. This bit is a self−resetting bit and also returns to "0" during two−wire serial interface reads.

Clocks

The MT9M034 requires one clock input (EXTCLK).

PLL−Generated Master Clock

The PLL contains a prescaler to divide the input clock applied on EXTCLK, a VCO to multiply the prescaler output, and two divider stages to generate the output clock. The clocking structure is shown in Figure 12. PLL control registers can be programmed to generate desired master clock frequency.

NOTE: The PLL control registers must be programmed while the sensor is in the software Standby state. The effect of programming the PLL divisors while the sensor is in the streaming state is undefined.

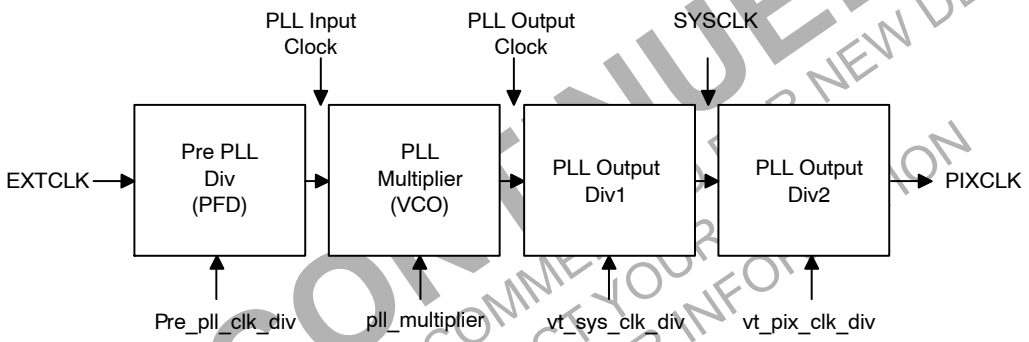


Figure 12. PLL−Generated Master Clock PLL Setup

The PLL is enabled by default on the MT9M034. To configure and use the PLL:

1. Bring the MT9M034 up as normal; make sure that ^{f}EXTCLK is between 6 and 50 MHz and ensure the sensor is in software standby (R0x301A−B[2] = 0). PLL control registers must be set in software standby.
2. Set pll_multiplier, pre_pll_clk_div, vt_sys_clk_siv, and vt_pix_clk_div based on the desired input (f_{EXTCLK}) and output (f_{PIXCLK}) frequencies. Determine the M, N, P1, and P2 values to achieve the desired f_{PIXCLK} using this formula:
   fPIXCLK= (fEXTCLK × M) / (N × P1 x P2)
   where
   M = PLL_Multiplier
   N = Pre_PLL_Clk_Div
   P1 = Vt_Sys_Clk_Div
   P2 = Vt_PIX_Clk_Div
3. Wait 1 ms to ensure that the VCO has locked.
4. Set R0x301A[2] = 1 to enable streaming and to switch from EXTCLK to the PLL−generated clock.

NOTE:

1. The PLL can be bypassed at any time (sensor will run directly off EXTCLK) by setting R0x30B0[14] = 1. The PLL is always bypassed in software standby mode. To disable the PLL, the sensor must be in standby mode (R0x301A[2] = 0)
2. The following restrictions apply to the PLL tuning parameters:
   32 ≤ M ≤ 255
   1 ≤ N ≤ 63
   1 ≤ P1 ≤ 16(P1 = 1, 2, 3, 4, 6, 8, 10, 12, 14, 16)
   4 ≤ P2 ≤ 16
3. The VCO frequency, defined as $f_{VCO} = f_{EXTCLK} \times M / N$ must be within 384−768 MHz.
4. When PLL_Multiplier is odd, 2 MHz <= f_{EXTCLK} / N <= 24 MHz

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The user can utilize the Register Wizard tool accompanying DevWare to generate PLL settings given a supplied input clock and desired output frequency.

Spread−Spectrum Clocking

To facilitate improved EMI performance, the external clock input allows for spread spectrum sources, with no impact on image quality. Limits of the spread spectrum input clock are:

- 5% maximum clock modulation
- 35 KHz maximum modulation frequency
- Accepts triangle wave modulation, as well as sine or modified triangle modulations.

Stream/Standby Control

The sensor supports two standby modes: Hard Standby and Soft Standby. In both modes, external clock can be optionally disabled to further minimize power consumption. If this is done, then the "Power−Up Sequence" must be followed.

Soft Standby

Soft Standby is a low power state that is controlled through register R0x301A[2]. Depending on the value of R0x301A[4], the sensor will go to standby after completion of the current frame readout (default behavior) or after the completion of the current row readout. When the sensor comes back from Soft Standby, previously written register settings are still maintained. Soft standby will not occur if the TRIGGER pin is held high.

A specific sequence needs to be followed to enter and exit from Soft Standby.

Entering Soft Standby:

1. Set R0x301A[2] = 0 and drive the TRIGGER pin LOW
2. External clock can be turned off to further minimize power consumption (Optional)

Exiting Soft Standby:

1. Enable external clock if it was turned off
2. R0x301A[2] = 1 or drive the TRIGGER pin HIGH

Hard Standby

Hard Standby puts the sensor in lower power state; previously written register settings are still maintained.

A specific sequence needs to be followed to enter and exit from Hard Standby.

Entering Hard Standby:

1. R0x301A[8] = 1
2. Assert STANDBY pin
3. External clock can be turned off to further minimize power consumption (Optional)

Exiting Hard Standby:

1. Enable external clock if it was turned off
2. De−assert STANDBY pin
3. Set R0x301A[8] = 0

Window Control

Registers x_addr_start, x_addr_end, y_addr_start, and y_addr_end control the size and starting coordinates of the image window.

The exact window height and width out of the sensor is determined by the difference between the Y address start and end registers or the X address start and end registers, respectively.

The MT9M034 allows different window sizes for context A and context B.

Blanking Control

Horizontal blank and vertical blank times are controlled by the line_length_pck and frame_length_lines registers, respectively.

- Horizontal blanking is specified in terms of pixel clocks. It is calculated by subtracting the X window size from the line_length_pck register. The minimum horizontal blanking is 370 pixel clocks.
- Vertical blanking is specified in terms of numbers of lines. It is calculated by subtracting the Y window size from the frame_length_lines register. The minimum vertical blanking is 26 lines.

The actual imager timing can be calculated using Table 5 and Table 6, which describe the Line Timing and FV/LV signals.

When in HDR mode, the maximum size is 1280 × 960.

Readout Modes

Digital Binning

By default, the resolution of the output image is the full width and height of the FOV as defined above. The output resolution can be reduced by digital binning. For RGB and monochrome mode, this is set by the register R0x3032. For Context A, use bits [1:0], for Context B, use bits [5:4]. Available settings are:

00 = No binning
01 = Horizontal binning
10 = Horizontal and vertical binning

Binning gives the advantage of reducing noise at the cost of reduced resolution. When both horizontal and vertical binning are used, a 2x improvement in SNR is achieved, therefore improving low light performance. Binning results in a smaller resolution image, but the FOVs between the binned and unbinned images are the same.

Bayer Space Resampling

All of the pixels in the FOV contribute to the output image in digital binning mode. This can result in a more pleasing output image with reduced subsampling artifacts. It also improves low−light performance. For RGB mode, resampling can be enabled by setting of register 0x306E[4] = 1.

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Mirror

Column Mirror Image

By setting R0x3040[14] = 1, the readout order of the columns is reversed, as shown in Figure 13. The starting Bayer color pixel is maintained in this mode by a 1−pixel shift in the imaging array.

When using horizontal mirror mode, the user must retrigger column correction. Please refer to the column correction section to see the procedure for column correction retriggering. Bayer resampling must be enabled, by setting bit 4 of register 0x306E[4] = 1.

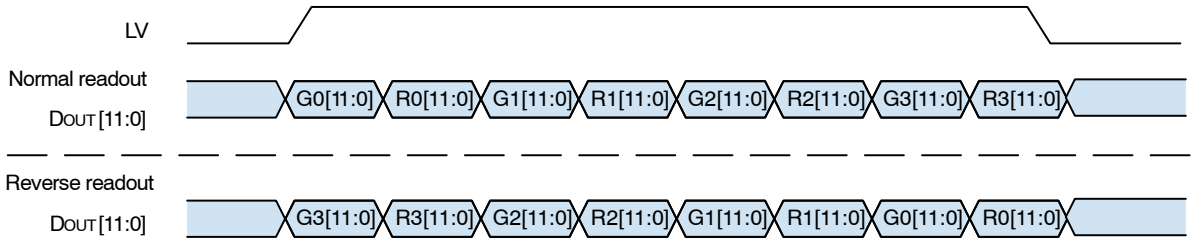


Figure 13. Eight Pixels in Normal and Column Mirror Readout Modes

Row Mirror Image

By setting R0x3040[15] = 1, the readout order of the rows is reversed as shown in Figure 14. The starting Bayer color pixel is maintained in this mode by a 1−pixel shift in the imaging array. When using horizontal mirror mode, the user must retrigger column correction. Please refer to the column correction section to see the procedure for column correction retriggering.

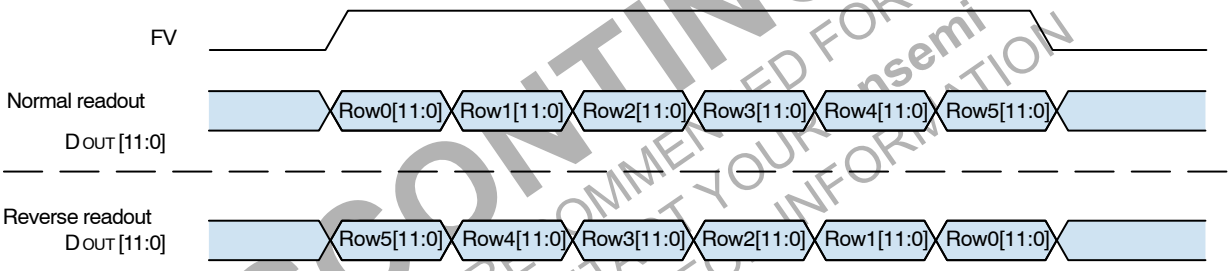


Figure 14. Six Rows in Normal and Row Mirror Readout Modes

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Maintaining a Constant Frame Rate

Maintaining a constant frame rate while continuing to have the ability to adjust certain parameters is the desired scenario. This is not always possible, however, because register updates are synchronized to the read pointer, and the shutter pointer for a frame is usually active during the readout of the previous frame. Therefore, any register changes that could affect the row time or the set of rows sampled causes the shutter pointer to start over at the beginning of the next frame.

By default, the following register fields cause a “bubble” in the output rate (that is, the vertical blank increases for one frame) if they are written in video mode, even if the new value would not change the resulting frame rate. The following list shows only a few examples of such registers; a full listing can be seen in the MT9M034 Register Reference.

- x_addr_start
- x_addr_end
- y_addr_start
- y_addr_end
- frame_length_lines
- line_length_pclk
- coarse_integration_time
- fine_integration_time
- read_mode

The size of this bubble is (Integration_Time × t_{ROW}), calculating the row time according to the new settings.

The Coarse_Integration_Time and Fine_Integration _Time fields may be written to without causing a bubble in the output rate under certain circumstances. Because the shutter sequence for the next frame often is active during the output of the current frame, this would not be possible without special provisions in the hardware. Writes to these registers take effect two frames after the frame they are written, which allows the integration time to increase without interrupting the output or producing a corrupt frame (as long as the change in integration time does not affect the frame time).

Synchronizing Register Writes to Frame Boundaries

Changes to most register fields that affect the size or brightness of an image take effect on two frames after the one during which they are written. These fields are noted as "synchronized to frame boundaries" in the MT9M034 Register Reference. To ensure that a register update takes effect on the next frame, the write operation must be completed after the leading edge of FV and before the trailing edge of FV.

Fields not identified as being frame−synchronized are updated immediately after the register write is completed. The effect of these registers on the next frame can be difficult to predict if they affect the shutter pointer.

Restart

To restart the MT9M034 at any time during the operation of the sensor, write a "1" to the Restart register (R0x301A[1] = 1). This has two effects: first, the current frame is interrupted immediately. Second, any writes to frame−synchronized registers and the shutter width registers take effect immediately, and a new frame starts (in video mode). The current row completes before the new frame is started, so the time between issuing the Restart and the beginning of the next frame can vary by about t_{ROW}.

Image Acquisition Modes

The MT9M034 supports two image acquisition modes: video(master) and single frame.

Video

The video mode takes pictures by scanning the rows of the sensor twice. On the first scan, each row is released from reset, starting the exposure. On the second scan, the row is sampled, processed, and returned to the reset state. The exposure for any row is therefore the time between the first and second scans. Each row is exposed for the same duration, but at slightly different point in time, which can cause a shear in moving subjects as is typical with electronic rolling shutter sensors.

Single Frame

The single−frame mode operates similar to the video mode. It also scans the rows of the sensor twice, first to reset the rows and second to read the rows. Unlike video mode where a continuous stream of images are output from the image sensor, the single−frame mode outputs a single frame in response to a high state placed on the TRIGGER input pin. As long as the TRIGGER pin is held in a high state, new images will be read out. After the TRIGGER pin is returned to a low state, the image sensor will not output any new images and will wait for the next high state on the TRIGGER pin.

The TRIGGER pin state is detected during the vertical blanking period (i.e. the FV signal is low). The pin is level sensitive rather than edge sensitive. As such, image integration will only begin when the sensor detects that the TRIGGER pin has been held high for three consecutive clock cycles. If the trigger signal is applied to multiple sensors at the same time, the single frame output of the sensors will be synchronized to within 1 PIXCLK if is PLL disabled or 2 PIXCLKs if PLL is enabled.

During integration time of single−frame mode and video mode, the FLASH output pin is at high.

Continuous Trigger

In certain applications, multiple sensors need to have their video streams synchronized (E.g. surround view or panorama view applications). The TRIGGER pin can also be used to synchronize output of multiple image sensors together and still get a video stream. This is called continuous trigger mode. Continuous trigger is enabled by holding the TRIGGER pin high. Alternatively, the TRIGGER pin can be held high until the stream bit is enabled (R0x301A[2] = 1) then can be released for continuous synchronized video streaming.

If the TRIGGER pins for all connected MT9M034 sensors are connected to the same control signal, all sensors will receive the trigger pulse at the same time. If they are configured to have the same frame timing, then the usage of the TRIGGER pin guarantees that all sensors will be synchronized within 1 PIXCLK cycle if PLL is disabled, or 2 PIXCLK cycles if PLL is enabled.

With continuous trigger mode, the application can now make use of the video streaming mode while guaranteeing that all sensor outputs are synchronized. As long as the initial trigger for the sensors takes place at the same time, all subsequent video streams will be synchronous.

Temperature Sensor

The MT9M034 sensor has a built−in PTAT−based temperature sensor, accessible through registers, that is capable of measuring die junction temperature.

The temperature sensor can be enabled by writing R0x30B4[0] = 1 and R0x30B4[4] = 1. After this, the temperature sensor output value can be read from R0x30B2[10:0].

The value read out from the temperature sensor register is an ADC output value that needs to be converted downstream to a final temperature value in degrees Celsius. Since the PTAT device characteristic response is quite linear in the temperature range of operation required, a simple linear function in the format of listed in the equation below can be used to convert the ADC output value to the final temperature in degrees Celsius.

$$\text{Temperature} = \text{slope} \times \text{R0x30B2[10 : 0]} + T_0 \quad \text{(eq. 5)}$$

For this conversion, a minimum of 2 known points are needed to construct the line formula by identifying the slope and y−intercept "T_0". These calibration values can be read from registers R0x30C6 and R0x30C8 which correspond to value read at 70°C and 55°C respectively. Once read, the slope and y−intercept values can be calculated and used in the above equation.

For more information on the temperature sensor registers, refer to the MT9M034 Register Reference.

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Automatic Exposure Control

The integrated automatic exposure control (AEC) is responsible for ensuring that optimal settings of exposure and gain are computed and updated every other frame. AEC can be enabled or disabled by R0x3100[0].

When AEC is disabled (R0x3100[0] = 0), the sensor uses the manual exposure value in coarse and fine shutter width registers and the manual gain value in the gain registers.

When AEC is enabled (R0x3100[0] = 1), the target luma value in linear mode is set by R0x3102. For the MT9M034 this target luma has a default value of 0x0800 or about half scale. For HDR mode, the luma target maximum auto exposure value is limited by R0x311C; the minimum auto exposure is limited by R0x311E. These values are in units of line−times.

The exposure control measures current scene luminosity by accumulating a histogram of pixel values while reading out a frame. It then compares the current luminosity to the desired output luminosity. Finally, the appropriate adjustments are made to the exposure time and gain. All pixels are used, regardless of color or mono mode. In HDR mode, the coarse and fine integration time is the longest integration time of the three integration, the other two shorter integration are generated automatically base on the pre−defined exposure ratios. When using non−default HDR exposure ratios, auto_dg_en should not be enabled (R0x3100[4] = 0) due to required digital gains as documented in Table 9.

Embedded Data and Statistics

The MT9M034 has the capability to output image data and statistics embedded within the frame timing. There are 2 types of information embedded within the frame readout:

1. Embedded Data: If enabled, these are displayed on the 2 rows immediately before the first active pixel row is displayed
2. Embedded Statistics: If enabled, these are displayed on the two rows immediately after the last active pixel row is displayed

NOTE: Embedded data and embedded statistics must be enabled or disabled together.

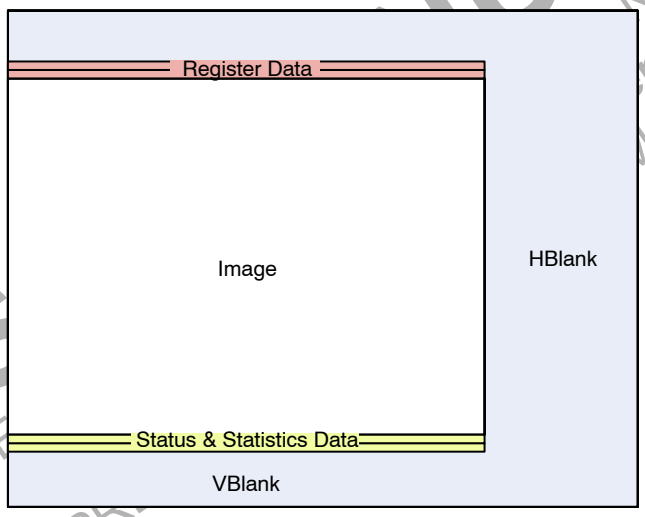


Figure 15. Frame Format with Embedded Data Lines Enabled

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Embedded Data

The embedded data contains the configuration of the image being displayed. This includes all register settings used to capture the current frame. The registers embedded in these rows are as follows:

Line 1:

Registers R0x3000 to R0x312F

Line 2:

Registers R0x3136 to R0x31BF, R0x31D0 to R0x31FF

NOTE: All non−defined registers will have a value of 0.

In parallel mode, since the pixel word depth is 12−bits/pixel, the sensor 16−bit register data will be transferred over two pixels where the register data will be broken up into eight msb and eight lsb. The alignment of the 8 bit data will be on the 8MSB bits of the 12−bit pixel word. For example, if a register value of 0x1234 is to be transmitted, it will be transmitted over 2, 12−bit pixels as follows: 0x120, 0x340.

The first pixel of each line in the embedded data is a tag value of 0x0A0. This signifies that all subsequent data is 8 bit data aligned to the MSB of the 12−bit pixel.

The figure below summarizes how the embedded data transmission looks like. It should be noted that data, as shown in Figure 16, is aligned to the MSB of each word:



Figure 16. Format of Embedded Data Output within a Frame

The data embedded in these rows are as follows:

- 0x0A0 – identifier
- 0xAA0
- Register Address MSB of the first register
- 0xA50
- Register Address LSB of the first register
- 0x5A0
- Register Value MSB of the first register addressed
- 0x5A0
- Register Value LSB of the first register addressed
- 0x5A0
- Register Value MSB of the register at first address + 2
- 0x5A0
- Register Value LSB of the register at first address + 2
- 0x5A0
- etc.

Embedded Statistics

The embedded statistics contain frame identifiers and histogram information of the image in the frame. This can be used by downstream auto−exposure algorithm blocks to make decisions about exposure adjustment.

This histogram is divided into 244 bins with a bin spacing of 64 evenly spaced bins for digital code values 0 to 2^{12}, 120 evenly spaced bins for values 2^{12} to 2^{16}, 60 evenly spaced bins for values 2^{16} to 2^{20}. In HDR with a 16x exposure ratio, this approximately corresponds to the T1, T2, T3 exposures respectively.

The first pixel of each line in the embedded statistics is a tag value of 0x0B0. This signifies that all subsequent statistics data is 10 bit data aligned to the MSB of the 12−bit pixel.

The figure below summarizes how the embedded statistics transmission looks like. It should be noted that data, as shown in Figure 17, is aligned to the msb of each word:

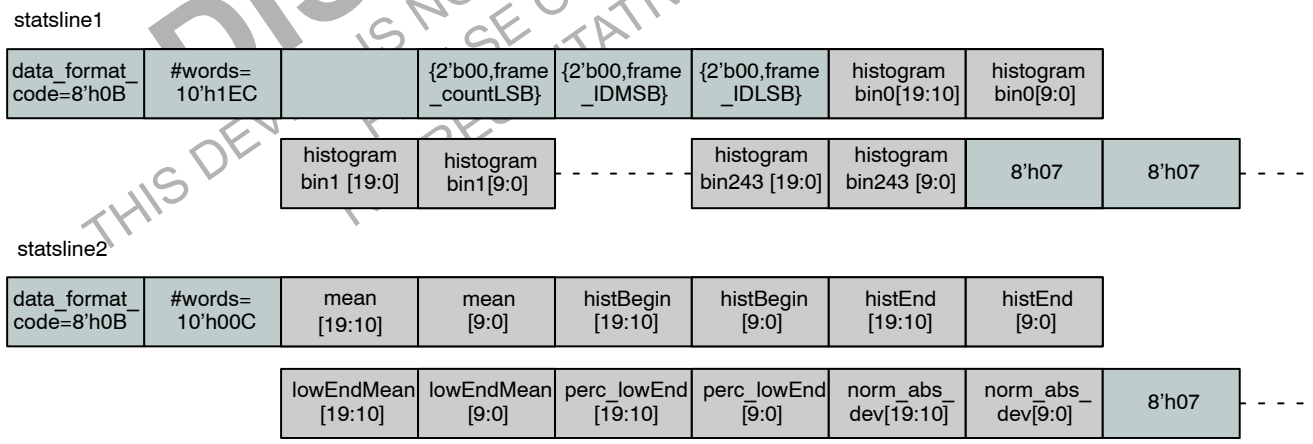


Figure 17. Format of Embedded Statistics Output within a Frame

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The statistics embedded in these rows are as follows:

Line 1:

- 0x0B0 – (identifier)
- Register 0x303A – frame_count
- Register 0x31D2 – frame ID
- Histogram data – histogram bins 0–243

Line 2:

- 0x0B0 (identifier)
- Mean
- Histogram Begin
- Histogram End
- Low End Histogram Mean
- Percentage of Pixels Below Low End Mean
- Normal Absolute Deviation

Gain

Digital Gain

Digital gain can be controlled globally by R0x305E (Context A) or R0x30C4 (Context B). There are also registers that allow individual control over each Bayer color (GreenR, GreenB, Red, Blue).

The format for digital gain setting is *xxx.yyyyy* where 0b00100000 represents a 1x gain setting and 0b00110000 represents a 1.5x gain setting. The step size for yyyyy is 0.03125 while the step size for xxx is 1. Therefore to set a gain of 2.09375 one would set digital gain to 01000011.

Analog Gain

The MT9M034 has a column parallel architecture and therefore has an Analog gain stage per column.

There are 2 stages of analog gain, the first stage can be set to 1x, 2x, 4x or 8x. This can be set in R0x30B0[5:4] (Context A) or R0x30B0[9:8] (Context B). The second stage is capable of setting an additional 1x or 1.25x gain which can be set in R0x3EE4[9:8].

This allows the maximum possible analog gain to be set to 10x.

Black Level Correction

Black level correction is handled automatically by the image sensor. No adjustments are provided except to enable or disable this feature. Setting R0x30EA[15] disables the automatic black level correction. Default setting is for automatic black level calibration to be enabled.

The automatic black level correction measures the average value of pixels from a set of optically black lines in the image sensor. The pixels are averaged as if they were light−sensitive and passed through the appropriate gain. This line average is then digitally low−pass filtered over many frames to remove temporal noise and random instabilities associated with this measurement. The new filtered average is then compared to a minimum acceptable level, low threshold, and a maximum acceptable level, high threshold. If the average is lower than the minimum acceptable level, the offset correction value is increased by a predetermined amount. If it is above the maximum level, the offset correction value is decreased by a predetermined amount. The high and low thresholds have been calculated to avoid oscillation of the black level from below to above the targeted black level.

Row−wise Noise Correction

Row (Line)−wise Noise Correction is handled automatically by the image sensor. No adjustments are provided except to enable or disable this feature. Clearing R0x3044[10] disables the row noise correction. Default setting is for row noise correction to be enabled.

Row−wise noise correction is performed by calculating an average from a set of optically black pixels at the start of each line and then applying each average to all the active pixels of the line.

Column Correction

The MT9M034 uses column parallel readout architecture to achieve fast frame rate. Without any corrections, the consequence of this architecture is that different column signal paths have slightly different offsets that might show up on the final image as structured fixed pattern noise.

MT9M034 has column correction circuitry that measures this offset and removes it from the image before output. This is done by sampling dark rows containing tied pixels and measuring an offset coefficient per column to be corrected later in the signal path.

Column correction can be enabled/disabled via R0x30D4[15]. Additionally, the number of rows used for this offset coefficient measurement is set in R0x30D4[3:0]. By default this register is set to 0x7, which means that 8 rows are used. This is the recommended value. Other control features regarding column correction can be viewed in the MT9M034 Register reference. Any changes to column correction settings need to be done when the sensor streaming is disabled and the appropriate triggering sequence must be followed as described below.

Column Correction Triggering

Column correction requires a special procedure to trigger depending on which state the sensor is in.

Column Triggering on Startup

When streaming the sensor for the first time after powerup, a special sequence needs to be followed to make sure that the column correction coefficients are internally calculated properly.

1. Follow proper power up sequence for power supplies and clocks
2. Apply sequencer settings if needed (Linear or HDR mode)
3. Apply frame timing and PLL settings as required by application
4. Set analog gain to 1x and low conversion gain (R0x30B0 = 0x1300)
5. Enable column correction and settings (R0x30D4 = 0xE007)

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6. Disable auto re−trigger for change in conversion gain or col_gain, and enable column correction always (R0x30BA = 0x0008)
7. Enable streaming (R0x301A[2] = 1) or drive the TRIGGER pin HIGH
8. Wait nine frames to settle (First frame after coming up from standby is internally column correction disabled)
9. Disable streaming (R0x301A[2] = 0)

After this, the sensor has calculated the proper column correction coefficients and the sensor is ready for streaming. Any other settings (including gain, integration time and conversion gain etc.) can be done afterwards without affecting column correction.

Column Correction Retriggering Due to Mode Change

Since column offsets is sensitive to changes in the analog signal path, such changes require column correction circuitry to be retriggered for the new path. Examples of such mode changes include: horizontal mirror, vertical mirror, changes to column correction settings.

When such changes take place, the following sequence needs to take place:

1. Disable streaming (R0x301A[2] = 0) or drive the TRIGGER pin LOW
2. Enable streaming (R0x301A[2] = 1) or drive the TRIGGER pin HIGH
3. Wait nine frames to settle

NOTE: The above steps are not needed if the sensor is being reset (soft or hard reset) upon the mode change.

Defective Pixel Correction

Defective Pixel Correction is intended to compensate for defective pixels by replacing their value with a value based on the surrounding pixels, making the defect less noticeable to the human eye. The defect pixel correction feature supports up to 200 defects. The locations of defective pixels are stored in a table on chip during the manufacturing process; this table is accessible through the two−wire serial interface. There is no provision for later augmenting the defect table entries.

The DPC algorithm is one−dimensional, calculating the resulting averaged pixel value based on nearby pixels within a row. The algorithm distinguishes between color and monochrome parts; for color parts, the algorithm uses nearest neighbor in the same color plane.

At high gain, long exposure, and high temperature conditions, the performance of this function can degrade.

Test Patterns

The MT9M034 has the capability of injecting a number of test patterns into the top of the datapath to debug the digital logic. With one of the test patterns activated, any of the datapath functions can be enabled to exercise it in a deterministic fashion. Test patterns are selected by Test_Pattern_Mode register (R0x3070). Only one of the test patterns can be enabled at a given point in time by setting the Test_Pattern_Mode register according to Table 11. When test patterns are enabled the active area will receive the value specified by the selected test pattern and the dark pixels will receive the value in Test_Pattern_Green (R0x3074 and R0x3078) for green pixels, Test_Pattern_Blue (R0x3076) for blue pixels, and Test_Pattern_Red (R0x3072) for red pixels.

NOTE: Turn off black level calibration (BLC) when Test Pattern is enabled.

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Table 11. TEST PATTERN MODES

Test_Pattern_Mode	Test Pattern Output
0	No test pattern (normal operation)
1	Solid color test pattern
2	100% color bar test pattern
3	Fade−to−gray color bar test pattern
256	Walking 1s test pattern (12−bit)

Color Field

When the color field mode is selected, the value for each pixel is determined by its color. Green pixels will receive the value in Test_Pattern_Green, red pixels will receive the value in Test_Pattern_Red, and blue pixels will receive the value in Test_Pattern_Blue.

Vertical Color Bars

When the vertical color bars mode is selected, a typical color bar pattern will be sent through the digital pipeline.

Walking 1s

When the walking 1s mode is selected, a walking 1s pattern will be sent through the digital pipeline. The first value in each row is 1.

TWO−WIRE SERIAL REGISTER INTERFACE

The two−wire serial interface bus enables read/write access to control and status registers within the MT9M034.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to V_{DD_IO} off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive SDATA LOW−the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two−wire serial interface specification allow the slave device to drive SCLK LOW; the MT9M034 uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two−wire serial interface bus are performed by a sequence of low−level protocol elements:

1. a (repeated) start condition
2. a slave address/data direction byte
3. an (a no) acknowledge bit
4. a message byte
5. a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH−to−LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a "repeated start" or "restart" condition.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A "0" in bit [0] indicates a WRITE, and a "1" indicates a READ. The default slave addresses used by the MT9M034 are 0x20 (write address) and 0x21 (read address) in accordance with the specification. Alternate slave addresses of 0x30 (write address) and 0x31 (read address) can be selected by enabling and asserting the SADDR input.

An alternate slave address can also be programmed through R0x31FC.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No−Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a "0" indicates a write and a "1" indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which the WRITE should take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8−bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The slave's internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

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Single READ from Random Location

This sequence (Figure 18) starts with a dummy WRITE to the 16−bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8−bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. Figure 18 shows how the internal register address maintained by the MT9M034 is loaded and incremented as the sequence proceeds.

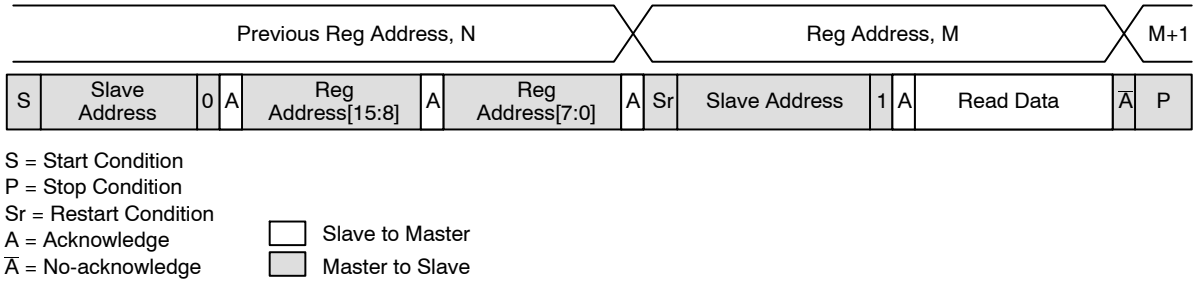


Figure 18. Single READ from Random Location

Single READ From Current Location

This sequence (Figure 19) performs a read using the current value of the MT9M034 internal register address. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

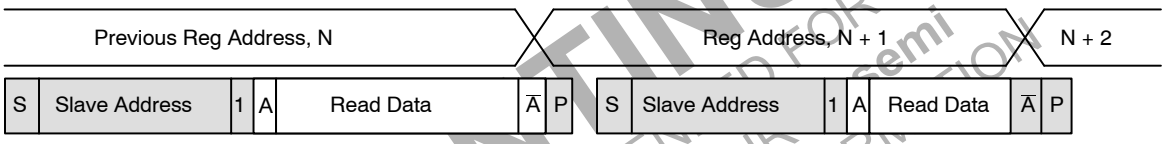


Figure 19. Single READ from Current Location

Sequential READ, Start From Random Location

This sequence (Figure 20) starts in the same way as the single READ from random location (Figure 18). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

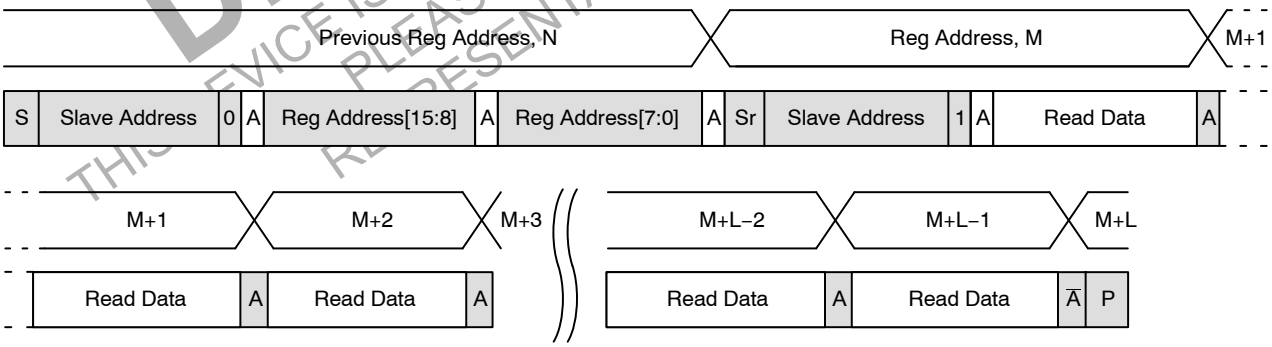


Figure 20. Sequential READ, Start from Random Location

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Sequential READ, Start From Current Location

This sequence (Figure 21) starts in the same way as the single READ from current location (Figure 19). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.



Figure 21. Sequential READ, Start from Current Location

Single WRITE to Random Location

This sequence (Figure 22) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

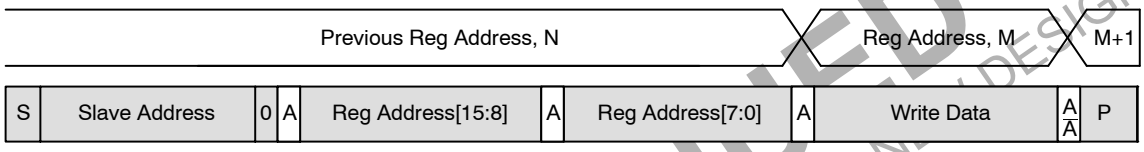


Figure 22. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 23) starts in the same way as the single WRITE to random location (Figure 22). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

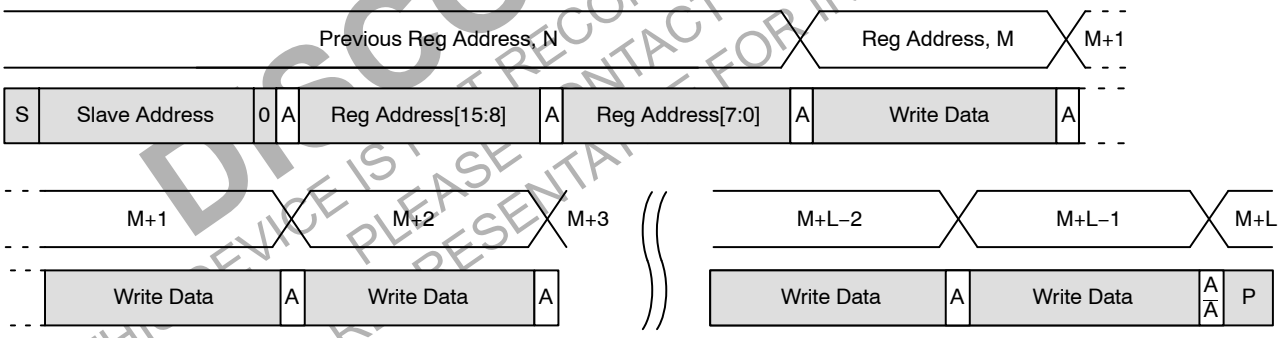


Figure 23. Sequential WRITE, Start at Random Location

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SPECTRAL CHARACTERISTICS

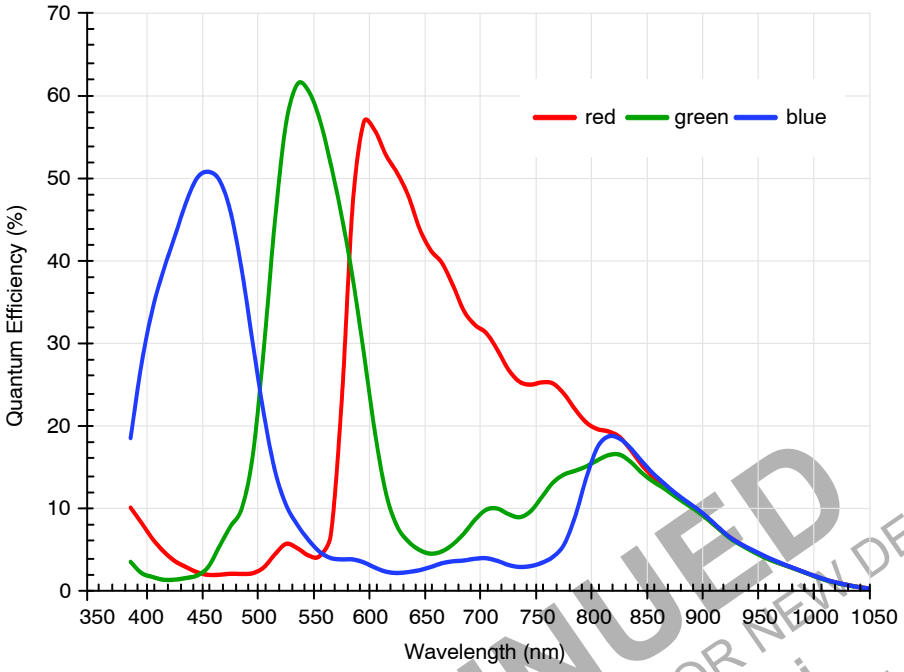


Figure 24. Quantum Efficiency – Color Sensor

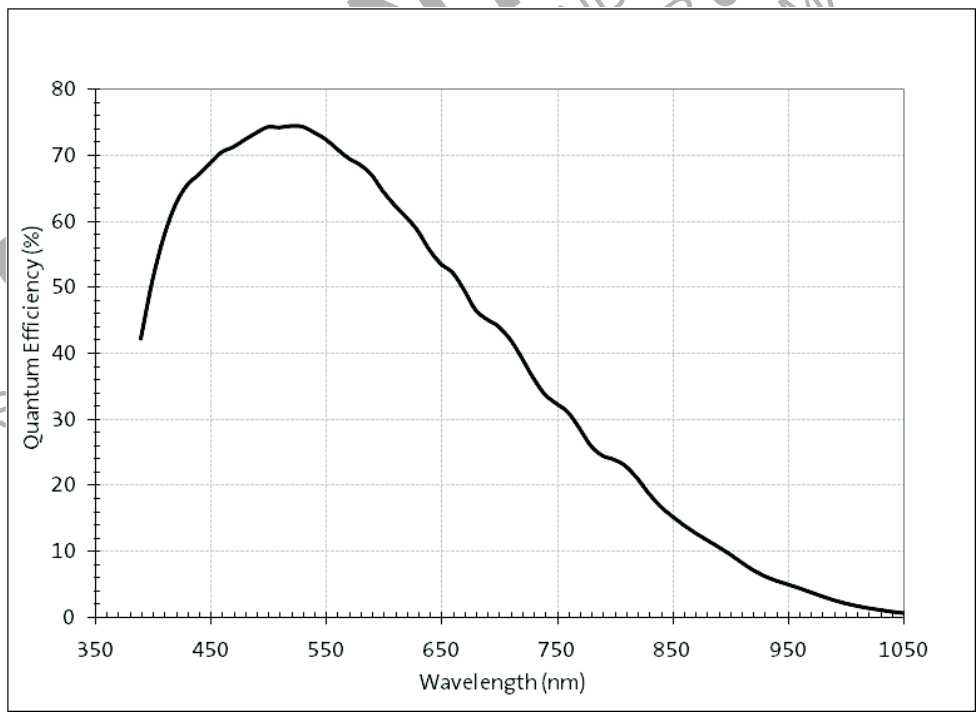


Figure 25. Estimated Quantum Efficiency – Monochrome Sensor

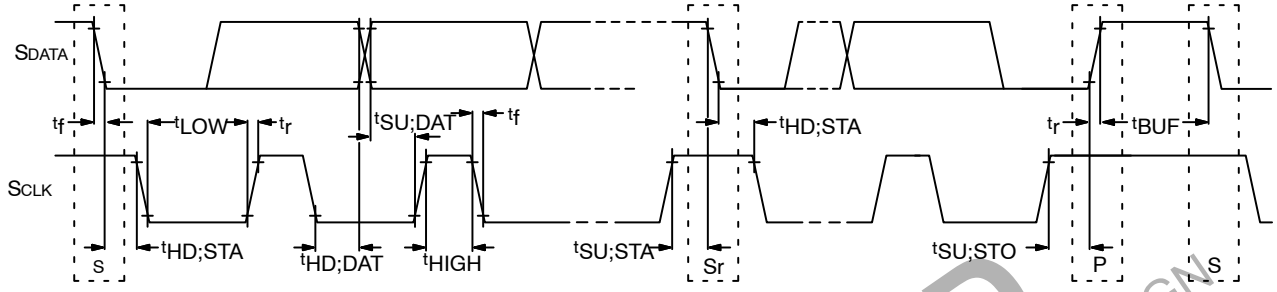
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ELECTRICAL SPECIFICATIONS

Unless otherwise stated, the following specifications apply to the following conditions:
V_{DD} = 1.8 V − 0.10 / +0.15; V_{DD}_IO = V_{DD}_PLL = V_{AA} = V_{AA}_PIX = 2.8 V ±0.3 V ;
T_A = −30°C to +70°C; output load = 10 pF; frequency = 74.25 MHz.

Two-Wire Serial Register Interface

The electrical characteristics of the two−wire serial register interface (S_{CLK}, S_{DATA}) are shown in Figure 26 and Table 12.



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Figure 26. Two-Wire Serial Bus Timing Parameters

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Table 12. TWO-WIRE SERIAL BUS CHARACTERISTICS

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V; T_A = 25°C

Parameter	Symbol	Standard−Mode		Fast−Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	^{f}SCL	0	100	0	400	kHz
Hold Time (Repeated) START Condition						
After this Period, the First Clock Pulse is Generated	^{t}HD;STA	4.0	–	0.6	–	μs
LOW Period of the SCLK Clock	^{t}LOW	4.7	–	1.3	–	μs
HIGH Period of the SCLK Clock	^{t}HIGH	4.0	–	0.6	–	μs
Set−up Time for a Repeated START Condition	^{t}SU;STA	4.7	–	0.6	–	μs
Data Hold Time	^{t}HD;DAT	0 (Note 5)	3.45 (Note 6)	0 (Note 7)	0.9 (Note 6)	μs
Data Set−up Time	^{t}SU;DAT	250	–	100[6]	–	ns
Rise Time of Both SDATA and SCLK Signals	^{t}r	–	1000	20 + 0.1Cb (Note 8)	300	ns
Fall Time of Both SDATA and SCLK Signals	^{t}f	–	300	20 + 0.1Cb (Note 8)	300	ns
Set−up Time for STOP Condition	^{t}SU;STO	4.0	–	0.6	–	μs
Bus Free Time between a STOP and START Condition	^{t}BUF	4.7	–	1.3	–	μs
Capacitive Load for Each Bus Line	Cb	–	400	–	400	pF
Serial Interface Input pin Capacitance	CIN_SI	–	3.3	–	3.3	pF
SDATA Max Load Capacitance	CLOAD_SD	–	30	–	30	pF
SDATA Pull−up Resistor	RSD	1.5	4.7	1.5	4.7	kΩ

2. This table is based on I^2C standard (v2.1 January 2000). **onsemi**.
3. Two−wire control is I^2C−compatible.
4. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1 V_{DD} levels. Sensor EXCLK = 27 MHz.
5. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
6. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the SCLK signal.
7. A Fast−mode I^2C−bus device can be used in a Standard−mode I^2C−bus system, but the requirement ^{t}SU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard−mode I^2C−bus specification) before the SCLK line is released.
8. Cb = total capacitance of one bus line in pF.

I/O Timing

By default, the MT9M034 launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV, and LV using the rising edge of PIXCLK. This can be changed using register R0x3028.

See Figure 27 and Table 13 for I/O timing (AC) characteristics.

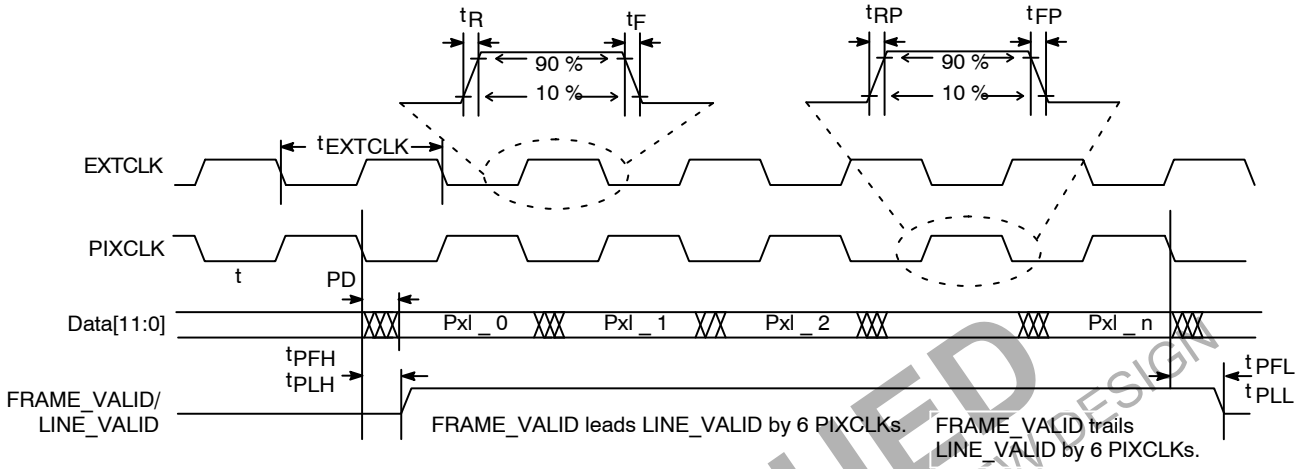


Figure 27. I/O Timing Diagram

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Table 13. I/O TIMING CHARACTERISTICS (2.8 V VDD_IO) (Note 9)

Symbol	Definition	Condition	Min	Typ	Max	Unit
fEXTCLK	Input Clock Frequency		6	–	50	MHz
tEXTCLK	Input Clock Period		20	–	166	ns
tR	Input Clock Rise Time		–	3	–	ns
tF	Input Clock Fall Time		–	3	–	ns
tJITTER	Input Clock Jitter		–	–	600	ps
tRP	Pixclk Rise Time	PCLK slew rate = 6	1.2	–	2.9	ns
tFP	Pixclk Fall Time	PCLK slew rate = 6	1.2	–	2.9	ns
	Pixclk Duty Cycle		45	50	55	%
fPIXCLK	PIXCLK Frequency (Note 10)		6	–	74.25	MHz
tPD	PIXCLK to Data Valid	PCLK slew rate = 6, Parallel slew rate = 7	–2	–	2.5	ns
tPFH	PIXCLK to FV HIGH	PCLK slew rate = 6, Parallel slew rate = 7	–2	–	2.5	ns
tPLH	PIXCLK to LV HIGH	PCLK slew rate = 6, Parallel slew rate = 7	–2	–	2.5	ns
tPFL	PIXCLK to FV LOW	PCLK slew rate = 6, Parallel slew rate = 7	–2	–	2.5	ns
tPLL	PIXCLK to LV LOW	PCLK slew rate = 6, Parallel slew rate = 7	–2	–	2.5	ns

9. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C at 2.5 V, and –30°C at 3.1 V. All values are taken at the 50% transition point. The loading used is 10 pF.
10. Jitter from PIXCLK is already taken into account as the data of all the output parameters.

Table 14. I/O TIMING CHARACTERISTICS (1.8 V VDD_IO) (Note 11)

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{EXTCLK}	Input Clock Frequency		6	–	50	MHz
t_{EXTCLK}	Input Clock Period		20	–	166	ns
t_R	Input Clock Rise Time		–	3	–	ns
t_F	Input Clock Fall Time		–	3	–	ns
t_{JITTER}	Input Clock Jitter		–	–	600	ps
t_{RP}	Pixel Rise Time	PCLK slew rate = 6	1.8	–	4.8	ns
t_{FP}	Pixel Fall Time	PCLK slew rate = 6	1.7	–	4.5	ns
	Pixel Duty Cycle		45	50	55	%
f_{PIXCLK}	PIXCLK Frequency (Note 12)		6		74.25	MHz
t_{PD}	PIXCLK to Data Valid	PCLK slew rate = 6, Parallel slew rate = 7	–2.5	–	2	ns
t_{PFH}	PIXCLK to FV HIGH	PCLK slew rate = 6, Parallel slew rate = 7	–2.5	–	2	ns
t_{PLH}	PIXCLK to LV HIGH	PCLK slew rate = 6, Parallel slew rate = 7	–2.5	–	2	ns
t_{PFL}	PIXCLK to FV LOW	PCLK slew rate = 6, Parallel slew rate = 7	–2.5	–	2	ns
t_{PLL}	PIXCLK to LV LOW	PCLK slew rate = 6, Parallel slew rate = 7	–2.5	–	2	ns

11. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C at 1.7 V, and –30°C at 1.95 V. All values are taken at the 50% transition point. The loading used is 10 pF.
12. Jitter from PIXCLK is already taken into account as the data of all the output parameters.

Table 15. I/O RISE SLEW RATE (2.8 V VDD_IO) (Note 13)

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Unit
7	Default	1.08	1.77	2.72	V/ns
6	Default	0.77	1.26	1.94	V/ns
5	Default	0.58	0.95	1.46	V/ns
4	Default	0.44	0.70	1.08	V/ns
3	Default	0.32	0.51	0.78	V/ns
2	Default	0.23	0.37	0.56	V/ns
1	Default	0.16	0.25	0.38	V/ns
0	Default	0.10	0.15	0.22	V/ns

13. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C at 2.5 V, and –30°C at 3.1 V. The loading used is 10 pF.

Table 16. I/O FALL SLEW RATE (2.8 V VDD_IO) (Note 14)

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Unit
7	Default	1.00	1.62	2.41	V/ns
6	Default	0.76	1.24	1.88	V/ns
5	Default	0.60	0.98	1.50	V/ns
4	Default	0.46	0.75	1.16	V/ns
3	Default	0.35	0.56	0.86	V/ns
2	Default	0.25	0.40	0.61	V/ns
1	Default	0.17	0.27	0.41	V/ns
0	Default	0.11	0.16	0.24	V/ns

14. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C at 2.5 V, and –30°C at 3.1 V. The loading used is 10 pF.

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Table 17. I/O RISE SLEW RATE (1.8 V VDD_IO) (Note 15)

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Unit
7	Default	0.41	0.65	1.10	V/ns
6	Default	0.30	0.47	0.79	V/ns
5	Default	0.24	0.37	0.61	V/ns
4	Default	0.19	0.28	0.46	V/ns
3	Default	0.14	0.21	0.34	V/ns
2	Default	0.10	0.15	0.24	V/ns
1	Default	0.07	0.10	0.16	V/ns
0	Default	0.04	0.06	0.10	V/ns

15. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C at 1.7 V, and –30°C at 1.95 V. The loading used is 10 pF.

Table 18. I/O FALL SLEW RATE (1.8 V VDD_IO) (Note 16)

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Unit
7	Default	0.42	0.68	1.11	V/ns
6	Default	0.32	0.51	0.84	V/ns
5	Default	0.26	0.41	0.67	V/ns
4	Default	0.20	0.32	0.52	V/ns
3	Default	0.16	0.24	0.39	V/ns
2	Default	0.12	0.18	0.28	V/ns
1	Default	0.08	0.12	0.19	V/ns
0	Default	0.05	0.07	0.11	V/ns

16. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C at 1.7 V, and –30°C at 1.95 V. The loading used is 10 pF.

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DC ELECTRICAL CHARACTERISTICS

The DC electrical characteristics are shown in the tables below.

Table 19. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max
V_{DD}	Core Digital Voltage		1.7	1.8	1.95
V_{DD_IO}	I/O Digital Voltage		1.7 / 2.5	1.8 / 2.8	1.9 / 3.1
V_{AA}	Analog Voltage		2.5	2.8	3.1
V_{AA_PIX}	Pixel Supply Voltage		2.5	2.8	3.1
V_{DD_PLL}	PLL Supply Voltage		2.5	2.8	3.1
V_{DD_SLVS}	HiSPi Supply Voltage for SLVS Mode		0.3	0.4	0.6
V_{DD_SLVS}	HiSPi Supply Voltage for HiVcm Mode		1.7	1.8	1.95
V_{IH}	Input HIGH Voltage		$V_{DD_IO} \times 0.7$	–	–
V_{IL}	Input LOW Voltage		–	–	$V_{DD_IO} \times 0.3$
I_{IN}	Input Leakage Current	No pull−up resistor; $V_{IN} = V_{DD_IO}$ or D_{GND}	–	–	20
V_{OH}	Output HIGH Voltage		$V_{DD_IO} - 0.3$	–	–
V_{OL}	Output LOW Voltage		–	–	0.4
I_{OH}	Output HIGH Current	At specified V_{OH}	−22	–	–
I_{OL}	Output LOW Current	At specified V_{OL}	–	–	22

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

CAUTION: Stresses greater than those listed in Table 20 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

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Table 20. ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Condition	Min	Max	Unit
V_{SUPPLY}	Power Supply Voltage (All Supplies)	−0.3	4.5	V	V_{SUPPLY}
I_{SUPPLY}	Total Power Supply Current	–	200	mA	I_{SUPPLY}
I_{GND}	Total Ground Current	–	200	mA	I_{GND}
V_{IN}	DC Input Voltage	−0.3	V_{DD_IO} + 0.3	V	V_{IN}
V_{OUT}	DC Output Voltage	−0.3	V_{DD_IO} + 0.3	V	V_{OUT}
T_{STG} (Note 17)	Storage Temperature	−40	+150	°C	T_{STG} (Note 17)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

17. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
18. To keep dark current and shot noise artifacts from impacting image quality, keep operating temperature at a minimum.

Table 21. OPERATING CURRENT CONSUMPTION IN PARALLEL OUTPUT AND LINEAR MODE

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 1280x960 45 fps	I_{DD1}	–	63	90	mA
I/O Digital Operating Current	Streaming, 1280x960 45 fps	I_{DD_IO}	–	35	40	mA
Analog Operating Current	Streaming, 1280x960 45 fps	I_{AA}	–	30	45	mA
Pixel Supply Current	Streaming, 1280x960 45 fps	I_{AA_PIX}	–	10	15	mA
PLL Supply Current	Streaming, 1280x960 45 fps	I_{DD_PLL}	–	7	15	mA
Digital Operating Current	Streaming, 720p 60 fps	I_{DD1}	–	63	90	mA
I/O Digital Operating Current	Streaming, 720p 60 fps	I_{DD_IO}	–	35	40	mA
Analog Operating Current	Streaming, 720p 60 fps	I_{AA}	–	30	45	mA
Pixel Supply Current	Streaming, 720p 60 fps	I_{AA_PIX}	–	10	15	mA
PLL Supply Current	Streaming, 720p 60f ps	I_{DD_PLL}	–	7	15	mA

19. Operating currents are measured at the following conditions:
   – V_{AA} = V_{AA_PIX} = V_{DD_IO} = V_{DD_PLL} = 2.8 V
   – V_{DD} =1.8 V
   – PLL Enabled and PIXCLK = 74.25 MHz
   – T_A = 25°C
   – C_{LOAD} = 10 pF Measured in dark

Table 22. OPERATING CURRENT CONSUMPTION IN PARALLEL OUTPUT AND HDR MODE

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	Streaming, 1280x960 45 fps	I_{DD1}	–	63	90	mA
Digital Operating Current	Streaming, 1280x960 45 fps	I_{DD}	–	95	115	mA
I/O Digital Operating Current	Streaming, 1280x960 45 fps	I_{DD_IO}	–	35	40	mA
Analog Operating Current	Streaming, 1280x960 45 fps	I_{AA}	–	65	75	mA
Pixel Supply Current	Streaming, 1280x960 45 fps	I_{AA_PIX}	–	15	20	mA
PLL Supply Current	Streaming, 1280x960 45 fps	I_{DD_PLL}	–	7	15	mA
Digital Operating Current	Streaming, 720p 60 fps	I_{DD}	–	95	115	mA
I/O Digital Operating Current	Streaming, 720p 60 fps	I_{DD_IO}	–	35	40	mA
Analog Operating Current	Streaming, 720p 60 fps	I_{AA}	–	61	75	mA
Pixel Supply Current	Streaming, 720p 60 fps	I_{AA_PIX}	–	15	20	mA
PLL Supply Current	Streaming, 720p 60 fps	I_{DD_PLL}	–	7	15	mA

20. Operating currents are measured at the following conditions:
   – V_{AA} = V_{AA_PIX} = V_{DD_IO} = V_{DD_PLL} = 2.8 V
   – V_{DD} =1.8 V
   – PLL Enabled and PIXCLK = 74.25 MHz
   – T_A = 25°C
   – C_{LOAD} = 10 pF Measured in dark

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Table 23. STANDBY CURRENT CONSUMPTION

Definition	Condition	Symbol	Min	Typ	Max	Unit
Hard Standby (Clock Off)	Analog, 2.8 V	–	–	30	100	μA
	Digital, 1.8 V	–	–	85	2500	μA
Hard Standby (Clock On)	Analog, 2.8 V	–	–	30	100	μA
	Digital, 1.8 V	–	–	1.55	4	mA
Soft Standby (Clock Off)	Analog, 2.8 V	–	–	85	100	μA
	Digital, 1.8 V	–	–	85	2500	μA
Soft Standby (Clock On)	Analog, 2.8 V	–	–	30	100	μA
	Digital, 1.8 V	–	–	1.55	4	mA

21. Analog – V_{AA} + V_{AA_PIX} + V_{DD_PLL}
22. Digital – V_{DD} + V_{DD_IO}

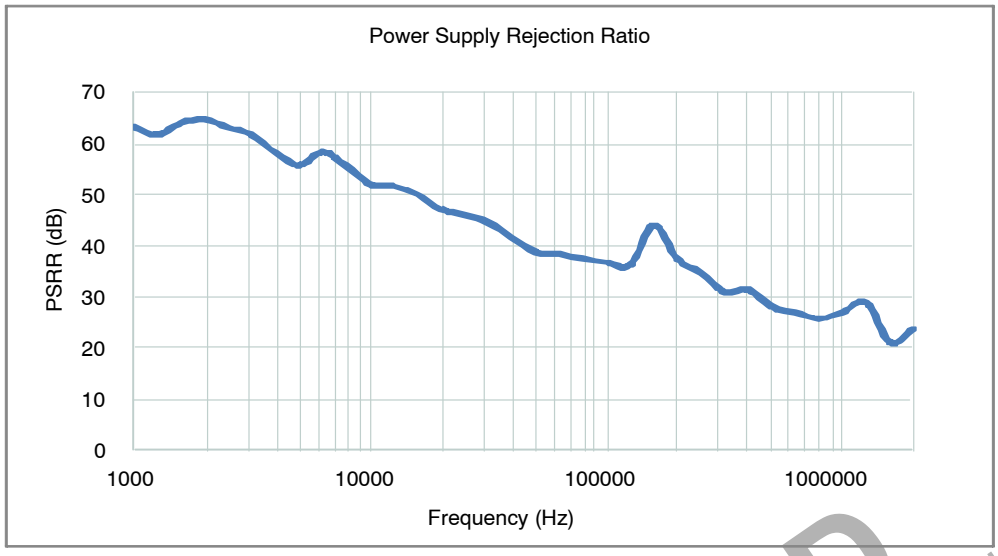


Figure 28. Power Supply Rejection Ratio

POWER−ON RESET AND STANDBY TIMING

Power−Up Sequence

The recommended power−up sequence for the MT9M034 is shown in Figure 29. The available power supplies (VDD_IO, VDD, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Turn on VDD_PLL power supply
2. After 0−10 µs, turn on VAA and VAA_PIX power supply
3. After 0−10 µs, turn on VDD_IO power supply
4. After the last power supply is stable, enable EXTCLK
5. Assert RESET_BAR for at least 1 ms
6. Wait 850000 EXTCLKs (for internal initialization into software standby)
7. Configure PLL, output, and image settings to desired values
8. Wait 1ms for the PLL to lock
9. Set streaming mode (R0x301A[2] = 1)

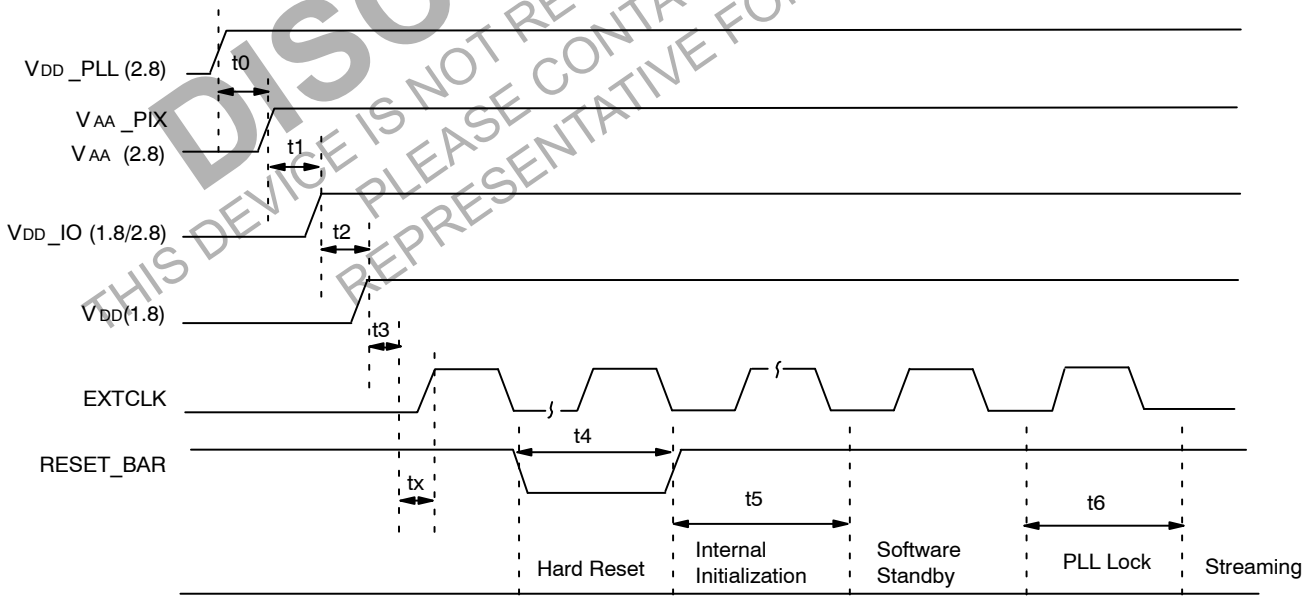


Figure 29. Power Up

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Table 24. POWER−UP SEQUENCE

Definition	Symbol	Min	Typ	Max	Unit
VDD_PLL to VAA/VAA_PIX (Note 25)	t0	0	10	–	µs
VAA/VAA_PIX to VDD_IO	t1	0	10	–	µs
VDD_IO to VDD	t2	0	10	–	µs
Xtal Settle Time	tx	–	30 (Note 23)	–	ms
Hard Reset	t4	1 (Note 24)	–	–	ms
Internal Initialization	t5	850000	–	–	EXTCLKS
PLL Lock Time	t6	1	–	–	ms

23. Xtal settling time is component−dependent, usually taking about 10−100 ms.
24. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
25. It is critical that VDD_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that VDD_PLL is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.

Power−Down Sequence

The recommended power−down sequence for the MT9M034 is shown in Figure 30. The available power supplies (VDD_IO, VDD, VDD_PLL, VAA, VAA_PIX) must have the separation specified below. Power may be removed from all supplies simultaneously, and a sudden loss of power on all rails does not cause damage or affect the lifetime of the device.

1. Disable streaming if output is active by setting standby R0x301A[2] = 0
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended
3. Turn off VDD
4. Turn off VDD_IO
5. Turn off VAA/VAA_PIX
6. Turn off VDD_PLL

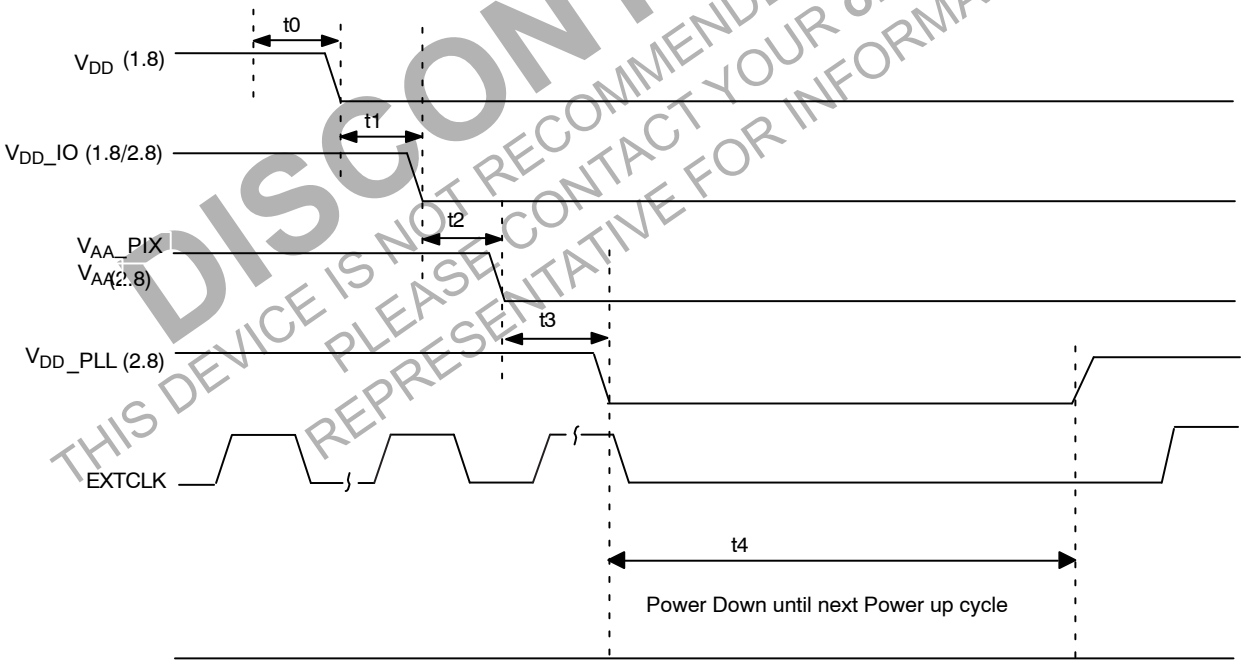


Figure 30. Power Down

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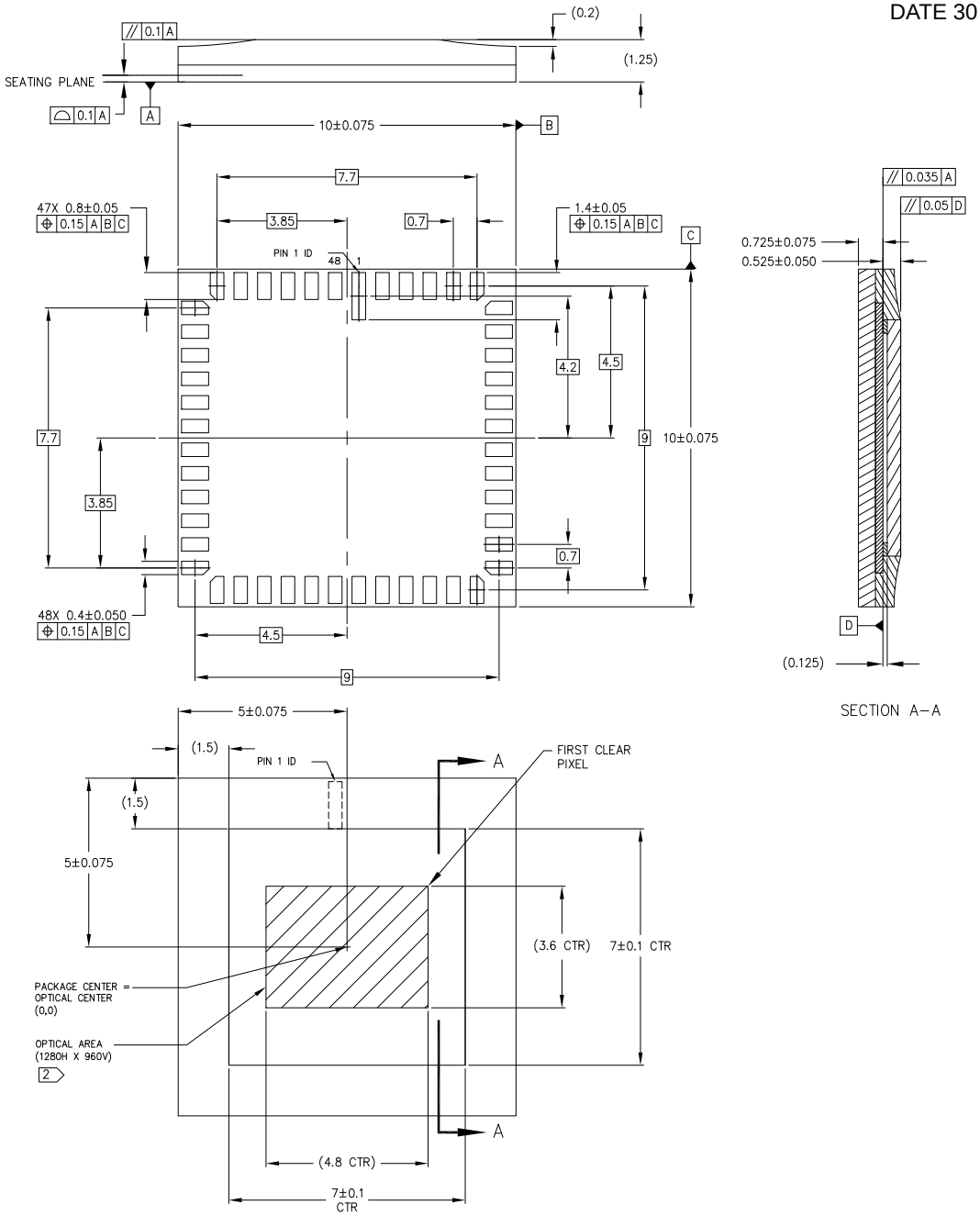
Table 25. POWER−DOWN SEQUENCE

Definition	Symbol	Min	Typ	Max	Unit
VDD to VDD_IO	t1	0	–	–	µs
VDD_IO to VAA/VAA_PIX	t2	0	–	–	µs
VAA/VAA_PIX to VDD_PLL	t3	0	–	–	µs
PwrDn until Next PwrUp Time	t4	100	–	–	ms

26. t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

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NOTES	
1	DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.
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