DAC5652 双路 10 位 275MSPS 数模转换器

1 特性

- 10 位双路发送数模转换器 (DAC)
- 275MSPS 更新速率
- 单电源：3.0V 至 3.6V
- 高无杂散动态范围 (SFDR)：5MHz 时为 80dBc
- 高三阶双音互调 (IMD3)：15.1MHz 和 16.1MHz 时为 78dBc
- 独立或单一电阻器增益控制
- 双路或交错式数据
- 1.2V 片上基准电压
- 低功耗：290mW
- 断电模式：9mW
- 封装：48 引脚薄四方扁平封装 (TQFP)

2 应用

- 蜂窝基站收发信台发射通道
  - CDMA：W-CDMA、CDMA2000、IS-95
  - TDMA：GSM、IS-136、EDGE/UWC-136
- 医疗/测试仪表
- 任意波形发生器 (ARB)
- 直接数字合成 (DDS)
- 线缆调制解调器终端系统 (CMTS)

3 说明

DAC5652 是一款具有片上电压基准的单片、双通道、10 位、高速 DAC。

DAC5652 可在高达 275MSPS 的更新速率下运行，具有卓越的动态性能、严格增益和失调电压匹配特性，因此非常适用于 I/Q 基带或直接 IF 通信应用。

每个 DAC 都具有高阻抗差动电流输出，适用于单端或差动模拟输出配置。外部电阻器允许对每个 DAC 的满量程输出电流进行单独或整体调节，通常使其介于 2mA 至 20mA 之间。精确的片上电压基准具有温度补偿特性，并可提供稳定的 1.2V 基准电压。也可选择使用外部基准。

DAC5652 具有两个 10 位并行输入端口，这两个端口具有单独的时钟和数据锁存器。在灵活性方面，当在交错模式下运行时，DAC5652 还可通过一个端口传输两个 DAC 的多路复用数据。

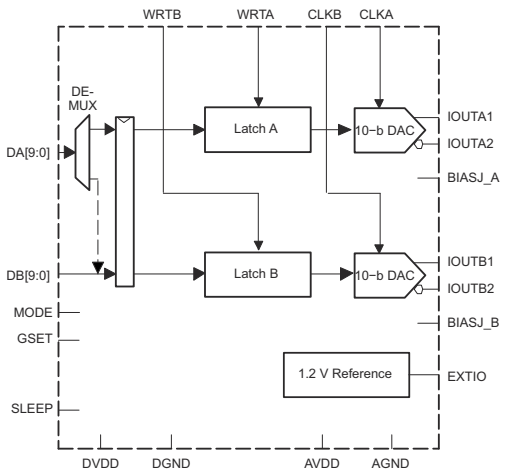
DAC5652 经过特别设计，可在 50Ω 双端接负载情况下提供差动变压器耦合输出。对于 20mA 满量程输出电流，支持 4:1 阻抗比（产生 4dBm 输出功率）和 1:1 阻抗比变压器（–2dBm 输出功率）。

DAC5652 采用 48 引脚 TQFP 封装。产品系列成员间引脚兼容，提供 10 位 (DAC5652)、12 位 (DAC5662) 和 14 位 (DAC5672) 分辨率。此外，DAC5652 还与 DAC2900 和 AD9763 双路 DAC 之间具有引脚兼容性。该器件可在 –40°C 至 85°C 的工业温度范围内运行。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
DAC5652	TQFP	7.00mm x 7.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能模块图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (October 2020) to Revision E (January 2021)	Page
• 更改了“功能方框图”以改善图像质量	1

Changes from Revision C (Decmeber 2010) to Revision D (October 2020)	Page
• 添加了“器件信息”表、“ESD 等级”表、“热阻特性”表、“特性说明”部分、“器件功能模式”、“应用和实施”部分、“电源相关建议”部分、“布局”部分、“器件和文档支持”部分以及“机械、封装和可订购信息”部分	1
• Changed 图 7-1 and 图 7-2 by removing extra wire connecting the gates of the CMOS inverter to the output node	12

Changes from Revision B (March 2005) to Revision C (December 2010)	Page
• Changed the non-printing μ symbols in the Digital Input section of the Electrical Characteristics table (Units column) to the correct μ symbols recognized by the PDF processor	8

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5 Pin Configuration and Functions

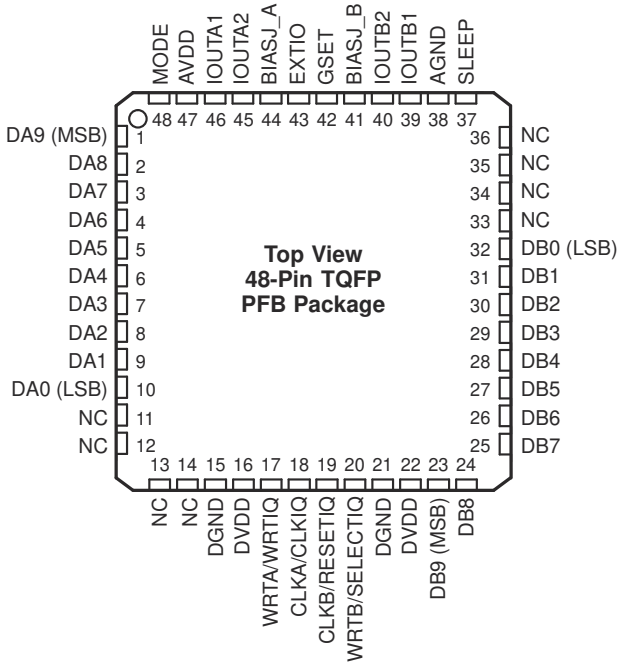


表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	38	I	Analog ground
AVDD	47	I	Analog supply voltage
BIASJ_A	44	O	Full-scale output current bias for DACA
BIASJ_B	41	O	Full-scale output current bias for DACB
CLKA/CLKIQ	18	I	Clock input for DACA, CLKIQ in interleaved mode
CLKB/RESETIQ	19	I	Clock input for DACB, RESETIQ in interleaved mode
DA[9:0]	1-10	I	Data port A. DA9 is MSB and DA0 is LSB. Internal pulldown.
DB[9:0]	23-32	I	Data port B. DB9 is MSB and DB0 is LSB. Internal pulldown.
DGND	15, 21	I	Digital ground
DVDD	16, 22	I	Digital supply voltage
EXTIO	43	I/O	Internal reference output (bypass with 0.1 μF to AGND) or external reference input
GSET	42	I	Gain-setting mode: H – 1 resistor, L – 2 resistors. Internal pullup.
IOUTA1	46	O	DACA current output. Full-scale with all bits of DA high.
IOUTA2	45	O	DACA complementary current output. Full-scale with all bits of DA low.
IOUTB1	39	O	DACB current output. Full-scale with all bits of DB high.
IOUTB2	40	O	DACB complementary current output. Full-scale with all bits of DB low.
MODE	48	I	Mode Select: H – Dual Bus, L – Interleaved. Internal pullup.
NC	11-14, 33-36	-	Factory use only. Pins must be connected to DGND or left unconnected.
SLEEP	37	I	Sleep function control input: H – DAC in power-down mode, L – DAC in operating mode. Internal pulldown.
WRTA/WRTIQ	17	I	Input write signal for PORT A (WRTIQ in interleaving mode)
WRTB/SELECTIQ	20	I	Input write signal for PORT B (SELECTIQ in interleaving mode)

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6 Specifications

6.1 Absolute Maximum Rationgs

over T_A (unless otherwise noted)(1)

		Min	Max	UNIT
Supply voltage range	AVDD(2)	–0.5	4	V
	DVDD(3)	–0.5	4	V
Voltage between AGND and DGND		–0.5	0.5	V
Voltage between AVDD and DVDD		–0.5	0.5	V
Supply voltage range	DA[9:0] and DB[9:0](3)	–0.5	DVDD + 0.5	V
	MODE, SLEEP, CLKA, CLKB, WRTA, WRTB(3)	–0.5	DVDD + 0.5	V
	IOUTA1, IOUTA2, IOUTB1, IOUTB2(2)	–1	AVDD + 0.5	V
	EXTIO, BIASJ_A, BIASJ_B, GSET(2)	–0.5	AVDD + 0.5	V
Peak input current (any input)			+20	mA
Peak total input current (all inputs)			–30	mA
Operating free-air temperature range		–40	85	°C
Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND.
(3) Measured with respect to DGND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

over operating free-air temperature range (unless otherwise noted)

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage	3	3.3	3.6	V
DVDD	Digital supply voltage	3	3.3	3.6	V
	Output voltage compliance range(1)	-1		1.25	V
	Clock input frequency			275	MHz
T_A	Operating free-air temperature	-40		85	°C

1. The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5652 device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.

6.4 Thermal Resistance Characteristics

THERMAL METRIC(1)		DAC5652 TQFP (PFB) 48-Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.3	°C/W

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6.4 Thermal Resistance Characteristics (continued)

THERMAL METRIC(1)		DAC5652 TQFP (PFB) 48-Pins	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, independent gain set mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Specifications						
	Resolution		10			Bits
DC Accuracy(1)						
INL	Integral nonlinearity	1 LSB = $I_{OUTFS}/2^{10}$, T_{MIN} to T_{MAX}	–1	±0.25	1	LSB
DNL	Differential nonlinearity		–0.5	±0.16	0.5	LSB
Analog Output						
	Offset error	Midscale value (internal reference)		±0.05		%FSR
	Offset mismatch	Midscale value (internal reference)		±0.03		%FSR
	Gain error	With internal reference		±0.75		%FSR
	Minimum full-scale output current(2)			2		mA
	Maximum full-scale output current(2)			20		mA
	Gain mismatch	With internal reference	–2	0.2	2	%FSR
	Output voltage compliance range(3)		–1		1.25	V
R_O	Output resistance			300		kΩ
C_O	Output capacitance			5		pF
Reference Output						
	Reference voltage		1.14	1.2	1.26	V
	Reference output current(4)			100		nA
Reference Input						
V_{EXTIO}	Input voltage		0.1		1.25	V
R_I	Input resistance			1		MΩ
	Small signal bandwidth			300		kHz
C_I	Input capacitance			100		pF
Temperature Coefficients						
	Offset drift			2		ppm of FSR/°C
	Gain drift	With external reference		±20		ppm of FSR/°C
		With internal reference		±40		ppm of FSR/°C
	Reference voltage drift			±20		ppm/°C

(1) Measured differentially through 50 Ω to AGND.
(2) Nominal full-scale current, I_{OUTFS}, equals 32x the I_{BIAS} current.

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(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5652 device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.
(4) Use an external buffer amplifier with high-impedance input to drive any external load.

6.6 Electrical Characteristics

over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, f_{DATA} = 200 MSPS, f_{OUT} = 1 MHz, independent gain set mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
AVDD	Analog supply voltage		3	3.3	3.6	V
DVDD	Digital supply voltage		3	3.3	3.6	V
I_{AVDD}	Supply current, analog	Including output current through load resistor		75	90	mA
		Sleep mode with clock		2.5		
		Sleep mode without clock		2.5		
I_{DVDD}	Supply current, digital			12	20	mA
		Sleep mode with clock		11.3	18	
		Sleep mode without clock		0.6		
	Power dissipation			290	360	mW
		Sleep mode with clock		45.5		
		Sleep mode without clock		9.2		
		f_{DATA} = 275 MSPS, f_{OUT} = 20 MHz		310		
APSRR	Analog power supply rejection ratio		– 0.2	– 0.01	0.2	%FSR/V
DPSRR	Digital power supply rejection ratio		– 0.2	0	0.2	%FSR/V
T_A	Operating free-air temperature		– 40		85	°C

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6.7 Electrical Characteristics, AC

AC specifications over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, independent gain set mode, differential 1:1 impedance ratio transformer coupled output, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Output						
f_{clk}	Maximum output update rate[1]		275			MSPS
t_s	Output settling time to 0.1% (DAC)	Mid-scale transition		20		ns
t_r	Output rise time 10% to 90% (OUT)			1.4		ns
t_f	Output fall time 90% to 10% (OUT)			1.5		ns
	Output noise	I_{OUTFS} = 20 mA		55		pA/ √ Hz
		I_{OUTFS} = 2 mA		30		
AC Linearity						
SFDR	Spurious-free dynamic range	1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = 0 dB		79		dBc
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = – 6 dB		78		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, I_{OUTFS} = – 12 dB		73		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz, I_{OUTFS} = 0 dB		80		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB		76		
		1st Nyquist zone, T_{MIN} to T_{MAX}, f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB	61	70		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 41 MHz, I_{OUTFS} = 0 dB		67		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 275 MSPS, f_{OUT} = 20 MHz		70		
SNR	Signal-to-noise ratio	1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz, I_{OUTFS} = 0 dB		63		dB
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 160 MSPS, f_{OUT} = 20 MHz, I_{OUTFS} = 0 dB		62		dB
IMD3	Third-order two-tone intermodulation	Each tone at – 6 dBFS, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 45.4 MHz and 46.4 MHz		61		dBc
		Each tone at – 6 dBFS, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 15.1 MHz and 16.1 MHz		78		
IMD	Four-tone intermodulation	Each tone at – 12 dBFS, T_A = 25°C f_{DATA} = 100 MSPS, f_{OUT} = 15.6, 15.8, 16.2, and 16.4 MHz		76		dBc
		Each tone at – 12 dBFS, T_A = 25°C f_{DATA} = 165 MSPS, f_{OUT} = 19.0, 19.1, 19.3, and 19.4 MHz		55		
		Each tone at – 12 dBFS, T_A = 25°C f_{DATA} = 165 MSPS, f_{OUT} = 68.8, 69.6, 71.2, and 72.0 MHz		70		
	Channel isolation	T_A = 25°C, f_{DATA} = 165 MSPS f_{OUT} (CH1) = 20 MHz, f_{OUT} (CH2) = 21 MHz		90		dBc

(1) Specified by design and bench characterization. Not production tested.

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6.8 Electrical Characteristics, DC

Digital specifications over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input						
V_{IH}	High-level input voltage		2		3.3	V
V_{IL}	Low-level input voltage		0		0.8	V
I_{IH}	High-level input current			±50		µA
I_{IL}	Low-level input current			±10		µA
$I_{IH(GSET)}$	High-level input current, GSET pin			7		µA
$I_{IL(GSET)}$	Low-level input current, GSET pin			–80		µA
$I_{IH(MODE)}$	High-level input current, MODE pin			–30		µA
$I_{IL(MODE)}$	Low-level input current, MODE pin			–80		µA
C_I	Input capacitance			5		pF

6.9 Switching Characteristics

Digital specifications over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timing - Dual Bus Mode						
t_{su}	Input setup time		1			ns
t_h	Input hold time		1			ns
t_{LPH}	Input clock pulse high time			1		ns
t_{LAT}	Clock latency (WRTA/B to outputs)		4		4	clk
t_{PD}	Propagation delay time			1.5		ns
Timing - Single Bus Interleaved Mode						
t_{su}	Input setup time			0.5		ns
t_h	Input hold time			0.5		ns
t_{LAT}	Clock latency (WRTA/B to outputs)		4		4	clk
t_{PD}	Propagation delay time			1.5		ns

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6.10 Typical Characteristics

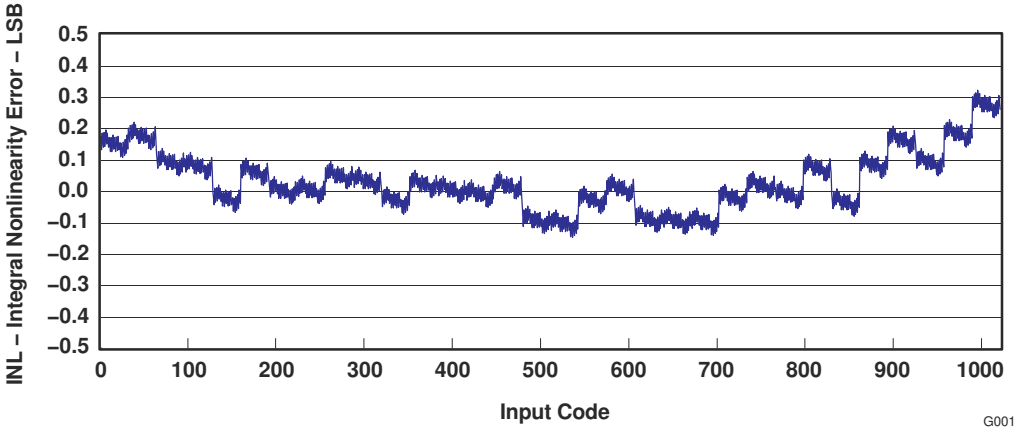


图 6-1. Integral Nonlinearity vs Input Code

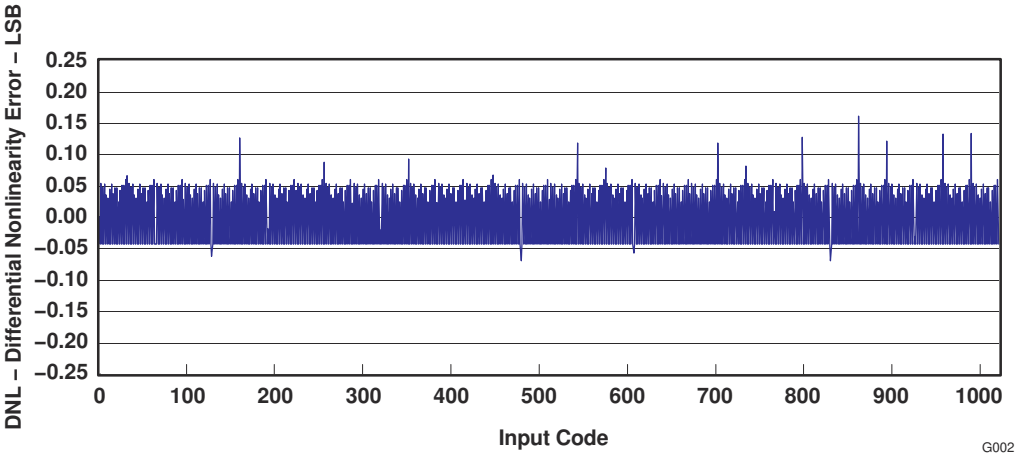


图 6-2. Differential Nonlinearity vs Input Code

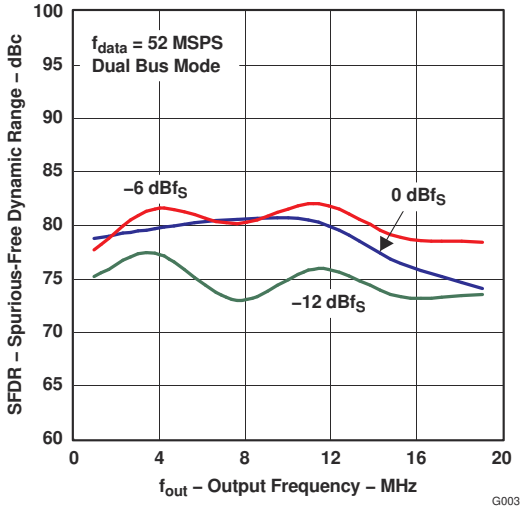


图 6-3. Spurious-Free Dynamic Range vs Output Frequency

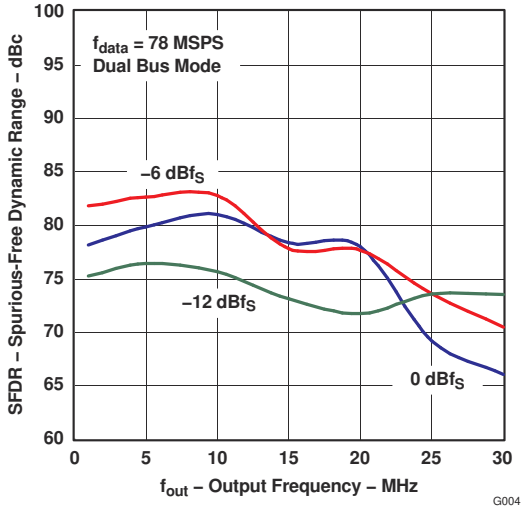


图 6-4. Spurious-Free Dynamic Range vs Output Frequency

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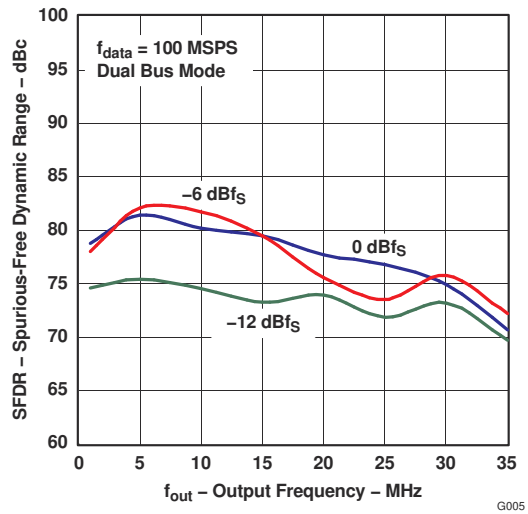


图 6-5. Spurious-Free Dynamic Range vs Output Frequency

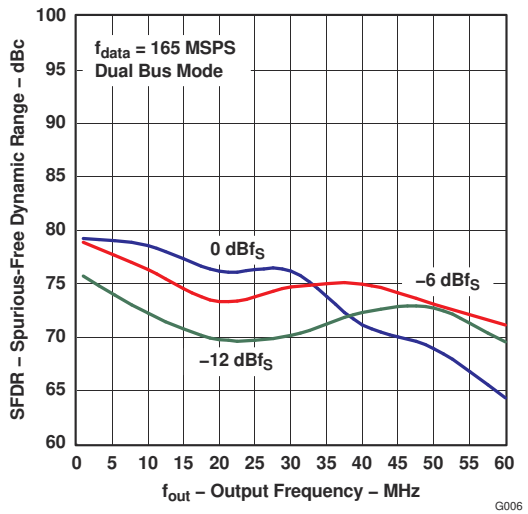


图 6-6. Spurious-Free Dynamic Range vs Output Frequency

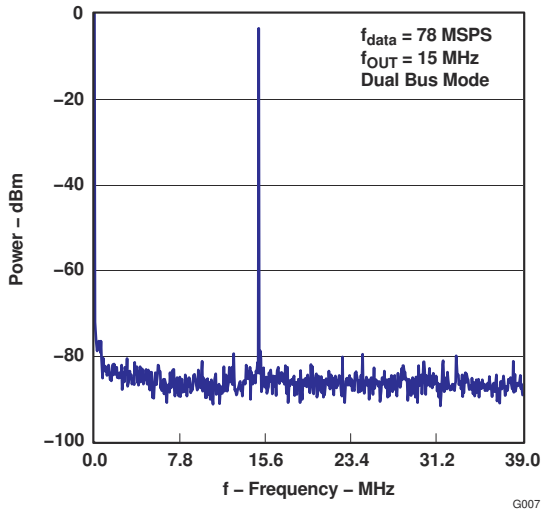


图 6-7. Single-Tone Spectrum

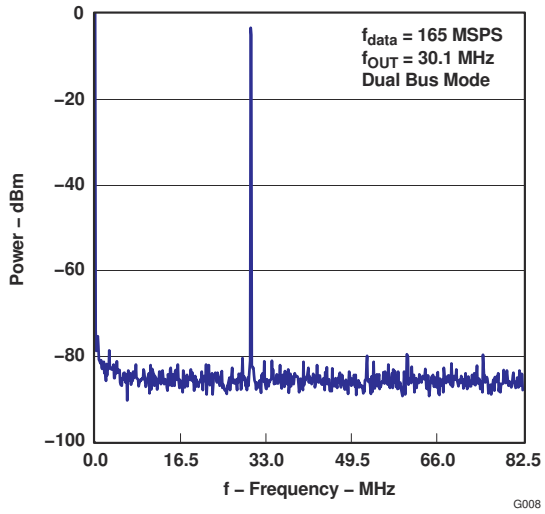


图 6-8. Single-Tone Spectrum

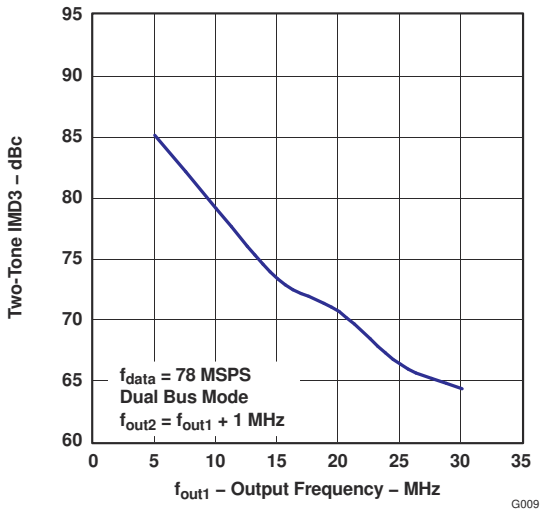


图 6-9. Two-Tone IMD3 vs Output Frequency

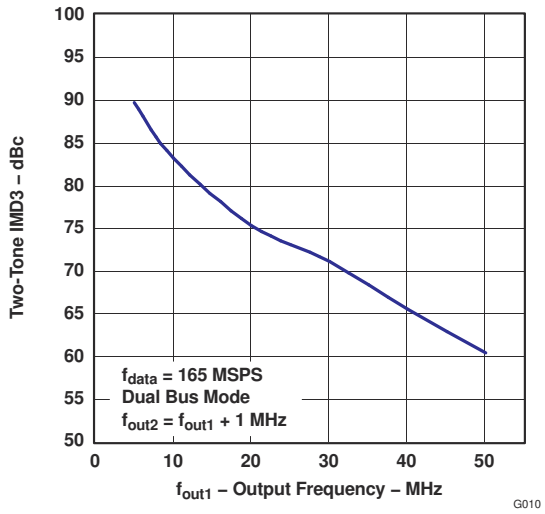


图 6-10. Two-Tone IMD3 vs Output Frequency

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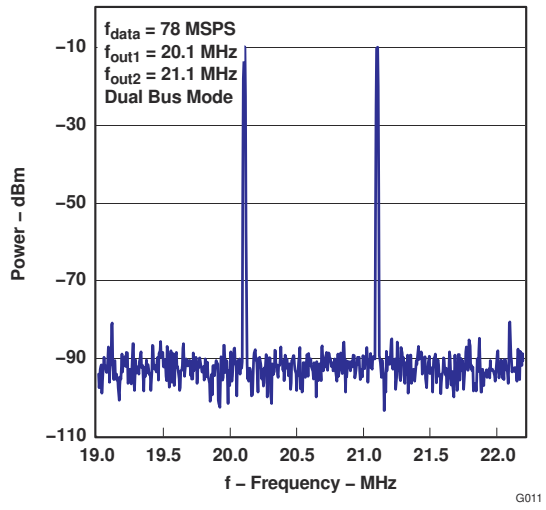


图 6-11. Two-Tone Spectrum

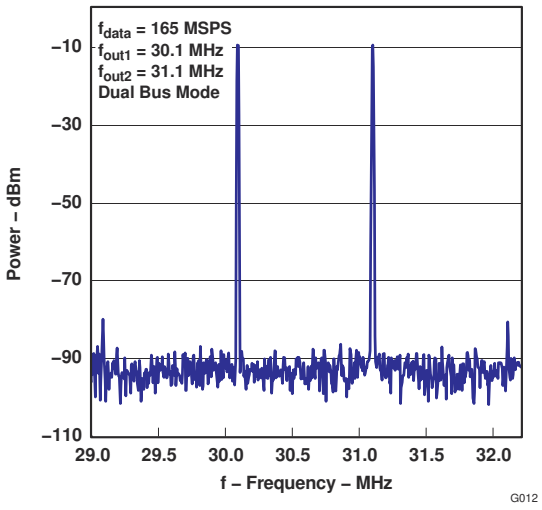


图 6-12. Two-Tone Spectrum

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7 Parameter Measurement Information

7.1 Digital Inputs and Timing

7.1.1 Digital Inputs

The data input ports of the DAC5652 accept a standard positive coding with data bits DA9 and DB9 being the most significant bits (MSB). The converter outputs support a clock rate of up to 275 MSPS. The best performance is typically achieved with a symmetric duty cycle for write and clock; however, the duty cycle may vary as long as the timing specifications are met. Similarly, the setup and hold times may be chosen within their specified limits.

All digital inputs of the DAC5652 are CMOS compatible. 图 7-1 and 图 7-2 show schematics of the equivalent CMOS digital inputs of the DAC5652. The pullup and pulldown circuitry is approximately equivalent to 100kΩ.The 10-bit digital data input follows the offset positive binary coding scheme. The DAC5652 is designed to operate with a digital supply (DVDD) of 3 V to 3.6 V.

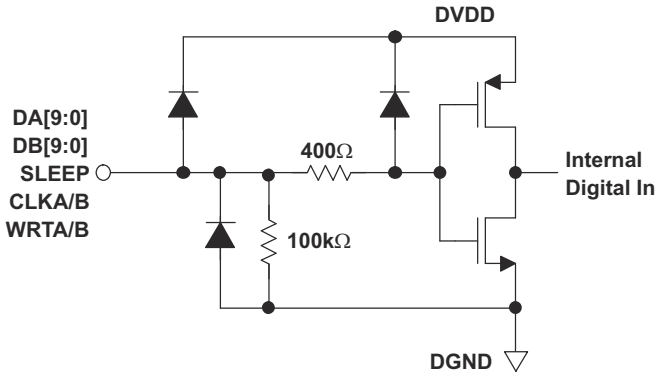


图 7-1. CMOS/TTL Digital Equivalent Input With Internal Pulldown Resistor

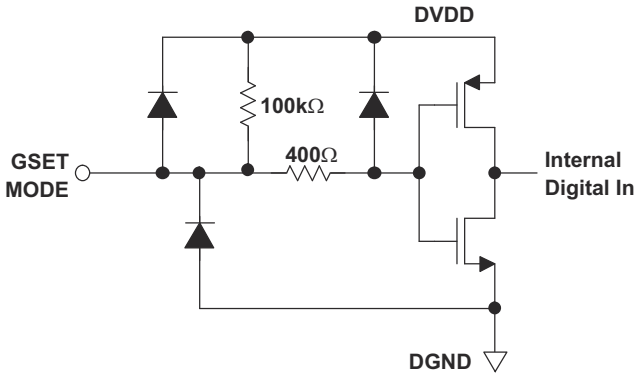


图 7-2. CMOS/TTL Digital Equivalent Input With Internal Pullup Resistor

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7.1.2 Input Interfaces

The DAC5652 features two operating modes selected by the MODE pin, as shown in 表 7-1.

- For dual-bus input mode, the device essentially consists of two separate DACs. Each DAC has its own separate data input bus, clock input, and data write signal (data latch-in).
- In single-bus interleaved mode, the data must be presented interleaved at the A-channel input bus. The B-channel input bus is not used in this mode. The clock and write input are now shared by both DACs.

表 7-1. Operating Modes

MODE Pin	MODE pin connected to DGND	MODE pin connected to DVDD
Bus input	Single-bus interleaved mode, clock and write input equal for both DACs	Dual-bus mode, DACs operate independently

7.1.3 Dual-Bus Data Interface and Timing

In dual-bus mode, the MODE pin is connected to DVDD. The two converter channels within the DAC5652 consist of two independent, 10-bit, parallel data ports. Each DAC channel is controlled by its own set of write (WRTA, WRTB) and clock (CLKA, CLKB) lines. The WRTA/B lines control the channel input latches and the CLKA/B lines control the DAC latches. The data is first loaded into the input latch by a rising edge of the WRTA/B line.

The internal data transfer requires a correct sequence of write and clock inputs, since essentially two clock domains having equal periods (but possibly different phases) are input to the DAC5652. This is defined by a minimum requirement of the time between the rising edge of the clock and the rising edge of the write inputs. This essentially implies that the rising edge of CLKA/B must occur at the same time or before the rising edge of the WRTA/B signal. A minimum delay of 2 ns must be maintained if the rising edge of the clock occurs after the rising edge of the write. Note that these conditions are satisfied when the clock and write inputs are connected externally. Note that all specifications were measured with the WRTA/B and CLKA/B lines connected together.

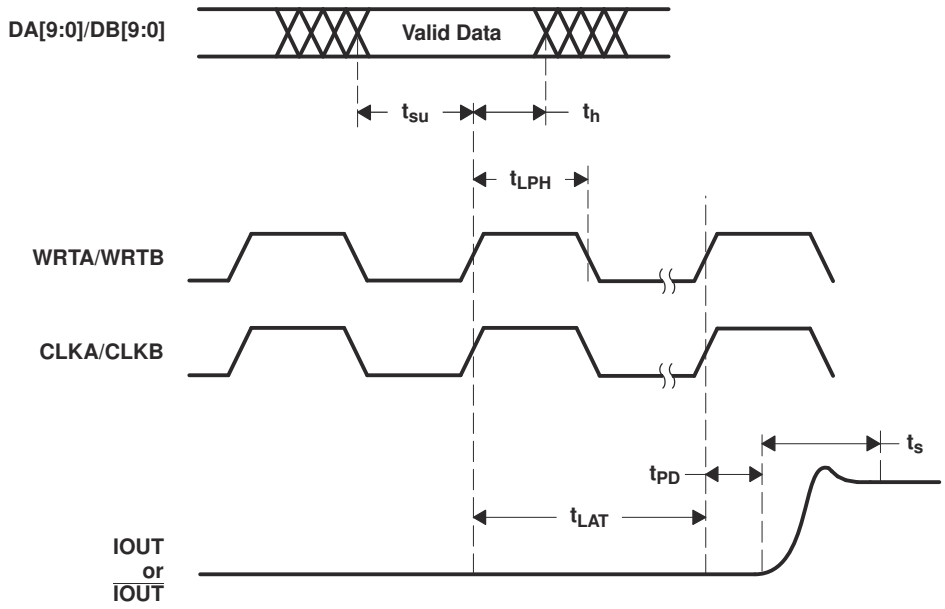


图 7-3. Dual-Bus Mode Operation

7.1.4 Single-Bus Interleaved Data Interface and Timing

In single-bus interleaved mode, the MODE pin is connected to DGND. 图 7-4 shows the timing diagram. In interleaved mode, the A- and B-channels share the write input (WRTIQ) and update clock (CLKIQ and internal CLKDACIQ). Multiplexing logic directs the input word at the A-channel input bus to either the A-channel input latch (SELECTIQ is high) or to the B-channel input latch (SELECTIQ is low). When SELECTIQ is high, the data value in the B-channel latch is retained by presenting the latch output data to its input again. When SELECTIQ is low, the data value in the A-channel latch is retained by presenting the latch output data to its input.

In interleaved mode, the A-channel input data rate is twice the update rate of the DAC core. As in dual-bus mode, it is important to maintain a correct sequence of write and clock inputs. The edge-triggered flip-flops latch the A- and B-channel input words on the rising edge of the write input (WRTIQ). This data is presented to the A- and B-DAC latches on the following falling edge of the write inputs. The DAC5652 clock input is divided by a factor of two before it is presented to the DAC latches.

Correct pairing of the A- and B-channel data is done by RESETIQ. In interleaved mode, the clock input CLKIQ is divided by two, which would translate to a non-deterministic relation between the rising edges of the CLKIQ and CLKDACIQ. RESETIQ ensures, however, that the correct position of the rising edge of CLKDACIQ with respect to the data at the input of the DAC latch is determined. CLKDACIQ is disabled (low) when RESETIQ is high.

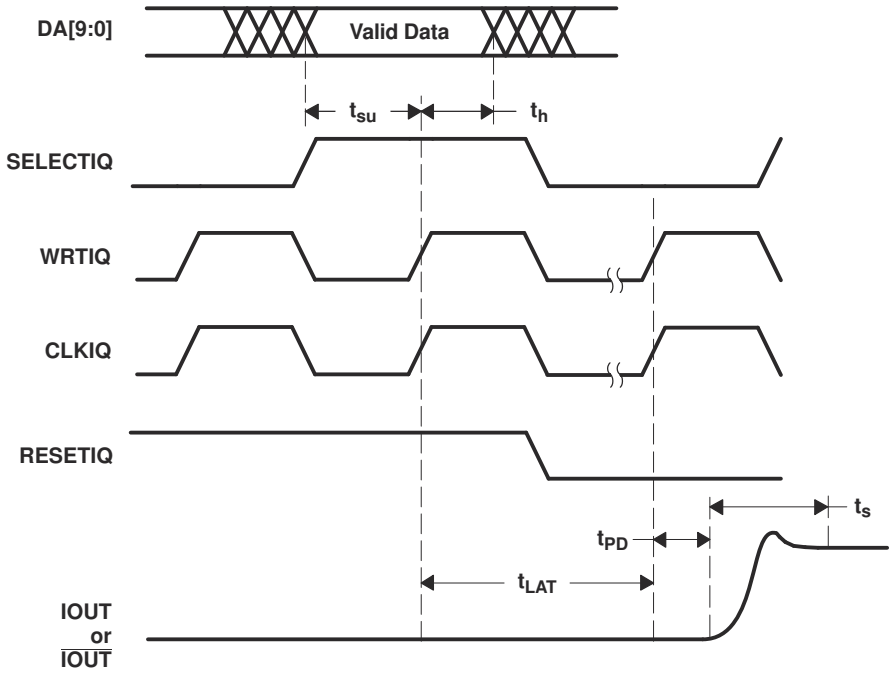


图 7-4. Single-Bus Interleaved Mode Operation

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8 Detailed Description

8.1 Overview

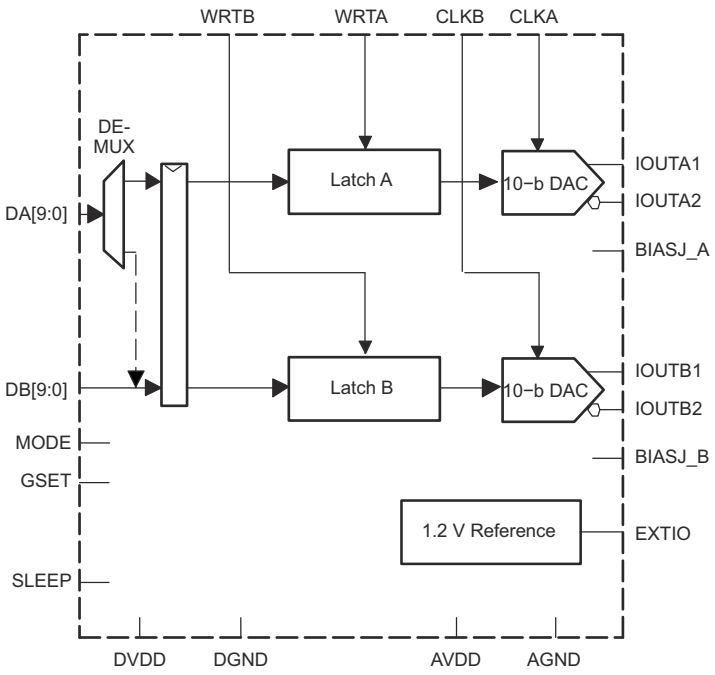
The architecture of the DAC5652 uses a current steering technique to enable fast switching and high update rate. The core element within the monolithic DAC is an array of segmented current sources that are designed to deliver a full-scale output current of up to 20 mA. An internal decoder addresses the differential current switches each time the DAC is updated and a corresponding output current is formed by steering all currents to either output summing node, IOUT1 or IOUT2. The complementary outputs deliver a differential output signal, which improves the dynamic performance through reduction of even-order harmonics, common-mode signals (noise), and double the peak-to-peak output signal swing by a factor of two, as compared to single-ended operation.

The segmented architecture results in a significant reduction of the glitch energy and improves the dynamic performance (SFDR) and DNL. The current outputs maintain a very high output impedance of greater than 300 kΩ.

When pin 42 (GSET) is high (simultaneous gain set mode), the full-scale output current for both DACs is determined by the ratio of the internal reference voltage (1.2 V) and an external resistor (R_{SET}) connected to BIASJ_A. When GSET is low (independent gain set mode), the full-scale output current for each DAC is determined by the ratio of the internal reference voltage (1.2 V) and separate external resistors (R_{SET}) connected to BIASJ_A and BIASJ_B. The resulting I_{REF} is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 2 mA to 20 mA, depending on the value of R_{SET}.

The DAC5652 is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section comprises both the current source array with its associated switches, and the reference circuitry.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Transfer Function

Each of the DACs in the DAC5652 has a set of complementary current outputs, I_{OUT1} and I_{OUT2}. The full-scale output current, I_{OUTFS}, is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT1} + I_{OUT2} \quad (1)$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT1} = I_{OUTFS} \times \left(\frac{Code}{1024}\right) \quad (2)$$

$$I_{OUT2} = I_{OUTFS} \times \left(\frac{1023 - Code}{1024}\right) \quad (3)$$

where Code is the decimal representation of the DAC data input word. Additionally, I_{OUTFS} is a function of the reference current I_{REF}, which is determined by the reference voltage and the external setting resistor (R_{SET}).

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (4)$$

In most cases, the complementary outputs drive resistive loads or a terminated transformer. A signal voltage develops at each output according to:

$$V_{OUT1} = I_{OUT1} \times R_{LOAD} \quad (5)$$

$$V_{OUT2} = I_{OUT2} \times R_{LOAD} \quad (6)$$

The value of the load resistance is limited by the output compliance specification of the DAC5652. To maintain specified linearity performance, the voltage for I_{OUT1} and I_{OUT2} must not exceed the maximum allowable compliance range.

The total differential output voltage is:

$$V_{OUTDIFF} = V_{OUT1} - V_{OUT2} \quad (7)$$

$$V_{OUTDIFF} = \frac{(2 \times Code - 1023)}{1024} \times I_{OUTFS} \times R_{LOAD} \quad (8)$$

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8.3.2 Analog Outputs

The DAC5652 provides two complementary current outputs, I_{OUT1} and I_{OUT2}. The simplified circuit of the analog output stage representing the differential topology is shown in 图 8-1. The output impedance of I_{OUT1} and I_{OUT2} results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

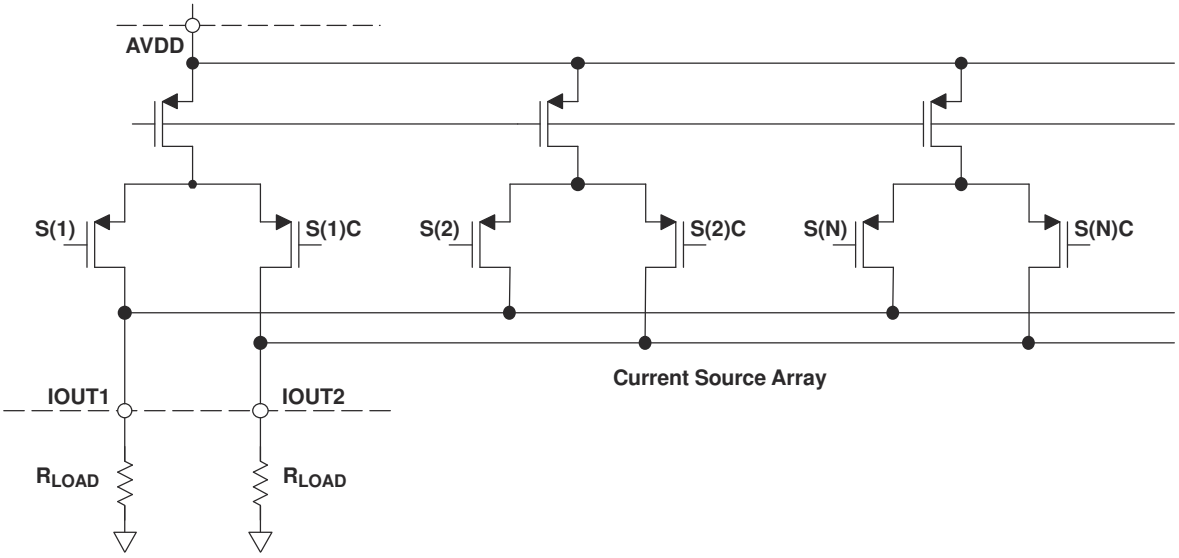


图 8-1. Analog Outputs

The signal voltage swing that may develop at the two outputs, I_{OUT1} and I_{OUT2}, is limited by a negative and positive compliance. The negative limit of –1 V is given by the breakdown voltage of the CMOS process and exceeding it compromises the reliability of the DAC5652 (or even causes permanent damage). With the full-scale output set to 20 mA, the positive compliance equals 1.2 V. Note that the compliance range decreases to about
1 V for a selected output current of I_{OUTFS} = 2 mA. Care must be taken that the configuration of DAC5652 does not exceed the compliance range to avoid degradation of the distortion performance and integral linearity.

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately 0.5 V_{PP}. This is the case for a 50-Ω doubly-terminated load and a 20-mA full-scale output current. A variety of loads can be adapted to the output of the DAC5652 by selecting a suitable transformer while maintaining optimum voltage levels at I_{OUT1} and I_{OUT2}. Furthermore, using the differential output configuration in combination with a transformer is instrumental for achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of 20 mA. A lower full-scale range of 2 mA may be considered for applications that require low power consumption, but can tolerate a slight reduction in performance level.

8.3.3 Output Configurations

The current outputs of the DAC5652 allow for a variety of configurations. As mentioned previously, utilizing the converter’s differential outputs yield the best dynamic performance. Such a differential output circuit may consist of an RF transformer or a differential amplifier configuration. The transformer configuration is ideal for most applications with ac coupling, while op amps are suitable for a dc-coupled configuration.

The single-ended configuration may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground converts the output current into a ground-referenced voltage signal. To improve on the dc linearity by maintaining a virtual ground, an I-to-V or op-amp configuration may be considered.

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8.3.4 Differential With Transformer

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance. The appropriate transformer must be carefully selected based on the output frequency spectrum and impedance requirements.

The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio) the transformer can provide optimum impedance matching while controlling the compliance voltage for the converter outputs.

图 8-2 and 图 8-3 show 50-Ω doubly-terminated transformer configurations with 1:1 and 4:1 impedance ratios, respectively. Note that the center tap of the primary input of the transformer has to be grounded to enable a dc-current flow. Applying a 20-mA full-scale output current would lead to a 0.5-V_{PP} output for a 1:1 transformer and a 1-V_{PP} output for a 4:1 transformer. In general, the 1:1 transformer configuration will have slightly better output distortion, but the 4:1 transformer will have 6 dB higher output power.

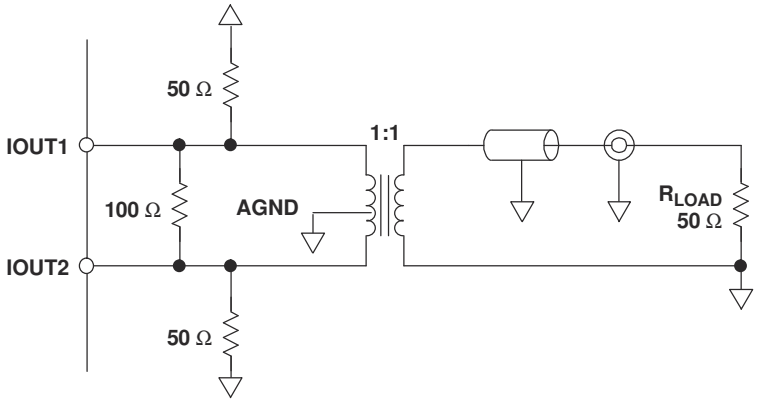


图 8-2. Driving a Doubly-Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

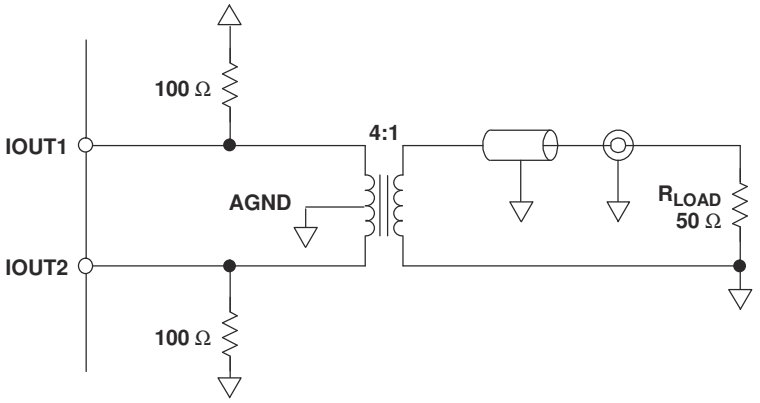


图 8-3. Driving a Doubly-Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

8.3.5 Single-Ended Configuration

图 8-4 shows the single-ended output configuration, where the output current I_{OUT1} flows into an equivalent load resistance of 25 Ω. Node IOUT2 must be connected to AGND or terminated with a resistor of 25 Ω to AGND. The nominal resistor load of 25 Ω gives a differential output swing of 1 V_{PP} when applying a 20-mA full-scale output current.

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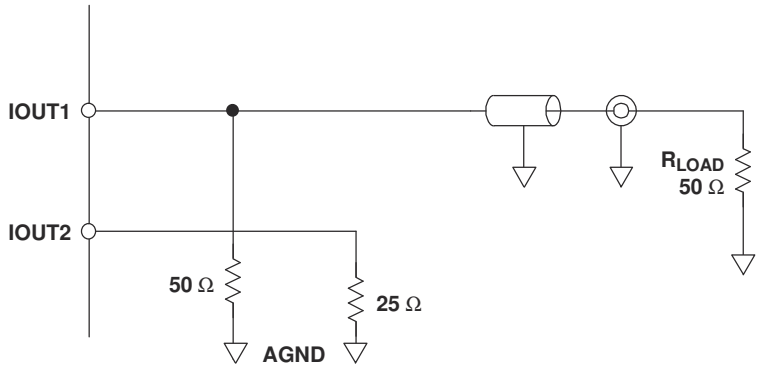


图 8-4. Driving a Doubly-Terminated 50-Ω Cable Using a Single-Ended Output

8.3.6 Reference Operation

8.3.6.1 Internal Reference

The DAC5652 has an on-chip reference circuit which comprises a 1.2-V bandgap reference and two control amplifiers, one for each DAC. The full-scale output current, I_{OUTFS}, of the DAC5652 is determined by the reference voltage, V_{REF}, and the value of resistor R_{SET}. I_{OUTFS} can be calculated by:

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \tag{9}$$

The reference control amplifier operates as a V-to-I converter producing a reference current, I_{REF}, which is determined by the ratio of V_{REF} and R_{SET} (see 方程式 9). The full-scale output current, I_{OUTFS}, results from multiplying I_{REF} by a fixed factor of 32.

Using the internal reference, a 2-kΩ resistor value results in a full-scale output of approximately 20 mA. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the output current can be adjusted from 20 mA down to 2 mA. Operating the DAC5652 at lower than 20-mA output currents may be desirable for reasons of reducing the total power consumption, improving the distortion performance, or observing the output compliance voltage limitations for a given load condition.

It is recommended to bypass the EXTIO pin with a ceramic chip capacitor of 0.1 µF or more. The control amplifier is internally compensated and its small signal bandwidth is approximately 300 kHz.

8.3.6.2 External Reference

The internal reference can be disabled by simply applying an external reference voltage into the EXTIO pin, which in this case functions as an input. The use of an external reference may be considered for applications that require higher accuracy and drift performance or to add the ability of dynamic gain control.

While a 0.1-µF capacitor is recommended to be used with the internal reference, it is optional for the external reference operation. The reference input, EXTIO, has a high input impedance (1 MΩ) and can easily be driven by various sources. Note that the voltage range of the external reference must stay within the compliance range of the reference input.

8.3.7 Gain Setting Option

The full-scale output current on the DAC5652 can be set two ways: either for each of the two DAC channels independently or for both channels simultaneously. For the independent gain set mode, the GSET pin (pin 42) must be low (that is, connected to AGND). In this mode, two external resistors are required — one R_{SET} connected to the BIASJ_A pin (pin 44) and the other to the BIASJ_B pin (pin 41). In this configuration, the user has the flexibility to set and adjust the full-scale output current for each DAC independently, allowing for the compensation of possible gain mismatches elsewhere within the transmit signal path.

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Alternatively, bringing the GSET pin high (that is, connected to AVDD), the DAC5652 switches into the simultaneous gain set mode. Now the full-scale output current of both DAC channels is determined by only one external R_{SET} resistor connected to the BIASJ_A pin. The resistor at the BIASJ_B pin may be removed; however, this is not required since this pin is not functional in this mode and the resistor has no effect on the gain equation.

8.4 Device Functional Modes

8.4.1 Sleep Mode

The DAC5652 features a power-down function which can reduce the total supply current to approximately 3.1 mA over the specified supply range if no clock is present. Applying a logic high to the SLEEP pin initiates the power-down mode, while a logic low enables normal operation. When left unconnected, an internal active pulldown circuit enables the normal operation of the converter.

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9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Informmation

The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5652 device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.

9.2 Typical Application

A typical application for the DAC5652 is a dual- or single-carrier transmitter. The DAC is provided with some input digital baseband signal, and outputs an analog carrier. A design example for a single-carrier transmitter is described in this section.

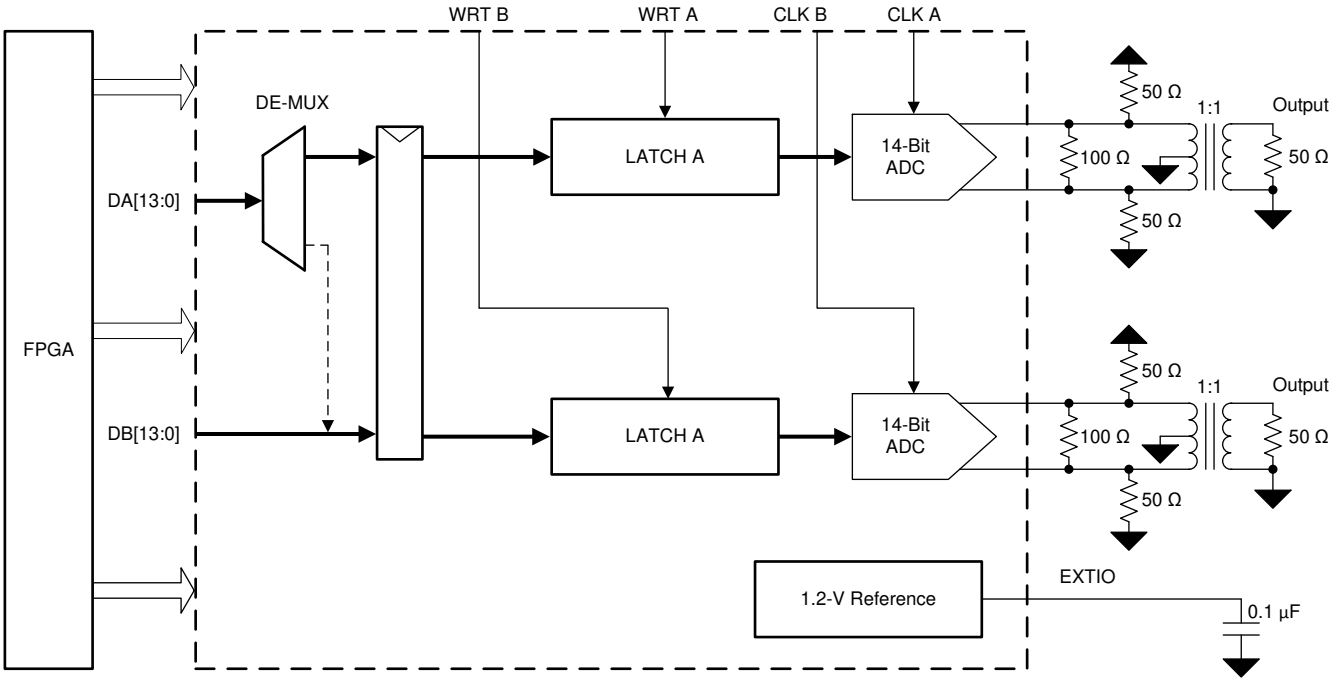


图 9-1. Single-Carrier Transmitter

9.2.1 Design Requirements

The requirements for this design are to generate a single WCDMA signal at an intermediate frequency of 30.72 MHz. The ACLR needs to be better than 72 dBc.

表 9-1. Design Parameters

FEATURE	SPECIFICATION
Number of carriers	1
AVDD and DVDD	3.3 V
Clock rate	122.88 MSPS

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表 9-1. Design Parameters (continued)

FEATURE	SPECIFICATION
Input data	WCDMA with IF at 30.72 MHz
ACPR	> 72 dB

9.2.2 Detailed Design Procedure

The single WCDMA carrier signal with an intermediate frequency (IF) of 30.72 MHz must be created in the digital processor at a sample rate of 122.88 MSPS for the DAC. These 10-bit samples are placed on the 10-bit CMOS input port of the DAC.

A CMOS DAC clock must be generated from a clock source at 122.88 MHz. This clock must be provided to the CLK pin of the DAC. The IOUTA and IOUTB differential connections must be connected to a transformer in order to provide a single-ended output. A typical 1:1 impedance transformer is used on the device EVM. The DAC5672A evaluation module (EVM) provides a good reference for this design example.

9.2.3 Application Performance Plots

This spectrum analyzer plot shows the adjacent channel power ratio (ACPR) for the transformeroutput, single-carrier signal with an intermediate frequency of 30.72 MHz. The results meet the system requirements for a minimum of 72 dBc ACPR.

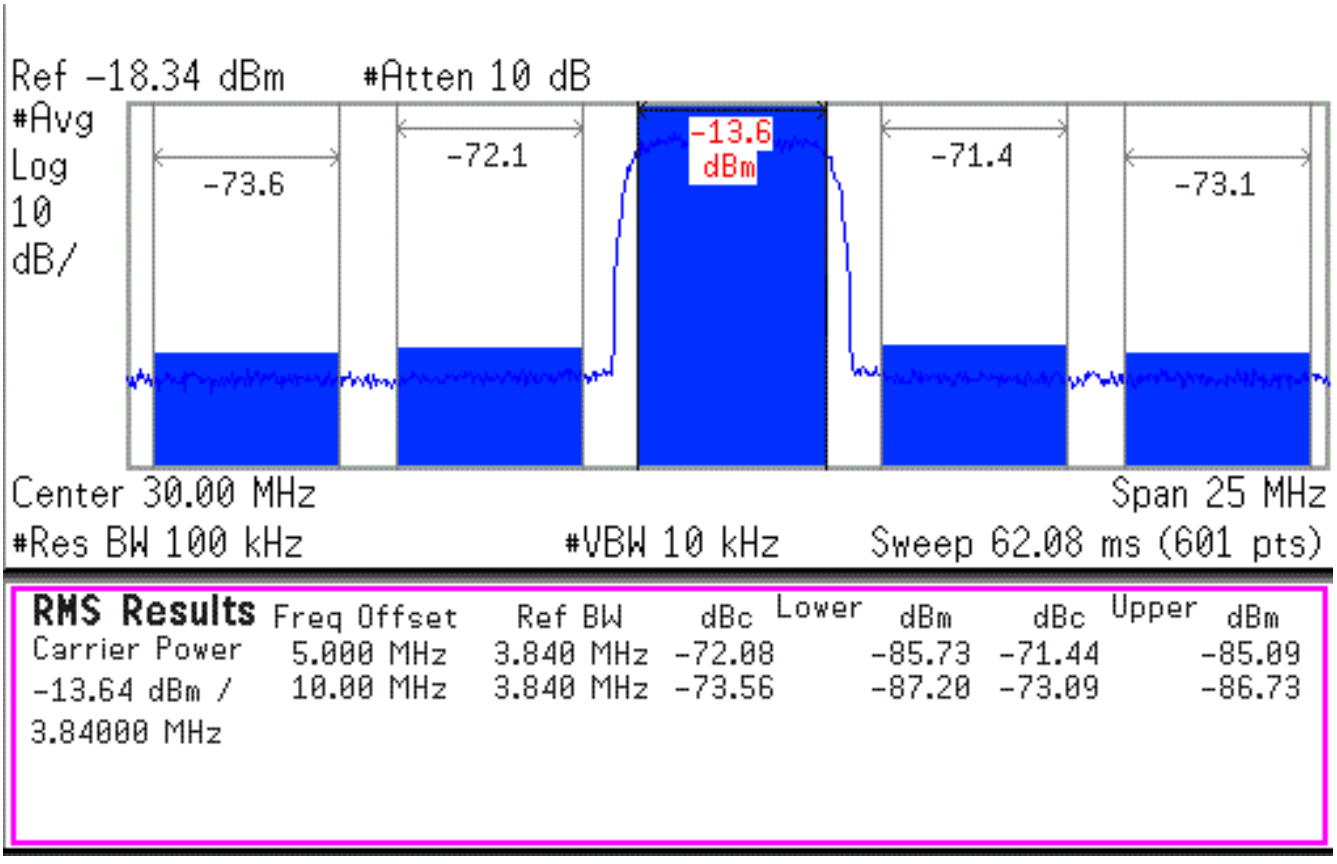


图 9-2. ACPR Performance

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10 Power Supply Recommendations

Power the device with the nominal supply voltages as indicated in the Recommended Operating Conditions.

In most instances, the best performance is achieved with LDO supplies. However, the supplies may be driven with direct outputs from a DC/DC switcher, as long as the noise performance of the switcher is acceptable.

For best performance:

- Use at least two power layers.
- Avoid placing digital supplies and clean supplies on adjacent board layers.
- Use a ground layer between noisy and clean supplies, if possible.
- Decouple all supply pins as close to the pins as possible, using small-value capacitors, with larger , bulk capacitors placed further away.

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11 Layout

11.1 Layout Guidelines

Use the DAC5652EVM layout as reference to obtain the best performance. A sample layout is shown in in the Figure 12-1 through Figure 12-4. Some important layout recommendations are:

1. Use a single ground plane. Keep the digital and analog signals on distinct separate sections of the board. This may be virtually divided down the middle of the device package when doing placement and layout.
2. Keep the analog outputs as far away from the switching clocks and digital signals as possible. This keeps coupling from the digital circuits to the analog outputs to a minimum.
3. Keep decoupling capacitors close to the power pins of the device.

11.2 Layout Example

图 11-1 through 图 11-4 show the layout examples.

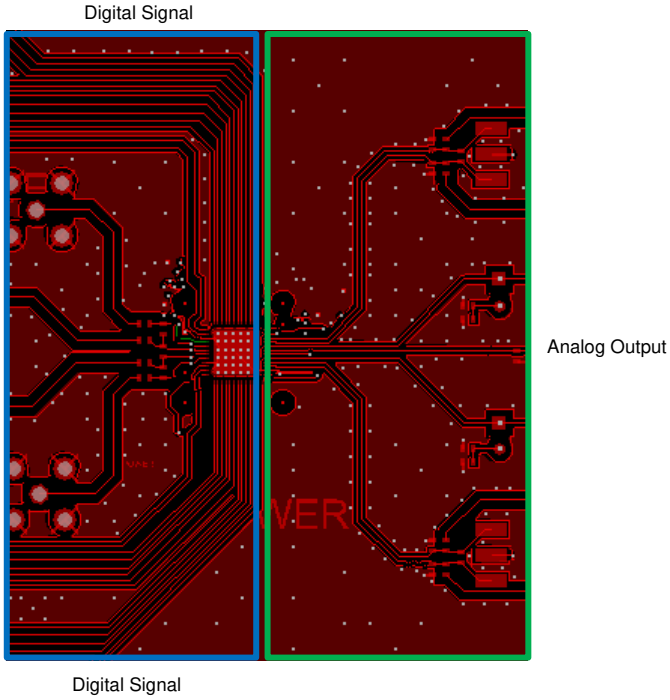


图 11-1. Top Layer (Layer 1)

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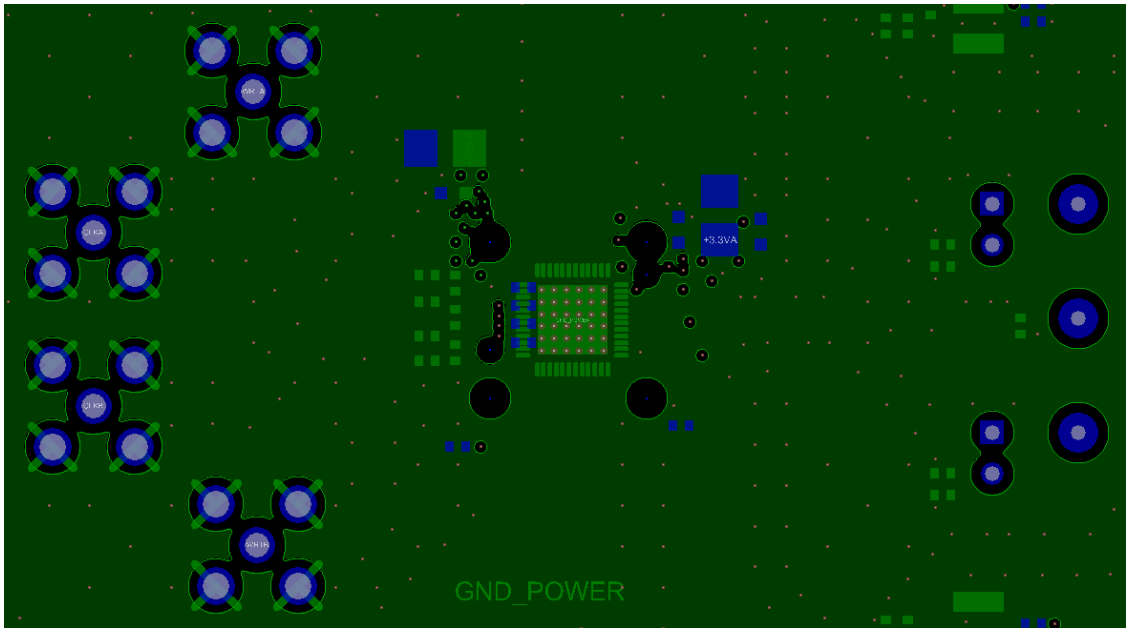
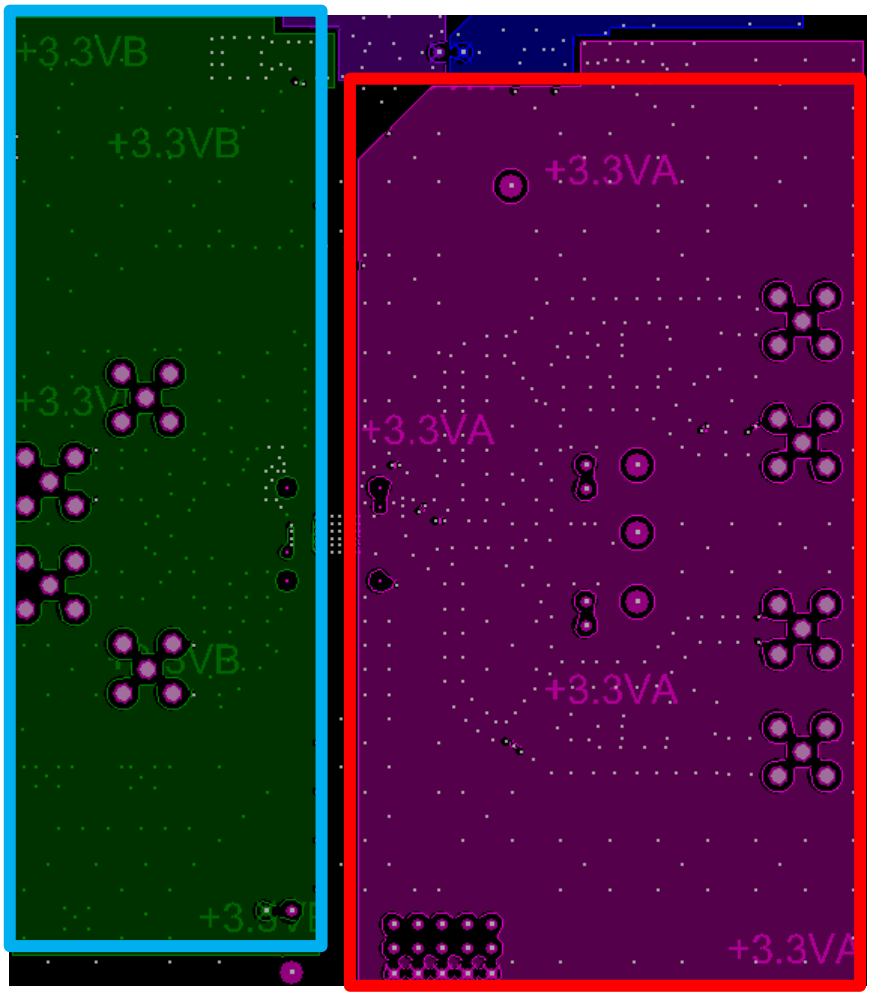


图 11-2. Single Ground Plane (Layer 2)



Digital Power Plane Analog Power Plane

图 11-3. Power Plane (Layer 3)

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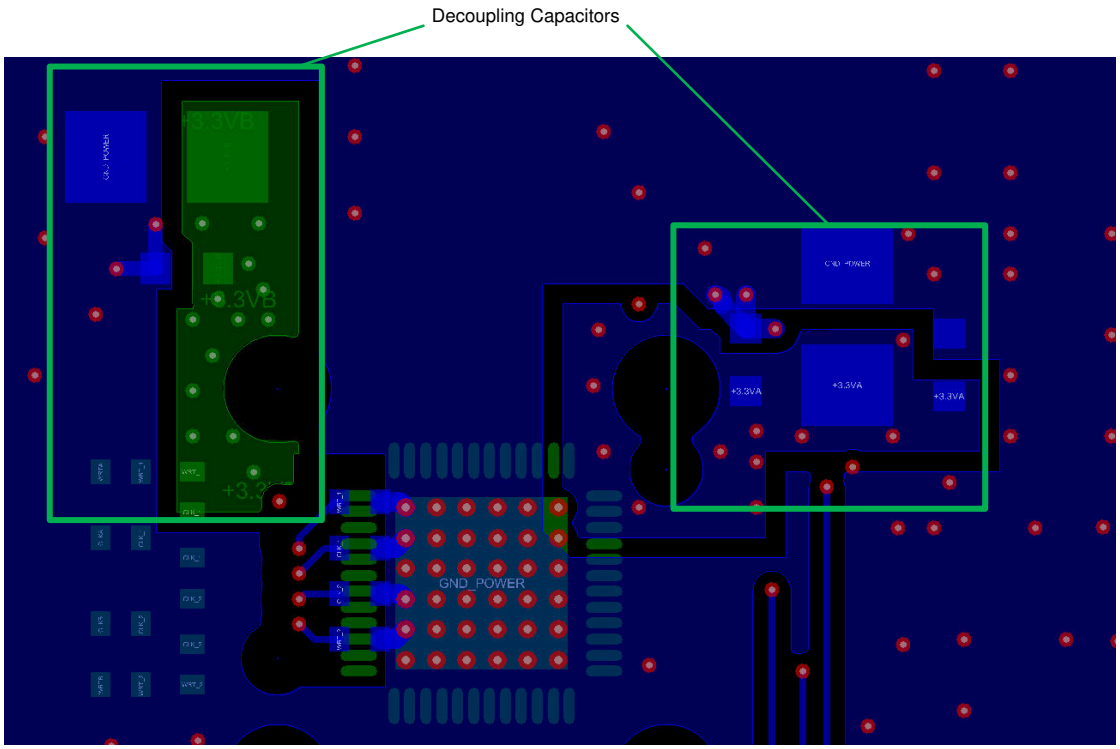


图 11-4. Bottom Layer (Layer 4)

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC5652IPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5652I
DAC5652IPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5652I
DAC5652IPFBG4	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5652I
DAC5652IPFBG4.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5652I
DAC5652IPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5652I
DAC5652IPFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5652I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DAC5652 :

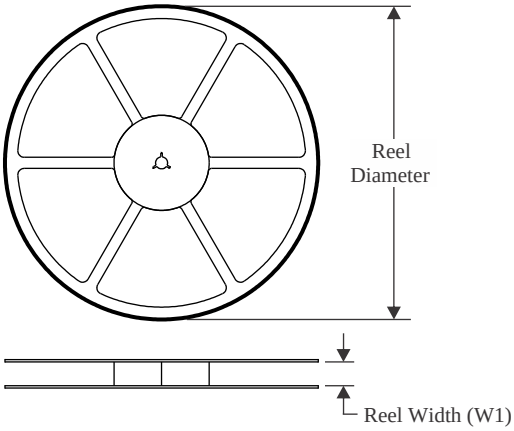
- Enhanced Product : DAC5652-EP

NOTE: Qualified Version Definitions:

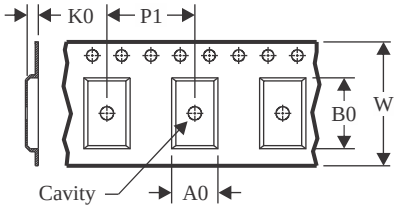
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

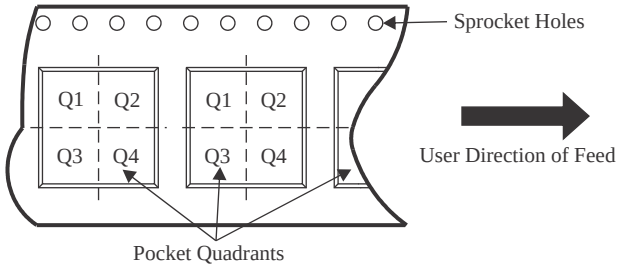


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

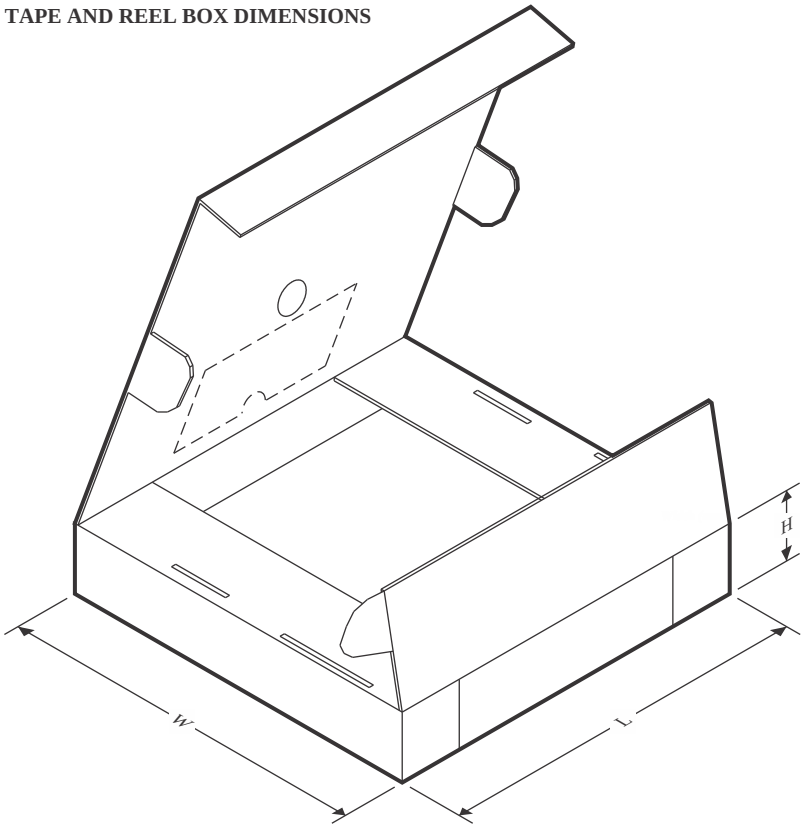
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5652IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

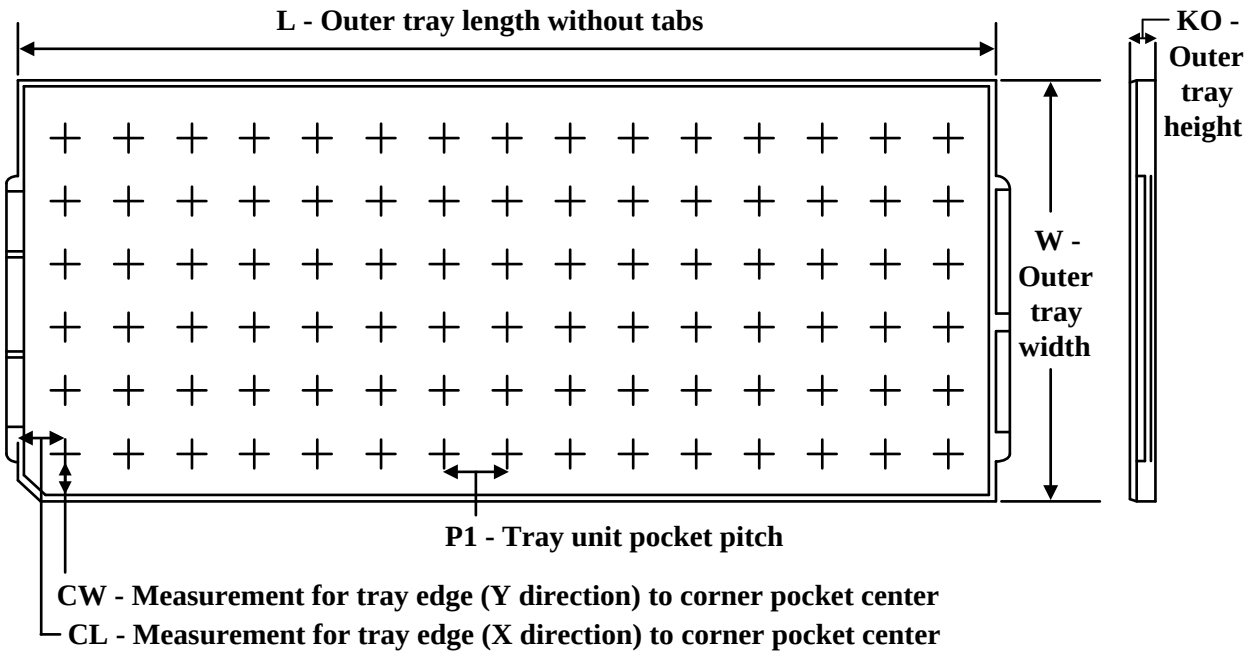
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5652IPFBR	TQFP	PFB	48	1000	367.0	367.0	38.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

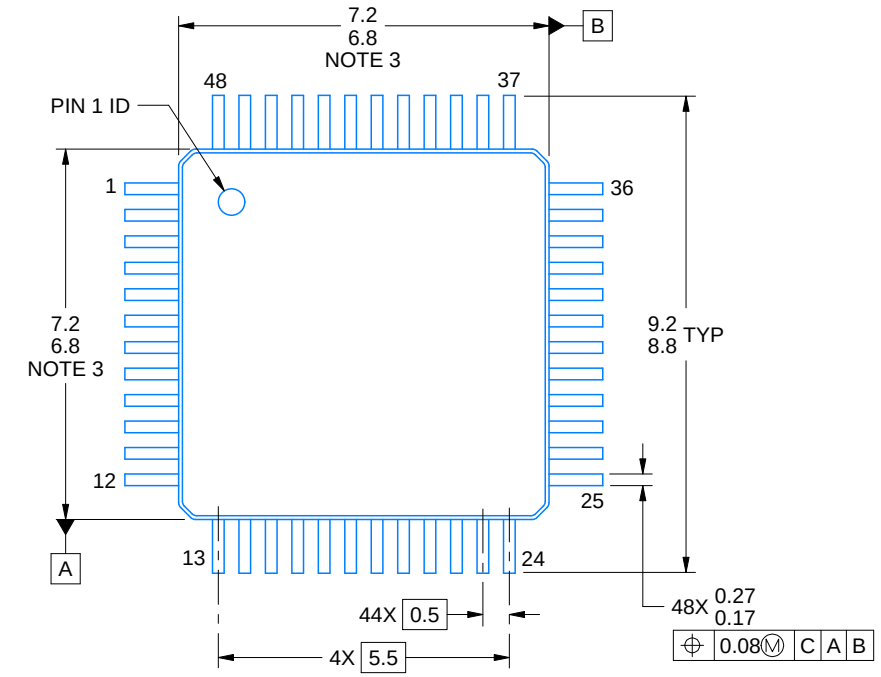
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC5652IPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25
DAC5652IPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25
DAC5652IPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25
DAC5652IPFBG4.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25

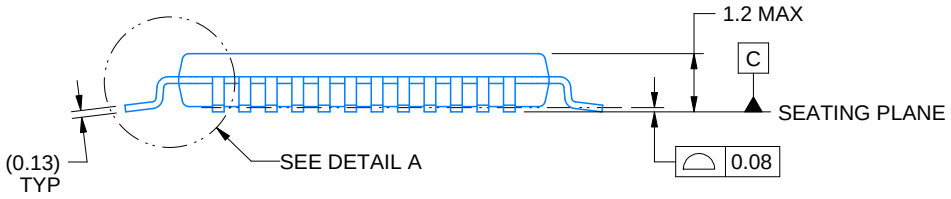
PACKAGE OUTLINE

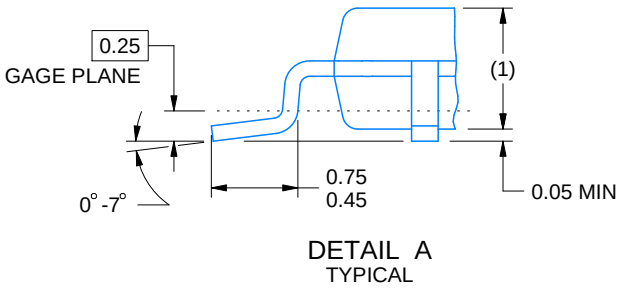
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK





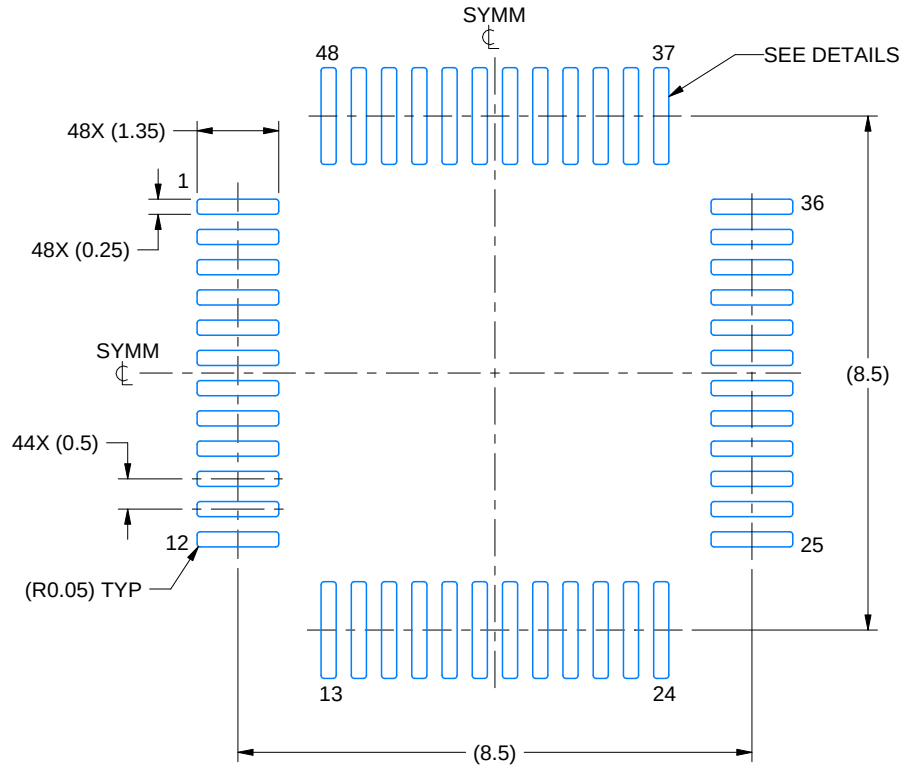


DETAIL A
TYPICAL

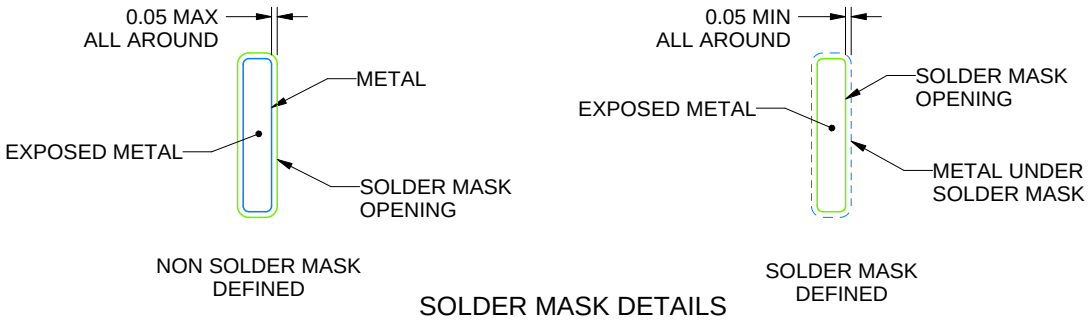
4215157/A 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

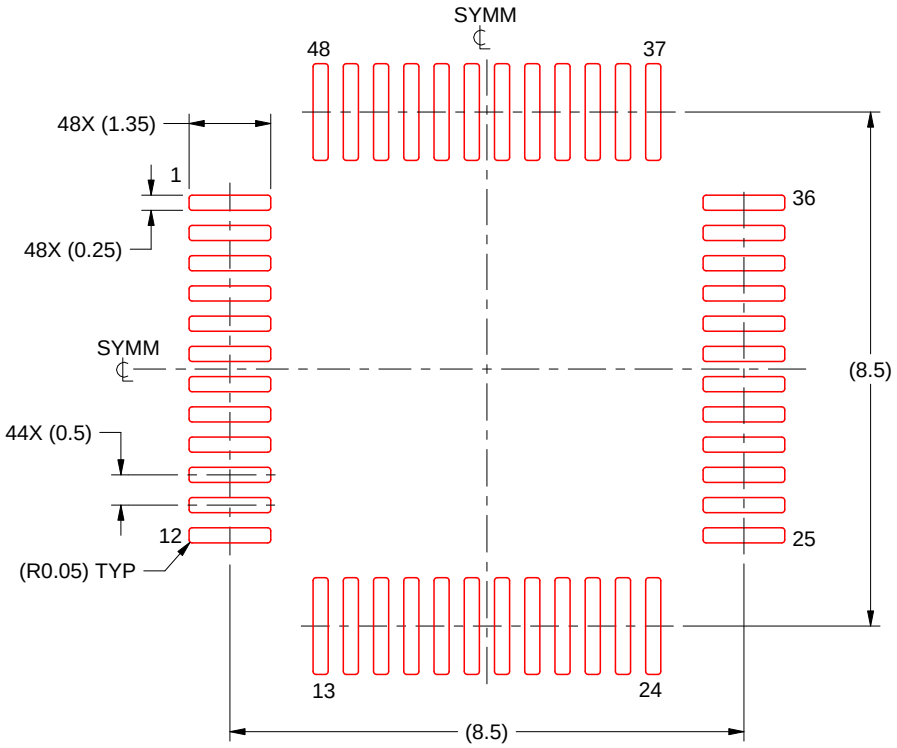


SOLDER MASK DETAILS

4215157/A 03/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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