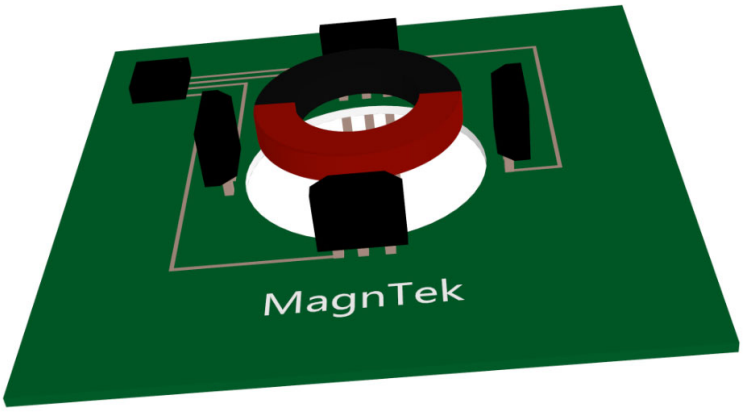
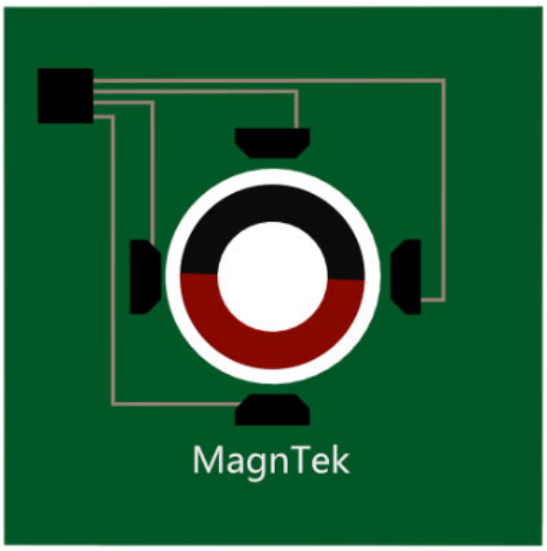
MT6708

Off-Axis Angle Position Encoder IC with External Hall Input

Features and Benefits

- Angle Encoder IC with External 4 Linear-Hall MT910X
- Off-Axis Mounting Application
- Independent Output Interface: I²C, SSI, ABZ，UVW and PWM Output
- Output Propagation Delay <35 us (Include MT910x and MT6708)
- Incremental ABZ Output Resolution 1~1024 Pulses per Magnet Pole-Pair
- UVW Output Resolution 1~16 Pairs per Magnet Pole-Pair
- RoHS Compliant 2011/65/EU
- QFN3x3-16L Package





Applications

- Absolute Position Applications
- Servo Motor Application
- Stepper Motor Application
- Robotics Joint Control

General Description

The MT6708 is an angle encoder IC working with 4 external linear hall sensors (MT910x) placed off-axis with a ring-magnet. The four linear hall sensors mounted at 90° to each other, deliver two differential sinusoidal output signals with a rotating ring magnet in the x-y plane indicating the angle (α) of the magnetic field direction.

The incremental ABZ output mode is available from this IC, making the chip suitable to replace various optical encoders. ABZ output resolution is 1~1024 pulse per magnet pole-pair user programmable.

The incremental UVW output mode is also available for brushless motor control. The UVW output resolution is 1~16 pole-pairs per magnet pole-pair user programmable.

A standard I²C or SSI interface allows a host microcontroller to read the 14-bit absolute angle position data from MT6708. The absolute angle position is also provided as PWM output.

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1. Pin Configuration

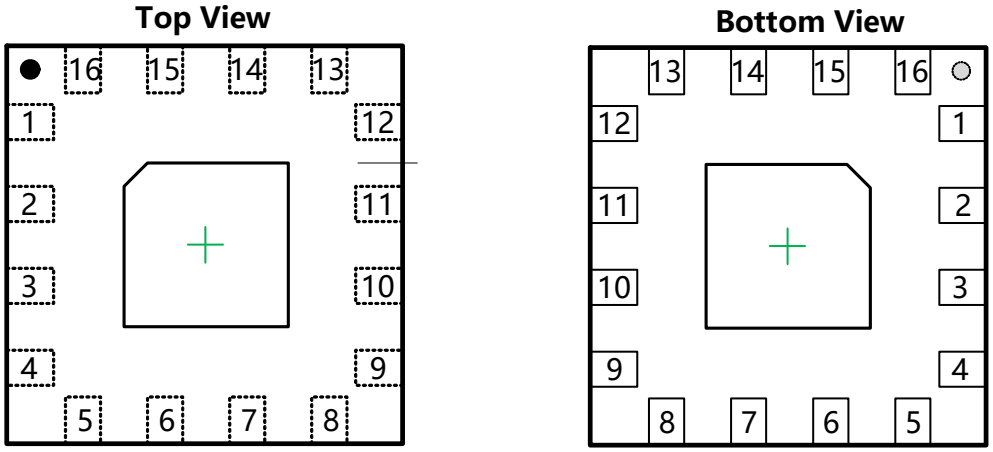


Figure 1: Pin Configuration

Pin List

Name	#	Type	Description
H1P	1	Analog Input	External Linear Hall1 Positive Input
H1N	2	Analog Input	External Linear Hall1 Negative Input
H2P	3	Analog Input	External Linear Hall2 Positive Input
H2N	4	Analog Input	External Linear Hall2 Negative Input
NC	5	-	Not Connected
A	6	Digital Input/output	Incremental Signal A, or I²C Data 'SDA', or SSI data 'DO'
B	7	Digital Input/output	Incremental Signal B, or I²C Clock 'SCL', or SSI Clock 'CLK'
Z	8	Digital Input/output with Build in 200KΩ Pull-up Resistor	Incremental Signal Z, or SSI 'CSN'
W	9	Digital Output	Incremental Signal W or –Z
NC	10	-	Not Connected
U	11	Digital Output	Incremental Signal U or –A
V	12	Digital Output	Incremental Signal V or –B
VDD	13	Power Supply	3.3~5.0V Supply
MODE	14	Digital Input with Build in 200KΩ Pull-up Resistor	ABZ or I²C/SSI Selection
OUT	15	Digital Output	PWM Output
GND	16	Power Supply	Ground

Family Members

Part Number	Description
MT6708QT-STD	QFN-16 Package, Reel Pack (1000pcs/Reel)

QFN-16 Reflow Sensitivity Classification: MSL-1

2. Functional Diagram

The MT6708 is manufactured in a standard CMOS process, it receives the external signal from 4 linear hall sensors' signal (MT910x) mounted at 90° to each other.

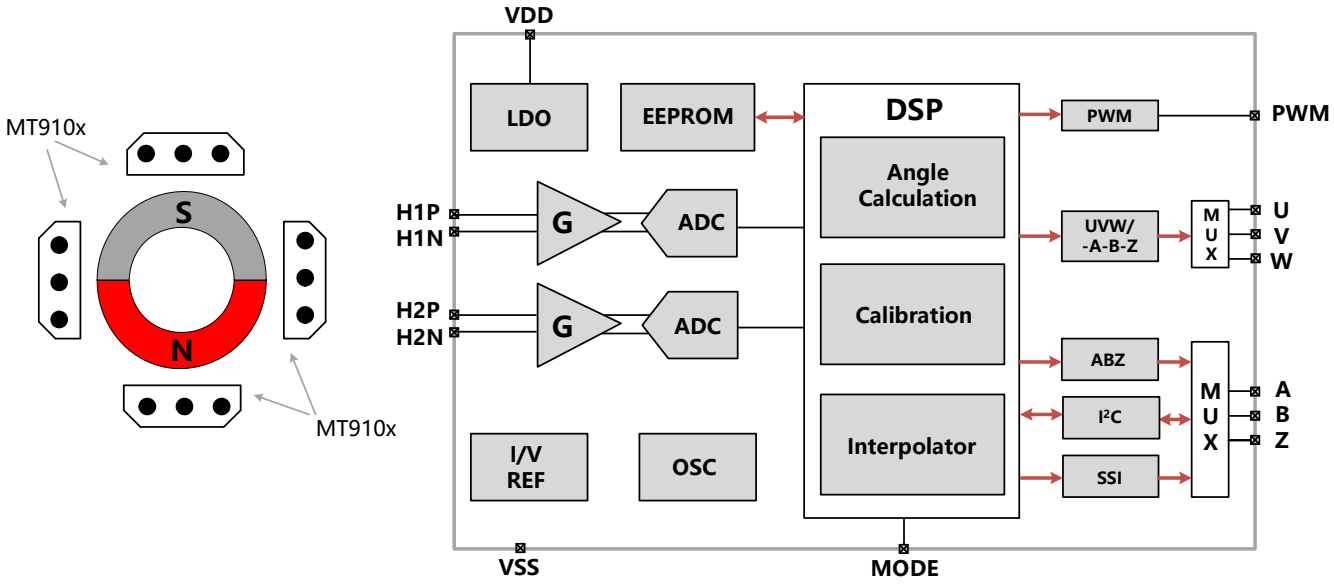


Figure 2: Block Diagram

Figure 2 shows a simplified block diagram of the chip, consisting of the external linear hall sensors to generate cosine and sine signals, gain stages, analog-to-digital converters (ADC) for signal conditioning, and a digital signal processing (DSP) unit for encoding. Other supporting blocks such as LDO, etc. are also included.

3. Absolute Maximum Ratings (Non-Operating)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Name	Min.	Max.	Unit
DC Voltage at Pin VDD	-0.5	7	V
Storage Temperature	-55	150	℃
Operating Temperature	-40	125	℃
Electrostatic Discharge (HBM)	-	±6.0	KV
Electrostatic Discharge (CDM)	-	±1.5	KV

4. Electrical Characteristics

Operation conditions: Ta=-40 to 125℃, VDD=3.0~5.5V unless otherwise noted.

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	Normal Operation	3.0	-	5.5	V
		EEPROM Programming	4.5		5.5	V
Idd	Supply Current	-	-	4	-	mA
LSB	Resolution (ABZ Mode)	N Steps per Cycle		360°/N	-	°
TN	Transition Noise (ABZ Mode)	25℃	-	0.03	-	°rms
Hyst	Hysteresis (ABZ Mode)		-	0.088	-	°
T_{PwrUp}	Power-Up Time	VDD Ramp<10us	-	-	1.0	ms
T_{Delay}	Propagation Delay	Constant Speed		35		us
PWM Output Characteristics						
FPWM	PWM Frequency	Programmable	-5% @27℃	994.4 /497.2	+5% @27℃	Hz
T_{Rise}	Rising Time	C_L=1nF	-	-	1	us
T_{Fall}	Falling Time	C_L=1nF	-	-	1	us
Digital I/O Characteristics (Push-Pull Type in Normal Mode)						
V_{IH}	High Level Input Voltage	-	0.7*VDD	-	-	V
V_{IL}	Low Level Input Voltage	-	-	-	0.3*VDD	V
V_{OH}	GPIO Output High Level	Push-pull (Iout=2mA)	VDD-0.1	-	-	V
V_{OL}	GPIO Output Low Level	Push-pull (Iout=2mA)	-	-	0.1	V
I_{LK}	Input Leakage Current	-	-	-	±1	uA

5. Magnetic Input Specifications

Operation conditions: Ta=-40 to 125℃, VDD=3.0~5.5V unless otherwise noted, 1 pole-pair diametrically magnetized ring magnet.

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
Bpk	Magnetic Input Field Amplitude	Measure at the IC Surface (1)	-	-	-	mT
AG	Air Gap	Magnetic to MT910x Distance	-	-	2.0	mm
RS	Rotation Speed	N is pole-pairs of the Ring Magnet	-	-	60000/N	RPM
TCmag1	Recommended Magnet Material and Temperature Drift Coefficient	NdFeB (Neodymium Iron Boron)	-	-0.12	-	%/℃
TCmag2		SmCo (Samarium Cobalt)	-	-0.035	-	

Note(1): Depends on the choice of linear hall sensor’ s sensitivity

6. Output Mode

The MT6708 provides ABZ, UVW and PWM at output pins, also angle position data could be transferred by I²C or SSI interface.

6.1 I/O Pin Configuration

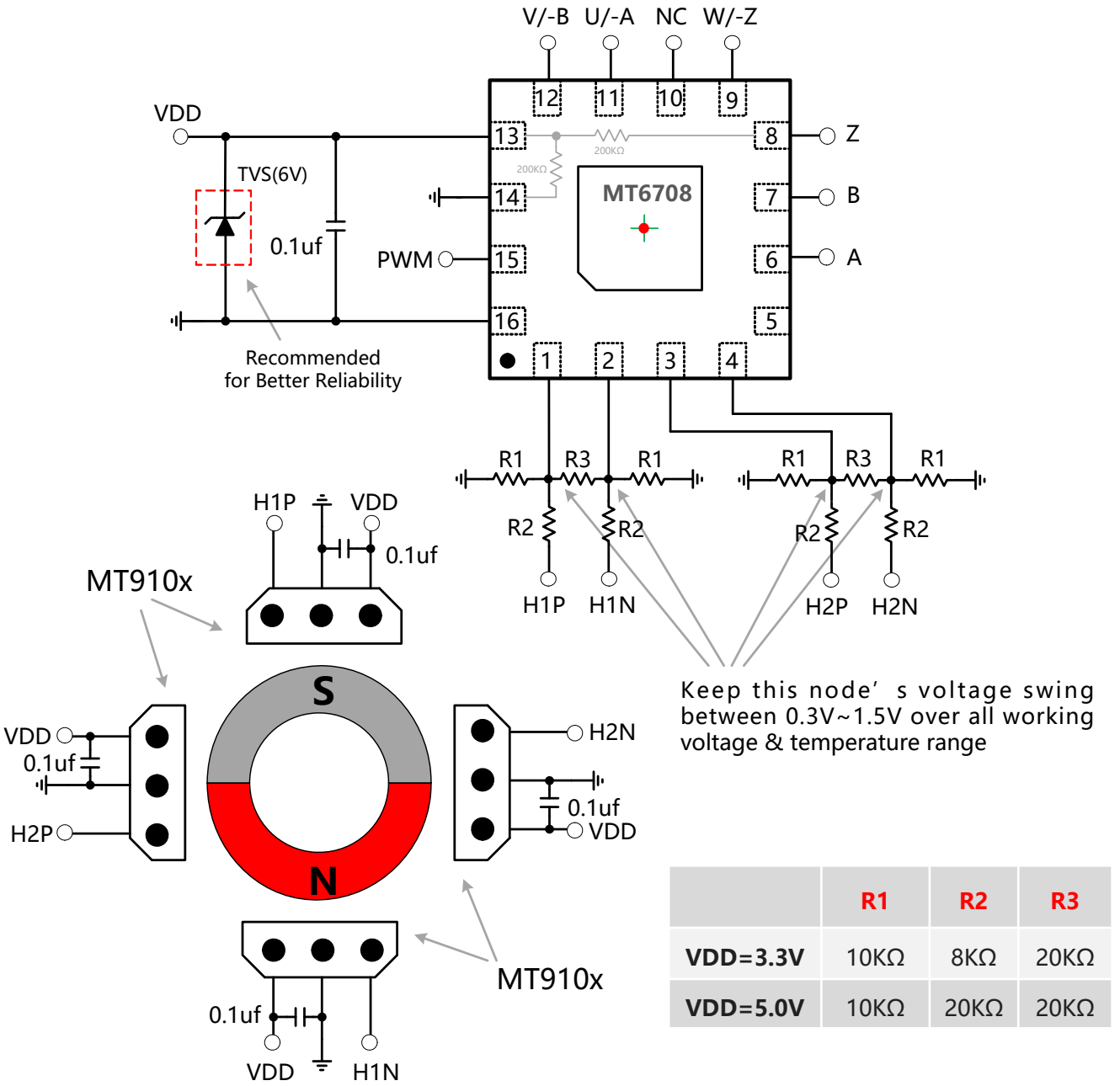
For QFN-16 package, ABZ (Single-end), I²C and SSI are configured to Pin.6, Pin.7 and Pin.8. UVW and –A-B-Z are configured to Pin.11, Pin.12 and Pin.9. PWM output is configured to Pin.15.

QFN-16 Package I/O Pin Configuration

Pin#	I²C	SSI	ABZ	ABZ+UVW	ABZ Differential	PWM
6	SDA	DO	A	A	A	
7	SCL	CLK	B	B	B	
8		CSN	Z	Z	Z	
9				W	-Z	
11				U	-A	
12				V	-B	
15						PWM

6.2 Reference Circuit for ABZ/UVW/PWM

Figure 3 shows the reference circuit for ABZ, UVW and PWM output. A degenerating resistor ladder (R1~R3) between the output of external linear hall sensors and the input of MT6708 is necessary to match the common mode voltage and signal swing.



	R1	R2	R3
VDD=3.3V	10KΩ	8KΩ	20KΩ
VDD=5.0V	10KΩ	20KΩ	20KΩ

Figure 3: Reference Circuit for ABZ/UVW/PWM Output

6.3 Quadrature A, B and Index Output

As shown in Figure 4, when the magnet rotates counter-clock-wise (CCW), output B leads output A by 1/4 cycle, when the magnet rotates clock-wise (CW), output A leads output B by 1/4 cycle (or 1 LSB). Output Z indicates the zero position of the magnet.

After chip power-on, the ABZ output is blocked for 30ms to guarantee proper output.

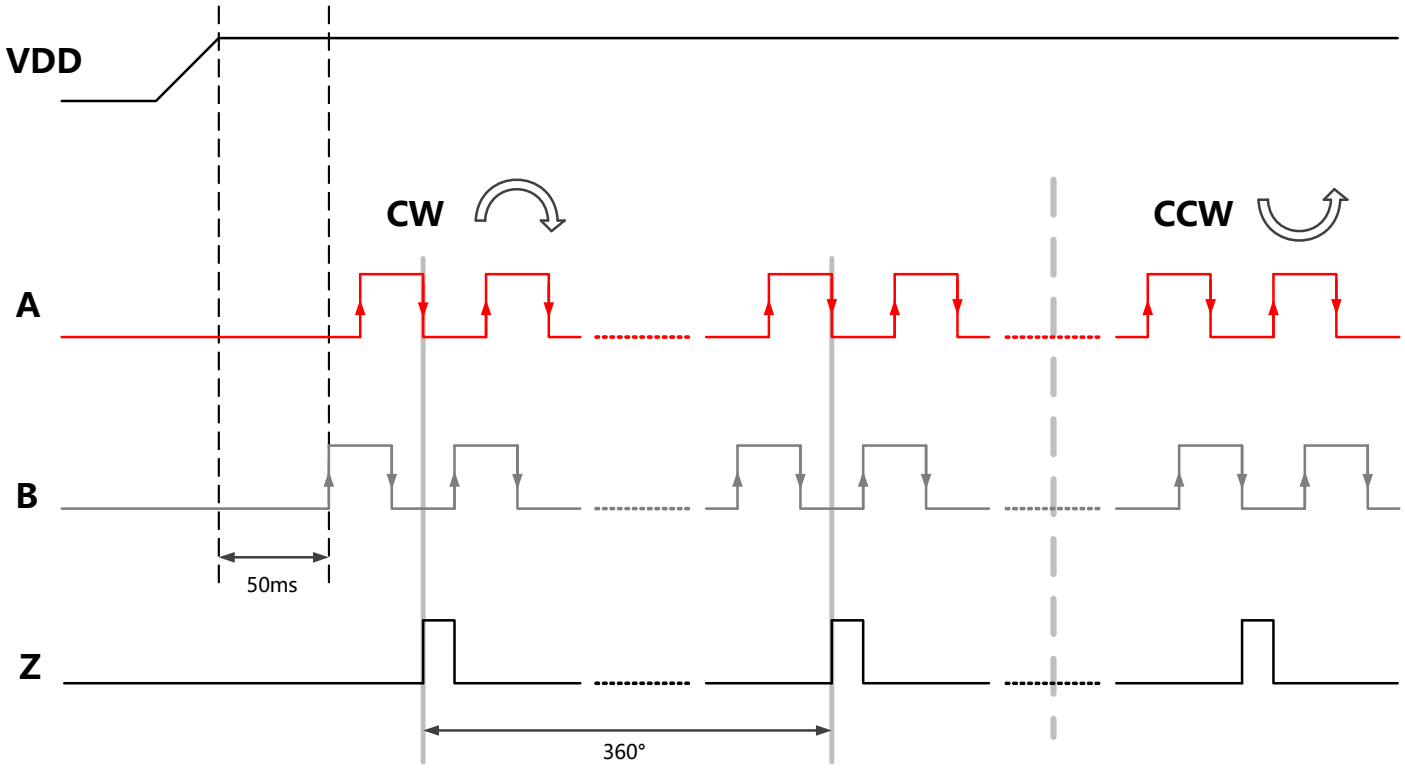


Figure 4: ABZ output with VDD power on

Output Z indicates the zero position of the magnet and the pulse width of Z is selectable as 1, 2, 4, 8, 12, 16 LSBs and 180° as shown in Figure 5 and Figure 6. It is guaranteed that one Z pulse is generated for every rotation. The zero position is user programmable。

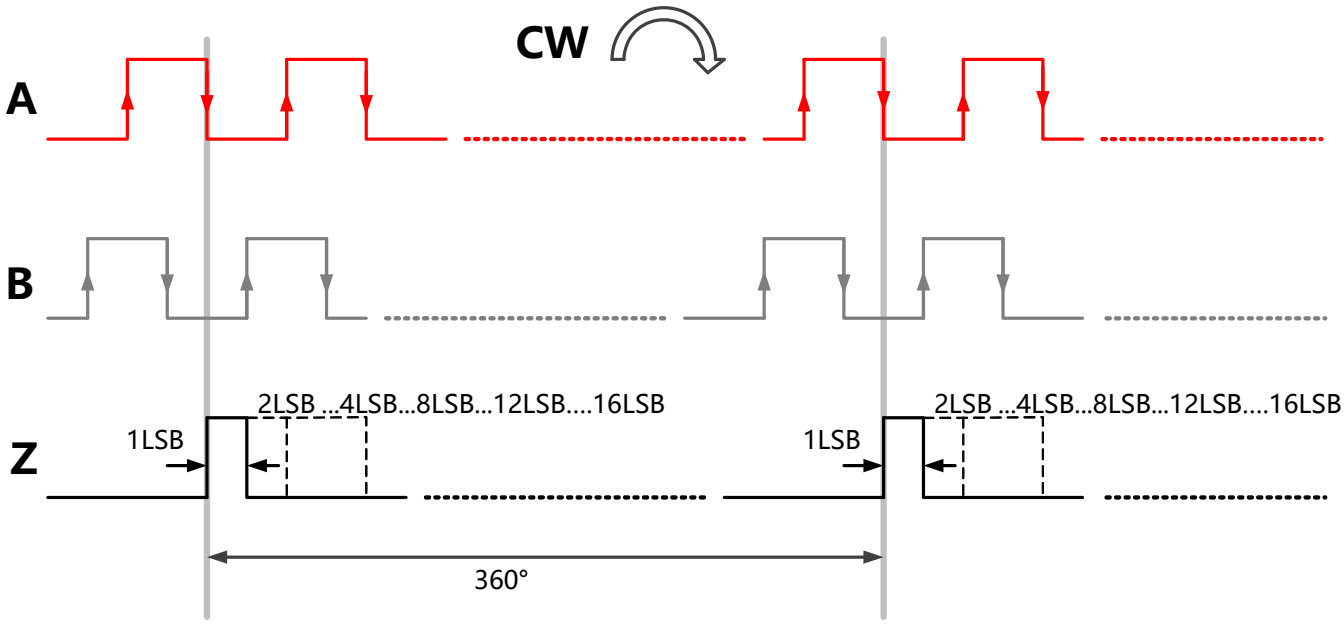


Figure 5: Typical ABZ Output w/i Z pules width=1,2,4,8,12 and 16 LSBs

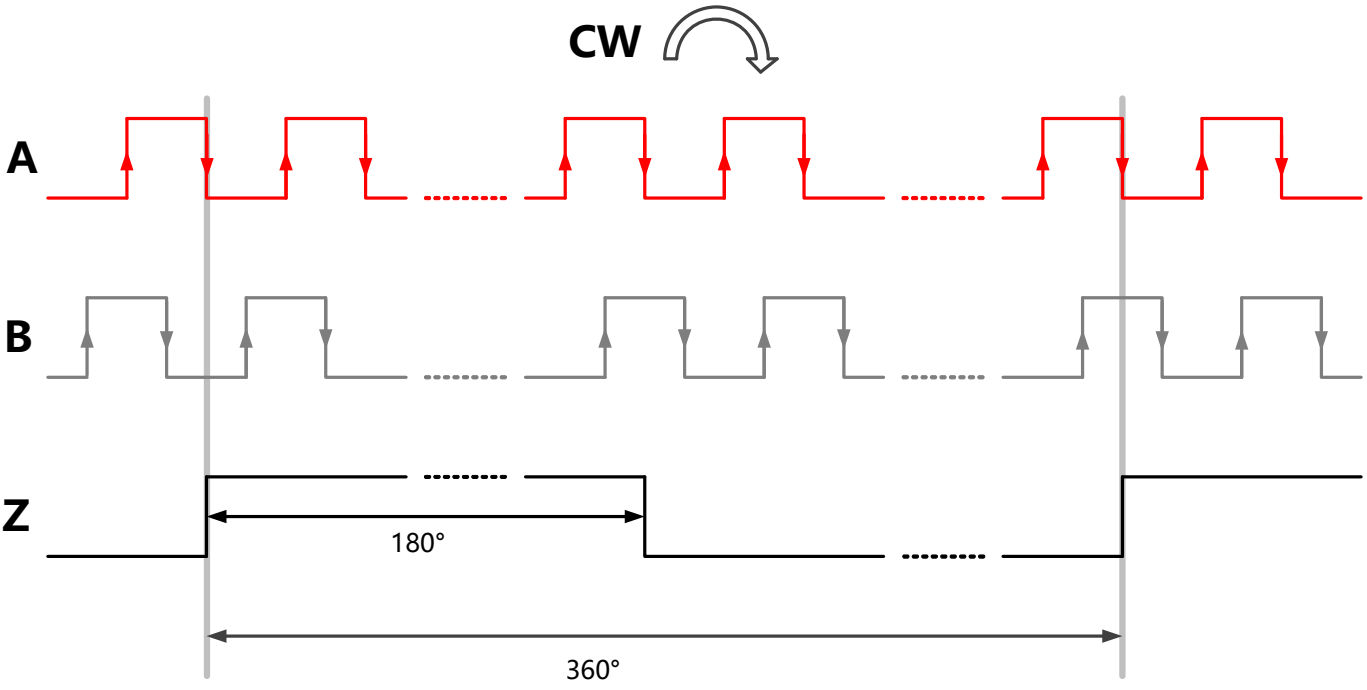
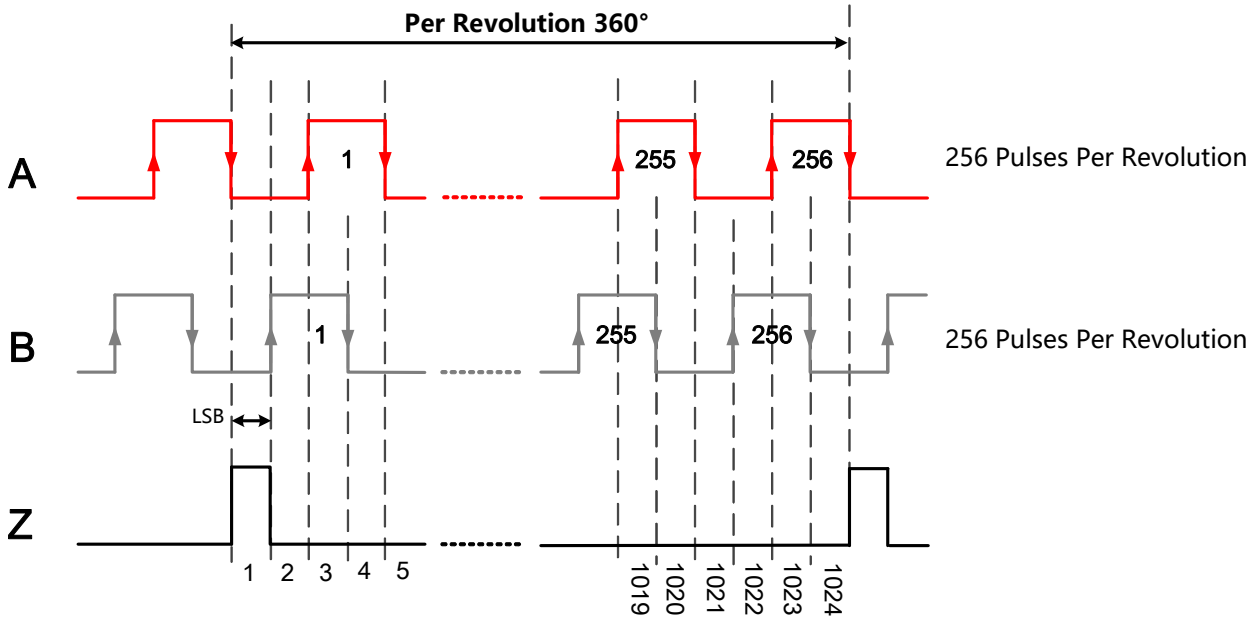


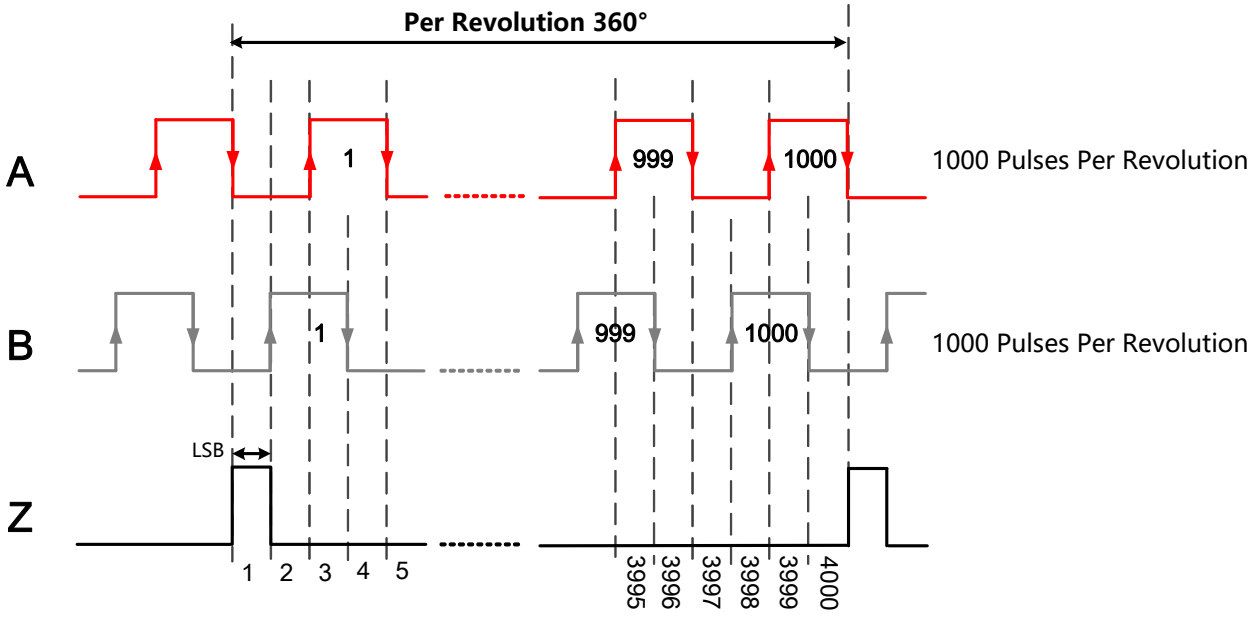
Figure 6: Typical ABZ Output w/i Z pules width=180°

ABZ resolution is user programmable from 1~1024 PPR. The relationship between binary bits, LSBs and PPR resolution of ABZ output are shown in Figure 7 and Figure 8.



10 bit=2^{10} LSBs=1024 Steps=256 PPR

Figure 7: ABZ Output Resolution=10 bit



1000 PPR=4000 Steps

Figure 8: ABZ Output Resolution=1000 PPR

The Z/Index pulse width could be programmed

Z/Index Pulse Width Register (EEPROM)

Reg. Z_Pulse_Width<2:0>	Width (LSBs)	Reg. Z_Pulse_Width<2:0>	Width (LSBs)
000	1	**100**	12
001	2	**101**	16
010	4	**110**	180°
011	8	**111**	1

The mechanical zero position could be programmed, it is a 12 bits data for 0~360°.

Zero Position Register (EEPROM)

Register	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Zero_MSB	NA	Z_Pulse_Width<2:0>			Zero<11:8>			
Zero_LSB	Zero<7:0>							

The resolution of ABZ could be programmed by a 10 bit register ‘ABZ_RES’

ABZ Resolution Register (EEPROM)

Register	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ABZ_RES	UVW_Res<3:0>				NA	NA	ABZ_RES<9:8>	
ABZ_RES	ABZ_RES<7:0>							

6.4 UVW Output Mode

The MT6708 provides U, V and W pulses which are 120° (electrical) out of phase as shown in Figure 9. The cycles of UVW per rotation can be programmed.

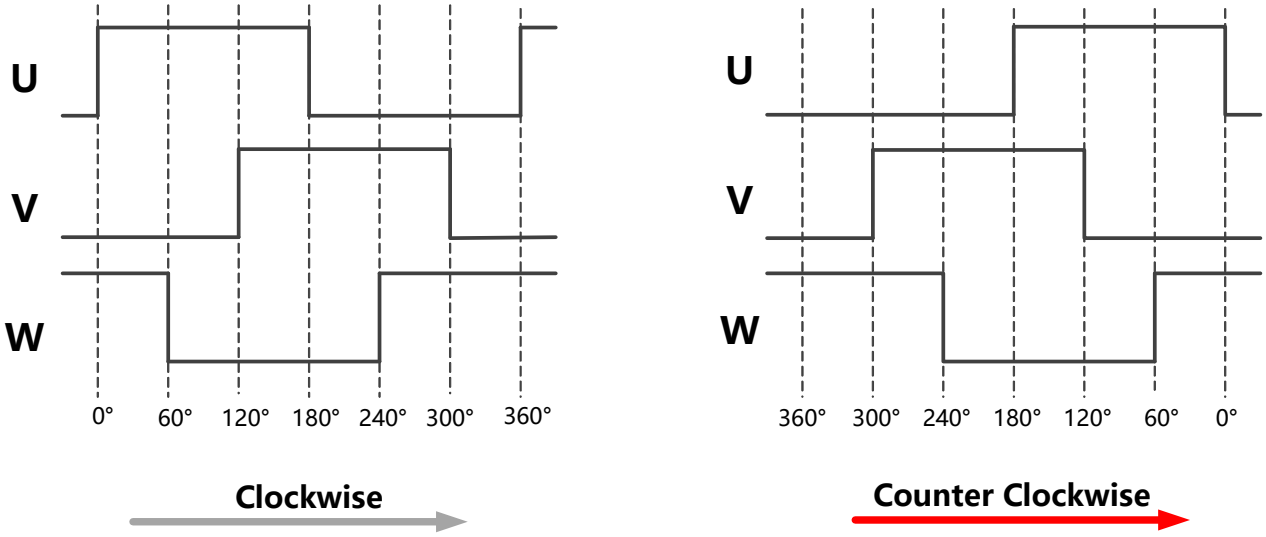


Figure 9: Typical Output Waveform for UVW Mode

UVW Pole Pairs Register (EEPROM)

Reg. UVW_RES<3:0>	UVW Pole Pairs
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1000	9
1001	10
1010	11
1011	12
1100	13
1101	14
1110	15
1111	16

6.5 Pulse Width Modulation (PWM) Output Mode

The MT6708 provides a digital Pulse Width Modulation (PWM) output, whose duty cycle is proportional to the measured angle as shown in Figure 10.

The PWM output consists of a frame of 4119 PWM clock periods. The angle data is represented with 12-bit resolution in the frame. One PWM clock period represents 0.088° and has a typical duration of 244ns which also could be programmed to be 488ns.

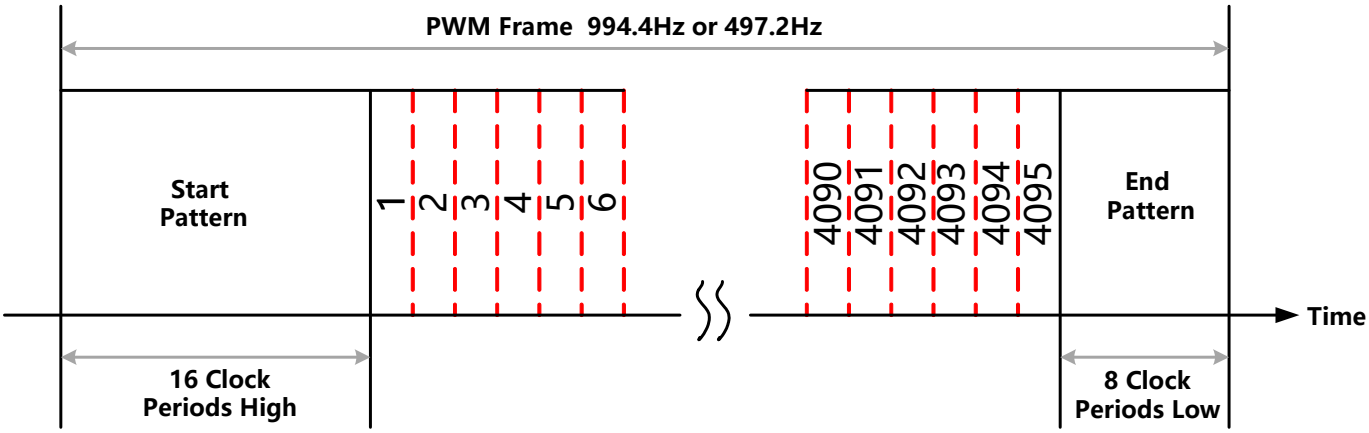


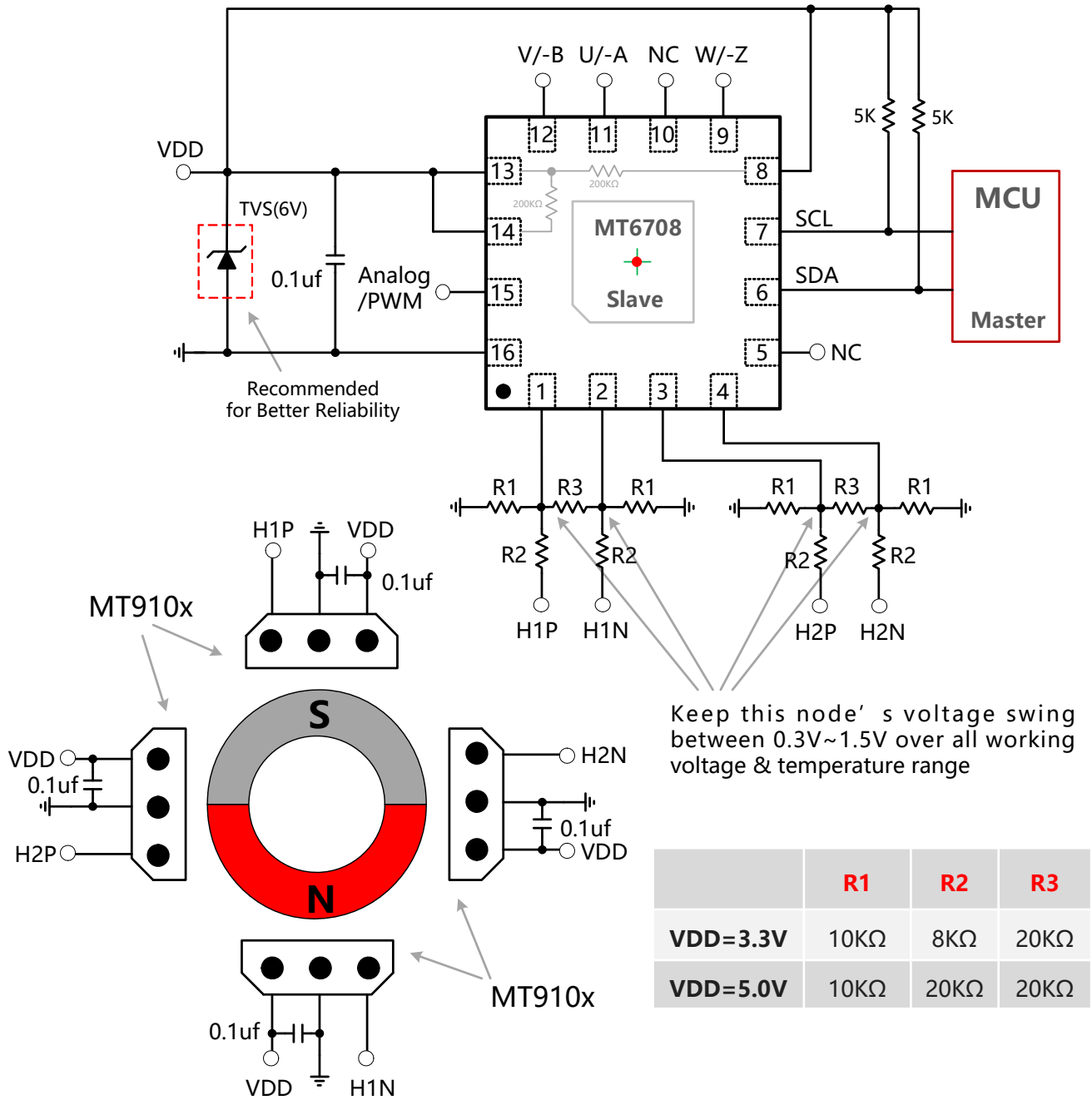
Figure 10: PWM Output Frame

PWM Frequency (EEPROM)

Reg. PWM_Freq	PWM Frame Frequency
0	994.4 Hz
1	497.2 Hz

6.6 I²C Interface

The MT6708 provides a slave I²C interface for host MCU to read back digital absolute angle information from its internal registers. The reference circuit for I²C interface is shown in Figure 11, whether the need for pull-up resistor on SCL is determined by MCU, for MT6708 SCL is a digital input.



	R1	R2	R3
VDD=3.3V	10KΩ	8KΩ	20KΩ
VDD=5.0V	10KΩ	20KΩ	20KΩ

Figure 11: I²C Reference Circuit

6.6.1 I²C Timing Diagram

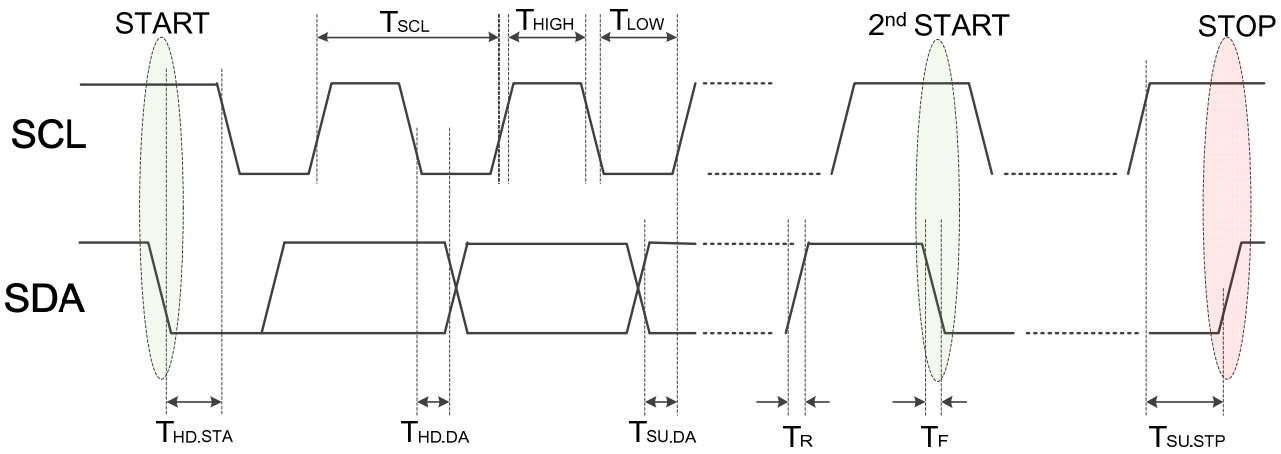


Figure 12: I²C Timing Diagram

I²C Timing Parameter

Parameter	Notes	Min.	Max.	Unit
T_{SCL}	SCL Clock Period	1	-	μs
$T_{HD.STA}$	Hold Time of 'START'	250	-	ns
T_{LOW}	Low Phase of SCL	250	-	ns
T_{HIGH}	High Phase of SCL	250	-	ns
$T_{SU.DA}$	Setup Time of SDA	100	-	ns
$T_{HD.DA}$	Hold Time of SDA	50	-	ns
T_R	Rising Time of SDA/SCL	-	150	ns
T_F	Falling Time of SDA/SCL	-	150	ns
$T_{SU.STP}$	Setup Time of 'Stop'	250	-	ns

6.6.2 I²C Read Angle Registers

The default slave ID of MT6708 is b' 0000110 in 7-bit binary form(It could be programmed to b' 0100110) . The 14 bits angle data is stored in internal register 0x03 and 0x04. Please follow the I²C timing of Figure 20 to read the angle data from 0x03 and 0x04 registers.

Note: Please read Register 0x03 first and then read 0x04

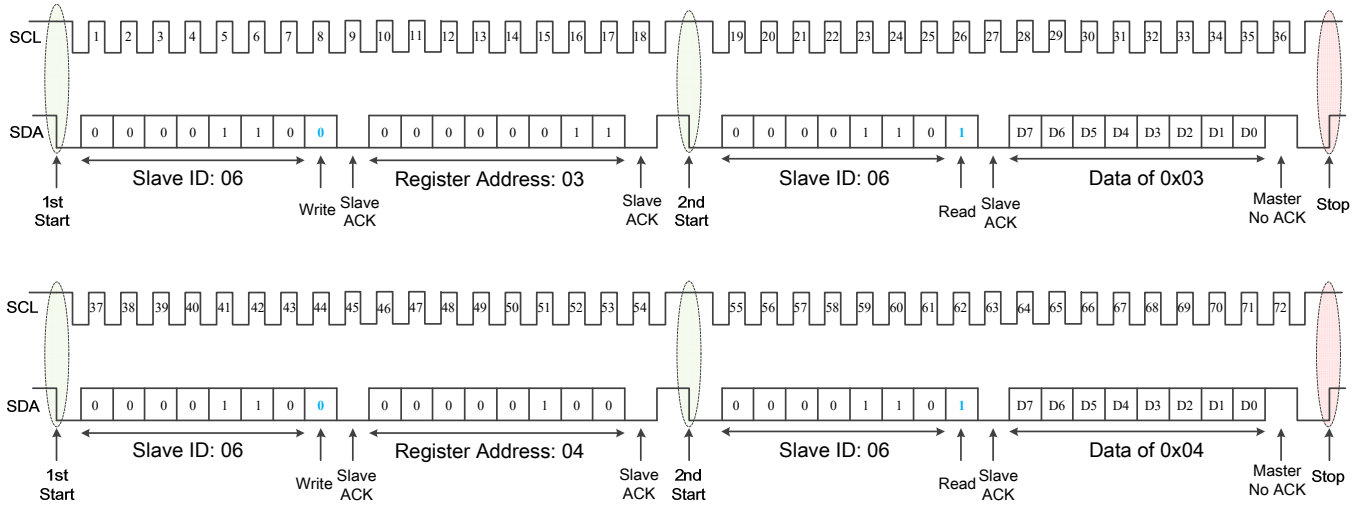


Figure 13: I²C Single Byte Read

Angle Data Register

Reg. Addresss	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Angle<13:6>							
0x04	Angle<5:0>						NA	NA

0~360° absolute angle θ could be calculated by the below formula:

$$\theta = \frac{\sum_{i=0}^{13} Angle<i> \cdot 2^i}{16384} \cdot 360°$$

6.6.3 I²C Write

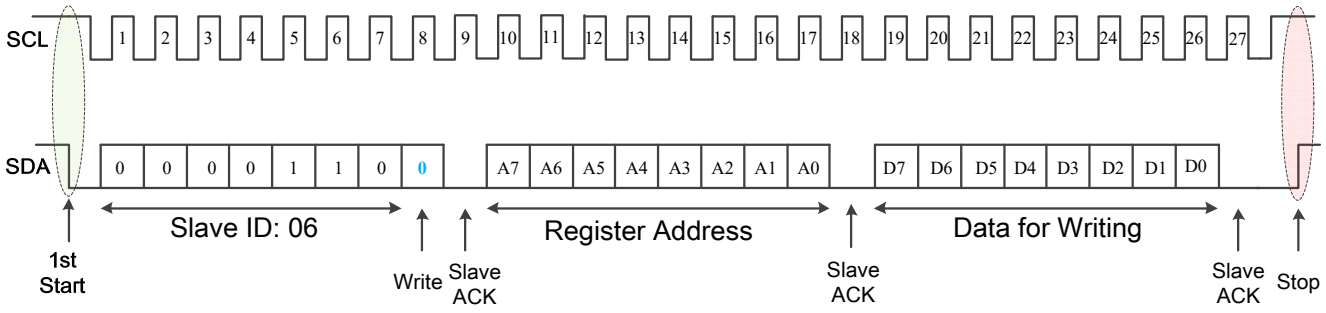
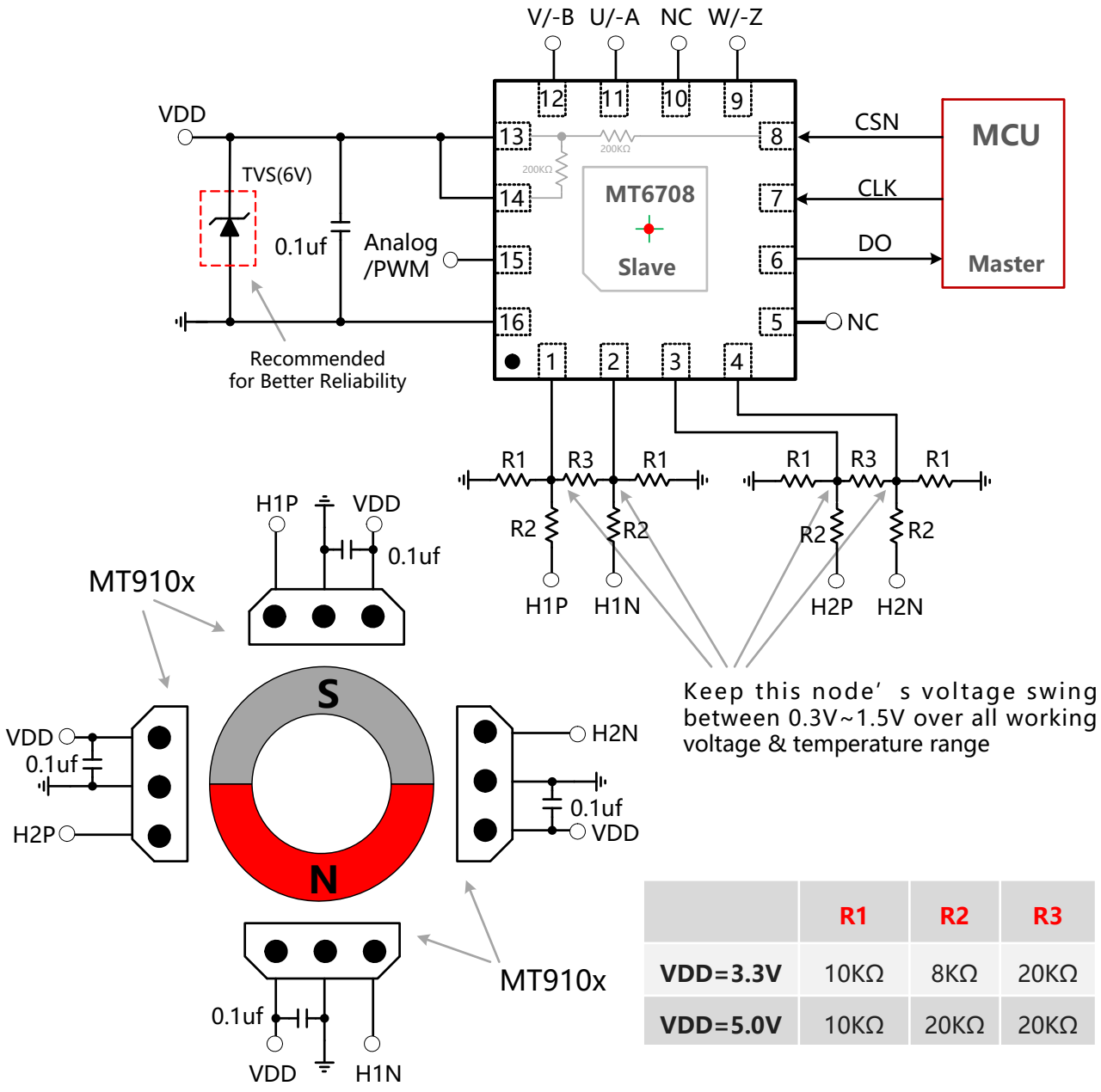


Figure 14: I²C Write

6.7 SSI Interface

The MT6708 also provides an SSI interface for host MCU to read back digital absolute angle information from its internal registers. The reference circuits for SSI interface are shown in Figure 15.



	R1	R2	R3
VDD=3.3V	10KΩ	8KΩ	20KΩ
VDD=5.0V	10KΩ	20KΩ	20KΩ

Figure 15: SSI Interface Reference Circuit

6.7.1 SSI Timing Diagram

The MT6708 SSI is shown in Figure 16, a data transfer starts when CSN is pulled to logic 'Low'. The MT6708 transfers data on the falling edge of CLK, and the data transfer finally stops when CSN is pulled to logic 'High'

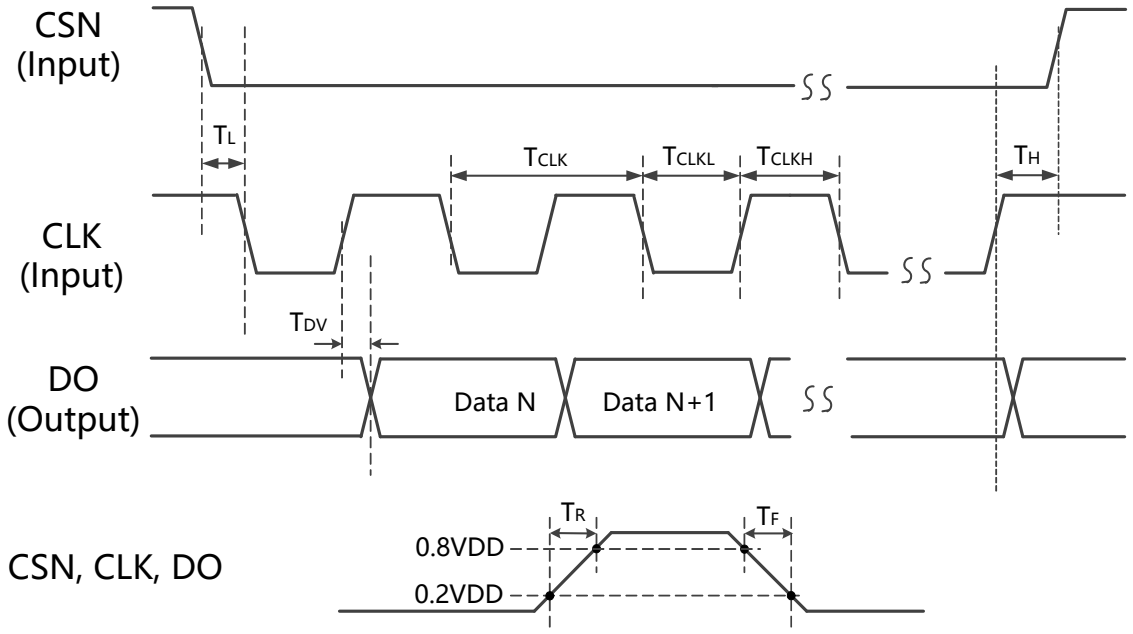


Figure 16: SSI Timing Diagram

SSI Timing Parameter

Symbol	Notes	Min.	Typ.	Max.	Unit
T_L	Time between CSN falling edge and CLK falling edge	100		-	ns
T_{CLK}	Clock period	64		-	ns
T_{CLKL}	Low period of clock	30		-	ns
T_{CLKH}	High period of clock	30		-	ns
T_H	Time between CLK last rising edge and CSN rising edge	$0.5 \cdot T_{CLK}$		-	ns
T_R	Rise Time of Digital Signal (with 20pf Loading Condition)	-	10	-	ns
T_F	Fall Time of Digital Signal (with 20pf Loading Condition)	-	10	-	ns
T_{DV}	Data valid time of DO (with 20pf Loading Condition)	-	-	15	ns

6.7.2 SSI Read Angle

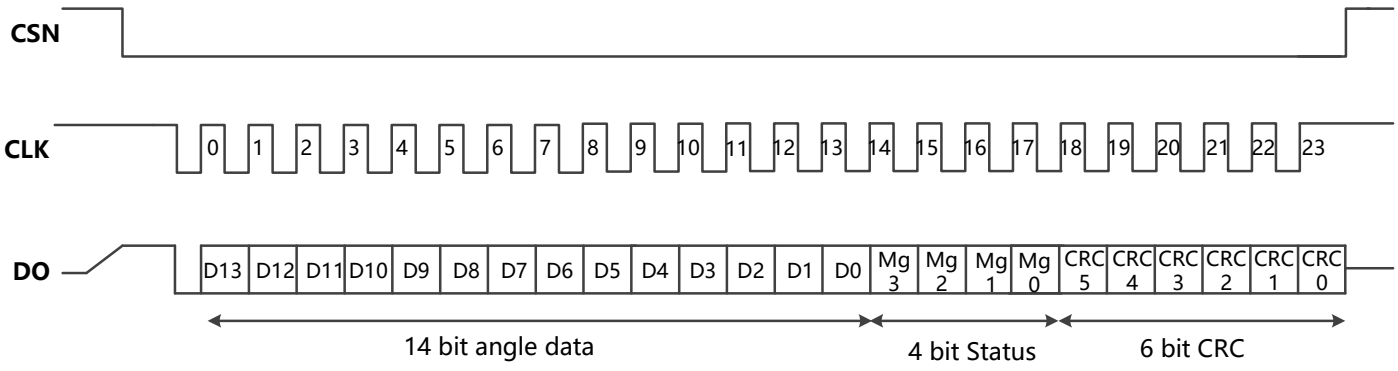


Figure 17: SSI Data Format

An SSI data transfer starts when CSN is pulled to logic 'Low', as shown in Figure 17. CLK is the Serial Port Clock and it is controlled by the SSI master; it is high when there is no SSI transmission. DO (Data Output) is the Serial Port Data Output from MT6708, it is driven at the rising edge of CLK and should be captured at the falling edge of CLK.

Bit 0-13: 14-bit Angle Data D[13:0]
Bit 14-17: 4-bit Magnetic Field Status Mg[3:0]
Bit 18-23: 6-bit CRC Code CRC[5:0]

0~360° absolute angle θ could be calculated by the below formula with D[13:0]:

$$\theta = \frac{\sum_{i=0}^{13} D<i> \cdot 2^i}{16384} \cdot 360°$$

Mg[3:0] Magnetic Field Status Truth Table:

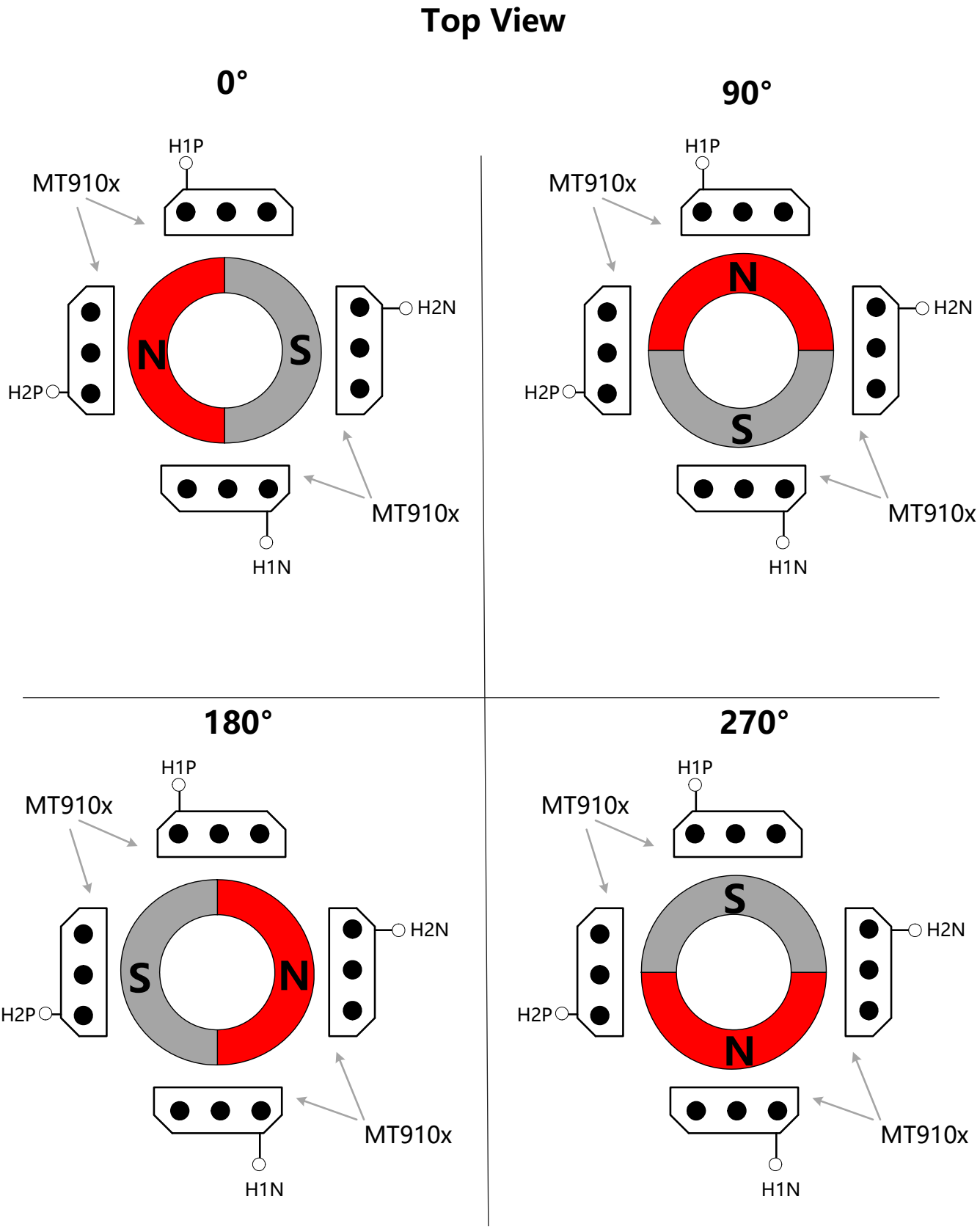
Mg[1:0]	Status
0	Normal
1	Magnetic Field is too Strong
2	Magnetic Field is too Weak
3	-

Mg[2]	Status
0	Normal
1	Push Button is Detected

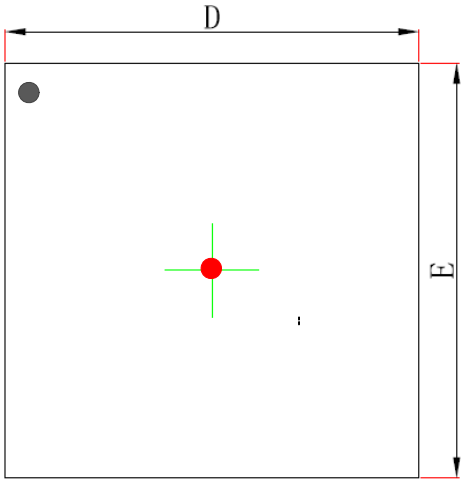
Mg[3]	Status
0	Normal
1	Loss of Track

CRC Data Range: D[13:0] and Mg[3:0] total 18-bit, D[13] is the MSB, Mg[0] is the LSB
CRC polynomials: X^6+X+1, MSB steam in first.

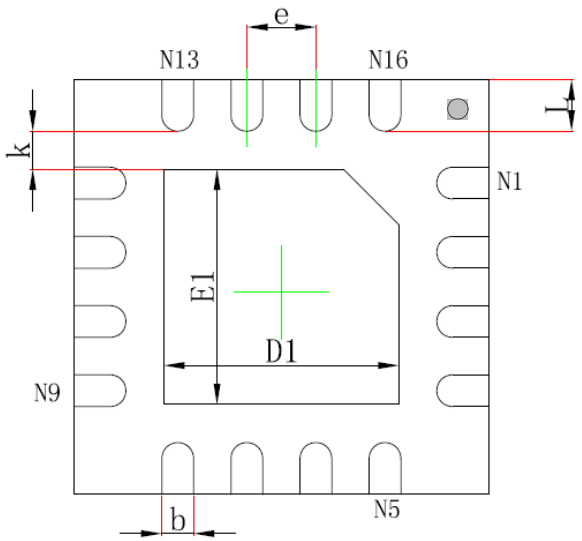
7. Mechanical Angle Direction



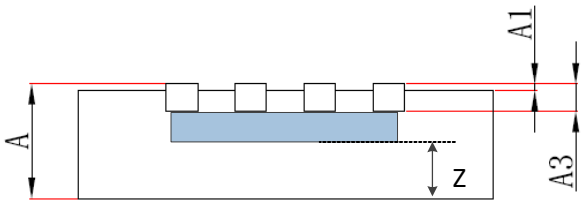
8. Package Information



Top View



Bottom View



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	1.600	1.800	0.063	0.071
k	0.275REF		0.011REF	
b	0.180	0.300	0.007	0.012
e	0.500REF		0.020REF	
L	0.300	0.500	0.012	0.020
Z	0.450	0.650	0.018	0.026

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10. Revision History

Revision Number	Date	Comments
1.0	2020.06	Initial Release
1.1	2021.03	Update PWM Clock Duration