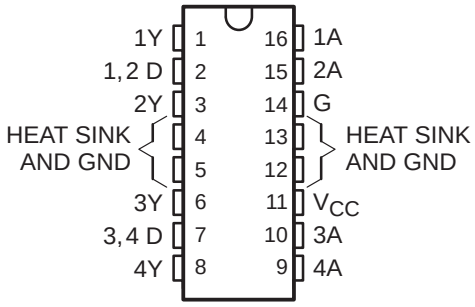
SLRS019B – DECEMBER 1986 – REVISED SEPTEMBER 2000

- **Saturating Outputs With Low On-State Resistance**
- **High-Impedance Inputs Compatible With CMOS and TTL Levels**
- **Very Low Standby Power . . . 21 mW Max**
- **High-Voltage Outputs . . . 70 V Min**
- **No Power-Up or Power-Down Output Glitch**
- **No Latch-Up Within Recommended Operating Conditions**
- **Output-Clamp Diodes for Transient Suppression**
- **Packaged in 2-W Power, Thermally Enhanced Plastic DIP**

NE PACKAGE
(TOP VIEW)



description

The SN75437A quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. This device features four inverting open-collector outputs with a common-enable (G) input that, when taken low, disables all four outputs. The envelope of 1-V characteristics exceeds the specifications sufficiently to avoid high-current latch-up. Applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand devices.

The SN75437A is characterized for operation over the free-air temperature range of 0°C to 70°C.

FUNCTION TABLE
(each NAND driver)

INPUTS		OUTPUT
A	G	Y
H	H	L
L	X	H
X	L	H

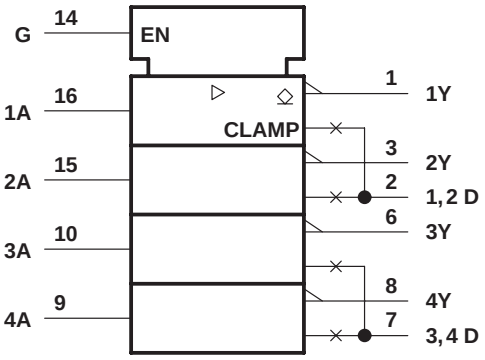
H = high level, L = low level,
X = irrelevant

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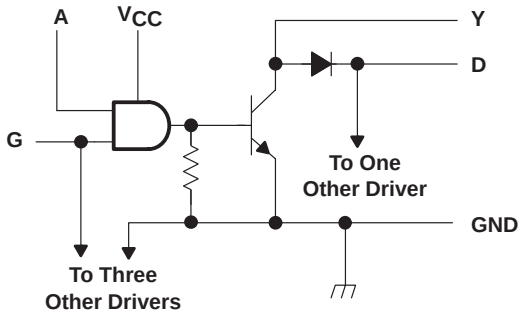
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logic diagram (positive logic)†

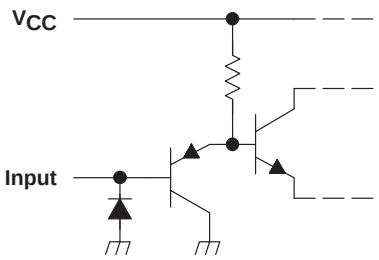


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

logic diagram (positive logic, each driver)



equivalent schematic of each input



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 30 V
Output current (see Note 1) . . . . . 0.75 A
Output clamp-diode current, I_{OK} . . . . . 1.25 A
Output voltage, V_O (off state) . . . . . 70 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 2075 mW
Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

NOTES: 1. All four sections of these circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
2. For operation above 25°C free-air temperature, derate linearly to 1328 mW at 70°C at the rate of 16.6 mW/°C.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Output supply voltage in inductive switching circuit (see Figure 2), V_S			35	V
Output current, I_O			0.5	A
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

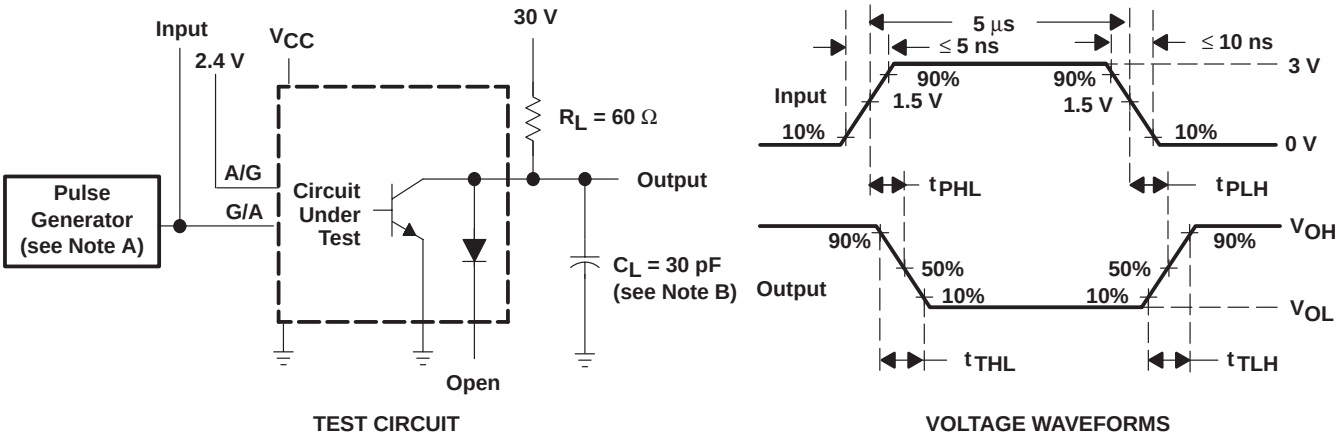
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = –12 mA		–0.9	–1.5	V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V	I_{OL} = 250 mA		0.14	0.25	V
			I_{OL} = 500 mA		0.28	0.5	
$V_{R(K)}$	Output clamp-diode reverse voltage	V_{CC} = 4.75 V,	I_R = 100 μA	70	100		V
$V_{F(K)}$	Output clamp-diode forward voltage	I_F = 500 mA			1	1.6	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V		1	100	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.25 V		0.1	10	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.8 V		–0.25	–10	μA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 0		1	4	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 5 V		45	65	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

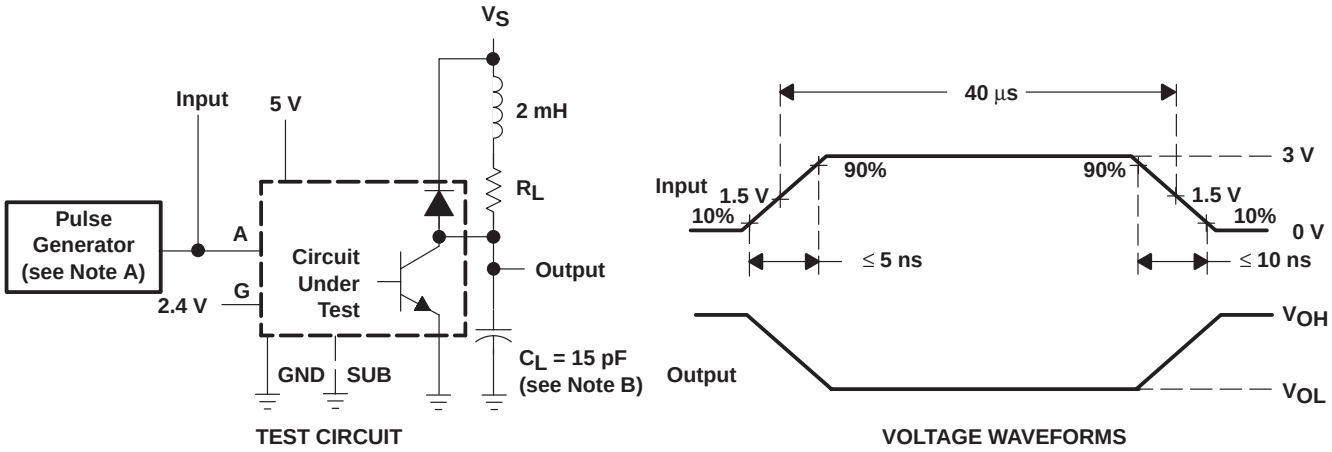
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1	R_L = 60 Ω,		1950	5000	ns
t_{PHL}	Propagation delay time, high-to-low-level output				150	500	ns
t_{TLH}	Transition time, low-to-high-level output				40		ns
t_{THL}	Transition time, high-to-low-level output				36		ns
V_{OH}	High-level output voltage after switching	V_S = 35 V, R_L = 70 Ω,	I_O ≈ 500 mA, See Figure 2	V_S–10			mV

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Latch-Up Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75437ANE	Active	Production	PDIP (NE) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75437ANE
SN75437ANE.A	Active	Production	PDIP (NE) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75437ANE
SN75437ANEE4	Active	Production	PDIP (NE) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75437ANE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

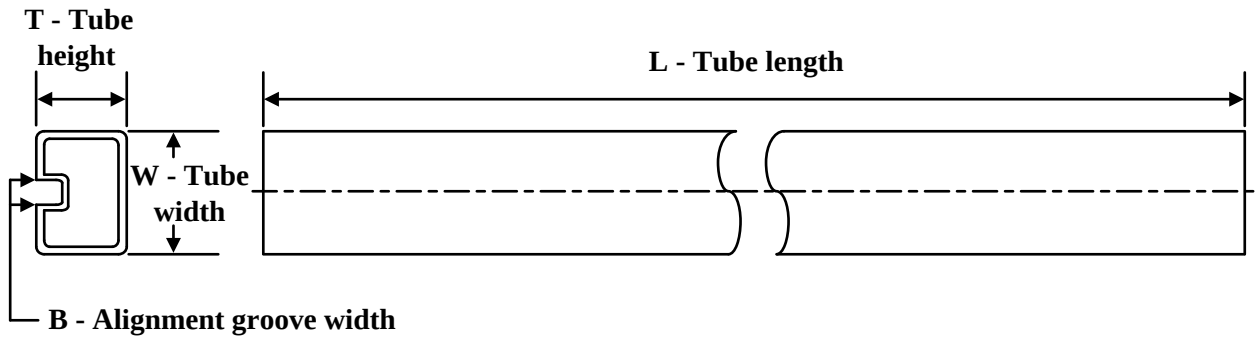
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



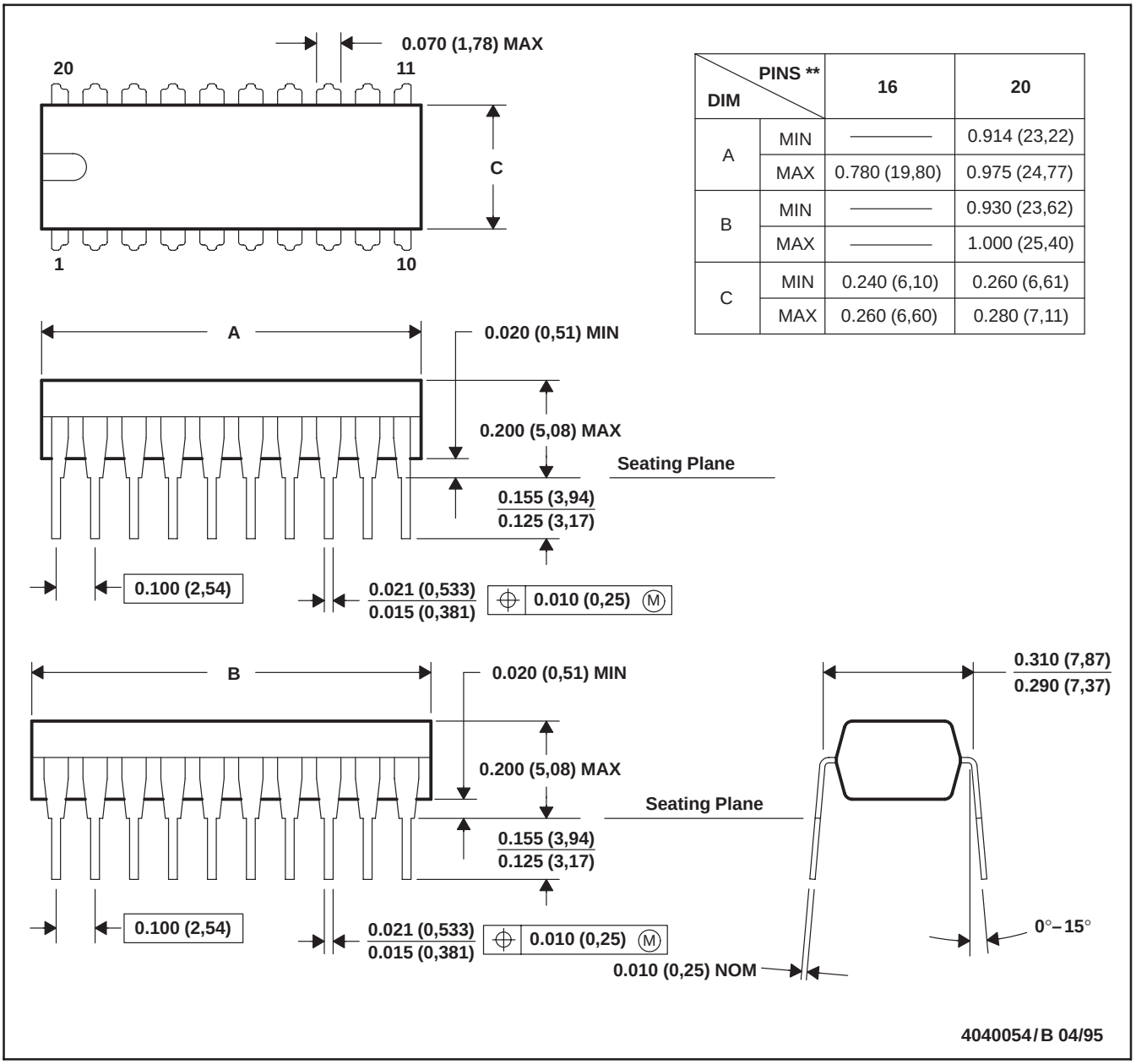
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75437ANE	NE	PDIP	16	25	506	13.97	11230	4.32
SN75437ANE.A	NE	PDIP	16	25	506	13.97	11230	4.32
SN75437ANEE4	NE	PDIP	16	25	506	13.97	11230	4.32

MPDI003 – OCTOBER 1994

NE (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

20 PIN SHOWN



DIM \ PINS **		16	20
A	MIN	———	0.914 (23,22)
	MAX	0.780 (19,80)	0.975 (24,77)
B	MIN	———	0.930 (23,62)
	MAX	———	1.000 (25,40)
C	MIN	0.240 (6,10)	0.260 (6,61)
	MAX	0.260 (6,60)	0.280 (7,11)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (16 pin only)

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